高速串行测试方案介绍

泰克华南区技术支持工程师  余岚
High-Speed Serial Data Test Solutions

- Design
- Verification
- Compliance Test

PCI Express
Serial ATA
SuperSpeed USB
ddr3
GbE DisplayPort
HDMI
MHL...

Transmitter Testing
System Integration
Digital Validation & Debug
Receiver Test Margin Testing
Arbitrary Waveform Generator
Real-time Scopes
Logic Analyzers
Interconnect Test
Compliance Test
Sampling Scopes
Compliance Test Software
Probing Fixtures
Storage Timelines and Solutions Development

<table>
<thead>
<tr>
<th>Year</th>
<th>Gen 2 - Silicon Phase</th>
<th>Gen 3 - Silicon Phase</th>
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<tbody>
<tr>
<td>2008</td>
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**6G Integration Phase**
- Product Development
- SATA I/O Unified Test Definition 1.4
- First official testing of Gen3 products in June 2009

**6G Deployment Phase**
- Commercial Gen3 product deployment.

**8G SATA-Express Integration Phase**
- S3 First Spec IOL SAS (12) Interop
- Draft Spec IOL SAS (12) Interop
- S3 First Spec IOL SAS (12) Interop

**8G SATA-Express Deployment Phase**
- 8G (Spec 3.2) SATA-Express Deployment Phase

**Gen 2 - Silicon Phase**
- SCSI Trade Association Plugfest (UNH IOL)
- STA test specification of SAS released.

**Gen 3 (12Gb/Sec) - Silicon Phase**
- Commercial product deployment.
**SATA UTD 1.4 TSG/PHY/OOB Measurements**

<table>
<thead>
<tr>
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<th>Test Name</th>
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<td>Informative-di/dt Measurement</td>
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<td>00B04-COMINIT_RESET Transmit Gap Length</td>
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<td>00B05-COMWAKE Transmit Gap Length</td>
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<td>00B07-COMINIT Gap Detection Windows</td>
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<td>TSG02-Rise-Fall Time</td>
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<td>TSG06-Amplitude Imbalance</td>
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<td>TSG09-TJ at Connector, Clock to Data, IBAUD-500</td>
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<td>TSG10-DJ at Connector, Clock to Data, IBAUD-500</td>
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<td>TSG11-TJ at Connector, Clock to Data, IBAUD-500</td>
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<td>TSG12-DJ at Connector, Clock to Data, IBAUD-500</td>
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<td>TSG13-Transmit Jitter</td>
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<td>TSG14-TX Maximum Differential Voltage Amplitude</td>
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<td>TSG15-TX Minimum Differential Voltage Amplitude</td>
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<td>TSG16-Tx AC Common Mode Voltage</td>
</tr>
</tbody>
</table>

- Different test program and degrees of regression testing user selectable.
- Debug and diagnostic tools (Informative measurements)
- Updated SATA Gen3 measurements
  - New OOB patterns
  - TSG ECN additions
Select Standard
- Serial ATA
- SAS

Select Device
- Drive

Select Test Suite
- PHY-TSG-OOB
- Rx-Tx

Version
SAS 2.0

Drive: PHY-TSG-OOB SAS 2.0

Test Name
- Test 5.2.4 - TX SSC DFUT (Informative)
- Test 5.3.1 - TX Physical Link Rate Long Term Stability
- Test 5.3.2 - TX Common Mode RMS Voltage Limit
- Test 5.3.3 - TX Common Mode Spectrum
- Test 5.3.4 - TX Peak-to-Peak Voltage
- Test 5.3.5 - TX VMA and EQ
- Test 5.3.6 - TX Rise and Fall Times
- Test 5.3.7 - TX Random Jitter (RJ)
- Test 5.3.8 - TX Total Jitter (TJ)
- Test 5.3.9 - TX Waveform Distortion Penalty (WDP)
SATA/SAS TSG/PHY/OOB test connection
# SATA/SAS: Test Report

## Test Details

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Pattern Name</th>
<th>Interface Speed</th>
<th>Measurement Details</th>
<th>Low Limit</th>
<th>Measured Value</th>
<th>High Limit</th>
<th>Margin</th>
<th>Units</th>
<th>Test Result</th>
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<td>-NA-</td>
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<td>-NA-</td>
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<td>SSC Modulation Frequency</td>
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<td>0.3</td>
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<td>HFTP</td>
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<td>Min SSC Modulation Frequency</td>
<td>&gt;= 30</td>
<td>29.9992</td>
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<td>Deviation symmetry</td>
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<td>dlt/dt</td>
<td>&gt;= -850</td>
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<td>Mean Period</td>
<td>&gt; -100</td>
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<td>CJTPat-Gen 2</td>
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<td>Common-mode RMS voltage at IT_SAS 2.0</td>
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<td>42.9227</td>
<td>&lt; 30</td>
<td>12.9227</td>
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<td>Test 5.3.3-TX Common Mode Spectrum</td>
<td>CJTPat-Gen 2</td>
<td>8.0 Gbps</td>
<td>Common-mode spectrum (dBm) at 100MHz_SAS 2.0</td>
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<td>-33.5689</td>
<td>&lt; 12.7</td>
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<td>CJTPat-Gen 2</td>
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<td>Common-mode spectrum (dBm) at first harmonic_SAS 2.0</td>
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<td>CJTPat-Gen 2</td>
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<td>Common-mode spectrum (dBm) at second harmonic_SAS 2.0</td>
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<td>39.2588</td>
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<td>Test 5.3.4-TX Peak-to-Peak Voltage</td>
<td>D30.3-Gen 2</td>
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<td>Peak to peak voltage (mVppd)_SAS 2.0</td>
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<td>D10.2</td>
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<td>Fall time in ps</td>
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<td>D24.3-Gen 2</td>
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<td>RJ before CIC</td>
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SAS-3 12Gbps PHY Transmitter Solution – Option SAS3

- Support per SAS-3 Spec 23Apr2012

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<th>Tests</th>
<th>Base Measurement</th>
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<td>TX Peak to Peak Voltage</td>
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<td>TX Rise/Fall Time</td>
<td>DPOJET</td>
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<td>TX Total Jitter</td>
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<td>TX Physical Link Rate Long Term Stability</td>
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<td>TX Common Mode Spectrum</td>
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<tr>
<td>TX VMA and EQ</td>
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<td>TX SAS Eye Opening</td>
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<td>Pre Cursor Equalization</td>
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<tr>
<td>Post Cursor Equalization</td>
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* SAS3 Eye measurement to be added
Mini-SAS HD Plug Test Adapters

- Color Coded and Imprinted Markings
  (Large Colored = Channel Number)
  (Short White = Transmitter Side)
  (Short Red = Positive Polarity)

- High-Performance Mini-SAS HD Plug Connector Configuration

- 8 Position Low-Speed Connector

- Small Form-Factor Housing (allows for 1x2 4X testing when using left-hand version TPA)

- 16 SMAs for High-Speed Testing
Bandwidth Considerations
SAS 12G NRZ Power Spectrum

![SAS 12G NRZ Power Spectrum Diagram]

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<tr>
<th>Marker</th>
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<th>Δ Frequency</th>
<th>Δ Time</th>
<th>Spectrum</th>
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<td>11.9999973 GHz</td>
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<td>-1.52 dB</td>
<td>-66.74 dBm</td>
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<td>M4</td>
<td>33.000001575 GHz</td>
<td>20.949995286 GHz</td>
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<td>-51.07 dBm</td>
<td>6.61 dB</td>
<td>-66.28 dBm</td>
<td>2.67 dB</td>
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12G PRBS from BERT (20ps 20-80% Tr)

- **18 GHz**
  - (3rd harmonic)

- **24 GHz**
  - (4th harmonic)

- **33 GHz**
  - (~5th harmonic)
Thunderbolt Overview

- High Speed Data Bus for PC’s
  - Brought to market by Intel/Apple in 2011
  - Interoperable with DisplayPort

- Thunderbolt signaling is dual NRZ (64/66b Encoded)
  - 10.3125 Gb/s data rate
  - It utilizes SFP+ technology with 2 diff Tx and Rx pairs.
Thunderbolt Transmitter Test Overview

- All measurements are near end with Fixtures fully de-embed.
- Requires DisplayPort 1.2 conformance testing

### Source Test Suite

- PHY1.1 – Transition Timing
- PHY1.2 – Intra-Pair Skew
- PHY1.3 – AC Common Mode RMS
- PHY1.4 – AC Common Mode Peak
- PHY1.5 – Eye Height
- PHY1.6 – Eye Width
- PHY1.7 – Max Differential Voltage
- PHY1.8 – Total Jitter at 10-12 BER
- PHY1.9 – Unit Interval
- PHY1.10 – SSC Modulation Frequency

### DUT Configuration

- **1. Bit Rates:** (DP1.2) + 10.3125Gb/sec
- **2. Patterns:** 8 1’s 8 0’s, PRBS-9, PRBS-11 and PRBS-31
- **3. SSC (Spread Spectrum):** On/Off
Thunderbolt Transmitter Testing
Fully supported in Tektronix’s current solutions
Thunderbolt Test Connectivity

- The Digital Port Micro is responsible for Test Pattern and general state control, as well as error polling in the DUT.

Thunderbolt Fixture Micro Controller, UART, and Power Testing Board:

Available directly from Wilder Technologies at part number.. 640-0503-000 (TBT-TPA-UH) USB to PC Connection for Control

8 Low Speed Signal lines for Control and Power Testing (10 – Position Connector)

Input Power Connectors

4 High Speed Thunderbolt Diff Pairs

Thunderbolt Plug Conn

USB to PC Connection for Control

The Digital Port Micro is responsible for Test Pattern and general state control, as well as error polling in the DUT.
10GBASE-T - Overview

- 10GBASE-T provides 10 gigabit/second connections over unshielded or shielded twisted pair cables, over distances up to 100 m. 2.5Gbps per lane (A, B, C & D)
- Baseband 16-level PAM signaling with a modulation rate of 800 Msymbols per second is used on each of the wire pairs.
- Supports full duplex operation only
- Compatibility of Auto Negotiation enabled to also operate 10/100/1000 BASE-T
- Supports a BER of less than or equal to 10E-12 on all supported distances and Classes
- Provides a cost advantage over fiber
Maximum Output Droop

- **Purpose** - To verify that the transmitter output level does not decay faster than the maximum specified rate.

- The resulting magnitude of both the positive and negative droop shall be less than 10%.

- Flexibility to test beyond compliance – XGbT provides the flexibility to perform testing beyond what is specified in IEEE standard 802.3an-2006. It helps users to analyze their PHY in addition to compliance tests.

- Configure the DUT for Test Mode 6 operation

- IEEE standard 802.3an-2006, sub clause 55.5.3.1
XGbT - Report

- TEKEXP software provides summary-reporting capability of all lanes in .mht (HTML) format with pass/fail status.
- A detailed report of each lane’s performance including test configuration details, waveform plots, and margin analysis is also produced by XGbT providing more insight into compliance efforts underneath the XGbT standard.
- Report also provides additional details like calibration status, scope model, probe model, software version etc.
TF-XGbT Test Fixture

- The XGbT test fixture provides easy access to the 10GBASE-T Electrical signals to perform conformance testing and device characterization as described in of IEEE 802.3an-2006 sub-clause 55.5.3 & 55.8.2.1. This fixture is used with the Tektronix’s XGbT- 10GBASE-T Automation Solution to provide fast and accurate design debugging and validation. XGbT fixture covers all seven measurements including Jitter Slave and MDI Return Loss.
10G-KR  Typical Backplane Ethernet

Transmitter

1. Chip and package

2. Package to board via

3. Daughter card trace

Backplane

4. Daughter card to connector via

5. Connector

6. Connector to backplane via

Receiver
10G-KR自动化测试软件

Test Description

The 10GBASE-KR signaling speed shall be 10.3125 Gb/s ± 100 ppm.
Testing connection for 10G-KR
# Tektronix SFP-TX – Automation & DPOJET Option

<table>
<thead>
<tr>
<th>SL No.</th>
<th>Measurements</th>
<th>Signal Type Recommended</th>
<th>Min</th>
<th>Target</th>
<th>Max</th>
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<td>Single Ended Output Voltage Range</td>
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<td>-0.3</td>
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<td>V</td>
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<td>PRBS31</td>
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<td>mV(RMS)</td>
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<td>3</td>
<td>Crosstalk source rise/fall time (20%-80%) (Tr, Tf)</td>
<td>8180</td>
<td>34</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Crosstalk source amplitude (p-p differential)</td>
<td>8180</td>
<td>1000</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Signal rise/fall time (20%-80%) (Tr, Tf)</td>
<td>8180</td>
<td>34</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Total Jitter (p-p) (Tj)</td>
<td>PRBS31</td>
<td>0.28</td>
<td>UI(p-p)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Data Dependent Jitter (p-p) (DDJ)</td>
<td>PRBS9</td>
<td>0.1</td>
<td>UI(p-p)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Data Dependent Pulse Width Shrinkage (p-p) (DDPWS)</td>
<td>PRBS9</td>
<td>0.055</td>
<td>UI(p-p)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Uncorrelated Jitter (RMS) (UJ)</td>
<td>PRBS9</td>
<td>0.023</td>
<td>UI(p-p)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Transmitter Qsq</td>
<td>8180</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Eye mask hit ratio (Mask hit ratio of 5×10⁻⁵)</td>
<td>PRBS31</td>
<td>X1=0.12UI, X2=0.33UI, Y1=95mV, Y2=350mV</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Host Transmitter output specifications for Cu (SFP+ host supporting direct:

<table>
<thead>
<tr>
<th>SL No.</th>
<th>Measurements</th>
<th>Voltage Modulation Amplitude (p-p)</th>
<th>8180</th>
<th>300</th>
<th>mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>Transmitter Qsq Output AC Common Mode voltage</td>
<td>8180</td>
<td>63.1</td>
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<tr>
<td>13</td>
<td>Output AC Common Mode Voltage</td>
<td>PRBS31</td>
<td>12</td>
<td>mV(RMS)</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Host Output TWDPc</td>
<td>PRBS9</td>
<td>10.7</td>
<td>dBe</td>
<td></td>
</tr>
</tbody>
</table>
SFP test connection
SFP Eye Mask hit ratio : less than 5E10-5
Tektronix Solutions for PCI Express 3.0 Measurements

- Introducing option PCE3 for DSA/DPO/MSO70K Scopes
- Support for NEW Base Spec measurements
- Support for CEM Specification
- Supports all versions of PCI Express
PCIE Dual-Port TX Measurement Example for System

100 MHz Reference Clock

PCI Express® 3.0 Compliance Data

All other lanes are terminated with 50 Ohm load
PCIE TX Measurement Example for Add-in Card

[Image of a Tektronix oscilloscope showing a waveform, and a close-up of a circuit board with labeled components such as CBB Power Switch, Compliance Mode Toggle Push-button, Add-in-card Power Reset, PCIE Connector, Add-in-card TX, and Add-in-card RX.]
RX Measurement Example for Host

ATX Power Supply

DUT

Tx out(Rear)

Tx (Out)

SI Combiner

From BERTScope SI o/p (rear)

12"

Power Repeater 3.3V

72"
USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate

- Low Frequency Periodic Signaling (LFPS)
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod

- SSC
  - Modulation Rate
  - Deviation
Transmitter Compliance Test Setup

- USB-IF or Tektronix fixtures can be used
  - Test configuration is the same
- Compliance channel and 3 meter cable are emulated in software
  - Compliance sparameters were used to create channel filters
  - CTLE is applied to open the eye, then compliance measurements are taken
  - Compliance channel and Cable are applied in software, resulting in a closed eye
USB 3.0 Compliance and Automation

- Complete Automation of USB 3.0 Measurements with TekExpress
- No need to learn technology specific software applications - TekExpress is a Common Framework from Serial Applications including SATA, USB, DisplayPort, HDMI, and Ethernet
- TekExpress utilizes DPOJET USB 3.0 Specific algorithms making it easy to move from compliance to DPOJET for debug
HDMI 测试方案-源端
HDMI 测试方案-接收端(TV/Monitor)
HDMI 1.4 HEAC Solution Configuration

Tx Test Setup

Rx Test Setup
HEAC Software

TekExpress HEAC Automated Solution (Evaluation Version) (Untitled)*

Select Device
- HEAC-Transmitter
- HEAC-Receiver

Select Test Suite
- Differential-Rx
- CommonMode-Rx
- SingleMode-Rx

Version
- CTS 1.4

DUT IP Address
- 255.255.255.255
- Auto Detect MAC Address

HEAC-Receiver : Differential-Rx CTS 1.4

Select
- Receiver Performance - Nominal Response
- 5.16 Receiver Performance - Amplitude
- 5.16 Receiver Performance - Clock Frequency
- 5.16 Receiver Performance - Common mode
- 5.16 Receiver Performance - Signal Source Impedance
- 5.16 Receiver Performance - Worst Case Cable

Test Description
This optional test verifies the receiver capability to respond to nominal amplitude, clock frequency and

Configure
Show Schematic
Select All
Deselect All
MHL Compliance Software for Automated Tx Tests: Option MHD

MHL Physical Layer Solution: MHL Transmitter: Spec 1.0

- MHL Clock
  - 3.1.1.7 Common-mode Rise and Fall Times-TR_CM, TF_CM
  - 3.1.1.10 MHL Clock Duty Cycle 24-Bit or Packed Pixel Mode
  - 3.1.1.11 MHL Clock Jitter

- MHL Data
  - 3.1.1.2 Single-ended High Level Voltage-VSE_HIGH
  - 3.1.1.3 Single-ended Low Level Voltages-VSE_LOW
  - 3.1.1.4 Differential Output Swing Voltage-VDF_SWINING
  - 3.1.1.5 Common-mode Output Swing Voltage-V_CMSWING
  - 3.1.1.6 Differential Rise and Fall Times-TR_DF, TF_DF
  - 3.1.1.8 Differential Intra-Pair Skew-TSKEW_DF
  - 3.1.1.12 MHL Data Eye Diagram

Test Description
Select individual measurement to view its description

Configure
Tektronix MHL Tx Setup

MHL Differential and CM Test Setup
7 tests

Single Ended and Intra Pair Skew Test Setup
3 Tests

Also same setup is used for MHL Protocol Testing

** C-Bus Sink and Source Board is needed for hand shaking and is available from Simplay Labs
Wilder Fixtures: Tektronix MHL Source Testing Setup

Tektronix P7313 SMA Differential Probe
Tektronix P7313 SMA Differential Probe

640-0452-000 MHL-TPA-TT

Tektronix P7240 Common Mode Clock

640-0453-000 MHL-TPA-P-WOSO

VBus/CBUS Receptacle
VBus/CBUS Jumpers

uUSB Plug

uUSB Receptacle
Tektronix MHL Solution Setup: Simple and Easy Sink and Dongle Min/Max Testing -2

Setup based on Direct Synthesis Capability of AWG7122C Series

AWG Sink Min/Max Signal (CM, SE and Diff) Verification Using Real Time Oscilloscope

Test Setup for Sink Min/Max Tests

AWG Dongle Min/Max Signal (CM, SE and Diff) Verification Using Real Time Oscilloscope

Test Setup for Dongle Min/Max Tests
Tektronix MHL Protocol Analyzer

![Tektronix MHL Protocol Analyzer Interface](image-url)
MIPI标准概述
移动终端方框图实例

- 显示单元
- CMOS图像传感器
- 摄像机
- 扬声器
- 耳机
- FM无线电
- 麦克风

基带IC
- 应用处理器
- Tx/Rx处理器
- 存储器接口
- 存储器（内存）
- 存储器（SD卡）

DSI = 显示器串行接口
CSI = 摄像机串行接口
SLIMbus = 串行低功率芯片间媒体总线

定义
- CSI = 摄像机串行接口
- DSI = 显示器串行接口
- SLIMbus = 串行低功率芯片间媒体总线

空中接口（如WiMax）
RF IC
- RF接口，不受MIPI标准影响
RF IC
(WCDMA, GSM, WLAN, FM, 蓝牙, GPS, MobileTV, 等等)

显示单元

CMOS图像传感器

摄像机

扬声器

耳机

FM无线电

麦克风

存储器（内存）

存储器（SD卡）
D-PHY Tx测试解决方案 – 续

- **示波器**
  - 推荐: DPO7354或DPO/DSA/MSO70404/B
    - 用来测量规范+/−5%误差范围内的上升时间(150ps)
    - 如果不考虑上升时间的测试，可以使用DPO7254

- **探头**
  - 探头考虑因素
    - 同时测量单端性能和差分性能
    - 动态范围必须>1.2V
    - 探头衰减要达到最小
      - 1X最好，2.5X或5X也行
  - 推荐:
    - DPO7000采用四只TAP3500；MSO/DPO/DSA70000/B采用四只P7240
    - (Ch1: D+), (Ch2: D-), (Ch3: Clk+), (Ch4: Clk-)
    - TAP2500也适合低数据速率的DUT
  - 也可以使用:
    - 焊接式探头
      - DPO7000采用TDP3500，70000系列采用P73xx
        - (Ch1: D+, Gnd), (Ch2: D-, Gnd), (Ch3: Clk+ &Clk-)
New Opt.D-PHYTX

  - TekExpress option for Fully-Automated testing
  - Automation similar to Opt.USB-TX
  - Provides Conformance and Characterization Testing
  - Based on D-PHY Base Spec v1.0 and UNH’s Conformance Test Suite v0.98.
  - Runs on DPO7000, DPO/DSA/MSO70000/B Series oscilloscopes

- Opt.TEKEXP is Pre-Requisite

- Differentiation
  - Un-parallel Automation (Auto-Cursors/ Regions)
  - For Conformance testing to Latest CTS (v0.98)
  - Based on Latest Base spec (v1.0)

- Value proposition
  - Custom-limits/ Limits-Editing on the fly
  - Test Reports
    - Zoom-in waveform captures at the Cursors/ Regions
    - Pass/Fail Summary with Margin details
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
    - i.e. unlike Agilent 4G scope at entry-level
D-PHY Rx : Test Solution Overview
Simple, Quick, Easy and Re-usable

- **100% Coverage to Rx CTS**
  - Meets all the requirements in UNH-IOL CTS document (v0.98)

- **Quick and Easy setup**
  - No complex VXI system, just stand alone instruments, and a probe.

- **Cost effective solution**
  - 70% Lower list price vs Competition

- **Re-usable for Protocol tests**
  - PG3A is the Only 4 channel solution for CSI & DSI test

- **PG3A Pattern Generator**
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver

- **AWG7082C Generator**
  - Adds jitter and interference to the D-PHY signals

---

**Recommended Setup**

- **PGRemote Software***
- **AWG7082C**
- **PG3ACAB***
- **P331 Probe***
- **D-PHY Coupler**
- **DUT**

---

*These Moving Pixel products are available as Tektronix part number
**Tektronix part number not available yet. Expected Soon.

Simultaneous Acquisition

- Probe using Analog, Digital or Mixed Channels
- Simultaneous probing of DSI & CSI using MSO channels
- Working on multi-lane support, using high performance MSO digital channels
- Supported on all 7KC, 70KC and MSO70K scopes. *(Win7-OS only)*
  - Option key bit #25
- Software installed as part of TekScope firmware v6.1.2.4 or later.
  - Browse to TekScope Menu --> Vertical --> Bus Setup --> Select Bus Type as Serial--> Select MIPI DSI or CSI from the drop down list.

Probe using Mixed Channels

Analog Clock, Digital Data

Digital Clock, Analog Data
Memory Technology – Quick Overview

- **DRAM** - dominant memory technology
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMMs
  - Embedded systems
    - Cell phones, printers, cars
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR3 now available at 1600 (1.6Gb/s) data rates
    - DDR3 2000 emerging soon (overclocked)

- **DRAM variants**
  - LPDDR – Low Power DDR
    - Power savings for portable computing
  - GDDR – Graphic DDR
    - Optimized for Speed - faster access
Installation Process

- Socket on Memory Component Interposer
- Memory Chip
- Memory Component Interposer
- Memory socket on target with guide posts
- Board under test
BGA Chip Interposer for Oscilloscopes

- Available in socket and solder-in versions
  - Socket design allows for multiple chip exchanges
  - Solder-in best for single use
- Recommended probes: P7500 Series
  - P7504, P7506, P7508, P7513A
  - 020-3022-00 TriMode solder tips for Nexus Interposer
Automated Test Setup

Step #1

Select DDR Generation

Select DDR Rate

Step #2

Choose measurements (Read / Write / CLK / Addr & Command)
Effective Reporting / Archiving
Automatically isolate & mark all read or write bursts

- Easily Identify, mark & measure all Read / Write bursts
  - Scroll through marked reads / writes across the entire waveform record
  - Measurements performed on ALL reads/writes
Visual Trigger and Serial Decode

- Next generation designs have less margin and additional analysis must be done to pinpoint in on pattern dependent issues
  - **NEW!** Visual Trigger qualifies hard to define trigger events
    - 8 customizable shapes for capture of real signal behaviors

- Electrical and Logic layer are merging and requires simultaneous analog and protocol views
  - **NEW!** 8b/10b Serial Decode
    - Trigger or Search on decoded traffic
    - Compare to analog views to speed up time to answer
Triggering Techniques for Debugging DRAM

- **Challenge: Dual-Rank System**
  - Need to Isolate & Measure a Single Rank
  - Difficult to isolate data bursts from one rank only
Triggering Techniques for Debugging DRAM

- ‘Visual’ Trigger Used to Qualify One Rank
  - Visual area (“keep-out” region) used to exclude low-amplitude signals
  - Eliminates lower-amplitude data bursts from rank 2

“After” gating with visual trigger
High-Speed Serial Data Test Solutions…

Design > Verification > Compliance Test

- PCI EXPRESS
- SERIAL ATA
- USB
- DDR3
- GbE DisplayPort
- HDMI
- MHL...

Transmitter Testing
System Integration
Digital Validation & Debug
Receiver Test
Margin Testing
Transmitter Testing

Interconnect Test

Real-time Scopes
Sampling Scopes
Probing Fixtures
Arbitrary Waveform Generator
Compliance Test Software

Logic Analyzers
DPO/DSA70000D 系列

<table>
<thead>
<tr>
<th>型号</th>
<th>带宽</th>
<th>采样率</th>
<th>存储深度 (最大)</th>
<th>上升时间</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPO/DSA73304D</td>
<td>33GHz(2Ch)</td>
<td>100GS/s(2Ch)</td>
<td>250Mb</td>
<td>9ps</td>
</tr>
<tr>
<td></td>
<td>23GHz(4Ch)</td>
<td>50GS/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DPO/DSA73254D</td>
<td>25GHz(2Ch)</td>
<td>100GS/s(2Ch)</td>
<td>250Mb</td>
<td>12ps</td>
</tr>
<tr>
<td></td>
<td>23GHz(4Ch)</td>
<td>50GS/s</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. 10 TS/s等效采样率
2. 输入灵敏度达到 6.25mV/div
3. 低本底噪声和抖动
4. 大于 300,000 wfms/sec 的最高波形捕获率
### DPO/DSA70000C 系列

<table>
<thead>
<tr>
<th>型号</th>
<th>带宽</th>
<th>采样率</th>
<th>存储深度(标配)</th>
<th>上升时间</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPO/DSA72004C</td>
<td>20GHz(2Ch)</td>
<td>100GS/s(2Ch)</td>
<td>10Mb/31.25Mb</td>
<td>14ps</td>
</tr>
<tr>
<td></td>
<td>20GHz(4Ch)</td>
<td>50GS/s(4Ch)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DPO/DSA71604C</td>
<td>16GHz(2Ch)</td>
<td>100GS/s(2Ch)</td>
<td>10Mb/31.25Mb</td>
<td>17ps</td>
</tr>
<tr>
<td></td>
<td>16GHz(4Ch)</td>
<td>50GS/s(4Ch)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DPO/DSA71254C</td>
<td>12.5GHz(2Ch)</td>
<td>100GS/s(2Ch)</td>
<td>10Mb/31.25Mb</td>
<td>22ps</td>
</tr>
<tr>
<td></td>
<td>12.5GHz(4Ch)</td>
<td>50GS/s(4Ch)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DPO/DSA70804C</td>
<td>8GHz(2Ch)</td>
<td>25GS/s(2Ch)</td>
<td>10Mb/31.25Mb</td>
<td>34ps</td>
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<tr>
<td></td>
<td>8GHz(4Ch)</td>
<td>25GS/s(4Ch)</td>
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<td></td>
</tr>
<tr>
<td>DPO/DSA70604C</td>
<td>6GHz(2Ch)</td>
<td>25GS/s(2Ch)</td>
<td>10Mb/31.25Mb</td>
<td>45ps</td>
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<tr>
<td></td>
<td>6GHz(4Ch)</td>
<td>25GS/s(4Ch)</td>
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</tr>
<tr>
<td>DPO/DSA70404C</td>
<td>4GHz(2Ch)</td>
<td>25GS/s(2Ch)</td>
<td>10Mb/31.25Mb</td>
<td>68ps</td>
</tr>
<tr>
<td></td>
<td>4GHz(4Ch)</td>
<td>25GS/s(4Ch)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
MSO70000C 高性能混合信号示波器
业内领先的配有高性能数字通道的实时示波器

- 20G带宽模拟通道
  4个通道

- 80ps 数字定时分辨率
- 20 ps 模拟定时分辨率

- 深存储
  对于模拟和数字通道全部为250M/ch

- iCapture™ 同时进行模拟数字时间相关调试

- 16数字通道
  连同4个模拟通道组成的采集系统

- 新数字逻辑探头
  提供高信号保证度以及最小的负载

- 事件触发能力
  隔离定位偶发的故障

- 集成了并行总线、I2C、SPI解码功能
<table>
<thead>
<tr>
<th>型号</th>
<th>带宽</th>
<th>采样率</th>
<th>存储深度(标配)</th>
<th>波形捕获率</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPO7054C</td>
<td>500MHz</td>
<td>10GS/s(1Ch) 5GS/s (2Ch) 2.5GS/s (2Ch)</td>
<td>10Mb/20Mb/40Mb</td>
<td>&gt;250,000</td>
</tr>
<tr>
<td>DPO7104C</td>
<td>1GHz</td>
<td>20GS/s(1Ch) 10GS/s (2Ch) 5GS/s (2Ch)</td>
<td>10Mb/20Mb/40Mb</td>
<td>&gt;250,000</td>
</tr>
<tr>
<td>DPO7254C</td>
<td>2.5GHz</td>
<td>40GS/s(1Ch) 20GS/s (2Ch) 10GS/s (2Ch)</td>
<td>10Mb/20Mb/40Mb</td>
<td>&gt;250,000</td>
</tr>
<tr>
<td>DPO7354C</td>
<td>3.5GHz</td>
<td>40GS/s(1Ch) 20GS/s (2Ch) 10GS/s (2Ch)</td>
<td>10Mb/20Mb/40Mb</td>
<td>&gt;250,000</td>
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# MSO/DPO5000系列示波器

<table>
<thead>
<tr>
<th></th>
<th>MSO5204 DPO5204</th>
<th>MSO5104 DPO5104</th>
<th>MSO5054 DPO5054</th>
<th>MSO5034 DPO5034</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>带宽</strong></td>
<td>2 GHz</td>
<td>1 GHz</td>
<td>500 MHz</td>
<td>350 MHz</td>
</tr>
<tr>
<td><strong>模拟通道</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>数字通道</strong></td>
<td>16（仅 MSO 型号）^1，带有新 P6616 16 通道数字探头</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>数字采样率</strong></td>
<td>500 MS/s 数字 Main，16.5 GS/s 数字 MagniVu™</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>模拟记录长度（最大/全部通道）</strong></td>
<td>可选：25M/12.5M</td>
<td>标配：12.5M；可选最大 40M</td>
<td>标配：12.5M；可选最大 40M</td>
<td>标配：12.5M；可选最大 40M</td>
</tr>
<tr>
<td><strong>数字记录长度</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>波形捕获率</strong></td>
<td>&gt; 250,000 个波形/秒</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>分段存储器</strong></td>
<td>FastFrame™</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>串行触发和解码</strong></td>
<td>可选：I2C, SPI, RS-232/422/485/UART, USB, CAN/LIN^2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>分析</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>标配模拟探头</strong></td>
<td>(4) TPP1000 – 1 GHz，3.9pf，10X 无源探头（1 和 2 GHz 型号）</td>
<td>(4) TPP0500 – 500 MHz，3.9pf，10X 无源探头（350 和 500 MHz 型号）</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>计算平台</strong></td>
<td>Intel Core2 Duo 处理器带 4GB RAM，运行 Windows 7 64 位操作系统</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>标配 I/O</strong></td>
<td>(6) USB 主机、USB 设备、LAN（LXI Class-C），视频输出、参考时钟输入、辅助（Aux）输出、音频、可移除硬盘驱动器</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>显示屏</strong></td>
<td>10.4 英寸 XGA 触摸屏</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

^1: DPO 型号可现场升级到 MSO 功能
^2: 通过 VNA 软件支持 CAN/LIN
^3: 1 GHz 和 2 GHz 型号可获得 DDR
MDO4000系列混合域示波器(数字,模拟,射频一体化)

- 多达21条通道
  支持复杂调试
- 内置频谱分析仪
- 时间相关的模拟、数字与RF

<table>
<thead>
<tr>
<th>型号</th>
<th>模拟通道</th>
<th>模拟带宽</th>
<th>数字通道</th>
<th>RF通道</th>
<th>RF频率范围</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDO4054-3</td>
<td>4</td>
<td>500 MHz</td>
<td>16</td>
<td>1</td>
<td>50 kHz – 3 GHz</td>
</tr>
<tr>
<td>MDO4054-6</td>
<td>4</td>
<td>500 MHz</td>
<td>16</td>
<td>1</td>
<td>50 kHz – 6 GHz</td>
</tr>
<tr>
<td>MDO4104-3</td>
<td>4</td>
<td>1 GHz</td>
<td>16</td>
<td>1</td>
<td>50 kHz – 3 GHz</td>
</tr>
<tr>
<td>MDO4104-6</td>
<td>4</td>
<td>1 GHz</td>
<td>16</td>
<td>1</td>
<td>50 kHz – 6 GHz</td>
</tr>
</tbody>
</table>
DSA8300 采样示波器

- 光信号测试
- 电信号测试
- 阻抗测试
- S参数测试

<table>
<thead>
<tr>
<th>DSA8300 / Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSA8300</td>
<td>Digital Signal Analyzer mainframe</td>
</tr>
<tr>
<td>Opt. ADTRIG</td>
<td>Add Advanced Trigger (required for JNB or JNB01)</td>
</tr>
<tr>
<td>Opt. JNB</td>
<td>Add 80SJNB Essentials</td>
</tr>
<tr>
<td>Opt. JNB01</td>
<td>Add 80SJNB Advanced</td>
</tr>
<tr>
<td>Opt JARB</td>
<td>Add 80SJARB (included in JNB &amp; JNB01)</td>
</tr>
<tr>
<td>Opt. ICMX</td>
<td>Add IConnect with Measurement Extractor</td>
</tr>
<tr>
<td>Opt. ICON</td>
<td>Add IConnect Signal Integrity Software</td>
</tr>
<tr>
<td>Opt. SPAR</td>
<td>Add IConnect S-parameter and Z-line</td>
</tr>
</tbody>
</table>
### Multi-mode, Broad Wavelength (750 - 1650 nm) Modules

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>80C07B</td>
<td>Supports rates to 2.7 Gb/s, high sensitivity, optional integrated clock recovery</td>
</tr>
<tr>
<td>80C08C</td>
<td>Supports all of the 8/10 Gb/s applications, high sensitivity, optional integrated clock recovery, optional Integrated CR</td>
</tr>
<tr>
<td><strong>80C12B</strong></td>
<td>Supports rates from 155 Mb/s – 11.3 Gb/s, high sensitivity - data pick-off for external CRU e.g. CR125A</td>
</tr>
<tr>
<td><strong>80C14</strong></td>
<td>Supports rates from 8.5 Gb/s – 14.063 Gb/s, high sensitivity – data pick-off for external CRU e.g. CR175A</td>
</tr>
</tbody>
</table>

### Single-mode, Long Wavelength (1100 - 1650nm) Modules

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>80C11</td>
<td>Optical bandwidth to 30GHz, supports 10Gbit/s up to 14G+ standards, optional Integrated CR</td>
</tr>
<tr>
<td>80C25GBE</td>
<td>Focused product that supports (4 x 25 Gb/s) emerging 100 Gb/s Ethernet standards</td>
</tr>
<tr>
<td>80C10B</td>
<td>Optical bandwidth to 80GHz, supports all 40 and 100 Gb/s (4 x 25 Gb/s) standards, optional CR trigger pickoff for e.g. CR286A CRU</td>
</tr>
</tbody>
</table>
### Electrical and TDR Acquisition Modules

<table>
<thead>
<tr>
<th>Electrical Modules</th>
<th>Channels</th>
<th>Vertical Resolution</th>
<th>Bandwidth</th>
<th>Risetime (10%-90%)</th>
<th>Monolithic or Remote</th>
</tr>
</thead>
<tbody>
<tr>
<td>80E02</td>
<td>1</td>
<td>16 bits</td>
<td>50 GHz</td>
<td>7 ps</td>
<td>Monolithic</td>
</tr>
<tr>
<td>80E03</td>
<td>2</td>
<td>16 bits</td>
<td>20 GHz</td>
<td>17.5 ps</td>
<td>Monolithic</td>
</tr>
<tr>
<td>80E06</td>
<td>1</td>
<td>16 bits</td>
<td>70+ GHz</td>
<td>5 ps</td>
<td>Monolithic</td>
</tr>
<tr>
<td>80E07</td>
<td>2</td>
<td>16 bits</td>
<td>30 GHz</td>
<td>11.7 ps</td>
<td>Remote (2 meter)</td>
</tr>
<tr>
<td>80E09</td>
<td>2</td>
<td>16 bits</td>
<td>60 GHz</td>
<td>5.8 ps</td>
<td>Remote (2 meter)</td>
</tr>
</tbody>
</table>

**DSA8300**采样示波器-电信号测试模块
逻辑分析仪系列 TLA6400

- **TLA6400 Series LA**
  - Replaces TLA5000 & TLA6200 products
  - TLA6401 34 ch
  - TLA6402 68 ch
  - TLA6403 102 ch
  - TLA6404 136 ch

- **P5900 Series Probes**
  - P5910 17 ch GP
  - P5934 34 ch Mictor
  - P5960 34 ch DMAX
## Models

<table>
<thead>
<tr>
<th>Models</th>
<th>Channels (per module)</th>
<th>State Clock Rate</th>
<th>Record Length (Full CH)</th>
<th>Timing</th>
<th>MagniVu™ Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLA6401</td>
<td>32</td>
<td>333 MHz (std)</td>
<td>2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb</td>
<td>1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)</td>
<td>40 ps (25 GS/s) 128 Kb</td>
</tr>
<tr>
<td>TLA6402</td>
<td>68</td>
<td>333 MHz (std)</td>
<td>2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb</td>
<td>1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)</td>
<td>40 ps (25 GS/s) 128 Kb</td>
</tr>
<tr>
<td>TLA6403</td>
<td>102</td>
<td>333 MHz (std)</td>
<td>2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb</td>
<td>1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)</td>
<td>40 ps (25 GS/s) 128 Kb</td>
</tr>
<tr>
<td>TLA6404</td>
<td>136</td>
<td>333 MHz (std)</td>
<td>2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb</td>
<td>1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)</td>
<td>40 ps (25 GS/s) 128 Kb</td>
</tr>
<tr>
<td>TLA6404GSA</td>
<td>136</td>
<td>333 MHz (std)</td>
<td>2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb</td>
<td>1.6 GS/s (all ch) 3.2 GS/s (1/2 ch)</td>
<td>40 ps (25 GS/s) 128 Kb</td>
</tr>
</tbody>
</table>
逻辑分析仪TLA7000系列

- TLA7012 Portable Mainframe
  支持2模块的主机(272通道)

- TLA7016 Benchtop Mainframe
  支持6模块的主机(支持136×6=816通道)
TPI4000 系列协议分析仪

TPI4202
- Portable
- Two Card Slots
- Built-in screen and keyboard

TPI4208
- 4U Rackmount
- 2 Card Slots
TPI4000 系列
一台仪器可以支持多种协议

- Fibre Channel
  - FICON, AS1760, ASM, FC-AE-1553, others

- Ethernet
  - iSCSI, FCoE, TCP/IP, IPv6, iFCP, AFDX, ARINC664, TTE, others

- Serial Front Panel Data Port (Serial FPDP)

- Serial Attached SCSI (SAS)

- Serial ATA (SATA)

- Common Public Radio Interface (CPRI)

- Serial RapidIO (SRIO)
BSA误码仪系列

误码仪主机
BSA260C
BSA175C
BSA125C
BSA850V

时钟恢复模块
CR286A
CR125A

• 预加重模块
• DPP125

BA1500/1600
• Basic BERT & Scope

26G
28.6G
12.5G
1.5G/1.6G

17.5G
17.5G
12.5G
12.5G

12.5G

接收端抖动容限测试

1. 配置
2. 游标示波器显示结果
3. 循环环回
4. 误码率测试结果

从压垮的模式发生器
到错误检测器

设备待测（DUT）

Detector Results

<table>
<thead>
<tr>
<th>Bits</th>
<th>837,430,471,808</th>
</tr>
</thead>
<tbody>
<tr>
<td>Errors</td>
<td>1,095,813,556</td>
</tr>
<tr>
<td>BER</td>
<td>1.67E-03</td>
</tr>
</tbody>
</table>
任意波形发生器 AWG5000C/7000C 系列

<table>
<thead>
<tr>
<th>AWG5000C</th>
<th>AWG7000C</th>
</tr>
</thead>
<tbody>
<tr>
<td>600MS/s and 1.2 GS/s models</td>
<td>8 GS/s and 12 GS/s</td>
</tr>
<tr>
<td>2 and 4 channels</td>
<td>1 and 2 channels</td>
</tr>
<tr>
<td>14 bit vertical resolution</td>
<td>Optional 16 &amp; 24 GS/s interleaving on the 2 channel 8 &amp; 12 GS/s models</td>
</tr>
<tr>
<td>4 or 8 markers</td>
<td>10/8 bit vertical resolution</td>
</tr>
<tr>
<td>Sequencing, Sub-sequencing &amp; Dynamic Jump capability</td>
<td>2 or 4 markers</td>
</tr>
<tr>
<td>28 bit digital output option on 2 channel models</td>
<td>Sequencing, Sub-sequencing &amp; Dynamic Jump capability</td>
</tr>
</tbody>
</table>