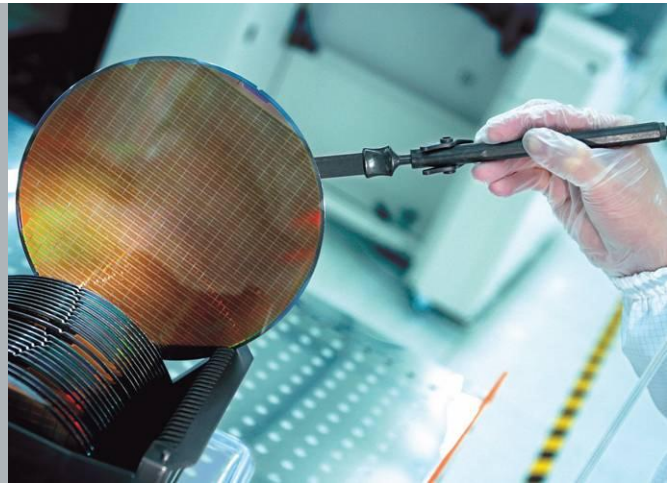
高速串行总线测试技术发展

Liu Jian

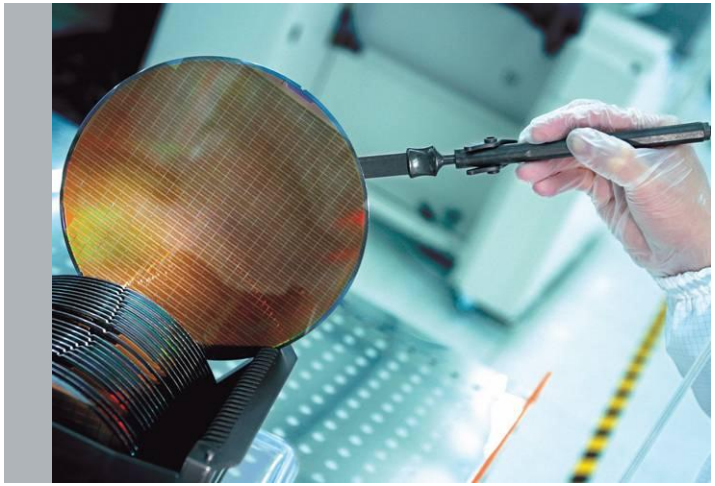
2012-11



SALES UNIVERSITY 2011
CHANGE THE GAME

Tektronix®

PHY Validation of Thunderbolt & DisplayPort



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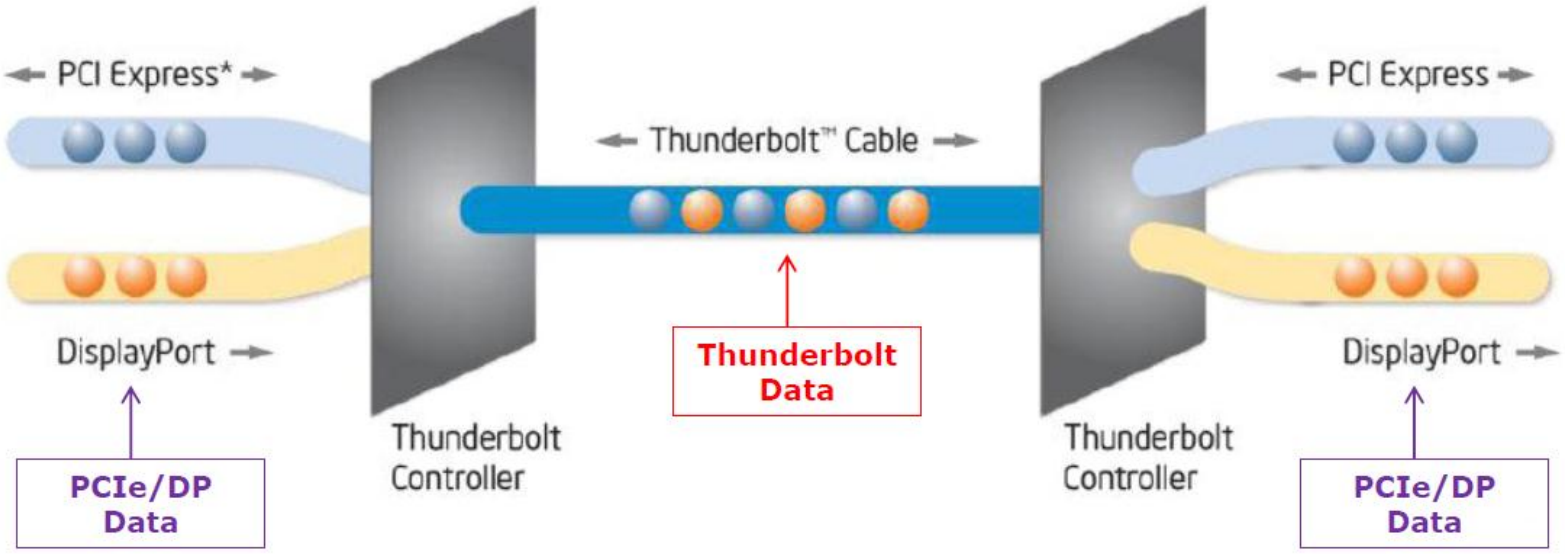
Thunderbolt Overview

- High Speed Data Bus for PC's
  - Brought to market by Intel/Apple in 2011
  - Interoperable with DisplayPort
- Thunderbolt signaling is dual NRZ (64/66b Encoded)
  - 10.3125 Gb/s data rate
  - It utilizes SFP+ technology with 2 diff Tx and Rx pairs.



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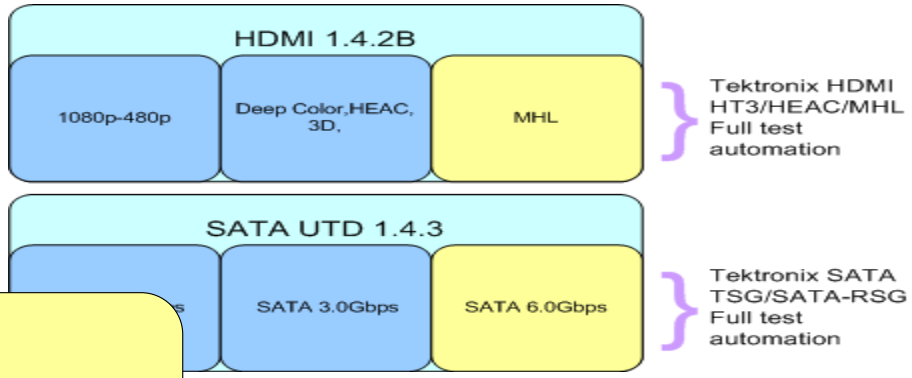
Thunderbolt Electrical Validation

Tektronix DPOJET
Thunderbolt .7 MOI
Manual Test



Thunderbolt (.7 Spec Revision)
10.3125Gbps

Thunderbolt (future Interop)

Display Port DP1.2

RBR (1.6Gbps),

HBR (2.7Gbps)

HBR2 (5.4Gbps)

DP++

Tektronix DP12
Full test automation

Dual Port Device Compliance Test Summary

- Physical Layer Testing
  - (Rev 0.7 Spec)
1. TBT Transmitter MOI
2. TBT Receiver MOI
3. TBT Return Loss MOI
4. DP Source MOI
5. DP++ (HDMI) Source MOI
6. Power Delivery MOI

- Functional Testing
  - Thunderbolt Functional CTS Rev 3.0.1
1. ROM Validation
2. Basic Device Functionality
3. EFI
4. Downstream Device Functionality
5. Downstream Display Functionality
6. Extended Test Functionality
7. Complex Topology
8. DUT Specific Verification
9. Negative Testing
10. Firmware Update Validation

CTS – Compliance Test Specification
MOI – Method of Implementation (Test Procedure)

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Single Port Device Compliance Test Summary

- Physical Layer Testing
  - (Rev 0.7 Spec)

1. TBT Transmitter MOI
2. TBT Receiver MOI
3. TBT Return Loss MOI
4. Power Consumption

- Functional Testing
  - Thunderbolt Functional CTS Rev 2.4 (IBL 488434)

1. ROM Validation
2. Basic Device Functionality
3. EFI
4. DUT Specific Verification
5. Negative Testing
6. Firmware Update Validation

CTS – Compliance Test Specification
MOI – Method of Implementation (Test Procedure)

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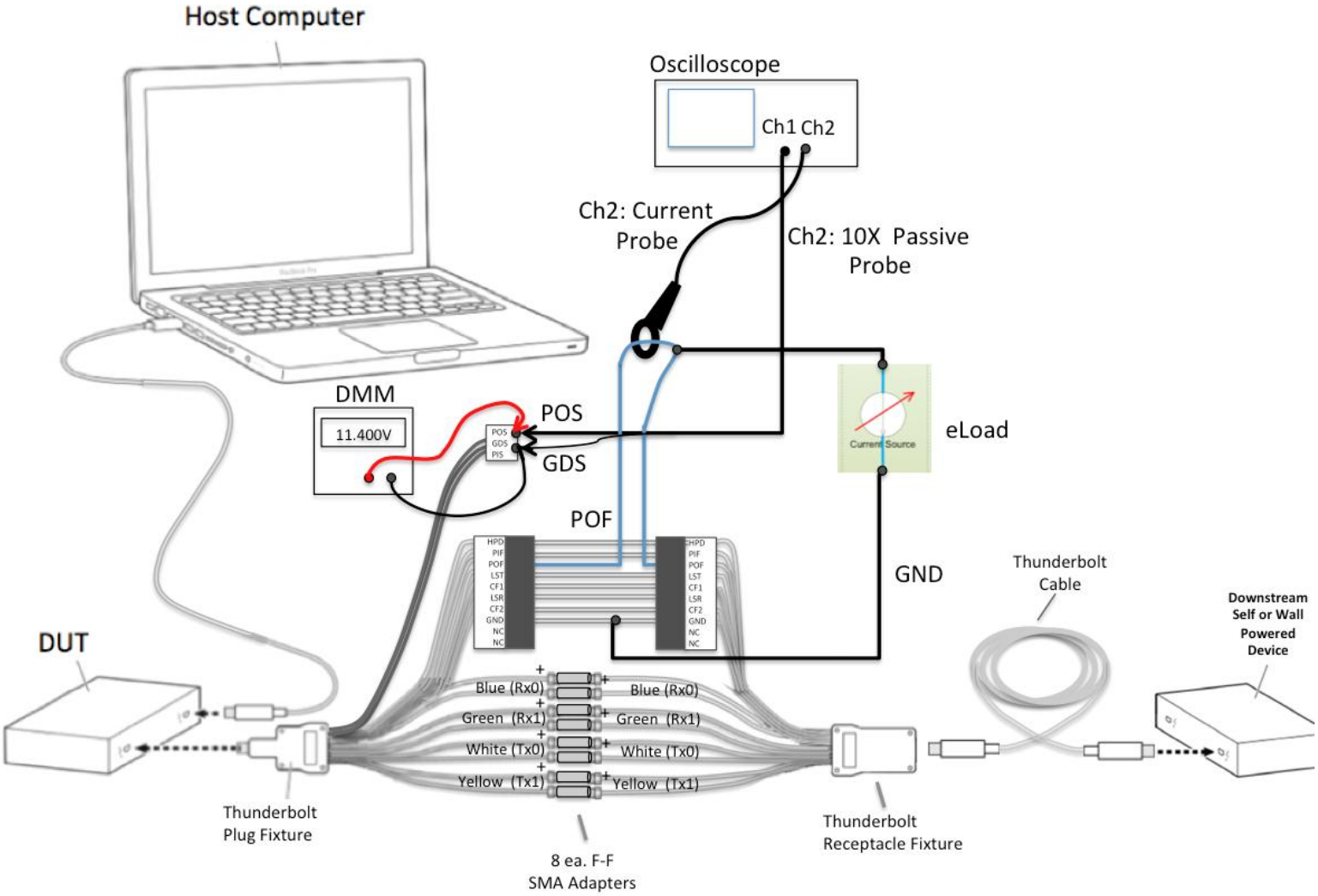
Power Delivery Testing Setup



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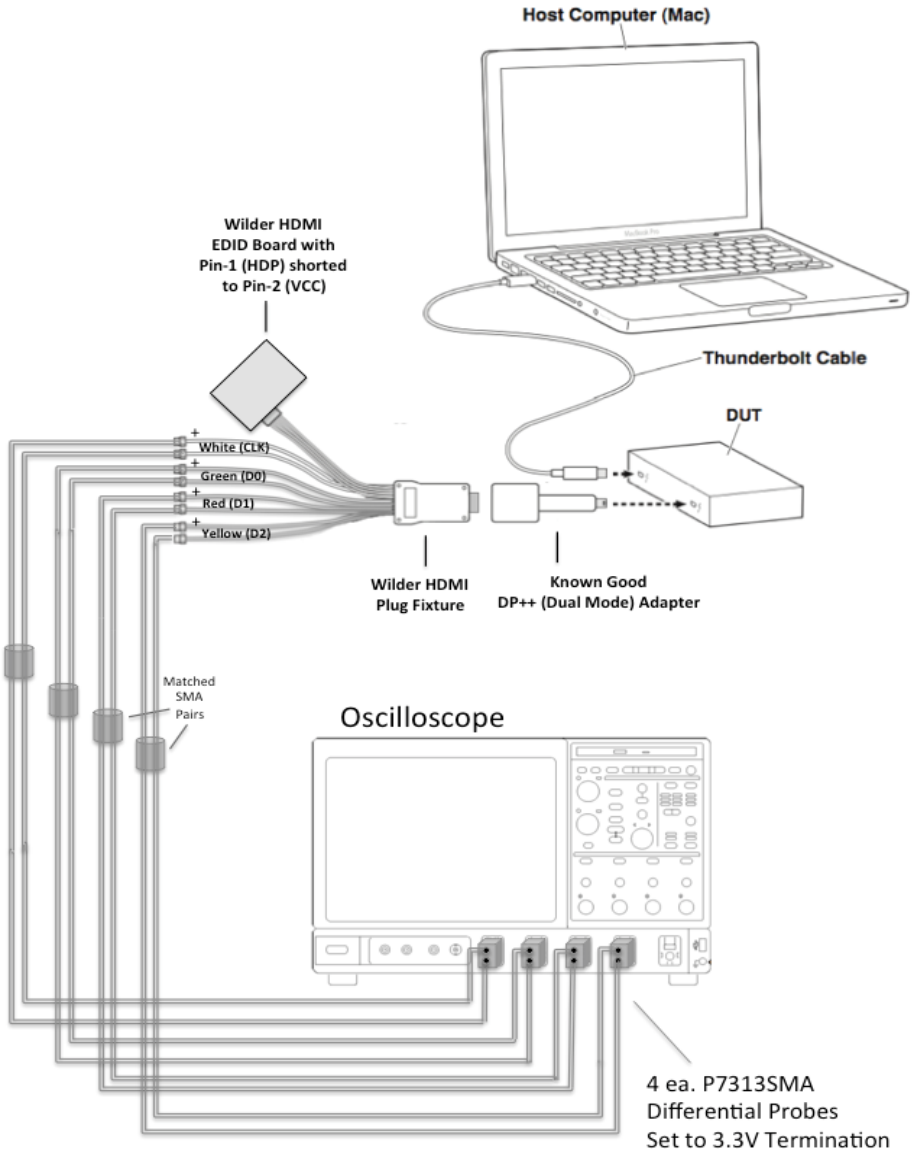
HDMI Test Setup

- DSA70804C or higher
- SMA Differential Probes
  - Provides 3.3V bias
- HT3 HDMI Compliance SW
- Mac or equivalent tool used to control downstream port on a 2 port device
- Both ports tested



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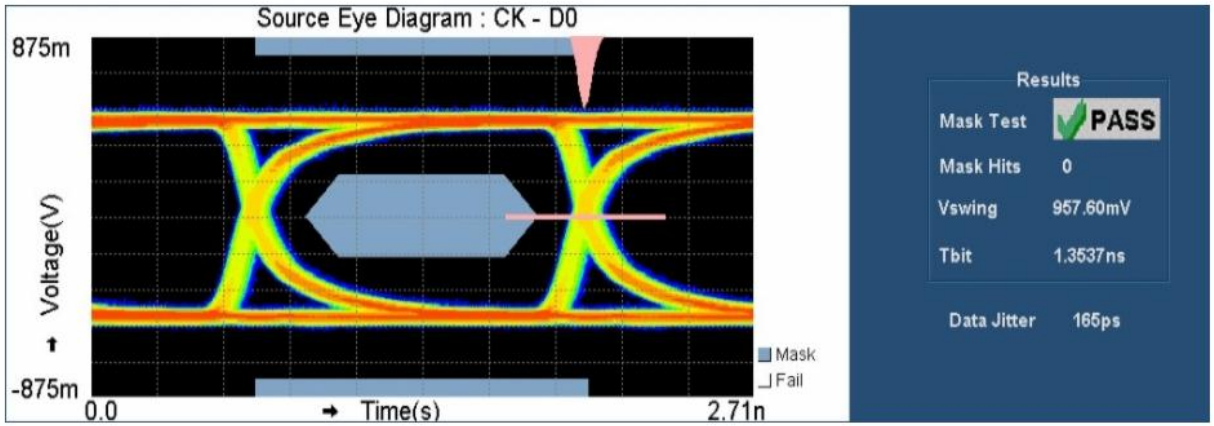
Example of HDMI Passing Results

- **Test Summary**

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.08*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.12*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.12*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.1*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0.007*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0.012*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0.005*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	220.23ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	208.34ps	Pass
10	7-4 : Source Rise Time	D1	75.00ps < TRISE;	210.28ps	Pass
11	7-4 : Source Rise Time	D2	75.00ps < TRISE;	223.47ps	Pass
12	7-4 : Source Fall Time	CK	75.00ps < TFALL;	212.71ps	Pass
13	7-4 : Source Fall Time	D0	75.00ps < TFALL;	219.38ps	Pass
14	7-4 : Source Fall Time	D1	75.00ps < TFALL;	208.07ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	254.07ps	Pass
16	7-8 : Max Duty Cycle	CK	--	--	Error
17	7-8 : Min Duty Cycle	CK	--	--	Error

- **Waveform/Plot**



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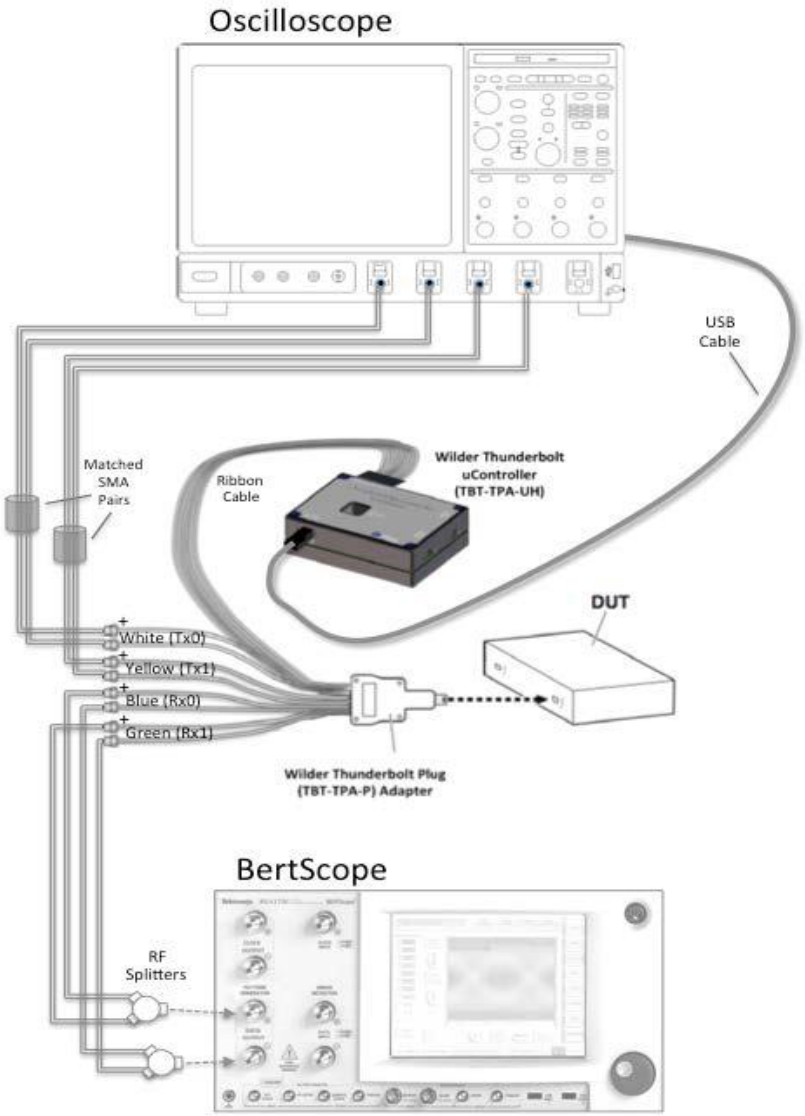
Automated Thunderbolt Tx Testing



Recommended Equipment

- DPO/DSA/MSO71604 (≥ 16 GHz BW)
- BSA125C (crosstalk source)
- Option DJA (DPOJET)
- Option TBT-TX (TekExpress)
- TF-TB-TPA-P (Plug fixture) & TBT-TPA-UH (port microcontroller)

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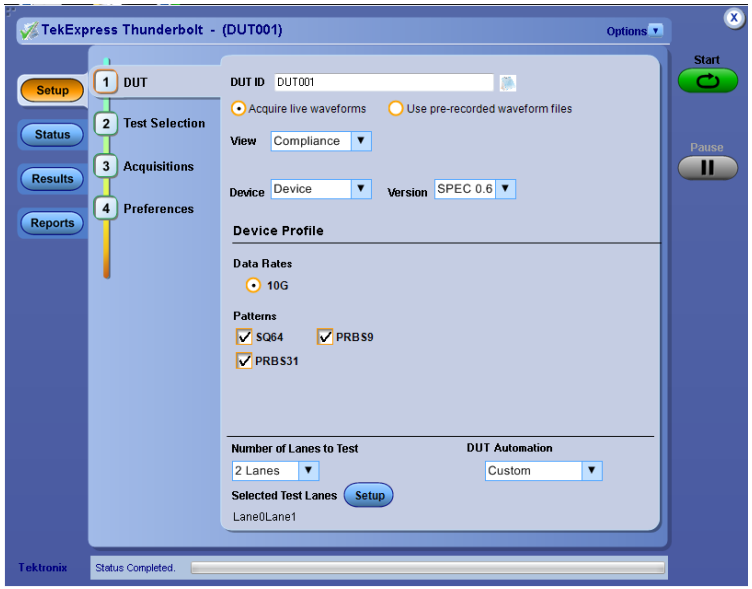
Option TBT-TX
Compliance Automation Software

- Automates scope setup & compliance measurements per the Tek Thunderbolt MOI
- Fast test execution
  - Simultaneous two lane testing
  - Automated DUT state control for devices
- User-selectable tests
- Creates complete test report



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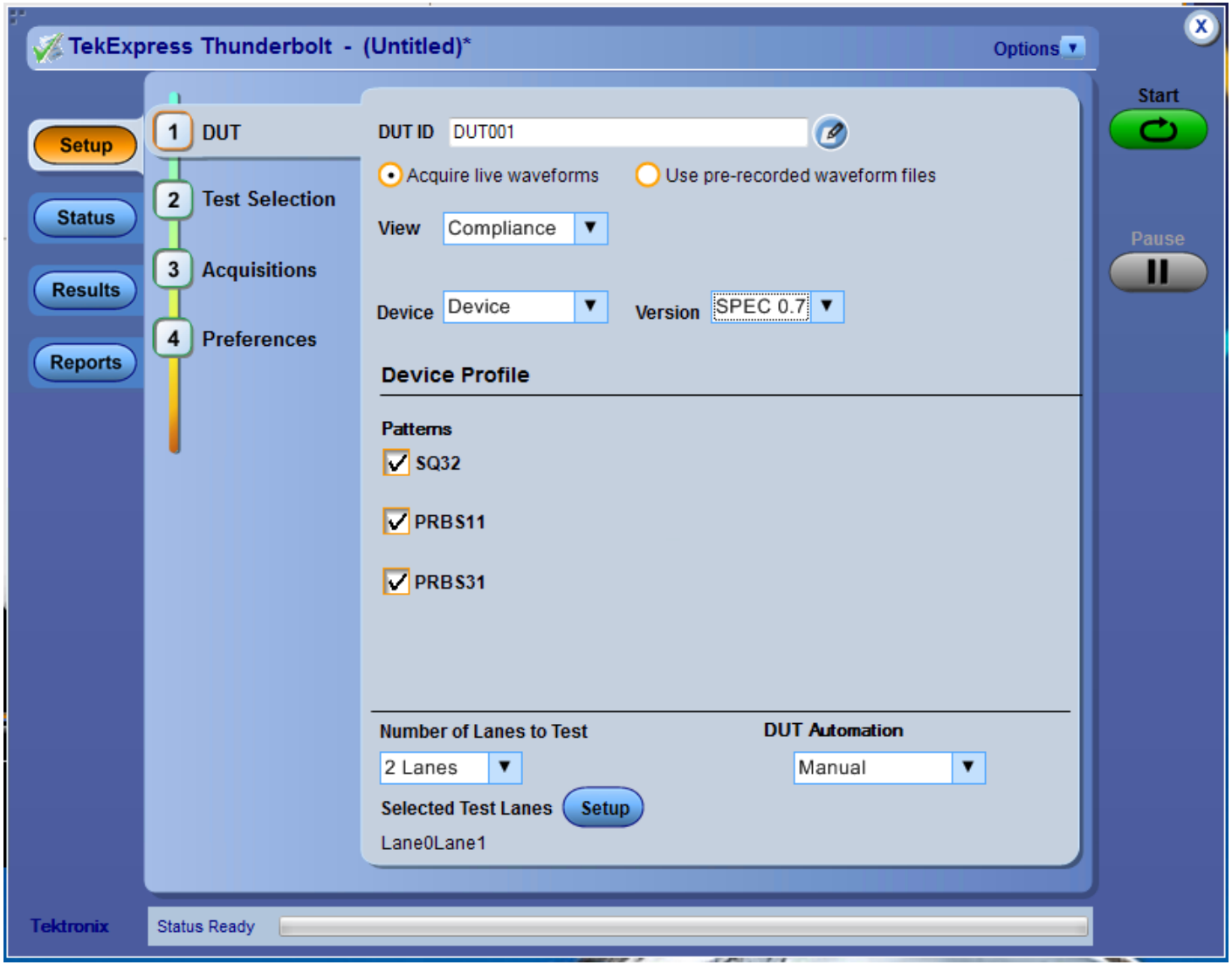
Thunderbolt Transmitter Testing

- **Step 1:** Select Measurement Setup



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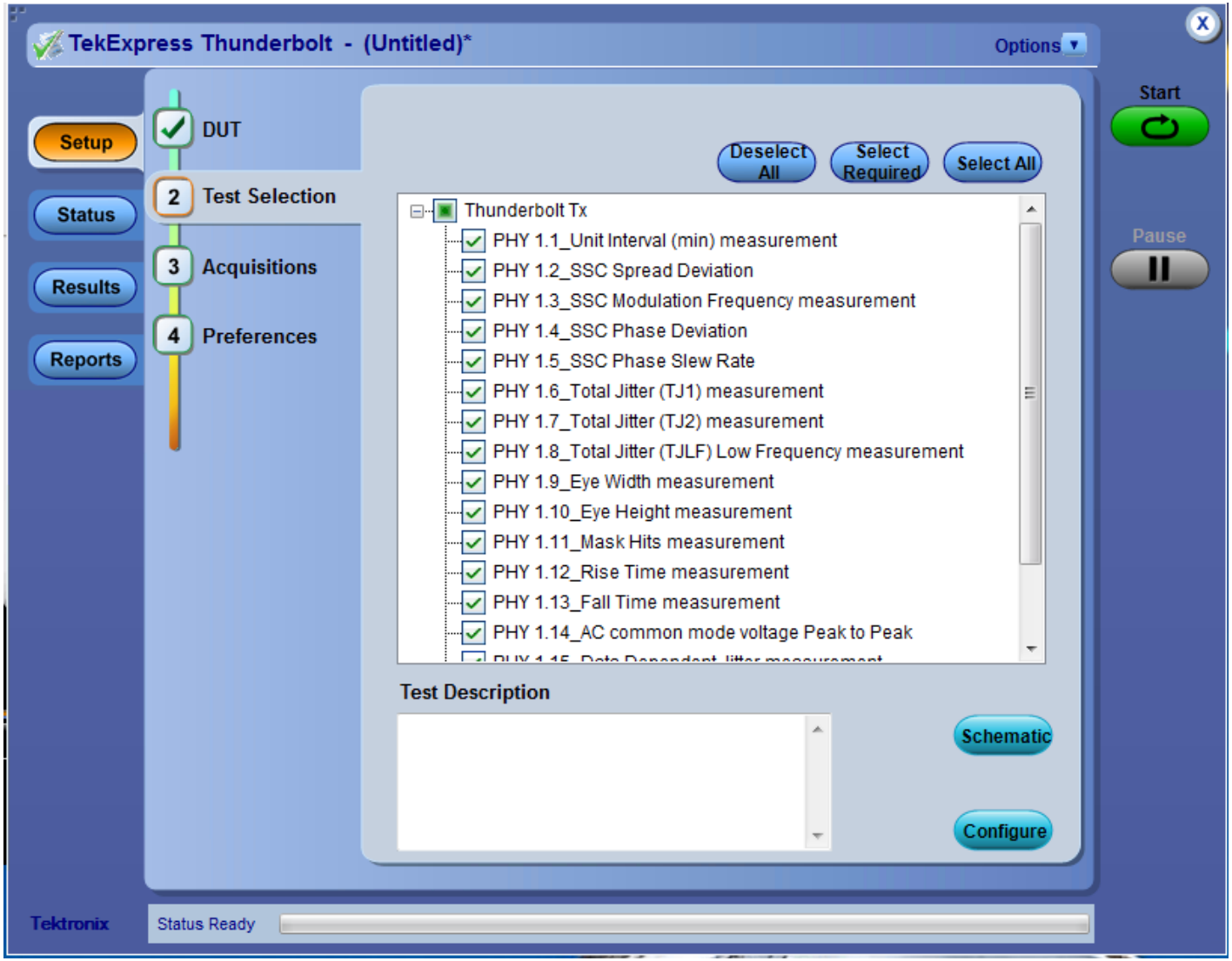
Thunderbolt Transmitter Testing

- **Step 2:** Select Measurements



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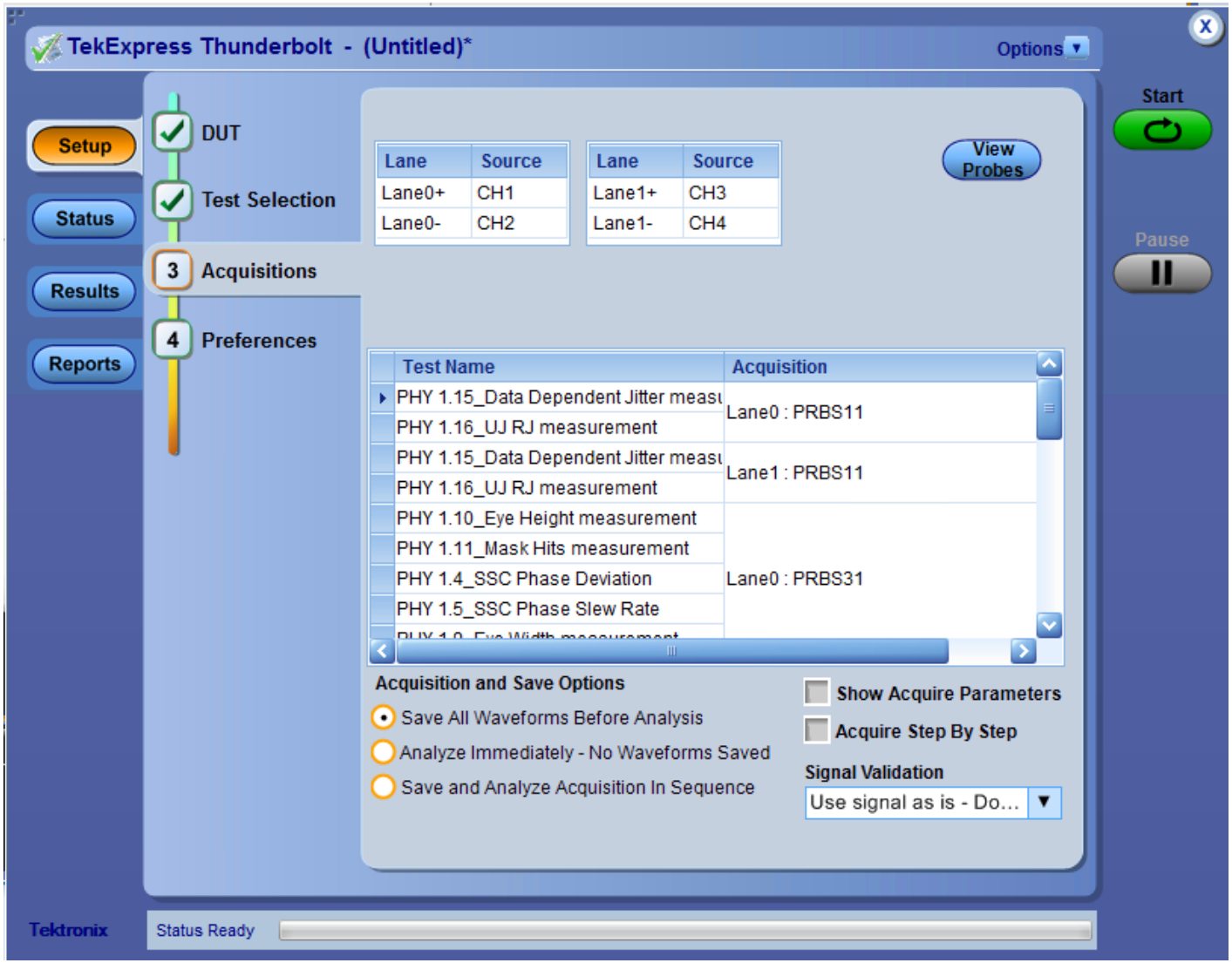
Thunderbolt Transmitter Testing

- **Step 3:** Configure Acquisitions



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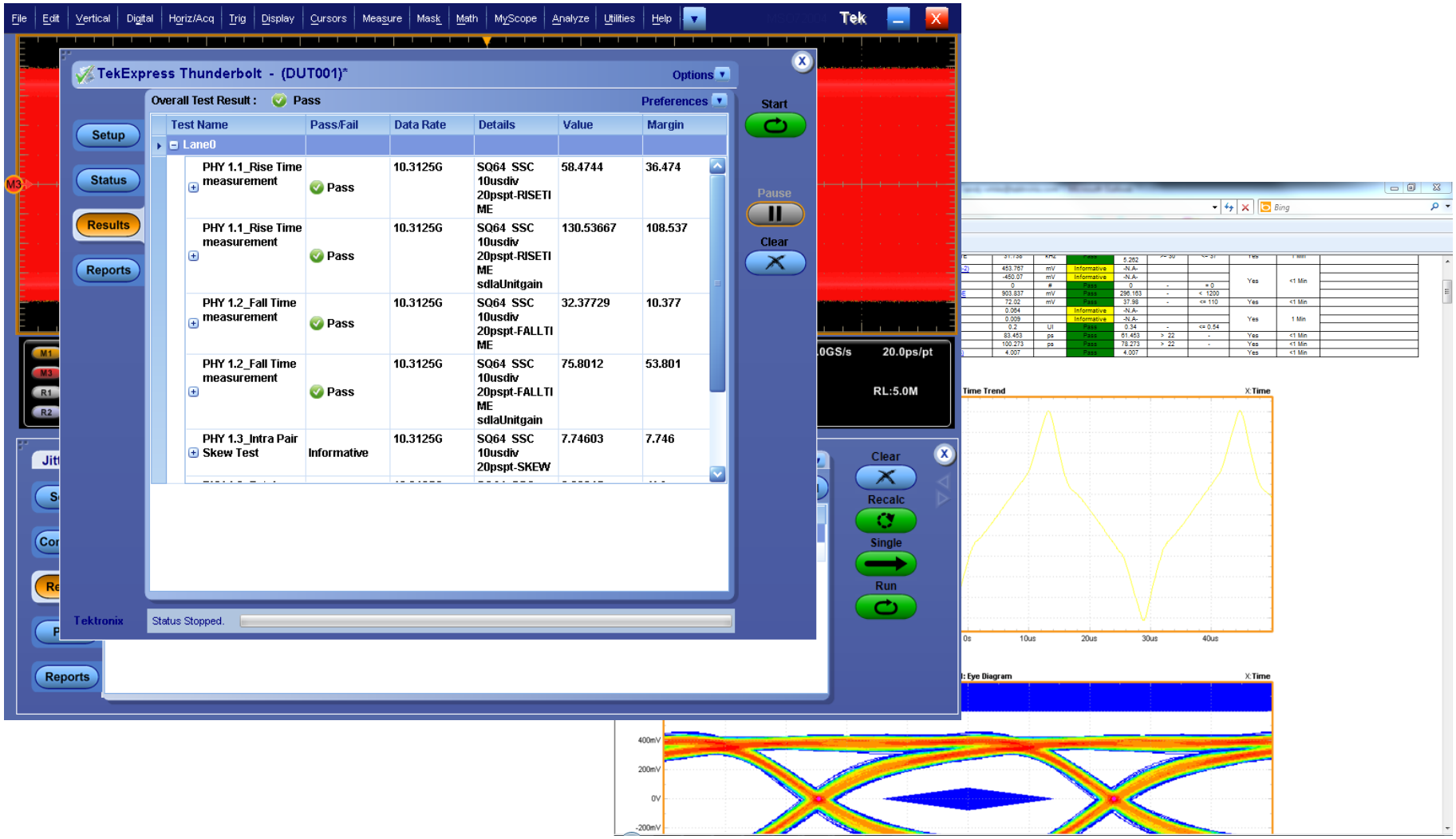
Thunderbolt Transmitter Testing

- **Step 4:** Start Tests and Generate Report



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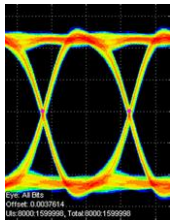
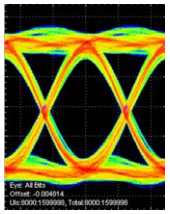
Test Challenge: De-Embedding
Transmitter Compliance Testing

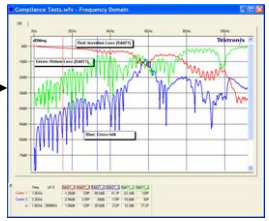
- Host/device compliance point at TP1 (mated plug/receptacle)
- De-embedding required to remove fixture effects
- S-Parameters are acquired from calibration fixture



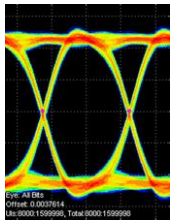
Signal at TP1



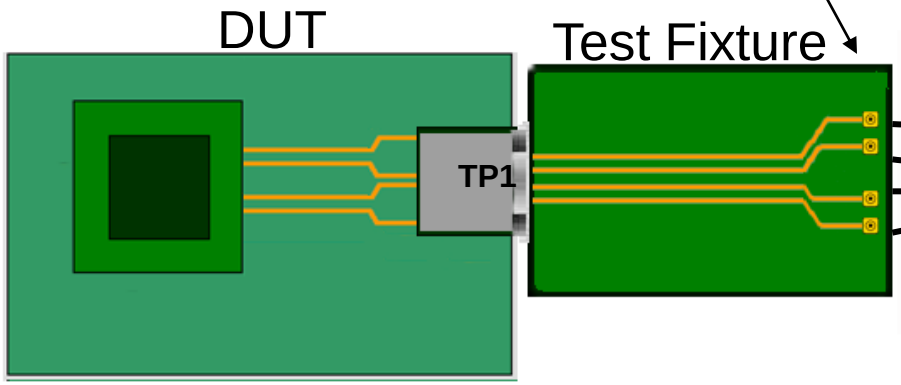
Measured Signal

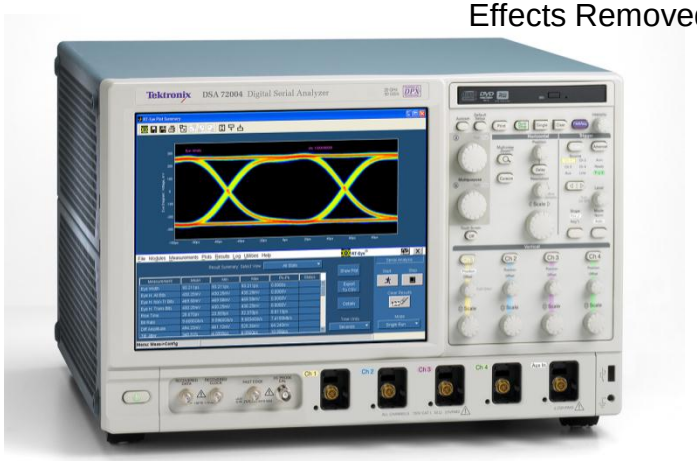


Apply S-Parameters



Signal with Fixture Effects Removed





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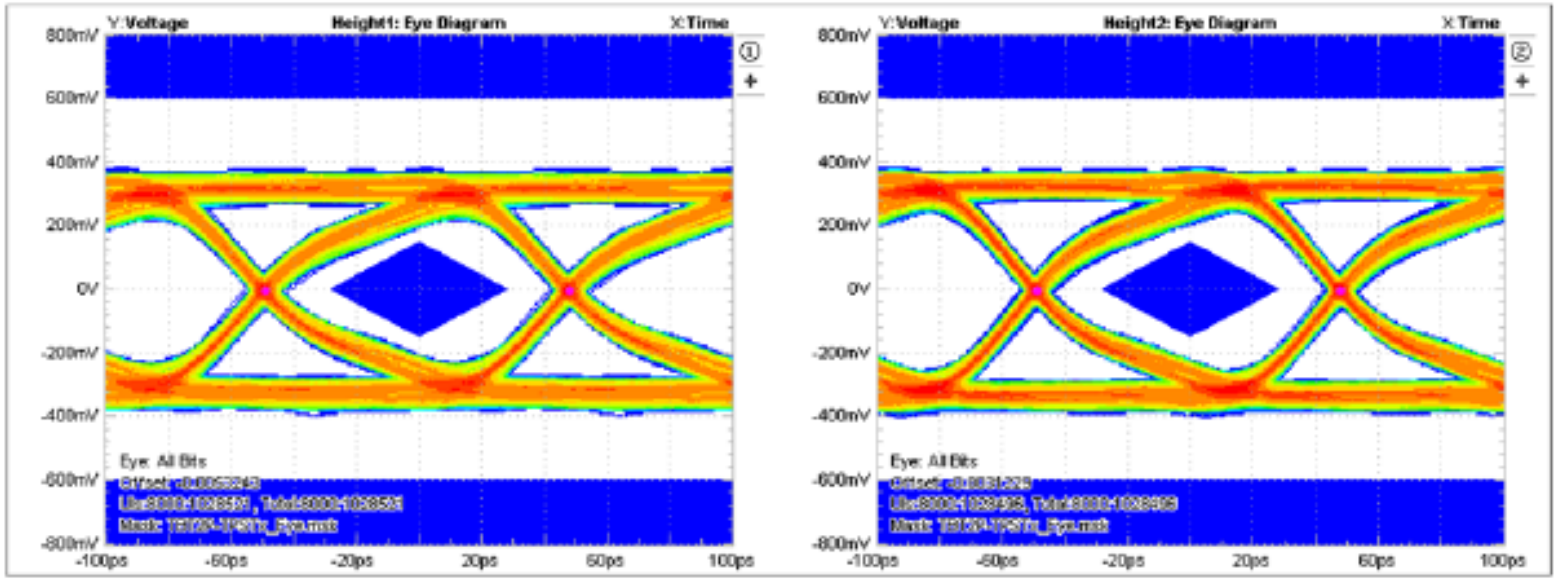
Thunderbolt Fixture De-Embed results

- **Measurement Results**

Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Height1, Math1	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Height2, Math3	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
TJ@BER1, Math1	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
TJ@BER2, Math3	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s

- **Pass/Fail Summary** No pass/fail limits are currently selected.
- **Plot Images**
  - **Measurement Plot(s)**



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Test Challenge: Crosstalk
Measuring Bounded Uncorrelated Jitter (BUJ) is Critical

- Interconnect and board layout technology is advancing and the greatest area of focus is in reducing the insertion loss and Signal-to-Crosstalk ratio.
- The implications of complex channel interaction can be observed and identified by examining the type and amount of BUJ.
- There is a strong Cause–and-Effect relationship between Crosstalk and BUJ which often gets classified as Random if special steps are not observed.

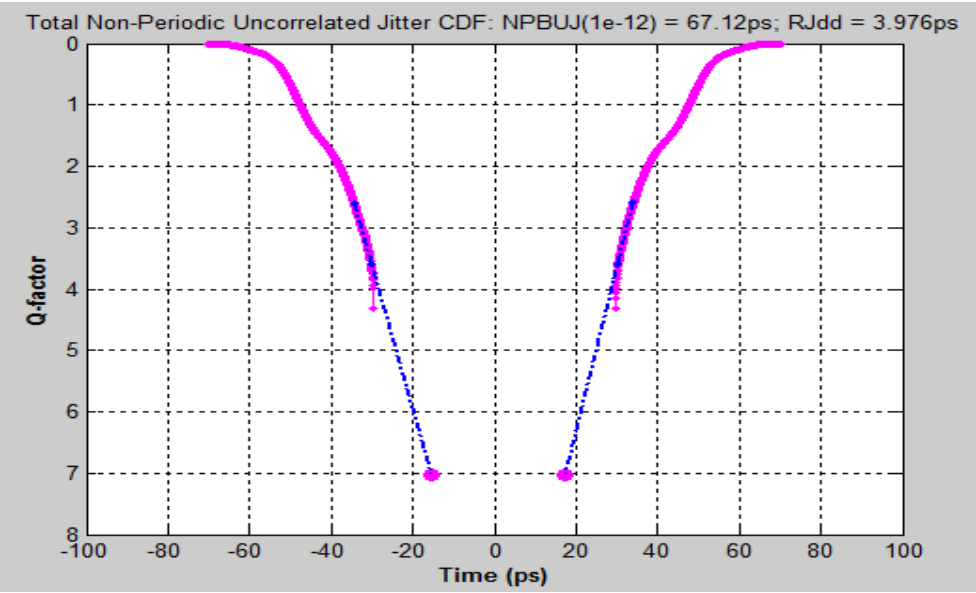

Table 4-6. Stressed Receiver Conditions

Symbol	Description
Input swing	Inner eye voltage
AC-CM_rms	AC Common Mode Voltage rms
AC-CM_pk_pk	AC Common Mode Voltage pp
BUJ	Bounded Uncorrelated Jitter
DDJ	Data Dependent Jitter
RJ	Random Jitter
TJ	Total Jitter

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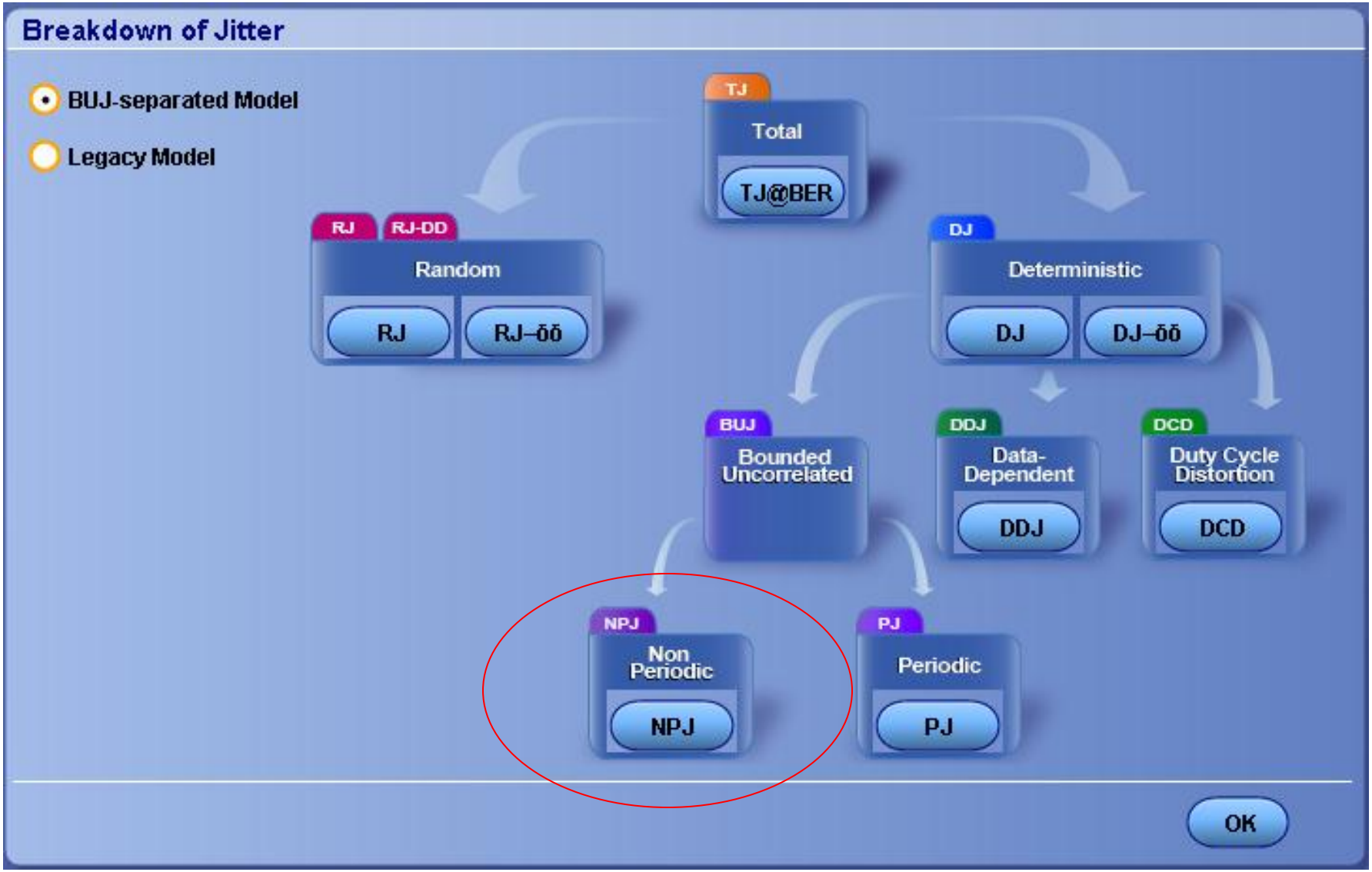
BUJ in real time jitter analysis



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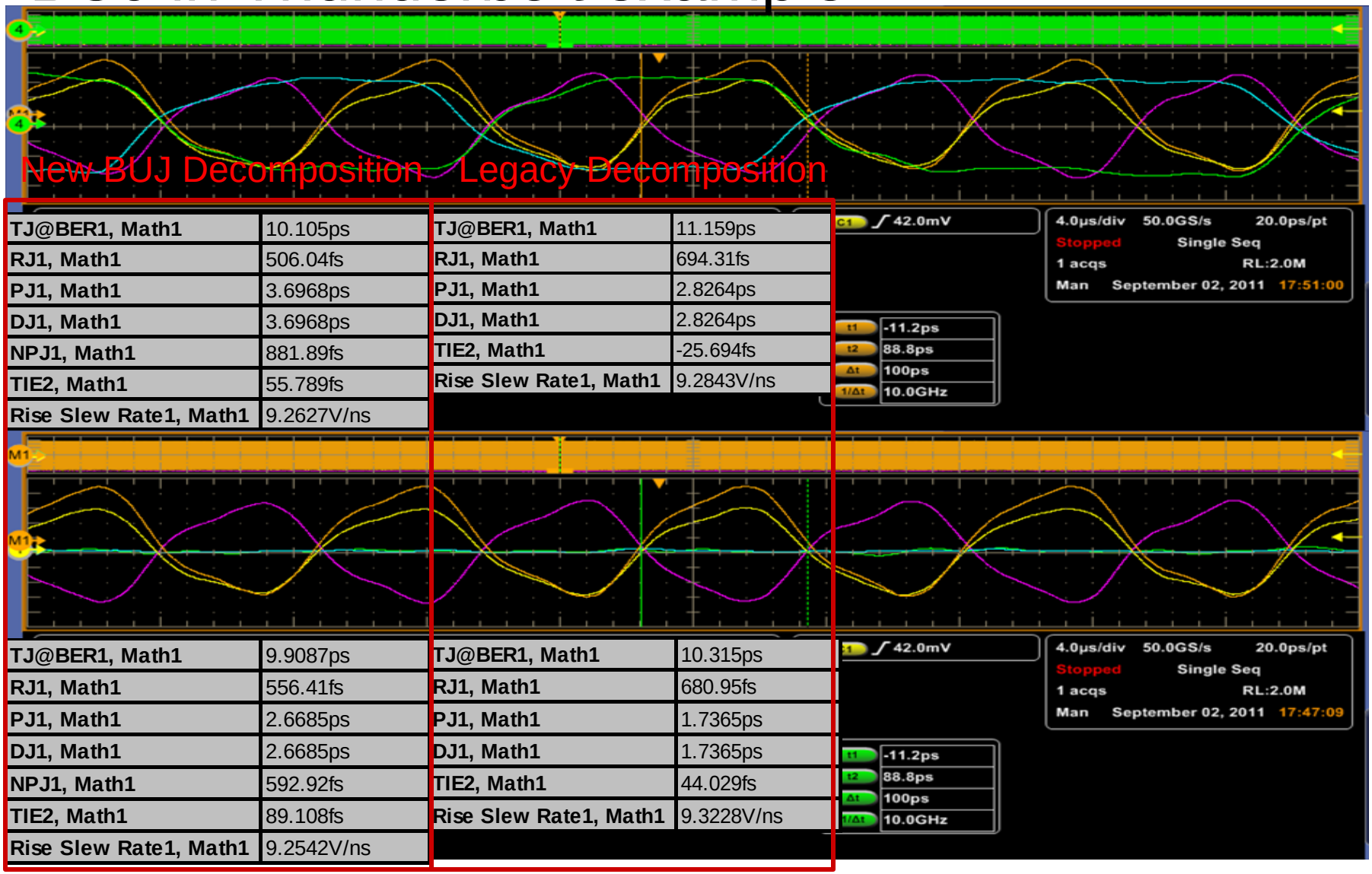
BUJ in Thunderbolt example



TJ@BER1, Math1	10.105ps
RJ1, Math1	506.04fs
PJ1, Math1	3.6968ps
DJ1, Math1	3.6968ps
NPJ1, Math1	881.89fs
TIE2, Math1	55.789fs
Rise Slew Rate1, Math1	9.2627V/ns

TJ@BER1, Math1	11.159ps
RJ1, Math1	694.31fs
PJ1, Math1	2.8264ps
DJ1, Math1	2.8264ps
TIE2, Math1	-25.694fs
Rise Slew Rate1, Math1	9.2843V/ns

TJ@BER1, Math1	9.9087ps
RJ1, Math1	556.41fs
PJ1, Math1	2.6685ps
DJ1, Math1	2.6685ps
NPJ1, Math1	592.92fs
TIE2, Math1	89.108fs
Rise Slew Rate1, Math1	9.2542V/ns

TJ@BER1, Math1	10.315ps
RJ1, Math1	680.95fs
PJ1, Math1	1.7365ps
DJ1, Math1	1.7365ps
TIE2, Math1	44.029fs
Rise Slew Rate1, Math1	9.3228V/ns

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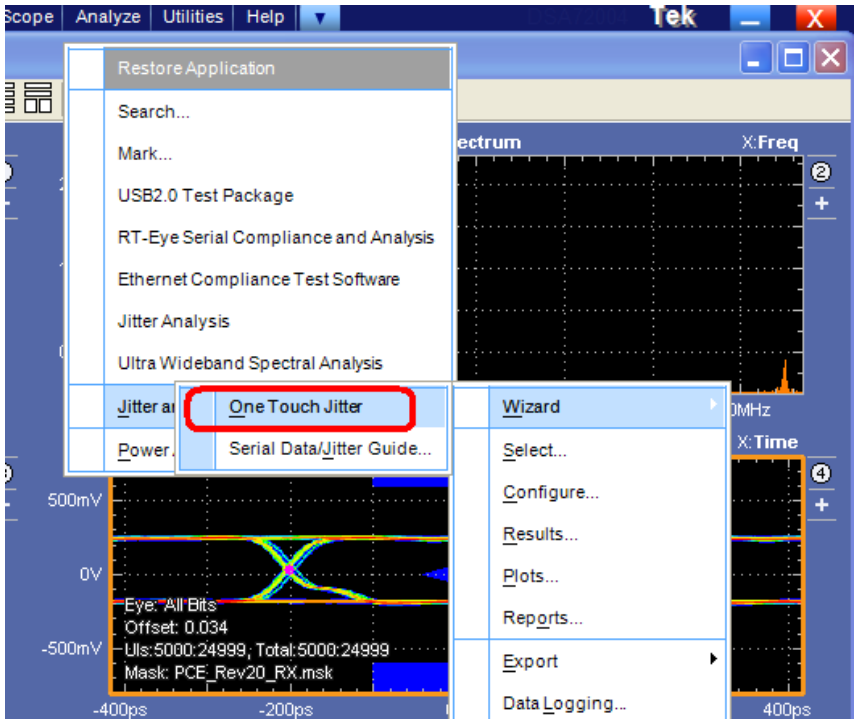
DPOJET业内使用*最简单*的抖动测试工具

- “ONE Touch”一键式的软件设计思路，任何抖动测量，无需复杂的设定，一键完成测试
  - 自动选择示波器输入通道
  - 自动判断测试信号类型(clock或data)
  - 最优化完成示波器采集参数
  - 自动测试参考电平
  - 自动选择抖动项目(用户可定制)
  - 自动完成测量项目参数设定
  - 自动完成结果分析、图表生成
- “ONE Touch”一键式功能使得工程师摆脱枯燥的、繁琐、易错的参数设置环节，直接将测试结果呈现在工程师面前！



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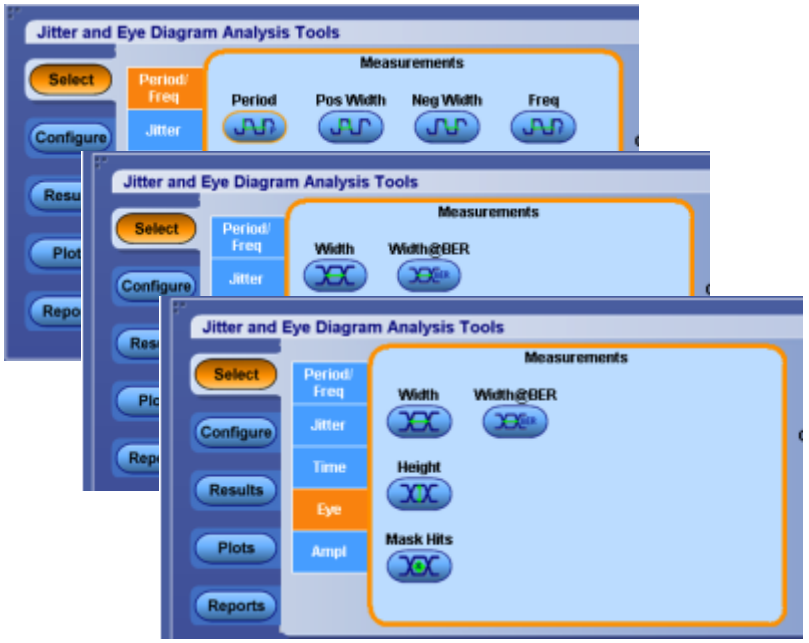
DPOJET业内测试内容*最丰富*的抖动测试工具

- 测试内容丰富多样，包括抖动、眼图和各种时序测量
- 支持各种测试标准、抖动分析模型
  - Tektronix专利的抖动分析模型
  - Dual Dirac抖动分析模型(PCIE2.0规范使用)
    - 标准定义模板以及用户自定义模板
- 最多可同时测试99个项目



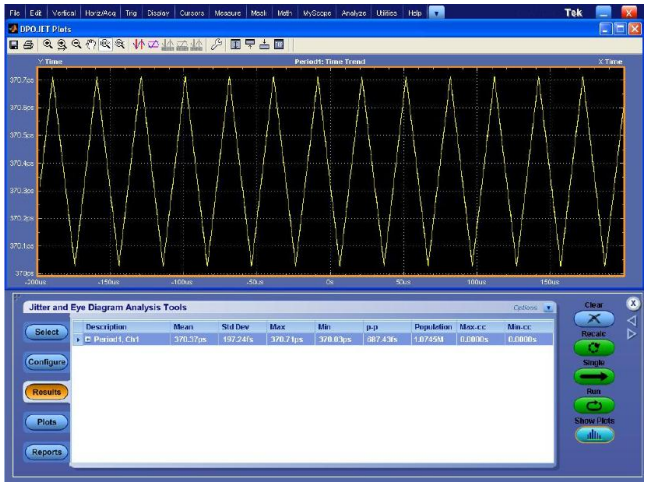
▶ Partial List of Measurements

Period/Frequency Measurements	Frequency, Period, N-Period, Cycle-Cycle Period, Positive Width, Negative Width, Positive Duty Cycle, Negative Duty Cycle, Positive Cycle-Cycle Duty, Negative Cycle-Cycle Duty
Time Measurements	Rise Time, Fall Time, High Time, Low Time, Setup, Hold, Skew
Amplitude Measurements Crossover	High, Low, High-Low, Common Mode, T/nT Ratio, Differential
Eye Diagram Measurements	Eye Height, Eye Width, Width@BER, Mask Hits
Jitter Measurements	TIE, RJ, DJ, TJ(BER), PJ, DCD, DDJ, RJ(σ-σ), DJ(σ-σ), Phase Noise

DPOJET测试举例－SSC测试

- SSC (Spread Spectrum Clock)
  - SSC目的是为了减小参考时钟对周围系统EMI的干扰，采用的人为将参考时钟进行FM调制，使其能量在一段频谱内平均，从而减小EMI。
  - 目前流行的高速总线中都采用了SSC的设计
  - SSC的测试要求考察调制的幅度以及频率是否满足规范要求

- SSC测试时，需要对DPOJET测量的抖动(clock/data period)进行低通滤波。如DisplayPort，滤波器是2阶、带宽1.98M的低通滤波器



DisplayPort中SSC调制精度以及偏移测试

DisplayPort中SSC测试中滤波器的设置

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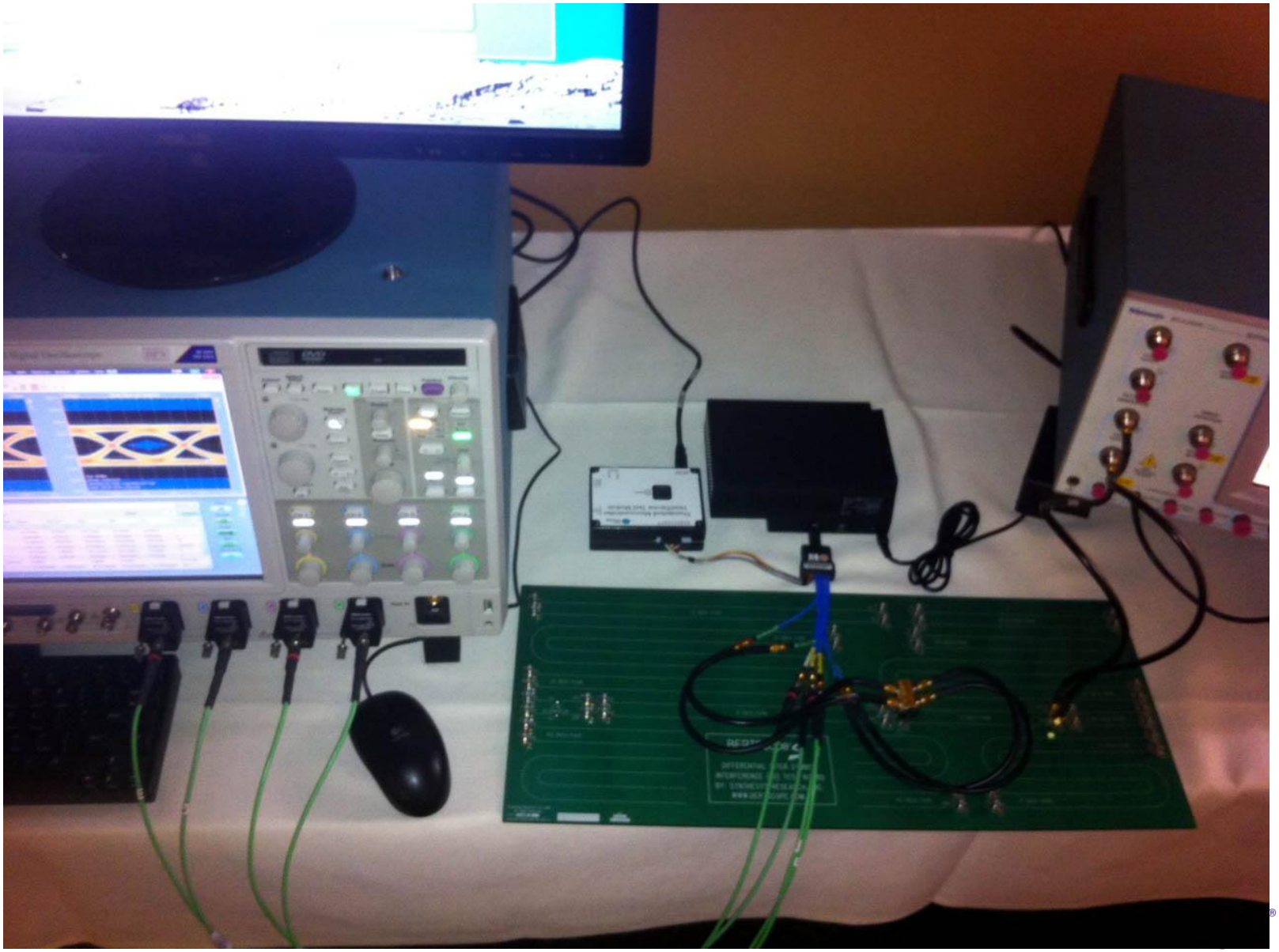
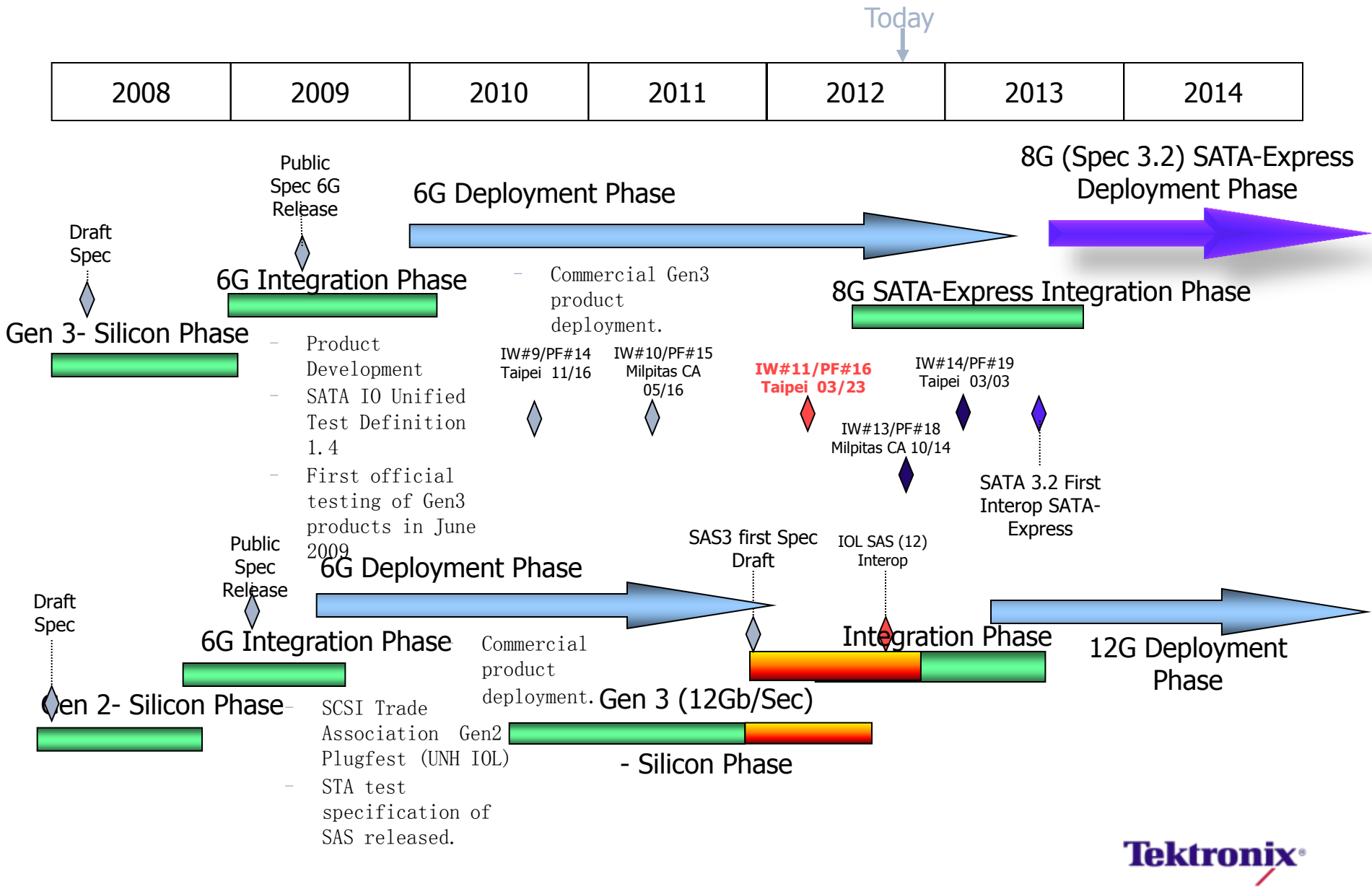
THUNDERBOLT™

DisplayPort

DEMO

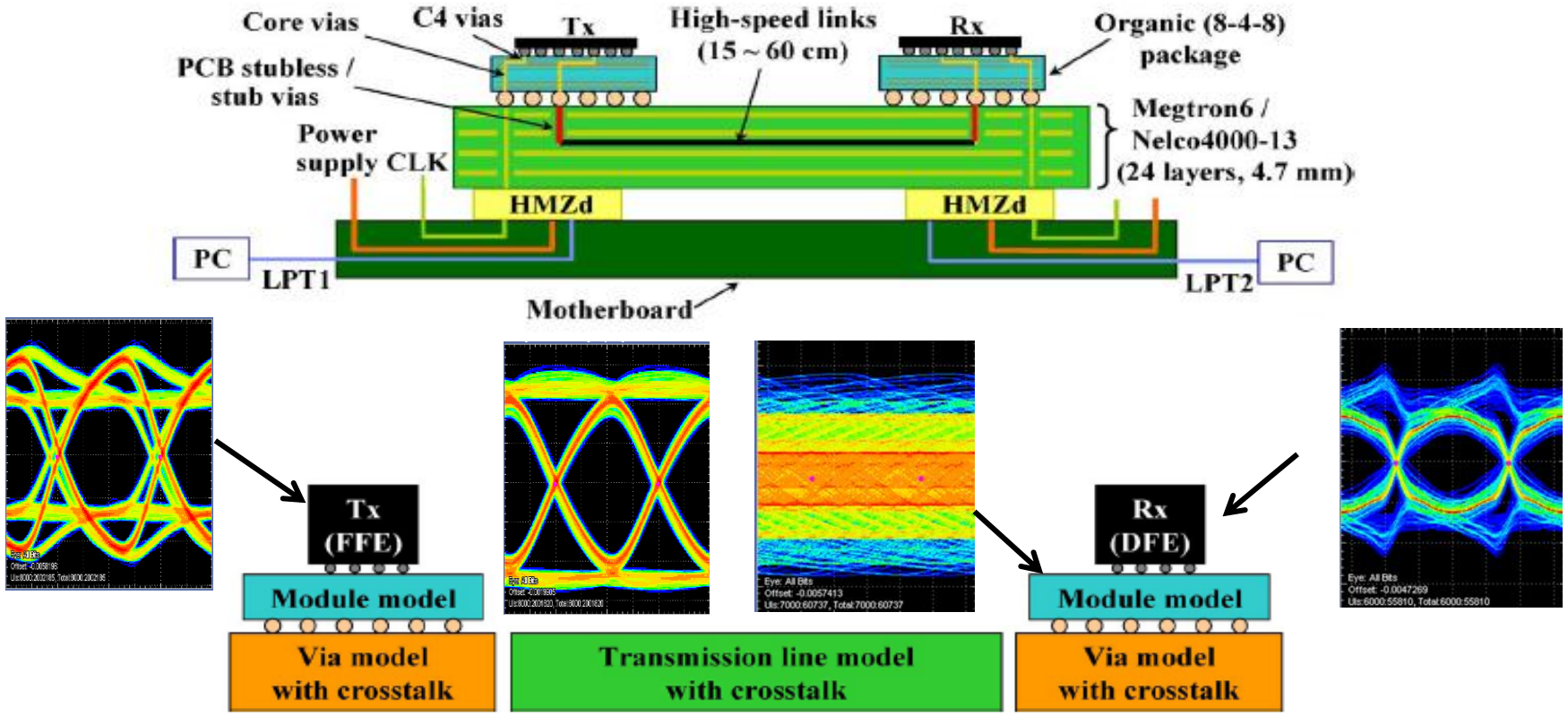


Storage Timelines and Solutions Development



12G+ Design Problem:
1000mV, FFE, Crosstalk, DFE, 50mV

- Crosstalk and signal loss problems are the largest design challenge today.
- Significant advances in high tap count Decision Feedback Equalization are key to operating at 12G+.



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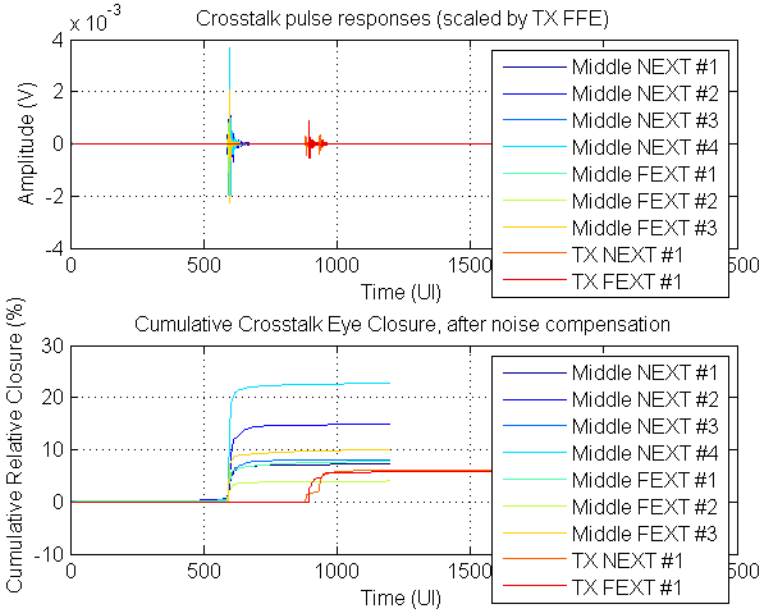
NEW Measurement for Crosstalk/ISI Evaluation

- SAS3_EYEOPENING* Measurement for accurate analysis of ISI and crosstalk effects
- Provides measure of relative vertical eye opening after reference equalization



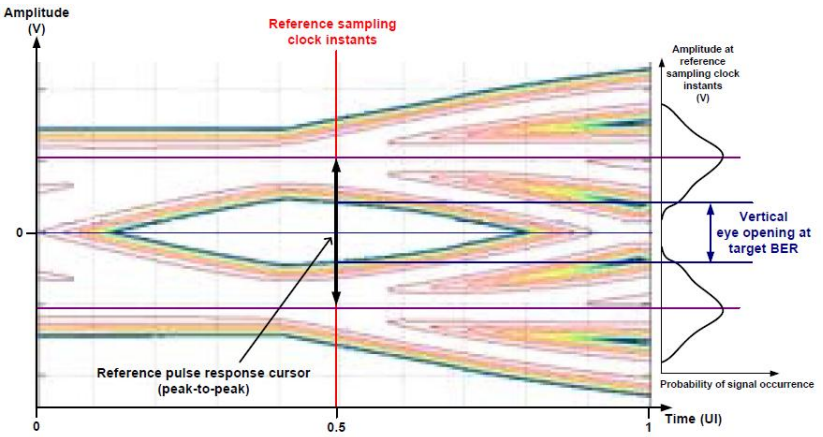


Figure Fe – Simulated Vertical eye opening and reference pulse response cursor

Source: 12-244r3

*Note, this measurement is similar to the SAS-2 Waveform Distortion Penalty (WDP) measurement but also includes Tx EQ in addition to DFE. The code was provided and distributed through the T10 Technical Committee and permission has been granted for Tektronix to reuse.

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Test Challenge: Crosstalk
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- The implications of complex channel interaction can be observed and identified by examining the type and amount of BUJ.
- There is a strong Cause–and-Effect relationship between Crosstalk and BUJ which often gets classified as Random if special steps are not observed.

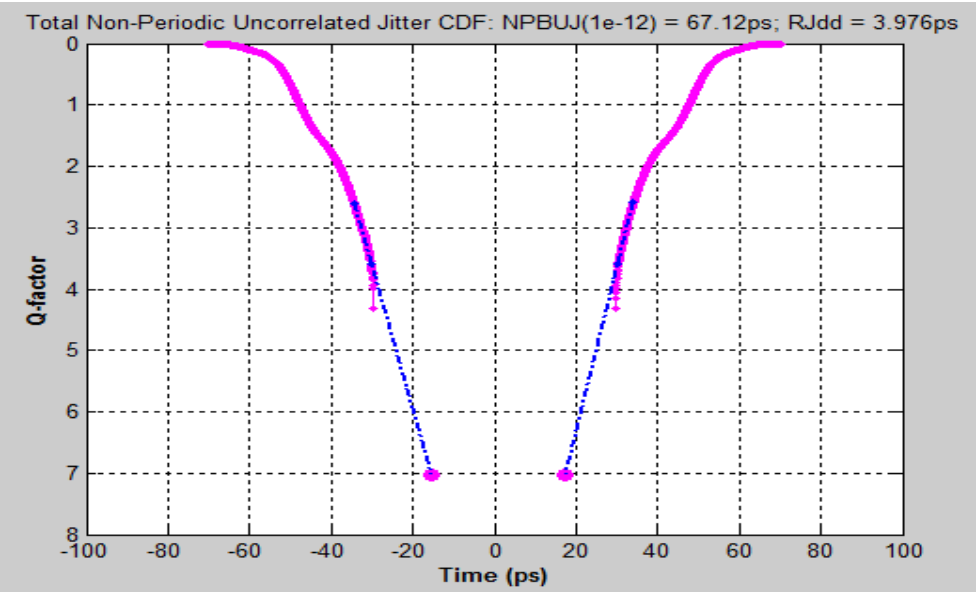

Table 4-6. Stressed Receiver Conditions

Symbol	Description
Input swing	Inner eye voltage
AC-CM_rms	AC Common Mode Voltage rms
AC-CM_pk_pk	AC Common Mode Voltage pp
BUJ	Bounded Uncorrelated Jitter
DDJ	Data Dependent Jitter
RJ	Random Jitter
TJ	Total Jitter

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SAS3_EYEOPENING provides 4 different metrics

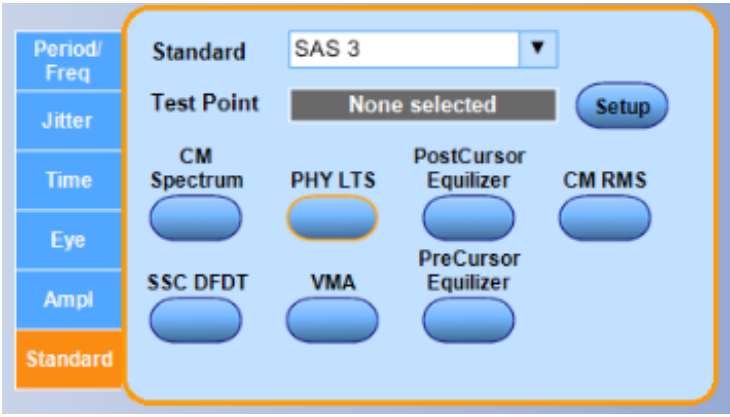
1. **Relative Vertical Eye Opening:** A direct indication of how much margin there is after equalization
   - Takes into account un-compensable ISI and crosstalk
   - ISI and crosstalk broken down in report
2. **Main Cursor Amplitude:** A direct indication of the amplitude after equalization
   - Assumes 800 mVppd max. TX launch amplitude, unless data is captured
3. **Maximal FFE correction**: A direct indication of how much FFE correction is required by the transmitter
   - Max(abs(Cpre/Ccntr,Cpost/Ccntr))
4. **Maximal DFE correction:** A direct indication of how much DFE correction is required by the receiver
   - Max(abs(DFE/Main))

Source: T10/11-234r1

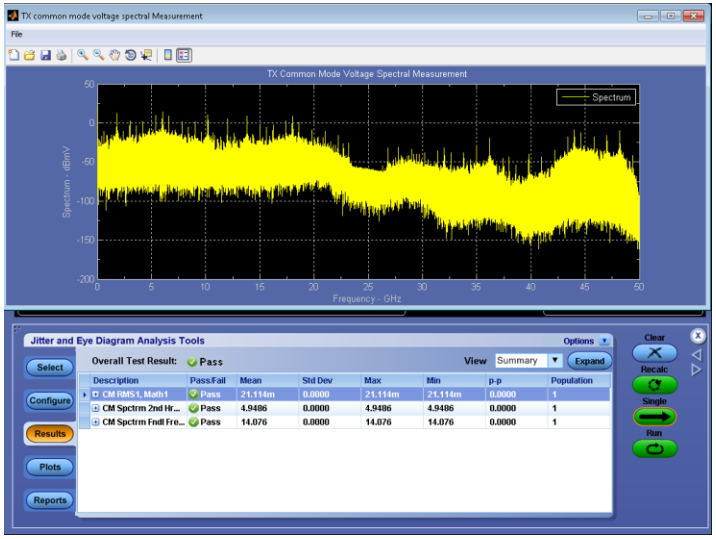
SAS-3 PHY Transmitter Solution – Option SAS3

Test0	Parameter	Conformance Min/Max
5.1.1	Maximum Noise During OOB IDLE	< 120 mV
5.1.2	OOB Burst Amplitude	> 240 mV
5.1.3	OOB Offset Delta	+/- 25 mV
5.1.4	OOB Common Mode Delta	+/- 50 mV
5.2.1	SSC Modulation Type	Center-, No- and Down-spreading
5.2.2	SSC Modulation Frequency	30 kHz < SSC_{freq} < 33 kHz
5.2.3	SSC Modulation Deviation	+/- 1000 ppm (center), 0 ppm (no spread) or +0/-1000 ppm (down)
5.2.4	SSC DFDT	850 ppm/µs
5.3.1	Physical Link Rate Long Term Stability	+/- 100 ppm
5.3.2	Common Mode RMS Voltage	< 30 mV
5.3.3	Common Mode Spectrum Mask Hits	Below Spectrum Limit Lines (0.1 to 6 GHz)
5.3.4	Peak to Peak Voltage	850 mV < Vpk-pk < 1200 mV
5.3.5	VMA	> 80 mV
5.3.6	Rise Time	> 20.8 ps
5.3.7	Fall Time	> 20.8 ps
5.3.8	Random Jitter	0.15 UI (12.5 ps)
5.3.9	Total Jitter	0.25 UI (20.8 ps)
5.3.10	SAS3_EYEOPENING	> 55 %
5.3.11	Pre Cursor Equalization	1 V/V < R_{pre} < 1.67 V/V
5.3.12	Post Cursor Equalization	1 V/V < R_{post} < 3.33 V/V

SAS3 12 Gb/s Tx Test Software



Common Mode Spectrum Measurement



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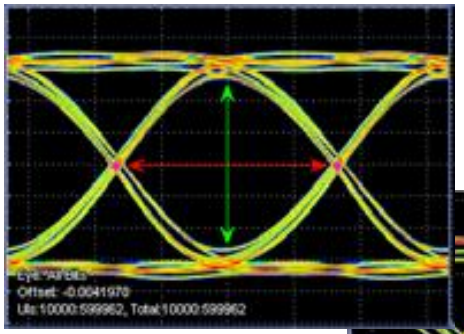
SAS-3 PHY Transmitter Solution – Option SAS3

- Automated transmitter validation for 12 Gb/s SAS physical layer specification
- Integrated SAS3_EYEOPENING measurement for accurate analysis of ISI and crosstalk effects and relative vertical eye opening after reference equalization
- Easily reconfigure existing measurements to create user-specified test parameters or test limits
- Multiple plots and measurement configurations provides a quick comparison of the same acquired data with different settings
- Simultaneous two lane testing of primary and secondary ports
- Detailed test reports with screenshots, setup details, and pass/fail limits

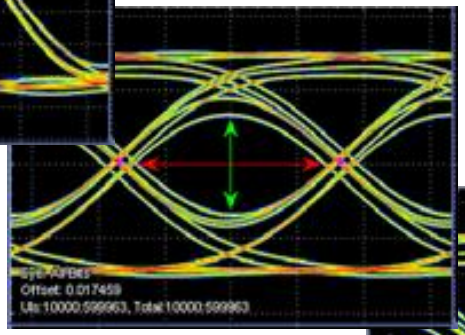
Beyond Compliance

- How much margin is there in my design?
- How many DFE/FFE taps are needed to meet the system budget?
- What is longest channel (cable/backplane) the system can tolerate?
- How does process/voltage/temperature affect device performance?

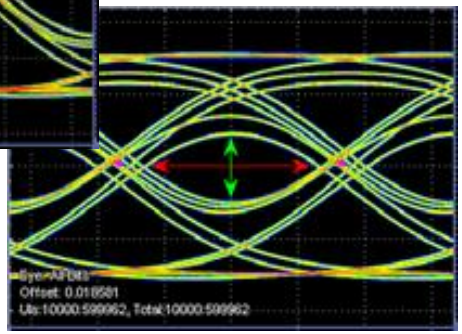
1m cable

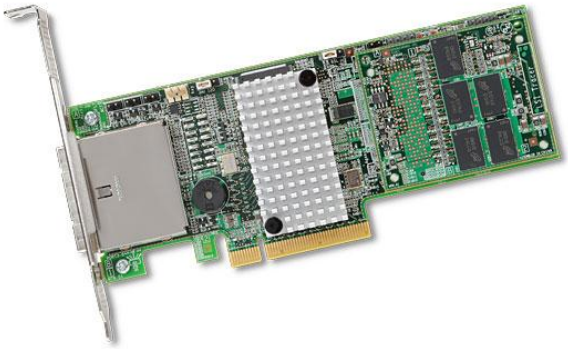


2m cable



3m cable





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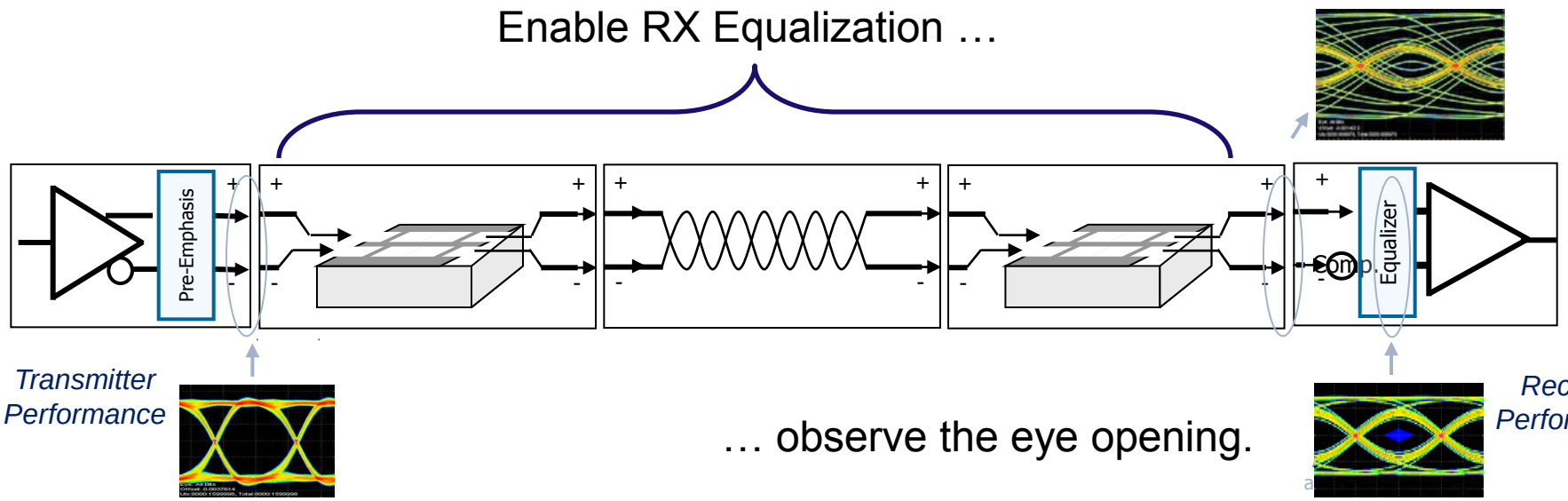
SDLA Overview
Receiver Equalization

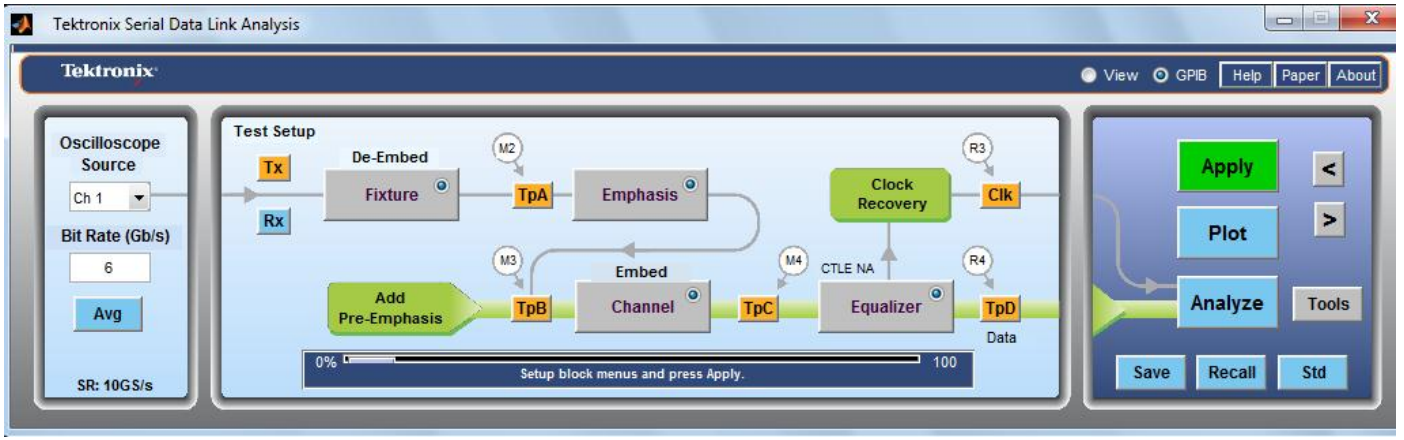
- Embedding the compliance channel or probing at the RX pins often results in a “closed” eye
  - The goal is to see the signal *inside* the Rx where the decision 0 or 1 is made by the comparator (aka the “slicer”).
- SDLA allows the user to insert different Equalizers (CTLE, FFE, DFE), then observe at the ‘virtual’ Rx.



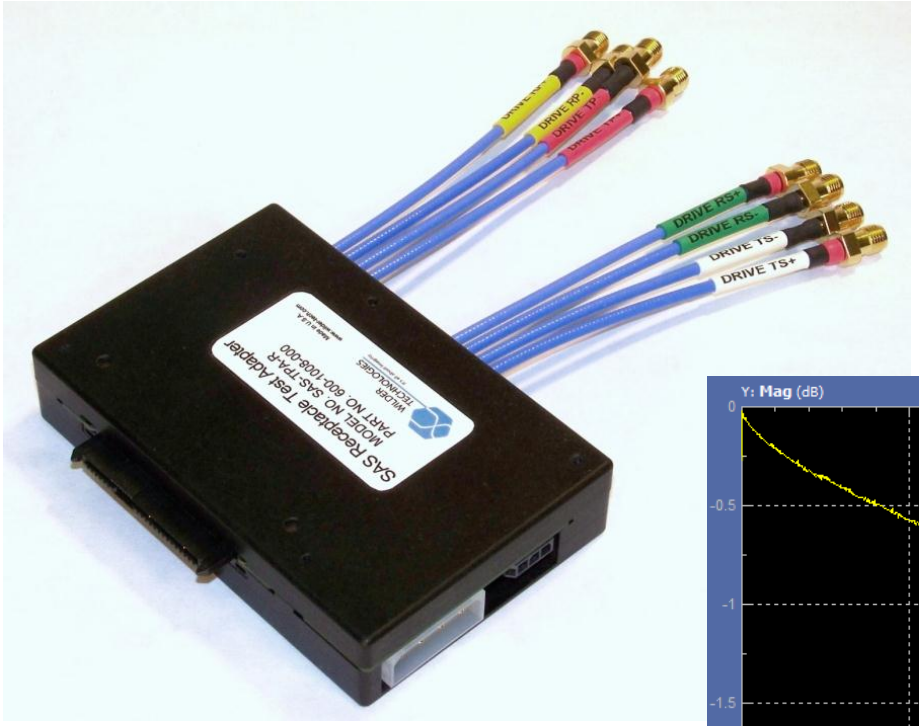
SDLA Overview

- **Oscilloscope Source:** Waveform from probe/scope
- **De-embed Block:** Remove fixtures, cables or channel elements
- **Emphasis Block:** Add or remove emphasis
- **Embed Block:** Add channel elements
- **RX Model:** Clock Recovery, CTLE, FFE/DFE
- **Test Points:** Virtual probe points (TpA, TpB, etc)
- **Analyze:** Measurements, Eye Diagrams with DPOJET

Complete visibility and analysis at multiple test points throughout the link



SAS Receptacle Test Adapter



Sdd21 (1x Thru) => -3dB@26 GHz

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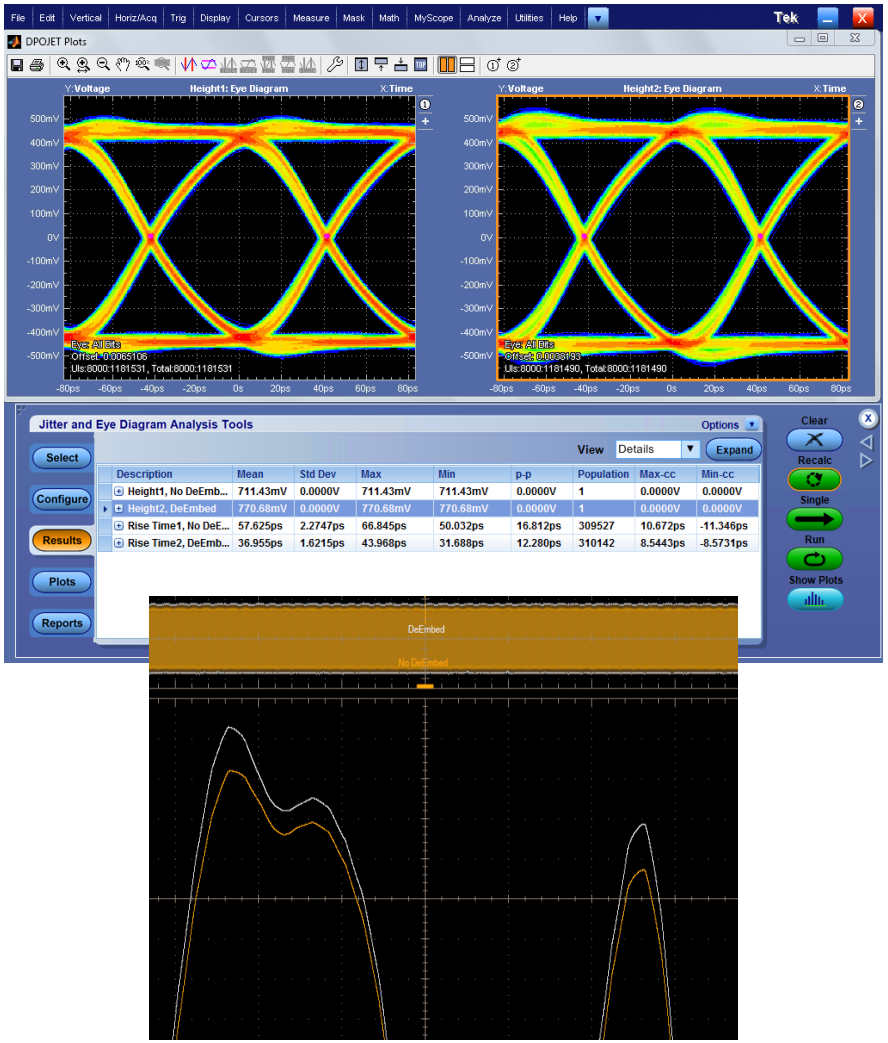
Test Fixture De-embedding

- Why de-embed?
  - Tx measurements referenced to die (ET)
  - Improve margin with removal of fixture effects
- S-Parameters acquired from calibration fixture or model extraction
- Use inverse response to compensate for loss

	Before De-Embed	After De-Embed
Eye Height	711 mV	770 mV
Rise Time	57	37

Before After



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Validate Equalizer

Analyze Raw Waveform

- On the scope, use cursors to measure the low frequency content of the signal on the acquired waveform (Math 1)
- In this example the low frequency content of the waveform is approx. 615mV

Validate Equalizer
Analyze Waveform After CTLE

- Based on the CTLE that was applied, we expect a 60% attenuation in the low frequency content after the CTLE
- This can quickly be verified, note the low frequency amplitude is approx. 240mV

Validate Equalizer: Analyze DFE

- Both waveform and eye diagram views of the signal after DFE are available
- The example shows validating the effects of DFE on a scope waveform
  - DFE will open the eye by approx 2 times the tap value
  - High frequency signal before DFE is 136mV and after 166mV, which is 2 tim

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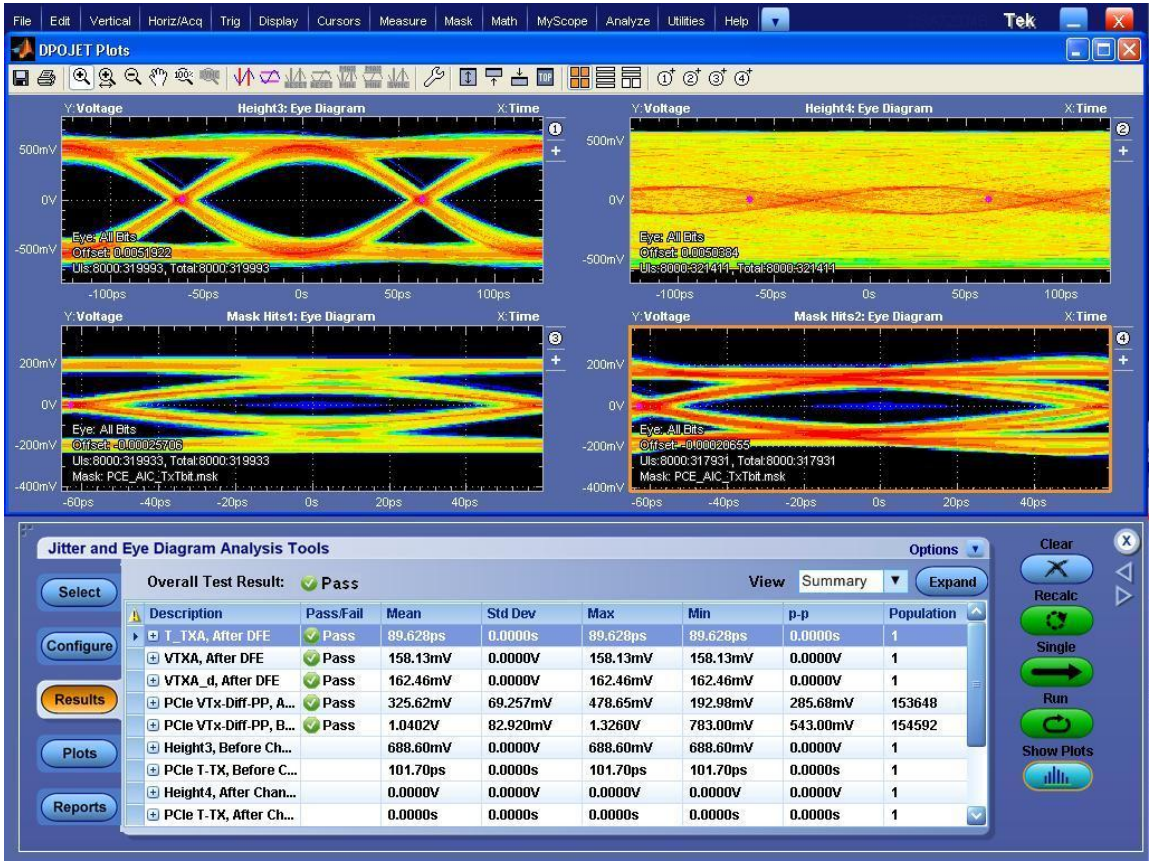
Complete System Visibility after Link Analysis

- After the waveform transformation is complete only SDLA/DPOJET provide simultaneous assessment of the signal at each point during the post processing stage to validate the effects



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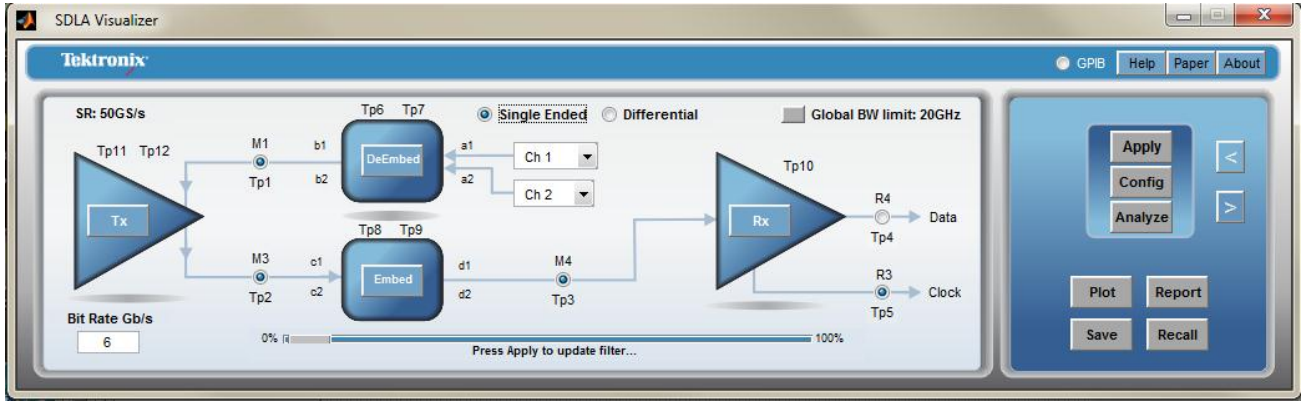
Emerging Requirements

- As data rates increase, new requirements are necessary for link analysis tools
  - Removing effects of test equipment in the context of the users DUT
  - Measuring at the pins of the transmitter or receiver while removing reflections caused by impedance mismatch
  - Allowing modeling of the DUT in absence of S-Parameters
  - Accurate modeling of silicon specific equalization algorithms
  - Plots and visual tools to validate the model
- Contact your Tektronix Account Manager for more details on how Tektronix can address these needs…



Recommended Equipment

The following components are required for performing SAS12 Tx measurements

- DSA/DPO/MSO70K(C/D) Series Oscilloscope with Opt. 5XL or higher (Min. 20 GHz BW, ≥25 GHz recommended*)
- DPOJET Advanced (DJA) - Prerequisite
- Option SAS3
- Test Fixtures:
  - TF-SAS-TPA-R SAS Gen3 Receptacle Adapter (drive form factor) or
  - TF-SASHD-TPA-R miniSASHD 12G SAS Receptacle (mini SAS HD 4i/x cables) or
  - Set of TF-SASHD-TPAR-P miniSASHD 12G SAS (Right Side) Plug and TF-SASHD-TPAL-P miniSASHD 12G SAS (Left Side) Plug (x8)
- PMCABLE1M or equivalent Phase Matched Cable Set (qty: 2)

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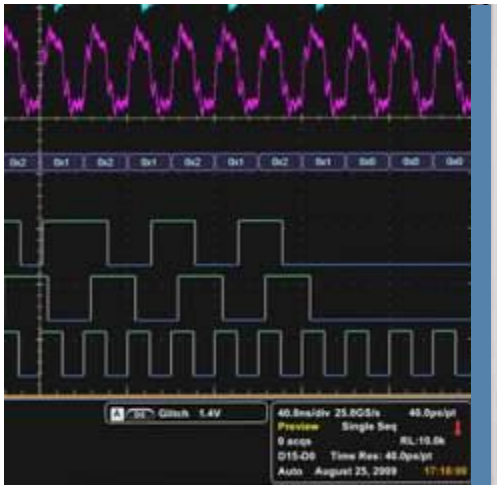
Serial ATA PHY Validation

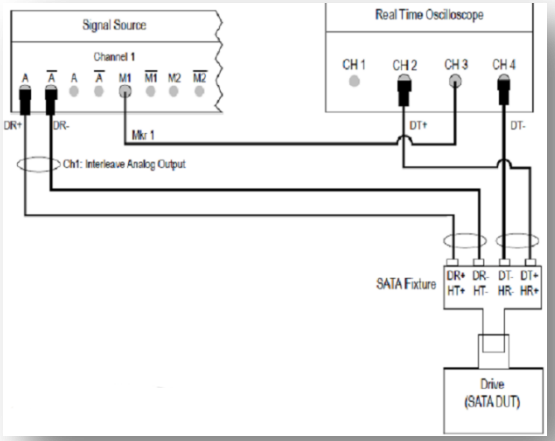


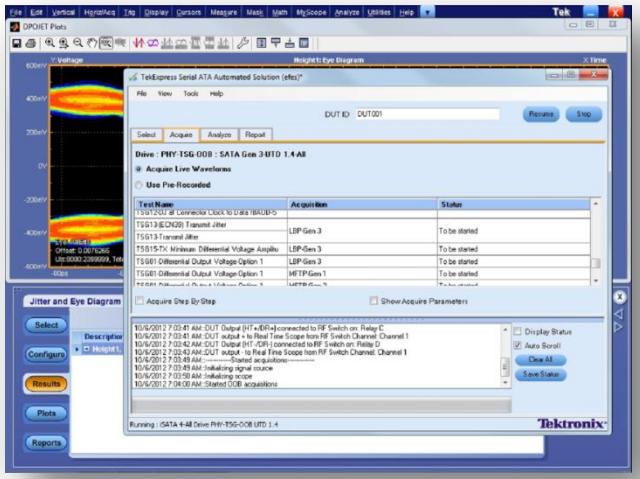
Basics of Serial ATA PHY Testing

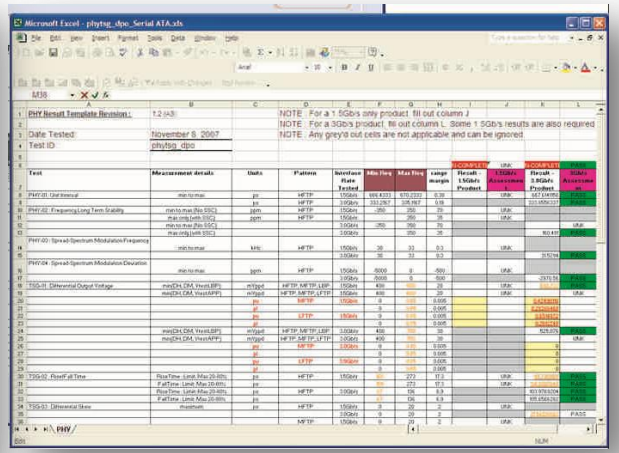
Startup
- Configure
- Calibrate

Validate
- Acquire
- Analyze

Report
- Save data
- Scorecard







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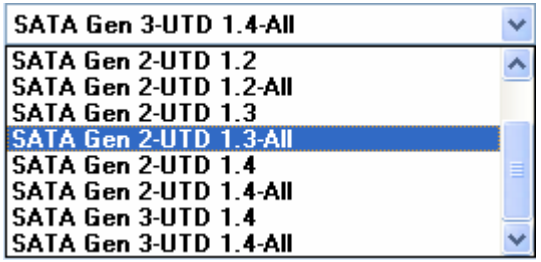
SATA UTD 1.4 TSG/PHY/OOB Measurements

Drive : PHY-TSG-OOB SATA Gen 3-UTD 1.4-All

Select	Test Name
☑	Informative-df/dt Measurement
☑	Informative-Eye diagrams
☑	OOB01-OOB Signal Detection Threshold
☑	OOB02-UI During OOB Signaling
☑	OOB03-COMINIT_RESET and COMWAKE Transmit Burst Length
☑	OOB04-COMINIT_RESET Transmit Gap Length
☑	OOB05-COMWAKE Transmit Gap Length
☑	OOB06-COMWAKE Gap Detection Windows
☑	OOB07-COMINIT Gap Detection Windows
☑	PHY01-Unit Interval
☑	PHY02-Frequency Long Term Stability
☑	PHY03-Spread-Spectrum Modulation Frequency
☑	PHY04-Spread-Spectrum Modulation Deviation
☑	TSG01-Differential Output Voltage-Option 1
☑	TSG01-Differential Output Voltage-Option 2
☑	TSG02-Rise-Fall Time
☑	TSG03-Differential Skew
☑	TSG04-AC Common Mode Voltage
☑	TSG05-Rise-Fall Imbalance
☑	TSG06-Amplitude Imbalance
☑	TSG09-TJ at Connector, Clock to Data, fBAUD-500
☑	TSG10-DJ at Connector, Clock to Data, fBAUD-500
☑	TSG11-TJ at Connector, Clock to Data, fBAUD-500
☑	TSG12-DJ at Connector, Clock to Data, fBAUD-500
☑	TSG13-Transmit Jitter
☑	TSG14-TX Maximum Differential Voltage Amplitude
☑	TSG15-TX Minimum Differential Voltage Amplitude
☑	TSG16-Tx AC Common Mode Voltage



- Different test program and degrees of regression testing user selectable.
- Debug and diagnostic tools (Informative measurements)
- Updated SATA Gen3 measurements
  - New OOB patterns
  - TSG ECN additions

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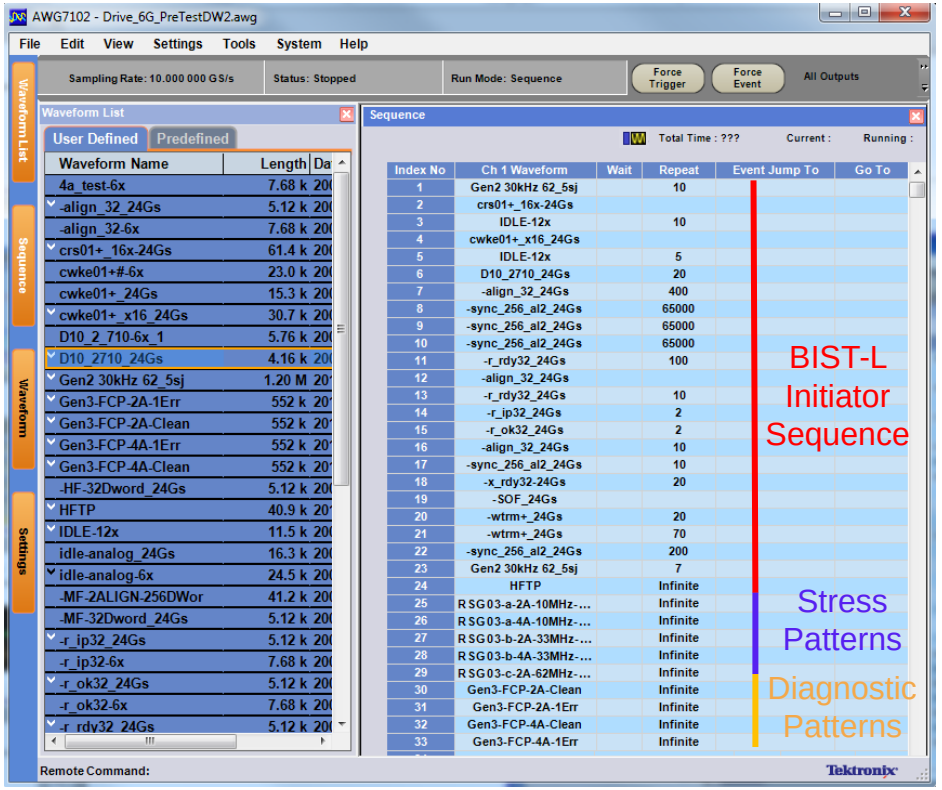
AWG Device State Control

Real Time Scope	DPO72004B (GPIB8::1::INSTR)
BIST-L initialization by	**Auto**
Set scope scale, resolution and sampling rate	Custom Utility Operation without AWG User Defined Batch Script
Set vertical scales automatically	
BIST-L validation required	Always
Number of times AWG is turned ON/OFF for putting DUT in BISTL mode	2
Horizontal scale for PHY-TSG BIST-L acquisition (us/div)	4
Resolution for PHY-TSG BIST-L acquisition (ps/pt)	20
OOB validation required	First time only

- DUT control a significant challenge
  - BIST-L (loopback) required for compliance
- AWG has a successful track record of DUT control
  - Initiates loopback while seamlessly transitioning to Tx/Rx testing
- 3rd party tools available (Drivemaster, serial port control)



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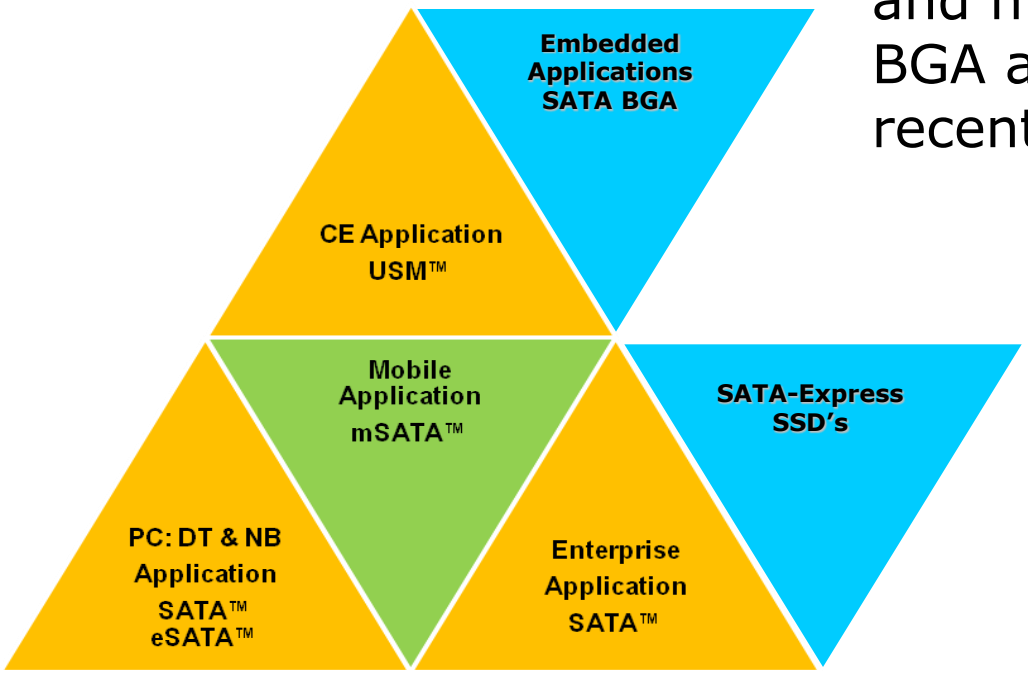
The SATA Ecosystem: Now



Today, SATA is expanding in specialized low power, compact and high performance areas with BGA and SATA-Express Solutions recently approved by SATA-IO.

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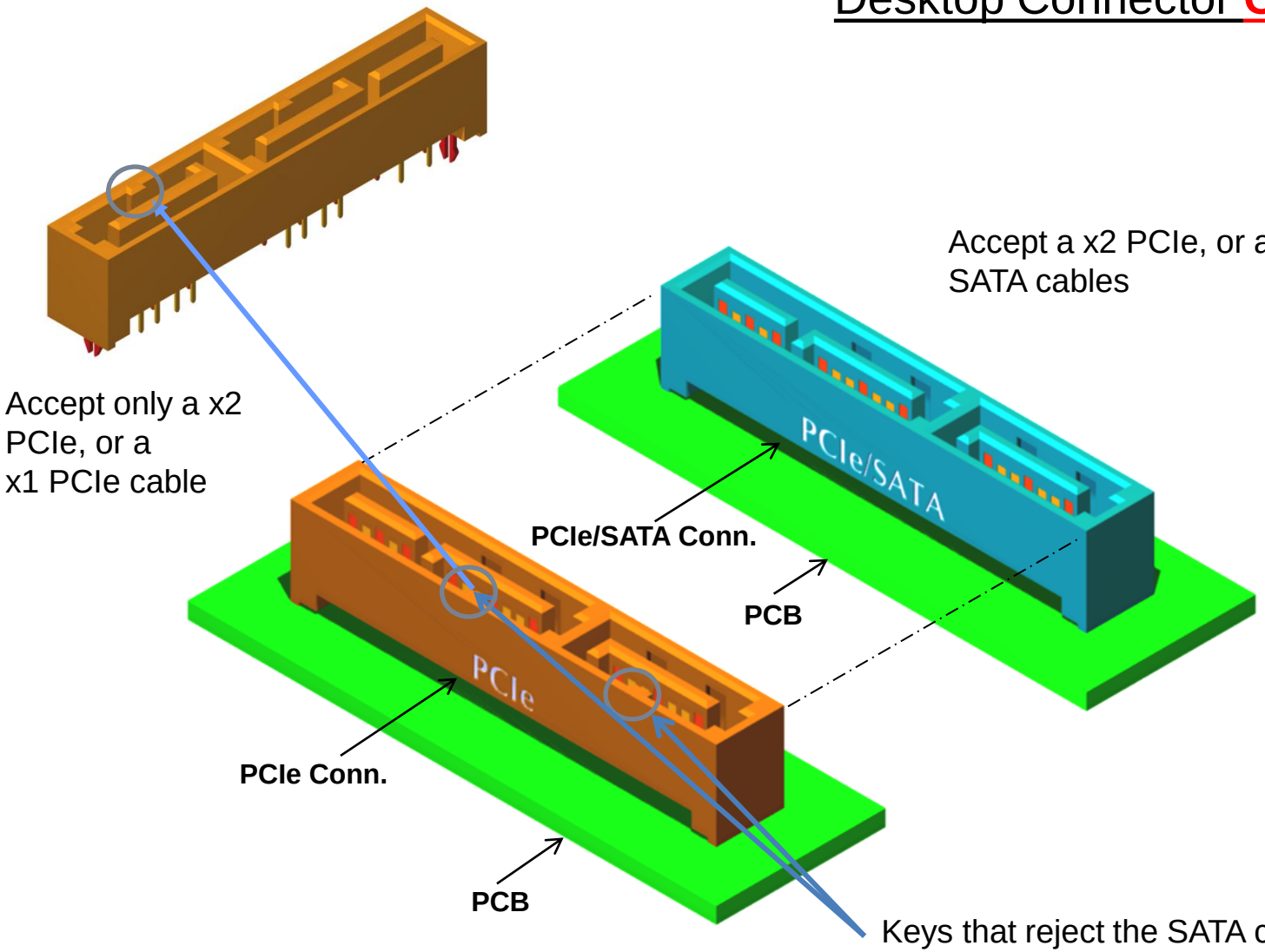
Enabling the New SATA Express Ecosystem

Desktop Connector **Concept**



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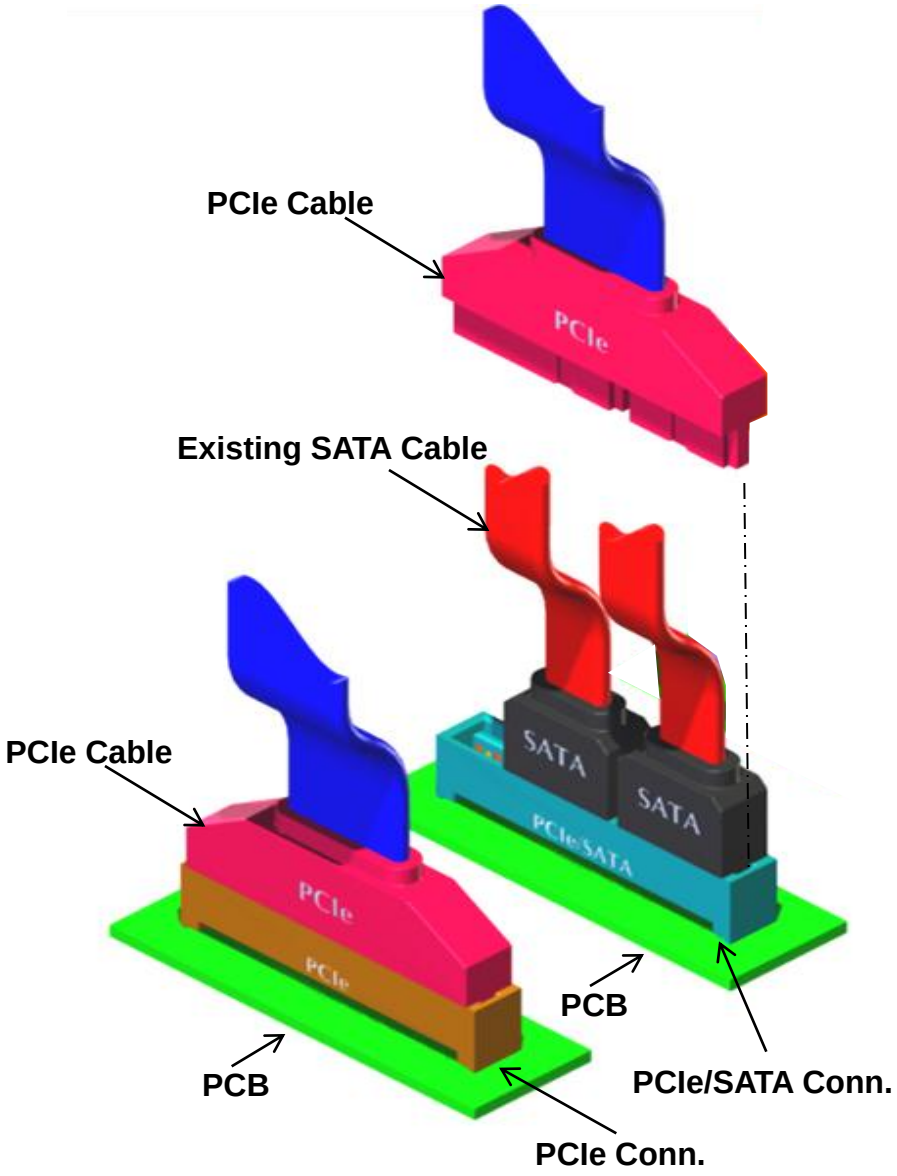
Enabling the New SATA Express Ecosystem



Desktop Cables **Concept**

- SATA devices will coexist with next generation PCIe devices
- SATA cost/performance benefits
- Requires a connector that supports both PCIe and SATA
  - Allows a single motherboard (backplane) connector to support both interfaces
- HDD-compatible form factors to be defined for PCIe devices
  - Enables system-level mechanical compatibility
  - Preserves high-capacity storage

SATA-IO CabCon has been chartered to develop SATA compatible connectors and form factors for PCIe SSD/hybrid drives

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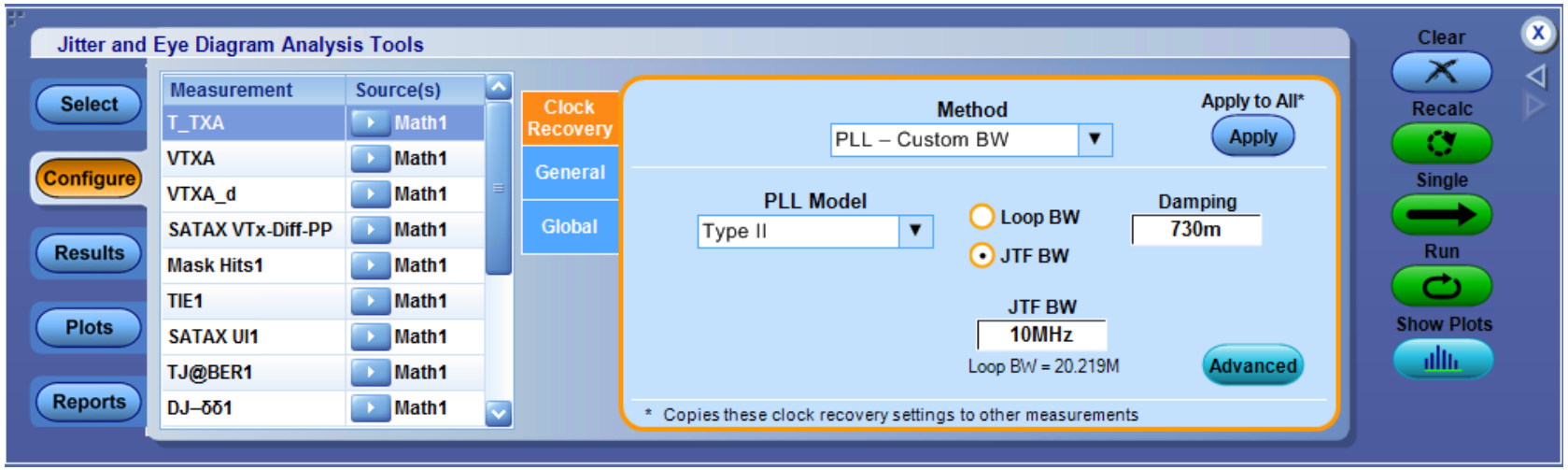
SATA Express = PCIe PHY Layer

- Tx Test parameters
  - Voltage
  - Package Loss
  - Transmitter Equalization
  - Jitter
- NEW Ref Clock Spec definition
  - Independent Ref Clock model
  - 2nd Order transfer function for SSC harmonics attenuation



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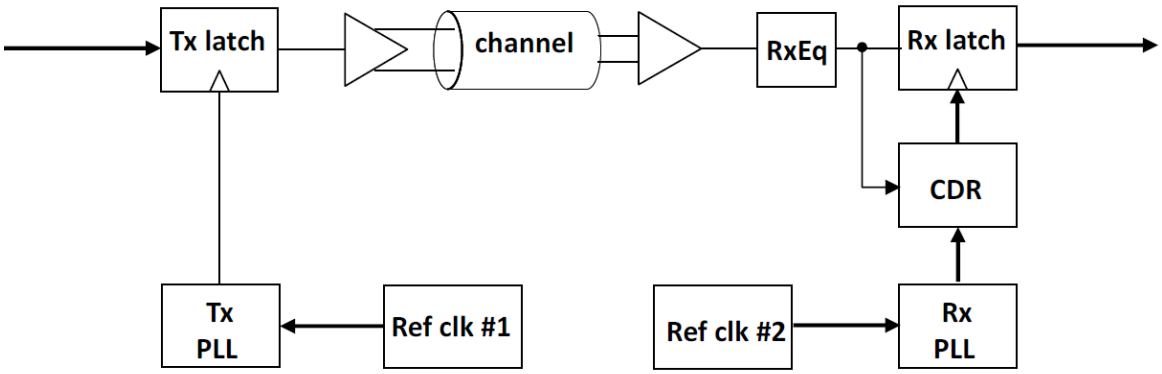
Clocking Architectures – PCIe vs. SATA

- SATA
  - Supports SSC
  - Embedded clock
- PCIe
  - Three different synchronization methods
    - Forwarded Ref clock
    - Data clocked Ref clock
    - Separate Ref clock
- Client PCIe application

  -> no need for "refclk“*



Independent Ref clock model for SATA Express

* PCI-SIG proposal under review

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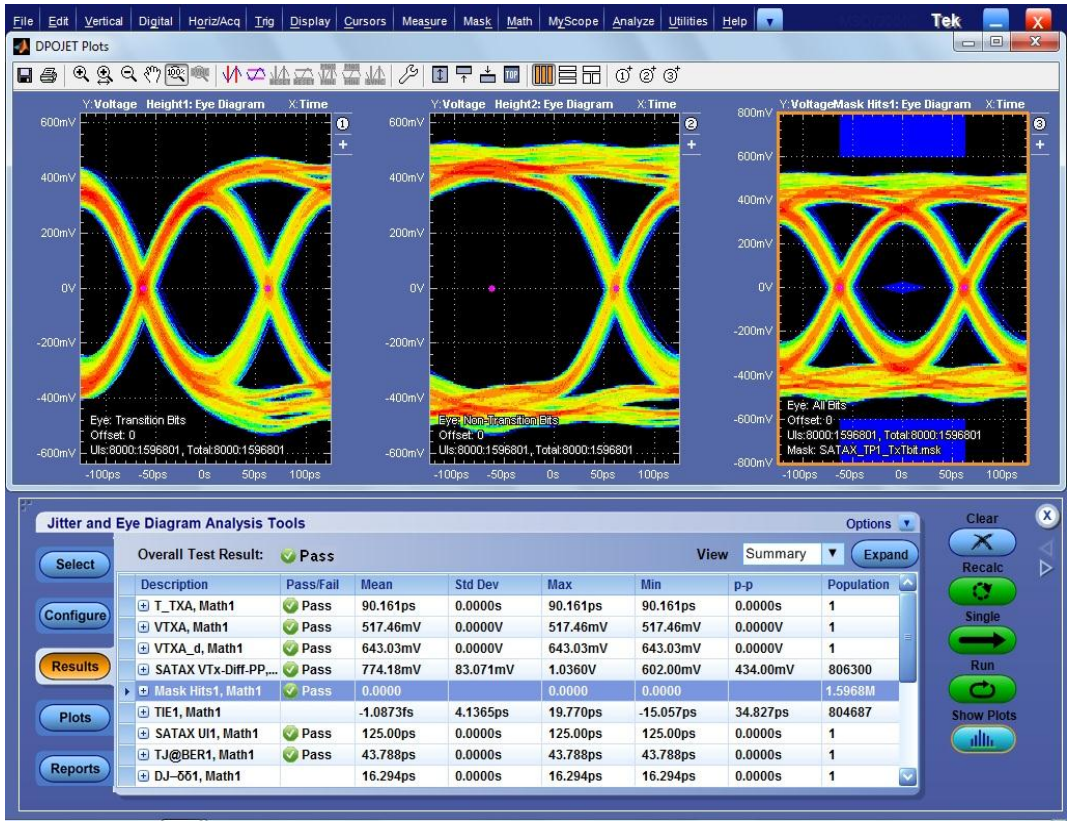
Tektronix Solutions for SATA Express Measurements

- DPOJET-based SATA Express setup (requires option PCE3)
- Support for Base/CEM spec measurements
- Supports all versions of PCI Express and includes SATA Express PLL configurations



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SATA Express Signal Access

- Recommend Luxshare-ICT Dual Port SAS fixtures (SFF-8482)
- Similar dimensions but different pinout
- For device testing use plug fixture (TF-4R21) to mate with SATAe plug
  - Both ports accessible (29 pin)
- For cable testing use receptacle fixture (TF-4P22) to mate with SATAe receptacle
  - Only port A is accessible (22 pin)

SAS Dual Port Plug Test Fixture

SAS Dual Port Receptacle Test Fixture

http://www.luxshare-ict.com/

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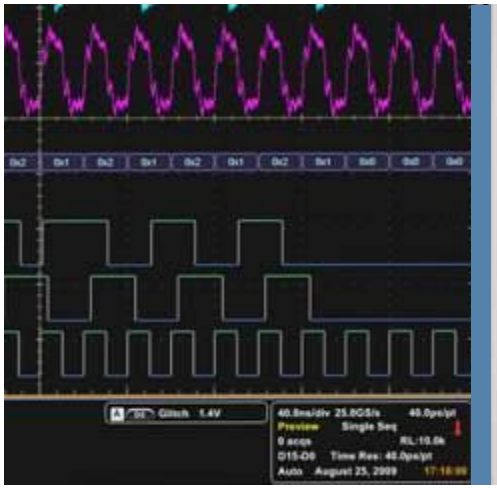
Simplifying Design, Debug and Validation of MHL Signals



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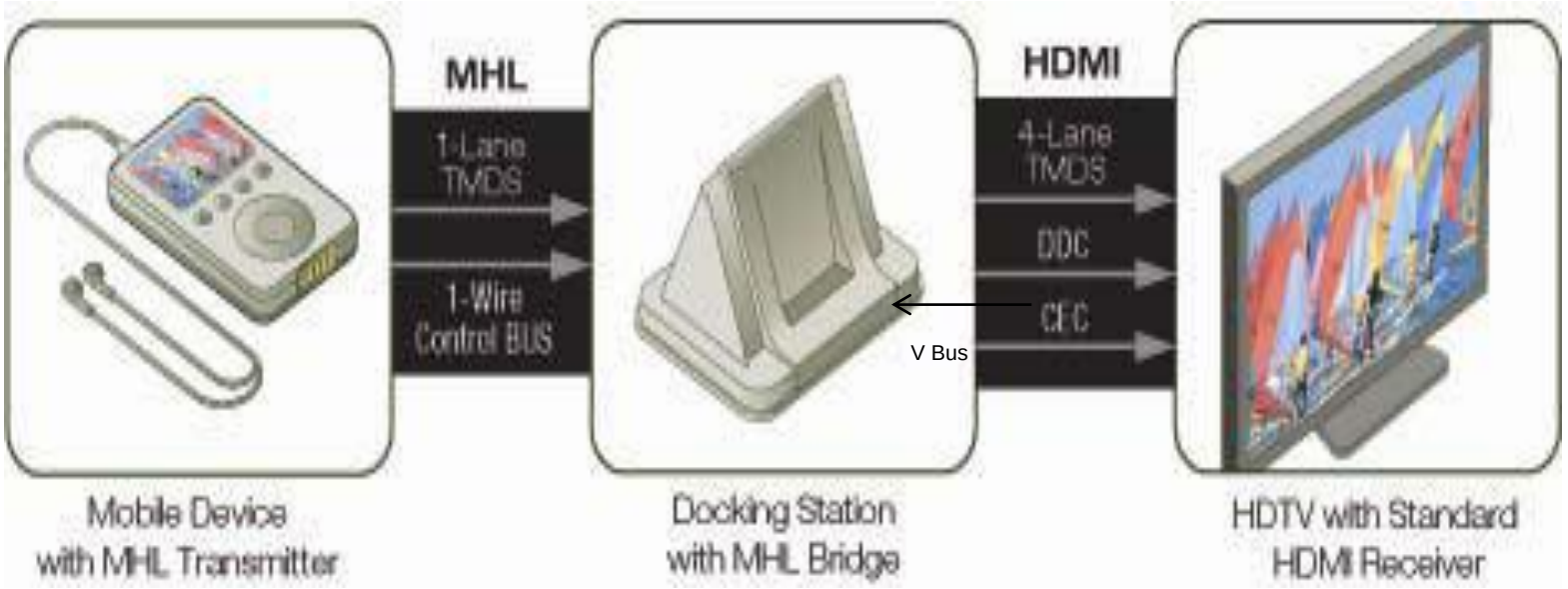
Tektronix is a Contributor Adopter for MHL CTS

Welcome MHL Adopters
BizLink Technologies, Inc.
www.bizlinktech.com
Cable Assemblies and Wiring Harnesses
Compal Electronics Inc.
www.compal.com
Electronics manufacturer of notebook computers and monitors
Explore Microelectronics, Inc.
http://www.epmi.com.tw
Fabless company developing high-speed interface ICs
Fairchild Semiconductor
www.fairchildsemi.com
Delivers semiconductor solutions for power and mobile designs
Hosiden Corporation
www.hosiden.com
Manufactures and sells electronic components, electromechanical parts and LCD elements
Johnson Component and Equipment Co., Ltd.
www.jcecable.com
Cable Manufacturer
Niketech Electronic Corporation
www.niketech.com.tw
Provider of connectors for the electronics industry
Parade Technologies, Inc.
www.paradetech.com
Develops and supplies advanced and cost-effective high-speed display interface solutions
Sumitomo Electric Industries, Ltd.
global-sei.com
Designs, manufactures and sells cable and components and advanced electronic devices
Sunplus Technology Co., Ltd.
www.sunplus.com
Provider of multimedia IC solutions
Sure-Fire Electrical Corporation
www.sure-fire.com.tw
Global OEM/ODM supplier of cables, connectors and devices
Synopsys
www.synopsys.com
Provider of electronic design automation (EDA) software, IP and services
Tektronix
www.tek.com
Test, measurement and monitoring solutions
YFC-BonEagle Electric Co., Ltd.
www.cables.com.tw
Manufactures power cord sets, LAN cable, patch cords and networking accessories

MHL Introduction



- Mobile HD Link (MHL) technology is a low pin count HD audio and video interface that connects portable electronics devices such as mobile phones, digital cameras, camcorders and portable media players, to HDTVs.
- The technology allows mobile devices to output digital 1080 Full HD resolution via the existing mobile connector without the real estate and cost of another dedicated video connector.
- Together with an MHL-to-HDMI bridge, the MHL-enabled mobile device becomes a fully compliant HDMI source and can connect to the television's standard HDMI input port.

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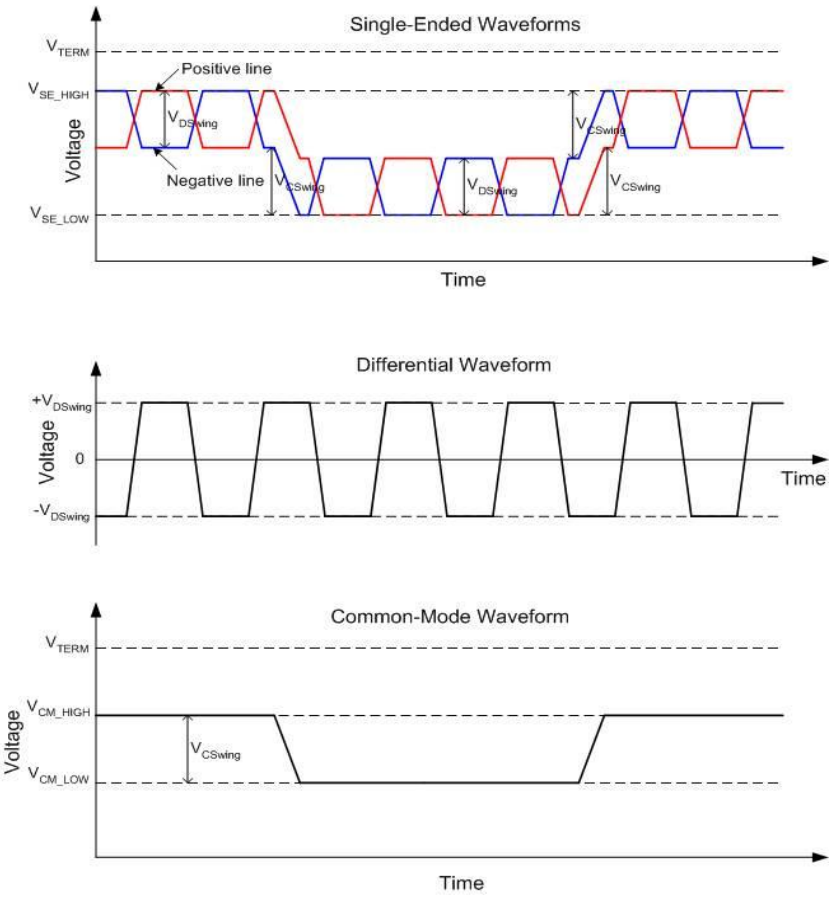
MHL Signal Complexity

- MHL Consortium was formed in Sept 2009 with the following founding members:
  - NOKIA
  - SAMSUNG
  - Silicon Image
  - Sony
  - Toshiba
- The Specification 1.1 version was announced in Q12011 and Specification 1.2 in Feb 2012.

  The Consortium released CTS 1.1 version in June 2011. CTS 1.2 is just announced.

  COMPLETE TEKTRONIX SOLUTION APPROVED in CTS1.1 and CTS 1.2.
- Tektronix is a Contributor adopter and actively involved in defining the CTS.



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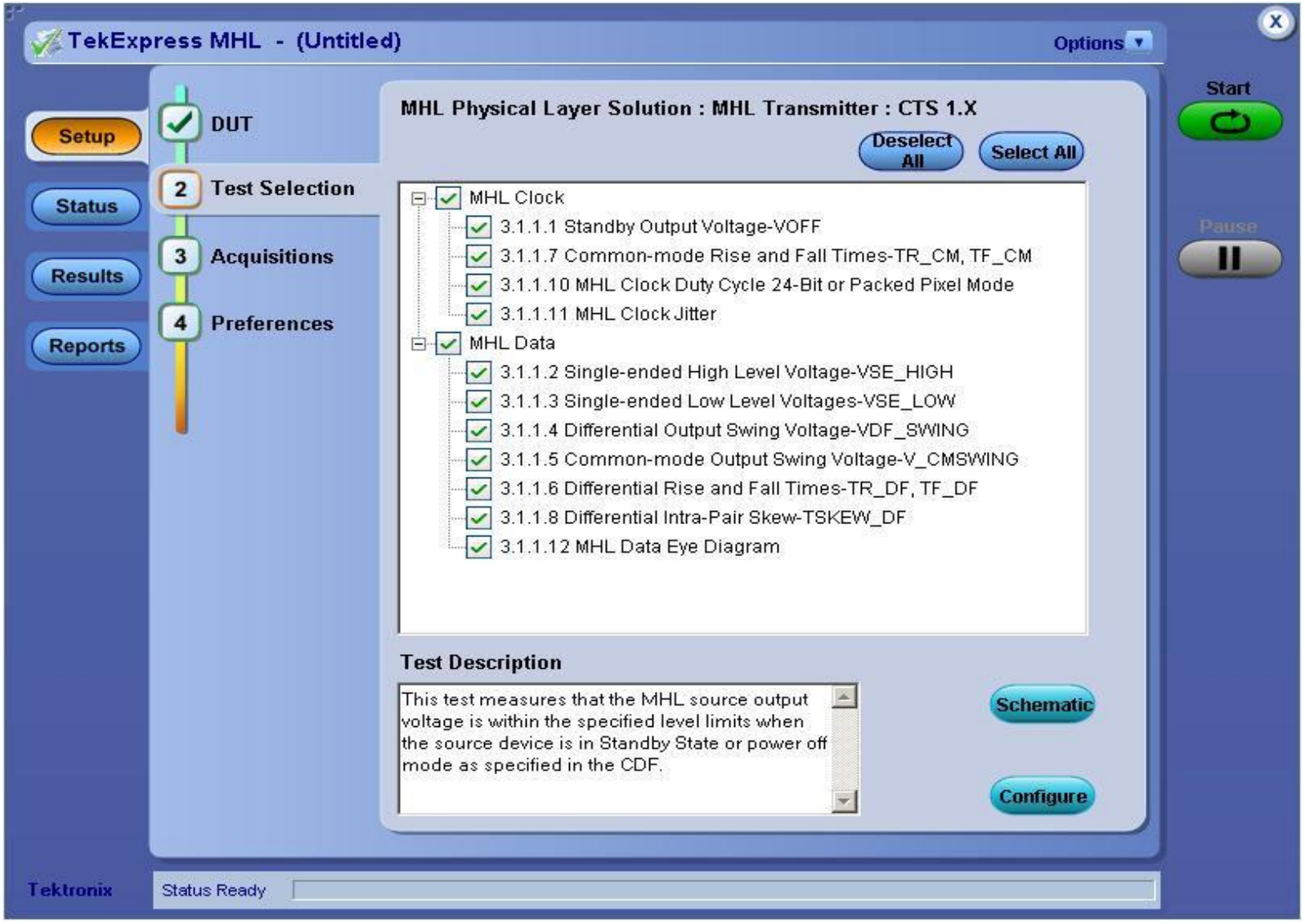
MHL Compliance Software for Automated Tx Tests: Option MHD



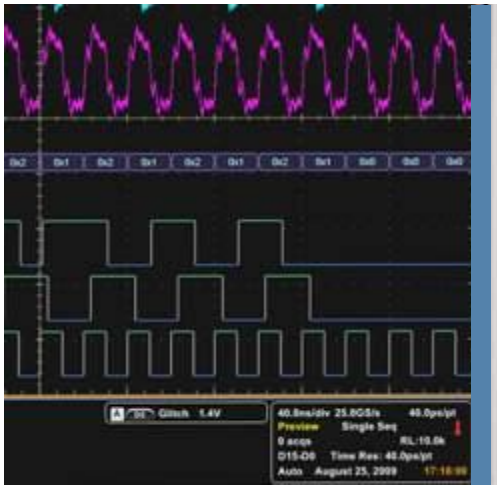
Tektronix MHL Solution

- DPO/DSA/MSO 70804B/C Series Real Time Oscilloscope with BW ≥ 8GHz
- MHL Compliance Software – Option MHD
- Innovative MHL Protocol Software from Third party – TEK-PGY-MHL-PA-SW
- Probes – P7313SMA (two) and P7240 (one)
- MHL Test Fixture – Available from Tektronix.
- AWG7122C with Opt 01,02 or 06 and 08 for the innovative direct Synthesis based MHL Rx/Dongle testing.
- AWG7122C based Sink and Dongle Protocol tests(manual method)
- C-Bus Sink and Source board is needed and is available from Simplaylabs
- DSA8200 or Equivalent with 80E03/80E04 and I-Connect Software for MHL cable testing (performed manually using MOIs)

Please contact local Tektronix account managers for further details.

Innovative MHL Protocol Analyzer Solution

Introducing Tektronix' MHL Protocol Solution



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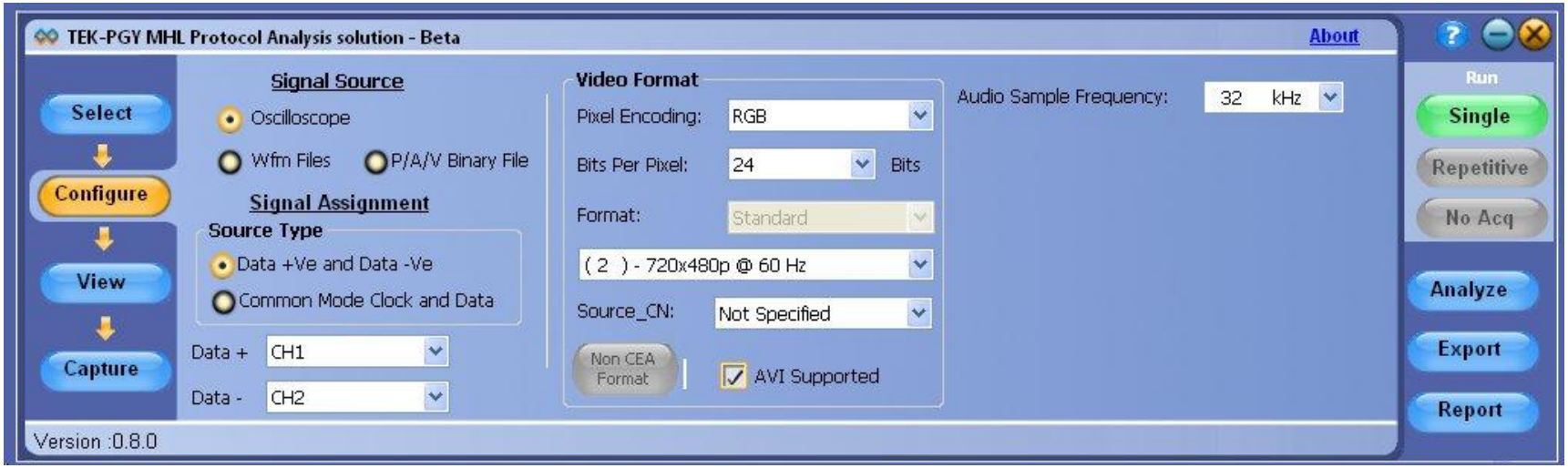
Tektronix MHL Protocol Analyzer



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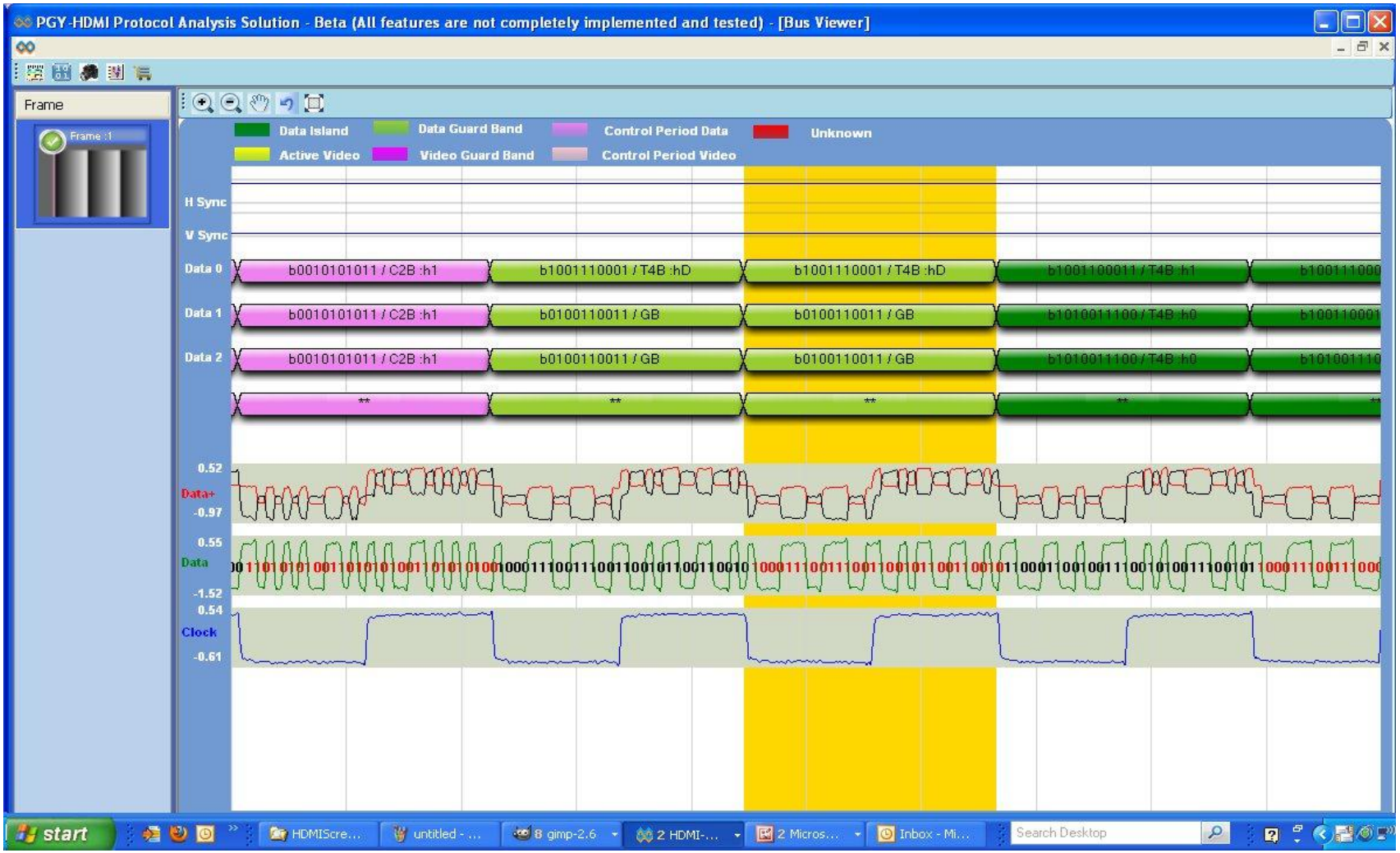
Tektronix MHL Protocol Analyzer: Seamless PHY and Link Layer Testing



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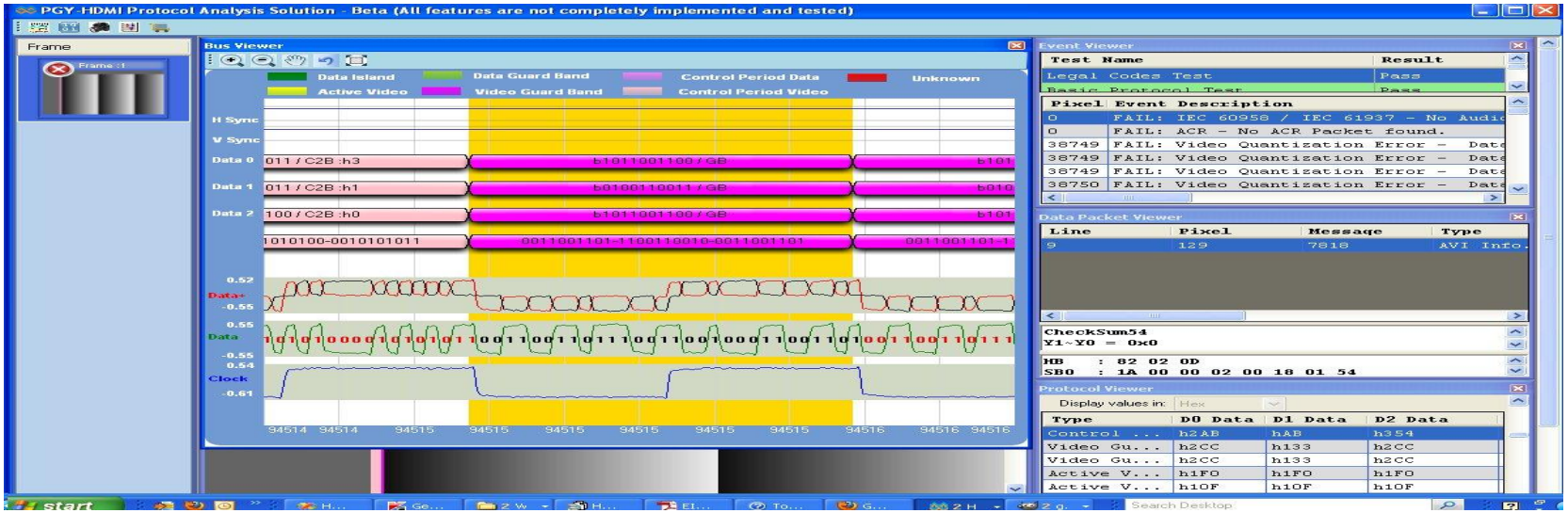
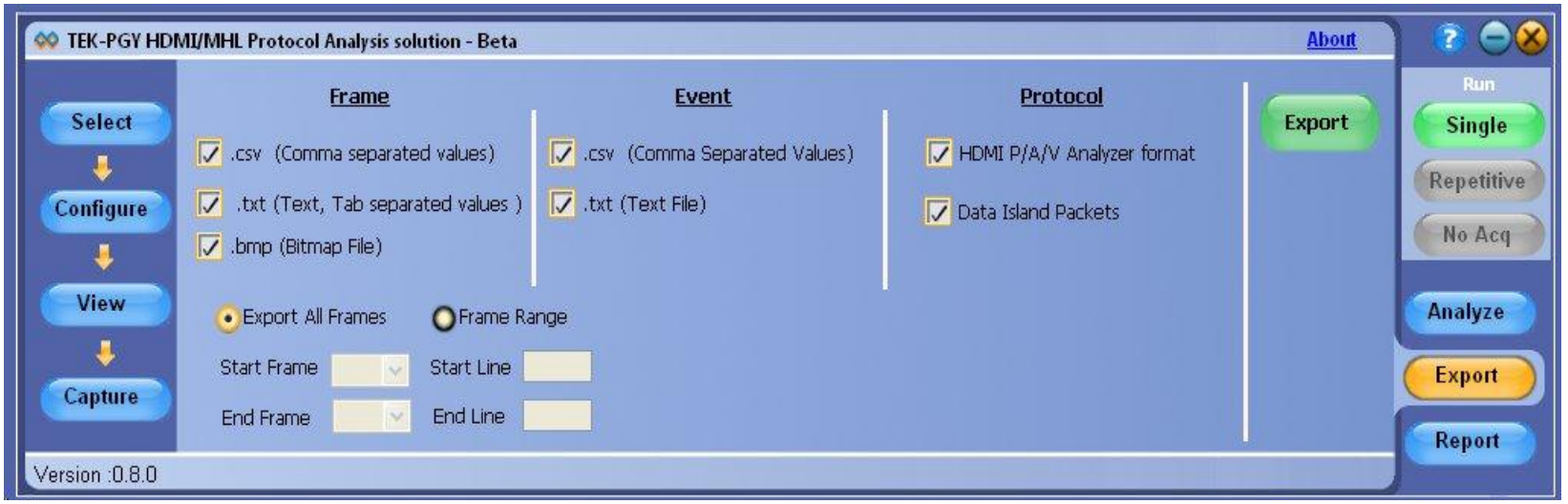
Tektronix MHL Protocol Analyzer





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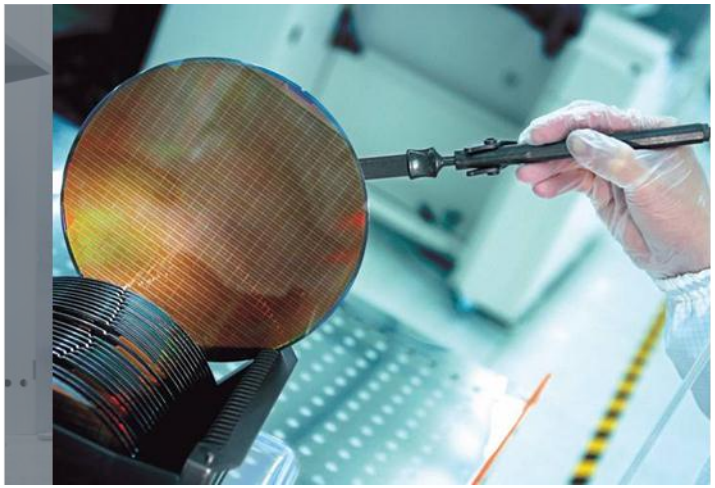
28G工用高速串行数据链路Rx/Tx测试

泰克



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Rx/Tx测试挑战

- 挑战.
  - 多种25 Gb/s - 28 Gb/s标准(IEEE802.3ba 100GBASE-*R, OIF CEI VSR, MSR, 32GFC)要求200 fs级测量和300 fs级系统BERT+Scope信号，以检验电接口单元和光接口单元(RX和TX)的性能
- 建立迎接主要挑战的解决方案
  - 全面的基于电接口和基于光接口的测试解决方案要求仪器同时跨越采样示波器技术和BERT技术，以确保规范要求的超低数值，如100GBASE-LR4规范第87节

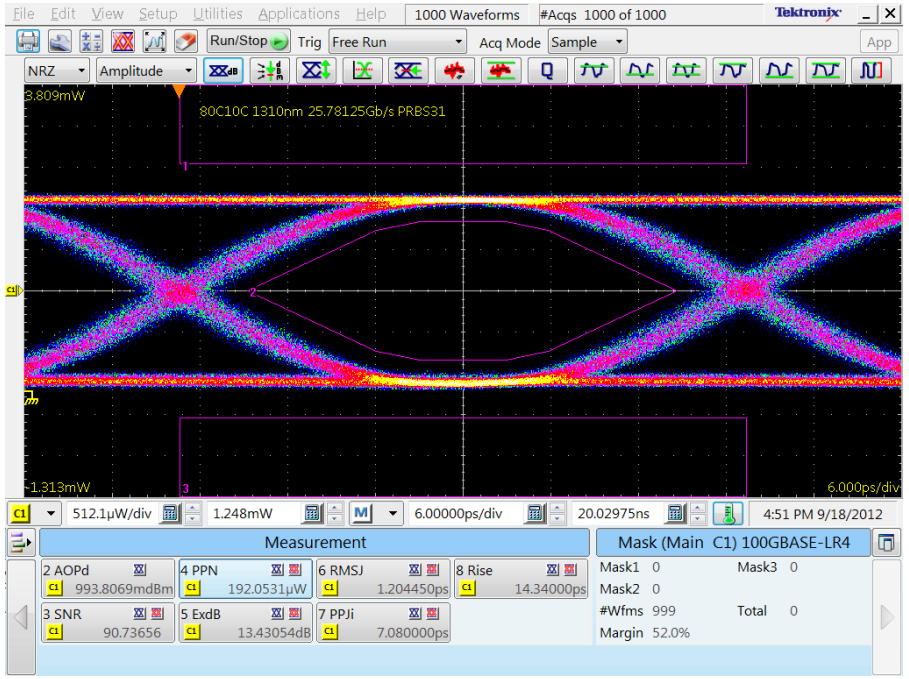
100 Gb/s TX物理层测试

- 挑战: 准确复现实际信号特点
  - 28 Gb/s的三阶谐波是42 GHz; 希望实现50 GHz
  - 动态范围：VECP要求50 dBm的动态范围
- 挑战: 光接口和电接口信号上的抖动
  - <100到<200 fs成分指标
  - 300 fs电接口系统指标
  - 400 fs光接口系统指标
- 挑战: 并发捕获电接口信号和光接口信号
  - 内置光电转换系统
  - 光接口信号的BER轮廓测试和物理层检验

以太网：40GBASE-LR4, 100GBASE-LR4/ER4测量

与**10GBASE-*R**单模光学系统类似
新规定的内容有：

- **19.34 GHz**光学**参考接收机**; **10 MHz PLL LBW**时钟恢复
- **模板** – 802.3ae成比例版本。泰克以文件方式提供**25和28 Gb/s新模板**
- 模板 – **命中率**0.005%; **在示波器数学运算中计算** (详情请联系泰克公司)
- **TDP**, 发射机色散代价: **与802.3ae类似**



100GBase-LR4模板测试
DSA8300 & 80C10C-F1
参考接收机

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抖动测量使用 – J2, J9和10^{-15}的BER:

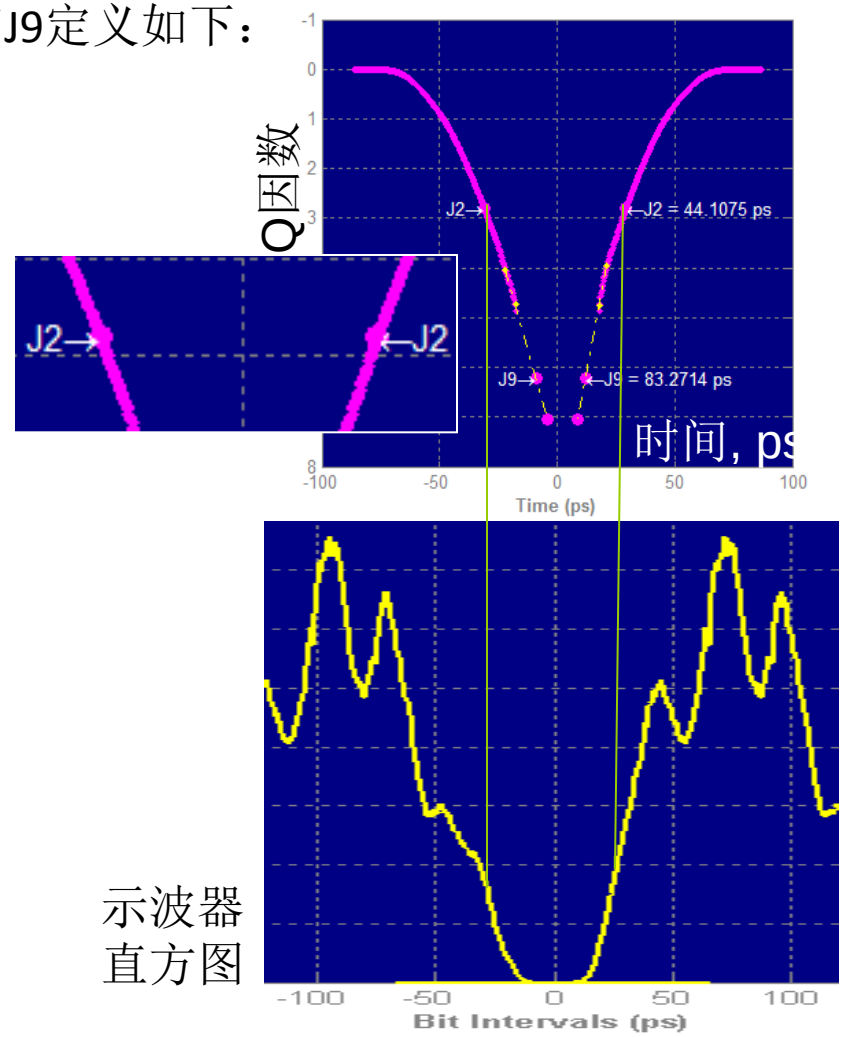
标准采用**J2** 和 **J9** 抖动测量
测量数据用来定义**压力眼图**，用于**nPPI**相关测量
下面讨论了这些测量。

抖动方法：J2和J9抖动 – **J2**

- IEEE 802.3ba要求J2和J9抖动测量，J2和J9定义如下：

IEEE 802.3ba 86.8.3.3.1 J2抖动

J2 抖动定义为包括10^{-2}以外所有抖动分布的时间间隔，其为抖动直方图0.5%处到99.5%处的时间间隔。这可以使用示波器测量，或者如果通过绘制BER随判定时间变化曲线测验量，那么J2是**BER等于2.5×10^{-3}**的两点之间的时间间隔。示波器直方图应包括至少 10,000次命中，应在大约1%的信号幅度上获得。测试码型是**PRBS31**, Scrambled Idle或实时业务。

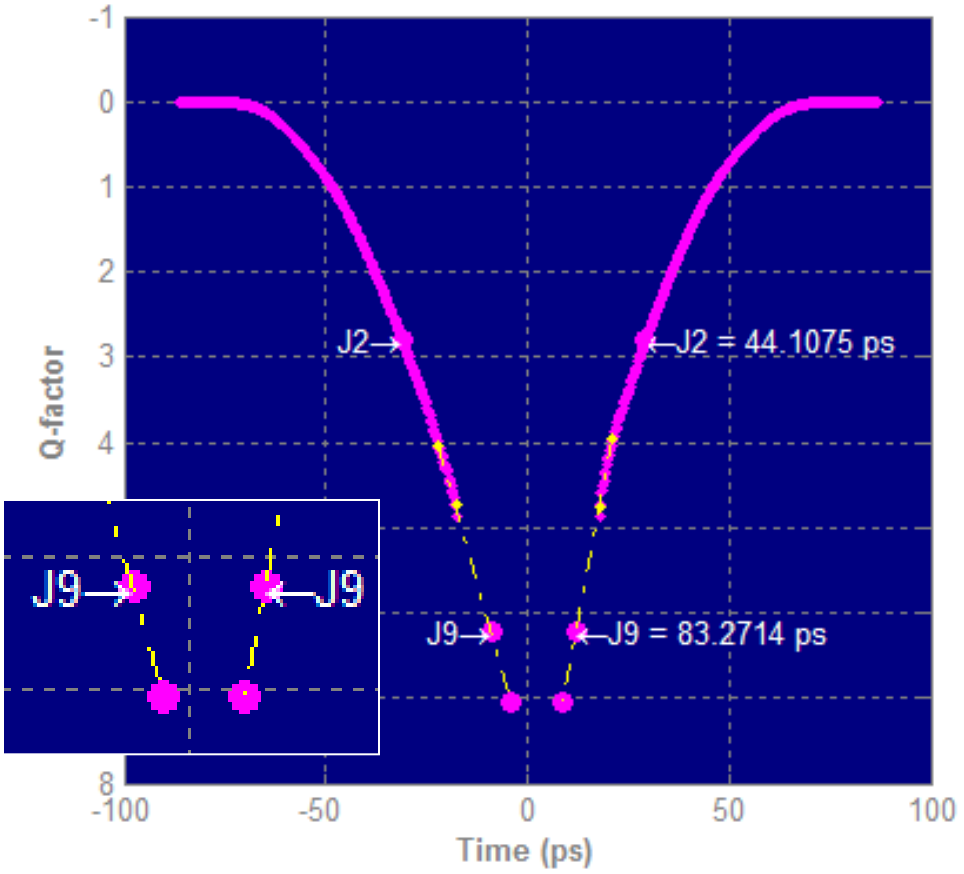


示波器直方图

抖动方法：J2和J9抖动 – **J9**

IEEE 802.3ba 86.8.3.3.2 J9抖动

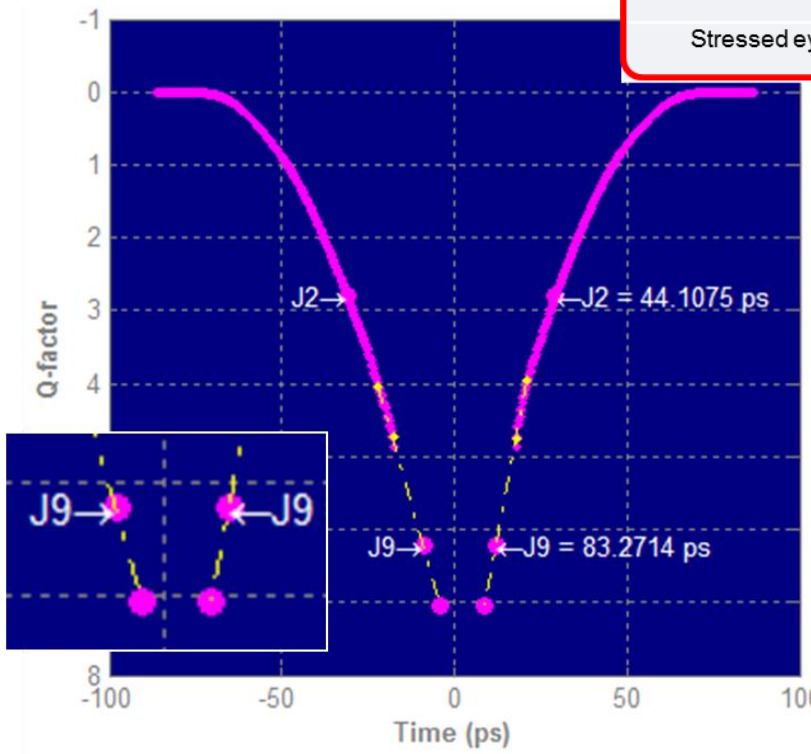
J9 抖动定义为包括10^{-9}以外所有抖动分布的时间间隔。如果通过绘制BER随判定时间变化曲线测验量，那么J9是**BER等于2.5×10^{-10}**的两点之间的时间间隔。测试码型是**PRBS31** 或Scrambled Idle。

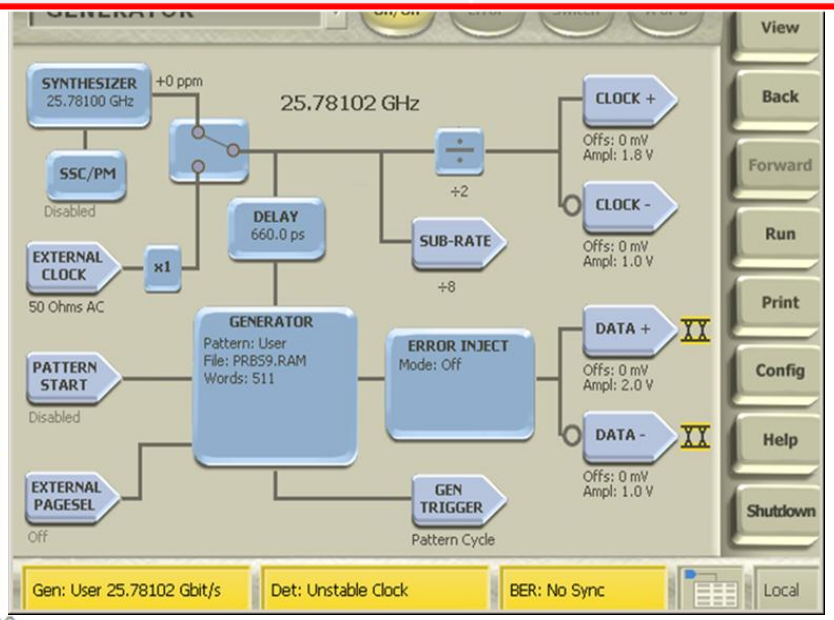


BERTScope作为信号源与DSA8300采样示波器作为示波器的组合

- 标准面临的挑战.
  - 器件检定要求需要精密的200fS级Tx测量成为主流，Rx检定需要类似的低抖动激励信号。除电接口验证外，光接口测试对检验100G系统的性能也至关重要。
- 我们有哪些解决方案、产品或应用可以解决主要挑战
  - 泰克拥有基于电接口和光接口的完善的解决方案，涵盖了采样示波器和BERTScope系列。

Conditions of stressed receiver sensitivity test		
Vertical eye closure penalty,f each lane	1.8	3.5
Stressed eye J2 Jitter,f each lane	0.3	
Stressed eye J9 Jitter,f each lane	0.47	

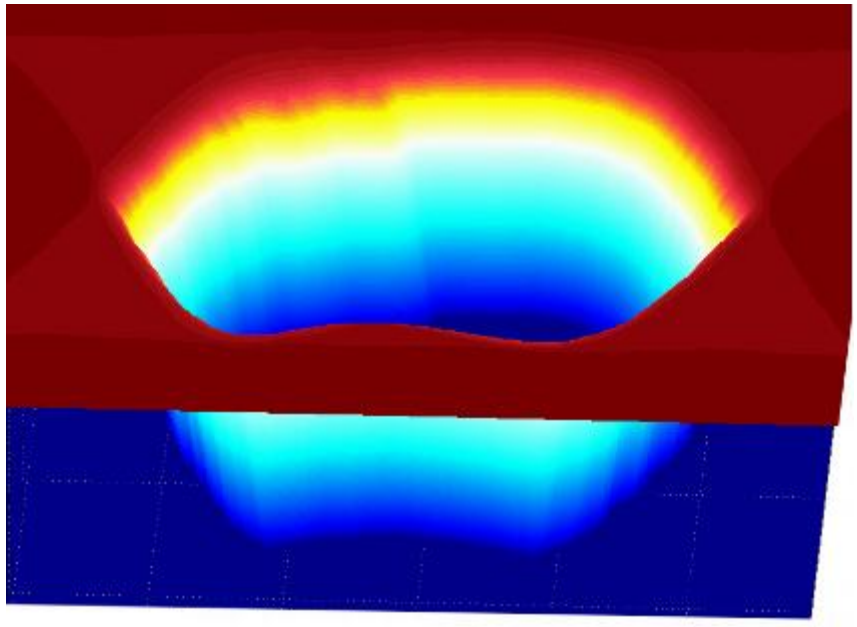




抖动方法：J2和J9抖动
示波器测量工具: **80SJNB**

- **80SJNB**, 适用于采样示波器的优秀抖动工具，由于采样示波器的**低噪声和抖动本底**，可以以优异的结果测量和**分解抖动**。
- 提供了**所有**PJ, RJ, DDJ, DCD, Dual Dirac模型, PWS, TJ, ***和*J2, J9**, 以及**噪声成分。**
- 全面分析要求被分析数据**短的、可重复的**码型。

- 在没有为J2和J9测量提供这种码型时，就需要一种**不同的方法**



小结: 80SJNB中的分析功能:
优秀的抖动工具,
但要求码型

80SJARB: 80SJNB配套工具: 在信号是PRBS31, 随机数据时是一种采样抖动工具

80SJARB应用软件

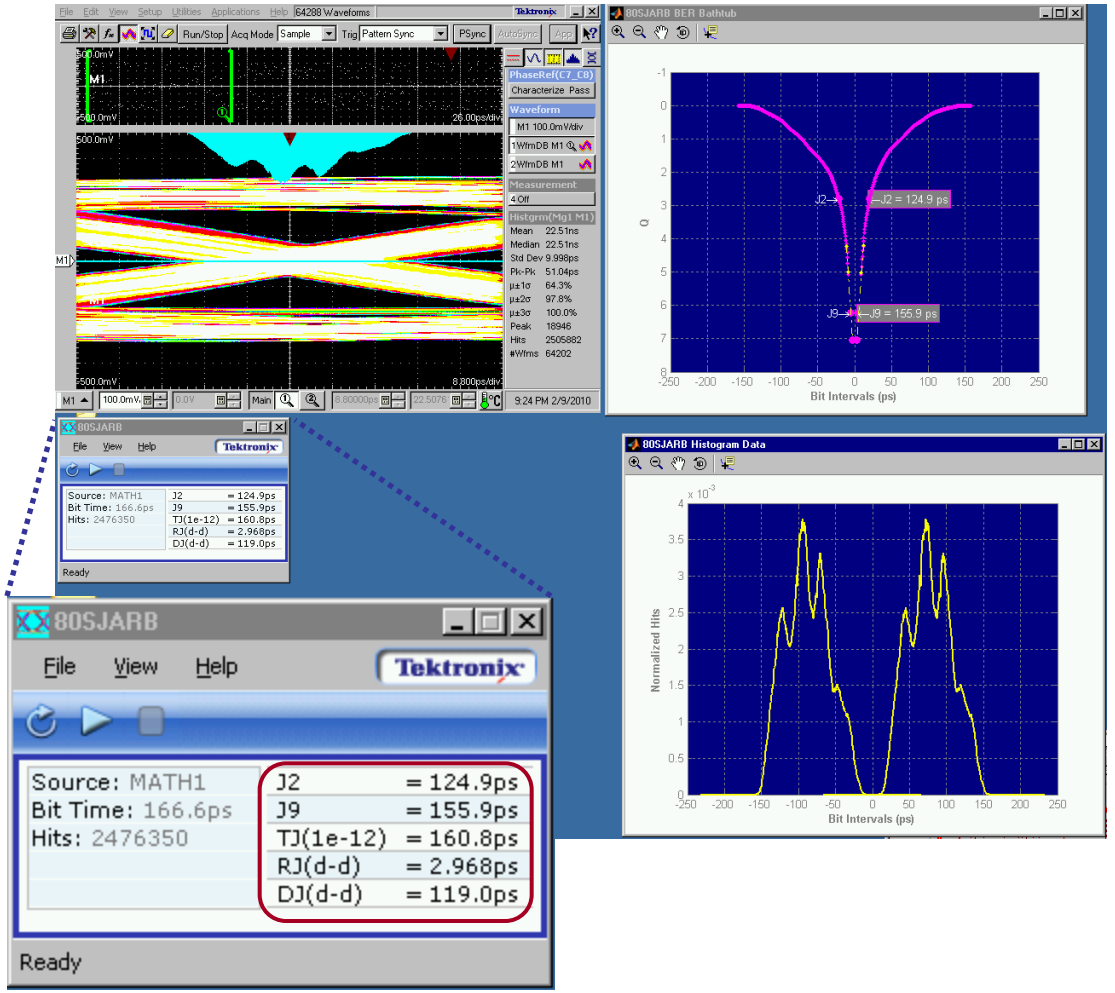
80SJARB **测量随机数据上的抖动** 及长码型 (如**PRBS31**)，报告:

J2

J9

$DJ_{\delta\delta}$, $RJ_{\delta\delta}$, (Dual Dirac)

TJ @ BER= 10^{-12}抖动



谢　谢！