Compliance Program Update

Allion / James Ou

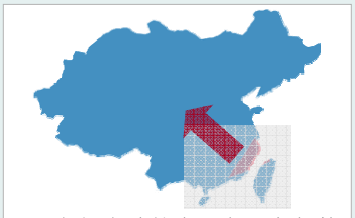
公司简介

Allion Test Labs, Inc / 百佳泰股份有限公司

Allion Seal-
Proof of Quality

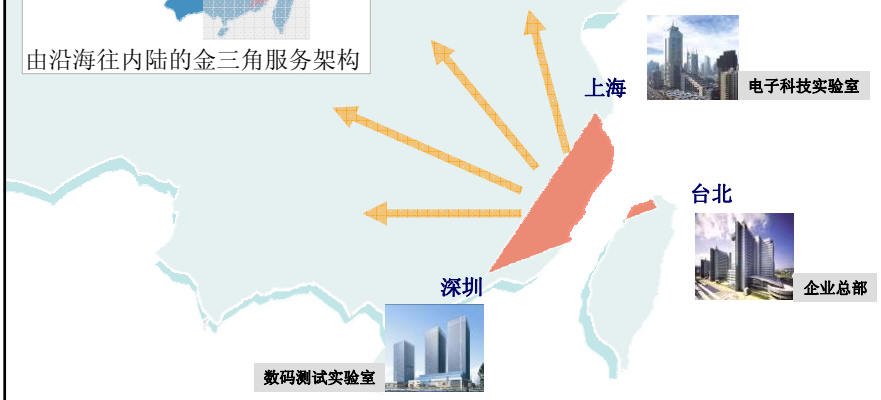
- 20年产品测试经验
- 拥有至少28项Logo标准认证方案
- 超过400名专业测试工程师为您服务
- 备有多达10,000台测试仪器和设备
- 执行超过300,000笔测试项目
- 全球营运分支机构提供本地化服务
- 通过ISO/IEC 17025实验室认证规范

大中华区全方位服务



由沿海往内陆的金三角服务架构

百佳泰位于台北、上海、深圳的营运机构皆拥有完整的测试设备与专业测试团队，不论您的公司或工厂座落在中国任何地方，百佳泰都能提供最优良的测试服务。



Logo标准认证分类

接口

射频/无线传输

操作系统,储存與数位内容

质量验证 –值得信赖的测试伙伴

➔可测试产品涵盖各种类别

家庭娱乐 | 计算机 | 储存装置 | 网路通讯

- 兼容性测试 Compatibility Test
- 互操作性测试 Interoperability Test
- 电气测试 Electrical Test
- 功能性测试 Functionality Test
- 可靠度测试 Reliability Test
- 可用性测试 Usability Test
- 效能测试 Performance Test
- 标竿测试 Benchmark Test

待测物评估 | 客制验证计划 | 测试执行 | 问题侦错 | 第三方报告与认证标章

ALLION Engineering Services

DisplayPort 1.2介绍

Agenda

- DisplayPort and VESA协会介绍
- DisplayPort 规格更新介绍
- DisplayPort Compliance Program 综览
- DisplayPort Compliance Program 更新介绍

DisplayPort and VESA协会介绍

- 新世代技术接口结合了数字音频 /视频的功能并用于个人计算机和消费电子领域
- 此新技术接口未来将会取代VGA和LVDS

Intel and AMD to phase out VGA by 2015

By Hilbert Hagedoorn, December 9, 2010 - 10:21 PM N/A

Well, it's about time really. AMD, Dell, Intel, Lenovo, Samsung and LG vowed to accelerate the adoption of HDMI and DisplayPort into the PC. Both Intel and AMD plan to end support for LVDS in 2013 and the funeral of the VGA output is planned by 2015.
AMD, Dell, Intel Corporation, Lenovo, Samsung Electronics LCD Business and LG Display today announced intentions to accelerate adoption of scalable and lower power digital interfaces such as DisplayPort and High-Definition Multimedia Interface® (HDMI) into the PC.

- 由VESA (**V**ideo **E**lectronics **S**tandards **A**ssociation)发表的技术
  - 非营利的事业机构
  - 提供一个开发新接口的技术平台
  - 此技术规格只有VESA会员可以拥有

DisplayPort 规格更新介绍 (1)

- DisplayPort Spec version 1.2
  - Published in 2010, in products by 2011
  - Main Line Data Rate is Doubled
    - 5.4 Gbit/sec speed option added (speed per lane)
    - Enables higher resolution, deeper color, and 3-D displays
      - Example resolution support: 3840 x 2160 x 30bpp @ 60Hz
  - Higher AUX Channel Bandwidth
    - Speed increased to 720 Mbit/sec
    - Will fully support USB 2.0 data transport and protocol

DisplayPort 规格更新介绍 (2)

- Multiple Streams
  - Support multiple monitors through daisy-chain configuration
    - micro-packet architecture

DP v1.2 source

Four WUXGA monitors (1920 x 1200)

- Mini Connector
  - Apple has contributed mini DP specification to VESA for industry standardize

DisplayPort Compliance Program 综览

- 产品类别
  - Sink
  - Source
  - Media (Cable)


- 测试类别
  - Physical Layer Test
  - Link Layer Test
  - HDCP Test
    - Not mandatory for DP Logo

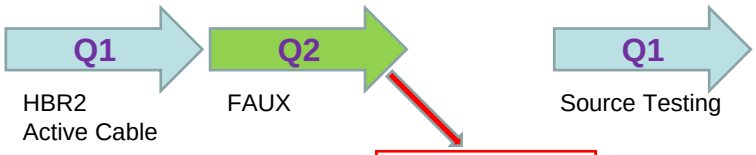


DisplayPort Compliance Program 更新介绍

- DisplayPort Compliance Test Spec 1.2
  - PHY Compliance Test Spec
    - HBR2
    - Active Cable
    - FAUX
  - Link Compliance Test Spec
    - 3D , Audio
    - HBR2, FAUX
    - SST, AV Sync
    - GTC

Roadmap of CTS 1.2

- PHY Layer Compliance
- EDID



HBR2
Active Cable

FAUX

Source Testing

Allion Ready

- Link Layer Compliance

HBR2 Link Training
HBR2 SST operation
HBR Audio transport
Stereo 3D transport

Sideband MSG/MST transport

AV Sync, GTC, FAUX

ALLION Engineering Services

Serial ATA 3.0介绍

Agenda

- SATA-IO Logo Program综览
- SATA-IO Integrators List
- 产品类别介绍
- SATA-IO Compliance Program更新介绍
- SATA-IO 新的应用

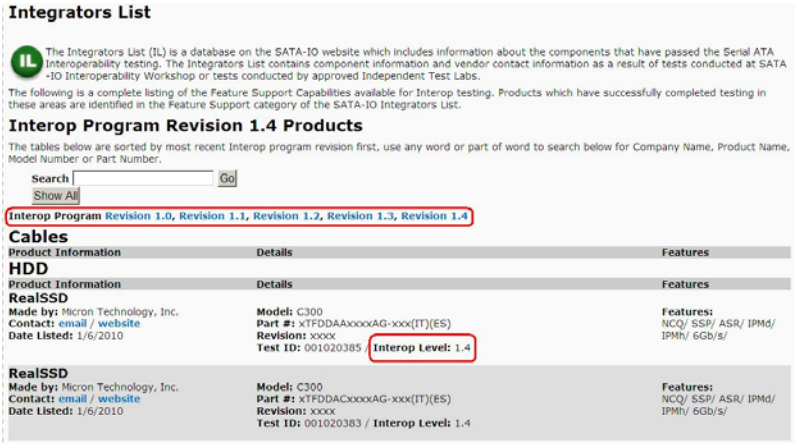
SATA-IO Logo Program综览

- *什么情况下才能合法使用SATA认证徽标?*

  只有当产品已经通过SATA Interoperability 测试并且将产品数据公布在Integrators List (IL)网页上才能合法使用SATA认证徽标

SATA-IO Integrators List

- 当产品已经通过SATA Interoperability 测试就可以将产品数据列于SATA-IO Integrators List 的网页上



Integrators List

The Integrators List (IL) is a database on the SATA-IO website which includes information about the components that have passed the Serial ATA Interoperability testing. The Integrators List contains component information and vendor contact information as a result of tests conducted at SATA -IO Interoperability Workshop or tests conducted by approved Independent Test Labs.

The following is a complete listing of the Feature Support Capabilities available for Interop testing. Products which have successfully completed testing in these areas are identified in the Feature Support category of the SATA-IO Integrators List.

Interop Program Revision 1.4 Products

The tables below are sorted by most recent Interop program revision first, use any word or part of word to search below for Company Name, Product Name, Model Number or Part Number.

Search Go

Show All

Interop Program Revision 1.0, Revision 1.1, Revision 1.2, Revision 1.3, Revision 1.4

Cables

Product Information	Details	Features

HDD

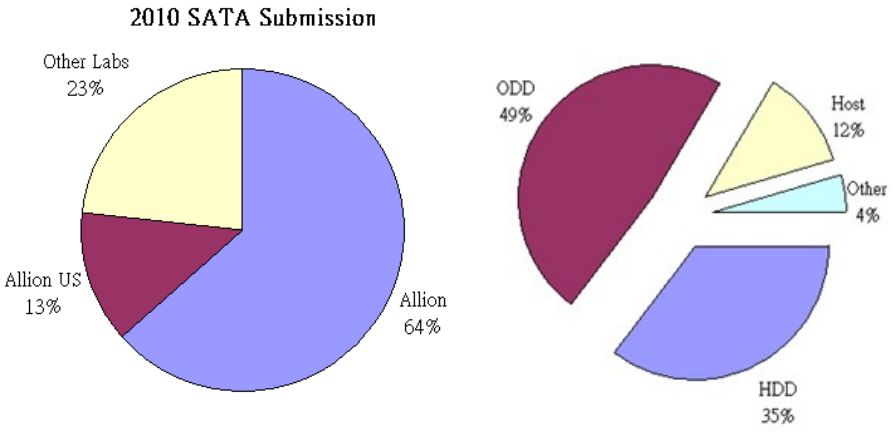
Product Information	Details	Features
RealSSD Made by: Micron Technology, Inc. Contact: email / website Date Listed: 1/6/2010	Model: C300 Part #: xTFDDAAxxxxAG-xxx(IT)(ES) Revision: xxxx Test ID: 001020385 / Interop Level: 1.4	Features: NCQ/ SSP/ ASR/ IPMd/ IPMh/ 6Gb/s/
RealSSD Made by: Micron Technology, Inc. Contact: email / website Date Listed: 1/6/2010	Model: C300 Part #: xTFDDACxxxxAG-xxx(IT)(ES) Revision: xxxx Test ID: 001020383 / Interop Level: 1.4	Features: NCQ/ SSP/ ASR/ IPMd/ IPMh/ 6Gb/s/

产品类别介绍

- **Device**
  - Hard disk drive (HDD & SSD)
  - 1.8 Inch micro-SATA Drive
  - Half-height ATAPI device
  - Slimline ATAPI device
- **Host**
  - Motherboard
  - Add-in controller
- **Building Block (member only)**
  - For silicon solution、IP solution vendor
  - Non-certified categories (Ex. eSATA, mini-SATA….)

SATA-IO Submission Status

- 2010年统计的数字有超过75%的产品是透过Allion测试并提交结果到SATA-IO协会



SATA-IO Compliance Program更新 – Electrical (TSG)

- Add 6Gbps tests from UTD1.4
  - Transmit Jitter RJ
  - TJ before/after CIC
  - TX Differential Voltage Amplitude
  - (6Gb/s) Tx AC Common Mode Voltage
- TSG-02: Rise / Fall time
  - Test Pattern: LFTP
- Obsolete Tests
  - TSG-05: Rise/Fall Imbalance
  - TSG-06: Amplitude Imbalance

SATA-IO Compliance Program更新 – Electrical (RSG)

- General RSG Calibration
  - TP1: Rise/Fall time, Rj, Sj,
  - TP2: Tj, Amplitude

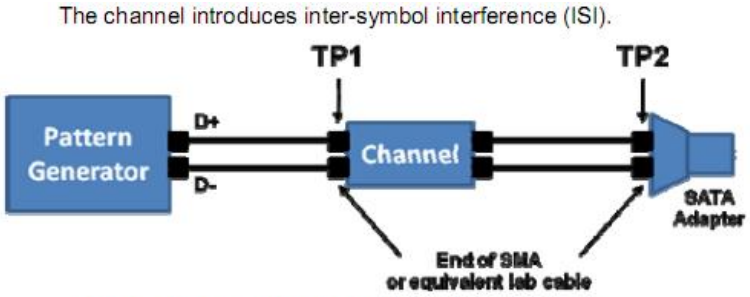


Figure 1 – Test points for RSG setup calibration.

SATA-IO Compliance Program更新 – Electrical (RSG)

- RSG Setup Calibration Steps and Settings

Step	Test Point	Calibration Pattern	1st Gen i	1st Gen m	2nd Gen i	2nd Gen m	3rd Gen
Rise / Fall Time	TP1	LFTP	100 ps (20/80%)		100 ps (20/80%)		62 ps to 75 ps (20/80%)
Rj	TP1	MFTP	8.57 ps RMS		4.285 ps RMS		2.14 ps RMS
Sj	TP1	MFTP	Sj=270mUI		Sj=270mUI		Sj=192mUI
Tj	TP2	Framed COMP	Tj(min)=501mUI Tj(max)=519mUI		Tj(min)=552mUI Tj(max)=588mUI		Tj(min)=498mUI Tj(max)=570 mUI
Amplitude	TP2	LBP	325mV	240mV	275mV	240mV	Host: 240mV Device: 200mV

SATA-IO Compliance Program更新 – Electrical (RSG)

- Receiver Jitter Tolerance Test
  - The device need to run the applicable RSG tests.
  - Ex: SATA 6.0Gb/s: RSG-01, RSG-02 and RSG-03

Test Patterns	SATA Mode	Test Time
RSG-01: Framed COMP Pattern (2 ALIGNp)	1.5Gbps	5MHz: 10 Min 10MHz: 10 Min 33MHz: 10 Min 62MHz: 10 Min
RSG-02: Framed COMP Pattern (2 ALIGNp)	3Gbps	5MHz: 5 Min 10MHz: 5 Min 33MHz: 5 Min 62MHz: 5 Min
RSG-03: Framed COMP Pattern (2 ALIGNp)	6Gbps	5MHz: 2.5 Min 10MHz: 2.5 Min 33MHz: 2.5 Min 62MHz: 2.5 Min

SATA-IO Compliance Program更新 – Electrical (RSG)

- Receiver Jitter Tolerance Test
  - RSG-05: Receiver Stress Test at +350ppm (Normative)
    - Data Rate of the pattern generator: 1.5Gb/s + 350ppm
  - RSG-06: Receiver Stress with SSC (Informative)
    - Data Rate range is between 1.5Gb/s – 5350ppm and 1.5Gb/s -350ppm

SATA-IO Compliance Program更新– Digital

- Digital Test
  - Multiple Signaling Speed establish
    - DUT need to verify compatible speed
    - Ex: IPM-03 : Speed matching upon resume
  - Digital Optional Features
    - Asynchronous Notification
      - A mechanism for a device to send a notification to the host the device requires attention
    - PHY Speed Indicator
      - Check the interface rate is equal to IDENTIFY DEVICE or IDENTIFY PACKET DEVICE info.

SATA-IO 新的应用 SATA 3.1 – LIF SATA

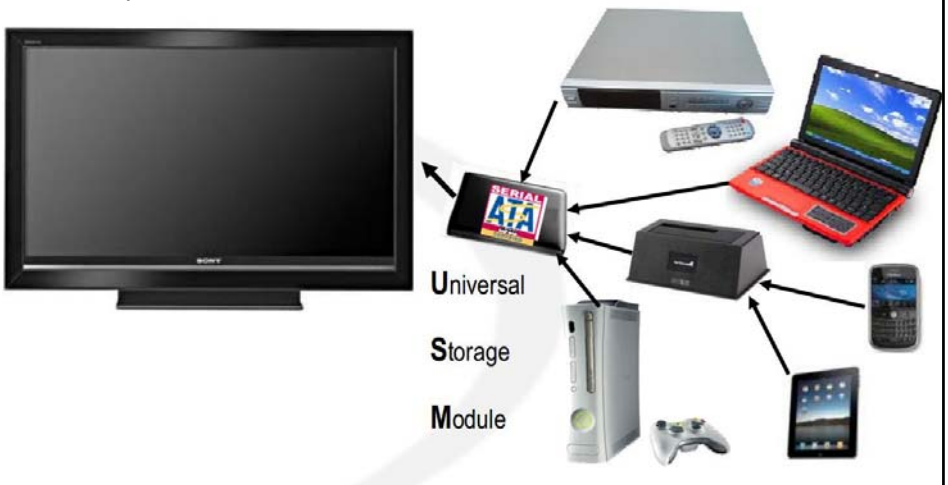
- LIF-SATA
  - Low Insertion Force Connector
  - Support 1.5 Gb/s and 3.0 Gb/s transfer rates
  - The LIF-SATA connector can only be mated with FPC cable
  - Support for 8.0 and 5.0 mm slim 1.8” Form Factor (FF) HDD’s
  - Support of 3.3 V with 5 V to meet future product requirements

SATA-IO 新的应用 Spec v3.1 – mSATA

- mini-SATA
  - Mini PCI-E Interface application
  - mSATA Extends Benefits of SATA Interface for Small Form Factor Applications.
  - mSATA is particularly beneficial for manufacturers planning to incorporate small form factor SSDs (approximately the size of a business card) in portable PC devices.
  - mSATA will support 1.5 Gb/s and 3.0 Gb/s transfer rates.

SATA-IO 新的应用 Spec 3.x - USM

- SATA Universal Storage Module™ (USM)
  - Up to 6 Gb/s



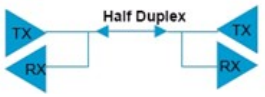
Agenda

- USB 3.0综览
- USB 3.0 Compliance测试范围
- USB 3.0 的更新

USB 2.0 和3.0 的差异比较

•USB 2.0 High-Speed

- ✓ 480Mbps
- ✓ NRZI, Half Duplex
  (1 bi-directional link)
- ✓ 4 signals
  Dp, Dm
  VCC, GND
- ✓ Cable Lmax= 5meter
- ✓ $I_{configLP/FP}$ = 100mA/500mA
- ✓ $I_{suspend}$ = 500uA
- ✓ No SSC

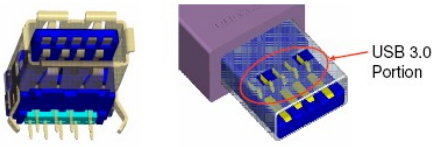


•USB 3.0 SuperSpeed

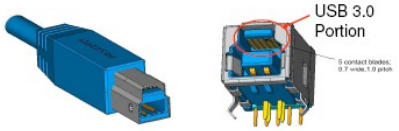
- ✓5 Gbps
- ✓8B/10B PRBS, Full Simplex
  (2 uni-directional links)
- ✓8 signals
  4 USB2
  4 SS Signals
- ✓Cable L_{max}= 3 meters
- ✓$I_{configLP/FP}$ = 150mA/900mA
- ✓$I_{suspend}$ = 2.5mA
- ✓SSC

USB 3.0 接口

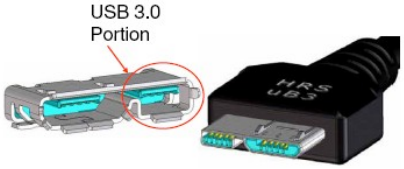
- Std A - Same interface as USB 2.0 Standard-A connector, but with added pins for USB 3.0 Super-Speed signals
- Complete compatibility with USB 2.0 Standard-A connector



- Std B - Defined for relatively large, stationary peripherals such as hard drives and printers
- Powered version variant is a defined
- Visually different from USB 2.0 Standard-B connector



- Micro B - Based on the proven USB 2.0 Micro-B connector design with an extended portion for the Super-Speed signals
- USB 3.0 Micro-A and –AB connectors are identical to USB 3.0 Micro-B connector except for keying/profile differences



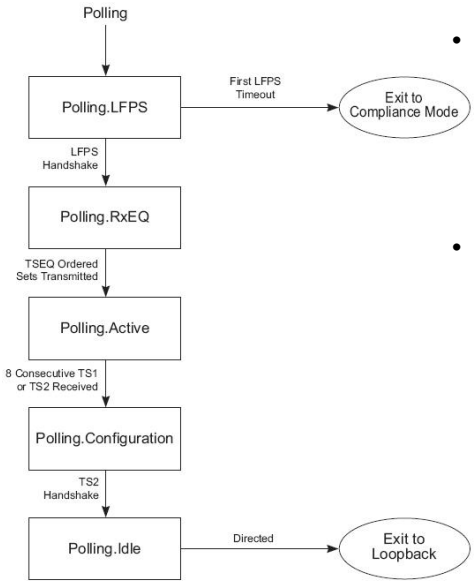
USB 3.0 Compliance测试范围

- 3.0 Electrical Test
- Link Layer Test
- Framework Test
- Interoperability Test
- USB 2.0 LS/FS/HS Test

USB 3.0 Electrical测试

- Low Frequency Periodic Signaling (LFPS) Tx Test
- Low Frequency Periodic Signaling (LFPS) Rx Test
- Transmitted Eye Test
- Transmitted SSC Profile Test
- Receiver Jitter Tolerance Test

Test Mode for SuperSpeed



- Tx test in Compliance Mode
  - 50ohm termination make it happen
  - Use Ping.LFPS to change test pattern
- Rx test in Loopback Mode
  - Need more steps of training sequence

Bit	TS1 Symbol 5
Bit 0	0 = Normal Training 1 = Reset
Bit 1	Set to 0
Bit 2	0 = Loopback de-asserted 1 = Loopback asserted
Bit 3	0 = Disable Scrambling de-asserted 1 = Disable Scrambling asserted
Bit 4:7	Set to 0

Compliance Test Pattern

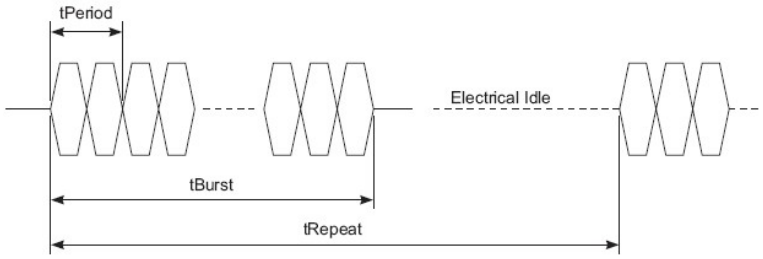
Table 6-7. Compliance Pattern Sequences

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	With without de-emphasis. Repeating 50-250 1's and then 50-250 0's.

Note: Unless otherwise noted, scrambling is disabled for compliance patterns.

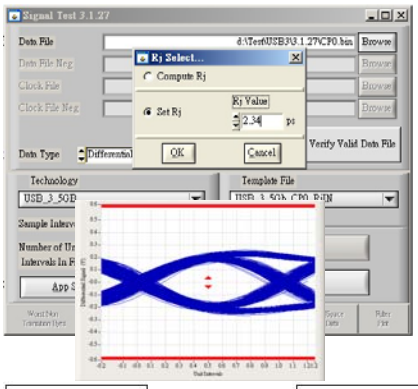
3.0 Electrical测试– LFPS Tx/Rx

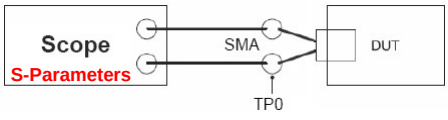
- Tx: Make sure LFPS meets specification
- Rx: Make sure Receiver can handle worst of LFPS
  - Differential voltage: 800, 1200mV
  - Duty Cycle: 40, 60%
  - Not yet to be added at last workshop as well as PIL

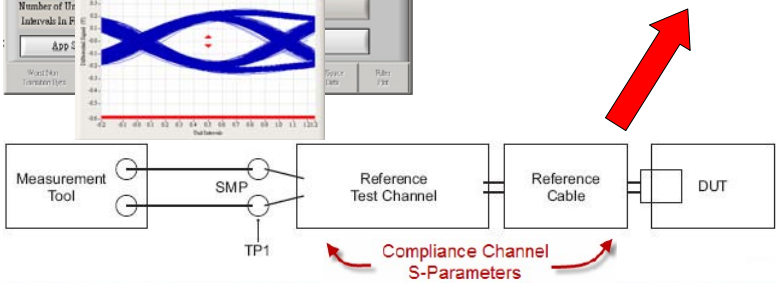


3.0 Electrical测试– Transmitted Eye

- SigTest has integrated CTLE feature

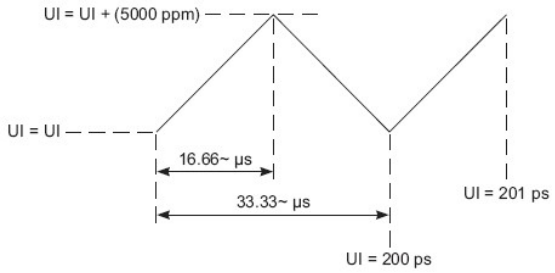






3.0 Electrical测试– Transmitted SSC Profile

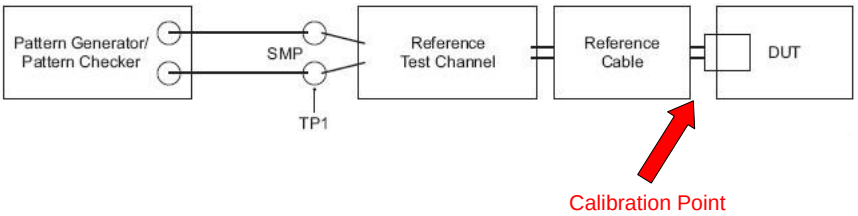
- 3.0 port has Spread Spectrum Clock (SSC) is required in specification



Symbol	Description	Limits		Units	Note
		Min	Max		
$t_{SSC-MOD-RATE}$	Modulation Rate	30	33	kHz	
$t_{SSC-FREQ-DEVIATION}$	SSC deviation	+0/-4000	+0/-5000	ppm	1, 2

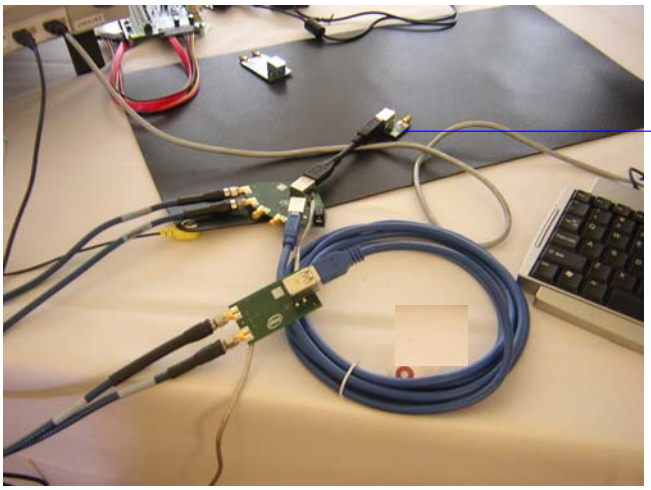
- Test spec for SSC Deviation: +300/-3700 and +300/-5300 ppm

3.0 Electrical测试– Receiver Jitter Tolerance



- Calibration Point
  - Eye Height is 145mV for Device and 180mV for Host
  - Total Jitter is about 0.6UI
- Test with 8 steps
  - Sj: 0.5, 1, 2, 4.9, 10, 20, 33, 50MHz
- External BERT is used

Receiver Jitter Tolerance Test Configuration



Link Layer测试

- USB-IF is co-working with protocol analyzer vendor
  - Come out test spec
  - Temporary solution by using protocol analyzer
- FYI at last USB workshop

Host Link Layer
- U3LET.005-Detecting Header frame Packet with Framing Error and a corrupted symbol
- U3LET.006-Detecting Header frame packet with Framing Error with more than a corrupted symbol
- U3LET.007-Detecting Header Packet Error (CRC5)
- U3LET.008-Detecting Header Packet Error (CRC16)
- U3LET.009-Detecting Header Packet Error (CRC5) for 3 times
- U3LET.010-Detecting Header Packet Error (CRC16) for 3 times
- U3LET.011-Detecting Header Packet Error (CRC16 and CRC5)
- U3LET.012-Go to recovery on Rx Header Sequence Number Error

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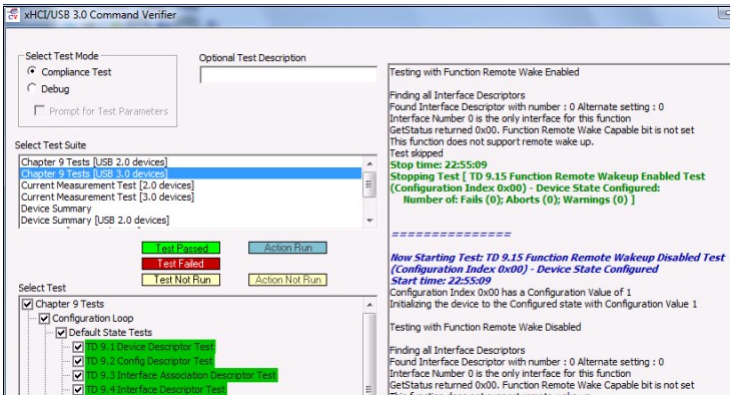
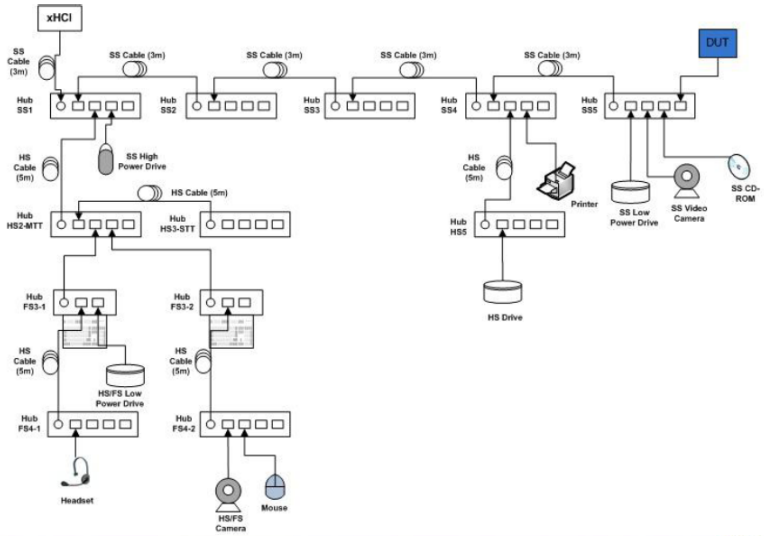
Framework测试

- Same with USB 2.0 test concept
  - Test by using USBCV 3.0
  - Test with known good devices for HUT



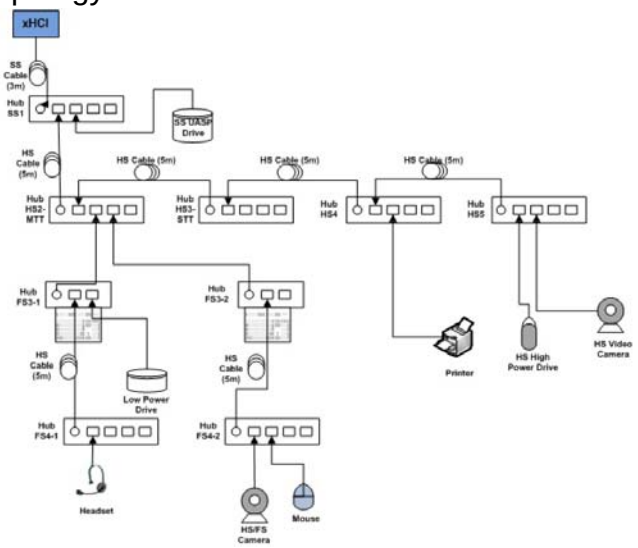
xHCI Interoperability测试

- Tree Topology



xHCI Backward兼容性测试

- Tree Topology



USB 2.0 LS/FS/HS测试

- All USB 3.0 products have to pass 2.0 compliance test
  - 2.0 Interoperability
  - Device Framework Tests (chapter 9)
    - Device Class Framework Tests (if applicable)
  - Average current
  - Backvoltage
  - Inrush
  - Signal quality
  - If high-speed signaling is supported, all packet parameter tests.

USB 3.0 的更新

- 在您的产品要安排到PIL送测3.0认证之前请先到指定实验室通过以下USB2.0 和USB3.0的项目
  - 2.0 Full compliance test
  - 3.0 Electrical, CV and Average Current
- 测试实验室预计可接受USB3.0认证的时间表
  - May-June, 2011

Q&A

Thank You