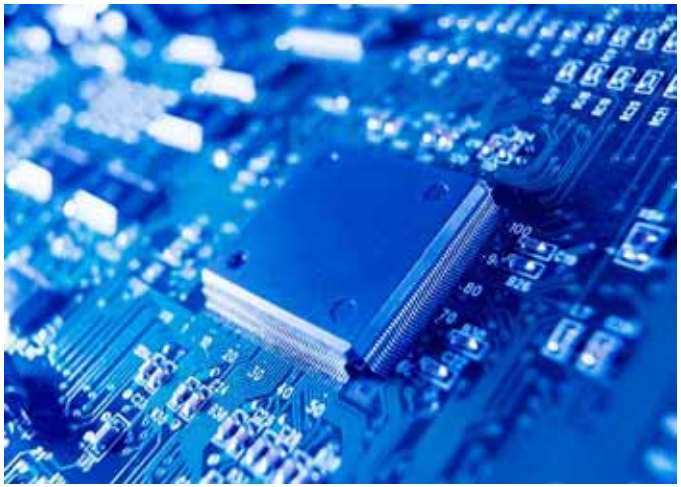
PCI Express 3.0 Testing Approaches for PHY and Protocol Layers

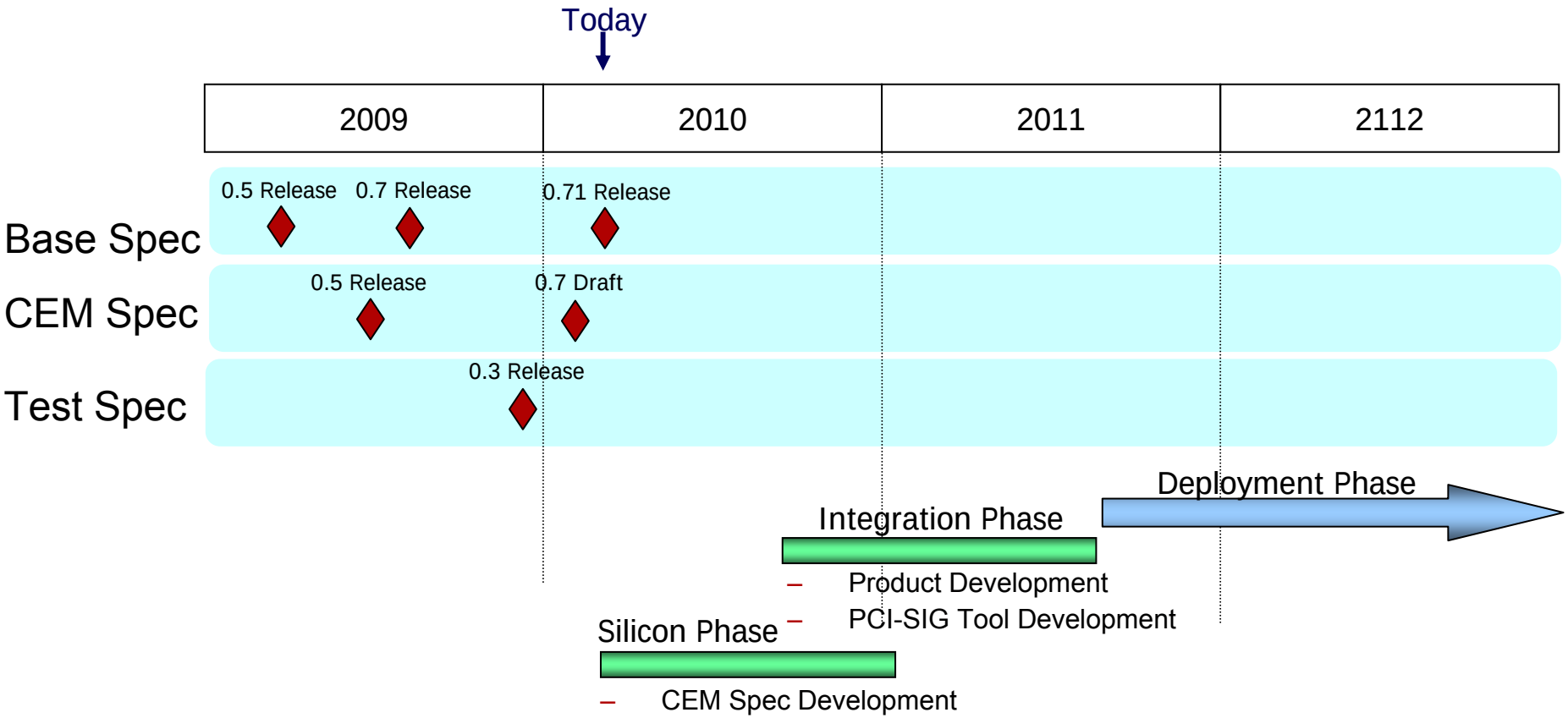


Tektronix

Agenda

- Introduction to PCI Express 3.0
  - Trends and Challenges
- Physical Layer Testing Overview
  - Transmitter Design & Validation
  - Transmitter Compliance
  - Receiver & Summary of Tools for PCIe PHY Testing
- Protocol
  - Planning probe access
  - Time to confidence
  - Information density
  - Applications
- Summary

PCI Express 3.0 Technology Timeline



Presentation Content based on
.9 Base Specification Draft and
.7 CEM Specification Draft

Tektronix Involved in PCIe EWG, CEM, and Serial Enabling Working Groups

Tektronix Innovation Forum

PCI Express 3.0
Trends and Implications

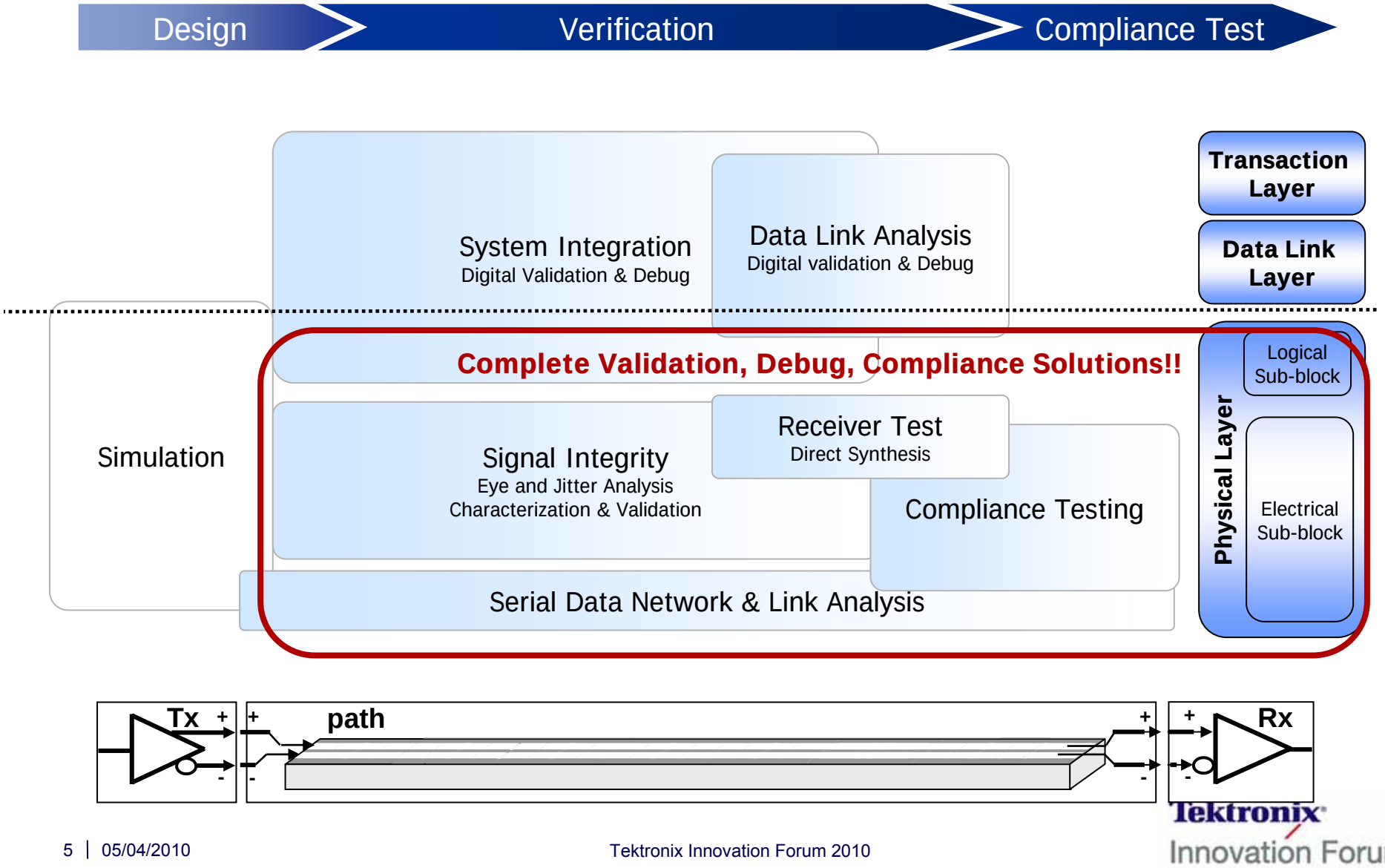
Industry/Technology Trends

- Data transfer rates continue to increase: 2.5 ➡ 5 ➡ 8 GT/s
- 128b/130b encoding
- Backwards interoperability
- Energy efficiency (Lower mW/Gb/s)

Implications

- Greater system complexity increases the engineering challenge
- Higher data rate signals have less margin – requires de-embedding
- Crosstalk, skew, noise and attenuation more significant
- Link training and power management continue to be the most difficult challenges

High Speed Serial Test Challenges



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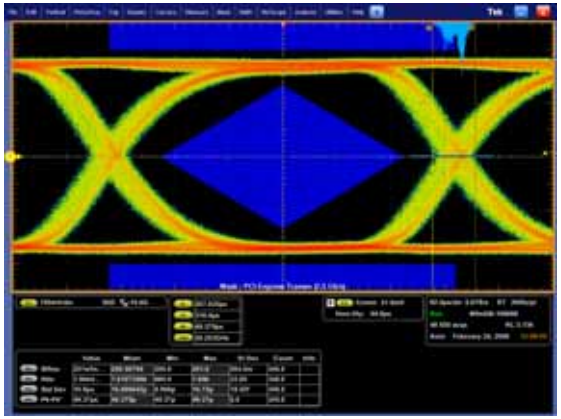
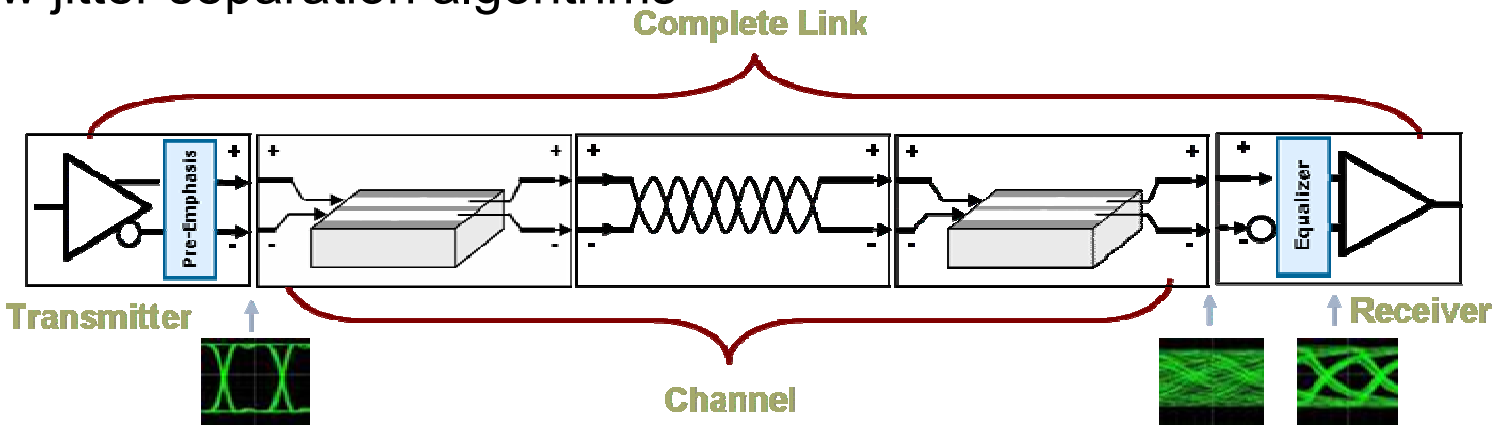
What's New for PCI Express Gen 3.0



- Double bandwidth (8GT/s with 128b/130b) while using traditional circuit board (FR-4)
- Requires de-embedding measurements to Tx pins, specifies breakout and replica channels.
- Large channel losses require Tx and Rx equalization
  - Tx equalization- Defined pre-shoot and de-emphasis Presets
  - Rx equalization– behavioral CTLE & DFE
- New jitter separation algorithms



Transmitter Design & Validation

PCI Express

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PCIe 3.0 Base Spec Transmitter Voltage and Jitter Measurements

- Base Spec Measurements defined at the pins of the transmitter
- New Jitter Measurements are defined for PCIe 3.0

Table 4-3: 8.0 GT/s Tx Voltage and Jitter Parameters

Symbol	Parameter	Value	Units	Notes
$V_{TX-FS-NO-EQ}$	Full swing Tx voltage with no TxEq	1200 (max) 800 (min)	mVPP	Note 1
$V_{TX-RS-NO-EQ}$	Reduced swing Tx voltage with no TxEq	1200 (max)	mVPP	Note 1
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 (min)	mVPP	Note 2
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232 (min)	mVPP	Note 2
T_{TX-UTJ}	Tx uncorrelated total jitter	31.25 (max)	ps PP @ 10^{-12}	
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	12 (max)	ps PP	
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	24 (max)	ps PP @ 10^{-12}	Notes 3,4
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	10 (max)	ps PP	Note 3,4
T_{TX-DDJ}	Data dependent jitter	15 (max)	ps PP	Note 4.
$ps21_{TX}$	Pseudo package loss	-4.0 (min)	dB	PP ratio of 64 ones/64 zeroes pattern vs. 0101 pattern. No Tx equalization. Note 5
$V_{TX-BOOST-FS}$	Tx boost ratio for full swing	8.0 (min)	dB	Assumes ±1.5 dB tolerance from diagonal elements in Figure 4-6.
$V_{TX-BOOST-RS}$	Tx boost ratio for reduced swing	2.5 (min) 4.5 (max)	dB	Assumes ±1.0 dB tolerance from diagonal elements in Figure 4-6.
$EQ_{TX-COEFF-RES}$	Tx coefficient resolution	1/24 (max) 1/63 (min)	N/A	

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New PCIe 3.0 Jitter Measurements

- Uncorrelated Total Jitter and Uncorrelated Deterministic Jitter
  - Uncorrelated jitter is not mitigated by Tx or Rx equalization and represents timing margin that cannot be recovered with equalization.
  - Data Dependent Jitter is determined by averaging from a repeated compliance pattern
  - Uncorrelated Jitter derived after removing Data Dependent Jitter
  - Construct the bathtub curve in Q scale
  - Estimate Total Jitter with Q Scale extrapolation

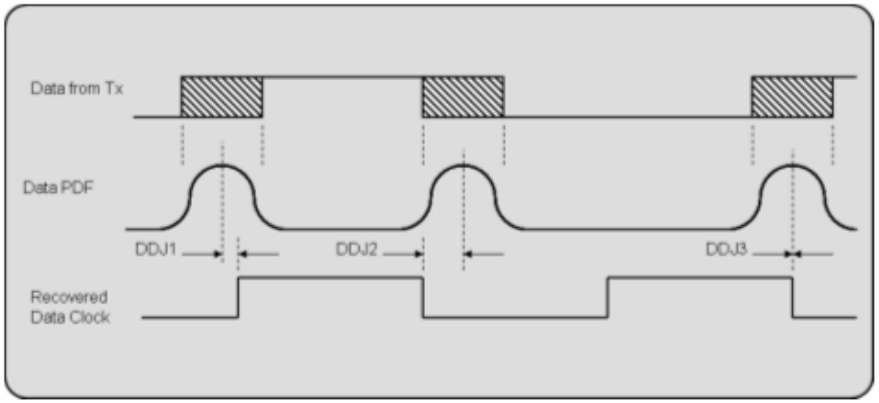

Figure 4-10: Relation Between Data Edge PDFs and Recovered Data Clock

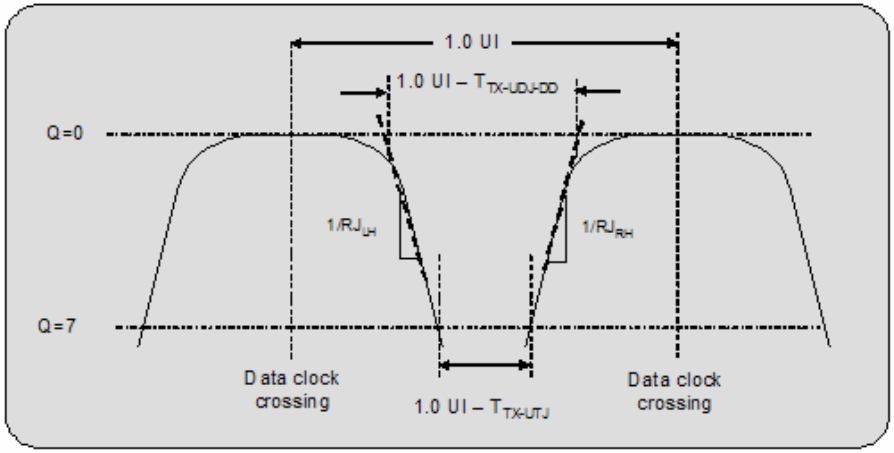

Figure 4-11: Derivation of T_{TX-UTJ} and $T_{TX-UDJDD}$

New PCIe 3.0 Jitter Measurements (cont'd)

- Uncorrelated Total and Deterministic PWJ
  - Long lossy channels cause single pulses to be attenuated
  - ISI contributions need to be removed to determine PWJ
  - Calculate the edge to edge Jitter
  - Construct the bathtub curve in Q scale
  - Estimate Total Jitter with Q Scale extrapolation

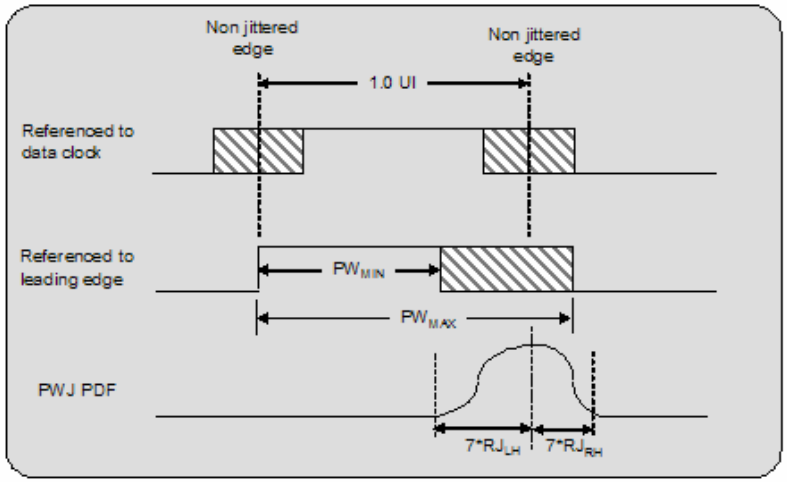

Figure 4-12: PWJ Relative to Consecutive Edges 1 UI Apart

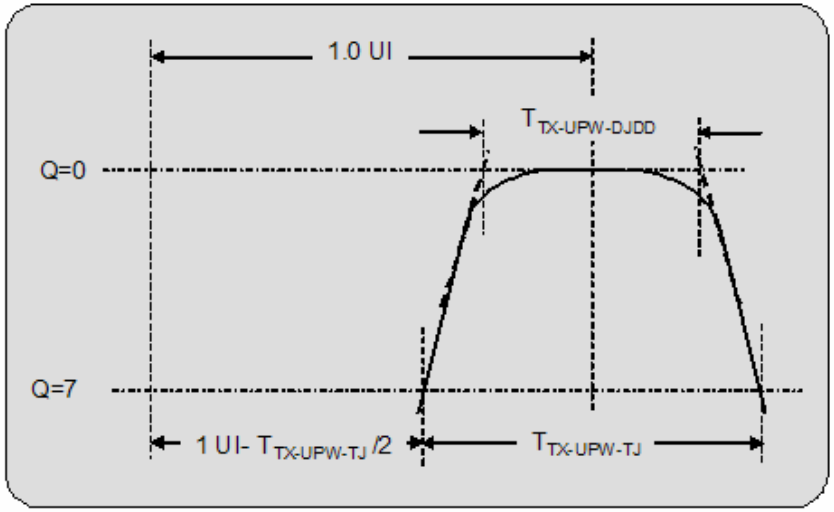

Figure 4-13: Definition of $T_{TX-UPW-DJDD}$ and $T_{TX-UPW-TJ}$

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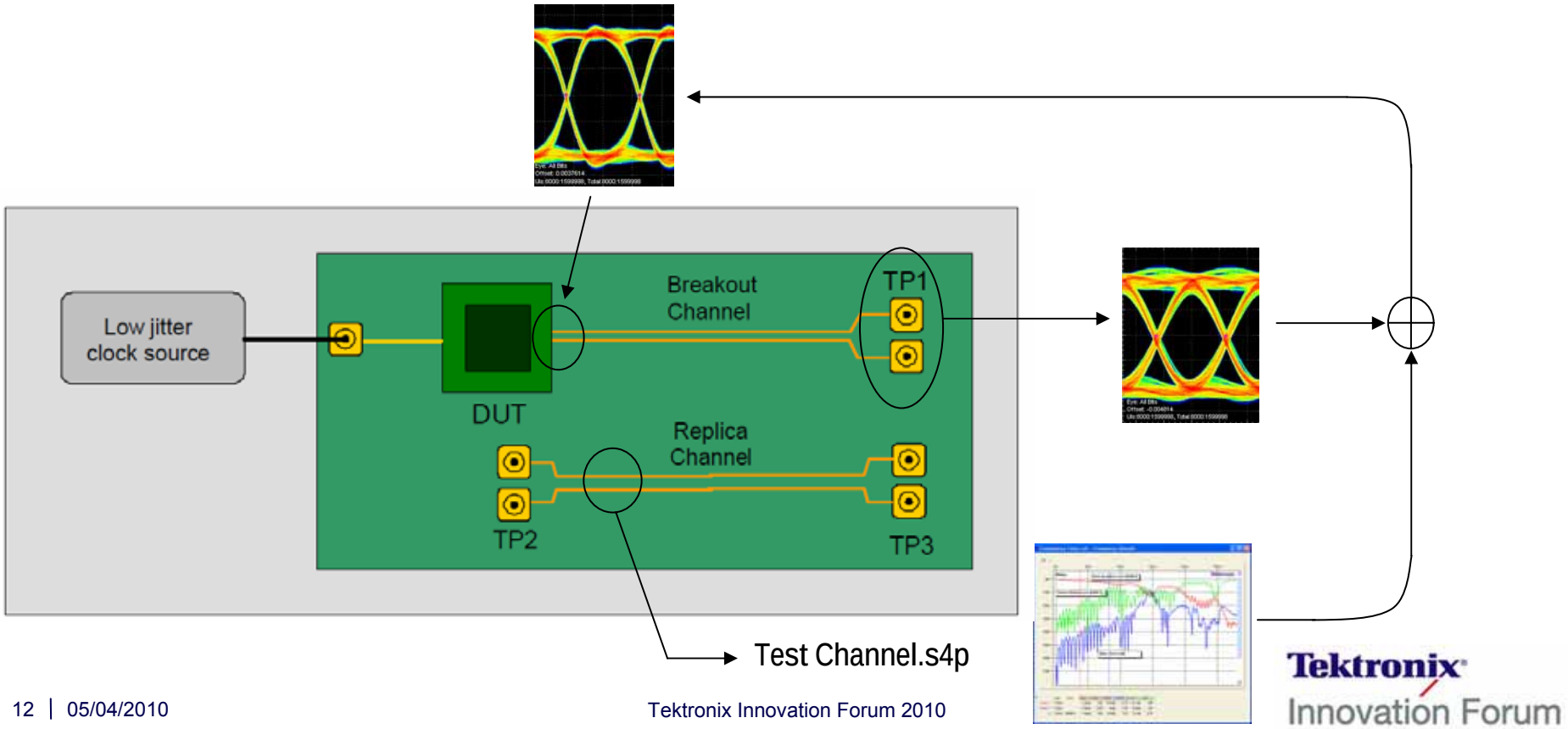
Transmitter Characterization

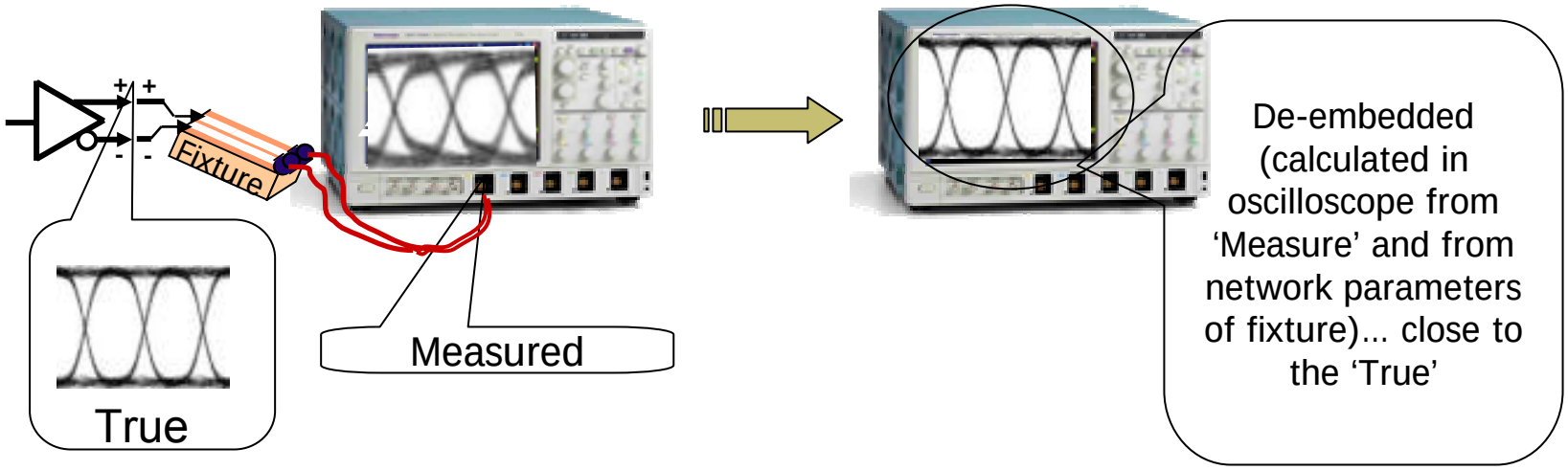
- Tx measurements referenced to pins but can only access TP1
- Extract replica channel transfer function (S-Parameter)
- Acquire signals at TP1 then mathematically remove channel effects



De-embedding

Removal of signal impairment caused by selected known part of the circuit.
Measurement setup often known – i.e., a fixture.

- When impacts does the test fixture add?
- What does the signal look like at the Tx, without the fixture?



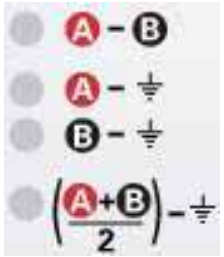
- Measure the Fixture (with TDR, VNA, etc) and and capture the network's parameters (e.g. as a S parameter touchstone file)
- In the oscilloscope Import the S parameter file, view the waveform as it was at the source.

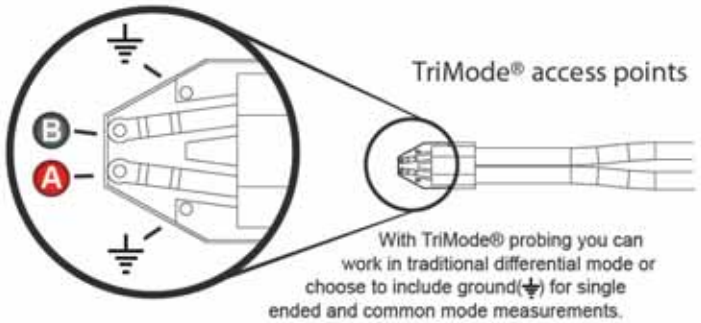
Probing and Signal Access

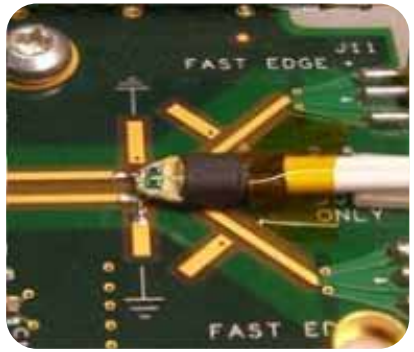
- Typically used when a signal needs to be measured and no SMA or RF connector is available

- Debug
  - Require a quick way to check that signals are present
  - Solder tips can be used for a more permanent connection for troubleshooting

- Validation and Compliance Testing
  - Chip to chip buses







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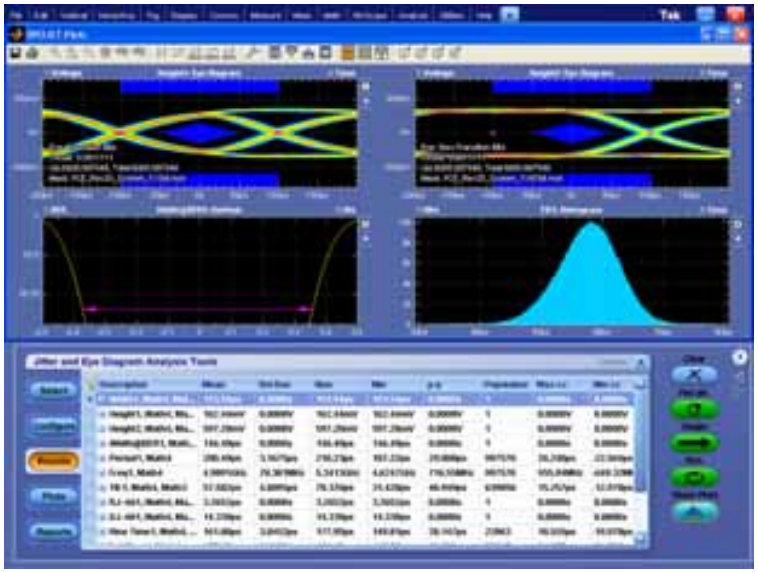
Tektronix' Solutions for PCIe 3.0 Base Spec Testing

Available Today

- Channel Embedding / De-embedding support with (Serial Data Link Analysis) Software
- TX Voltage $V_{TX\text{-}FS\text{-}NO\text{-}EQ}$ and $V_{TX\text{-}RS\text{-}NO\text{-}EQ}$ Measurements available today in DPOJET
- 20Ghz Real-Time Oscilloscope and Probes for Fifth Harmonic Capture



Tektronix DPOJET PCIe 3.0 SW

Transmitter Compliance

PCI Express

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CEM Specification Add-In Card Transmitter Testing

- TX measurements based on one preset value (assumption is the best preset will be used for compliance)
- Measurements taken after RX Equalization using the Compliance Base Board
- Voltage Measurements on Both Transition and Non-Transition Bits at a BER of 10^{-6}
- Eye Width Measurements taken with a sample of at least 10^6 UI and Eye opening is computed at 10^{-6}

Preset Number	preshoot (dB)	de-emph (dB)	c_{-1}	c_{+1}
P4	0.0	0.0	0.000	0.000
P1	0.0	-3.5 ±1 dB	0.000	-0.167
P0	0.0	-6.0 ±1.5 dB	0.000	-0.250
P9	3.5 ±1 dB	0.0	-0.166	0.000
P8	3.5 ±1 dB	-3.5 ±1 dB	-0.125	-0.125
P7	3.5 ±1 dB	-6.0 ±1.5 dB	-0.100	-0.200
P5	1.9 ±1 dB	0.0	-0.100	0.000
P6	2.5 ±1 dB	0.0	-0.125	0.000
P3	0.0	-2.5 ±1 dB	0.000	-0.125
P2	0.0	-4.4 ±1.5 dB	0.000	-0.200
P10	0.0	-9.5 ± 1.5 dB	0.000	-0.333

Va	Vb	Vc
1.000	1.000	1.000
1.000	0.668	0.668
1.000	0.500	0.500
0.668	0.668	1.000
0.750	0.500	0.750
0.800	0.400	0.600
0.800	0.800	1.000
0.750	0.750	1.000
1.000	0.750	0.750
1.000	0.600	0.600
1.000	0.333	0.333

Table 4-13: Add-in Card Transmitter Path Compliance Eye Requirements at 8 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	18	1200	mV	Notes 1, 2, 4
V_{TXA_d}	18	1200	mV	Notes 1, 2, 4
T_{TXA}	37.5		ps	Notes 1, 3, 4

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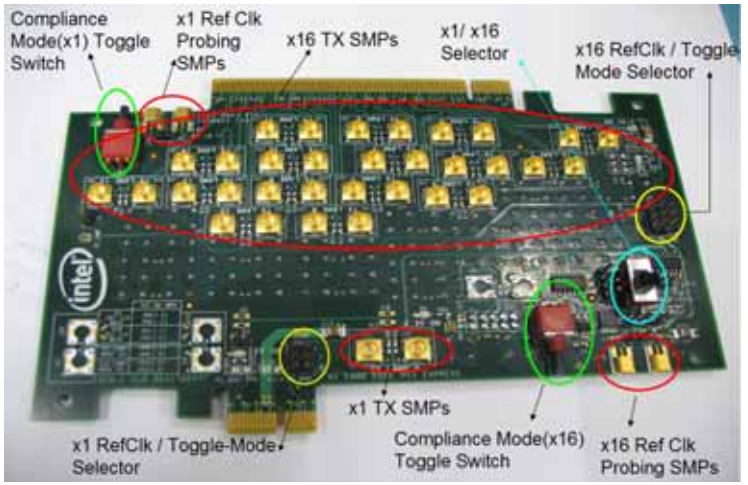
CEM Specification System Transmitter Testing

- Same methodology as Add-In Card Testing, but uses the dual port method (clock and data)
- Measurements taken after RX Equalization using the Compliance Load Board
- Voltage Measurements on Both Transition and Non-Transition Bits at a BER of 10^{-6}
- Eye Width Measurements taken with a sample of at least 10^{6} UI and Eye opening is computed at 10^{-6}



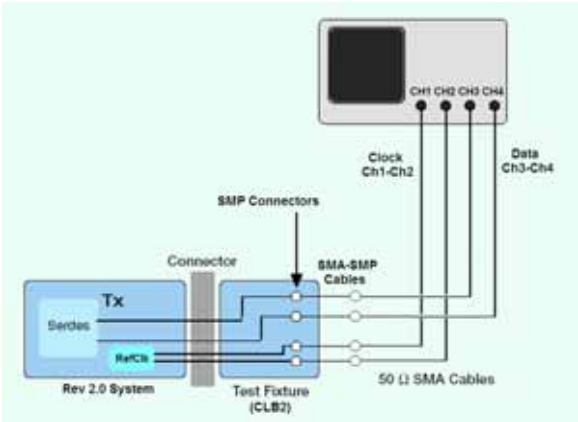


Table 4-10: System Board Transmitter (TX) Output Test Requirements at 8 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXS}	21	1200	mV	Notes 1, 2, 4
V_{TXS_d}	21	1200		Notes 1, 2, 4
T_{TXS}	37.5		ps	Notes 1, 3, 4

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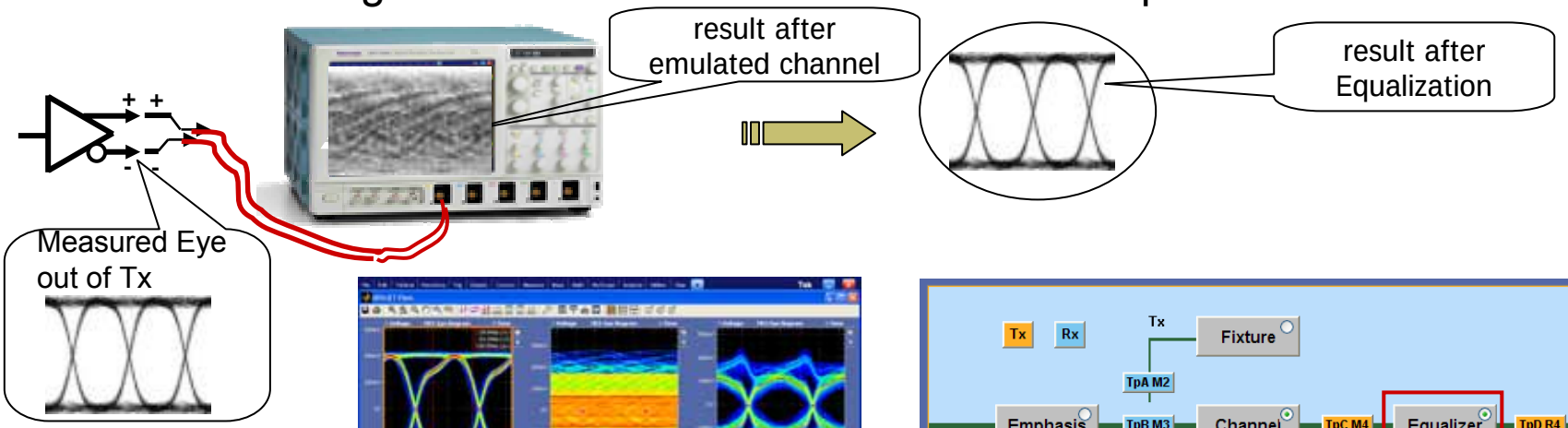
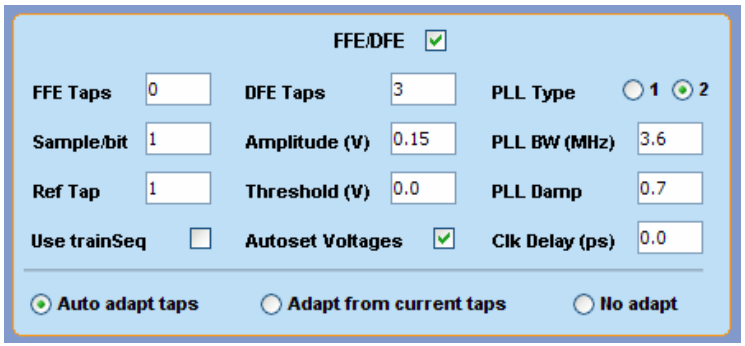
Receiver Equalization

- PCIe Gen 3.0 uses Transmitter De-emphasis plus RX CTLE and Dfe
- What would the signal look like inside the receiver after equalization?



- Link analysis with Continuous Time Linear Equalizer (CTLE) or Decision Feedback (DFE) Equalizers
- Three DFE modes
  - Coefficients values adapted based on measured data- Auto adapt taps
  - Coefficient values adapted based on existing taps- Adapt from current taps
  - Do not adapt
- *Slicer controls and training sequence support*



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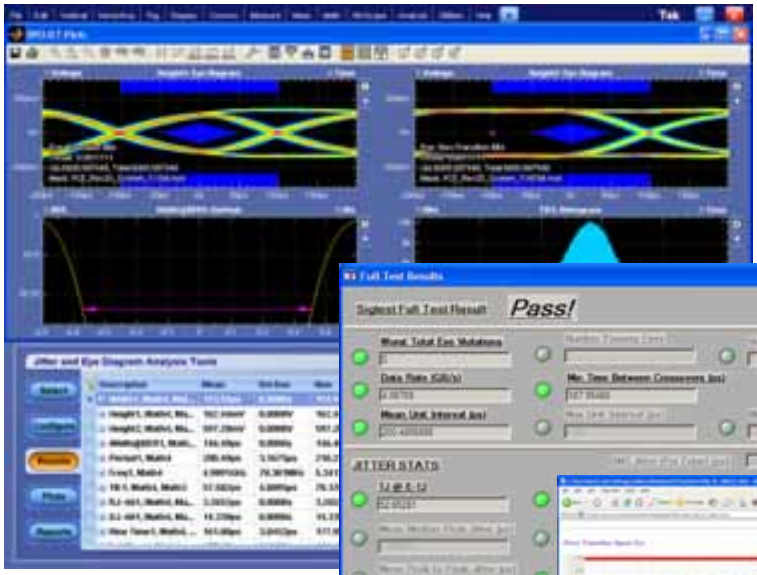
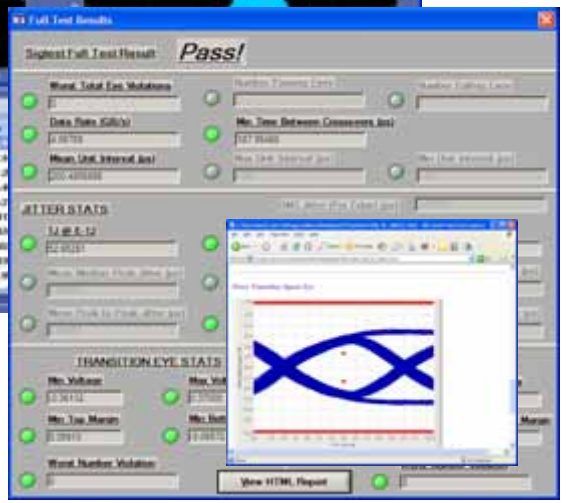
Tektronix' Solutions for PCIe 3.0 CEM Testing

Available Today

- Receiver Equalization support for CTLE and DFE with SDLA (Serial Data Link Analysis) Software
- Measurements available today in DPOJET



Tektronix DPOJET SW



PCI-SIG SigTest SW

Summary of Tektronix Tools for PCIe Testing

TDR/TDT/IConnect for Serial Data Network Analysis

- 50 GHz TDR/TDT system and S-Parameter measurements, highly accurate impedance and loss measurements
- Up to 1M record length

Real-Time Oscilloscope and Analysis Tools

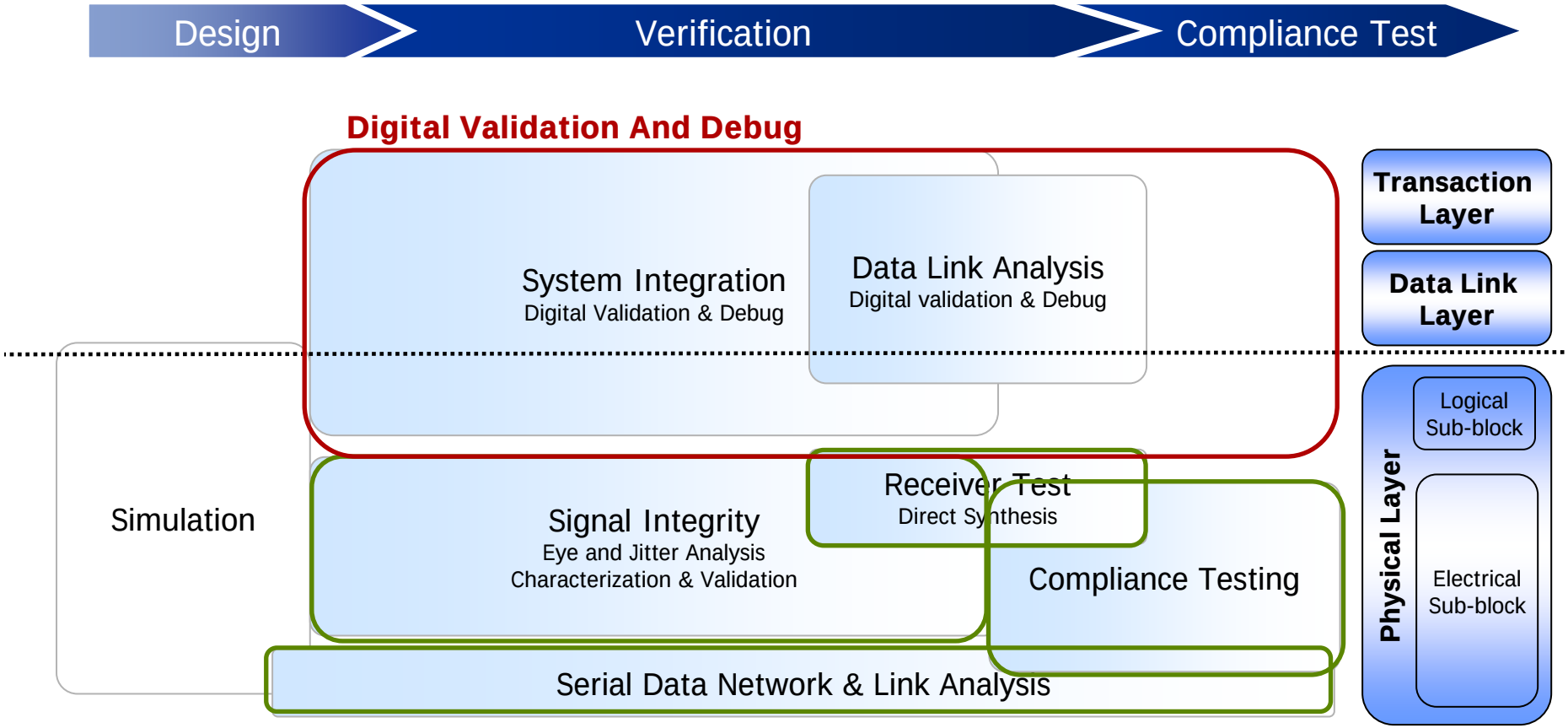
- Transmitter Validation, Debug, Compliance, and Receiver Calibration
- “Complete Link” – channel embedding/de-embedding, equalization (CTLE/DFE) with SDLA
- CEM and Base Spec Measurements with DPOJET and TekExpress
- TriMode Differential probes – 20GHz to the probe tip

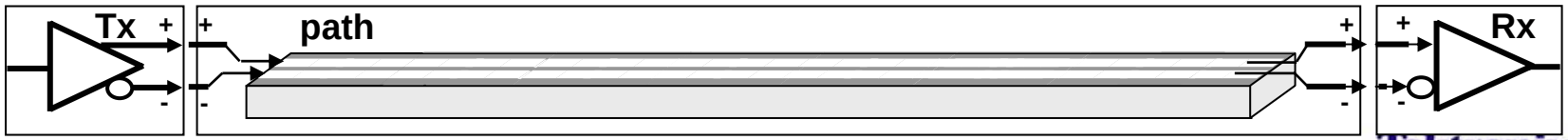
Receiver Stress Generation

- Flexibility to support all signal impairments required for jitter tolerance testing
- Model real-world complexities of SSC profiles to avoid system interoperability issues

Digital Validation And Debug

Logic layer validation





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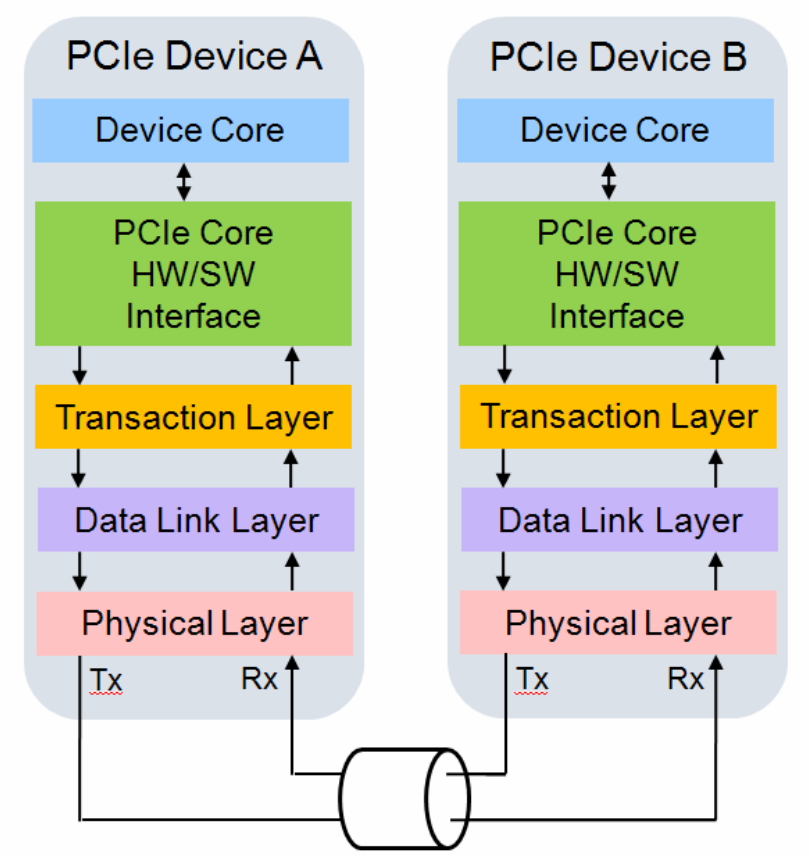
Testing Challenges with PCI Express 3.0



Transaction Layer

- Creates Request/Completion Transactions
- Messaging
- TLP Flow Control

Data Link Layer

- Flow control information
- Data Integrity, Error Checking/Correction
- Calculates/Check TLP Sequence Number
- Calculate/Check CR

Physical Layer – Logical Sub Block

- Link Initialization and Training
- Distribution of packet information over multiple lanes
- Power management and link power state transitions

Physical Layer – Electrical Sub Block

- Transmitter Signal Quality and Ref Clock Testing
- Receiver Testing
- Interconnect Testing
- PLL Loop BW

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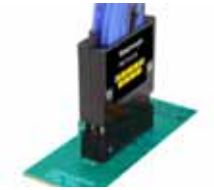
Challenges Selecting Tools for PCI Express 3.0

- Planning probe access
  - Accessing PCIe3 signals
  - Assessing probing impact
  - Probing flexibility
- Time to confidence
  - Automating setup
  - Recovery options
  - Powerful triggering
  - Wide acquisition window
- Information density
  - Four (4) different data visualizations that provide views dedicated to different types of investigations:
    - Summary statistics window
    - Transaction window
    - Listing window
    - Waveform window
- Applications
  - Transaction Window – Intro
  - Transaction Window – Normal Traffic
  - Transaction Window – Transaction Error
  - Transaction Window – Physical Layer
  - Summary Profile Window



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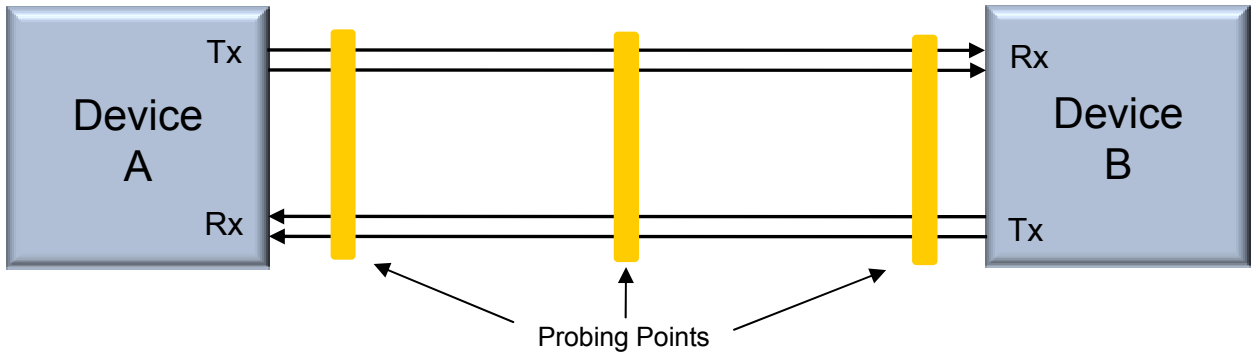
Challenges Selecting Tools for PCI Express 3.0

- Planning probe access
  - How access PCIe3 signals?
    - Is there a probe design guide available showing a variety of probing access?
    - Does it include mechanical KOV (Keep Out Volume) info?
    - Are PCB CAD symbols available for their midbus footprints?
    - Is probing available for legacy PCIe2 midbus footprints?
    - Is there a probe available that I can solder-down as a last resort?
  - How assess the probing impact?
    - How is the PCIe3 signal recovered without breaking the link?
    - What is the maximum PCIe3 channel length supported?
    - Are electrical load models of all probes available for computer simulation?
  - How flexible is the probing?
    - How long are the probe cables?
    - Can I reconfigure my PCIe3 probe channels if there are layout errors?

Primary Debug Challenges When Implementing PCIe 3.0



Probing Access

- Midbus vs interposer vs solder-down
- Need to compensate for Tx de-emphasis
- Need to compensate for channel loss
- Need to compensate for reflections

Link training

- Multi-lane systems x1, x4, x8, x16
- Dynamic speed negotiations 2.5 GTs → 5 GTs → 8 GTs 2.5 GTs → 8 GTs
- Dynamic link width changes x16 → x8 → x4 → x1

Active State Power Management (ASPM)

- Power Management: Electrical Idle Entry and Exit for power savings (L0 → L0s → L0)
- Dynamic link width and link speed changes depending on data bandwidth requirements

Total System Visibility

- Critical cross bus dependencies increase with speed
- Flow Control
- Time-correlated visibility across multiple buses
- Signal access across the entire system

Link training and power management continue to be the most difficult challenges!

Challenges Selecting Tools for PCI Express 3.0

- Planning probe access
  - Accessing PCIe3 signals
  - Assessing probing impact
  - Probing flexibility
- Time to confidence
  - Automating setup
  - Recovery options
  - Powerful triggering
  - Wide acquisition window
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  - Four (4) different data visualizations that provide views dedicated to different types of investigations:
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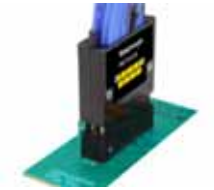
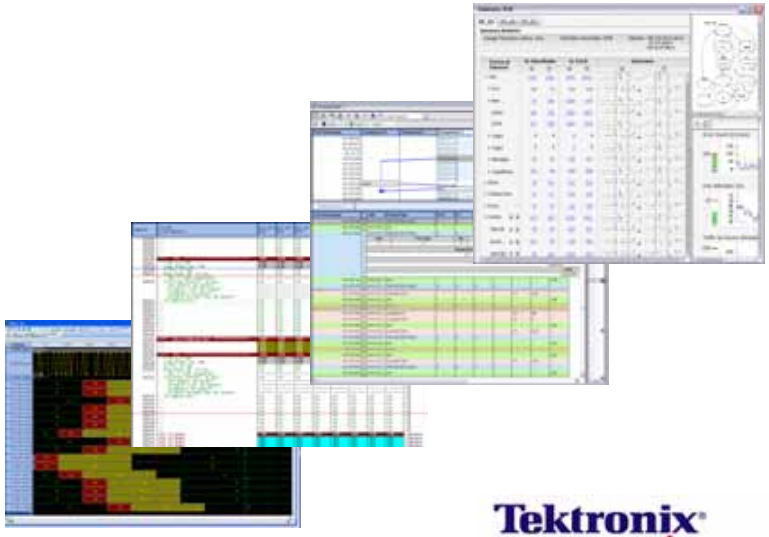
  - Summary Profile Window





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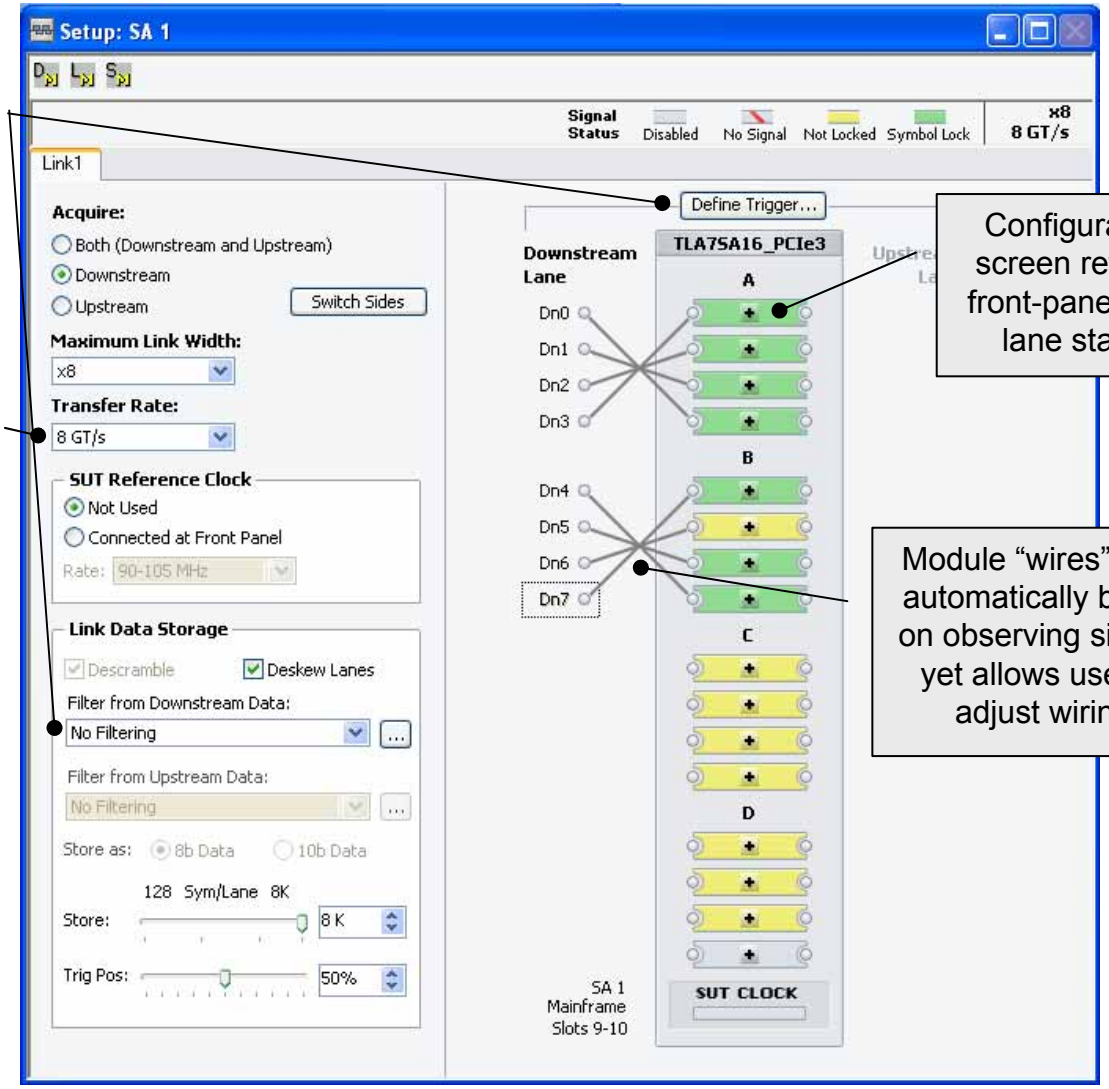
Challenges Selecting Tools for PCI Express 3.0

- Time to confidence
  - Does the analyzer automatically configure?
    - Are there real-time statistics that show bus utilization, link width, etc. so that I can get an overall indication of the link health?
    - Does the GUI show the health of each lane?
    - Are there front-panel LEDs that show me the status of the link?
  - What options do I have if I can't get the analyzer to automatically configure?
    - Is there an option to use my oscilloscope so that I can see whether my signal meets the input requirements or whether the probe is inoperable?

PCIe3 Setup Window

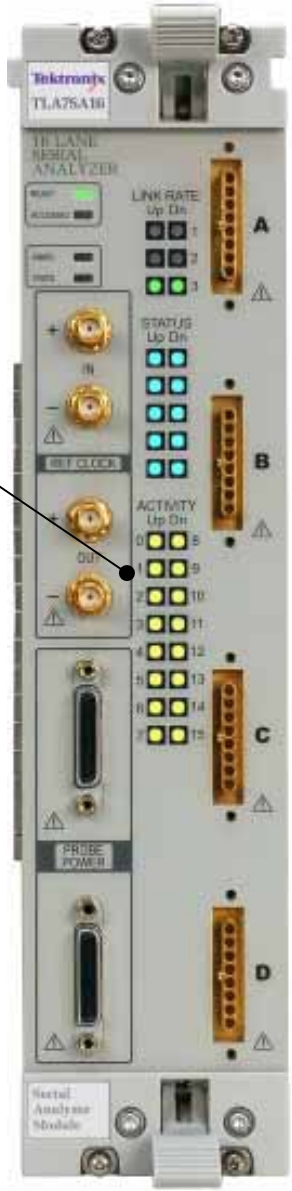
Additional key hardware settings (filtering, triggering) easily accessed

Auto-training, auto-tracking as well as manual modes



Configuration screen reflects front-panel LED lane status

Module "wires" itself automatically based on observing signals yet allows user to adjust wiring



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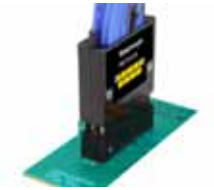
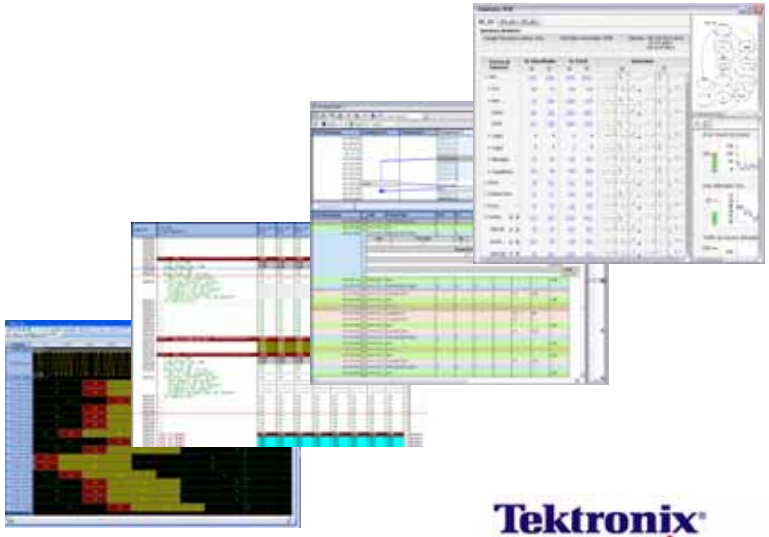
Challenges Selecting Tools for PCI Express 3.0

- Planning probe access
  - Accessing PCIe3 signals
  - Assessing probing impact
  - Probing flexibility
- Time to confidence
  - Automating setup
  - Recovery options
  - Powerful triggering
  - Wide acquisition window
- Information density
  - Four (4) different data visualizations that provide views dedicated to different types of investigations:
    - Summary statistics window
    - Transaction window
    - Listing window
    - Waveform window
- Applications
  - Transaction Window – Intro
  - Transaction Window – Normal Traffic
  - Transaction Window – Transaction Error
  - Transaction Window – Physical Layer
  - Summary Profile Window





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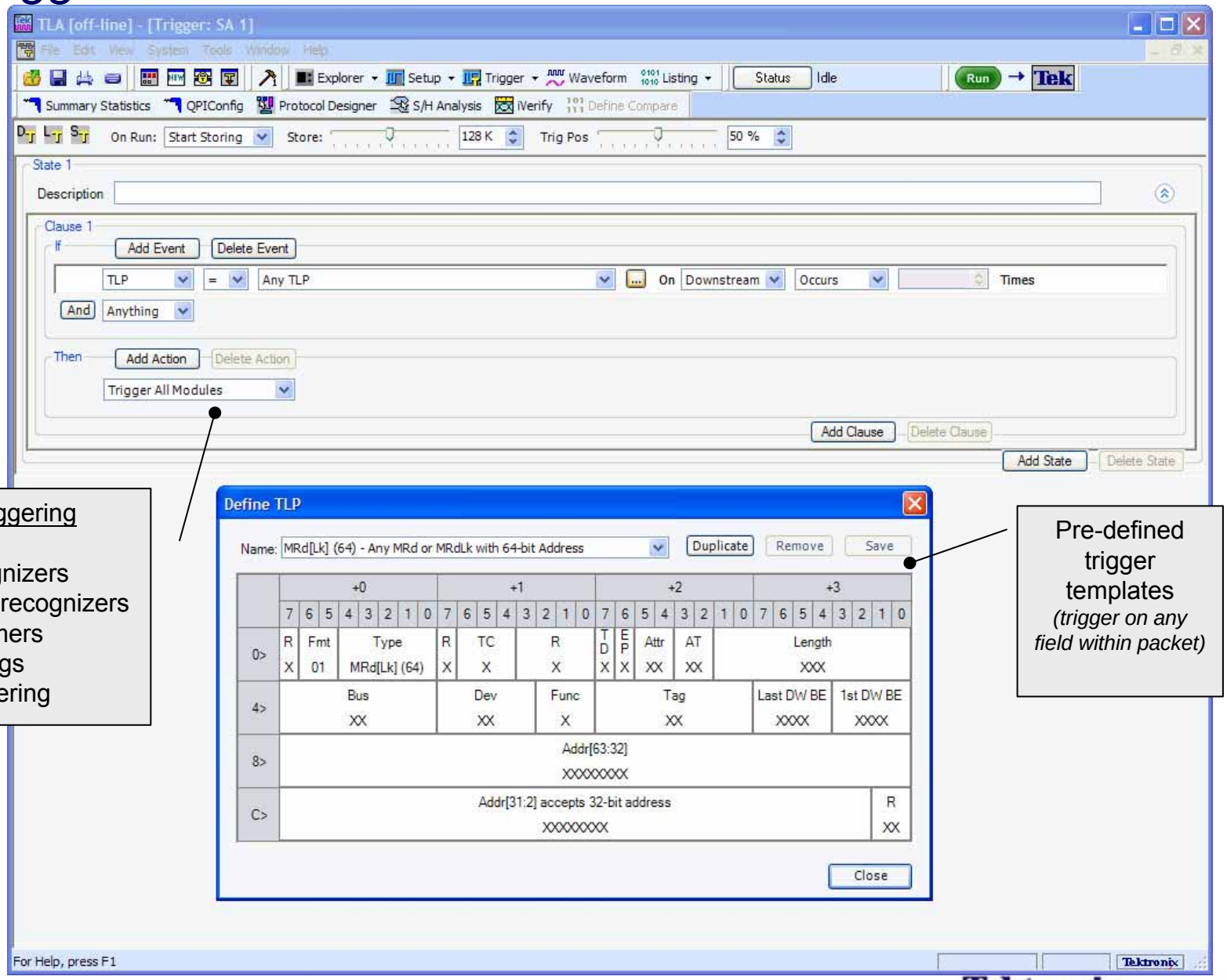
Challenges Selecting Tools for PCI Express 3.0

- Information density
  - How powerful is the triggering?
    - Can I trigger on ordered sets or packet types?
    - Can I trigger on errors, e.g., loss of framing, illegal sync characters?
  - How wide is the acquisition time window?
    - Can I control what gets stored?
    - How fast can I access and move around within the acquisition record?
  - What information do each of the data windows provide?
    - **Summary Profile** (Statistics) **-** *Acquisition summary statistics* based view of protocol elements (distribution of protocol elements across acquisition)
    - **Transaction -** *Link* based behavior of protocol elements (transactions, packets, fields, ordered sets)
    - **Listing -** *Lane* based behavior of protocol elements (symbols, tokens, ordered sets, DLLPs, TLPs)
    - **Waveform** - *Time* based view of the data on each lane
  - Can I correlate data from my PCIe3 bus with other buses (e.g., DDR3) and see it all on a single display?

PCIe3 Trigger Window



Packet level triggering
8 states
8 packet recognizers
4 symbol sequence recognizers
4 counter/timers
4 event flags
Real-time filtering

Pre-defined trigger templates *(trigger on any field within packet)*

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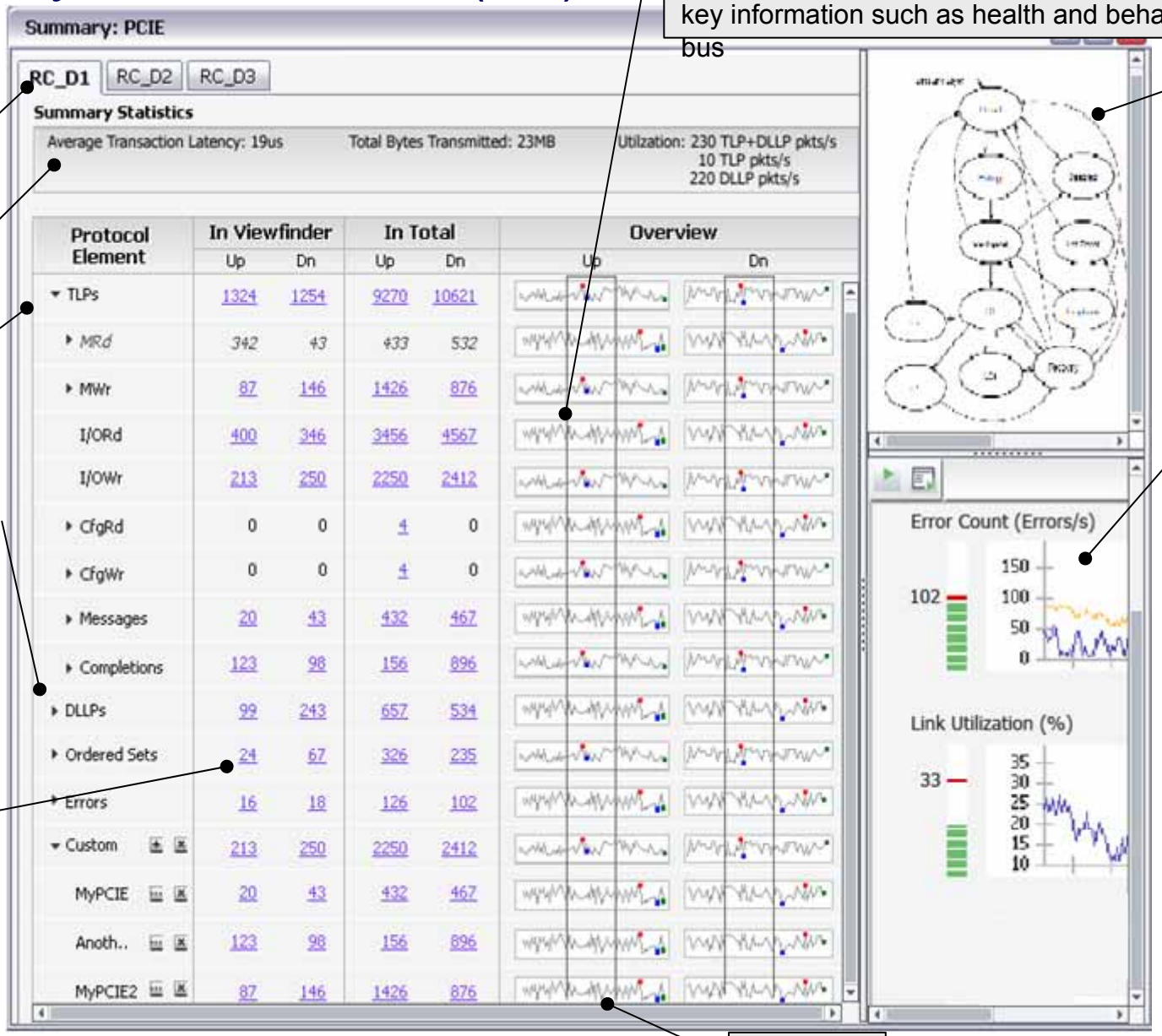
Summary Profile Window (1/2)



"At a glance" review of sparklines (divides acqmem into 100 slices or centiles) provides key information such as health and behavior of bus

1 or more Links

Summary statistics

Trace elements view

Each protocol element represented with its statistics

1st occurrence hyperlink

LTSSM view

Real-time statistics view (utilizes module acquisition HW)

Region markers

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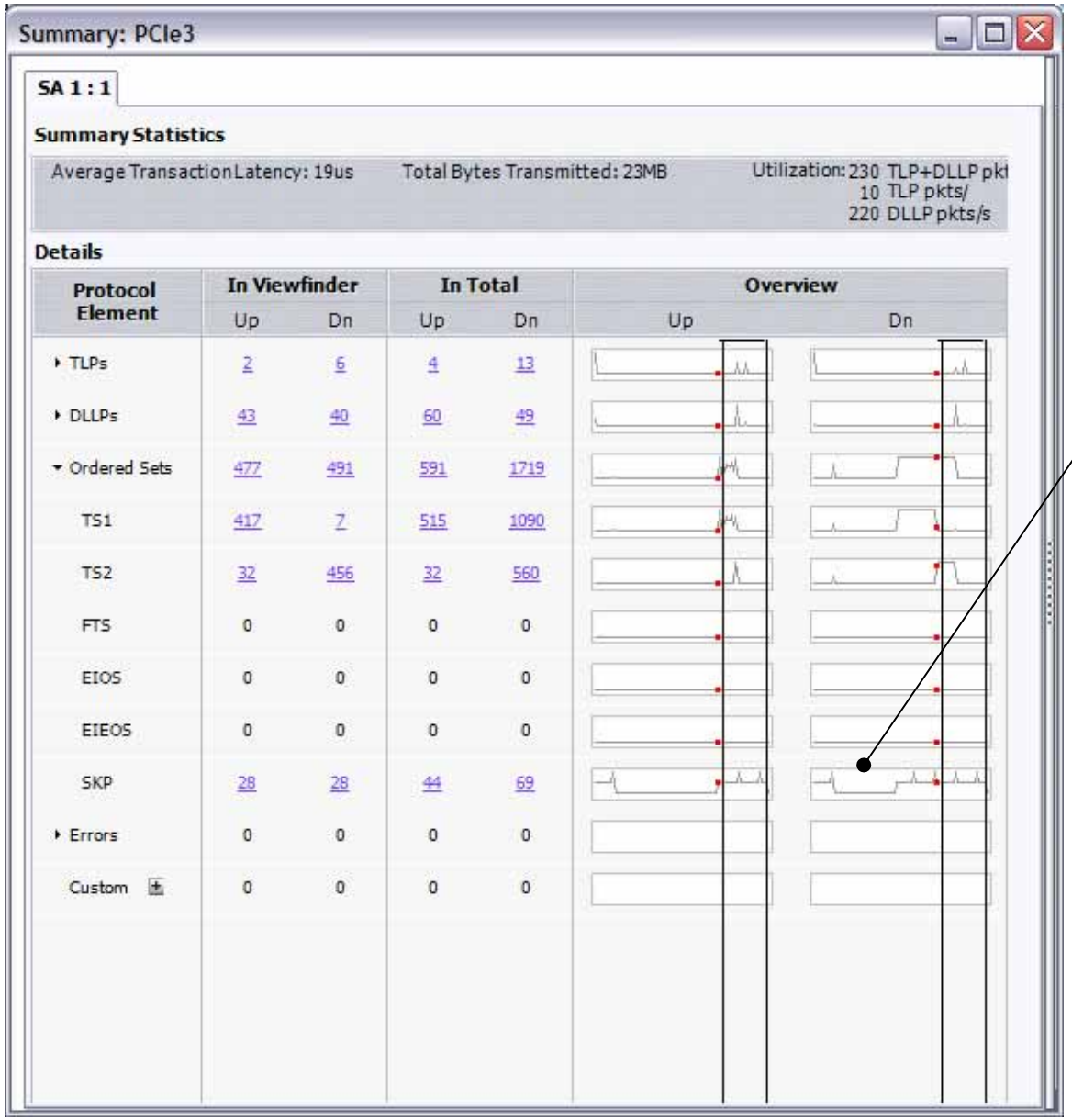
Summary Profile Window (2/2)



Visually see training occur by recognizing patterns. For example, can see electrical idle (gap in SKP) followed by training (TS1 & TS2).

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Transaction Window (1/3)

Transaction stitching shows packets participating in transaction – or incomplete transactions as errors – mouse over shows time – arrowheads/squares filled or not based upon completion

Toolbar (Search, filter, display management)

Status bar & access to "Summary Profile Window"

Each row of the Packet View pane represents a single packet

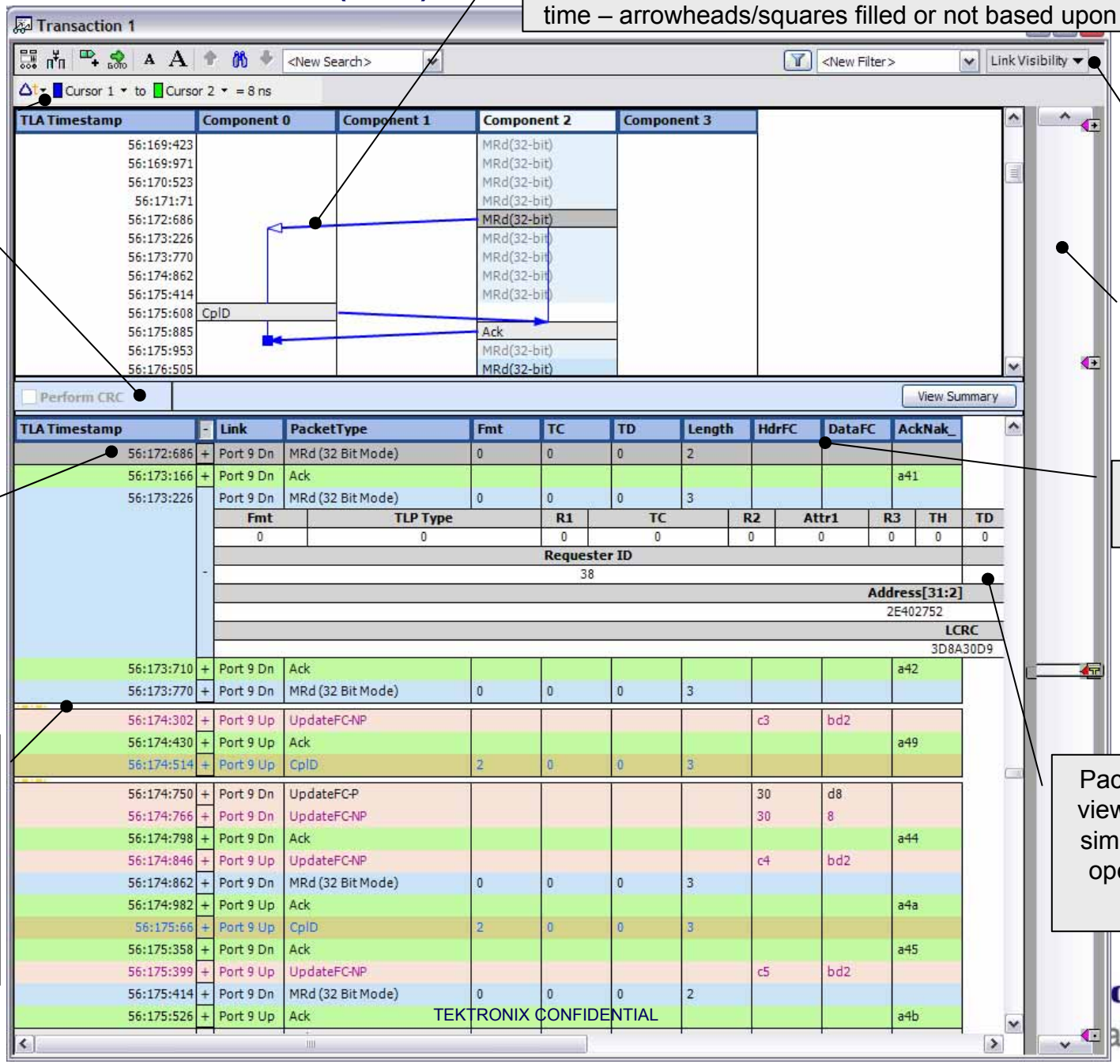
PHY layer info (shows sub-packet info such as ordered sets – view in more detail in Listing Window)

Config Links

BEV (Bird's Eye View)

Flow control credit tracking

Packet pane to view fields (can simultaneously open multiple packets



Transaction Window (2/3)

Transaction stitching shows packets participating in transaction

Toolbar (Search, filter, display management)

Status bar & access to "Summary Profile Window"

PHY layer info (shows sub-packet info such as ordered sets – view in more detail in Listing Window))

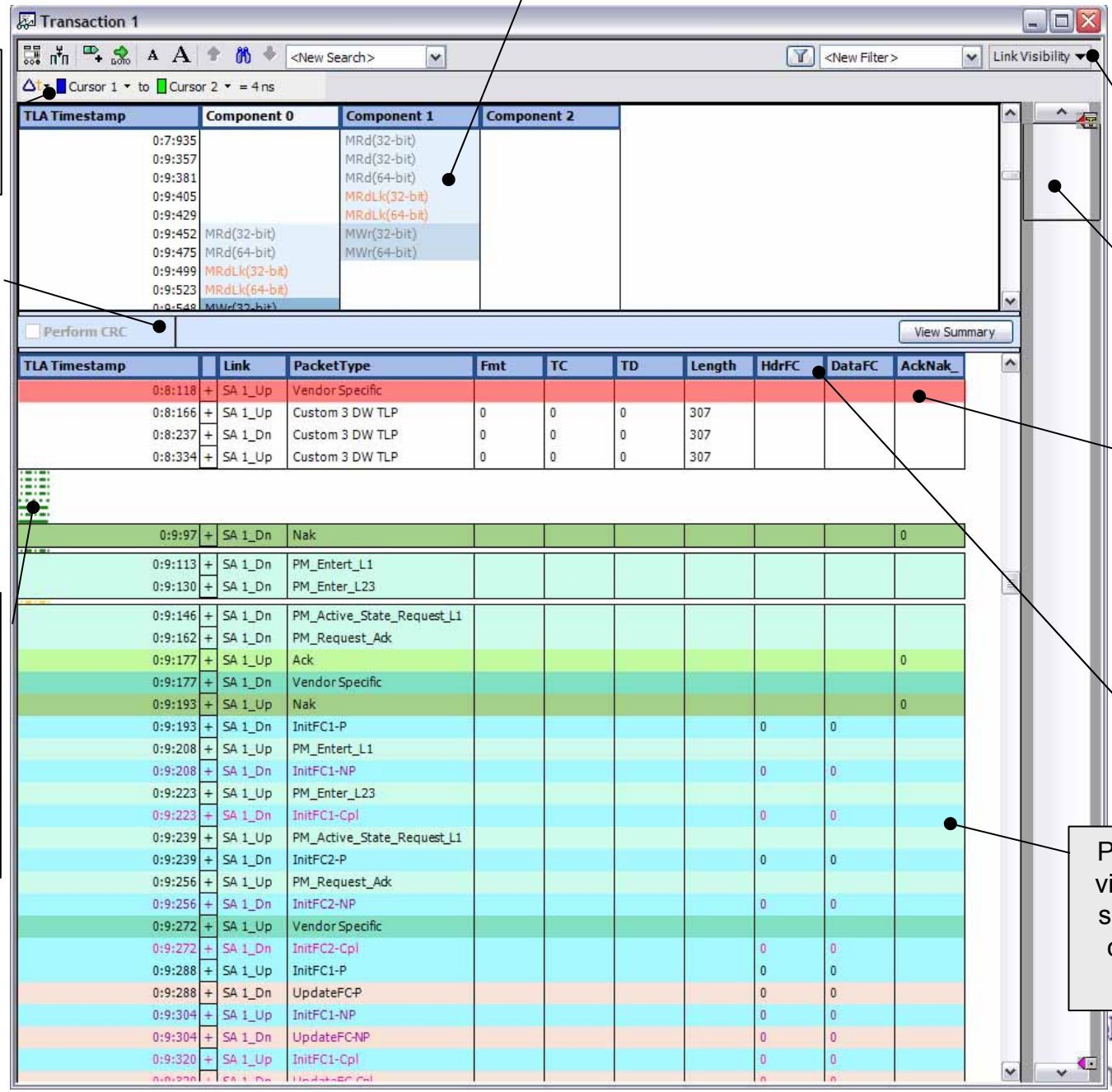
Config Links

BEV (Bird's Eye View)

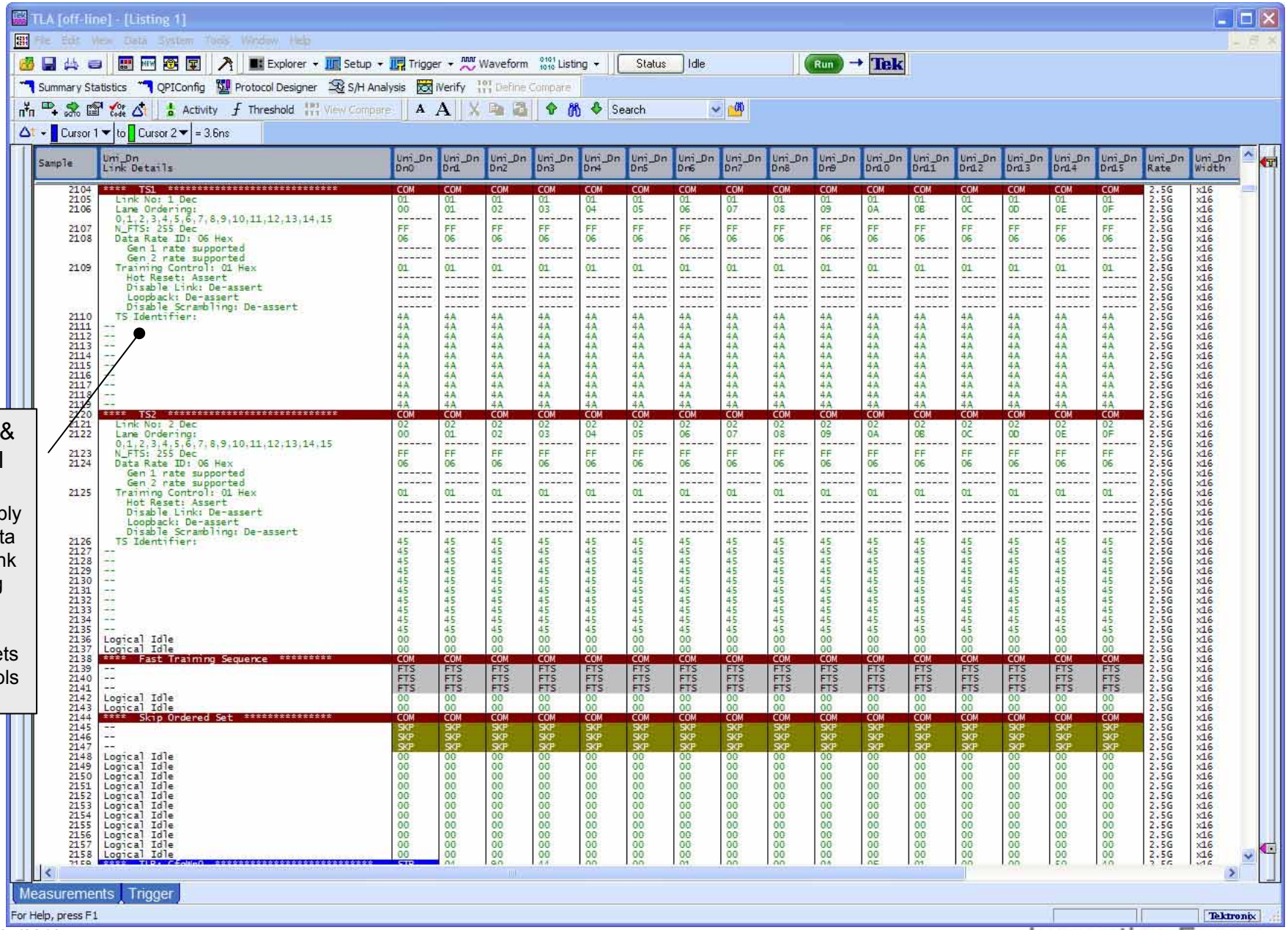
Color-coding to distinguish normal traffic from error conditions

Flow control credit tracking

Packet pane to view fields (can simultaneously open multiple packets)



Listing Window



Packet & Symbol View (disassembly of lane data on each link including TLPs, DLLPs, ordered sets and symbols

Waveform Window

Waveform symbolic decode (lane alignment disabled for accurate time correlation)

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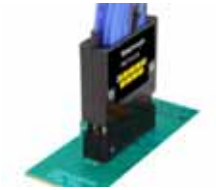

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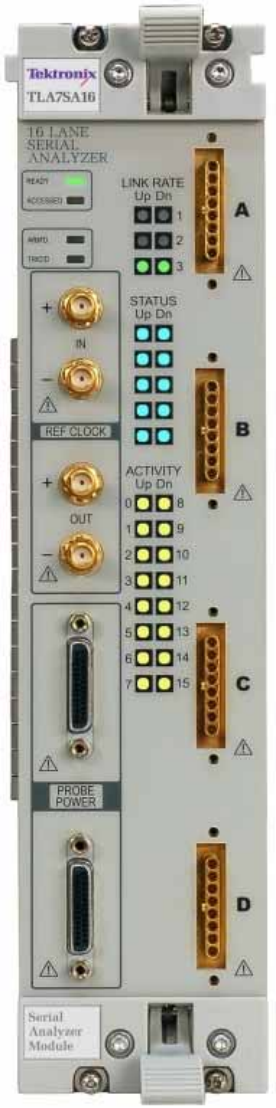
PCI Express 3.0 Acquisition Solutions



- 8.0 GTs, 5GTs, and 2.5GTs acquisition rates for PCIe3/2/1
- Sync to L0s within 4 FTS PCIe3 packets or 12 FTS PCIe2 packets
- Automatic configuration of link training speed changes and link width
  - Track 2.5 GTs to 5.0 GTs to 8.0 GTs data rate changes without dropping parts of transactions or critical packets
  - Dynamically track changes in link width
  - Front-panel LEDs that show link rate and link status for both Upstream/Downstream links
- Powerful trigger state machine spans all layers of the protocol
  - 8 states
  - 8 packet recognizers
  - 4 symbol sequence recognizers
  - 4 counter/timers
  - 4 event flags
  - Conditional storage
- 8 GB memory/module (16 GB memory, x16 link) with 160 Msymbols/lane record length
- Two acquisition modules available:
  - 16 differential inputs, x8 (2 required for x16)
  - 8 differential inputs, x4

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Tektronix PCIe3 Probes – With Active Equalization

Slot Interposer Probes

- Available in x16, x8, x4, x1 link widths
- Probe cover
- Bracket for SUT end point card provides mechanical stabilization and reliable connection
- 6’ probe cable
- Ships in antistatic, foam-lined, plastic case

Midbus Probes

- Available in x8 or x4 link widths (2 for x16)
- Rugged probe head with contacts contained in retention module
- Retention module securely attaches to PCB (0.031” to 0.250”) using back mounting plate with screws
- Midbus probe also available for legacy PCIe2 x16 midbus footprint
- 6’ probe cable
- Ships in antistatic, foam-lined, plastic case

Solder-down Probes

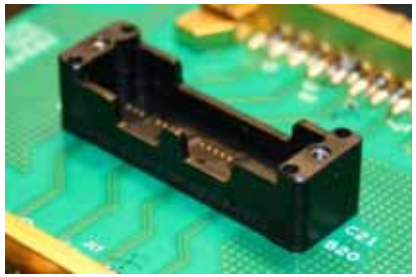
- High-performance solder-down probing of one (1) PCIe3 differential pair
- Supports 8 GT/s
- Compatible with P7500 Series TriMode probing leadsets that can be shared with oscilloscope
- 6’ probe cable
- Ships in antistatic, foam-lined, plastic case

Midbus footprint (PCB land pattern) support

TLA7SAxx
PCIe3 Module

P67SA16 x8 midbus probe
P67SA08 x4 midbus probe

8 GT/s



P67SA16G2 x8 midbus probe

5 GT/s

TLA7Sxx
PCIe2 Module

5 GT/s

P6716 x8 midbus probe
P6708 x4 midbus probe

P67SA16G2

PCIe **Gen2** midbus probe head

P67SAxx Series PCIe Gen3 midbus probe with **16** diff inputs

TLA Mainframe Solutions

TLA7012 2-module mainframe
Shown with 2 TLA7SA16 modules for x16 PCIe3 link

- Mainframe with integrated 15” display and PC controller
- Connects to PC via GbE for running TLA Application Software

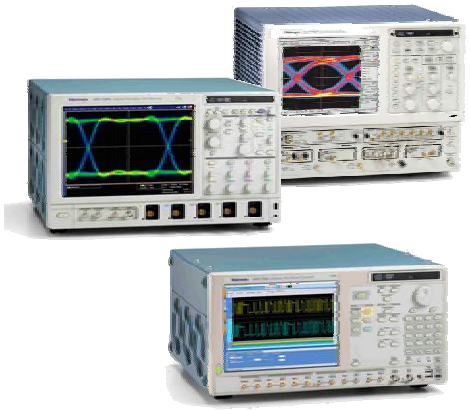
TLA7016 6-module mainframe
Shown with 2 TLA7SA16 modules for x16 PCIe3 link

TLA7016 6-module mainframe
Shown with 2 TLA7SA16 modules for x16 PCIe3 link & 4 TLA7BB4 modules for 2 channels DDR3-1600

- Mainframe with GbE controller
- Connects to PC via GbE for running TLA Application Software
- Up to 8 frames interconnected via TekLink

PCI Express Test Summary

- Tektronix is heavily involved in PCI Express Standards Development
  - Electrical Working Group (EWG) for Base Specification Development
  - Card Electromechanical Group (CEM) for CEM Specification Development
  - Serial Enabling Group (SEG) for Compliance Program
- PCI Express 3.0 specification is at 0.7 (.9 draft)
  - Expect Rev 0.9 spec. in Q2 2010
- Physical layer testing
  - De-embedding important for accurate measurements
  - Minimum 12 GHz bandwidth scope for validation
  - DPOJET for measurement automation and test reporting
  - SDLA for measurement-based link analysis
- Protocol validation and debug
  - TLA7000 series mainframes and TLA7SAxx serial acquisition modules
  - Flexible probing and triggering
  - Data visualization
  - Cross-bus analysis



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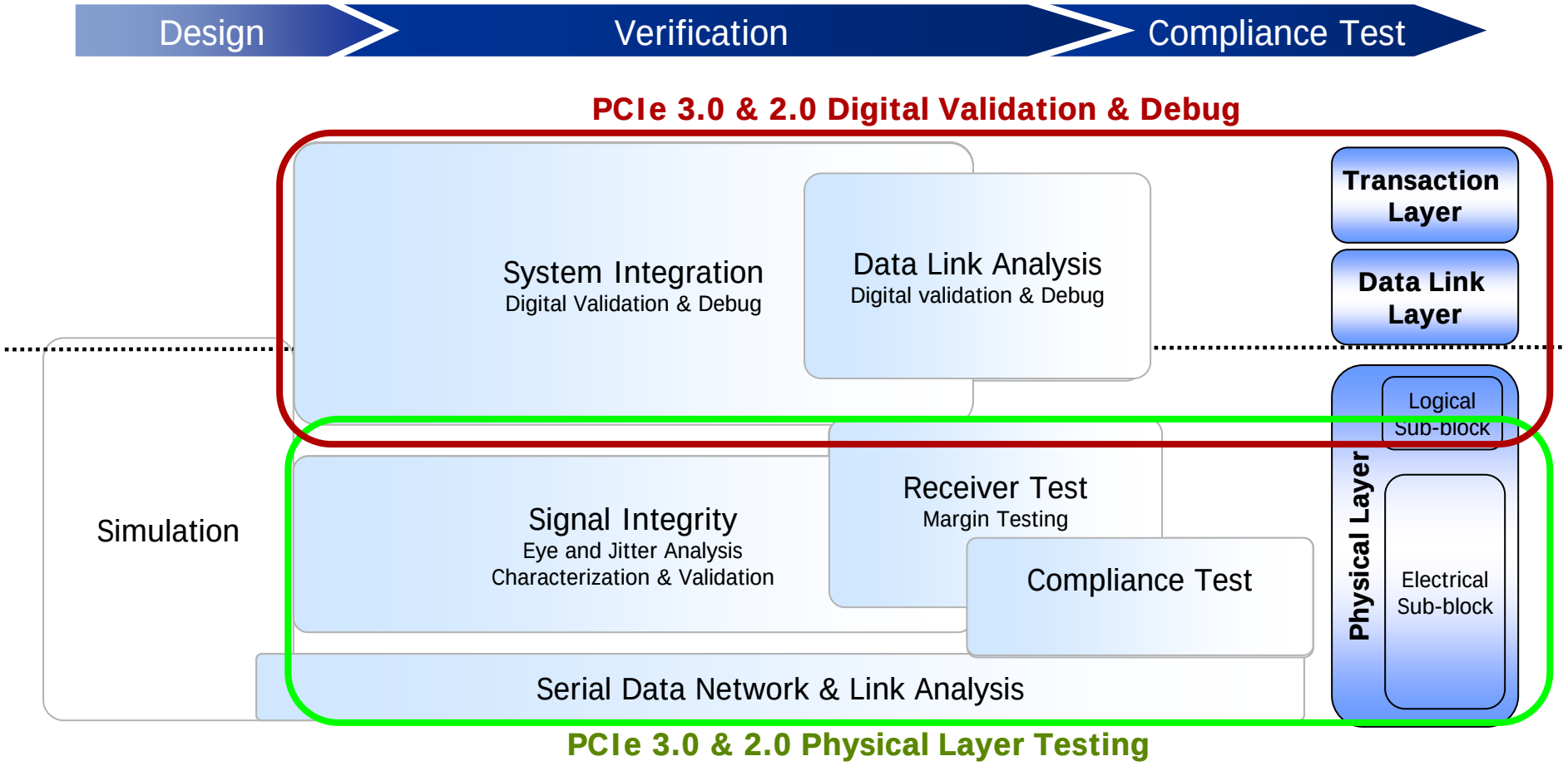
Proven Expertise in High Speed Serial Data Design & Test

High-Speed Serial Data Test Solutions



Most Complete Serial Data Test Coverage