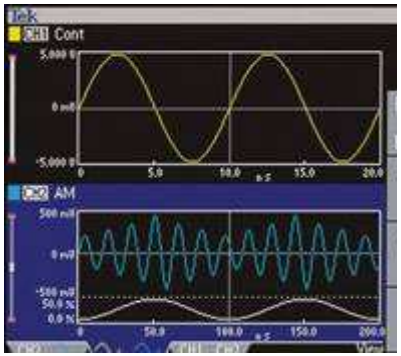
Validating and Debugging DDR2, DDR3 SDRAM Designs

- Comprehensive Test solution from Analog to Digital Validation for All DDR Versions



name

title

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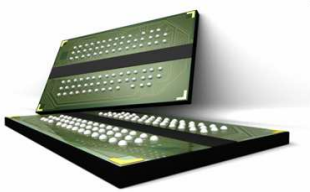
Innovation Forum

Memory Design and Validation

Chip/Component Design

- Precise understanding of circuit behavior under range of conditions
- Margin testing



System Integration

- Signal integrity and timing analysis, discovery of issues under nominal conditions
- Debug interoperability issues

Embedded Systems

- Easy test setup
- Quick pass/fail results

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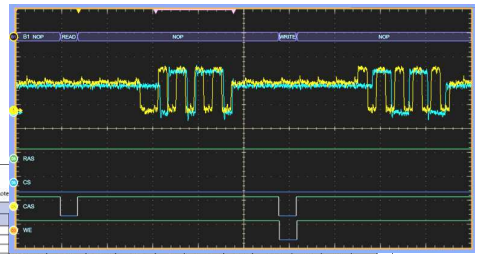
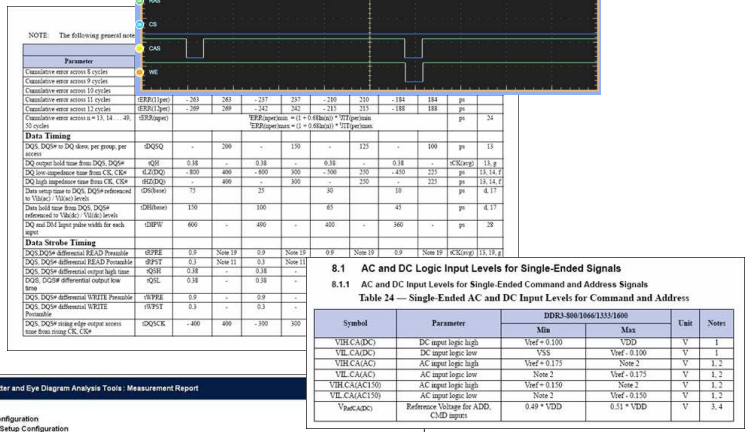
DDR Test Challenges

- Signal Access & Probing
  - Easy-to-use / reliable connections
  - Bandwidth & Signal Integrity
  - Affordable
- Isolation of Read/Write bursts
  - Triggering or Post-Processing
- Complexity of JEDEC Conformance Tests
  - Parametric timing/amplitude measurements
  - Vref / Vih / Vil, Derating
- Results Validity / Statistics
- Effective Reporting / Archiving
- Advanced Analysis
  - Characterization
  - Debug



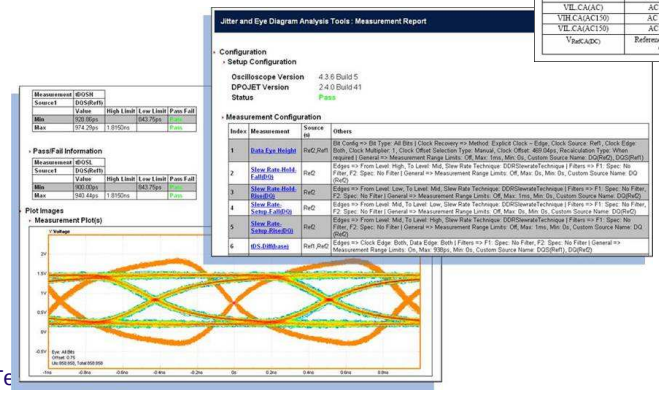


8.1 AC and DC Logic Input Levels for Single-Ended Signals

8.1.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 24 — Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600 Min	DDR3-800/1066/1333/1600 Max	Unit	Notes
VIH.CA(DC)	DC input logic high	Vref + 0.100	VDD	V	1
VIL.CA(DC)	DC input logic low	VSS	Vref - 0.100	V	1
VIH.CA(AC)	AC input logic high	Vref + 0.175	Note 2	V	1, 2
VIL.CA(AC)	AC input logic low	Note 2	Vref - 0.175	V	1, 2
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note 2	V	1, 2
VIL.CA(AC150)	AC input logic low	Note 2	Vref - 0.150	V	1, 2
$V_{REFCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4



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Fast & Accurate instrument solutions

DDR, DDR2 & DDR3 SDRAM Solutions

Signal Path Characterization and Circuit Board Verification

D*SA Sampling Oscilloscopes*

Verify correct design and circuit board performance

Analog & Electrical Debug

DPO/DSA real time scopes & software

Signal integrity measurements

Digital Validation & Debug

TLA Logic Analyzers with Nexus & FuturePlus

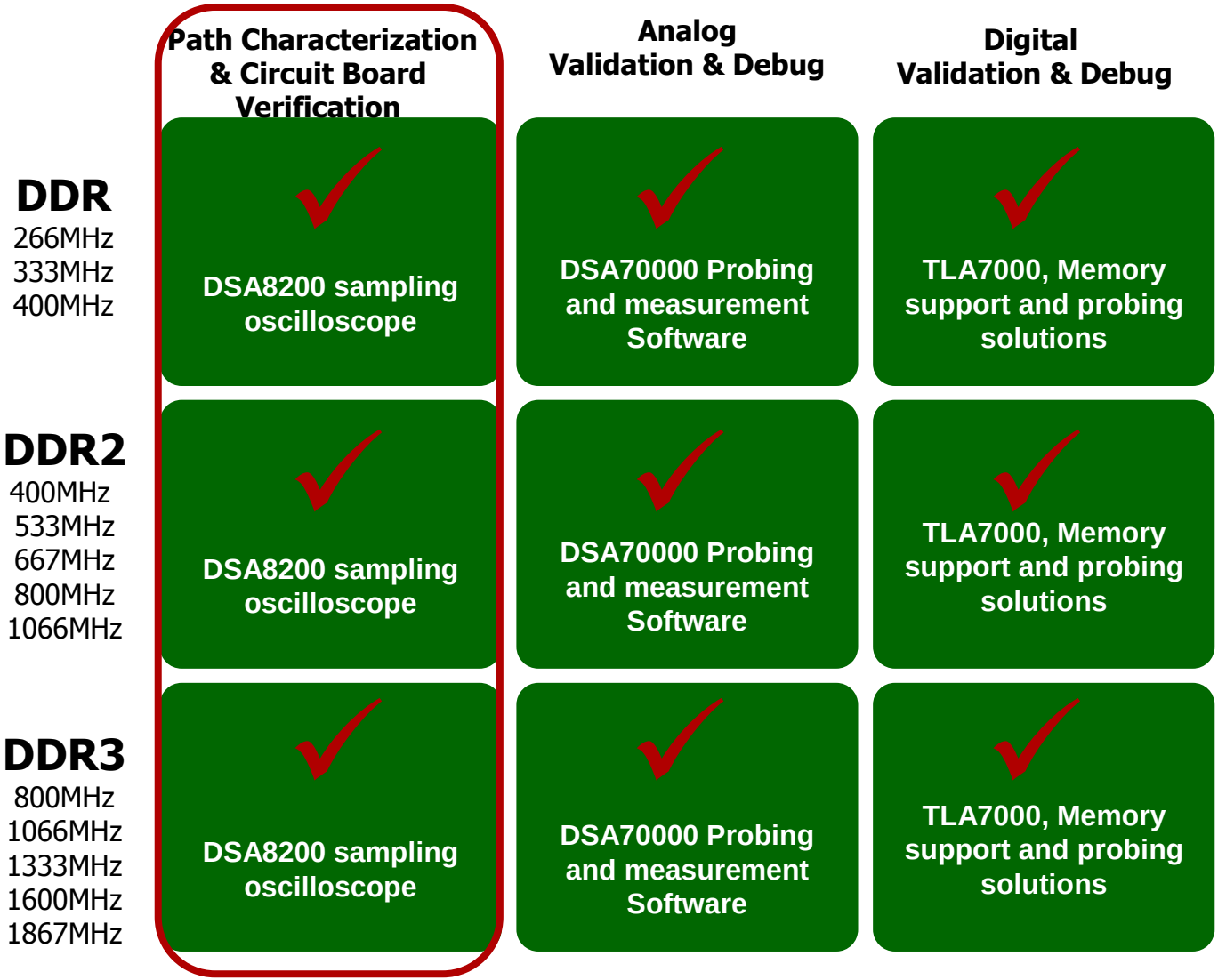
Technology memory supports

Verify and debug command sequence, timing, data, and more

SDRAM Probing Solutions

Easy and reliable physical connection with minimal loading

Tektronix DDR Test Solutions



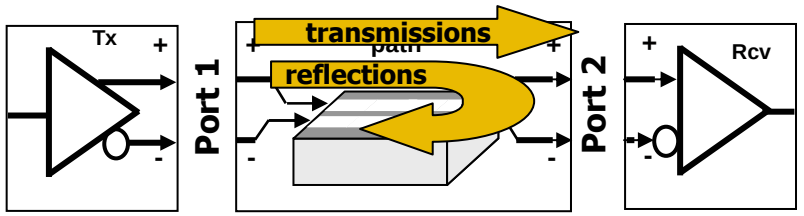
Problem: verify correct design and performance

Path Characterization & Circuit Board Verification

Characterize board/DIMM with TDR and S-Parameters

Frequency-domain characterization of reflections and loss in a network

Quantitative insight into the causes of signal integrity problems



Measurements:

- Impedance measurements
- Insertion & Return Loss
- Frequency domain crosstalk

Verify correct design and circuit performance

Path Characterization & Circuit Board Verification

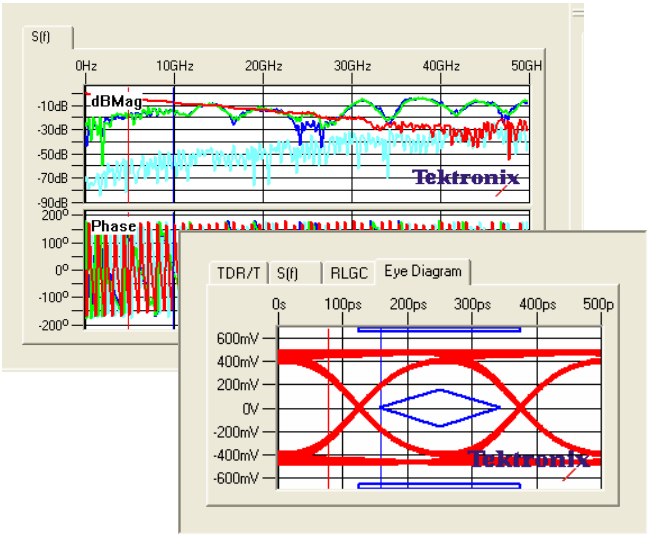
DSA8200 Sampling Oscilloscope with TDR and S-parameter generation software

Performance

- Over 70GHz sampling bandwidth & lowest Jitter floor
- Improved impedance measurement accuracy and resolution (Z-Line)
- 1M record length enables measurements of long interconnects at higher frequency

Efficiency & Simplicity

- Emulate channel effect on jitter & noise using TDR/TDT or S-parameter description
- Automated procedures minimize errors & reduce test time
- Complete analysis tasks in minutes not hours



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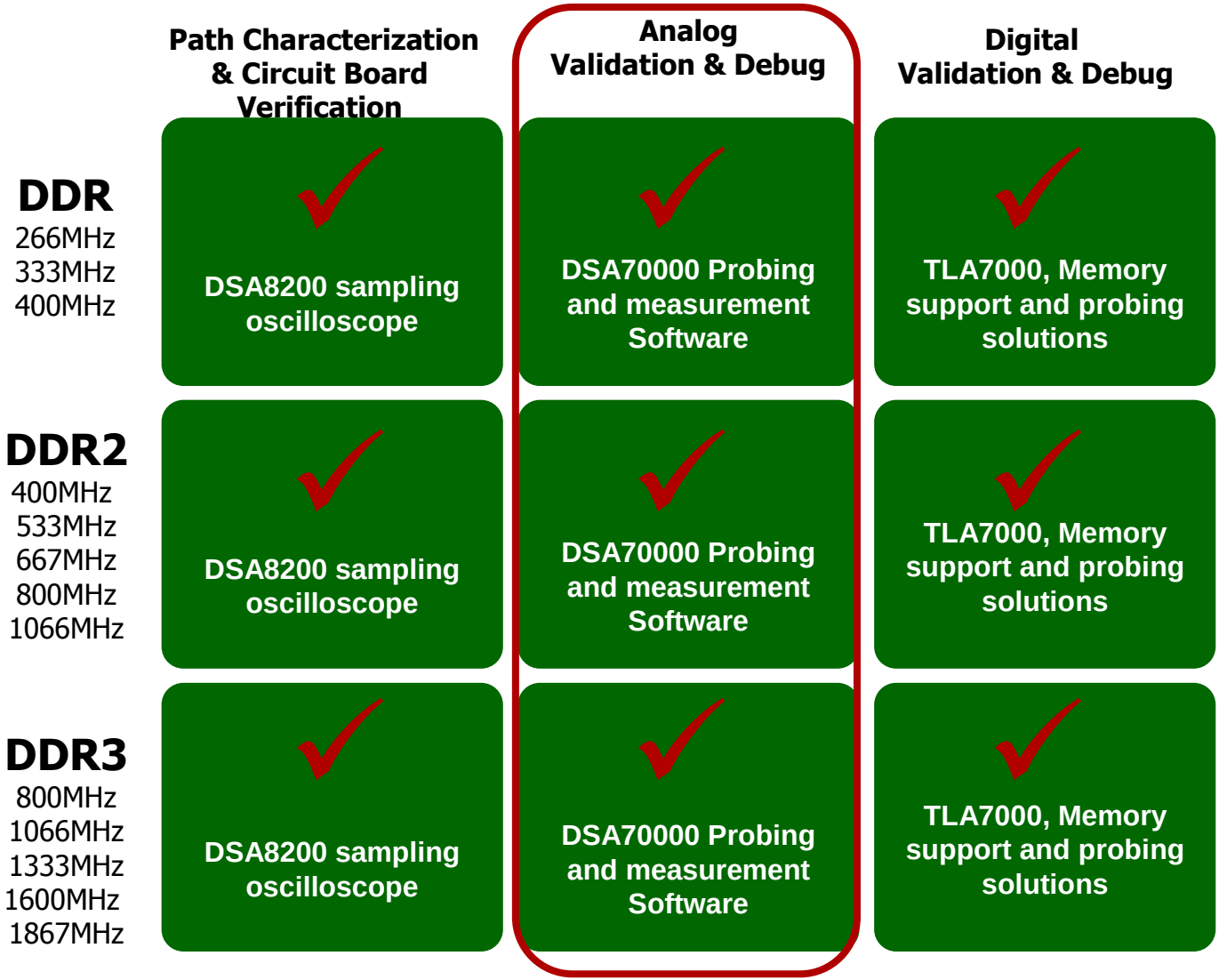
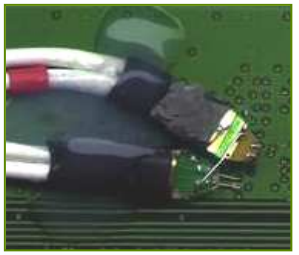
Tektronix DDR Test Solutions



DDR Analog Validation & Debug – Tektronix Solutions

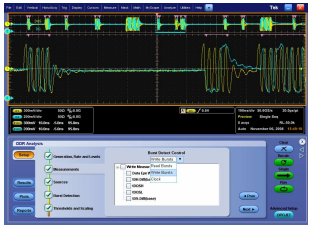
Signal Access - Probing

- Requires easy but reliable physical connectivity
  - access to various measurement points on DRAM or Memory
- Requires maximum signal integrity
  - sufficient performance for signal speeds



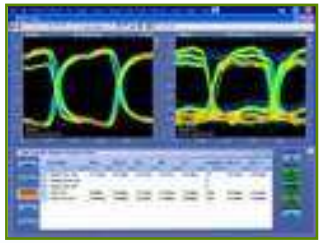
Signal Acquisition

- Automatically trigger and capture DDR signals
  - Identify and trigger directly on DQ, DQS in real-time to isolate Reads/Writes
  - Automatically set voltage levels and data rates
- Capture long time duration at high resolution
  - Direct connection to DPOJET for signal analysis



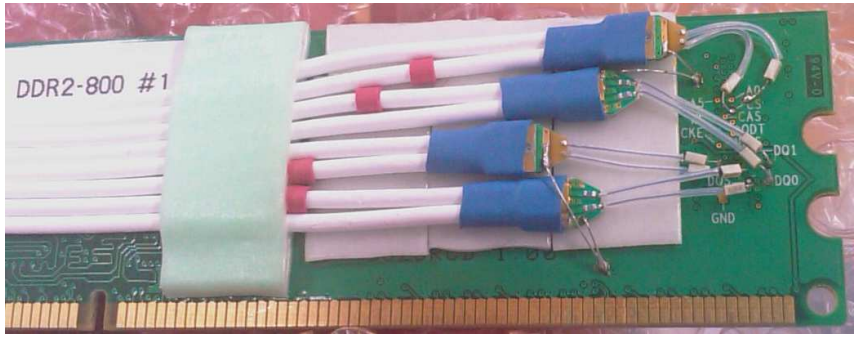
Signal Analysis

- DDRA – Automated setup, read/write burst detection, JEDEC pass/fail meas.
- DPOJET – The most powerful Jitter, Eye and Timing analysis tool
  - Time, Amplitude, Histogram, measurements
  - Advanced Jitter, Eye diagram measurements and Pass/Fail testing
  - Many display and plotting options
  - Report generator



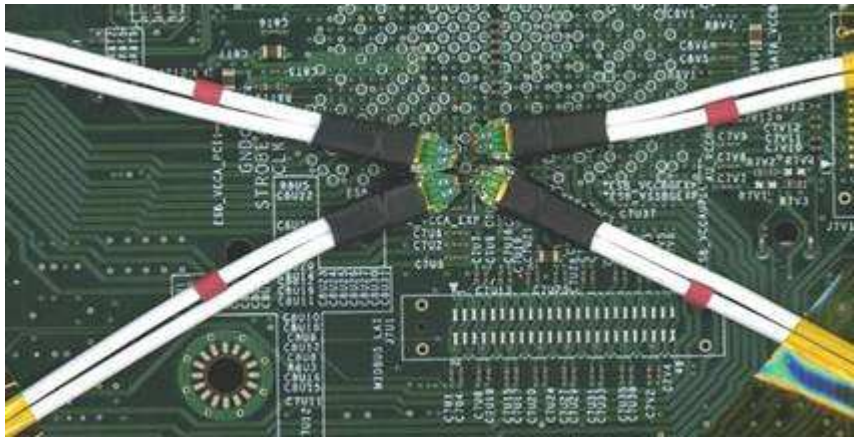
Signal Access Complexity

- Higher Data Rates Drive Probe Connection Complexity
  - Higher data rate = less margin
  - Higher signal fidelity requirements
  - Component geometries shrinking
  - Fine pitch pin spacing of <20 mils
  - Fewer & nearly inaccessible test points



DDR probing: signal integrity challenges

- Key Applications: Validation, Debug & Troubleshooting
  - Semi-permanent & reliable fine pitch solder down connections for repeatable system validation
  - Mobile probing without compromise for debug & troubleshooting requirements
  - Low cost leave-behind solder points for less critical measurements



Densely packed high-speed circuits stress probe access

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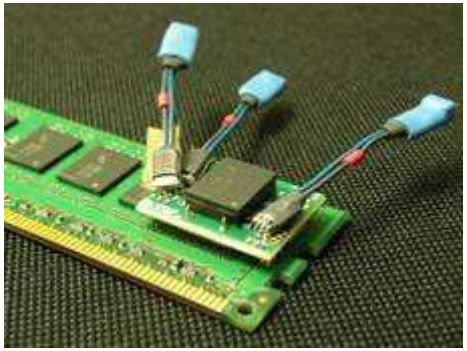
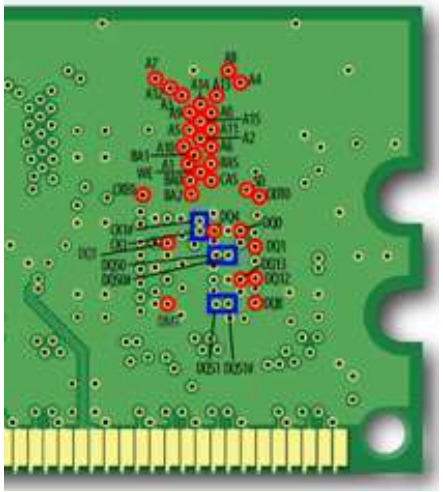
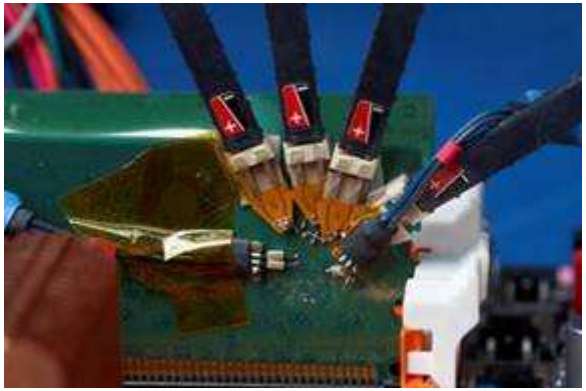
Signal Access

- Computer Systems use standardized DIMM's for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB
- All DDR2 & DDR3 Components use BGA Packages
- Probing a BGA package is Difficult
  - Unable to probe at the Balls of the Device
- Signal Access Solutions
  - Component Interposers
  - Direct Probing
  - Analog Probing
    - DQ, DQS, Clock
  - Digital Probing
    - Address
    - Command
    - Power, Reset, and Reference



Component Interposer





Analog and Digital Probing

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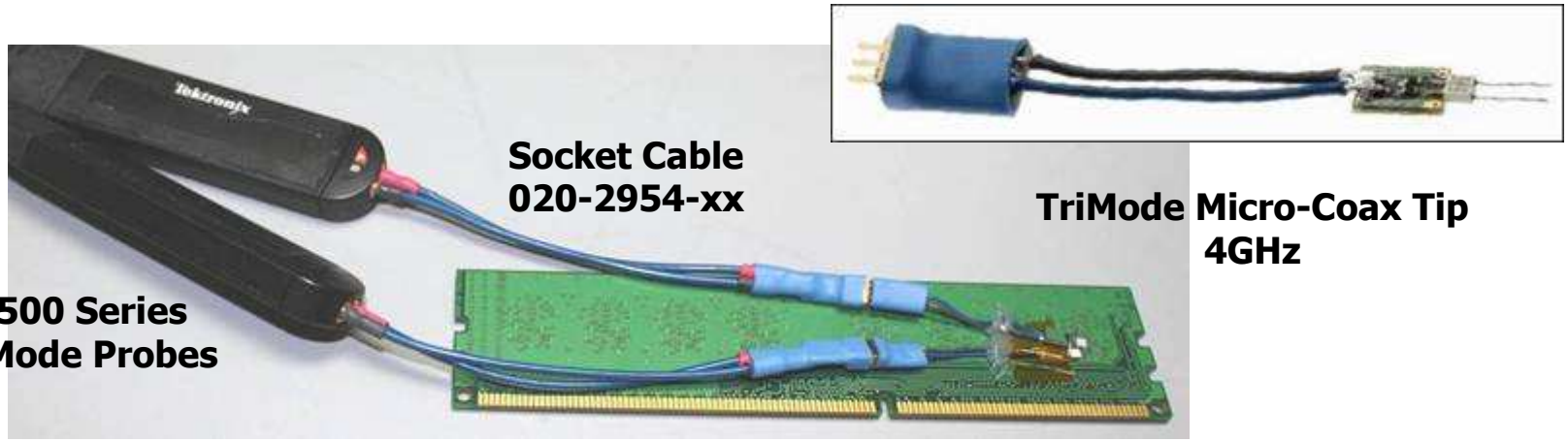
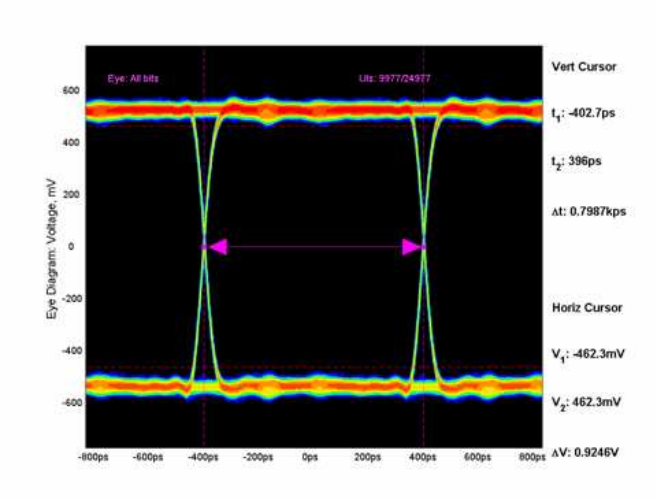
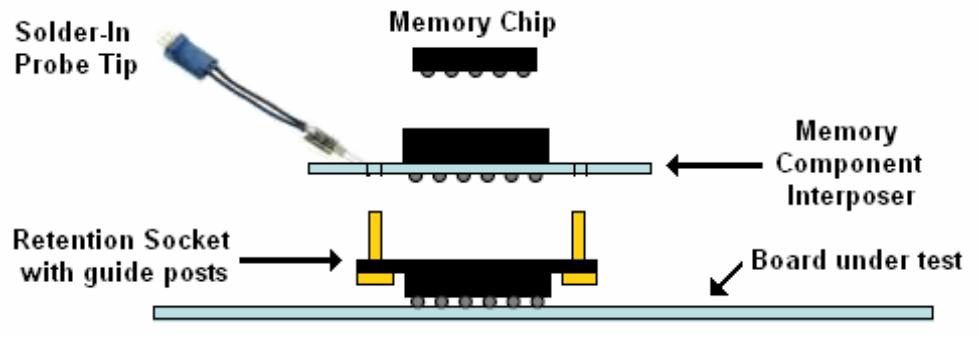
Analog Solder-In Probing Solutions



BGA Chip Access For DDR2, DDR3

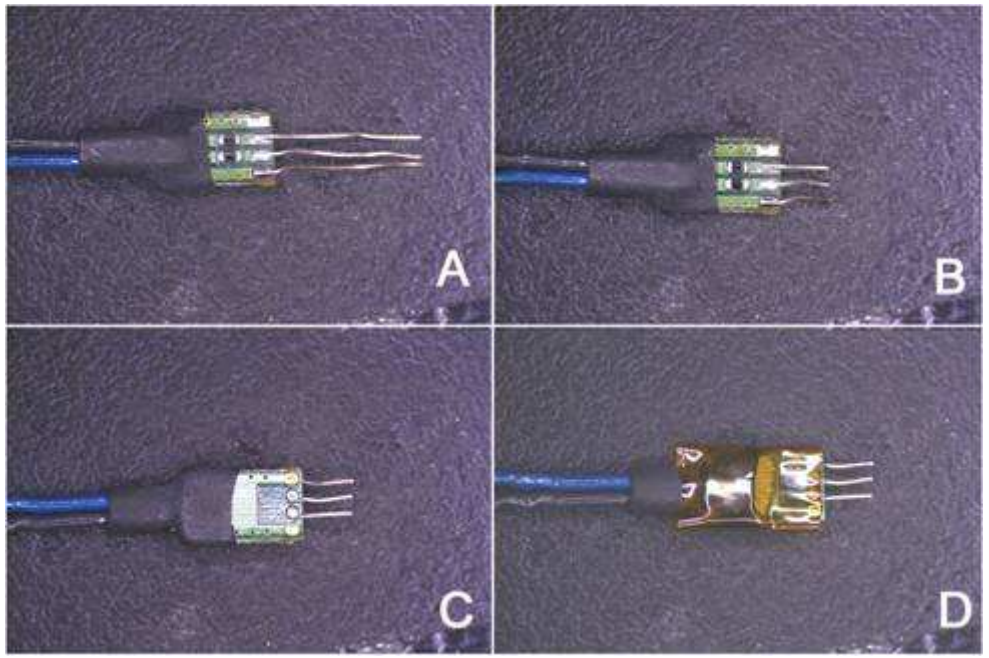
- Unique, reusable socket design allows for multiple chip exchanges
- Nexus DDR Interposers sold by Tektronix
  - DDR2 and DDR3 versions
  - X4/x8, x16 pins
  - Socket and solder models



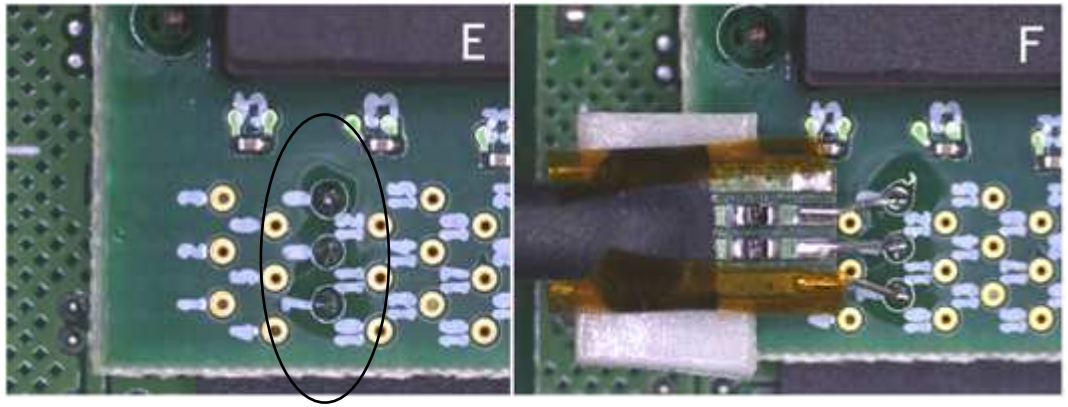


Soldering Probe Tips – Example

- A – Tip with long wires
- B – Wires cut short
- C – Back side of tip
- D – Tip covered with anti-static tape



- E – Solder placed on signal vias
- F – Tip soldered to vias and secured with tape



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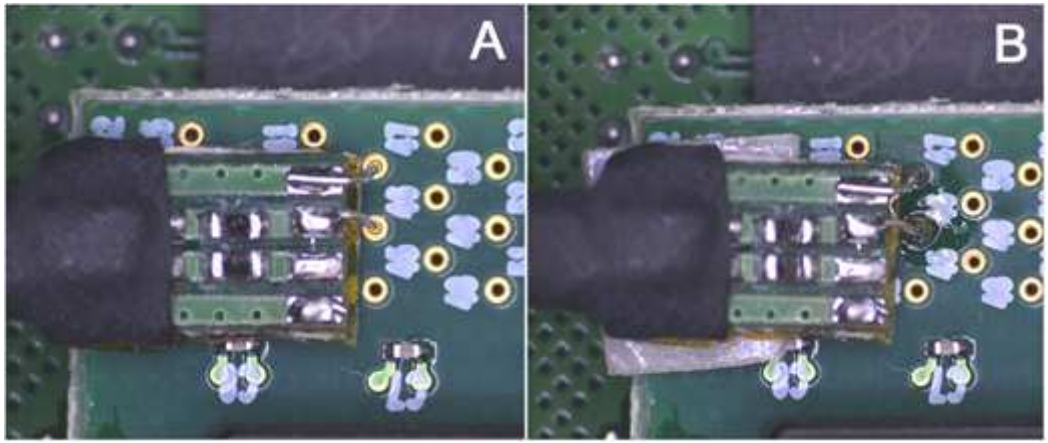
Soldering Probe Tips – Example (cont'd)

- A - Tip wires in via and ready for soldering
- B - Tip soldered to board



- All tips soldered to DDR Component Interposer
  - 5 signals of interest
  - A4, CK0, DQ0, DQS0, and CS2
  - Minimized wire length for best signal fidelity

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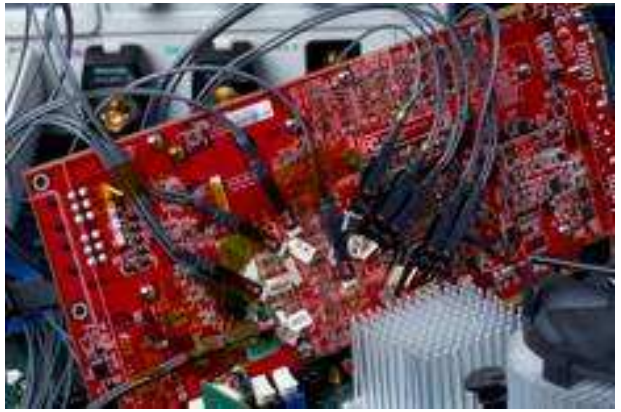
Mixed Analog and Digital Validation

- P6780 Active Differential Logic Probe
  - 16 channel + 1 Clock Qualifier (CQ)
  - 2.5 GHz bandwidth with low loading (<0.5pf)
  - Small form factor for high density circuit access
- P6717 Single-Ended Logic Probe
  - 16 channel + 1 CQ
  - > 350 MHz bandwidth
  - General purpose mixed signal applications
- iCapture on MSO70000
  - Route digital signal through analog system
  - Removes need for double-probing



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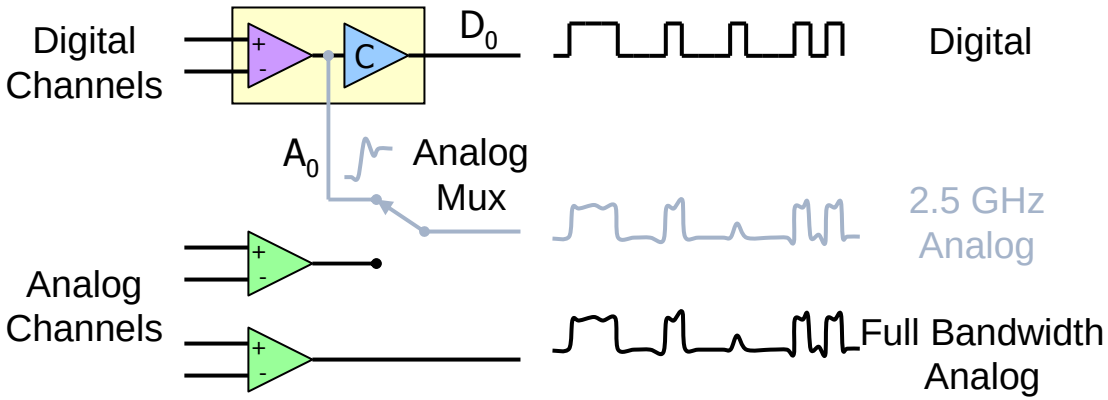
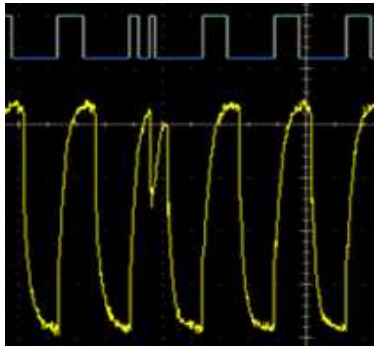
iCapture™ - One Connection for Analog and Digital

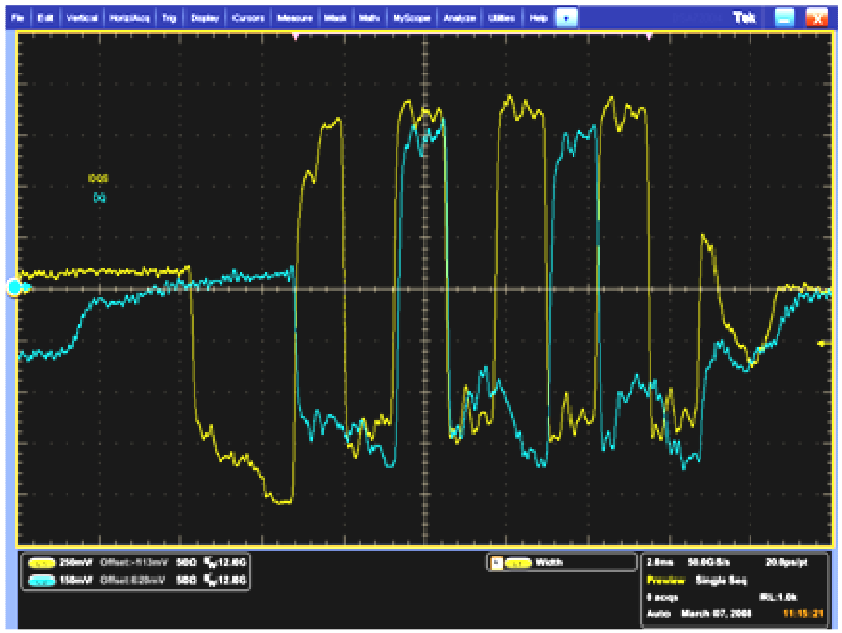
- Industry's only single probe connection for analog and digital
  - Measurement flexibility while preserving signal access
  - No need to reconfigure probing
- Quickly route any digital channel to any analog channel – *Simultaneously*
  - See both digital and analog views of the same signal
  - Validate signal connection, logic threshold
  - Check signal integrity, improve timing resolution



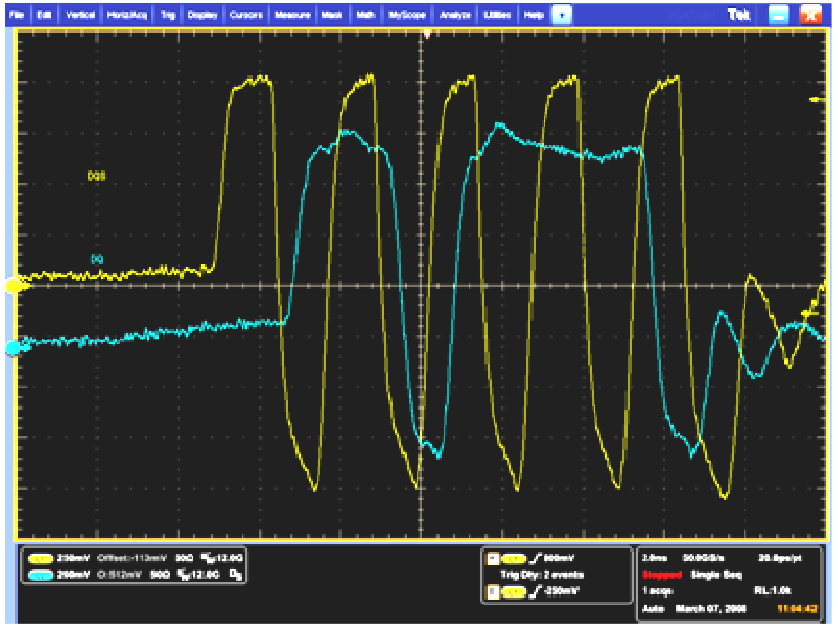


Read/Write Burst Identification

- Locate the right kind of bursts (read vs write)
- Locate the precise edges of each burst
- Refine burst identity based on other criteria (rank, secondary bus state, etc)



DDR3 Read Burst



DDR3 Write Burst

Symbol Files for Bus Decoding

Basic Command Bus
(CS, RAS, CAS, WE)

DDR3 Symbol File Example.tsf - Notepad

File Edit Format View Help

```
# DDR3 SDRAM Symbol Table
#
# TSF Format                Type          Display Radix
File Radix
# ==============  =======                 ============
==========
#+ Version 2.1.0  PATTERN                          BIN
                  BIN
#
#                           Command Signals Pattern
#                           S0# RAS# CAS# WE#
#
# Command                   Command
# Symbol Name               Pattern
#==============            ========
MODE_REG                    0000
REFRESH                     0001
PRECHARGE                   0010
ACTIVATE                    0011
WRITE                       0100
READ                        0101
NOP                         0111
DESELECT                    1XXX
```

JEDEC Command Truth Table
(CKE,CS, RAS, CAS, WE, MRS, BA0/1, Address)

JEDEC Std Cmd Truth Table.tsf - Notepad

File Edit Format View Help

```
# DDR3 SDRAM Command Truth Table - Symbol File

#
# TSF Format File
# Tektronix Nov 4, 2009
#     TSF Format      Type    Display Radix  File Radix

#  ===============  =======  =============  ==========

#+ Version 2.1.0    PATTERN       BIN                   BIN

#  ============================================================
#       MSB                                                    LSB
#       CKE#    CS#     RAS#    CAS#    WE#     BA0     BA1     BA3     A12/BC# A10/AP
MRS     1       0       0       0       0       X       X       X       X       X
REF     1       0       0       0       1       X       X       X       X       X
SRE     0       0       0       0       1       X       X       X       X       X
SRX     1       1       X       X       X       X       X       X       X       X
PRE     1       0       0       1       0       X       X       X       X       0
PREA    1       0       0       1       0       X       X       X       X       1
ACT     1       0       0       1       1       X       X       X       X       X
WR      1       0       1       0       0       X       X       X       X       0
WRS4    1       0       1       0       0       X       X       X       0       0
WRS8    1       0       1       0       0       X       X       X       1       0
WRA     1       0       1       0       0       X       X       X       X       1
WRAS4   1       0       1       0       0       X       X       X       0       1
WRAS8   1       0       1       0       0       X       X       X       1       1
RD      1       0       1       0       1       X       X       X       X       0
RDS4    1       0       1       0       1       X       X       X       0       0
RDS8    1       0       1       0       1       X       X       X       1       0
RDA     1       0       1       0       1       X       X       X       X       1
RDAS4   1       0       1       0       1       X       X       X       0       1
RDAS8   1       0       1       0       1       X       X       X       1       1
NOP     1       0       1       1       1       X       X       X       X       X
DES     1       1       X       X       X       X       X       X       X       X
PDE     0       0       1       1       1       X       X       X       X       X
PDX     1       0       1       1       1       X       X       X       X       X
ZQCL    1       0       1       1       0       X       X       X       X       1
ZQCS    1       0       1       1       0       X       X       X       X       0
```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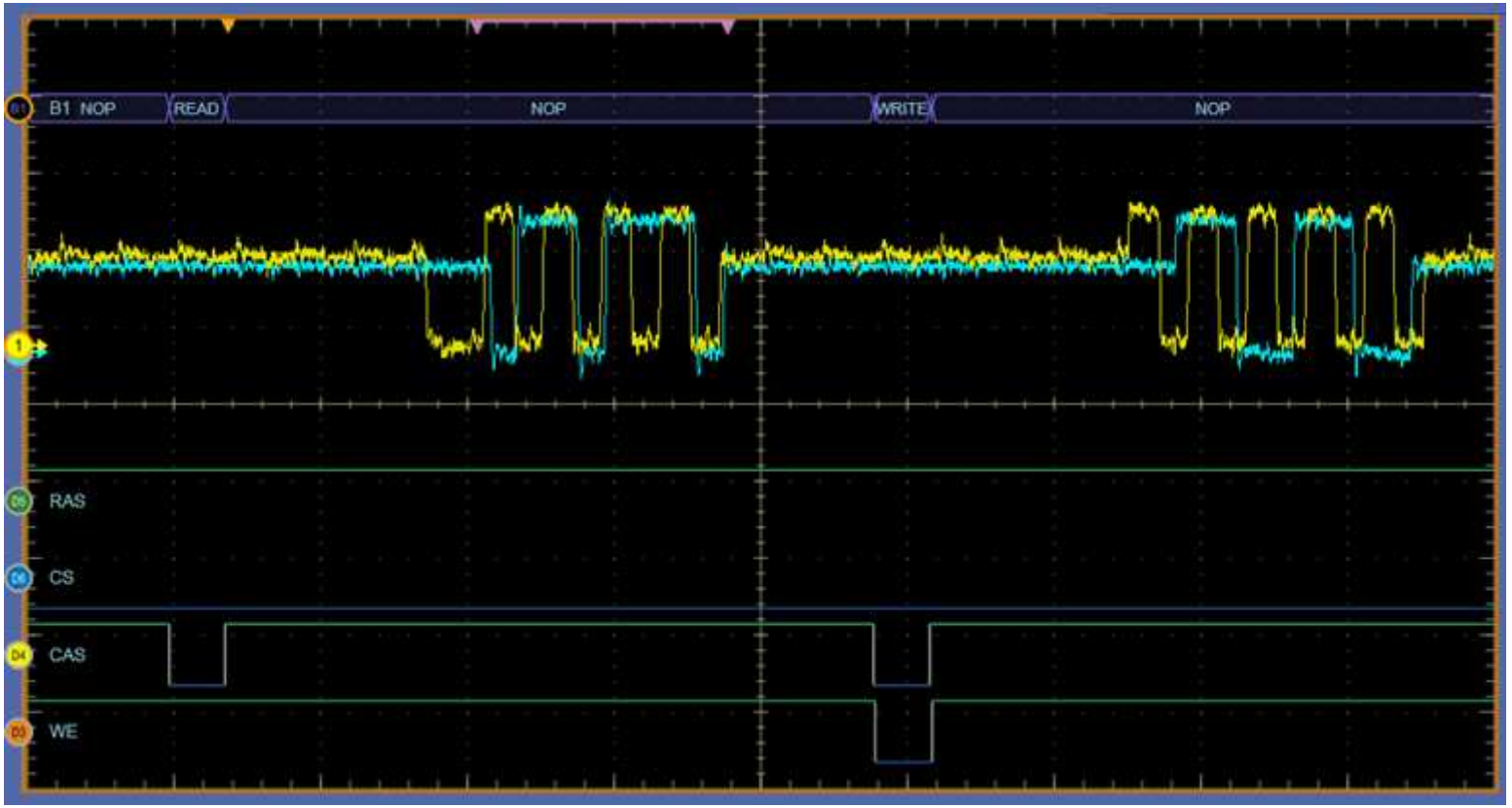
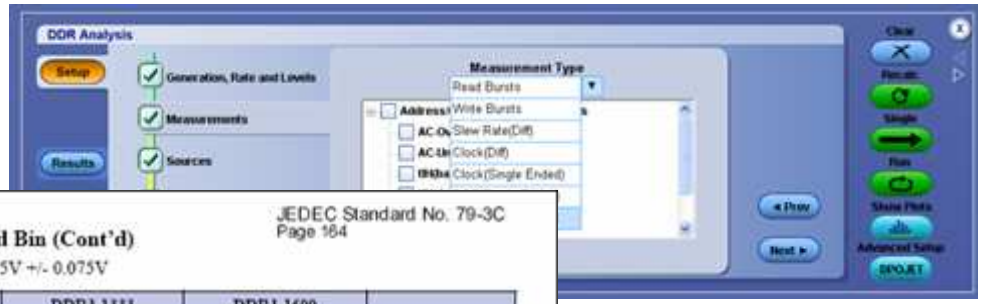
Burst Identification using Command Bus

- Using bus state, specific transactions can be isolated
  - For example, locate only Reads from a specific memory rank
  - Advanced Search & Mark is used for fine burst positioning



Measurement Setup

- JEDEC Standards specify measurements & methods



JEDEC Standard No. 79-3C
Page 164

Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Cumulative error across 8 cycles	tERR(8per)	- 241	241	- 217	217	- 193	193	- 169	169	ps	
Cumulative error across 9 cycles	tERR(9per)	- 249	249	- 224	224	- 200	200	- 175	175	ps	
Cumulative error across 10 cycles	tERR(10per)	- 257	257	- 231	231	- 205	205	- 180	180	ps	
Cumulative error across 11 cycles	tERR(11per)	- 263	263	- 237	237	- 210	210	- 184	184	ps	
Cumulative error across 12 cycles	tERR(12per)	- 269	269	- 242	242	- 215	215	- 188	188	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	$^{j}ERR(nper)min = (1 + 0.68ln(n)) * {}^{j}TJ(per)min$ $^{j}ERR(nper)max = (1 + 0.68ln(n)) * {}^{j}TJ(per)max$								ps	24
Data Timing											
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, CK#	tLZ(DQ)	- 800	400	- 600	300	- 500	250	- 450	225	ps	13, 14, f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	400	-	300	-	250	-	225	ps	13, 14, f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base)	75		25		30		10		ps	d, 17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base)	150									
DQ and DM Input pulse width for each input	tDIPW	600	-								
Data Strobe Timing											
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 1								
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 1								
DQS, DQS# differential output high time	tQSH	0.38	-								
DQS, DQS# differential output low time	tQSL	0.38	-								
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-								
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-								
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	- 400	400								

8.1 AC and DC Logic Input Levels for Single-Ended Signals

8.1.1 AC and DC Input Levels for Single-Ended Command and Address Signals

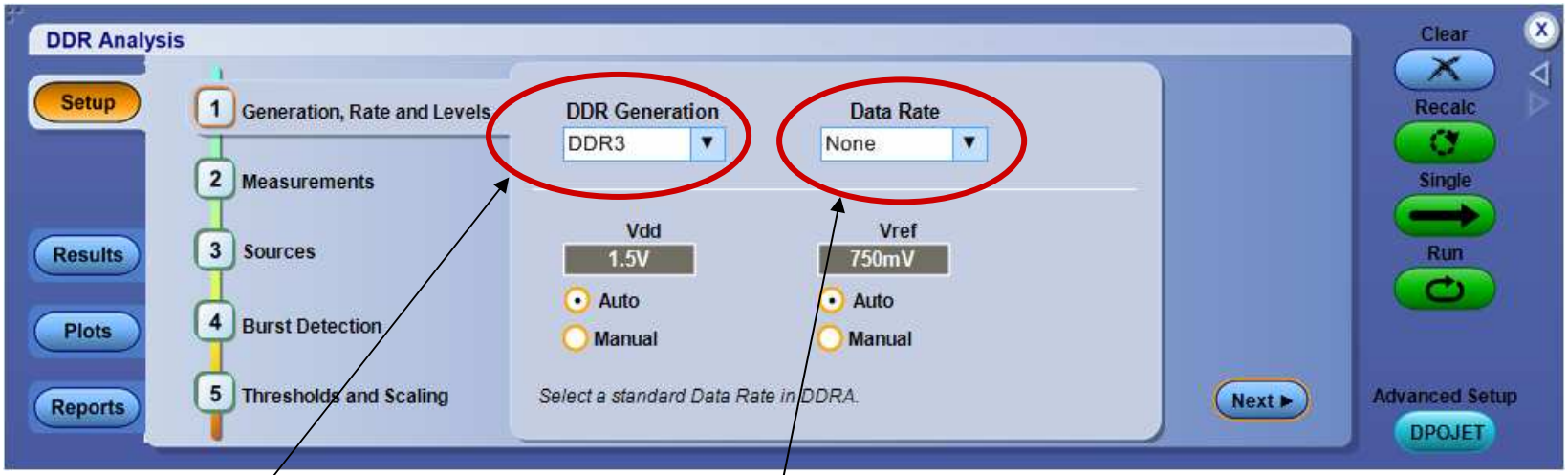
Table 24 — Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		Unit	Notes
		Min	Max		
VIH.CA(DC)	DC input logic high	Vref + 0.100	VDD	V	1
VIL.CA(DC)	DC input logic low	VSS	Vref - 0.100	V	1
VIH.CA(AC)	AC input logic high	Vref + 0.175	Note 2	V	1, 2
VIL.CA(AC)	AC input logic low	Note 2	Vref - 0.175	V	1, 2
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note 2	V	1, 2
VIL.CA(AC150)	AC input logic low	Note 2	Vref - 0.150	V	1, 2
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

Tektronix®

Automated Test Setup

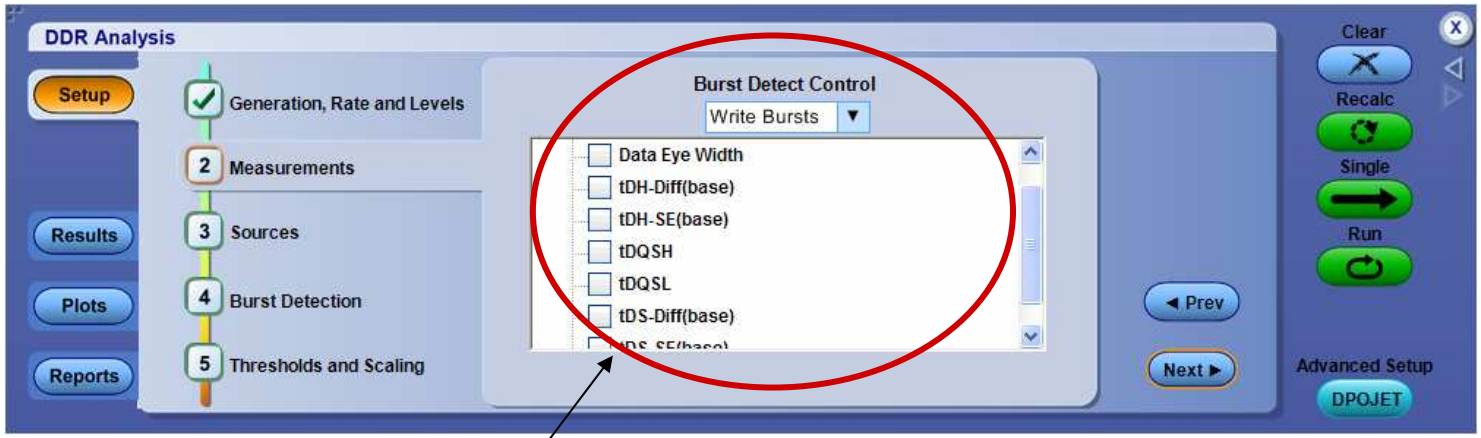
Step #1



Select DDR Generation

Select DDR Rate

Step #2



Choose measurements (Read / Write / Clock)

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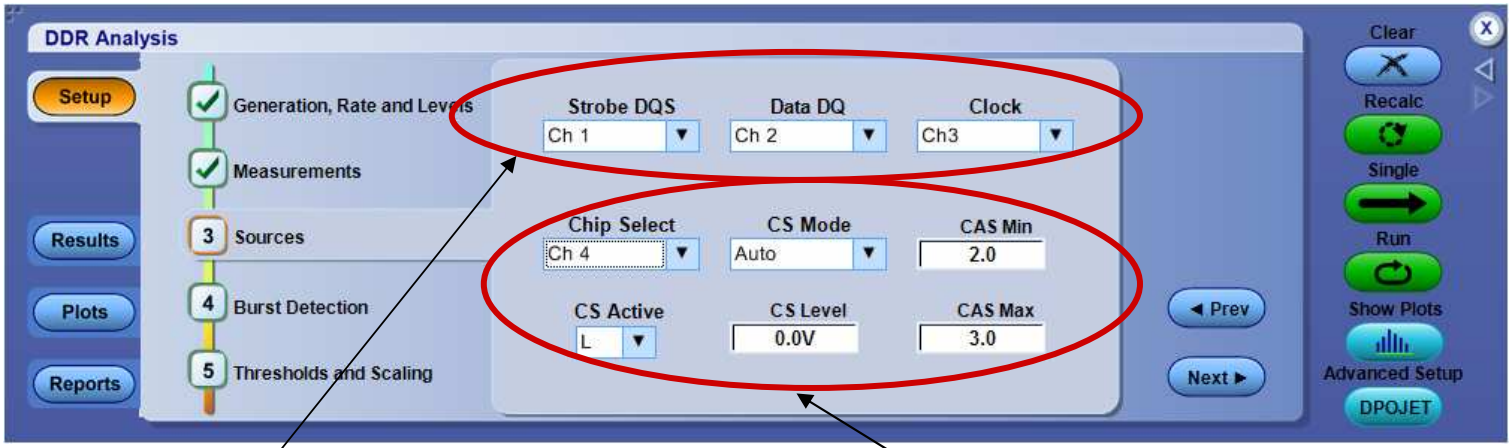
Source and Level Selection

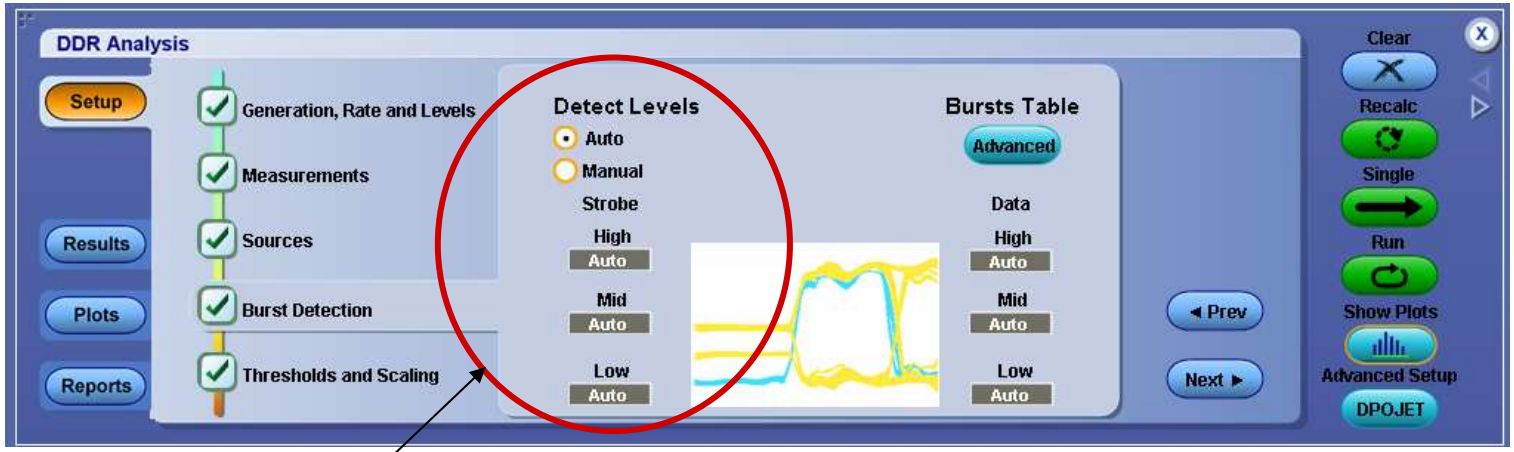
Step #3



Identify scope input channels for DQS, DQ, CLK

Optional **Chip Select** qualifier

Step #4

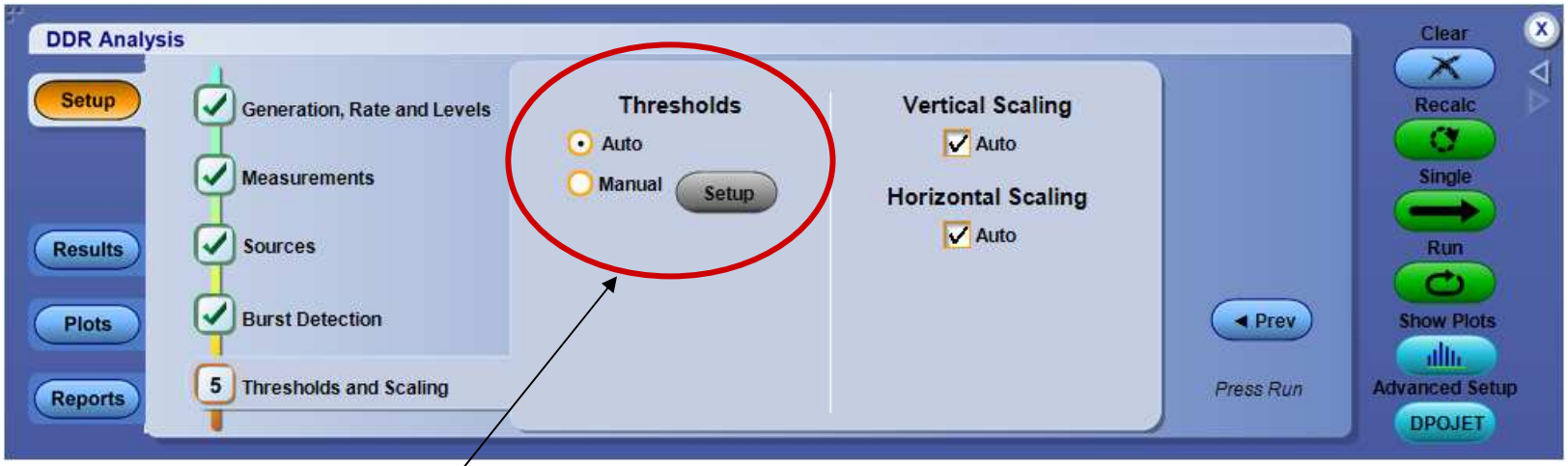


Let DDRA set Read/Write Burst Detect Levels automatically, or customize if needed

Tektronix®

Threshold and Auto Scaling

Step #5



Let DDRA set Measurement Ref Levels automatically (per JEDEC), or customize if needed

Comprehensive Measurement Support

Option DDRA supports a broad range of JEDEC-specified measurements for DDR, DDR2, DDR3, LPDDR, LPDDR2

- Example measurements list for DDR2 :

- tCK(avg)
- tCK(abs)
- tCH(avg)
- tCH(abs)
- tCL(avg)
- tCL(abs)
- tHP
- tJIT(duty)
- tJIT(per)
- tJIT(cc)
- tERR(02)
- tERR(03)
- tERR(04)
- tERR(05)
- tERR(6 - 10 per)
- tERR(11 - 50 per)
- tDQSH
- tDS - diff (base)
- tDS - SE (base)
- tDS -diff - DERATED
- tDS -SE - DERATED
- tDH - diff (base)
- tDH - SE (base)
- tDH -diff - DERATED
- tDH -SE - DERATED
- tDIPW
- tAC - diff
- tDQSCK -diff
- tDQSCK - SE
- tDQSQ - diff
- tDQSQ - SE
- tQH
- tDQSS
- tDSS
- tDSH
- tIPW
- tIS (base)
- tIH (base)
- tIS - DERATED
- tIH - DERATED
- Vid - diff (AC)
- Vix (AC) - DQS
- Vix (AC) - CLK
- Vox (AC) - DQS
- Vox (AC) - CLK
- Input Slew-Rise (DQS),
- Input Slew-Fall (DQS),
- Input Slew-Rise (CLK),
- Input Slew-Fall (CLK),
- AC - Overshoot Amplitude - diff
- AC -Undershoot Amplitude - diff
- AC - Overshoot Amplitude - SE
- AC - Undershoot Amplitude - SE
- Data Eye Width

Measurement De-rating

- JEDEC stipulates de-rating of DDR2 and DDR3 pass / fail limits for Setup & Hold measurements based on signal slew rate*
- Option DDRA automatically calculates slew rates and applies the appropriate de-rating values to the measurement limits.

  - tDS - diff (base)
  - tDS -diff - DERATED
  - tDS - SE (base)
  - tDS -SE - DERATED
  - tDH - diff (base)
  - tDH -diff - DERATED
  - tDH - SE (base)
  - tDH -SE - DERATED
  - tIS (base)
  - tIS - DERATED
  - tIH (base)
  - tIH - DERATED

JEDEC Standard No. 79-3C
Page 176

13 Electrical Characteristics and AC Timing (Cont'd)
13.3 Address / Command Setup, Hold and Derating (Cont'd)

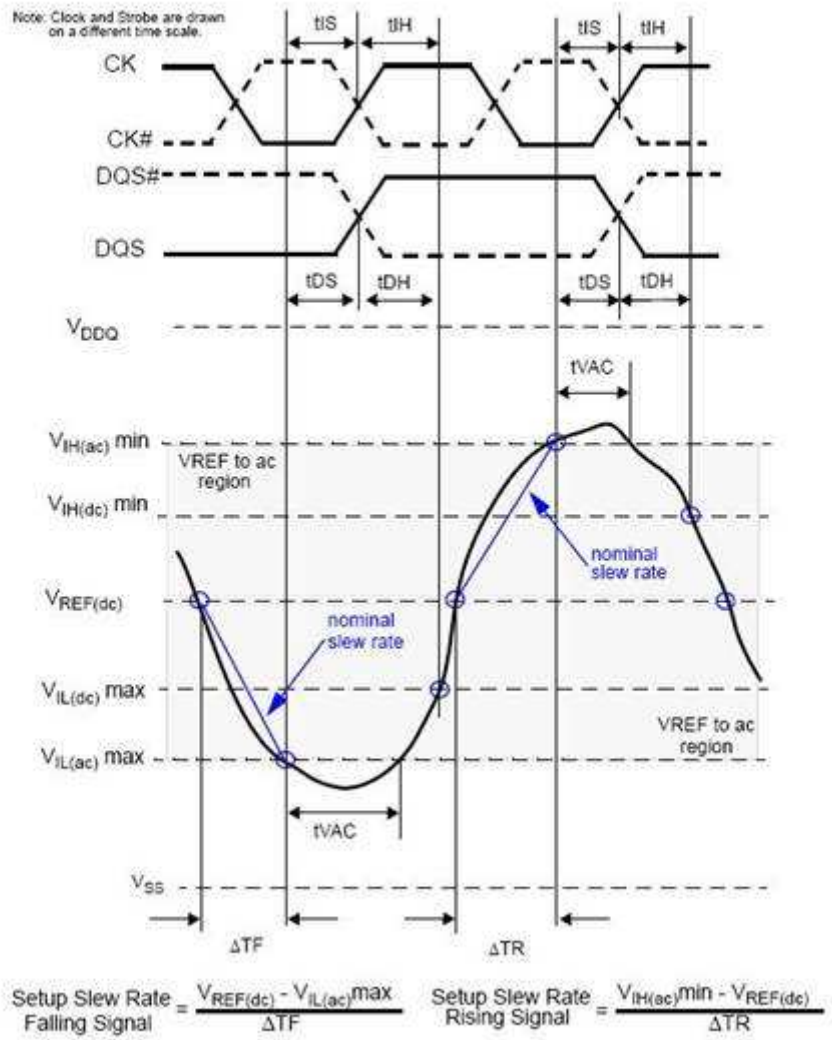


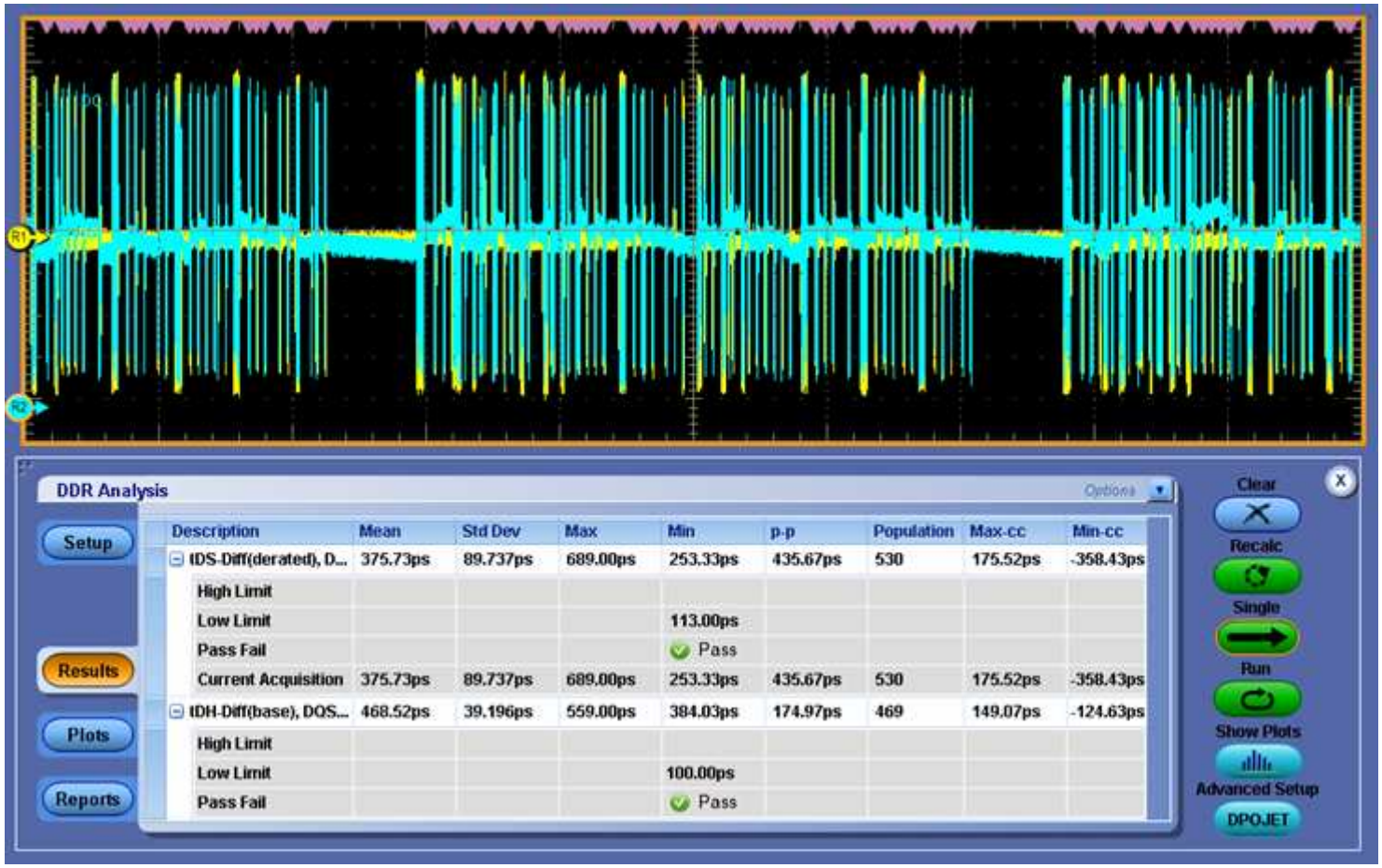
Figure 110 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

* JESD79-2E, JESD79-3C specifications

Tektronix®

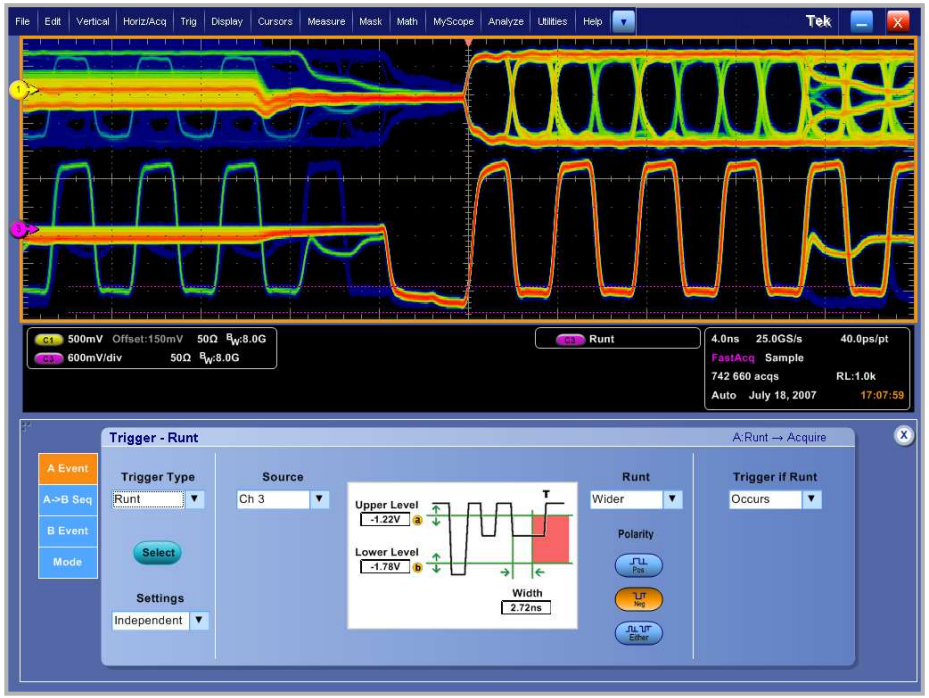
Results and Statistical Validity

- To have confidence in your test results, you need 100's, 1000's or even more observations of each measurement
- As a practical matter, measurement throughput is essential

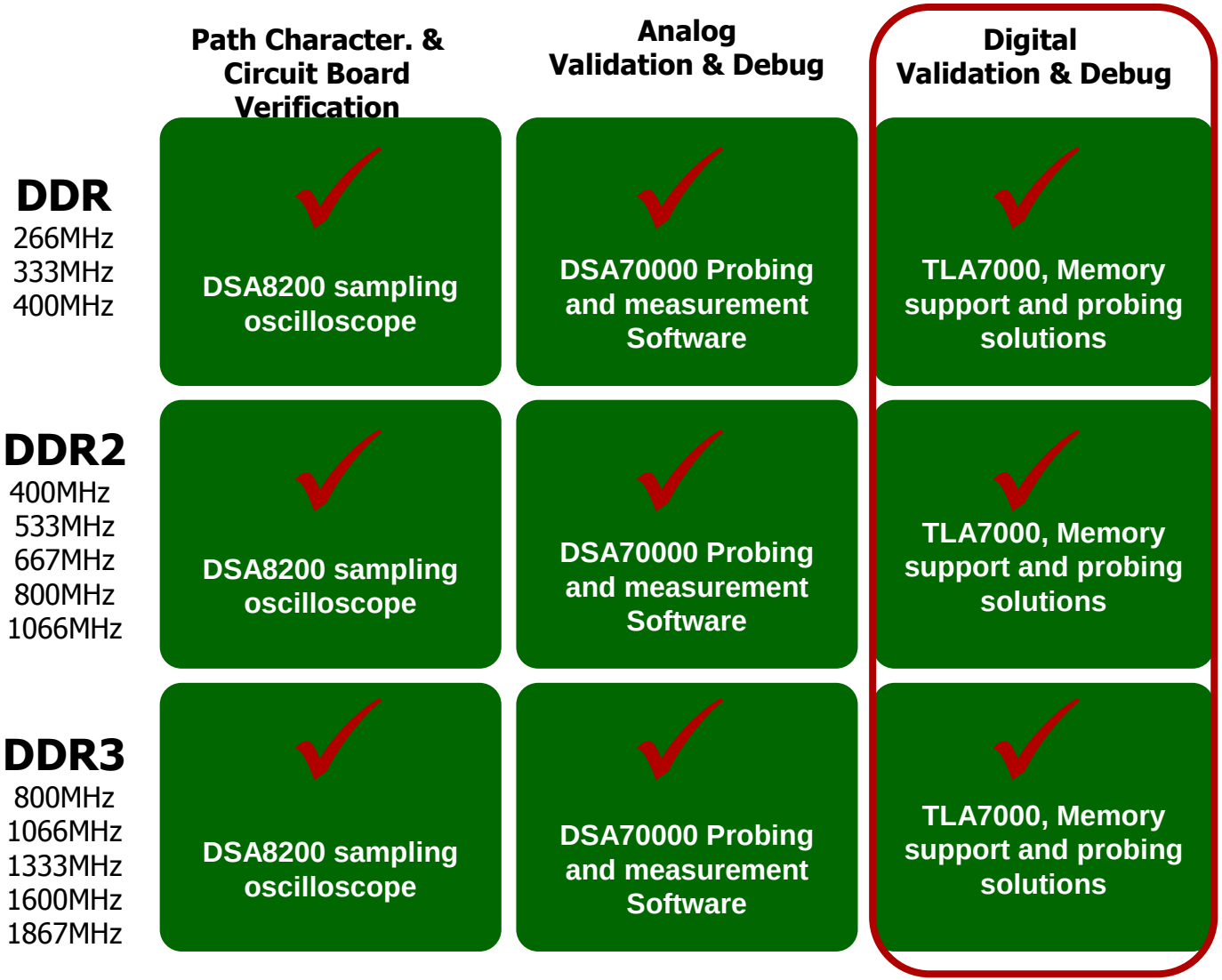


Beyond DDRA: Other Tektronix Scope DDR Debug Tools

- Fastest way to solve sophisticated Memory signaling issues
  - Superior real-time insight into the complex DDR2/DDR3 signaling
    - DPX (FastAcq) and Pinpoint Triggering gives you “the power to see what others can’t”
  - FastAcq shows any disparities on strobe/data – like infrequent glitch on Write data. You can choose to display consecutive eyes on the data only (w/o showing the strobe information)

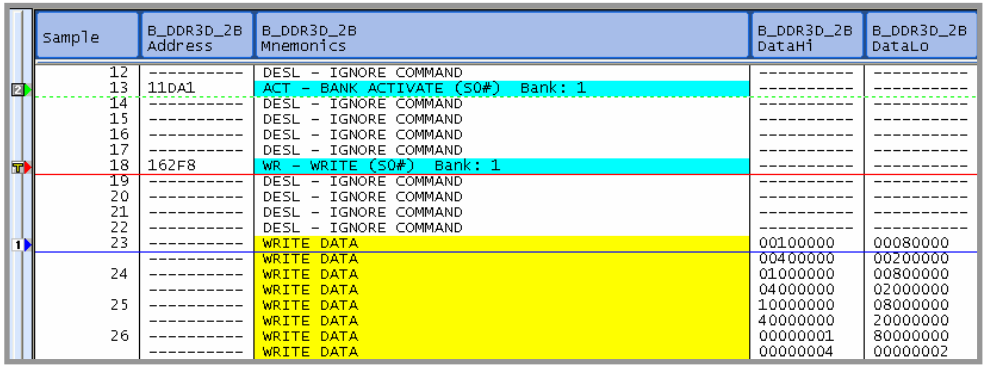


Tektronix DDR Test Solutions

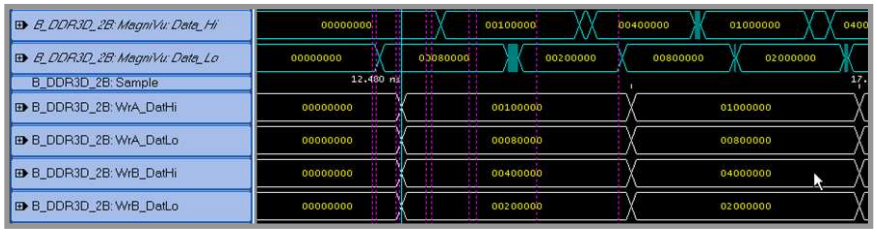


Digital Design and Validation

- Additional Visibility Needed
  - Data flow in and out of memory
  - Timing across many channels - all strobes and clock.
  - Data flow to/from a processor and memory
- Identify bus/system level issues
  - Protocols Sequences & Timing
  - Memory system power up initialization protocols & timing
  - DRAM Mode register settings
  - Refresh operations
  - Time Correlation with other system buses
  - Time Correlation with Oscilloscope waveforms



Sample	B_DDR3D_2B Address	B_DDR3D_2B Mnemonics	B_DDR3D_2B DataHi	B_DDR3D_2B DataLo
12	----------	DESL - IGNORE COMMAND	----------	----------
13	11DA1	ACT - BANK ACTIVATE (S0#) Bank: 1	----------	----------
14	----------	DESL - IGNORE COMMAND	----------	----------
15	----------	DESL - IGNORE COMMAND	----------	----------
16	----------	DESL - IGNORE COMMAND	----------	----------
17	----------	DESL - IGNORE COMMAND	----------	----------
18	162F8	WR - WRITE (S0#) Bank: 1	----------	----------
19	----------	DESL - IGNORE COMMAND	----------	----------
20	----------	DESL - IGNORE COMMAND	----------	----------
21	----------	DESL - IGNORE COMMAND	----------	----------
22	----------	DESL - IGNORE COMMAND	----------	----------
23	----------	WRITE DATA	00100000	00080000
	----------	WRITE DATA	00400000	00200000
24	----------	WRITE DATA	01000000	00800000
	----------	WRITE DATA	04000000	02000000
25	----------	WRITE DATA	10000000	08000000
	----------	WRITE DATA	40000000	20000000
26	----------	WRITE DATA	00000001	80000000
	----------	WRITE DATA	00000004	00000002



Tektronix Innovation Forum

DDR2/3 Data Access - Probing

Performance

- Sufficient performance for all DDR signal speeds
- Preservation of frequency components
- Preservation of timing
- Minimizes effects of reflections
- Lowest probe loading in industry <0.5pF

Connectivity

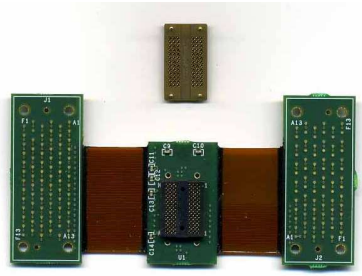
Wide Range of probes for all DDR2/3 speeds – up to DDR3-1867

- NEXVu instrument DIMMs – only for Tektronix Logic Analyzers
  - Enhanced JEDEC layout DIMMs to include logic analyzer probing very close to the SDRAM
- DIMM Interposers
- BGA Memory Component Interposers that use Innovative Socket Design
- Direct probing to circuit board

DDR3 DIMM Interposer

DDR3 NEXVu Instrumented DIMM

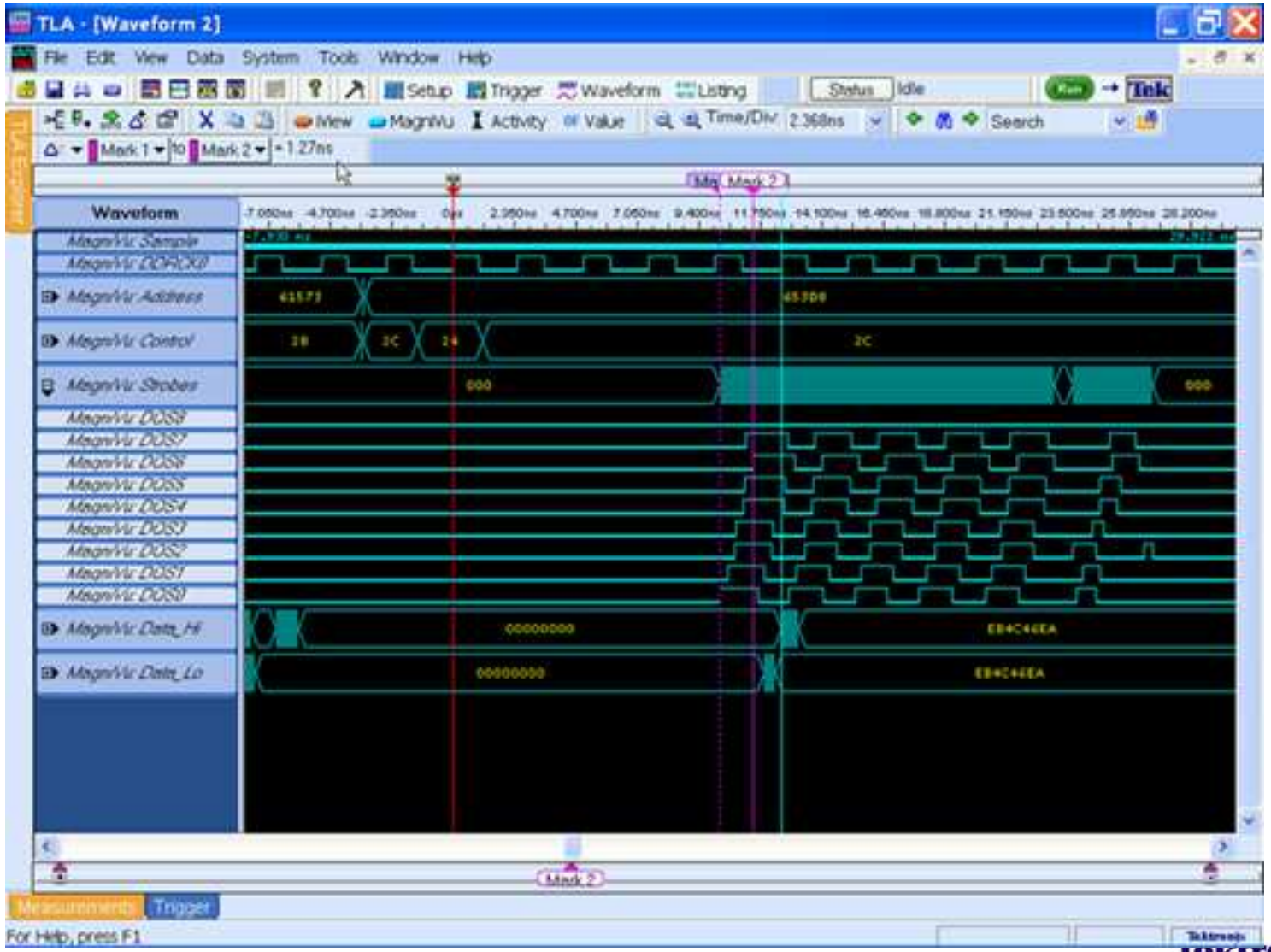
Direct Probing



BGA Memory Component interposer

Write Data Strobes Skew Analysis

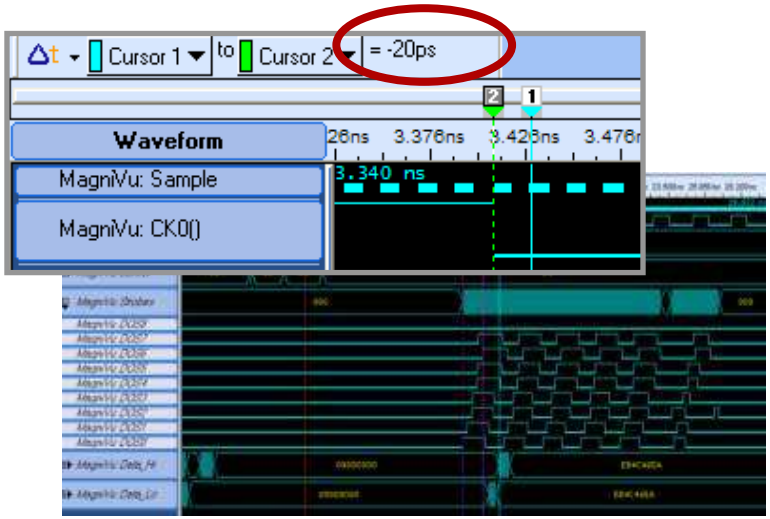
Logic Analyzer MagniVu 20 ps (50 GS/s) timing resolution



Tektronix Innovation Forum

Data Acquisition

- Acquisition
  - 1.4 Gb/s data, 1.4GHz clock, 64Mb, Full Channel
  - 2.8 Gb/s data, 1.4GHz clock, 128Mb, Half Channel
  - Simultaneous timing & state acquisition
    - MagniVu 20ps (50GHz) timing resolution @ 128K record length
- Triggering
  - 16 state IF-THEN-ELSE trigger state machine
  - 24 word recognizers
- Module
  - 136 channel module
  - Merge with other modules
  - Uses P68xx and P69xx probes
  - Uses TLA7016 and TLA7012 mainframes



The only Logic Analyzer module fast enough to address all DDR3 speeds

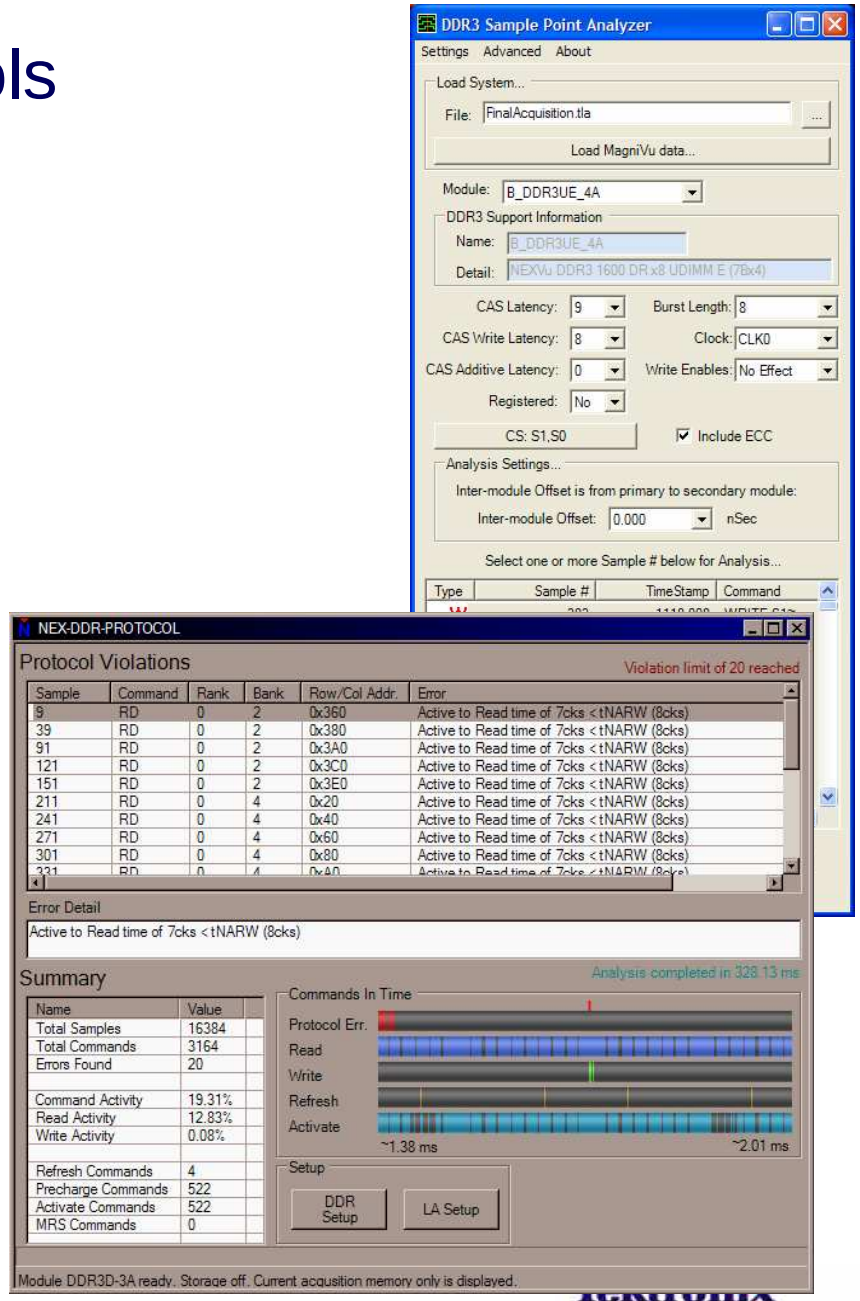
DDR3 Enhanced Analysis Tools

DDR3 Sample Point Analysis Tool

- Helps to easily and quickly setup the Logic Analyzer for Acquiring the DDR data
- Optimally Adjusts the Threshold on the DQS and DQ Channels
- Determines the best sample point for each data group

DDR3 Protocol Violation Tool

- Quickly Identifies Protocol Violations
- Gives Global view of the DDR Bus Activity across the Entire LA Memory
- Navigates the user to the protocol errors in the listing or waveform window



DDR3 Sample Point Finder (SPF) Software

Select module that is connected to the interposer

Auto runs the analyzer to acquire the desired number of read and write transactions

Identify Support Package

Apply single threshold as starting point

Cancel test at any time

Setup for min, max threshold along with increments

Number of commands analyzed

Select the Read or Write data

Personality file for different DDR3 Raw cards, pinouts or unique system requirements

See results of multi-thresh old run

Single button to apply all sample points and set all thresholds

Blue area is data transitions

White area is stable data

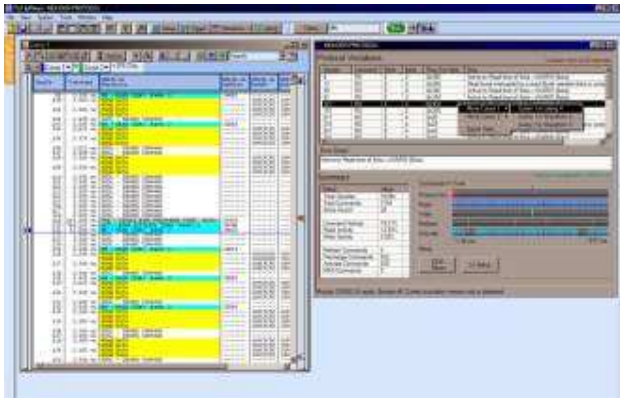
Sample Point, Red is suggested and Green is current

Data Analysis

TLA7000 Series & Nexus & FuturePlus Memory support:

Extensive Analysis capability enabled by exceptional timing resolution (MagniVu)

- SDRAM initialization, commands, sequence and timing analysis
- Read and Write Data analysis
- Complete system visibility, directly transfer signals to an oscilloscope *without the need of double probing*



Nexus & FuturePlus Memory support

- Protocol analysis features automates the analysis of DDR2 and DDR3 to quickly and easily identify protocol violations
- Provision of easy to read DDR symbols
- Decode of DDR/2/3 SDRAM command signals into mnemonics.

Tektronix + Nexus & FuturePlus = the world's leading DDR3 test solution

Verify and debug command sequence, timing, data, and more

Digital Validation & Debug

Tektronix
Embedded Systems Tools Partner

Data Access - Probing

- Requires reliable physical connectivity with minimal loading
  - Interposers
  - instrument DIMMs
  - Direct probing to circuit board
- Requires maximum signal integrity

NEW DDR probing solution

Data Acquisition

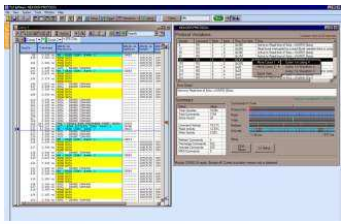
- The only Logic Analyzer fast enough to capture all DDR3 speeds
- Timing resolution high enough for thorough debugging
- Trigger state machine flexible enough to trigger only on relevant events
- Channel count scalable and high enough to capture all required signals
- Scalable and time correlated system for cross bus analysis

NEW DDR3 Logic Analyzer module

Data Analysis

- Verify and debug memory system operation
  - Data valid windows
  - Read/Write data operation
  - DDR commands and mode register initialization
- Quickly and easily identify protocol violations

New Memory support packages



Tektronix Innovation Forum

Fast & Accurate instrument solutions

DDR, DDR2 & DDR3 SDRAM Solutions

Signal Path Characterization and Circuit Board Verification

D*SA Sampling Oscilloscopes*

Over 70GHz of sampling bandwidth & the lowest Jitter floor

Emulate the channel effect on jitter & noise using channels' TDR/TDT or Touchstone® (S-parameter) description

TDR impedance measurements & S-parameter characterization of the PCB traces

Analog & Electrical Debug

DPO/DSA real time scopes & software

Pinpoint triggering on DDR reads & writes

Automatic detection of voltage levels & data rates

Automated clock jitter measurements based on JEDEC specification

SDRAM eye diagram measurements for read or write cycles

Digital Validation & Debug

TLA Logic Analyzers with Nexus & FuturePlus Technology memory supports

Only solution available to capture and analyze all DDR3 speeds

Up to 20 ps timing resolution on all channels, all the time

Selective clocking only stores useful data

Complete system visibility with digital/analog correlation

SDRAM Probing Solutions

Active differential oscilloscope probes

Slot interposers

Midbus probes

Instrumented DIMMs

Oscilloscopes can either use direct probing or probing via the logic analyzer with logic analyzer probes

The world's leading DDR3 test solution

DDR SDRAM Memory Support

	DDR	DDR2	DDR3
Logic Analyzer Mainframe	TLA7102 Portable or TLA7016 Benchtop		
Logic Analyzer Module**	TLA7AA4	TLA7BB4	
Test Fixture/Support Package	Nexus Technology NEXVu & FuturePlus System DDR Support		
Probing	Tektronix midbus probes or Nexus & FuturePlus slot interposer and instrumented DIMMs		P6960HCD (>1500MT/s) or NEX-PRB1XL (< 1500MT/s)

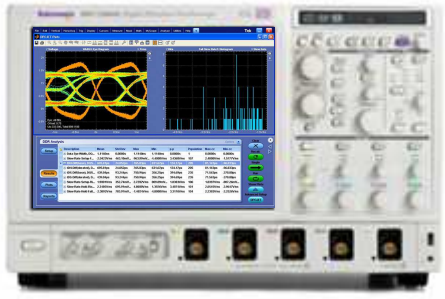
DDR SDRAM Memory Support

	LPDDR LPDDR2 DDR	DDR2	GDDR3 DDR3*
Oscilloscope	DPO/DSA70404B or MSO70404 or higher	DPO/DSA70604B or MSO70604 or higher	DPO/DSA70804B or MSO70804 or higher
Probing	P7300 or P7500 Series Differential Probes		
Analysis Software	DDR Analysis (DDRA), Advanced Search & Mark (ASM), DPOJET Jitter/Eye Analysis (DJA)		
Command Bus Triggering/Decode iCapture (Analog Mux)	MSO70404 or higher	MSO70604 or higher	MSO70804 or higher

*Additional speeds supported with custom clocking selection in analysis software

Tektronix®

Should I use a Logic Analyzer, MSO, or Digital Oscilloscope?

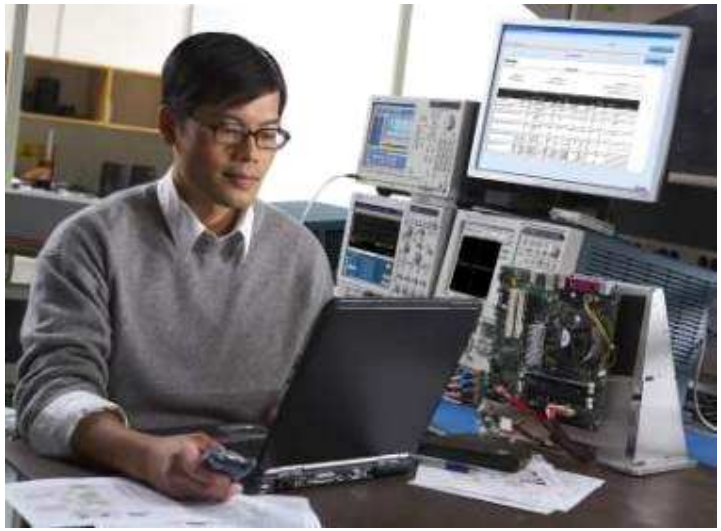


	TLA7000 Logic Analyzer	MSO70000 MSO	DPO/DSA70000B
	Full digital system visibility	Debugging high-speed events in a mixed signal environment	Debug & measurements to 20 GHz
Applications	Processor bus validation Full System (CPU, mem., I/O) visibility	High-speed timing analysis and Debug High Speed FPGA or Embedded Memory interfaces	High speed transceiver analysis/characterization, Physical layer analysis
	Memory bus protocol verification DDR2/DDR3 Debug	Memory bus analog verification DDR2/DDR3 Debug	Memory bus analog verification
	System validation	HSS Phy layer, characterization & debug Low-speed serial/parallel (command) bus correlated to high-speed signals (data/strobe/clock)	High speed validation and margin analysis
Capabilities	State and Timing analysis (sync & async sampling), Correlated Analog + Digital with iView	Timing Analysis, Correlated Analog + Digital validation	Timing Analysis, Analog characterization
	Powerful, complex, 16-stage trigger equations, Memory bus disassembly	Hardware-based bus triggering, Bus/State qualified signal integrity	Single stage trigger for finding analog faults and logic patterns
	Hundreds of channels	4 analog + 16 digital channels	4 analog

Tektronix®

Summary – World's Best DDR Test Solution

- **COMPLETE**
  - Provides total validation and characterization and full measurement support
  - DDR1/2/3, LP-DDR1/2 and GDDR3 support in one tool
  - Partnership with Nexus & FuturePlus provides most complete protocol and probing support
- **Performance**
  - Based upon highest performing oscilloscopes, Logic Analyzers and software analysis tools
  - TriMode probing enables three
  - Read/Write burst identification on all bursts
  - Automated setup with JEDEC pass/fail limits



DDRA Validation Software

DPO/DSA70000B Series Oscilloscopes

P7500 Series TriMode Probes

TLA7BBx Logic analyzer module for DDR

Comprehensive Test from Analog to Digital Validation for All DDR Versions

Resources

- What equipment do I need to test DDR?
- *Tektronix Knowledge Center:* *www.tektronix.com/memory*
- How can I learn more about DDR testing?
- *DDR Application Note:* *www.tektronix.com/ddr*
- *Memory Implementers Forum:* *www.memforum.org*
- *JEDEC:* *www.jedec.org*