D-2

DisplayPort
eDP1.4の機能解説と製品への応用

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✓	社名	株式会社ジップス
✓	本社所在地	東京都文京区後楽1－1－5
✓	創立	1990年10月
✓	代表	水野勝弘
✓	資本金	2500万円
✓	売上	5.2億円（2012）
✓	従業員	50名
✓	主要業務	System委託開発・SI事業・映像デバイス技術サポート
✓	主な取引先	CANON, EIZO, Mitsubishi, Panasonic AVC, SEIKO EPSON, SHARP, SONY, NEC Personal Computer, STMicroelectronics, Tokyo electron device
✓	VESA Member	2009年

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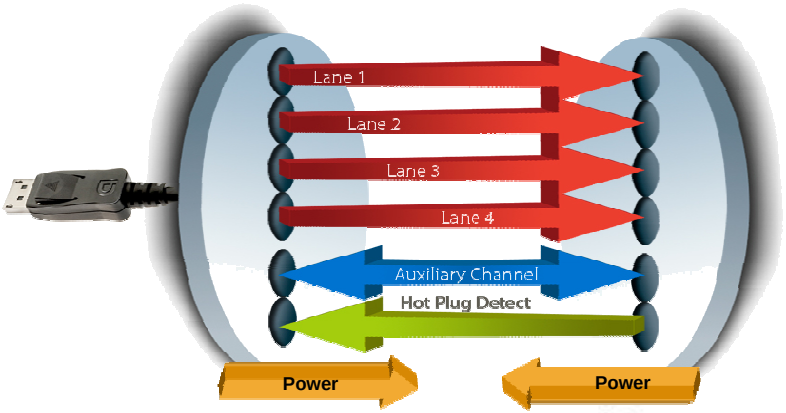
Agenda

- Displayport 1.2 概要
- Displayport Famiry 概要
- Thunderboltってなに？
- eDP発生要因
- eDPの特徴的System Diagram
- DP1.2とeDPの相違
- eDP1.3 と eDP1.4の相違
- PSR (Panel Self refresh)の技術解説
- eDPの製品への応用 （STMs ICの提案）
- VESA Update

Displayport 1.2　概要

- VESA（Video Electronics Standard Association）のOpen standard規格
  Royalty free　装置間・内部接続
- 1, 2, or 4 high-speed differential pairs (Main Link) from Stream Source to Stream Sink
  - 固定 link rates; 1.62-/2.7-/5.4-Gbps
  - Clock embedded with ANSI8B10B coding; no separate clock forwarding
  - AC-coupled to allow for different termination voltages between TX and RX
  - Single/Multiple video stream transport,
  - Audio transport and content protection (HDCP1.3)
- Sideband channel consisting of AUX CH and HPD
  - AUX CH = Half-duplex bi-directional, initiated by Stream Source, AC-coupled
  - HPD = Used as IRQ pulse, driven by Stream Sink

	Raw Bit Rate (incl. coding overhead)	Application Bandwidth /Throughput
1 x lane	1.62-/2.7-/5.4-Gbps	162-/270-/540-Mbytes/s
2 x lanes	3.24-/5.4-/10.8-Gbps	324-/540-/1080-Mbytes/s
4 x lanes	6.48-/10.8-/21.6-Gbps	648-/1080-/2160-Mbytes/s
AUX CH	1Mbps / 675Mbps (optional)	~ 16 bytes per 0.5ms * / ~ 64 bytes per 1.3 us **



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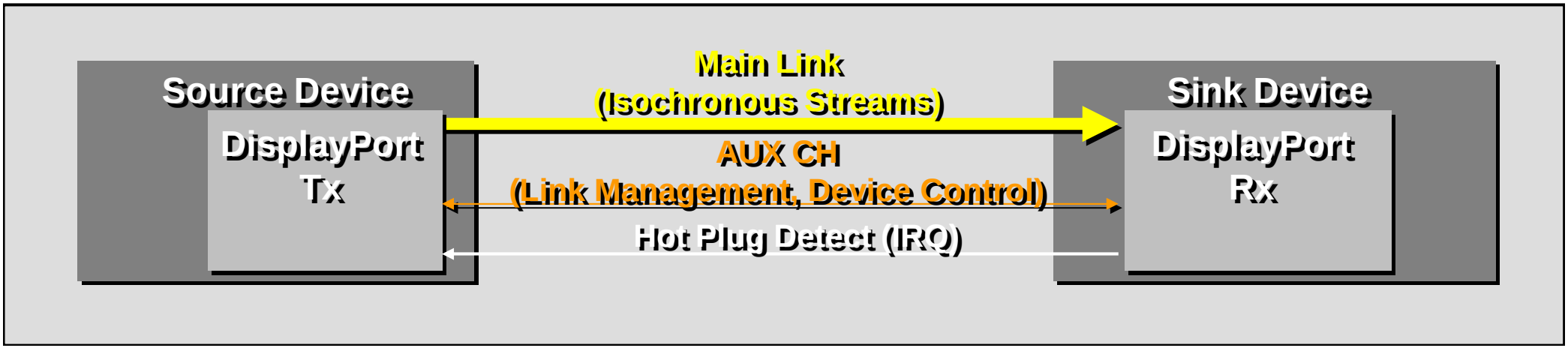
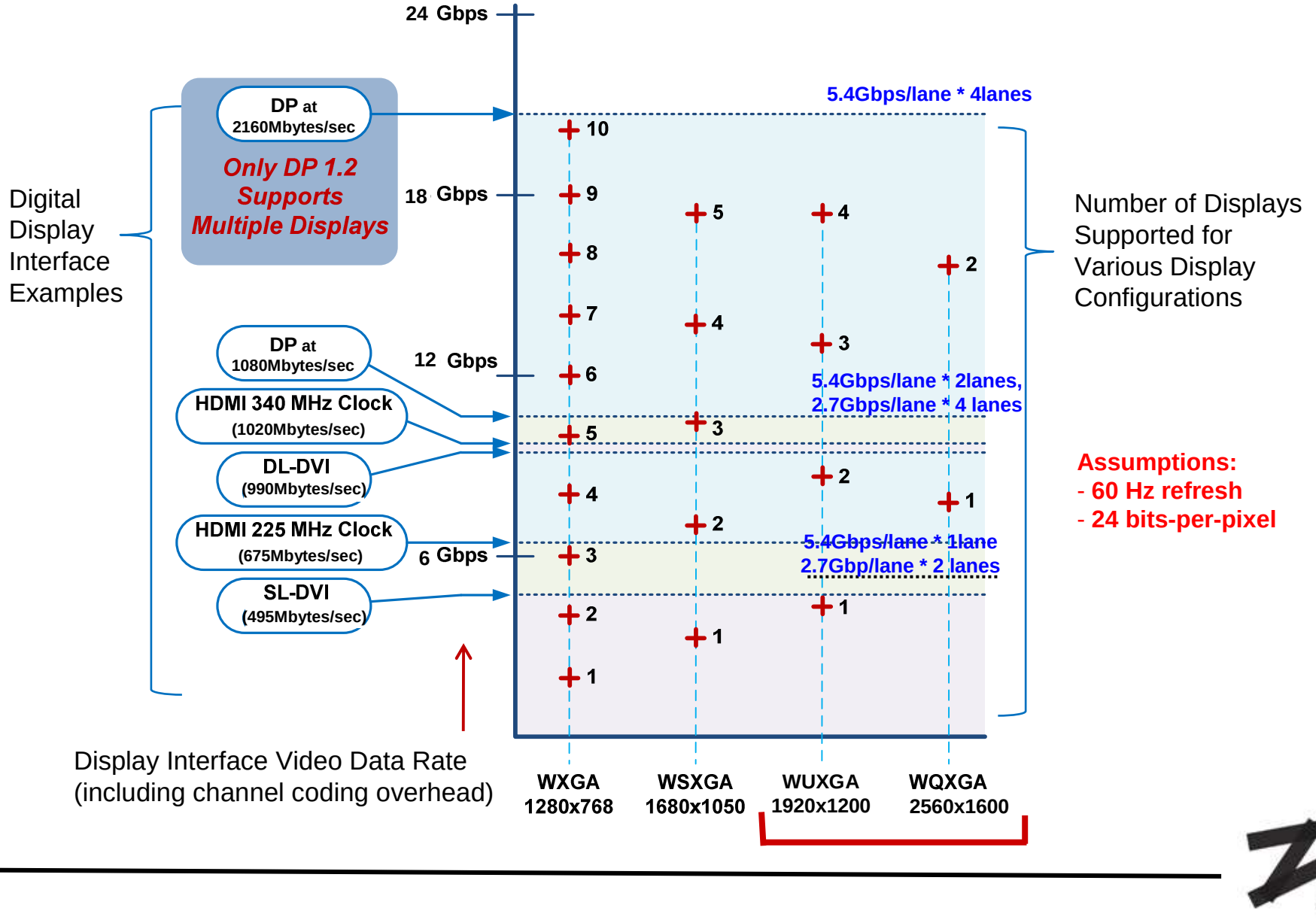
Displayport 1.2 概要

- **Main Link**
  - **High-bandwidth, low-latency, unidirectional, differential signaling, Isochronous stream transport**
- **AUX CH (Auxiliary Channel)**
  - **Consistent bandwidth, low-latency, bi-directional, differential signaling**
  - **Main Link management, Device control (EDID, MCCS),**
  - **Supports *Active Source Detection* by Sink Device**
- **HPD (Hot Plug Detect)**
  - **Supports *Active Sink Detection* by Source Device,**
  - **Interrupt Request, LVTTL(3.3V) signaling**



Data rate .vs. Num of Display（DP1.2概要）



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DP Family DP 1.2 概要

	DP1.2	eDP	iDP	*MYDP*
Standard	VESA Ver. 1.2 Jan 2010	VESA Ver. 1.4: Feb 2013	VESA Ver.1.0 Apr 2010	*VESA* *Ver. 1.0 May 21 2012*
Channel coding	*ANSI8B10B*			
Bandwidth (per lane)	HBR2 5.4Gbps HBR 2.7Gbps RBR 1.62Gbps	Rate_1 1.62Gbps (RBR) Rate_2 2.16Gbps Rate_3 2.43Gpps Rate_4 2.7Gbps (HBR) Rate_5 3.24Gbps Rate_6 4.23Gbps Rate_7 5.4Gbps(HBR2)	Nominal 3.24Gbps/lane Other link rates: Implementation Choice (e.g., 3.78Gbps/lane)	*HBR2 5.4Gbps* *HBR 2.7Gbps* *RBR 1.62Gbps*
Lane Count	1, 2, or 4 lanes	1. 2, or 4 lanes	1 ~ 16 lanes per bank	*1 lane*
Secondary Data Packet	YES	Optional	NO	*Yes*
AUX CH	YES (incl.vUSB2.0 transport over AUX)	Optional (used for backlight, color control, etc.)	NO	*Yes; AUX transaction and HPD supported over a single wire* *DP_PWR : 5V±10% 0.5A* *Config1/2*
HPD	YES	Optional	YES (Used for Link Training Pattern transmission trigger)	
Transported data	Multiple A/V streams, Control data	Video stream, Control data	Video stream	*AV stream(s),* *Control Data*
Stream Clocking Mode	Synchronous or Asynchronous to Link Symbol Clock		Synchronous mode only; Nvid fixed to 48 decimal	*Synchronous or Asynchronous*
Target Application	Box2Box connection to TV/Monitor with Multi-streaming capability	Internal to Notebook/Netbook /Tablet/All-in-one PC	Internal to TV/monitor chassis	*Mobile device to an external display connectivity*

Thunderboltって？（DP1.2概要）

Intel社開発のInterface Technology for Data & Video/Audio on on one connector Adopted by Apple on miniDP Connector

- High speed dual-ch.10 Gbps bi-directional communication
- Compatible with existing DisplayPort devices
- Enables up to 7 daisy-chained devices
- Provides up to 10W power for bus-powered devices
- Targeting Notebook market, single connector for data and display

Impact on DisplayPort ?

- Accelerated adoption in Notebooks as the de-facto interface
- More reason for CE makers to embrace DP

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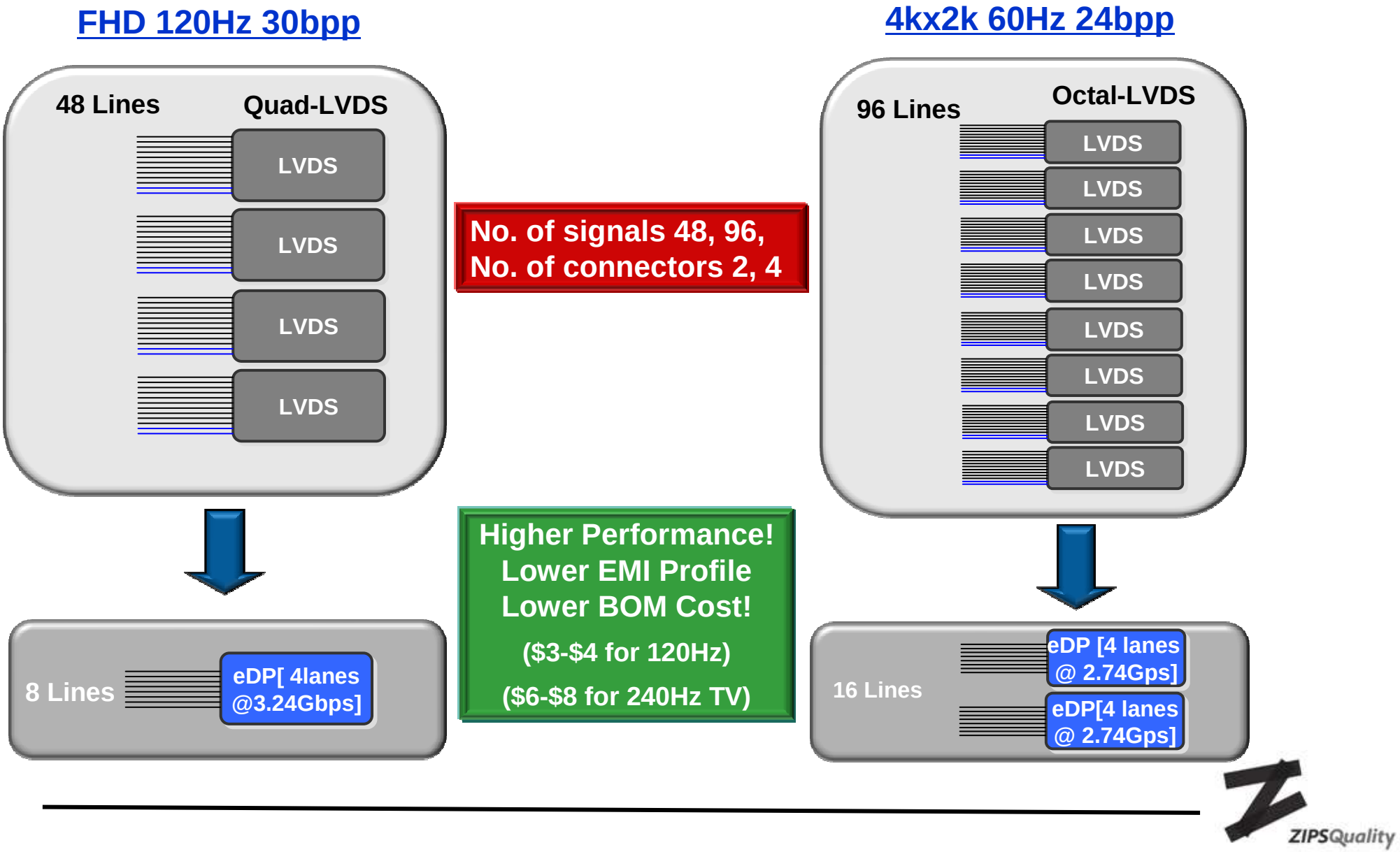
eDP 発生要因　高精細･高速伝送



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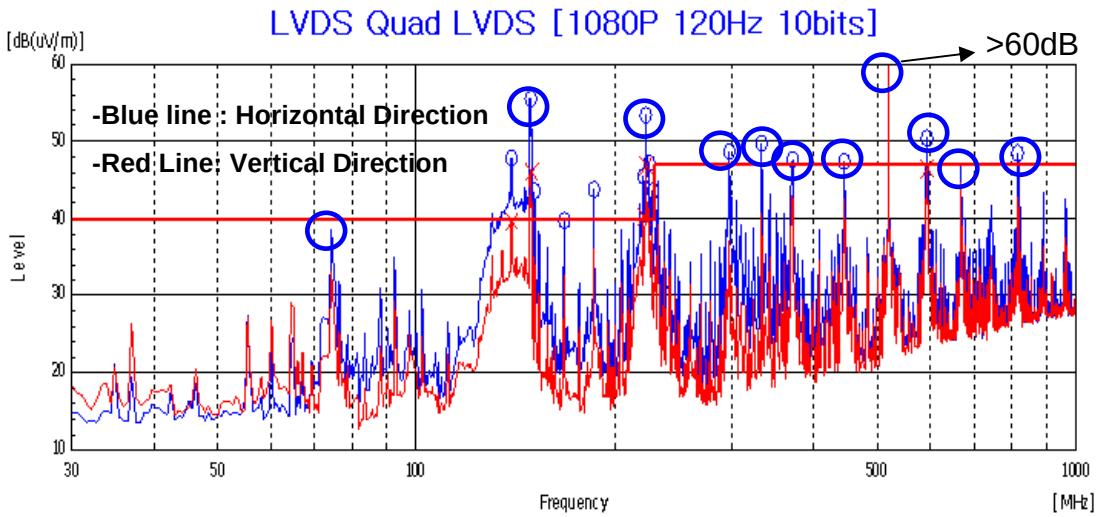
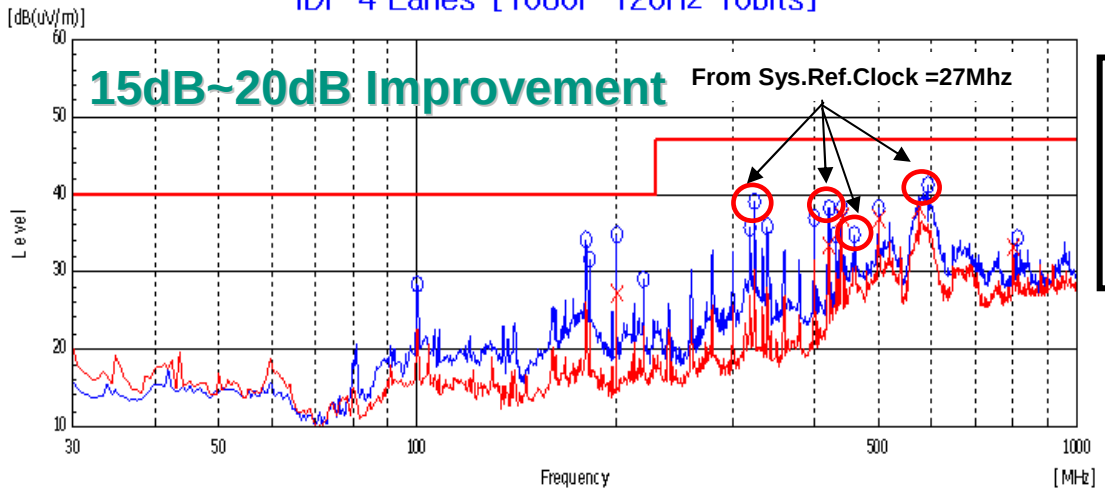
EMI 特性　eDP/iDPとQuadLVDSの比較





-1.0 meter FFC

-STM TX and RX Board

-5 Volts AC Adaptor [1)]

-Video Pattern: Blue/Grey Bar

1) 5-volt switching regulator
(12V →5V) disabled from the boards

EMI Peaks

-LVDS: from LVDS CLK=74.28MHz [2)]

-iDP: from System Ref.CLK=27MHz [3)]

2) Blue Circles. EMI peaks from System Ref. Clock (27MHz) smaller than by LVDS EMI peaks

3) Red Circles

STMicroelectronics　Lab.　測定

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GPU Displayport(eDP)出力

- source (CPU and GPU)
  - AMD:
    - Desktop GPU – Since Q4’10 (HD6
    - NB and AIO PC GPU – Since Q2’11
    - High performance APU - Since Q4’11
  - NVIDIA
    - Desktop GPU – Since 2H’11
    - NB GPU – Since 2H’11
  - Intel
    - Desktop/NB CPU – Since 2H’12?
    - Ivy-Bridge / Haswell HD4000 only has eDP output.
  - Qualcomm
  - Samsung Processor

eDP Typical System Implementation

Device Motherboard

Or Video Subsystem

Video / Gfx

Processing

Circuit

eDP

Source device

functions

eDP Interface

Main Link

AUX CH

HPD

Display panel

EDID Memory

Display

Controller

eDP

Sink device

functions

Panel

Backlight Control

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DP1.2 と eDPの相違

Feature	eDP System Configuration	Description
AUX CH		
Backlight Control by way of AUX	Optional	The Source device can control the display backlight, using the AUX CH. Alternatively, the display backlight can be controlled by dedicated signals on the eDP connector. Both methods are described in Section 10.1.
DPCD Registers Reserved for eDP	Required	DisplayPort DPCD Addresses 00700h through 007FFh are reserved for eDP display control use, and are described in Table 10-4.
DPCD Revision	Required	The DPCD revision number is specified at DPCD Address 00000h. For *eDP v1.4* devices, the revision number is 1.3 (indicated by the value 13h), as listed in Table 3-2.
Low AUX Voltage Swing	Optional	Source and Sink devices can use a lower AUX CH voltage swing, as described in Section 4.
Reduced AUX Timing	Required	Reduced timing protocol must be supported, as described in Section 4.
Source device Detection by way of AUX CH	Optional	Pull-up and pull-down resistors are not required on the Source device AUX CH pin for Source device detection. Likewise, the Sink device is not required to perform Source device detection by way of the AUX CH. See the Recommended eDP AUX CH Topology in Figure 3-1.

DP1.2 と eDPの相違（Cont.）

Feature	eDP System Configuration	Description
Main-Link		
Advanced Link Power Management (ALPM)	Required for PSR2 or display stream compression; otherwise, Optional	The ALPM feature is an implementation-specific option that enables fast wake/fast sleep capability in the Sink device. ALPM is required for the support of Panel Self Refresh Version 2 (PSR2) or display stream compression. See Section 5 for ALPM details.
Enhanced Framing	Required	Provides increased robustness over Basic Framing.
Link Rates	A single link rate can be supported	Use a link rate that minimizes the number of lanes needed. eDP includes additional link rates that are not defined in *DP v1.2a*. eDP also includes the option to use a custom link rate. See Section 4 for eDP link rate options.
Fast Link Training	Required for Sink devices	eDP devices must support both Full and Fast Link Training, as defined in *DP v1.2a*.
	Optional for Source devices	eDP devices must support Full Link Training, as defined in *DP v1.2a*; Fast Link Training support is optional.
Main Stream Attribute (MSA) Data	Option to ignore certain Data Fields	See Section 3.7.
Number of Main-Link Lanes	It is recommended to use the fewest number of lanes possible	The general preference for an eDP implementation is to use the minimum number of lanes, which is done by choosing a higher link rate. Appendix B discusses lane count considerations.
Reduced Main-Link Voltage Swing Level	Optional	Can be supported by Source and Sink devices, as described in Section 4.
Secondary-Data Packet	Required for PSR1 or PSR2; otherwise, Optional	Dependent on usage requirements. Required for the optional Panel Self Refresh (PSR) modes, as described in Section 6.

DP1.2 と eDPの相違（Cont.）

Protocol/Policy		
Audio	Optional	Dependent on usage requirements.
Display Authentication / Content Protection	Optional	See Section 3.5. Support of Method 3a is recommended for Sink devices.
Display Stream Compression	Optional	See Section 8.
EDID	Optional	EDID, as well as VESA DisplayID, are recommended implementation-specific options that simplify the use of different Sink devices within a system.
Frame Sync	Required for PSR2; otherwise, Optional	The Frame Sync feature, which uses the Global Time Code (GTC) feature defined in *DP v1.2a*, is required for the support of PSR2. See Section 7.
LCD Panel Self-Test	Optional	Provides a useful system diagnostics tool. See Section 10.2.

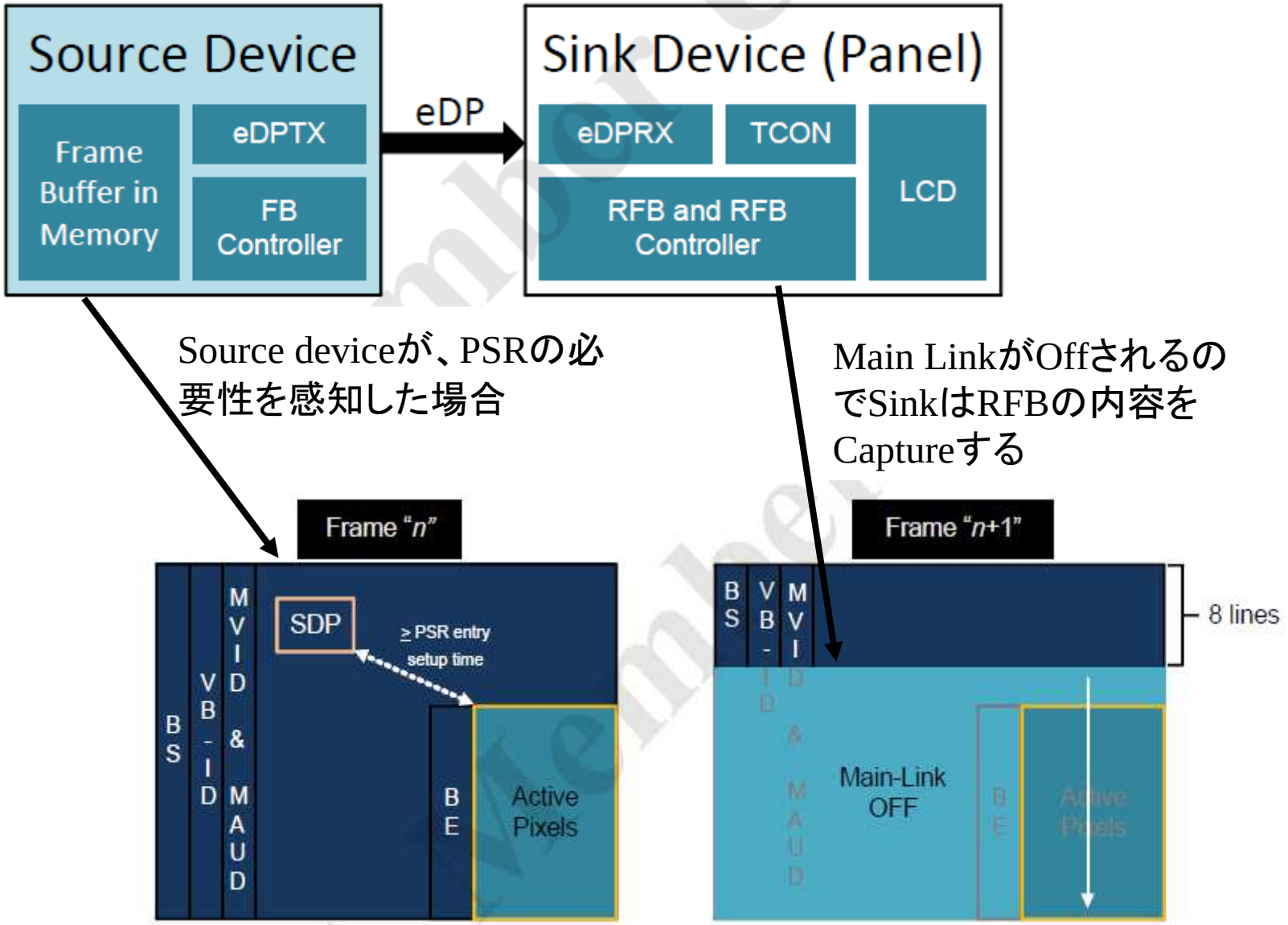
DP1.2 と eDPの相違（Cont.）

Feature	eDP System Configuration	Description
MCCS Support	Optional	Can be used for display control and host-based software on-screen display (OSD), including, for example, backlight control. The Display Control registers defined in Section 3.4 and referenced in Section 10.1 can alternately be used for display control.
Multi-Touch over AUX	Optional	See Section 9.
PSR1	Optional	See Section 6.1.
PSR2	Optional	See Section 6.2.
Regional Backlight Control	Optional	See Section 10.1.
Safe Mode (640x480 or other default video resolution)	Not required	The panel is always driven at native resolution.
Other		
HPD Pin on Sink Device	Optional	Similar to DisplayPort Source and Sink devices, eDP Source and Sink devices typically implement the Hot Plug Detect (HPD) signal, and support all functions related to this signal, including the IRQ HPD pulse used for Sink device status change notification, which also includes link failure notification. Use of the HPD signal, however, is optional. To replace the Sink device-asserted HPD interrupt function, the Source device can instead use Sink device polling. To monitor Main-Link integrity, the Source device should poll the Sink device at regular intervals. Use of HPD is generally preferred over polling by the Source device, because Source device polling increases system power dissipation.
Interface Cable and Connector	Implementation-Specific	The eDP Standard does not specify standard interface connectors or cables, but does provide interconnect recommendations (see Section 12). Connector and cable requirements are implementation-specific, and are influenced by lane count, link rate, system topology, Source device transmitter characteristics, Sink device receiver capability, and other system design factors.
LCDVCC Single Supply	Optional	Use of a single power rail is an implementation-specific option, as is the supply voltage level. See Section 3.6.
Power Sequencing	Implementation-Specific	The eDP Standard does not mandate power sequencing requirements, but does provide recommendations in Section 11.

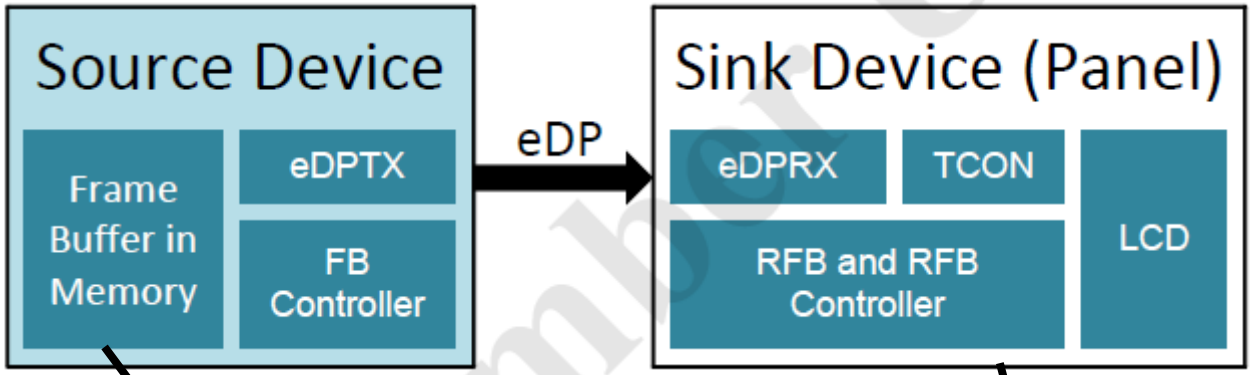
eDP1.3 と eDP1.4の相違

機能	eDP1.3	eDP1.4
Swing Level	4 Level (Std. DP)	6 Level (200mV – 450mV)
Bit rate	3 (Std. DP)	7 (1.62 – 5.4Gbps)
Pre-emphasis	4 (Std. DP)	Arbitrary
PSR (Panel Self Refresh)	Whole Frame only	Partial Frame enable
Compression	No	Yes
Multi touch	No	Yes
Backlight control	Yes	Yes Regional control as well

Panel Self Refresh（PSR1）

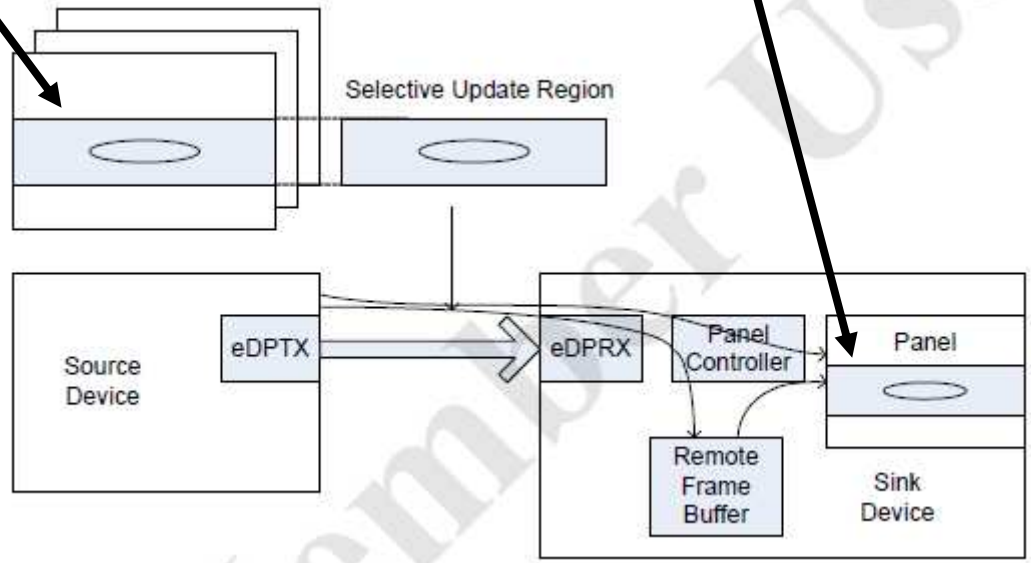


Panel Self Refresh（PSR2）

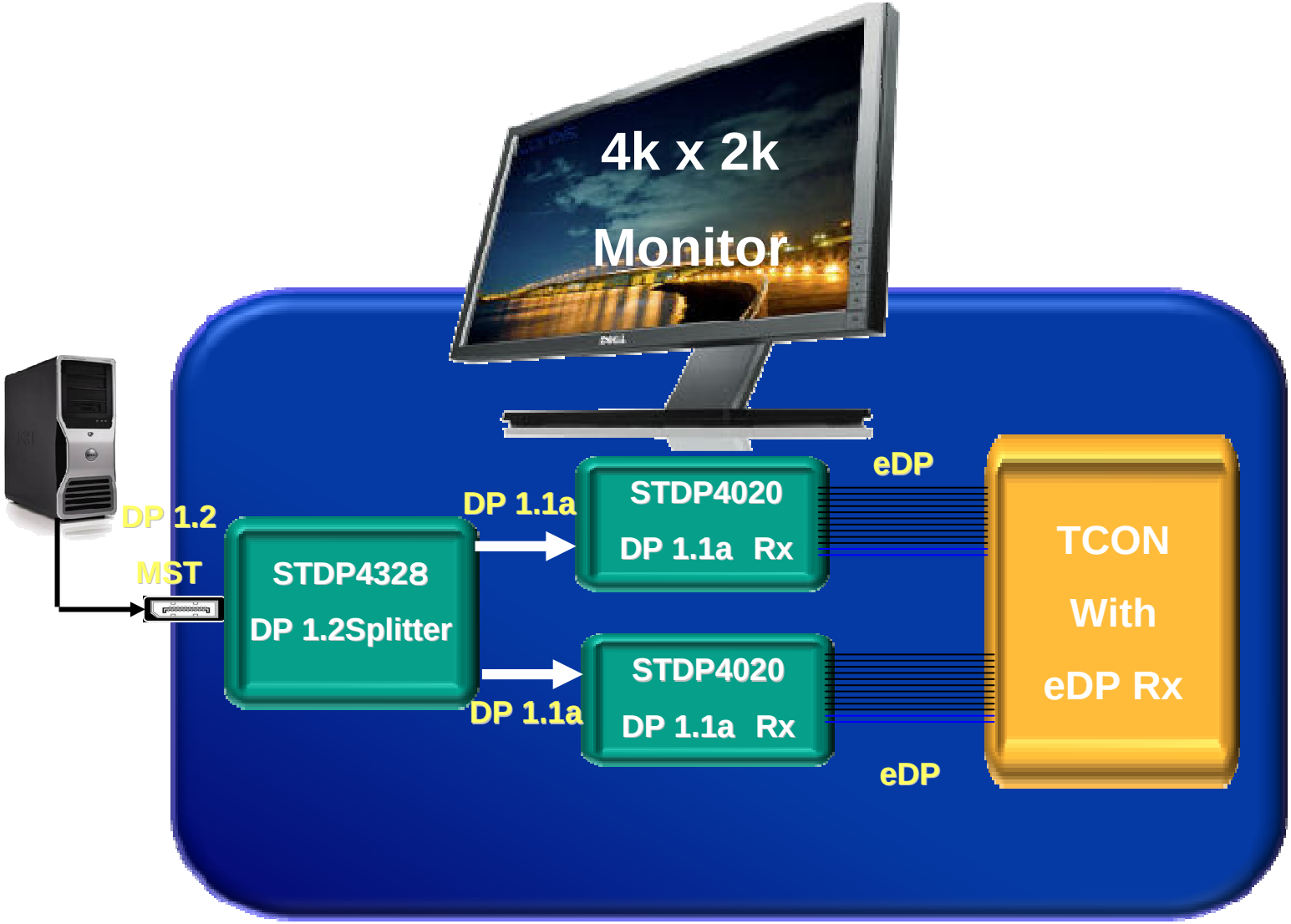


Source deviceが、PSRの必要性を感知した場合、一旦Full FrameをRFBにCaptureし、Region情報をSDPに付加する。

Sink deviceは、SDPのRegion情報に従い、Videoを表示する



eDPのPanel製品への応用



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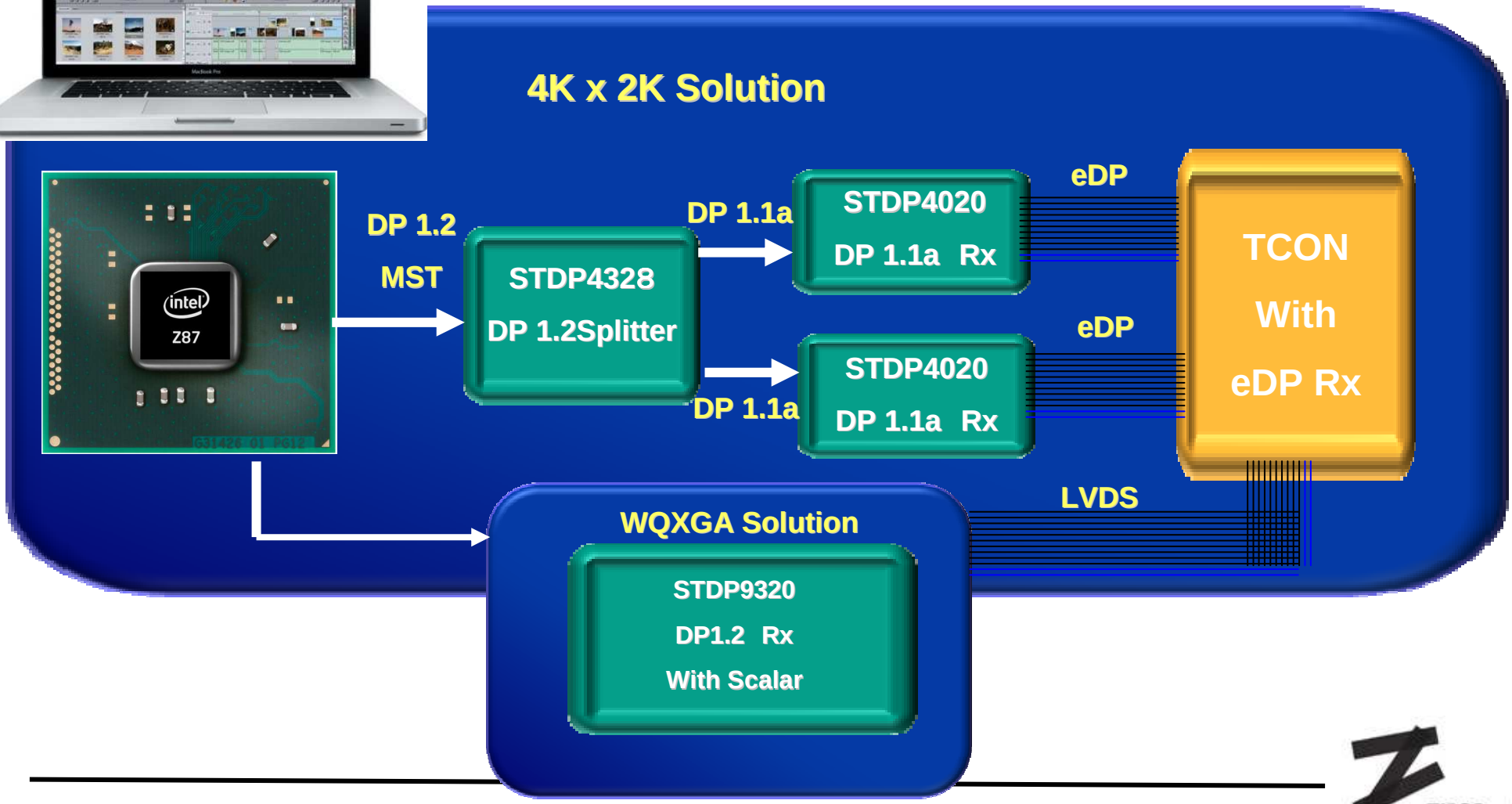
NotePC / AIO PCへの応用



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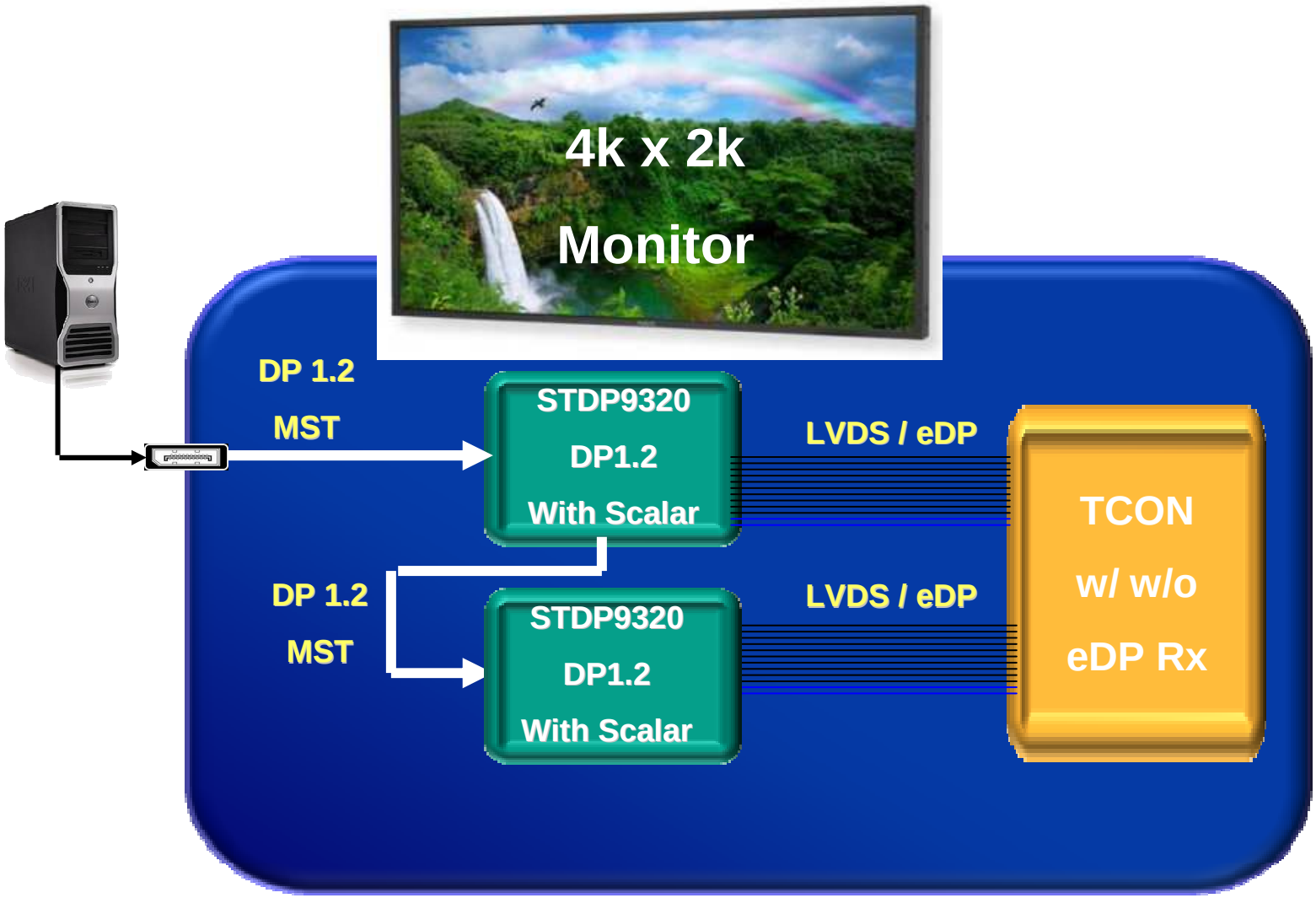
4K x 2K Monitor の実現



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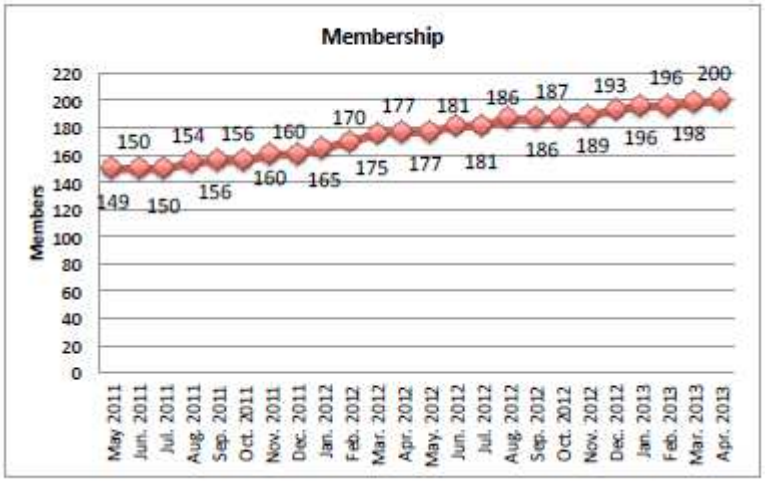
VESA Update（VESA DP Workshop Asiaより）



Global industry alliance としてのVESAメンバーが200社を超えています。

VESA DisplayPort

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VESA Update (Cont.) メンバーの利点

- Be an integral member of an organization that establishes the future direction of the display industry and influences important industry trends.
- Maintain competitive edge by gaining knowledge of new technology standards initiatives as they are originated.
- Network with industry experts from more than 200 leading PC and consumer electronics companies, participate in state-of-the-art technical discussions.
- Decrease manufacturing costs, increase reliability and productivity, and access global markets through participation in standards development efforts and members-only interoperability PlugTests and workshops.
- Expand promotional opportunities by linking to VESA's web site (www.vesa.org) and being featured in VESA literature, press events/releases & trade show demonstrations.

VESA DisplayPort

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VASA Update (Cont.)　現在の検討事項

- DP 1.2b
- DP 1.3
- eDP 1.4 CTG Proposal
- MyDP v1.1
- MPAC v1
- DSC v1
- VHSD Proposal

Displayport Vision

- The Vision: DP would be the only video port on a computer. Particularly on ultra-thin notebook designs.
- It's here today! No VGA, DVI or HDMI!

Microsoft Surface Pro

Dell XPS 13

Lenovo X1 Carbon

Dell XPS 12 Convertible Touch

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Thank you!!