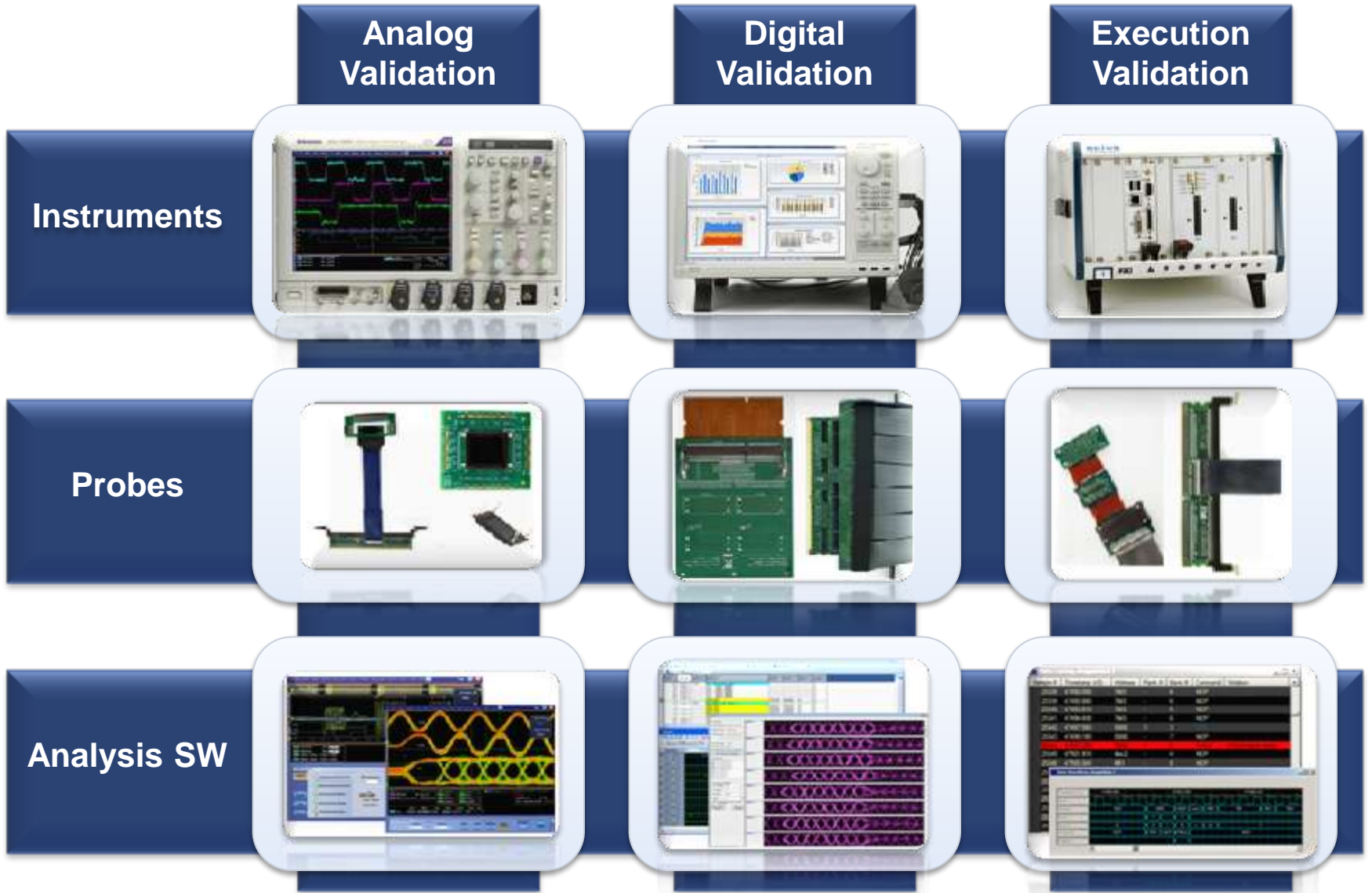


Memory Interface Verification and Debug

Execution Validation Presentation



Memory Validation Continuum



Memory Interface Execution Validation

Measure the bus command and control timing sequences, and compare them to a specification or evaluate them as indicators of bus utilization or performance

Compliance Parameters										
Stat	Num.	Name	Occurrences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)
?	22	SRE Separation from RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,488
?	23	MRS Settle	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,500
?	24	MRS Burst	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,500
?	25	sSREF Time	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	7,500
✓	26	WR Burst	13,386	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	168,523	128102389400761000.0	7,200
✓	27	RD to WR(A) Separation	13,386	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	64,028	70310809855578300.0	13,118
?	28	PDX Slow Exit	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	24,000
?	29	Rank DLL Reset to RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	959,700
✓	30	WR to RD(A) Separation	22,075	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	910,959	35155404927789100.0	26,236
✓	31	RD Burst	22,075	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	164,742	128102389400761000.0	7,200
?	32	sPD Time Min.	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	5,625
?	33	sPD Time Max.	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	70,200,000
✗	34	PRE(A) Bank Settle	26,733	29	R7 R6 R5 R4 R3 R2 R1 R0	00	00	947,528	70273310756988700.0	13,125
✓	35	sREF Time	1,527	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	5,297,689	8384883669867880.0	110,000
✓	36	sACT Time Min.	19,499	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	265,733	24595658764946000.0	37,500
✓	37	sACT Time Max.	19,499	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	265,733	13138706605106.2	70,200,000
✓	38	ACT to RD(A)/WR(A)	19,636	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	19,999	70273310756988700.0	13,125
✓	39	RD to PRE(A)	15,227	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	175,659	82029278164841400.0	11,244
?	40	RD to ACT	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	20,614
✓	41	WR to PRE(A)	4,217	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	164,649	27343092721613700.0	33,732
?	42	WR to ACT	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	20,614
?	43	CKEx Signal After DLL Reset	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	959,700

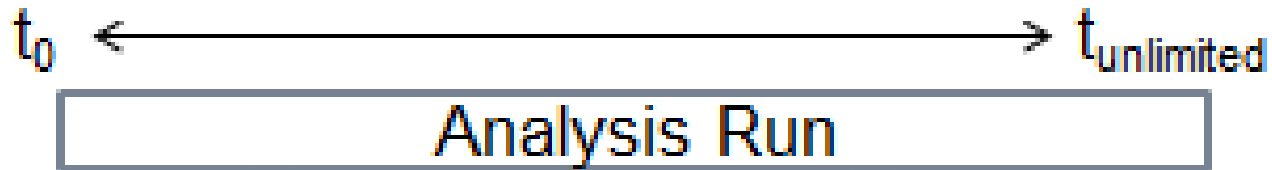
What's unique about Execution Validation



- Typical instrument use a post-capture model

TRIGGER → ACQUIRE → ANALYZE

- Execution Validation use model



- Two equipment options
 1. Logic Analyzer - S/W automates acquisitions
 2. Memory Compliance Analyzer - Real-time Analysis

Specifications Published in JEDEC Standards

**JEDEC
STANDARD**



DDR3 SDRAM Specification

JESD79-3E

192	Pages
118	Figures
80	Tables

What specs are checked?

Num.	Name	Description
1	CMD w/sSREF Rank	Sequential check. A non-NOP/DES command can not occur on a self-refreshing rank.
2	SRE w/sACT Rank	Sequential check. A Self-Refresh Entry (SRE) command can not occur on an active rank.
3	MRS w/sACT Rank	Sequential check. An Mode Register Set (MRS) command can not occur on an active rank.
4	RD(A)/WR(A) during MRS	Sequential check. A read (RD or RDA) or write (WR or WRA) command can not occur during rank MRS cycle.
5	CMD w/sPD Rank	Sequential check. A non-NOP/DES command can not occur on a powered-down rank.
6	RD(A)/WR(A) w/sREF Bank	Sequential check. A read (RD(A)) or write (WR(A)) command can not occur during bank refresh.
7	ACT/REF w/sACT Bank	Sequential check. A activate (ACT) or refresh (REF) command can not occur on an active bank.
8	REF w/sACT Bank	Sequential check. A refresh (REF) command can not occur on an active bank that is reading or writing.
9	RD(A)/WR(A) to sPRE Bank	Sequential check. A read (RD(A)) or write (WR(A)) command can not occur during on an inactive (precharged) bank.
10	d4ACT	The minimum time between any four activate (ACT) commands to the same rank must meet tFAW.
11	PDX Fast Exit	Power-Down Exit (PDX/PRX) to any valid command (PRE(A)/REF/ACT/MRS) must meet tXP.
12	SRX Exit	Self-Refresh Exit (SRX/PRX) to any command not requiring a locked DLL (PRE(A)/REF/ACT/MRS/SRE) must meet tXS.
13	dACT	The minimum time between two activate (ACT) commands must meet tRRD.
14	PRE(A) Rank Settle	Minimum time from a PRE(A) command to any valid command on the same rank (MRS/SRE) must meet tRP.
15	REF Before SRE	Sequential check. At least one refresh (REF) command is required between self refreshed (SRX to SRE).
16	SRE Separation from PRE(A)	If the last valid command received before a self-refresh entry (SRE) was any precharge PRE(A), then the separation between these two commands must meet tPREPDEN.
17	SRE Separation from REF	If the last valid command received before a self-refresh entry (SRE) was a refresh (REF), then the separation between these two commands must meet tREFPDEN.
18	SRE Separation from ACT	If the last valid command received before a self-refresh entry (SRE) was a activate (ACT), then the separation between these two commands must meet tACTPDEN.
19	SRE Separation from MRS	If the last valid command received before a self-refresh entry (SRE) was a mode register set(MRS), then the separation between these two commands must meet tMRSPDEN.
20	SRE Separation from WR	If the last valid command received before a self-refresh entry (SRE) was a write (WR), then the separation between these two commands must meet tWRPDEN.
21	SRE Separation from WRA	If the last valid command received before a self-refresh entry (SRE) was a write w/auto-precharge (WRA), then the separation between these two commands must meet tWRAPDEN.
22	SRE Separation from RD(A)	If the last valid command received before a self-refresh entry (SRE) was a read (RD(A)), then the separation between these two commands must meet tRDPDEN.
23	MRS Settle	Minimum time from an mode register set (MRS) command to any other valid command that is not an MRS must meet tMOD.
24	MRS Burst	Minimum from the first to the next and subsequent mode register set (MRS) commands must meet tMRD.
25	sSREF Time	The minimum amount of time in self-refresh must meet tCKESR.
26	WR Burst	The minimum amount of time between write (WR(A)) commands must meet tCCD.
27	RD to WR(A) Separation	The minimum amount of time between read (RD) and write (WR(A)) commands must meet tNRTW.
28	PDX Slow Exit	Power-Down Exit (PDX/PRX) Slow Exit (MRS_A12 bit low) to read (RD(A) command must meet tXPDLL.
29	Rank DLL Reset to RD(A)	Read (RD(A)) must wait tDLLK after reset.
30	WR to RD(A) Separation	The minimum amount of time between write (WR) and read (RD(A)) commands must meet tNWSTR.
31	RD Burst	The minimum amount of time between read (RD(A)) commands must meet tCCD.
32	sPD Time Min.	The minimum amount of time a rank must stay in power-down (PDE to PDX) must meet tPDmin.
33	sPD Time Max.	The maximum amount of time a rank can stay in power-down (PDE to PDX) must meet tPDmax.
34	PRE(A) Bank Settle	Minimum time from a PRE(A) command to any valid command on the same bank must meet tRP.
35	sREF Time	The minimum amount of time in refresh must meet tRFC.
36	sACT Time Min.	The minimum amount of time a bank must stay active (ACT to PRE(A)) must meet tRASmin.
37	sACT Time Max.	The maximum amount of time a bank can stay active (ACT to PRE(A)) must meet tRASmax.
38	ACT to RD(A)/WR(A)	The minimum amount of time from a activate (ACT) command to a read (RD(A)) or write (WR(A)) command must meet tNARW.
39	RD to PRE(A)	The minimum amount of time from a read (RD) command to a precharge (PRE(A)) command must meet tNRP.
40	RD to ACT	The minimum amount of time from a read (RD) command to a activate (ACT) command must meet tNRA.
41	WR to PRE(A)	The minimum amount of time from a write (WR) command to a precharge (PRE(A)) command must meet tNWP.
42	WR to ACT	The minimum amount of time from a write (WR) command to a activate (ACT) command must meet tNWA.
43	CKEx Signal After DLL Reset	Rank CKEx must remain high tDLLK time after a DLL Reset.

How are the event values set?

DDR System Setup

System Name: Add Del Rename

DDR System: DDR Spec.

MHz DDR Clock

of Ranks (Chip Selects)

Total Addressable Space

Data bus (DQ) Addressing Length

High Temp. Env. (85C-95C)

Read/Writes

Additive Latency

Additive Latency Reserved (AL)

CAS Latency (CL)

CAS Write Latency (CWL)

Burst Length

Write Recovery (WR)

Registered

Information

8 # of Banks

536 MB Rank Memory (64-bit)

2144 MB System Memory (64-bit)

1 KB Page Size

11 Read Latency (RL)

8 Write Latency (WL)

13 Row Address Length (bits)

10 Column Address Length (bits)

24 WRA Precharge Delay

4 Min. RDA Precharge Delay

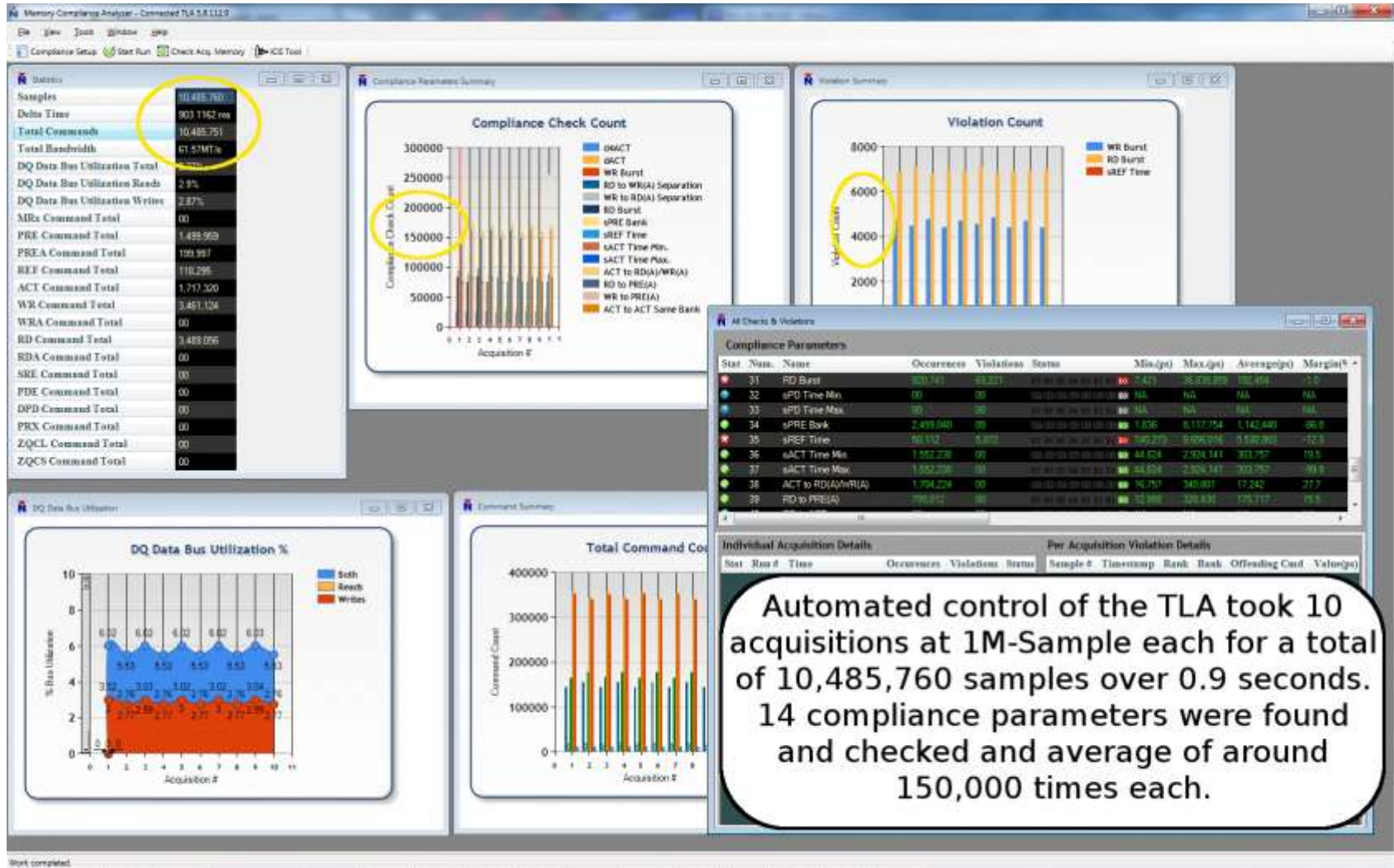
Compliance Timing Parameters

Timing Parameters: Add Del Rename

tACTPDEN	<input type="text" value="1"/> ck	tRASmin	<input type="text" value="37500"/> ps	tWRAPDEN	<input type="text" value="Derived"/> ck
tCCD	<input type="text" value="4"/> ck	tRCD	<input type="text" value="12500"/> ps	tWTR	<input type="text" value="7500"/> ps
tCKESR	<input type="text" value="10"/> ns	tRDPDEN	<input type="text" value="Derived"/> ck	tXP	<input type="text" value="7500"/> ps
tDLLK	<input type="text" value="512"/> ck	tREFPDEN	<input type="text" value="1"/> ck	tXPDLL	<input type="text" value="25"/> ns
tFAW_1Kb	<input type="text" value="40"/> ns	tRFC_512Mb	<input type="text" value="90"/> ns	tXS	<input type="text" value="Derived"/> ck
tFAW_2Kb	<input type="text" value="50"/> ns	tRFC_1Gb	<input type="text" value="110"/> ns	tNARW	<input type="text" value="Derived"/> ck
tMOD	<input type="text" value="12"/> ck	tRFC_2Gb	<input type="text" value="160"/> ns	tNRA	<input type="text" value="Derived"/> ck
tMRD	<input type="text" value="4"/> ck	tRFC_4Gb	<input type="text" value="300"/> ns	tNRP	<input type="text" value="Derived"/> ck
tMRSPDEN	<input type="text" value="12"/> ck	tRFC_8Gb	<input type="text" value="350"/> ns	tNRTW	<input type="text" value="Derived"/> ck
tPDmin	<input type="text" value="7500"/> ps	tRP	<input type="text" value="12500"/> ps		<input type="text" value=""/> ck
tPDmax	<input type="text" value="70200"/> ns	tRRD_1Kb	<input type="text" value="10"/> ns		<input type="text" value=""/> ck
tPDmax_HT	<input type="text" value="35100"/> ns	tRRD_2Kb	<input type="text" value="10"/> ns		<input type="text" value=""/> ck
tPREPDEN	<input type="text" value="1"/> ck	tRTP	<input type="text" value="7500"/> ps		
tRASmax	<input type="text" value="70200"/> ns	tWR	<input type="text" value="15"/> ns		
tRASmax_HT	<input type="text" value="35100"/> ns	tWRPDEN	<input type="text" value="Derived"/> ck		

- Standard system setups are provided, and can then be modified
- Once the memory system is setup, any timing parameter can be modified

Execution Validation Produces Performance Stats



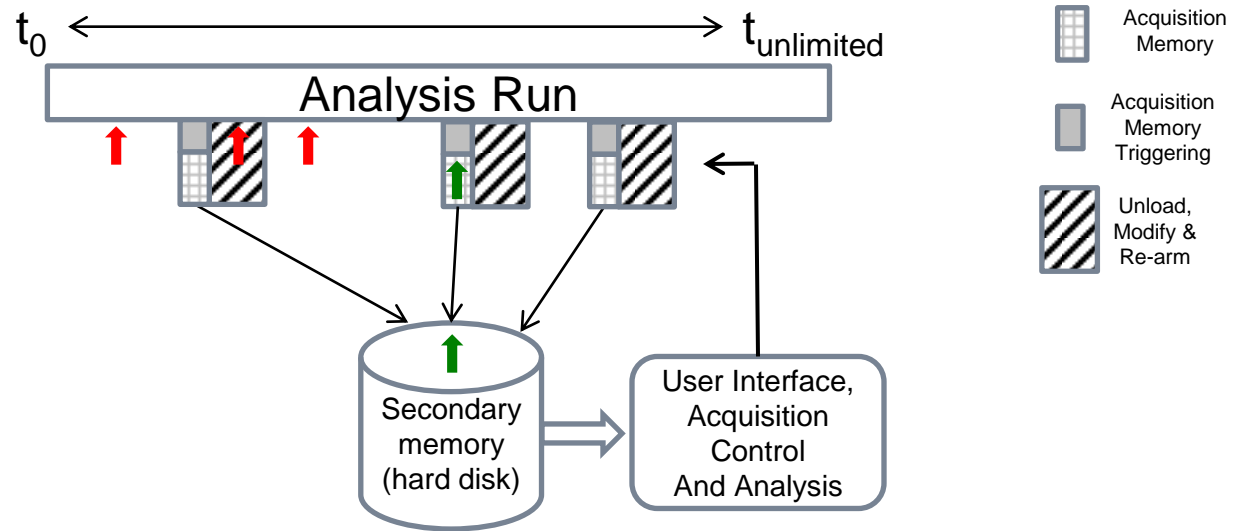
Automated control of the TLA took 10 acquisitions at 1M-Sample each for a total of 10,485,760 samples over 0.9 seconds. 14 compliance parameters were found and checked and average of around 150,000 times each.

Benefits of Real-Time + Post Capture

	ACC (Address/Command/Control)	ACC+DQ (Address/Command/Control/Data)
At-Speed / Real-Time	MCA	MCA+LA
Post Capture		LA

MCA Advantages	LA Advantages
Capture Depth 1Gcycles	State Capture of ALL DDR Signals
Cost	20ps High Speed Timing / MagniVu
PA Real Time + LA State Analysis	Analog Mux
	Multi Bus Cross Correlation

Post-Capture Protocol Compliance Analysis



- LA Memory Compliance Analysis Package enables automated sweeps of multiple transitions, which would result in violation detection over many acquisitions.
- When violations are occurring frequently the likelihood of capture increases and the analysis time decreases.
- However, near the edge of margin envelopes, intermittency increases, resulting in difficulty to observe and capture the event.

Results per *Session* & per *Acquisition*

Compliance Parameters										
Stat	Num.	Name	Occurrences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)
?	22	SRE Separation from RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,488
?	23	MRS Settle	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,500
?	24	MRS Burst	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,500
?	25	sSREF Time	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	7,500
?	26	WR Burst	13,386	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	168,523	128102389400761000.0	7,200
?	27	RD to WR(A) Separation	13,386	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	64,028	70310809855578300.0	13,118
?	28	PDX Slow Exit	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	24,000
?	29	Rank DLL Reset to RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	959,700
?	30	WR to RD(A) Separation	22,075	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	910,959	35155404927789100.0	26,236
?	31	RD Burst	22,075	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	164,742	128102389400761000.0	7,200
?	32	sPD Time Min.	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	5,625
?	33	sPD Time Max.	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	70,200,000
*	34	PRE(A) Bank Settle	26,733	29	R7 R6 R5 R4 R3 R2 R1 R0	00	00	947,528	70273310756988700.0	13,125
?	35	sREF Time	1,527	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	5,297,689	8384883669867880.0	110,000
?	36	sACT Time Min.	19,499	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	265,733	24595658764946000.0	37,500
?	37	sACT Time Max.	19,499	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	265,733	13138706605106.2	70,200,000
?	38	ACT to RD(A)/WR(A)	19,936	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	19,999	70273310756988700.0	13,125
?	39	RD to PRE(A)	19,227	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	175,659	82029278164841000.0	11,244
?	40	RD to ACT	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	20,614
?	41	WR to PRE(A)	4,217	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	164,649	27343032721613700.0	33,750
?	42	WR to ACT	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	20,614
?	43	CKEx Signal After DLL Res	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	99,700

Event occurrences and details per Acquisition

Total Event Occurrences

Individual Acquisition Details									
Stat	Run #	Time	Occurrences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	
*	1	10/10/2011 1:38:00 PM	2501	2	R7 R6 R5 R4 R3 R2 R1 R0	00	00	1,038,534	
*	2	10/10/2011 1:38:05 PM	2644	3	R7 R6 R5 R4 R3 R2 R1 R0	00	00	950,031	
*	3	10/10/2011 1:38:11 PM	2545	3	R7 R6 R5 R4 R3 R2 R1 R0	00	00	1,029,172	
*	4	10/10/2011 1:38:16 PM	2722	3	R7 R6 R5 R4 R3 R2 R1 R0	00	00	936,685	
*	5	10/10/2011 1:38:22 PM	2670	4	R7 R6 R5 R4 R3 R2 R1 R0	00	00	970,402	
*	6	10/10/2011 1:38:28 PM	2800	4	R7 R6 R5 R4 R3 R2 R1 R0	00	00	890,874	
*	7	10/10/2011 1:38:33 PM	2543	2	R7 R6 R5 R4 R3 R2 R1 R0	00	00	980,858	
*	8	10/10/2011 1:38:39 PM	2806	1	R7 R6 R5 R4 R3 R2 R1 R0	00	00	896,071	
*	9	10/10/2011 1:38:44 PM	2697	7	R7 R6 R5 R4 R3 R2 R1 R0	00	00	880,706	
?	10	10/10/2011 1:38:50 PM	2805	0	R7 R6 R5 R4 R3 R2 R1 R0	00	00	920,762	

Individual Event Analysis

All Checks & Violations

Compliance Parameters

Name	Occurences	Violations	Status	ps	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)
WR Burst	13	00	R7 R6 R5 R4 R3 R2 R1 R0 00	00	168,523	128102389400761000.0	7,200	
RD to WR(A) Separation	13	00	R7 R6 R5 R4 R3 R2 R1 R0 NA	00	64,028	70310809855578300.0	13,118	
PDX Slow Exit	00	00	R7 R6 R5 R4 R3 R2 R1 R0 NA	NA	NA	NA	24,000	
Rank DLL Reset to RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0 NA	NA	NA	NA	959,700	
WR to RD(A) Separation	22	00	R7 R6 R5 R4 R3 R2 R1 R0 00	00	910,959	35155404927789100.0	26,236	
RD Burst	22,075	00	R7 R6 R5 R4 R3 R2 R1 R0 00	00	164,742	128102389400761000.0	7,200	
sPD Time Min.	00	00	R7 R6 R5 R4 R3 R2 R1 R0 NA	NA	NA	NA	5,625	
sPD Time Max.	00	00	R7 R6 R5 R4 R3 R2 R1 R0 NA	NA	NA	NA	70,200.0	
PRE(A) Bank Settle	26,733	29	R7 R6 R5 R4 R3 R2 R1 R0 00	00	947,528	70273310756988700.0	13,125	
sREF Time	1,527	00	R7 R6 R5 R4 R3 R2 R1 R0 00	00	5,297,689	8384883669867880.0	110,000	
sACT Time Min.	19,499	00	R7 R6 R5 R4 R3 R2 R1 R0 00	00	265,733	24595658764946000.0	37,500	
sACT Time Max.	19,499	00	R7 R6 R5 R4 R3 R2 R1 R0 00	00	265,733	13138706605106.2	70,200,000	

Individual Acquisition Details

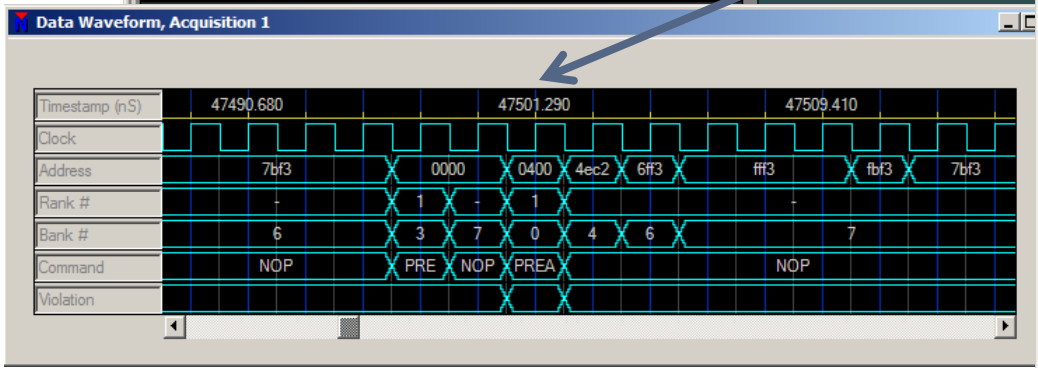
Stat	Run #	Time	Occurences	Violations	Status
✖	1	10/10/2011 1:38:00 PM	2501	2	R7 R6 R5 R4 R3 R2 R1 R0
✖	2	10/10/2011 1:38:05 PM	2644	3	R7 R6 R5 R4 R3 R2 R1 R0
✖	3	10/10/2011 1:38:11 PM	2545	3	R7 R6 R5 R4 R3 R2 R1 R0
✖	4	10/10/2011 1:38:16 PM	2722	3	R7 R6 R5 R4 R3 R2 R1 R0
✖	5	10/10/2011 1:38:22 PM	2670	4	R7 R6 R5 R4 R3 R2 R1 R0
✖	6	10/10/2011 1:38:28 PM	2800	4	R7 R6 R5 R4 R3 R2 R1 R0
✖	7	10/10/2011 1:38:33 PM	2543	2	R7 R6 R5 R4 R3 R2 R1 R0

Per Acquisition Violation Details

Sample #	Timestamp	Rank	Bank	Offending Cmd	Value(ps)	Margin
25344	49860801	1	3	PRE	3,731	-71.6
114431	216905195	0	7	PRE	11,894	-94

Individual acquisition and event selection

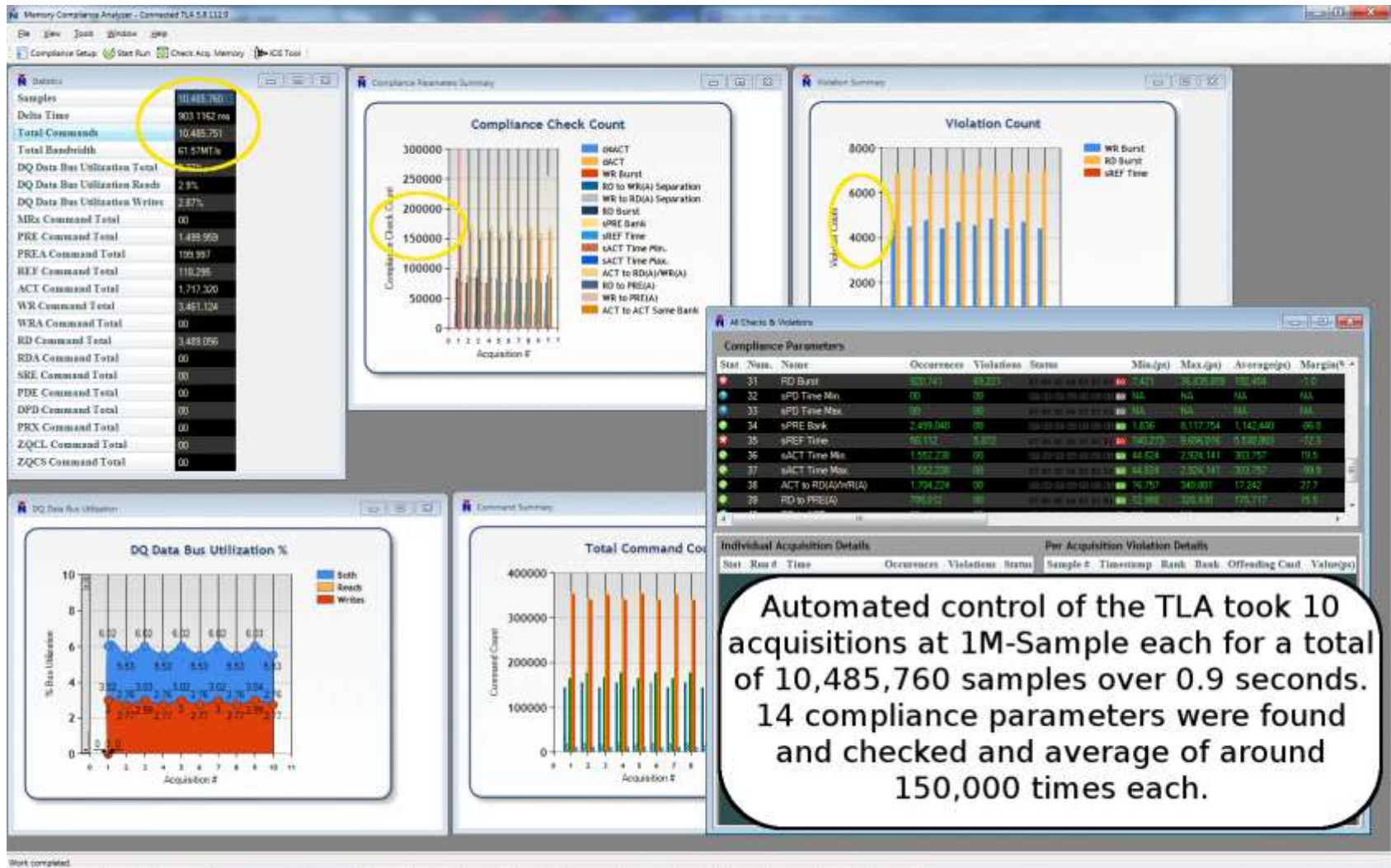
State and Timing before and after an event



Data Listing, Acquisition 1

Sample #	Timestamp (nS)	Address	Rank #	Bank #	Command	Violation
25338	47490.050	7bf3	-	6	NOP	
25339	47490.680	7bf3	-	6	NOP	
25340	47493.310	7bf3	-	6	NOP	
25341	47494.430	7bf3	-	6	NOP	
25342	47497.560	0000	1	3	PRE	
25343	47498.180	0000	-	7	NOP	
25344	47501.290	0400	1	0	PREA	PRE(A) Bank Settle
25345	47501.910	4ec2	-	4	NOP	
25346	47505.040	6ff3	-	6	NOP	
25347	47505.660	fff3	-	7	NOP	
25348	47508.790	fff3	-	7	NOP	
25349	47509.410	fff3	-	7	NOP	
25350	47512.540	fbf3	-	7	NOP	
25351	47513.160	7bf3	-	7	NOP	
25352	47516.270	7bf3	-	7	NOP	
25353	47516.890	7bf3	-	6	NOP	

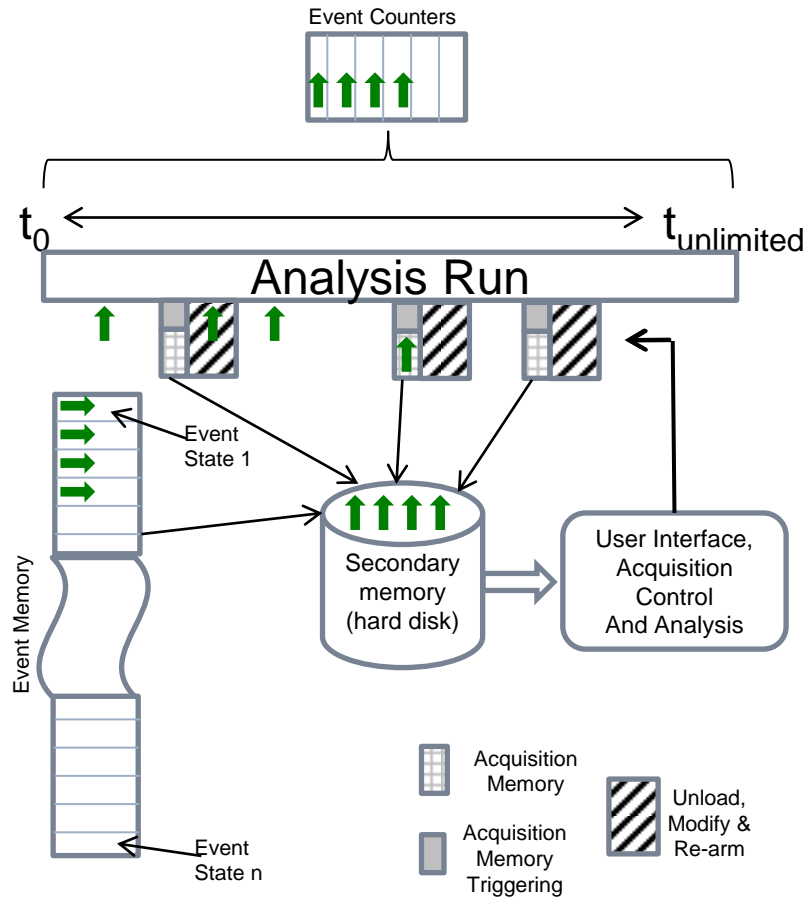
Multi-acquisition Automation Session



Automated control of the TLA took 10 acquisitions at 1M-Sample each for a total of 10,485,760 samples over 0.9 seconds. 14 compliance parameters were found and checked and average of around 150,000 times each.

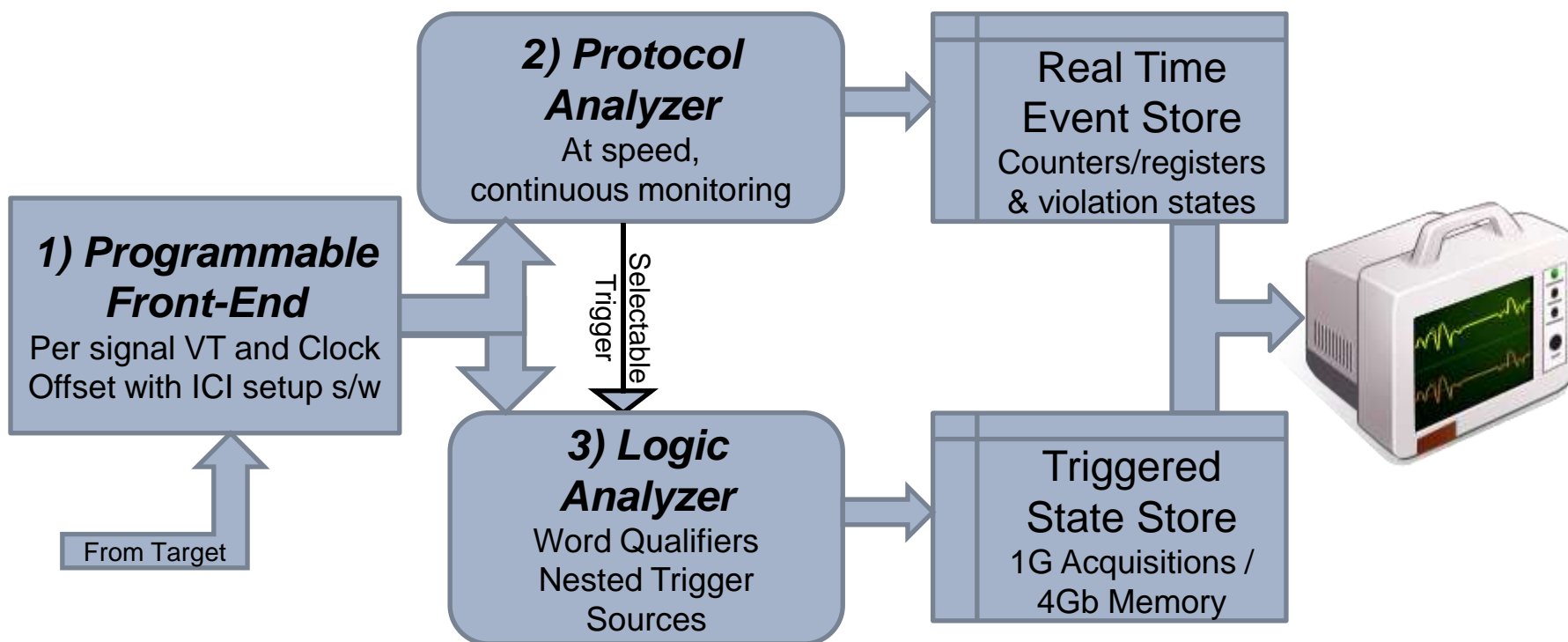
Real-time Protocol Compliance Analysis

Event Counters and State Memory continue to update **AT-SPEED**, with results displayed in **REAL-TIME**, **While....**



...the Acquisition Memory is unloaded, analyzed and trigger re-armed

Real-time Memory Compliance Analyzer



DUAL INSTRUMENT PLUS PROGRAMMABLE FRONT-END

Memory Compliance Analyzer

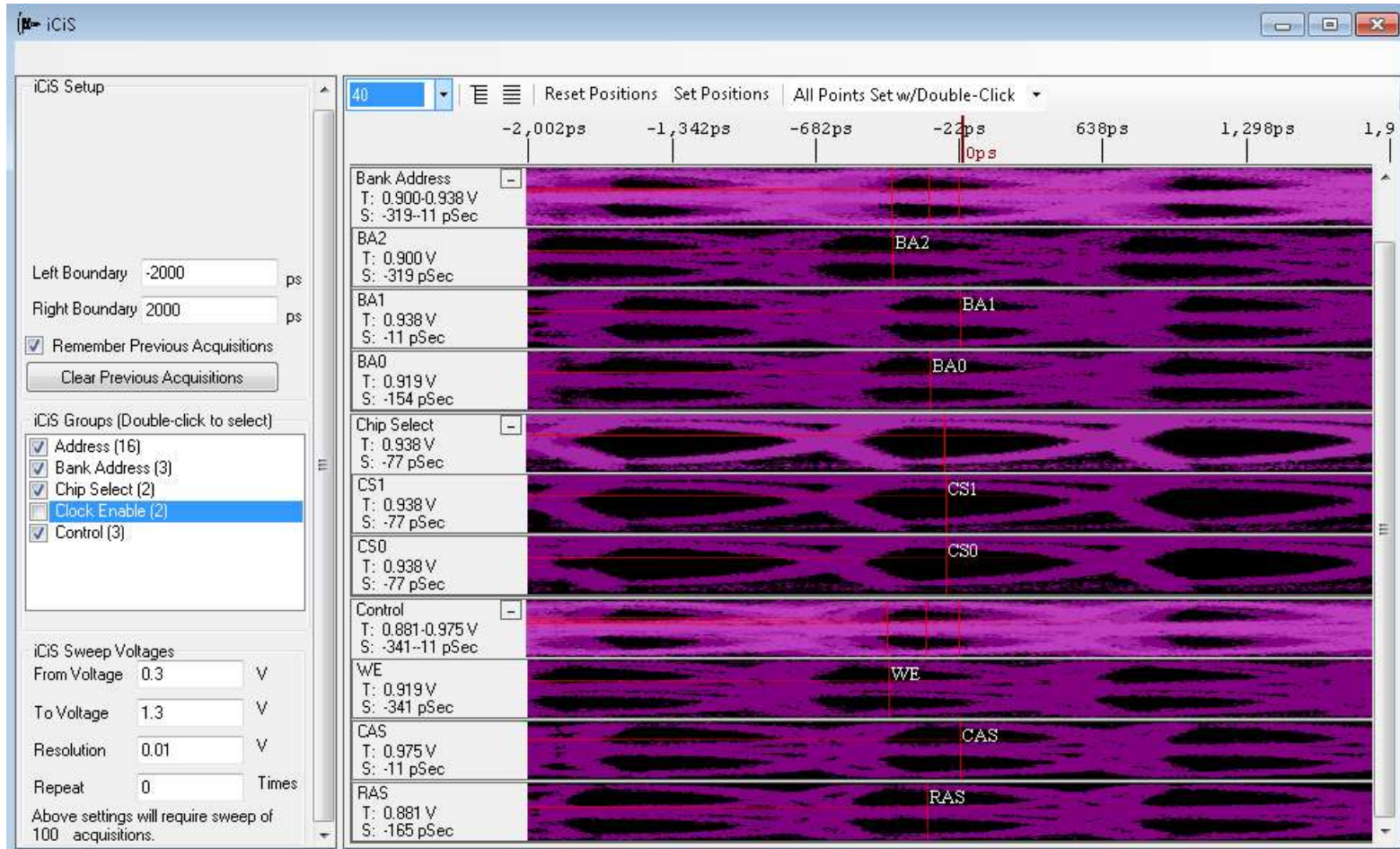
REAL-TIME PROTOCOL COMPLIANCE ANALYSIS

- Analysis 160+ categories of JEDEC spec parameters
- Includes Power up/down, self-refresh and auto-precharge (RDA/WRA) analysis
- Timing and State analysis
- HTML reports / XML exporting



Real-time
AND
Post Capture
Compliance Analysis
=====
Command/Address

Programmable Front-End / High Speed Eye Diagrams

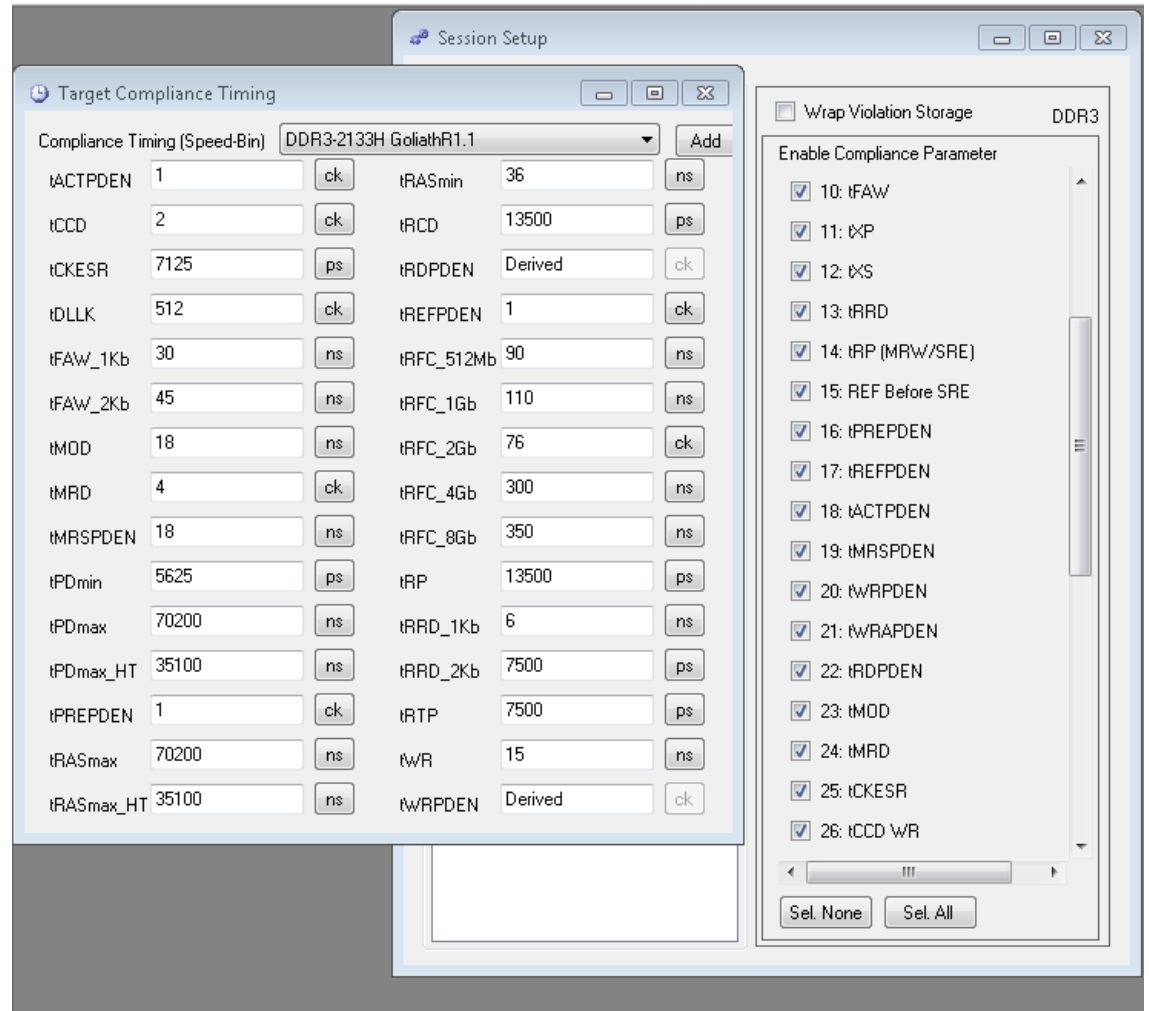


Automated Analysis Sessions

- One or Many Acquisitions / One or Both Analyzers
- Protocol Analysis Session
 - Protocol Analyzer runs until stopped
 - Violations and statistics are reported
- Single Acquisition Session
 - Protocol Analyzer runs until the state analyzer is triggered
 - Violations and statistics are reported.
 - State/Timing data is acquired and available for analysis
- Multi-Acquisition Session
 - Protocol Analyzer runs until the state analyzer is triggered
 - Results are stored in disk memory and analysis is restarted
 - Trigger conditions can be modified mid-session.

Compliance Timing and Parameter Selection

- Spec timing included
- Customize timing per target and margin
- Enable one, some or all violations



Logic Analyzer Acquisition Control

- 8 IF/THEN/ELSE States
- Each State supports multiple AND/OR clauses
- 1 Global Storage qualifier
- 4 Word Recognizers
- 2 Counters

The screenshot shows the 'Acquisition Control' window for a setup named 'Goliath'. The interface is divided into several sections:

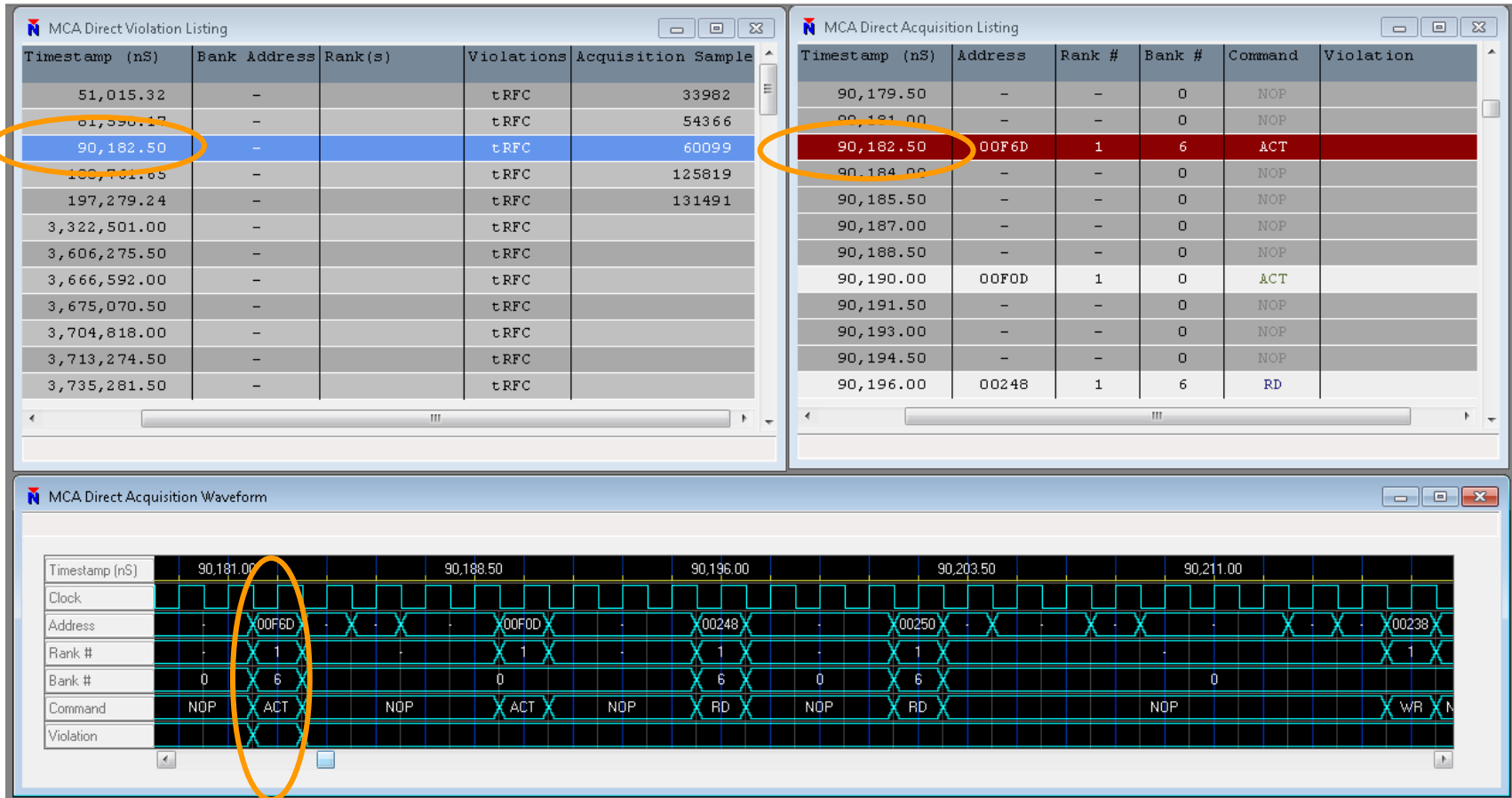
- Storage Control:** Post-Trigger Delay is set to 1,000; Pre-Trigger Limit is set to None; Trigger In is set to Off.
- Violation Control:** Includes an 'Edit Violations' button and a checkbox for 'Wrap Violation Store' which is currently unchecked.
- Word Recognizers:** A table with columns for Signal, Bank Addr, Command, Address, and Rank. It lists four recognizers (WR1-WR4) with various settings.
- Counter Load Values:** Counter 1 is set to 1000000 (Start at Load Value); Counter 2 is set to 2222 (Start at 0).
- Trigger Control:** Trigger Status is OK. Buttons for 'Edit', 'Add', 'Insert', 'Delete', 'Clause Logic', and 'Else If' are present.
- Global:** If Anything, Then Store.
- State 1:** State 1. If Anything, Then Load Counter 1 AND Go To State 2.
- State 2:** State 2. If WR2 Matches, Then Increment Counter 2 AND Go To State 3. Else If Anything, Then Go To State 3.

Real-time Compliance Results

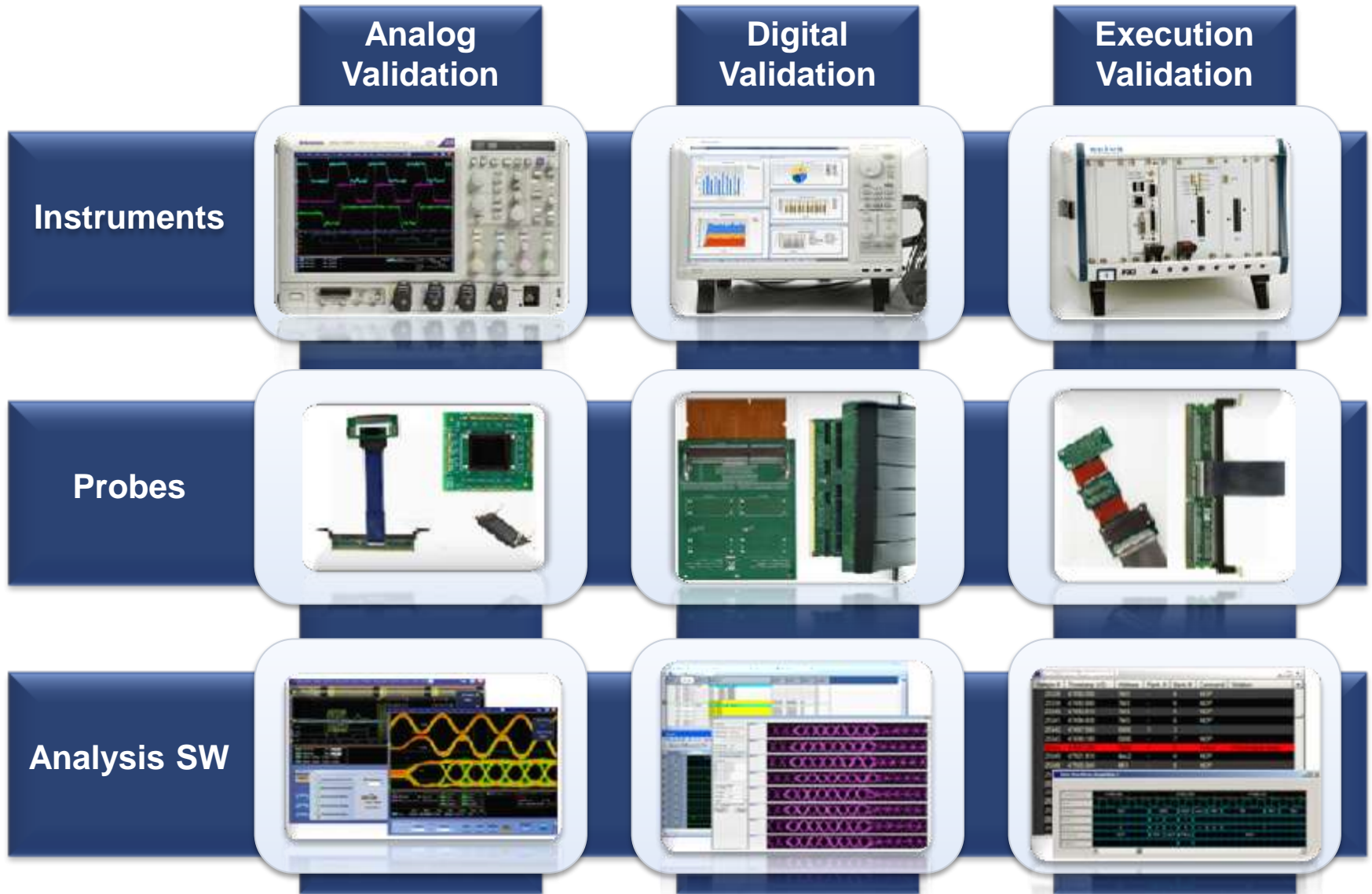
Compliance Parameters										
Stat	Num.	Name	Occurrences	Violations	Status	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec. Value(ps)
?	22	SRE Separation from RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,488
?	23	MRS Settle	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,500
?	24	MRS Burst	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	22,500
?	25	sSREF Time	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	7,500
✓	26	WR Burst	13,386	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	168,523	128102389400761000.0	7,200
✓	27	RD to WR(A) Separation	13,386	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	64,028	70310809855578300.0	13,118
?	28	PDX Slow Exit	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	24,000
?	29	Rank DLL Reset to RD(A)	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	959,700
✓	30	WR to RD(A) Separation	22,075	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	910,959	35155404927789100.0	26,236
✓	31	RD Burst	22,075	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	164,742	128102389400761000.0	7,200
?	32	sPD Time Min.	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	5,625
?	33	sPD Time Max.	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	70,200,000
✗	34	PRE(A) Bank Settle	26,733	29	R7 R6 R5 R4 R3 R2 R1 R0	00	00	947,528	70273310756988700.0	13,125
✓	35	sREF Time	1,527	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	5,297,689	8384883669867880.0	110,000
✓	36	sACT Time Min.	19,499	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	265,733	24595658764946000.0	37,500
✓	37	sACT Time Max.	19,499	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	265,733	13138706605106.2	70,200,000
✓	38	ACT to RD(A)/WR(A)	19,636	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	19,999	70273310756988700.0	13,125
✓	39	RD to PRE(A)	15,227	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	175,659	82029278164841400.0	11,244
?	40	RD to ACT	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	20,614
✓	41	WR to PRE(A)	1,217	00	R7 R6 R5 R4 R3 R2 R1 R0	00	00	164,649	27343092721613700.0	33,732
?	42	WR to ACT	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	20,614
?	43	CKEx Signal After DLL Reset	00	00	R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	959,700

Real-time event statistics

Violations and Acquisitions Must Be Time Correlated



Memory Validation Continuum

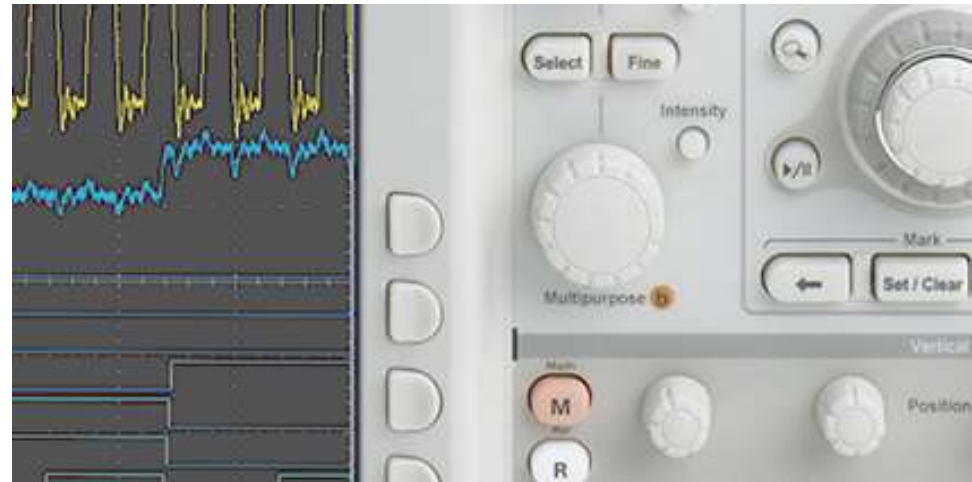


Benefits of Real-Time + Post Capture

	ACC (Address/Command/Control)	ACC+DQ (Address/Command/Control/Data)
At-Speed / Real-Time	MCA	MCA+LA
Post Capture		LA

MCA Advantages	LA Advantages
Capture Depth 1Gcycles	State Capture of ALL DDR Signals
Cost	20ps High Speed Timing / MagniVu
PA Real Time + LA State Analysis	Analog Mux
	Multi Bus Cross Correlation

Thank You



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