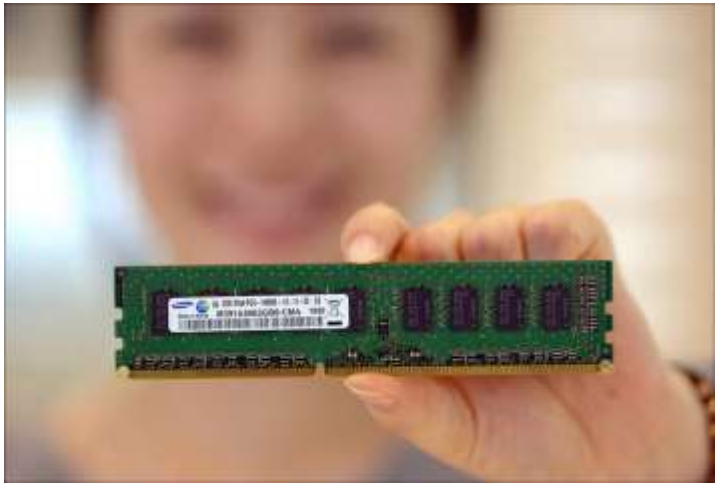
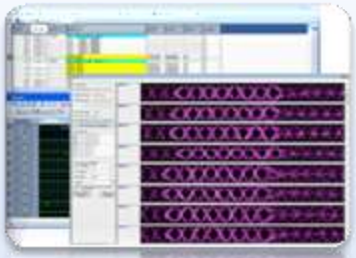
Memory Interface Verification and Debug

Digital Validation Presentation



Tektronix®

Memory Validation Continuum

	Analog Validation	Digital Validation	Execution Validation
Instruments			
Probes			
Analysis SW			

Tektronix®

Key differentiators

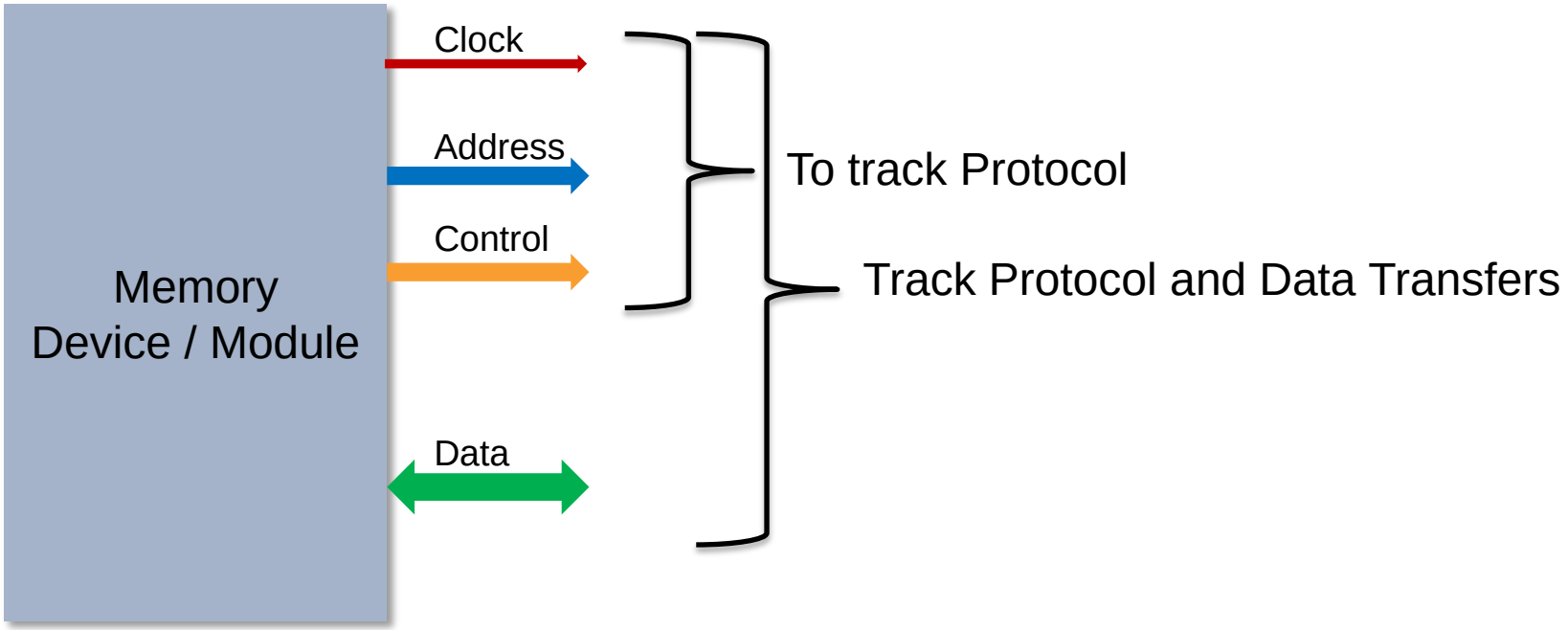
- Instruments capable of supporting all the DDR3/4 debug and validation needs available
- High Fidelity Probing solutions preserve the analog characteristics and bridge different stages of validation
- A large portfolio of probing solutions for various applications.
  - Slot Interposers for various form factors
    - ACC & ACCD types
  - Socketed and solder down Memory Component Interposers for different package types
- Unique capabilities with Industry leading specification for Logic Debug and Protocol validation
  - Analog Mux (quickly scan through all the signals on the DDR bus)
  - 50GHz (20ps) High Speed Timing (MagniVu) across all channels
  - Any channel can be used as a clock*
- Execution / Compliance validation
  - On TLA : CMD/ADDR/DATA Post capture
  - On MCA; CMD/ADDR Real-Time+Post capture
  - Single probe enables TLA, MCA or both simultaneously
- Correlation across different validation phases
  - Common Probing
  - iView and Analog Mux
  - Compliance Analysis common to both TLA and MCA

* needs a custom support package

Memory Probing

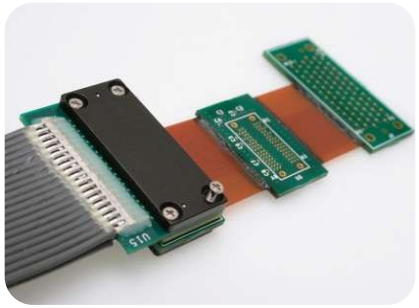
Tektronix®

Memory Probing



DDR3/4 Memory Form Factors and Probing Solutions

BGA Component



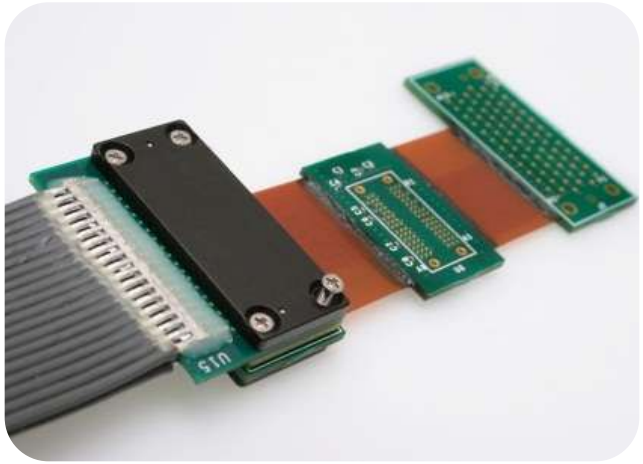
DIMM

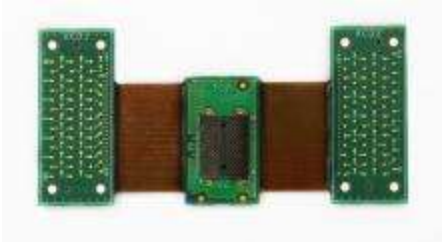
SO-DIMM

Tektronix®

DDR3/4 Memory Component Interposers

- MCI's are used for probing signals from individual Memory Components
- Comes with a Custom Socket that needs to be soldered to Target system
- Quickly swap TLA & oscilloscope interposers on the same target. Quickly move interposers to different target.
- No special footprints or special routing requirements
- Memory Component Interposer Types
  - Logic Analyzer and Oscilloscope
  - Direct Attach or Socketed interposers
  - x4/x8 and x16 Memory Component types





Tektronix®

DDR3/4 ACC Interposers

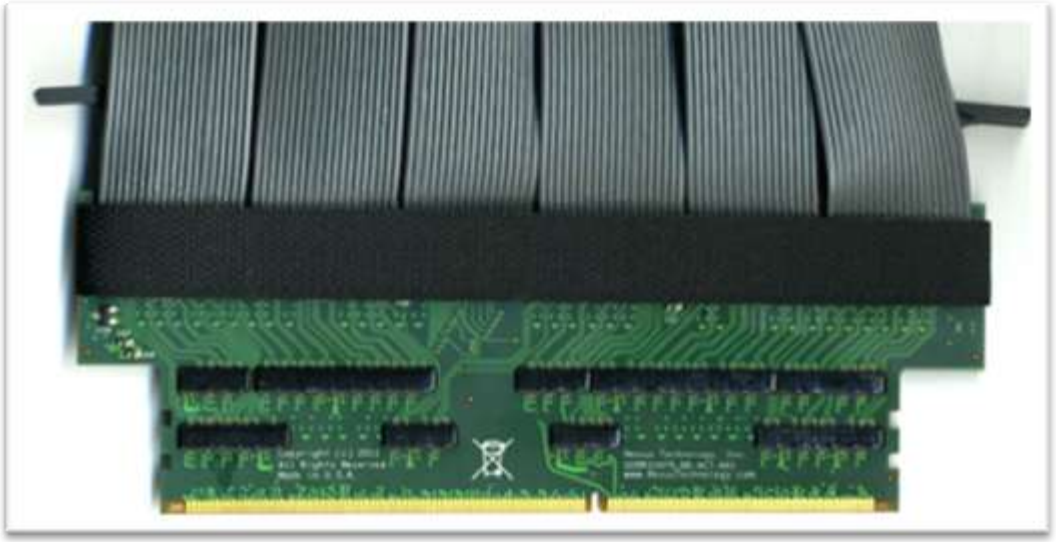
- Protocol / Execution Validation
  - DIMM and SODIMM Interposers
  - Targeted for protocol compliance analysis
  - Automated Setup
  - Use with Nexus Compliance Analysis S/W
  - Compatible with P6960HCD or NEX-PRB1XL

Tektronix®

Introducing New DDR3/4 High Speed Interposer

Next Generation DDR3 Probing Technology

Gain Unprecedented Visibility Into Your DDR3/4 Signal Activity



DIMM Interposer

SODIMM Interposer

Collaborative design combining years of Logic Analyzer acquisition and DDR3/4 probing experience between Tektronix and Nexus Technology

Tektronix®

New DDR3/4 High Speed Interposer

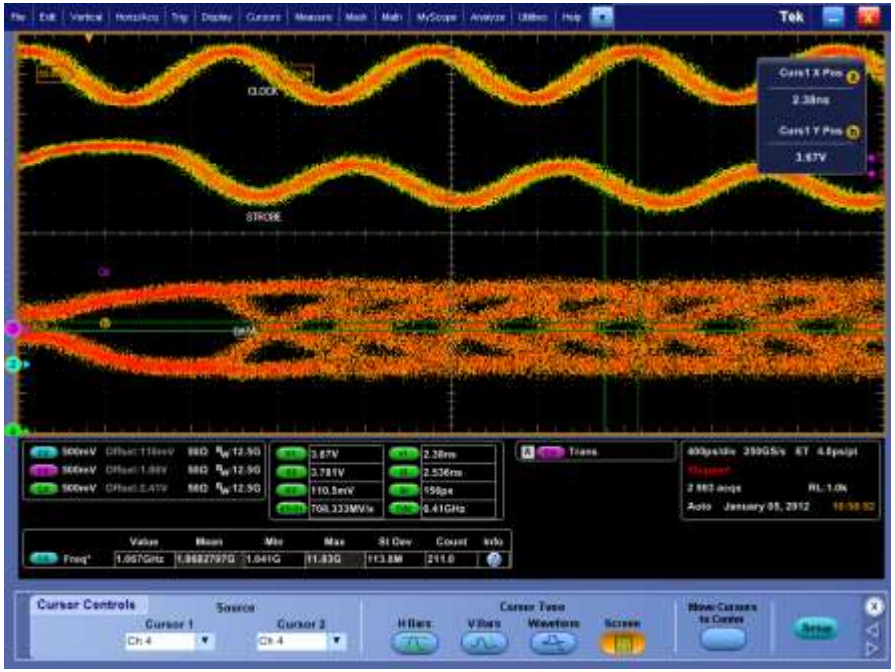
Next Generation DDR3/4 Probing Technology

- Provides significant performance improvements to DDR3 probing
  - Integrates Tektronix ultra-high performance SiGe Hybrid ASIC technology
  - Compensation for platform trace loss on writes
- Improved interposer input impedance (5.2k to 0.73V)
  - Reduces load on target with minimal effect on bus
  - Provides an accurate representation of the signal on the target
- Enables probing DDR3/4 speeds at 2400MT/s and beyond
- Enables probing lower voltage signals on LVDDR3/4
- Interposers compatible with UDIMM, RDIMM, LRDIMM

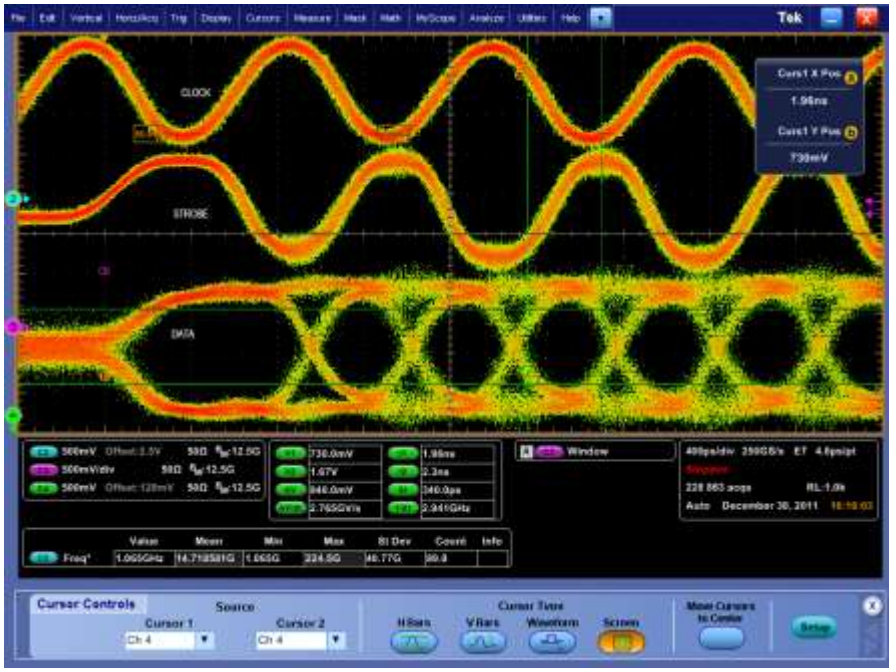
Tektronix®

Scope Screenshots at DDR3 2133MT/s – Writes

OLD Interposer



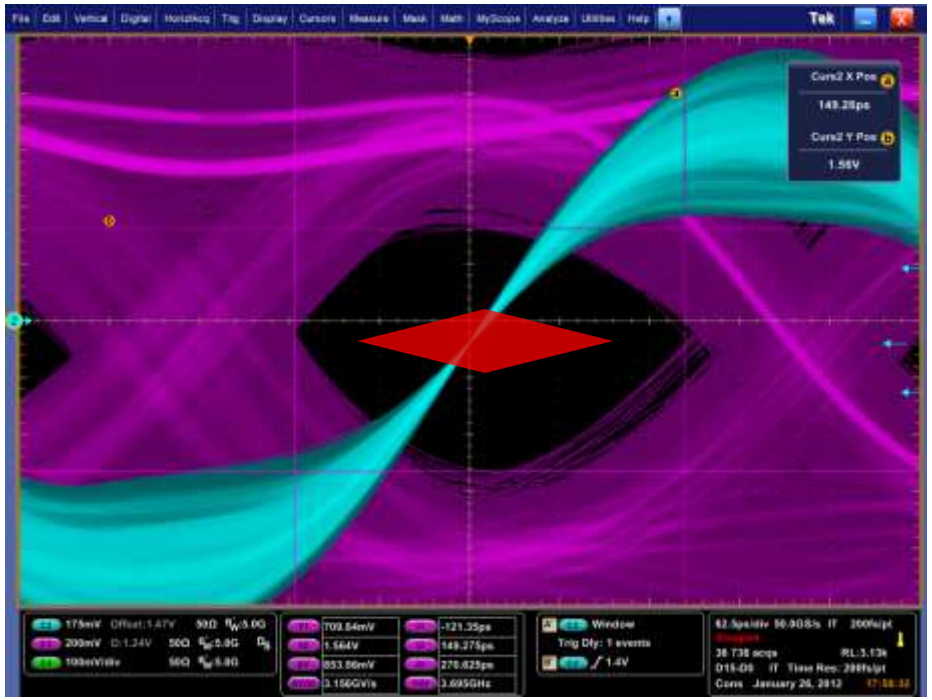
NEW Interposer



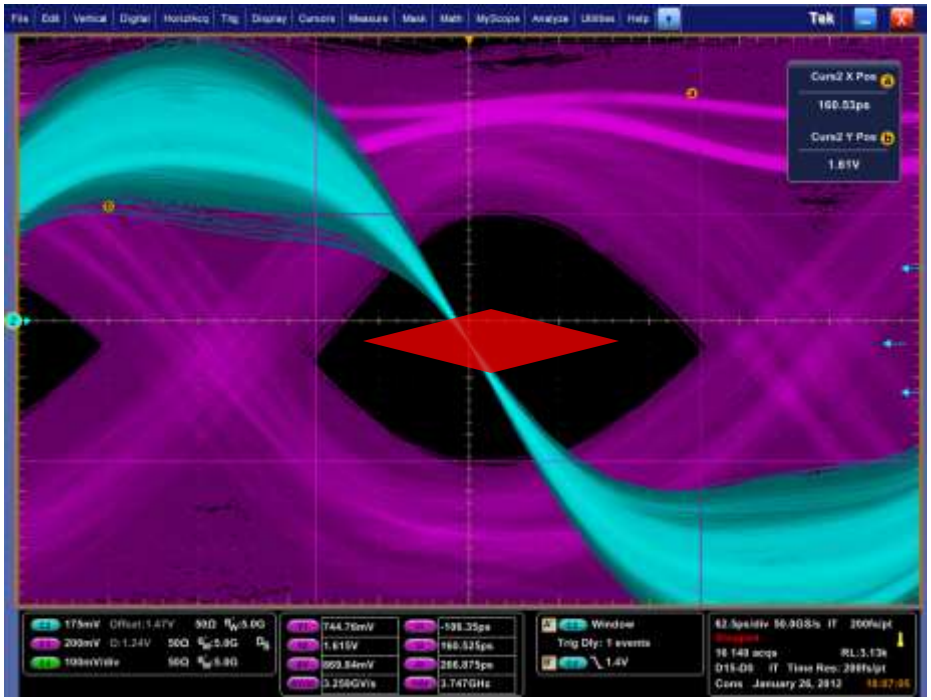
ICI's Tool

Tektronix®

Write Data Eye – DDR3 2400MT/s



Write data eye, rising strobe edge, 853mV x 270ps



Write data eye, falling strobe edge, 869mV x 266ps

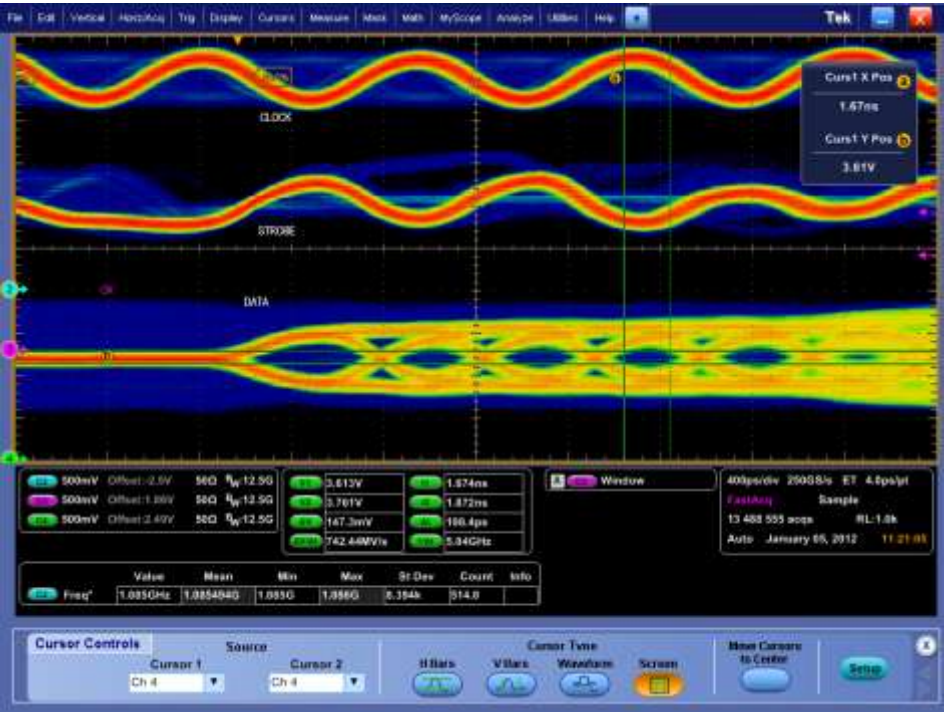
Represents minimum TLA7BB4 eye size, 180ps x 200mV

NOTE: Signals probed via TLA7BB4 analog mux into a 70000C series real time scope.

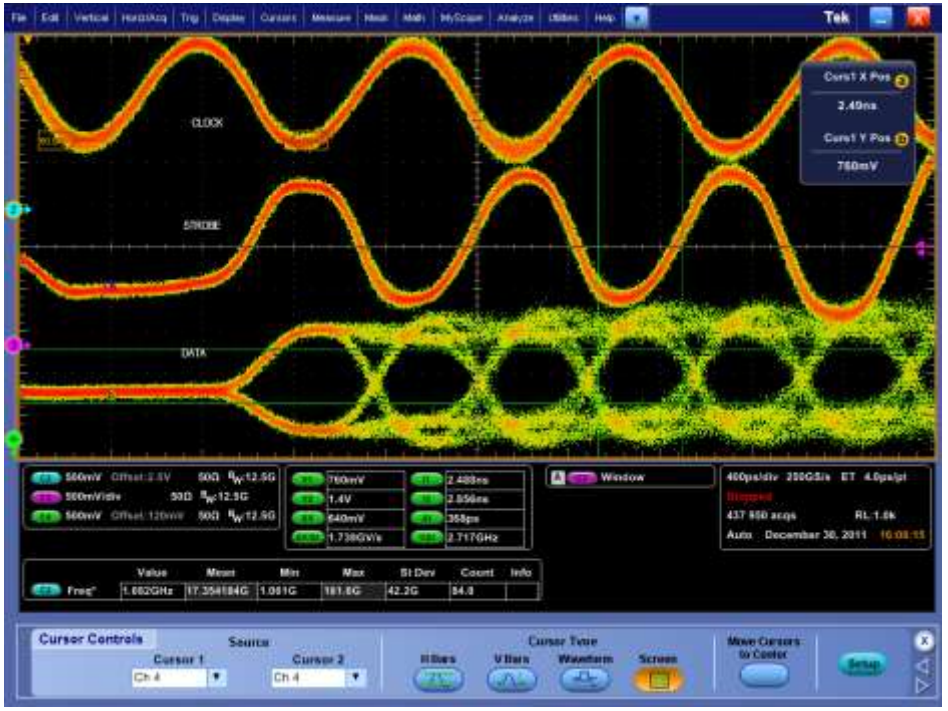
Tektronix®

Scope Screenshots at DDR3 2133MT/s – Reads

OLD Interposer



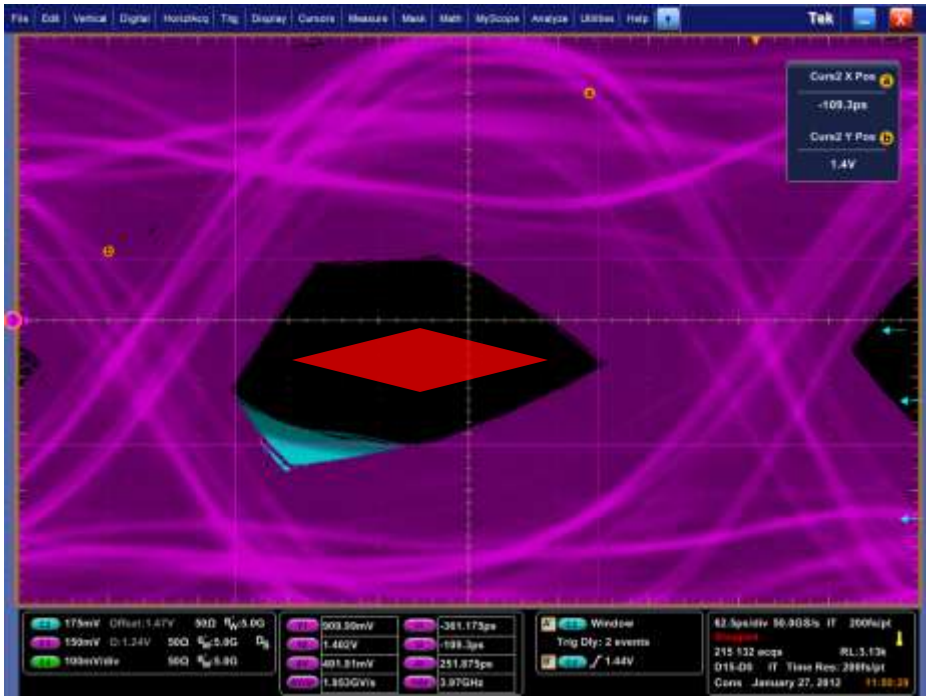
NEW Interposer



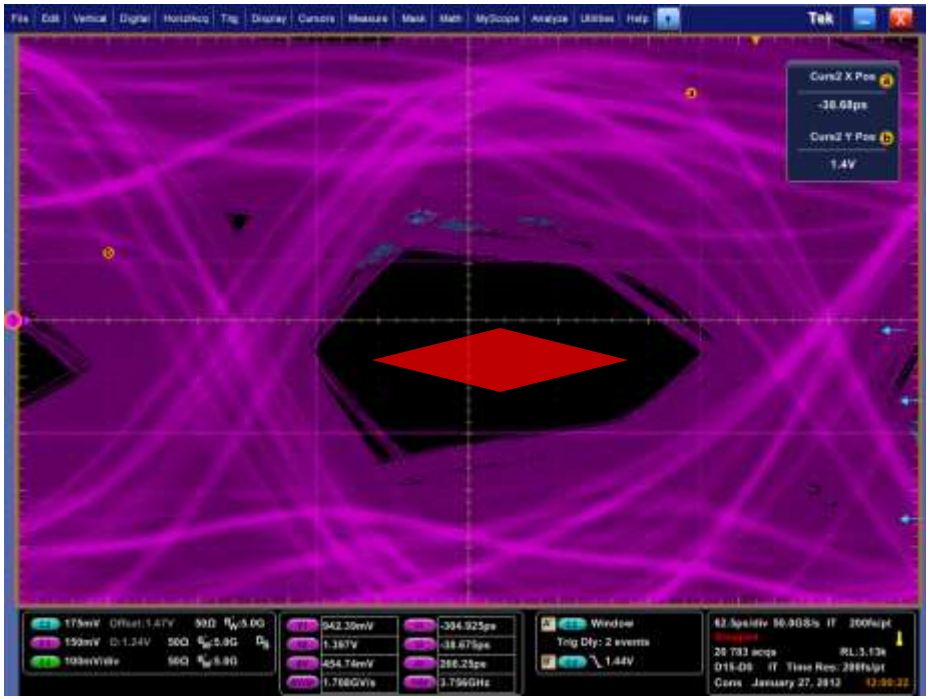
ICI's Tool

Tektronix®

Read Data Eye – DDR3 2400MT/s



Read data eye, rising strobe edge, 492mV x 252ps



Read data eye, falling strobe edge, 454mV x 266ps

Represents minimum 7BB4 eye size, 180ps x 200mV

NOTE: Signals probed via TLA7BB4 analog mux into a 70000C series real time scope.

Tektronix®

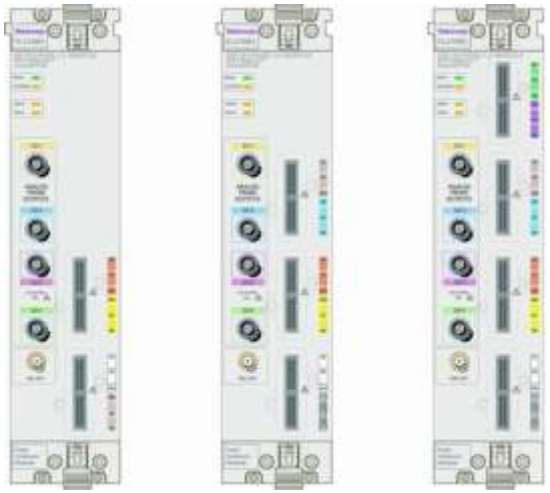
TLA

Tektronix®

TLA7BBx Logic Analyzer Modules

Proven Technology for Analyzing DDR3 SDRAM

DIGITAL CHARACTERISTICS	TLA7BB2	TLA7BB3	TLA7BB4
Digital Channels	68	102	136
High Speed Timing (MagniVu)	50GS/s (20ps)		
Deep Memory Timing	Up to 6.4GS/s		
State Speed	Up to 1.4GHz/3.0Gbps		
Memory Depth	Standard 2Mb, Maximum 64Mb		
Probes	All P68xx and P69xx		
iCapture (Analog Mux)	3 GHz		

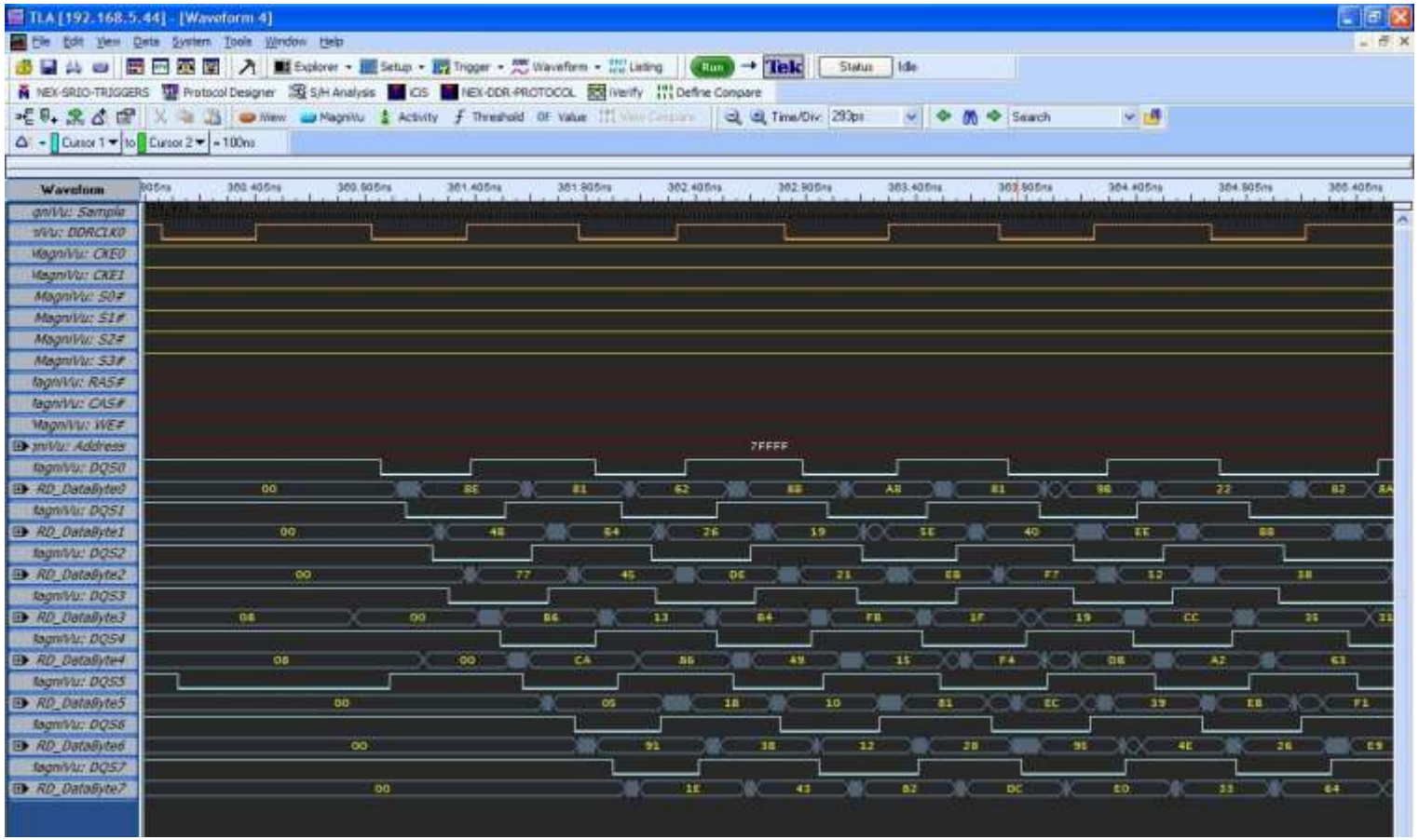


- Preserve investment in TLA7BBx modules
- Enable higher DDR3 speed support with new interposer

Tektronix®

MagniVu 20ps (50 GS/s) High Speed timing

Industry Leading Sampling Resolution



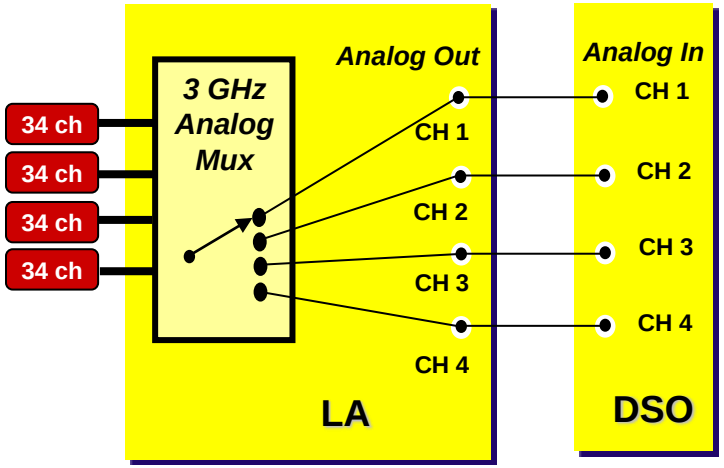
- 50GHz timing analysis on every channel
- Acquired simultaneously and time-correlated with state acquisition data
- Enables acquisition and debug of S/H violations, glitches, and other timing violations
- Reveals fly-by command/address/control bus timing

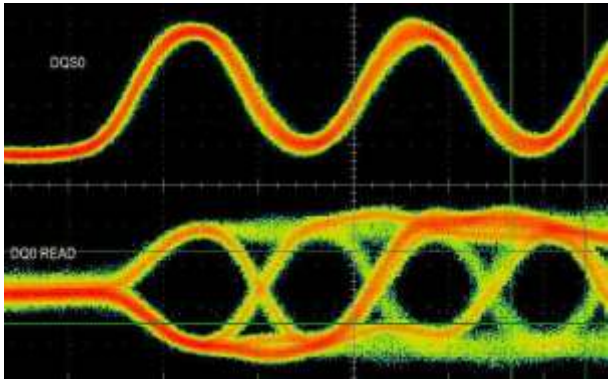
Tektronix®

Analog Mux, iCapture

Enables Signal Integrity Troubleshooting

- Unrivaled capability of the TLA that provides single-point digital and analog probing
- No need to separately probe with a scope, as probing done through the interposer
- Walk through all the signals on your DDR bus in less than 15 minutes to review channel behavior and isolate any potential problems
- Quickly perform detailed analog characterization on signals of interest using a scope component interposer



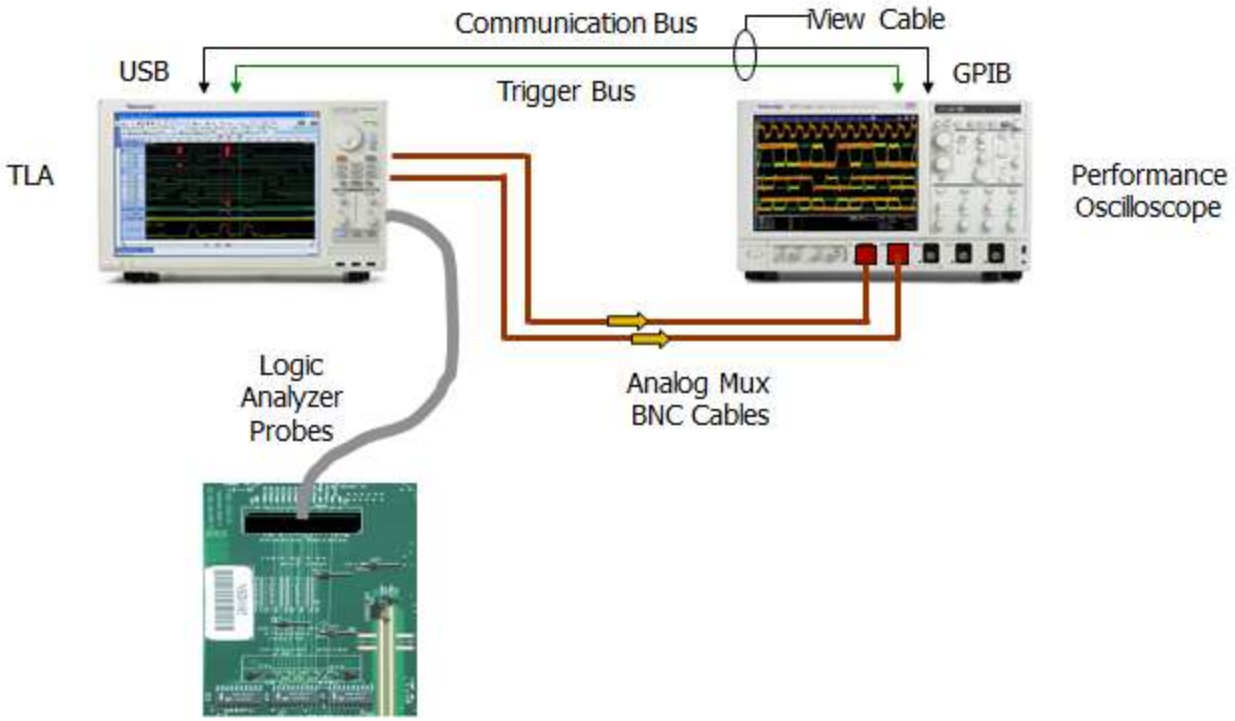


Tektronix®

iView

View Correlated Analog & Digital Characteristics in the Same Display

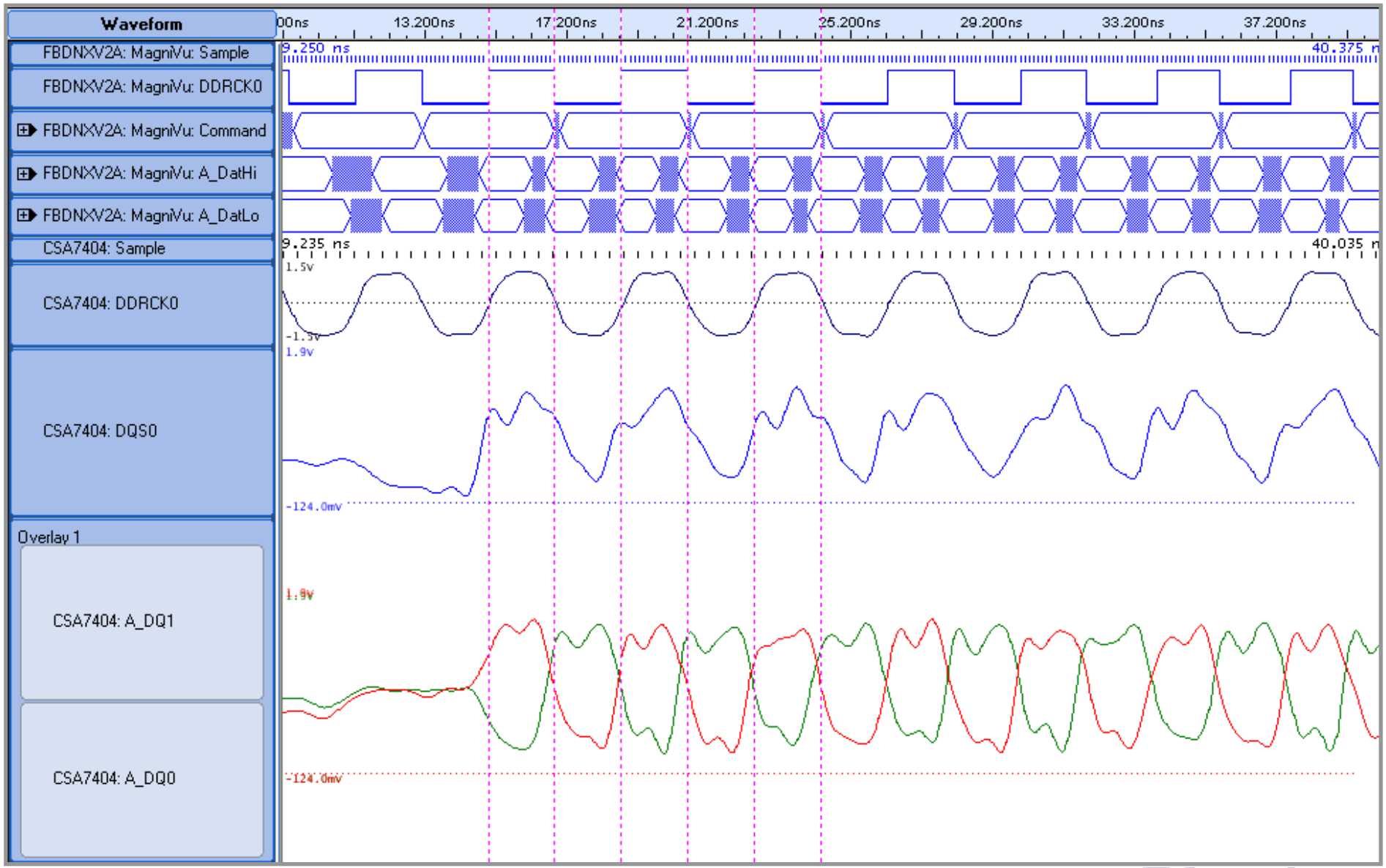
- Unique capability on the TLA that provides time correlated state acquisition, high-speed MagniVu timing acquisition, and analog scope capture results on the same screen.
- Capture events that occur in analog or digital domain through cross triggering
- Enables cross domain analysis by quickly capturing and isolating potential problems



Tektronix®

iView

Correlated High-Speed MagniVu Acquisition & Scope Capture Data Example



Tektronix®

TLA - Single GUI & Frame Supports 1-6 Buses

Note that this image has not been updated to show the new NEX-DDR3-INTR-HS3. Therefore, the TLA probes shown in the image are not needed as the interposer connects directly to the logic analyzer.

TMS160PCIE3
PCI Express 3.0 Software
(requires V5.7+ TLA App SW)

DDR3 SW
R_DDR3D_2B & NEX-DDR-PROTOCOL2

TLA7SA16 x8 Serial Module
(2 req'd for x16)

TLA7BB4 136 ch Parallel Module
(2 req'd for DDR3-1600 & faster)

PCI Express graphics card

DDR3 Slot Interposer Probe
NEX-DDR3INTR-HS3

P67SA16S
x16 Slot Interposer Probe

TLA7016
6-module mainframe
(requires connection to external PC via GbE)

DDR3 Probes
3- P6960HCD
1- NEX-PRB1-XL

Desktop PC motherboard target system

x16 PCI Express 3.0 + DDR3-2133 Solution Shown
(2 additional module slots available for probing additional buses; up to 8 frames supported)

Tektronix®

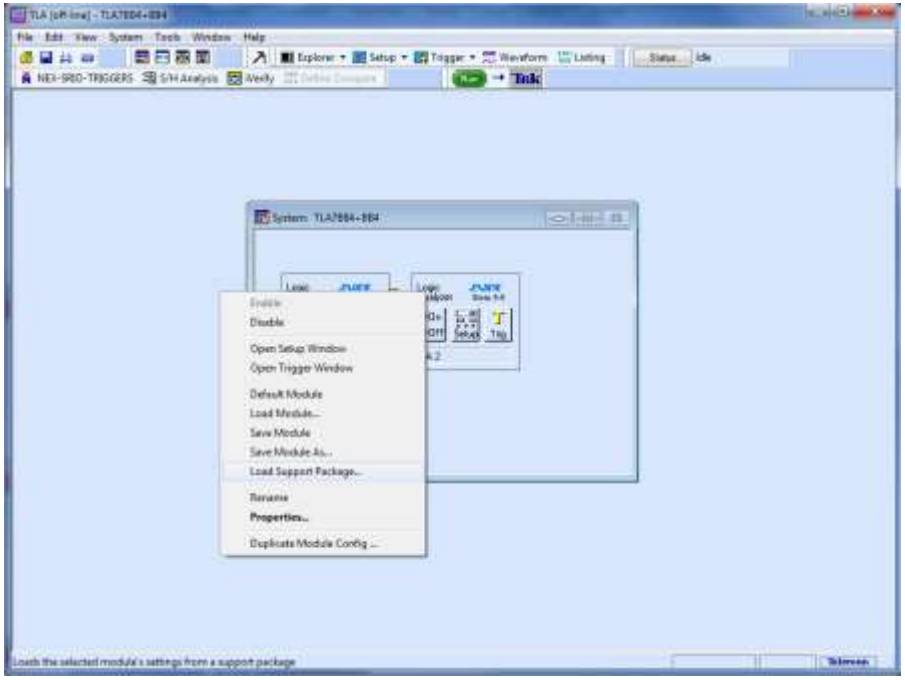
TLA Setup and Analysis

Tektronix®

TLA - Initial Setup

- New Fast & Easy Setup
  - Quick and easy connection
  - Fast software setup
  - No calibration needed for CMD/ADDR/CTRL
  - Automated and graphical DQ data calibration
  - Up and running acquiring ALL data in 15-30 minutes!
  - Identify problem channels at the same time!

- Load the TLA Software
- Load the Support Package
- Ready to Acquire CMD / ADDR / CTRL!



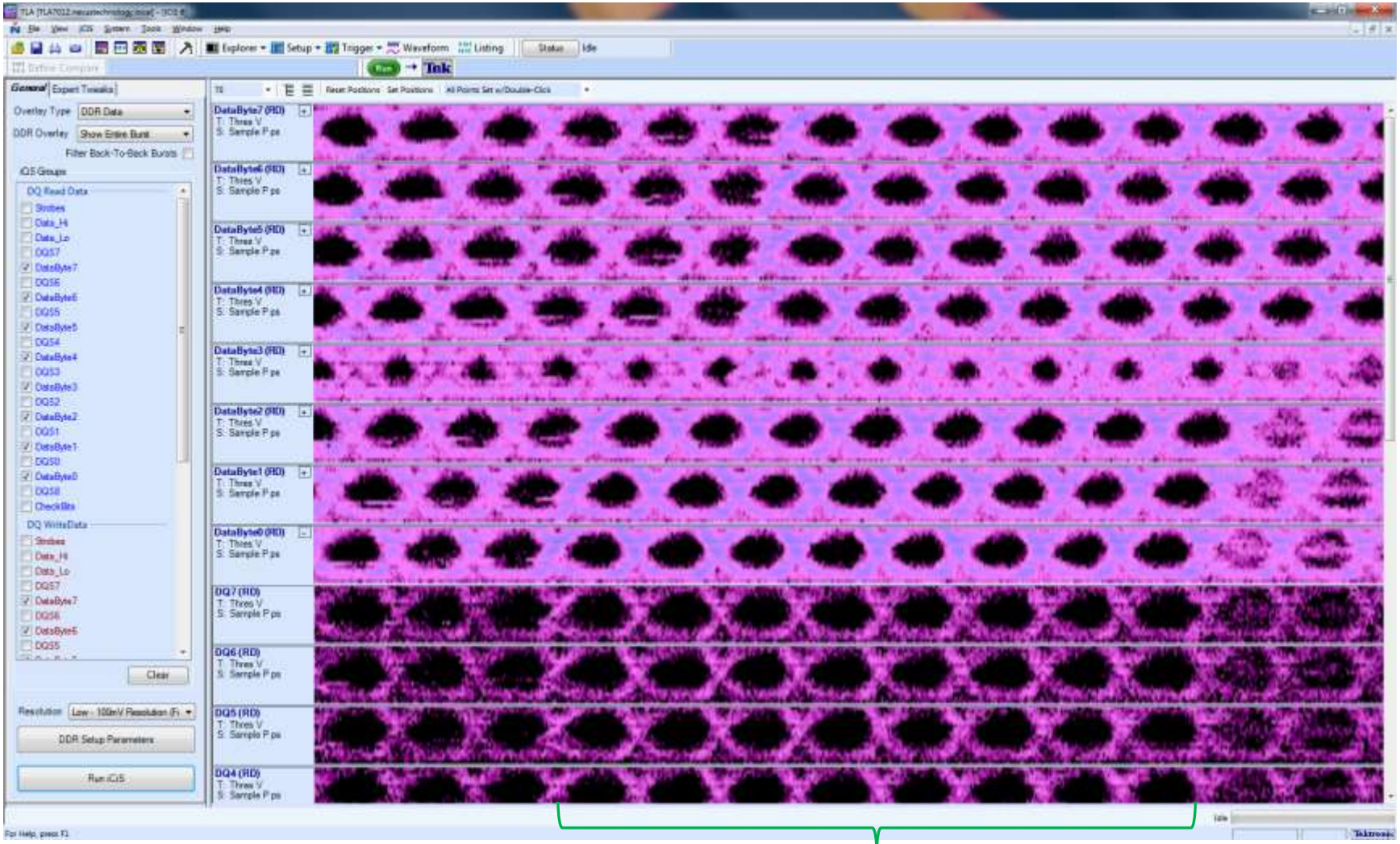
Tektronix®

iCis Overview

- Goals of iCiS
  - Make LA memory tuning easier and quicker
  - Less dependency on platform specific DQ valid regions
  - Less dependency on DQS placement
  - Put more power in the users hands
  - Allow both Vth and sample point to be determined at same time
  - Quick check of signal integrity on the memory bus
  - Allow tuning of address and command signals
  - Simultaneous tuning of Read and Write sample points
  - Double mouse click method to set Vth and sample point for all signals
  - Single tuning tool leveraged for DDR3, DDR4, LPDDR2/3
- User control
  - DDR bus parameters
  - Voltage sweep step size
  - Voltage sweep range
  - Which signals to tune
    - Address bit(s)
    - Command bit(s)
    - DQ-byte lane or individual DQ
      - Read & Write, read only, write only

DDR3 Sweep

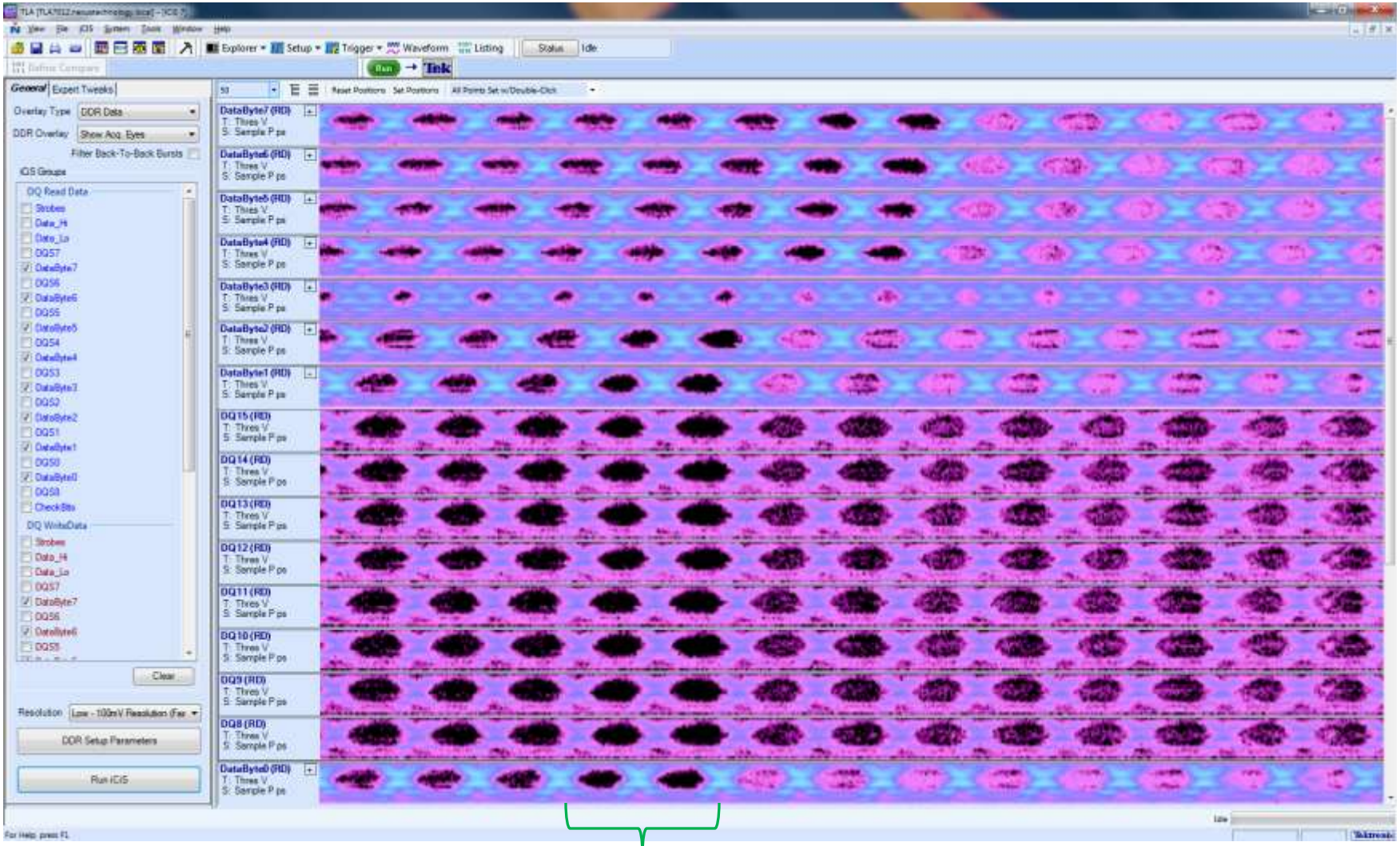
100mV Resolution, Full Burst Mode / 8 DQ Eyes, Reads



Tektronix

DDR3 Sweep

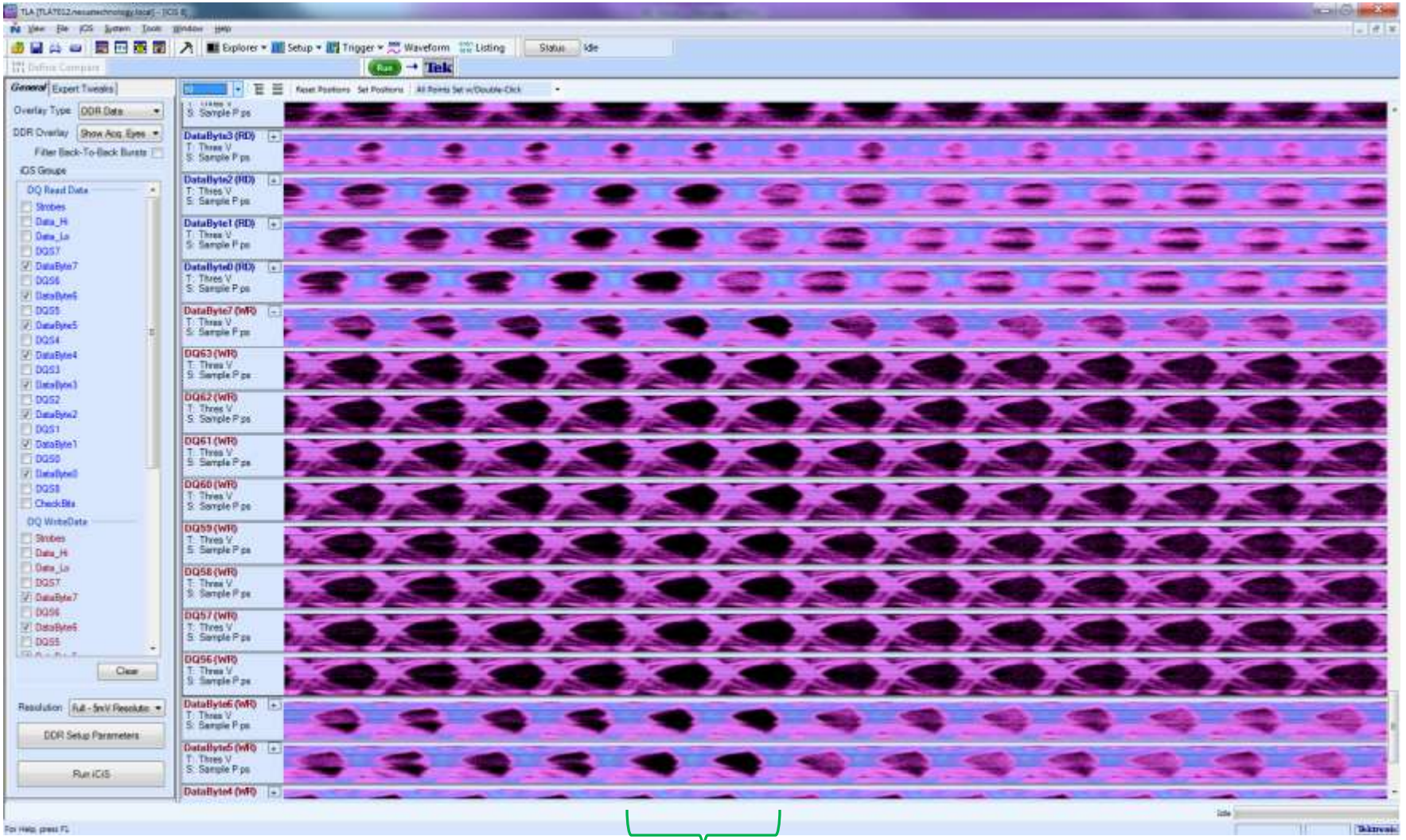
100mV Resolution, Acq Eyes Only Mode / 2 DQ Eyes, Reads



Tektronix®

DDR3 Sweep

100mV Resolution, Acq Eyes Only Mode / 2 DQ Eyes, Writes



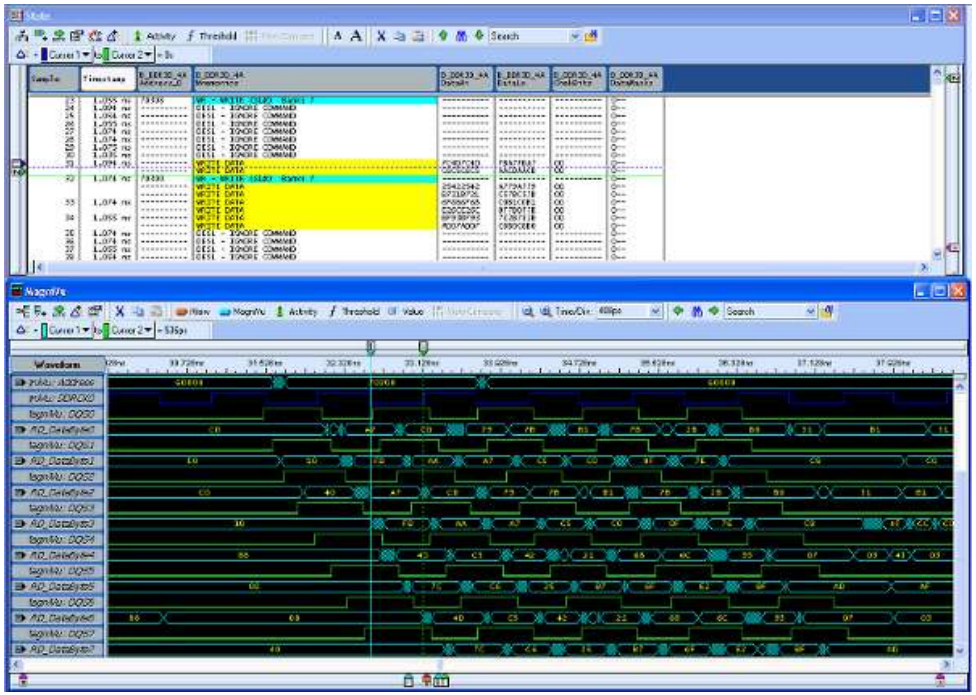
Tektronix®

TLA Data Analysis

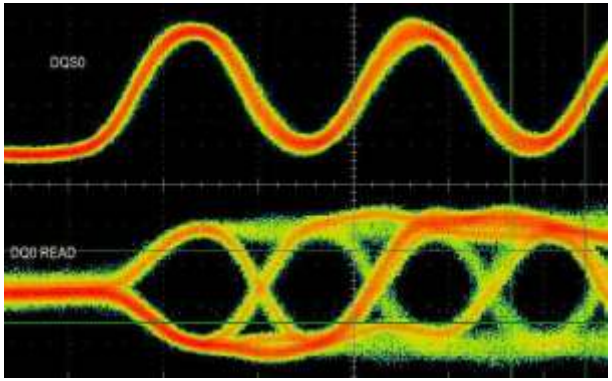
Tektronix®

TLA Data Analysis

- State, MagniVu timing, & analog mux at your fingertips
- Compliance analysis tools
  - Fast setup
  - Comprehensive coverage and violation detection



	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec.
R1 R0	NA	NA	NA	NA	959,880
R2 R1 R0	28,007	10,273,985	2,106,353	6.7	26,250
R2 R1 R0	7,441	878,808	123,227	3.3	7,200
R2 R1 R0	NA	NA	NA	NA	5,625
R2 R1 R0	NA	NA	NA	NA	70,200,000
R2 R1 R0	1,855	8,189,726	945,496	-85.9	13,125
R2 R1 R0	114,121	8,169,101	6,001,631	3.7	110,000
R2 R1 R0	42,969	2,839,180	267,945	14.6	37,500
R2 R1 R0	42,969	2,839,180	267,945	-99.9	70,200,000
R2 R1 R0	18,652	116,172	20,254	42.1	13,125
R2 R1 R0	13,066	316,308	170,537	16.1	11,250
R1 R0	NA	NA	NA	NA	20,625
R0	37,383	326,054	162,946	10.8	33,750



Tektronix®

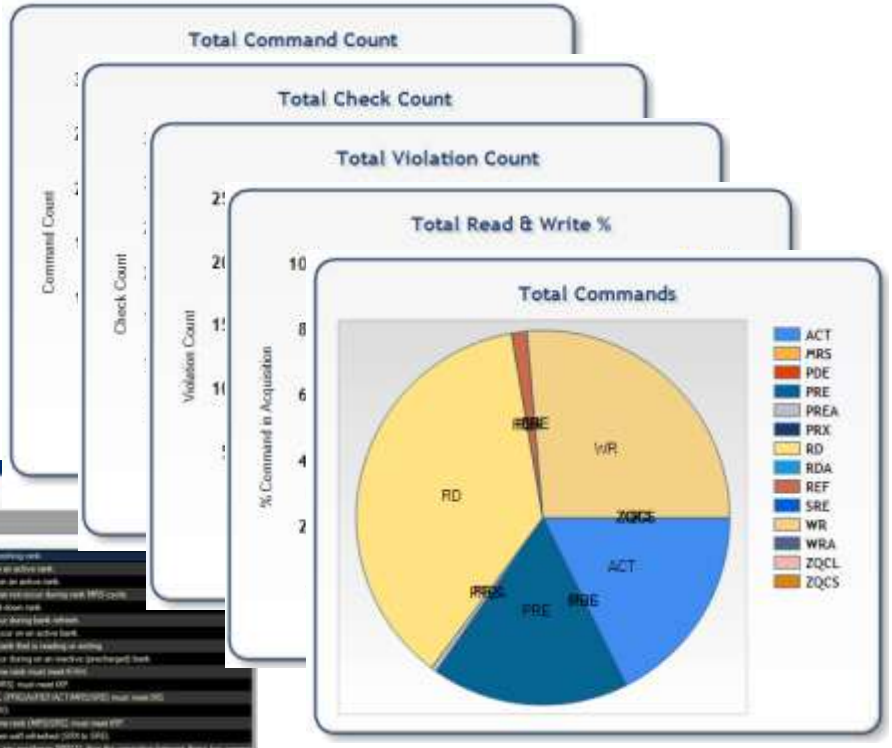
TLA- Example State / MagniVu Display

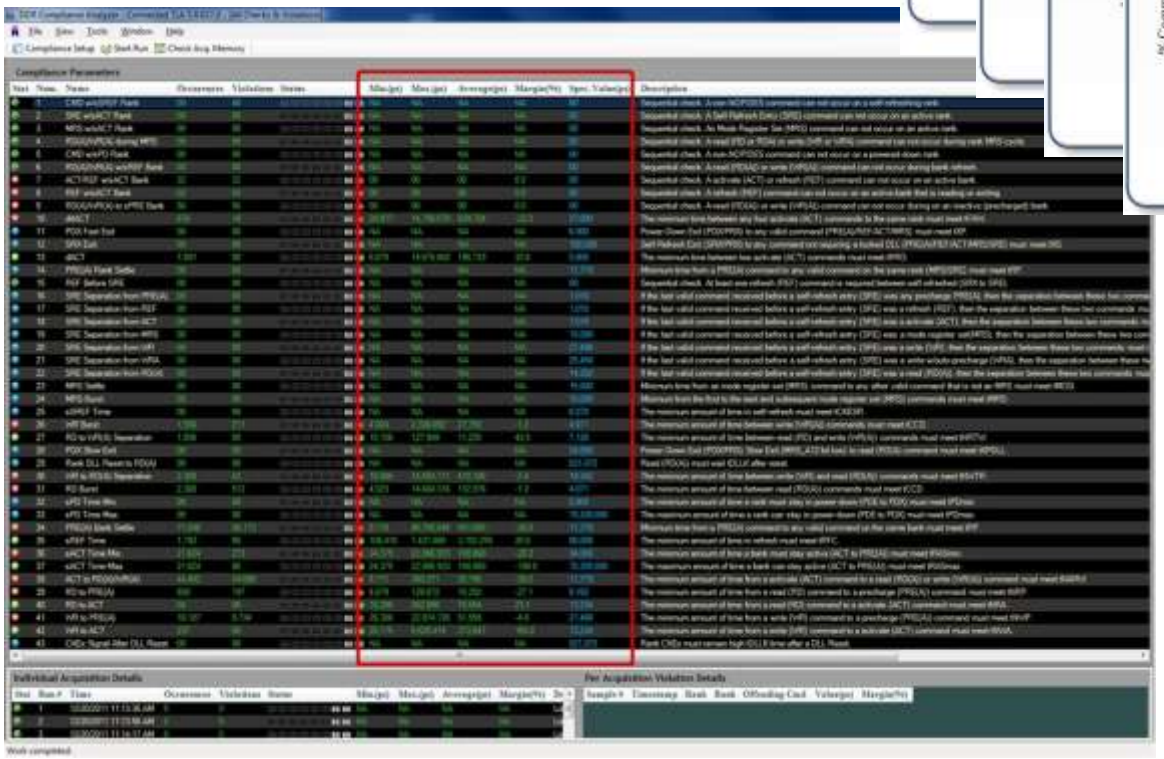
- Command / Address / Control
- DQ Read and Write Data
- Up to 64M-sample state memory
- Simultaneous 50GHz MagniVu timing

Tektronix®

Acquired Data - Compliance Analysis

- Automated acquisition and measurement for analysis of intermittent or infrequent events
- Flexible & easy to configure
- Analysis of over 43 JEDEC compliance parameters
- Powerful in-application graphical and tabular analysis results



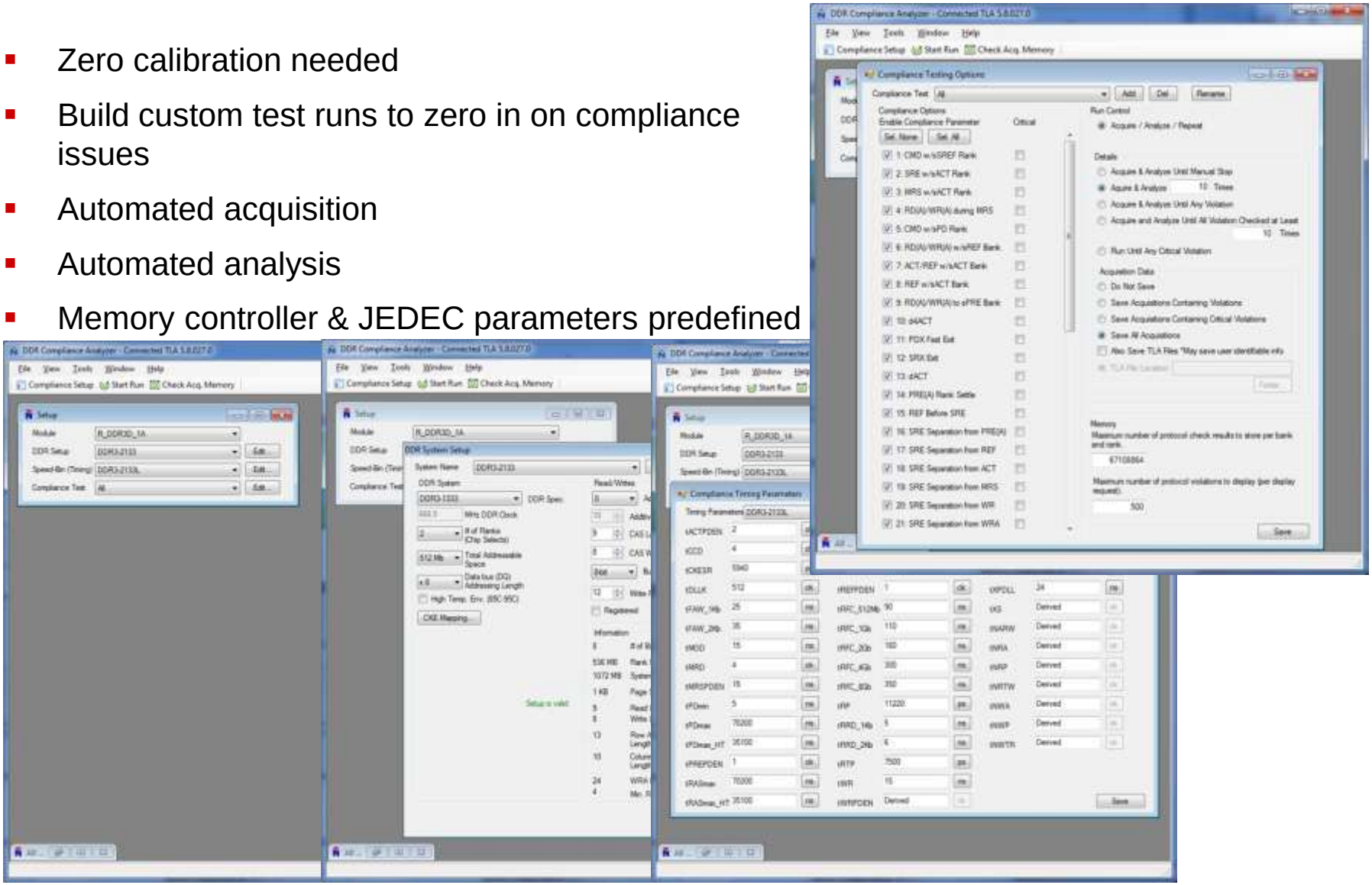


	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec.
R1 R0	NA	NA	NA	NA	959,880
R1 R0	28,007	10,273,985	2,106,353	6.7	26,250
R1 R0	7,441	878,808	123,227	3.3	7,200
R1 R0	NA	NA	NA	NA	5,625
R1 R0	NA	NA	NA	NA	70,200,000
R1 R0	1,855	8,189,726	945,496	-85.9	13,125
R1 R0	114,121	8,169,101	6,001,631	3.7	110,000
R1 R0	42,969	2,839,180	267,945	14.6	37,500
R1 R0	42,969	2,839,180	267,945	-99.9	70,200,000
R1 R0	18,652	116,172	20,254	42.1	13,125
R1 R0	13,066	316,308	170,537	16.1	11,250
R1 R0	NA	NA	NA	NA	20,625
R1 R0	37,383	326,054	162,946	10.8	33,750

Tektronix®

Acquired Data - Compliance Analysis (cont.)

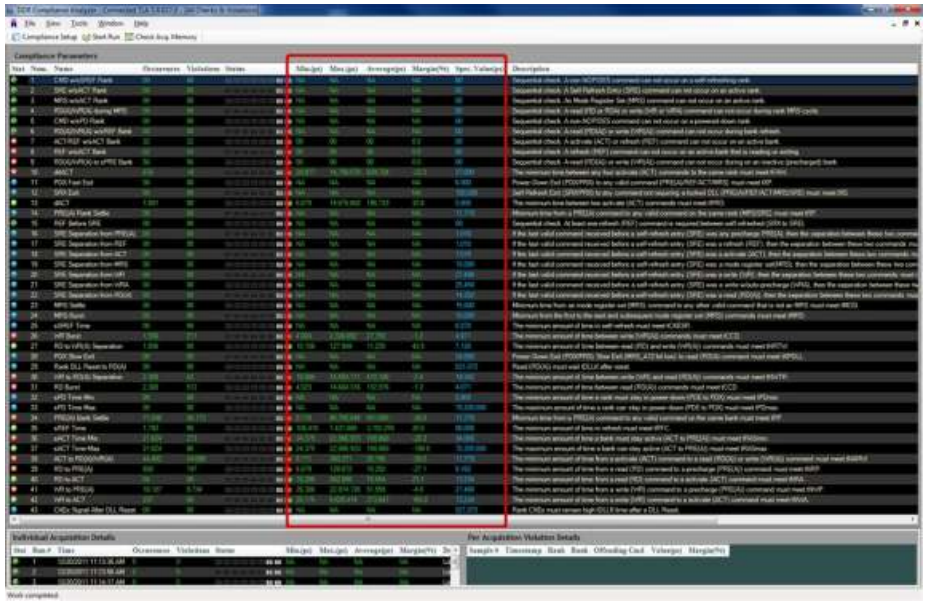
- Zero calibration needed
- Build custom test runs to zero in on compliance issues
- Automated acquisition
- Automated analysis
- Memory controller & JEDEC parameters predefined

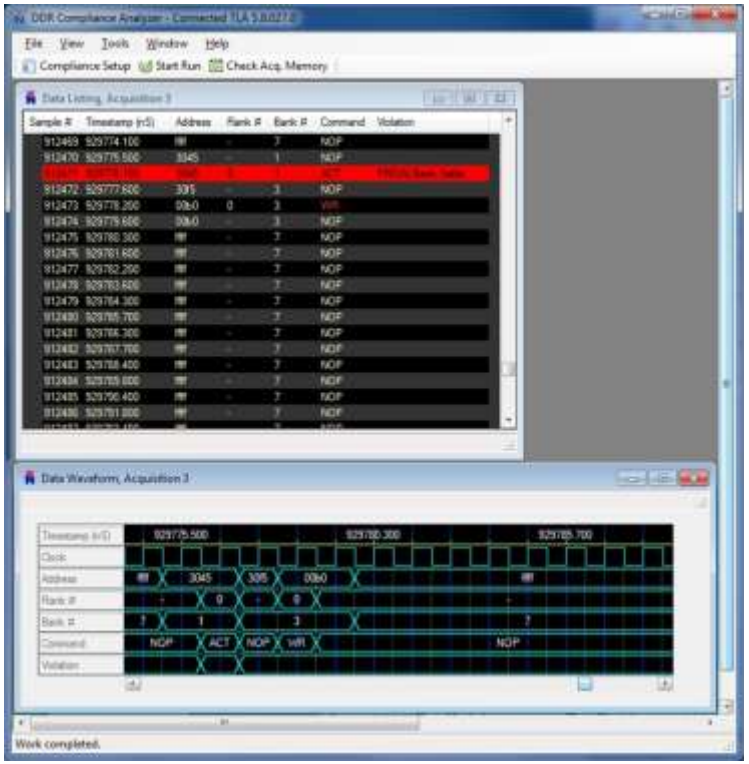


Tektronix®

Acquired Data - Compliance Analysis (cont.)

- Quickly navigate through multiple acquisitions
- Zero in on compliance problems right inside a listing or waveform window
- Listing and waveform windows with compliance violations built in
- Add cursors, jump to violations, see min/max measurements, lock data windows and more!
- Multi-acquisition data management

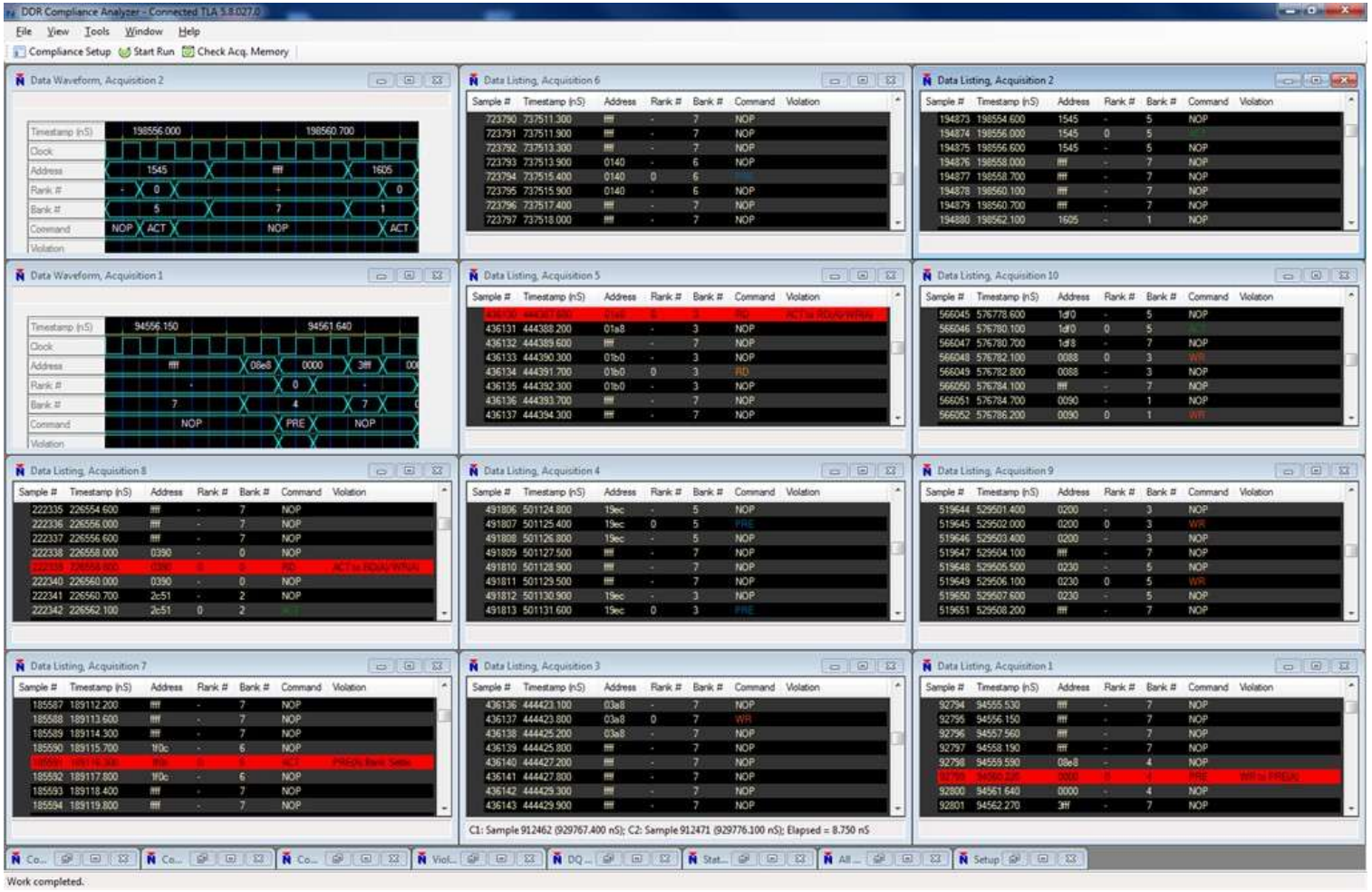




Tektronix®

Acquired Data - Compliance Analysis (cont.)

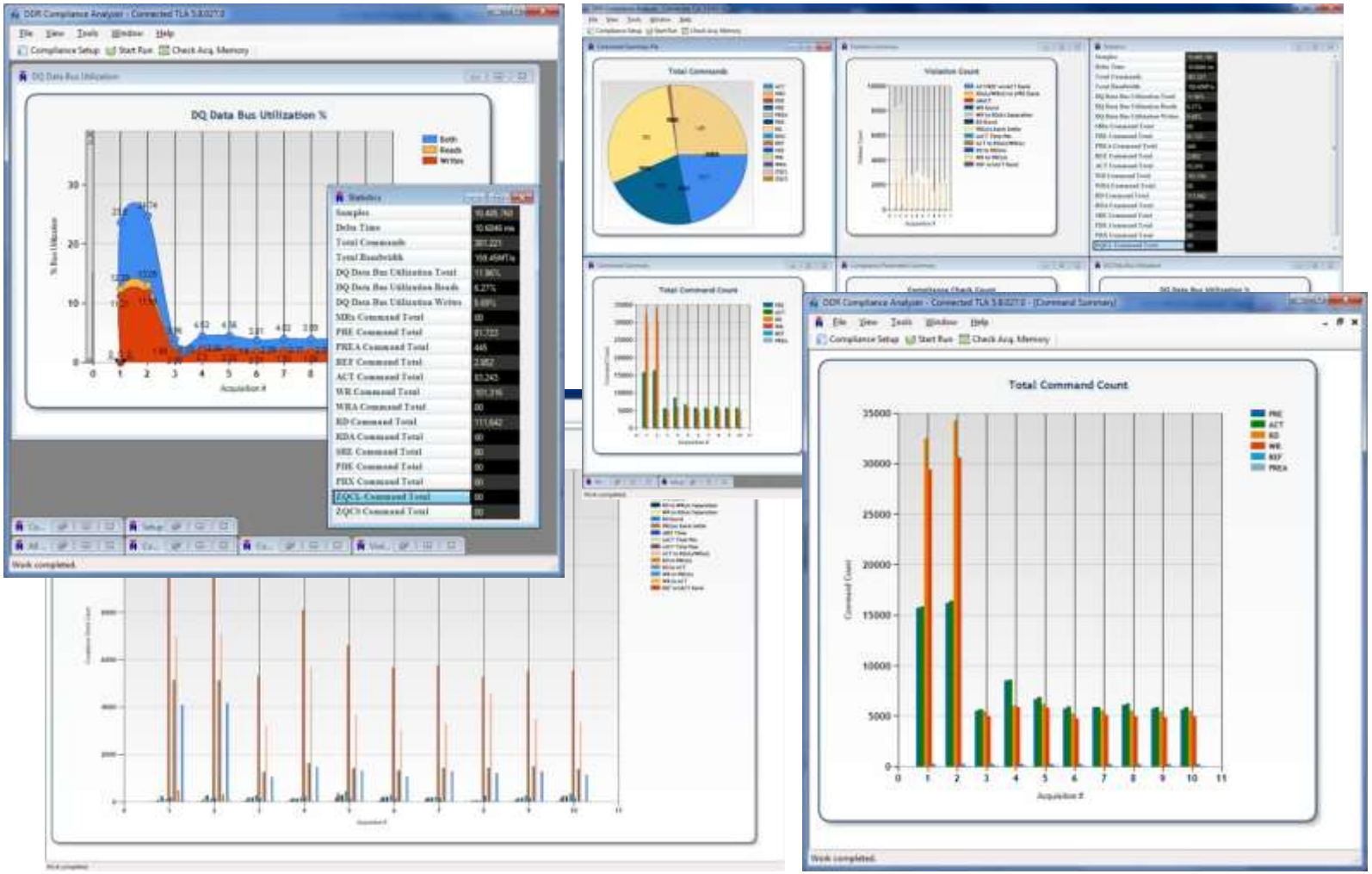
- Example display of multiple acquisitions at once



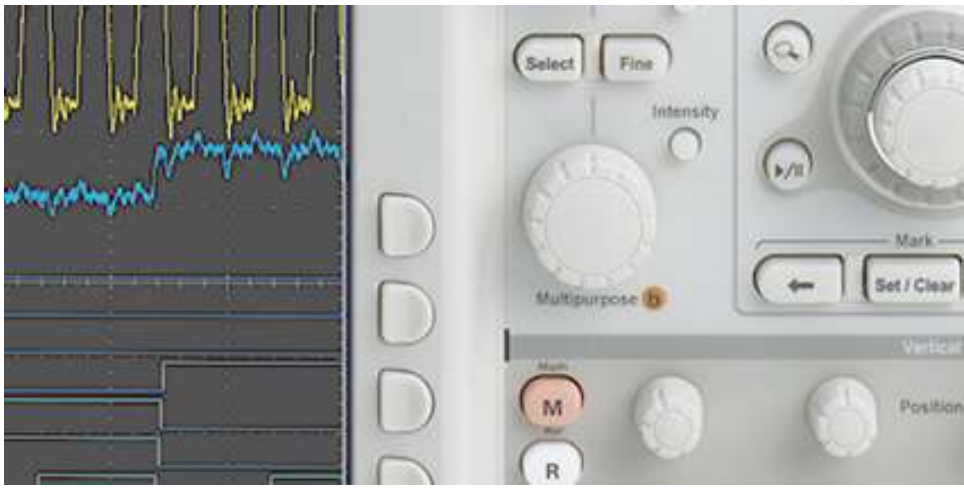
Tektronix®

Acquired Data - Compliance Analysis (cont.)

- Example displays of statistics and charts



Thank You



Tektronix®