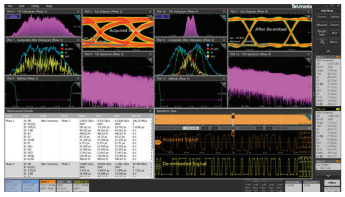
Tektronix®

Testing at the Edge of Innovation

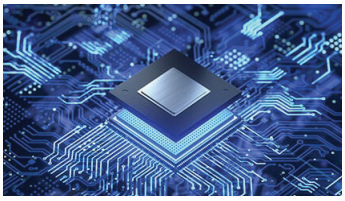
DesignCon 2026 / Visit us at Booth 819

Experience Our Demos



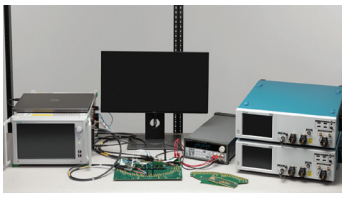
Signal Integrity Modeling and Validation

- De-embed probes, cables, and fixtures to isolate true DUT behavior
- Embed real and hypothetical channel models for what-if system analysis
- Apply Rx equalization directly on the oscilloscope to emulate real-world behavior



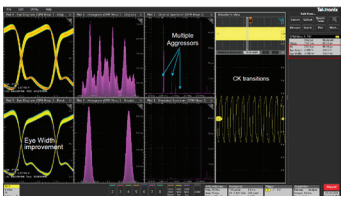
PCI Express 7.0 Electrical Pathfinding at 128 GT/s PAM4

- PAM4 signal integrity analysis at 128 GT/s including eye, jitter, SNDR, and RLM metrics
- Measurement system noise characterization and compensation for higher-confidence results
- Reference receiver equalization with channel embed and de-embed for early SerDes insight



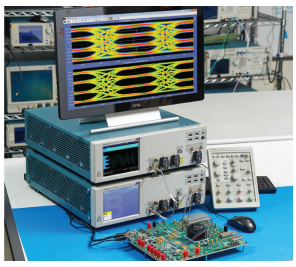
PCI Express 6.0 Compliance Validation at 64 GT/s

- Automated Tx and Rx compliance testing aligned with the PCI Express 6.0 CEM specification
- Wizard-based receiver calibration and transmitter testing for repeatable 64 GT/s PAM4 measurements
- Seamless transition from compliance testing to deep debugging with integrated analysis



Power Integrity Validation for AI Servers

- High-current, nanosecond-level transient measurements for AI-class PDNs
- Direct stability assessment of large-signal, time-variant power delivery networks
- Ultra-low impedance validation under real-world load conditions

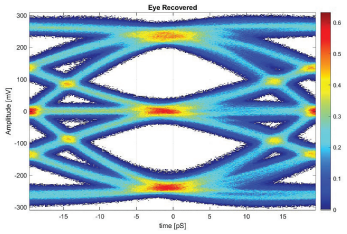


DDR5 Transmitter and Receiver Compliance

- Unified DDR5 Tx and Rx compliance workflow accelerates bring-up
- Automated testing with flexible debugging for rapid root-cause analysis
- Advanced analysis delivers deeper insight into signal behavior

(continued on back)

Tektronix®



USB4 Version 2.0 Compliance at 40 Gbps

- Automated compliance testing for USB4 v2 PAM3 signaling at 40 Gbps per lane
- Parallel acquisition and analysis increases test throughput
- Low intrinsic jitter for improved measurement accuracy

Energy-Efficient Bidirectional DC Power System Validation

- Triple-channel bidirectional DC testing with three fully isolated outputs
- Built-in PV simulation and MPP tracking for realistic energy workflows
- Energy recovery during sink operation to reduce lab power and heat

Hear From Tektronix Experts

Tuesday, February 24 4:45 PM | Ballroom C	Panel: The Case of the Closing Eyes: 200G/Lane (and pp) AI Hardware Dogfight Is Still Escalating — The Impact on You, Ethernet, NVLink, OIF, UEC, and IB
Wednesday, February 25 12:15 PM | Ballroom A	Adaptive Scope Noise Removal: A Practical Trade-Off Between Measurement Bias and Variation
Wednesday, February 25 12:15 PM | Great America Ballroom J	PCI Express 7.0 Electrical Pathfinding Updates
Wednesday, February 25 3:00 PM | Ballroom C	An Experimental Study of PCIe Transmitter Equalization Preset Measurement Methods for 64 and 128 GT/s PAM4 Signaling
Wednesday, February 25 3:15 PM | Chiphead Theater	Stability and More: Going Beyond Bode Stability Assessment
Thursday, February 26 12:15 PM | Ballroom A	Uncertainty Looms Large: Improving the Accuracy of Step Load Testing
Thursday, February 26 2:40 PM | Chiphead Theater	AI-Driven Emulation of Power Supply Ripple via HSS Jitter Analysis and TIE-Based Source Isolation for PI-SI Co-Design