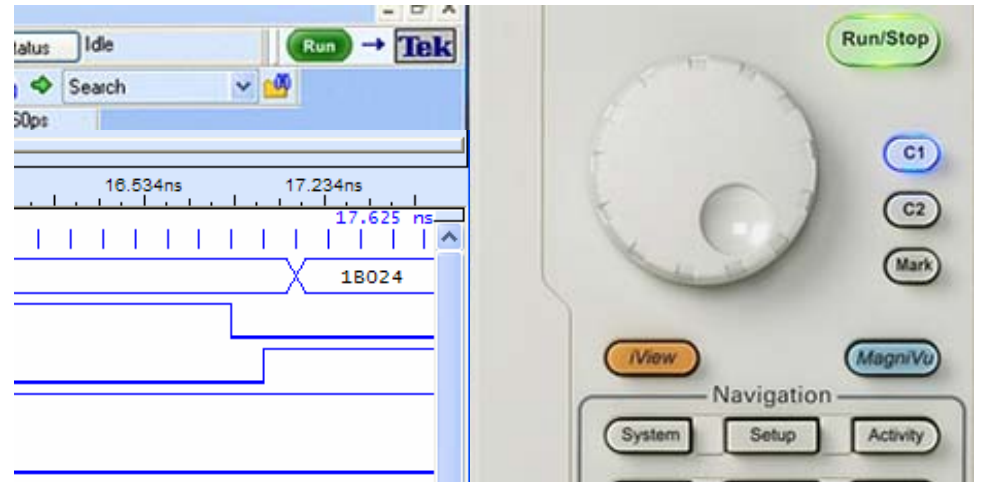


Mastering Validation and Debug of Digital Systems



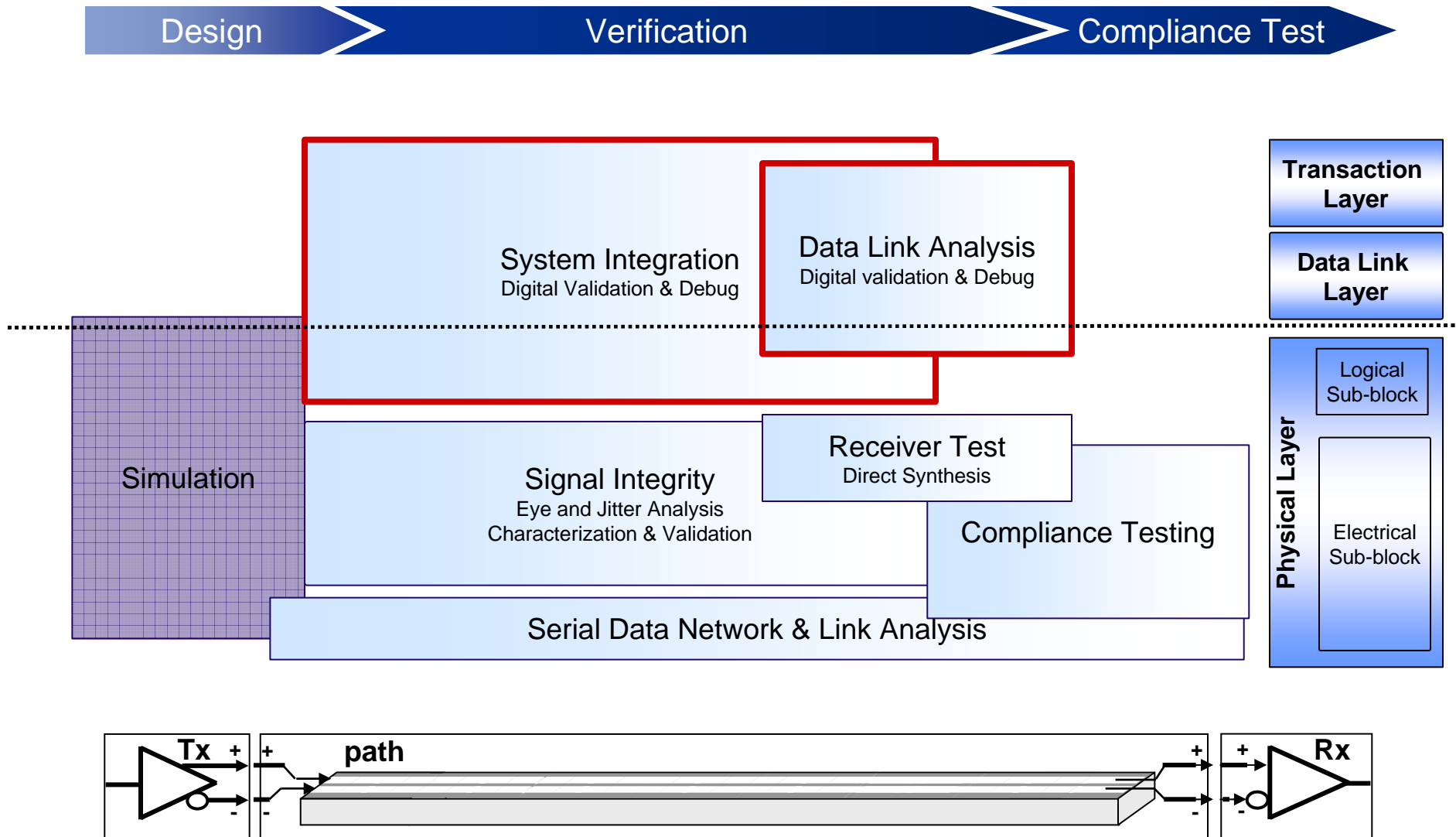
Tektronix®



Agenda

- High Speed Serial Data Test Challenges
- PCI Express® Digital Validation and Debug
- DDR Memory Validation and Debug
 - Probing
 - Acquisition
 - Analysis
- DDR2 Demo
- Summary

High Speed Serial Test Challenges





High Speed Serial Test Challenges

- Giga-bit data rates require higher performance instruments
 - Decreased timing budget: Faster timing resolution
 - Transmission line effects: Low loading
- Industry focus on reducing power consumption
 - Link width down configure for power savings and upconfigure when additional bandwidth is required
 - Electrical Idle Entry and Exit for power savings, design ease, and robustness
- Industry standards are defining stringent measurement and analysis requirements

Digital Validation & Debug

Data Access - Probing

- Requires reliable physical connectivity with minimal loading
 - Mid Bus Probes
 - Interposers
 - Instrument DIMMs
 - Direct probing to circuit board
- Requires maximum signal integrity



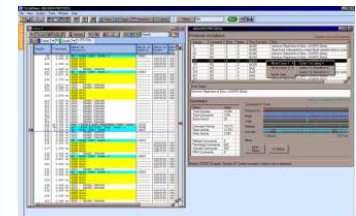
Data Acquisition

- Timing resolution high enough for thorough debugging
- Trigger state machine flexible enough to trigger only on relevant events
- Channel count scalable and high enough to capture all required signals
- Scalable and time correlated system for cross bus analysis



Data Analysis

- Verify and debug memory system operation
 - Data valid windows
 - Read/Write data operation
 - DDR commands and mode register initialization
- Quickly and easily identify protocol violations
- Analyze link training, power management, and advanced packet level decoding



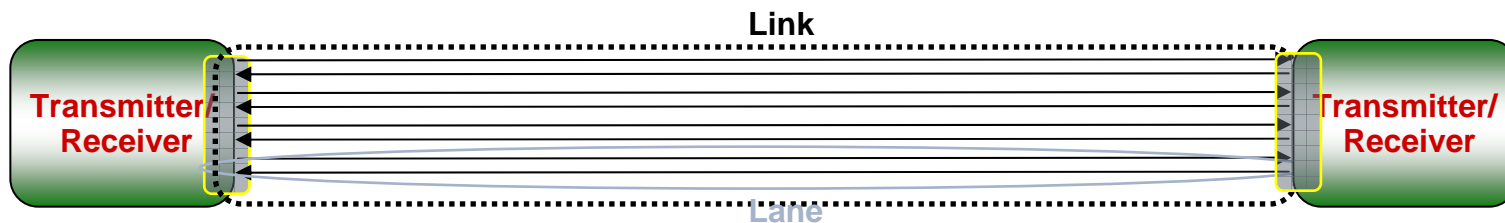


Agenda

- High Speed Serial Data Test Challenges
- PCI Express Digital Validation and Debug
- DDR Memory Validation and Debug
 - Probing
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Primary PCIe 2.0 Digital Debug Challenges

Power management and link training continue to be the most difficult challenges



- Power Up & Link Initialization
 - Multi-lane systems (x1, x4, x8, x16)
 - PCIe 1.0 <-> PCIe 2.0 systems compatibility: Speed negotiation from 2.5Gb/s to 5.0Gb/s and 5.0Gb/s to 2.5Gb/s
 - Dynamic speed & link width changes
- Active State Power Management
 - Power Management: Electrical Idle Entry and Exit for power savings,
 - Dynamic link width and link speed changes depending on data transfer volume requirements
- A PCIe Bus Remains Part of a Total System
 - Critical cross bus dependencies increase with speed
 - Time-correlated visibility across multiple buses
 - Signal access across the entire system

PCI Express 2.0 – Power Management

ASPM Active State Power Management

Need for Lower Power Consumption and Longer Battery Life

- Power management
 - Less energy consumption
 - Longer battery lifetime
 - Government regulations: EnergyStar®

- PCIe 2.0 power management implementations
 - Dynamic link width changes depending on current data transfer volume.
 - Dynamic link speed changes depending on data transfer requirements (2.5Gb/s <-> 5Gb/s)
 - Short term idle states of one or both direction of a link (L0s, L1)
 - L0s: autonomous Idle-state of a link for a very short time
 - L1: short term Idle-state initiated by a higher level protocol

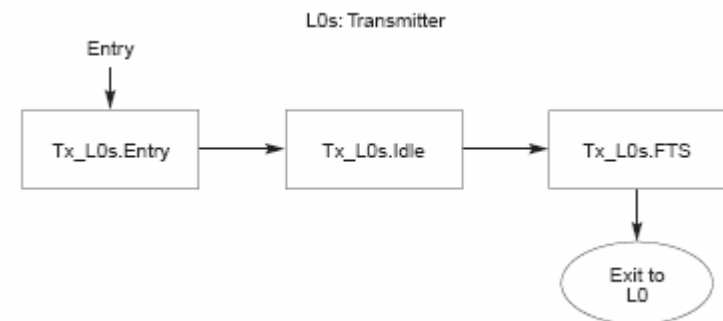
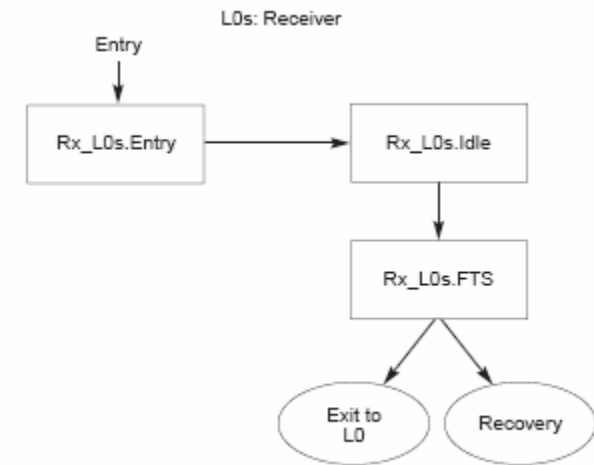
When a lane is in Idle,
no Power is consumed
by that lane

PCI Express 2.0 – Power Management

ASPM Active State Power Management

Power Management Sequence (L0s-example)

- L0s Power management is being used more frequently in PCI Express designs
- L0s: autonomous Idle-state of one or both direction of a link for a very short time
 - Efficiency depends on how fast a system can enter and exit the L0s state.
 - L0s Exit Latency is measured by the number of “Fast Training Set’s” (FTS) packets required by the system, to exit the L0s state.
 - Number of FTS = 1...255 (~16nS...4μS)
- Past designs have exhibited failures during ASPM events, thus visibility of these events is critical to the debug engineer

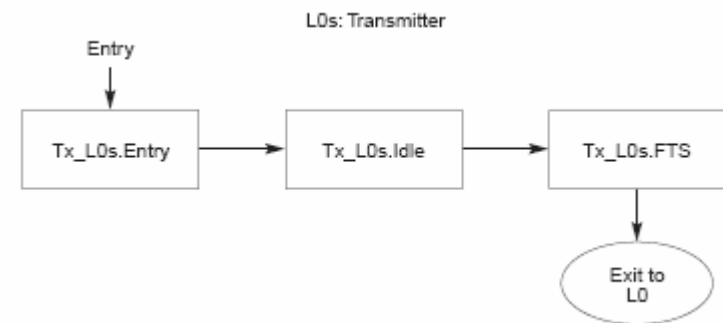
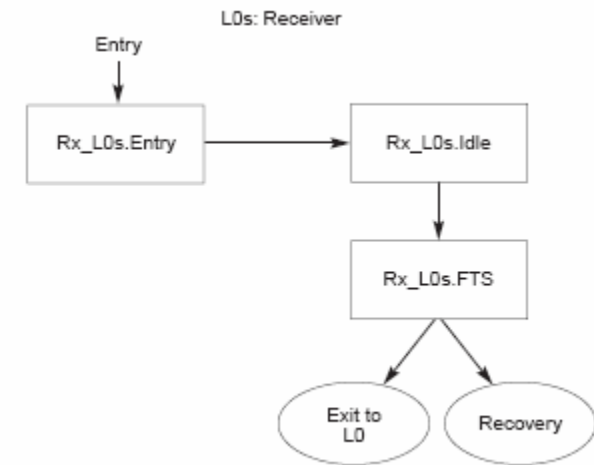


PCI Express 2.0 – Power Management

ASPM Active State Power Management

How to Debug:

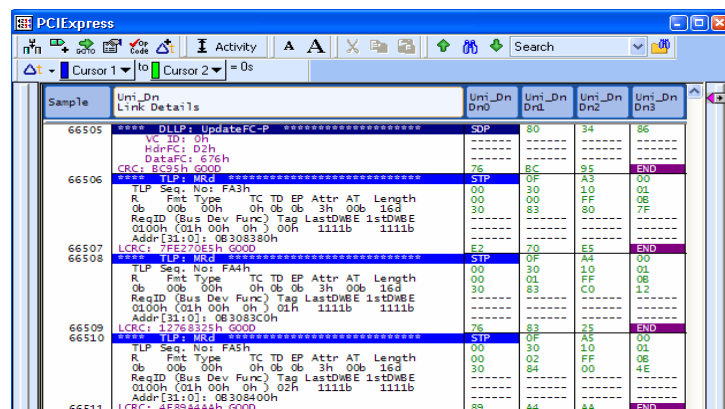
- Detect and quickly re-sync as the bus employs ASPM in order to acquire all packets as the link exits L0s
- Tektronix supports maximum visibility of these transitions
 - Typical sync within 12 FTS packets for both 2.5Gb and 5Gb



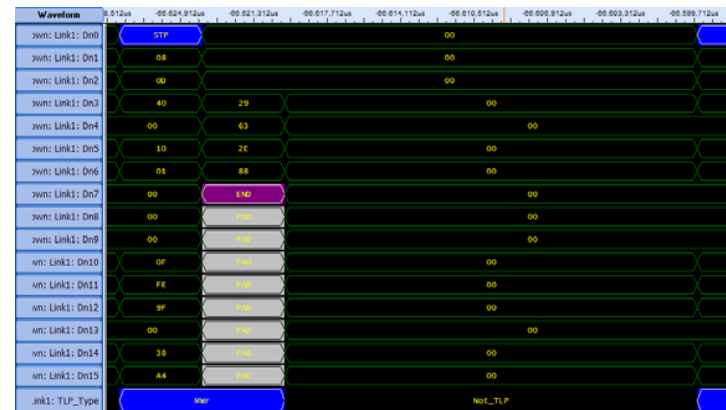
Multiple Analysis Options

Packet Decode and Multi-bus Correlation

- Packet Decode and Transaction support in the Listing Window
 - Complete decode of PCI Express Packets
 - Symbolic decode on a lane by lane basis
 - View Tx and Rx in a common listing window or lock listing windows for transaction support
- Quick insight to system problems- View all system buses in the waveform window
 - View all system buses correlated to the TLA common system timestamp
 - Correlate analog and digital waveforms



Sample	Uni_Dn	Link Details	Uni_Dn	Uni_Dn	Uni_Dn
66505	----	**** DLLP: UpdateFC-P ****	SDP	30	34
66506	----	VC ID: 0h	----	----	----
66506	----	Header: 02h	----	----	----
66506	----	DataFC: 676h	----	----	----
66506	----	CRCL: 8635h GOOD	----	----	----
66506	----	**** TLP Seq. No: FA3h ****	SDP	30	34
66506	----	R: First Type TC TD EP Attr AT Length	00	30	10
66506	----	Ob 00b 00h 0h 0b 3h 00b 16d	00	00	01
66506	----	RegID (Bus Dev Func) Tag LastDWE 1stDWE	30	83	80
66506	----	0100h 01h 00h 0h 01h 1111b 1111b	----	----	----
66506	----	Addr[31:0]: 0E308380h	----	----	----
66506	----	LCRC: 7FE270Esh GOOD	----	----	----
66506	----	**** TLP Seq. No: FA4h ****	SDP	30	34
66506	----	R: First Type TC TD EP Attr AT Length	00	30	10
66506	----	Ob 00b 00h 0h 0b 3h 00b 16d	00	01	01
66506	----	RegID (Bus Dev Func) Tag LastDWE 1stDWE	30	83	80
66506	----	0100h 01h 00h 0h 01h 1111b 1111b	----	----	----
66506	----	Addr[31:0]: 0E3083C0h	----	----	----
66506	----	LCRC: 1776832sh GOOD	----	----	----
66506	----	**** TLP Seq. No: FA5h ****	SDP	30	34
66506	----	R: First Type TC TD EP Attr AT Length	00	30	10
66506	----	Ob 00b 00h 0h 0b 3h 00b 16d	00	02	01
66506	----	RegID (Bus Dev Func) Tag LastDWE 1stDWE	30	84	00
66506	----	0100h 01h 00h 0h 02h 1111b 1111b	----	----	----
66506	----	Addr[31:0]: 0E308400h	----	----	----
66506	----	LCRC: 4E894AAh GOOD	----	----	----



Correlate Cross Bus Data

Sample	Timestamp	Down Link1 Uni_Dn Link Details	Up Link1 Uni_Up Link Details
Down: Link1 15139	7.375 ns	**** TLP: MWr **** TLP Seq. No:546h R Fmt Type TC TD EP Attr AT Length 0b 10b 00h 0h 0b 0b 1h 00b 16d ReqID (Bus Dev Func) Tag LastDWB 1 0000h (00h 00h 0h) 00h 1111b 1111b Addr[31:0]: 15325EC0h +00h: 000055E5h 000055E5h 000055E5h 000055E5h +10h: 000055E5h 000055E5h 000055E5h 000055E5h +20h: 000055E5h 000055E5h 000055E5h 000055E5h +30h: 000055E5h 000055E5h 000055E5h 000055E5h LCRC: FB083C7Ah GOOD	**** TLP: MWr **** TLP Seq. No:546h R Fmt Type TC TD EP Attr AT Length 0b 10b 00h 0h 0b 0b 1h 00b 16d ReqID (Bus Dev Func) Tag LastDWB 1 0000h (00h 00h 0h) 00h 1111b 1111b Addr[31:0]: 15325EC0h +00h: 000055E5h 000055E5h 000055E5h 000055E5h +10h: 000055E5h 000055E5h 000055E5h 000055E5h +20h: 000055E5h 000055E5h 000055E5h 000055E5h +30h: 000055E5h 000055E5h 000055E5h 000055E5h LCRC: FB083C7Ah GOOD
Down: Link1 15140	2.025 ns		
Down: Link1 15141	1.975 ns		
Down: Link1 15142	2.000 ns		
Down: Link1 15143	1.975 ns		
Down: Link1 15144	2.025 ns		
Up: Link1 11650	12.550 ns		
Up: Link1 11651	22.000 ns		
Up: Link1 11652	11.975 ns		
Down: Link1 15145	9.400 ns	**** TLP: MWr **** TLP Seq. No:547h R Fmt Type TC TD EP Attr AT Length 0b 10b 00h 0h 0b 0b 1h 00b 16d ReqID (Bus Dev Func) Tag LastDWB 1 0000h (00h 00h 0h) 00h 1111b 1111b Addr[31:0]: DBE4B040h +40h: 000055E5h 000055E5h 000055E5h 000055E5h +50h: 000055E5h 000055E5h 000055E5h 000055E5h +60h: 000055E5h 000055E5h 000055E5h 000055E5h +70h: 000055E5h 000055E5h 000055E5h 000055E5h LCRC: 148DC2EEh GOOD	**** TLP: MWr **** TLP Seq. No:547h R Fmt Type TC TD EP Attr AT Length 0b 10b 00h 0h 0b 0b 1h 00b 16d ReqID (Bus Dev Func) Tag LastDWB 1 0000h (00h 00h 0h) 00h 1111b 1111b Addr[31:0]: DBE4B040h +40h: 000055E5h 000055E5h 000055E5h 000055E5h +50h: 000055E5h 000055E5h 000055E5h 000055E5h +60h: 000055E5h 000055E5h 000055E5h 000055E5h +70h: 000055E5h 000055E5h 000055E5h 000055E5h LCRC: 148DC2EEh GOOD
Down: Link1 15146	1.975 ns		
Down: Link1 15147	2.000 ns		
Down: Link1 15148	1.975 ns		
Down: Link1 15149	2.025 ns		
Down: Link1 15150	1.975 ns		

Sample	IA3	IA32G11 A[31:00]	IA32G11 Request	IA32G1 Snoop	IA32G1 Response
13423	--	--	--	DEFER	DEFER
13424	--	--	--	CLEAN	DEFER
13425	00	159307D8	MEM_READ_8	--	NORM_D
13426	--	--	--	--	--
13427	00	15325EC0	MEM_WRITE_8	--	--
13428	00	0E74D080	MEM_WRITE_64	--	--
13429	--	--	--	CLEAN	--
13430	00	00250000	DEFER_REPLY	--	--
13431	00	00260000	DEFER_REPLY	CLEAN	NO_DATA
13432	--	--	--	CLEAN	NO_DATA
13433	00	16E65580	MEM_RD_INV_64	--	--
13434	--	--	--	CLEAN	--
13435	--	--	--	--	00000223
13436	00	16E656C0	MEM_READ_64	--	--
13437	--	--	--	HIT	--
13438	00	00200000	DEFER_REPLY	--	NO_DATA
13439	--	--	--	--	00286AE0
13440	--	--	--	--	00286AE0
13441	--	--	--	--	00286AE0
13442	--	--	--	--	00286AE0
13443	--	--	--	--	00286AE0
13444	--	--	--	--	00286AE0
13445	--	--	--	--	00286AE0
13446	--	--	--	--	00286AE0
13447	--	--	--	--	00286AE0
13448	--	--	--	--	00286AE0
13449	--	--	--	--	00286AE0
13450	--	--	--	--	00286AE0

Graphics Bus
response
TLP MWr to
15325EC0h

FSB issues a
Memory Write
to Address
15325EC0h

Complete System Digital Debug & Design Verification PCI Express 2.0 Logic Analyzer Solution

■ Performance

- Auto detect 2.5Gb/s to 5.0Gb/s data rate change
- Dynamically track link width Upconfigure/Downconfigure
- World class ASPM support - L0s and L1 sync time

■ Visibility

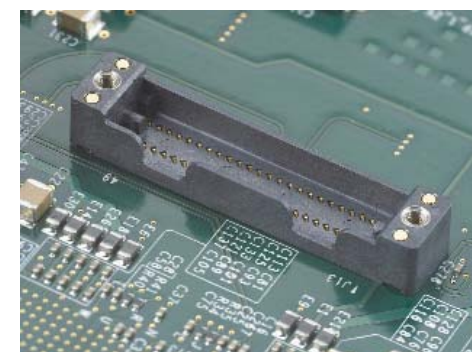
- Correlate all system buses to the common TLA timestamp
- Import scope waveforms for analog / digital correlation
- See the data you want with HW and SW filtering 32M 8b/10b symbols per lane acquisition depth

■ Flexibility

- Backwards compatible to PCIe 1.x (data rate/footprint)
- Acquire x1, x4, and x8 links in a single TLA7S16 module
- Acquire x1 and x4 links in a single TLA7S08

■ Best Probing Solution

- Mid-bus or Interposer probing options at 5.0Gb/s
- Minimal impact on probed signals
- No need for multiple probes to support different routings
- Easy access to SUTs with 6 foot cable length
- C-springs are integrated with the retention mechanism



Tektronix



Agenda

- High Speed Serial Data Test Challenges
- PCI Express Digital Validation and Debug
- DDR Memory Validation and Debug
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 - Acquisition
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Memory Systems

Gigabit Data Rates

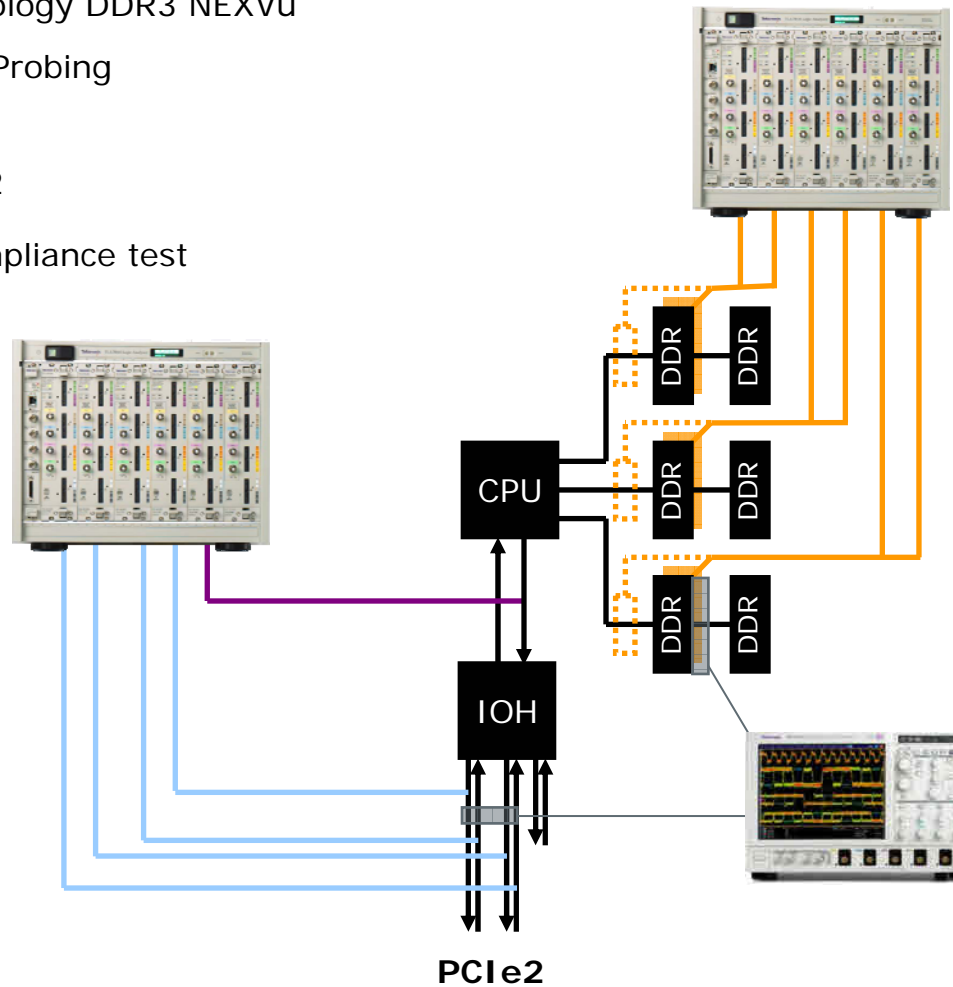
SDRAM Standards			
SDRAM	Data Rate MT/S	Clock MHz	VDD V
DDR-266	266	133	2.5
DDR-333	333	166	2.5
DDR-400	400	200	2.5
DDR2-400	400	200	1.8
DDR2-533	533	267	1.8
DDR2-667	667	334	1.8
DDR2-800	800	400	1.8
DDR2-1066	1066	533	1.8
DDR3-800	800	400	1.5
DDR3-1066	1066	533	1.5
DDR3-1333	1333	667	1.5
DDR3-1600	1600	800	1.5
DDR3-1867	1867	933	1.5

- DDR/2/3 SDRAM
 - Driven by increasing computer performance
 - Performance doubles every ~ 3 years
- Complex parallel bus
 - Fast clock speeds
 - Small data valid eyes
 - Small timing margins
 - Crosstalk, impedance & jitter
- Memory system verification is critical to reliable product operation

Tektronix Platform Validation System

Complete System Visibility with Time Correlation

- Nexus Technology DDR3 NEXVu
- - - - - DDR3 Direct Probing
- QPI Bus
- PCI Express 2
- Electrical compliance test



TLA7000 Series Logic Analyzer with Nexus Memory Supports

DPO/DSA70000 Series Oscilloscope

DDR/2/3 Verification & Debug

Memory protocols & data

- Operations, Commands & Data
 - Memory initialization
 - Mode registers settings
 - Read & write data
 - Command sequences & timing
 - Data valid windows
 - Export read & write data to other tools
 - Time correlated memory operations
 - With oscilloscope waveforms
 - Other buses (QPI, FSB, PCI-Express 2, etc)



TLA7000 Series Logic Analyzers
with Nexus Memory Supports

**Capture errors that cannot be captured or
be seen by other logic analyzers with 20 ps high resolution timing**

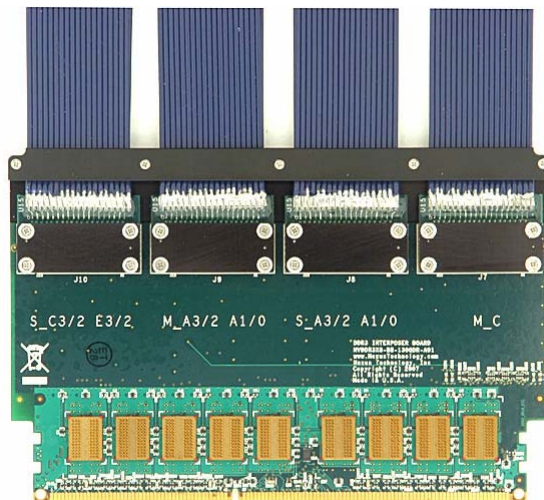
Logic Analyzer Probing

DDR/2/3 SDRAMs, DIMMs & SODIMMs

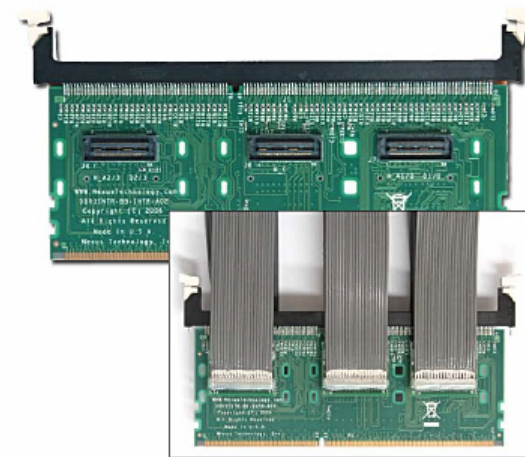
- Direct probing to circuit board
- Interposers
- NEXVu instrument DIMMs



Direct probing



240 pin unbuffered DDR3
DIMM NEXVu



DDR3 DIMM interposer

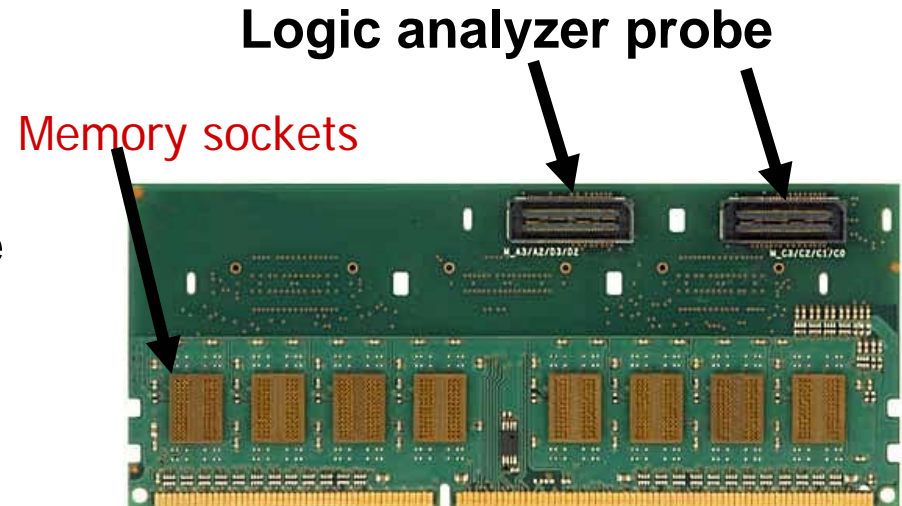
Lowest probe loading in industry at <0.5pF

NEXVu: Instrumented DIMMs

JEDEC layout with measurements at the Memory IC pins



- Visibility of signals as seen by the memory chips
- Least signal integrity intrusive
- Logic analyzer connects above the normal DIMM height



240 pin unbuffered DDR3 UDIMM

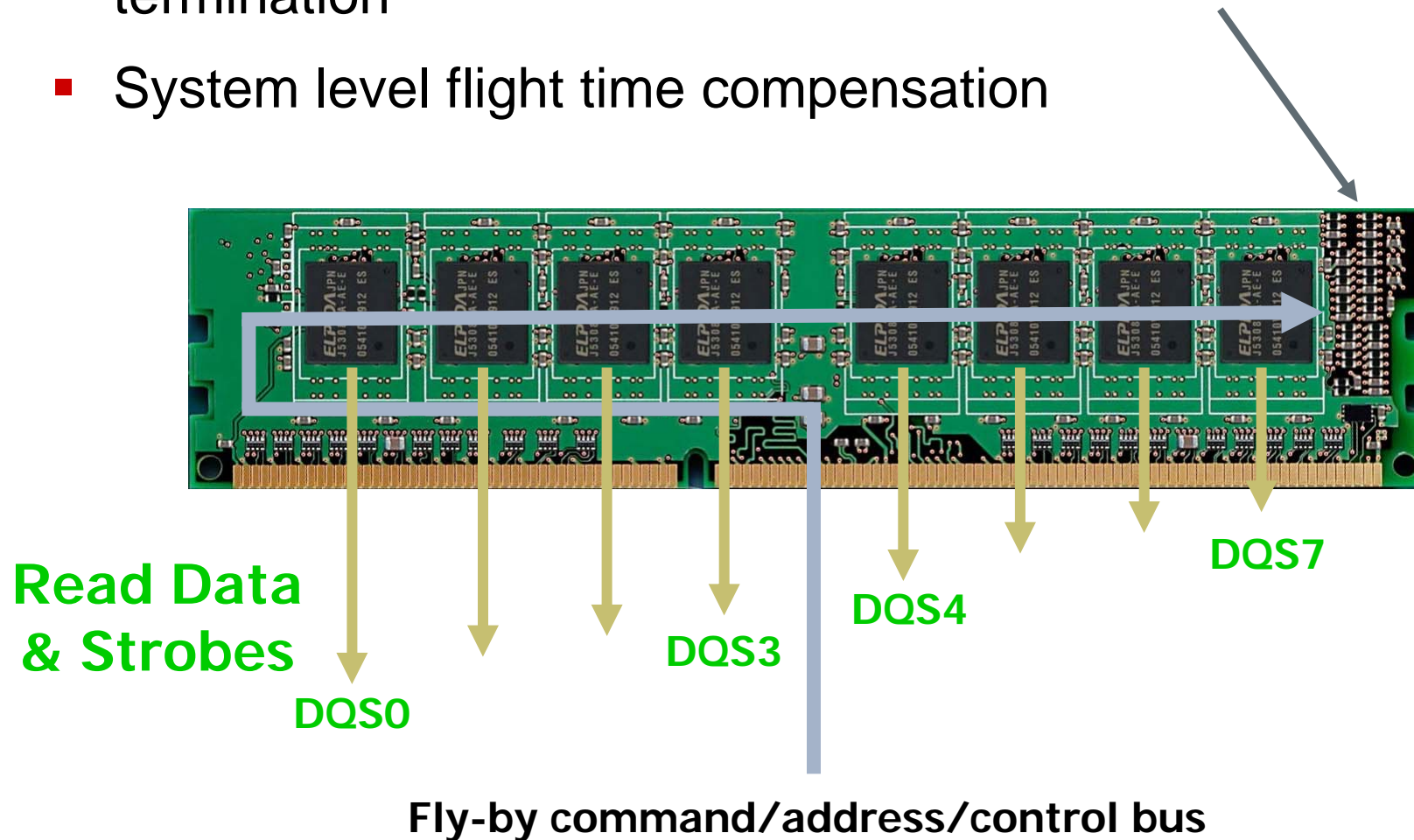
Best measurement of the signal quality at the memory IC.

Signals are probed at the memory IC pins with an inner circuit board isolation resistors to reduce probe loading.

DDR3 240-pin UDIMM Signal Skew

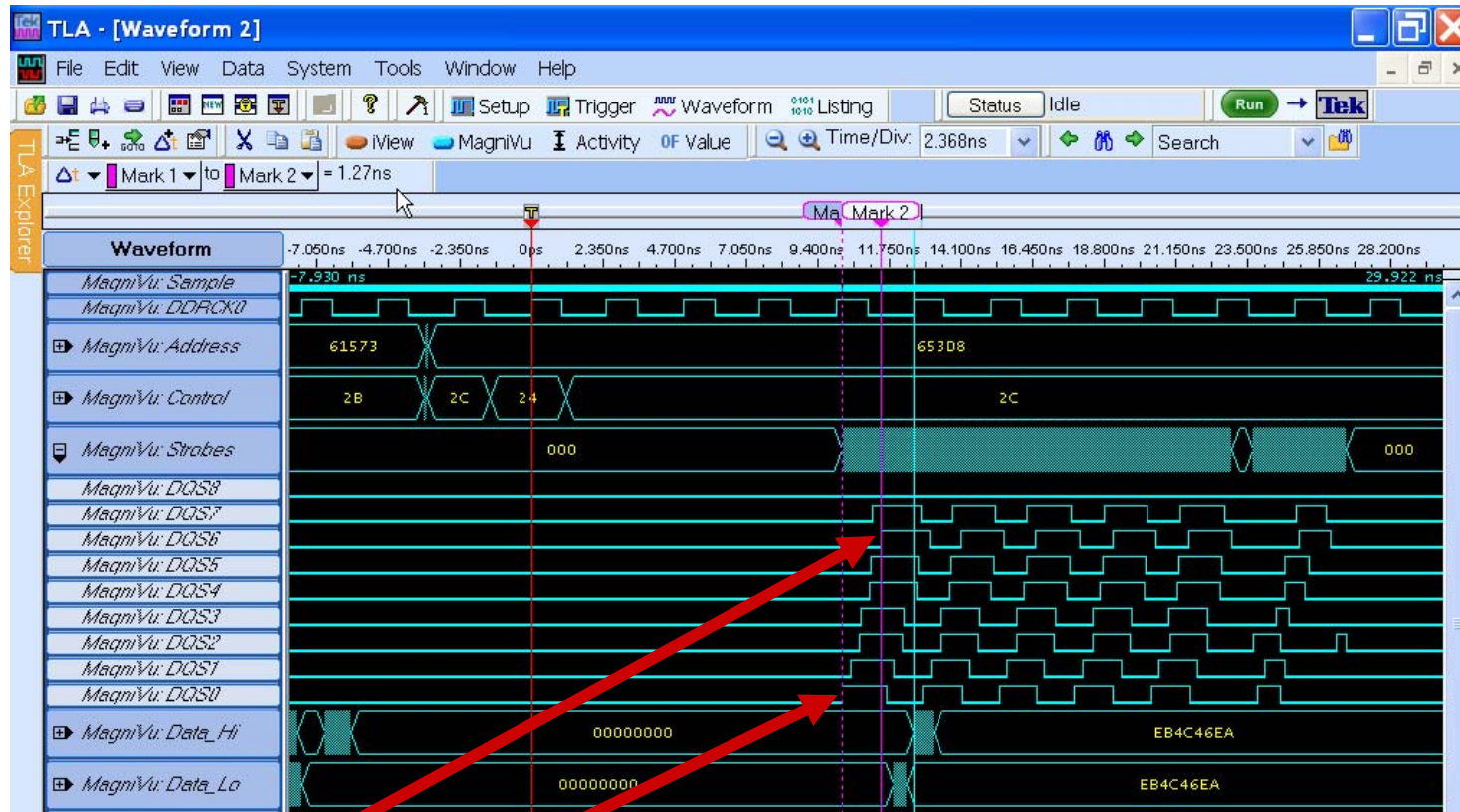
No ECC

- Fly-by command/address/control bus with On-DIMM termination
- System level flight time compensation



Write Data Strobes Skew Analysis

Logic Analyzer MagniVu 20 ps (50 GS/s) timing resolution



1.27ns DQS6 to DQS0 skew captured with 20ps timing resolution

Oscilloscope timing performance on
all logic analyzer channels all the time

Logic Analyzer Probes used by the Oscilloscope

TLA7016 & TLA7BB4s

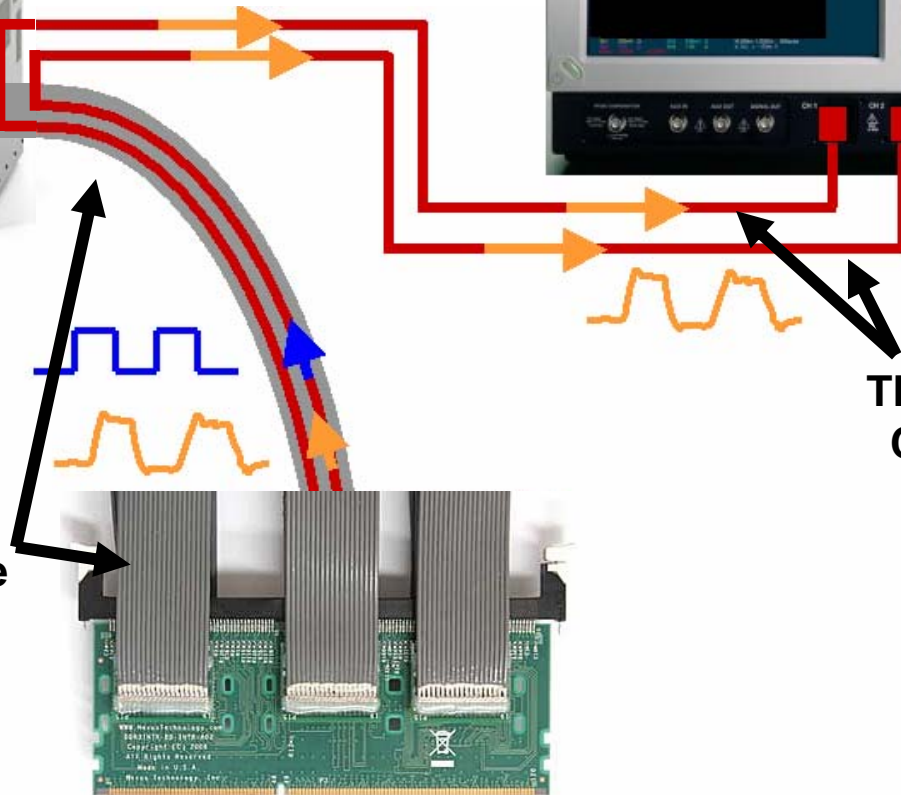


Any Oscilloscope



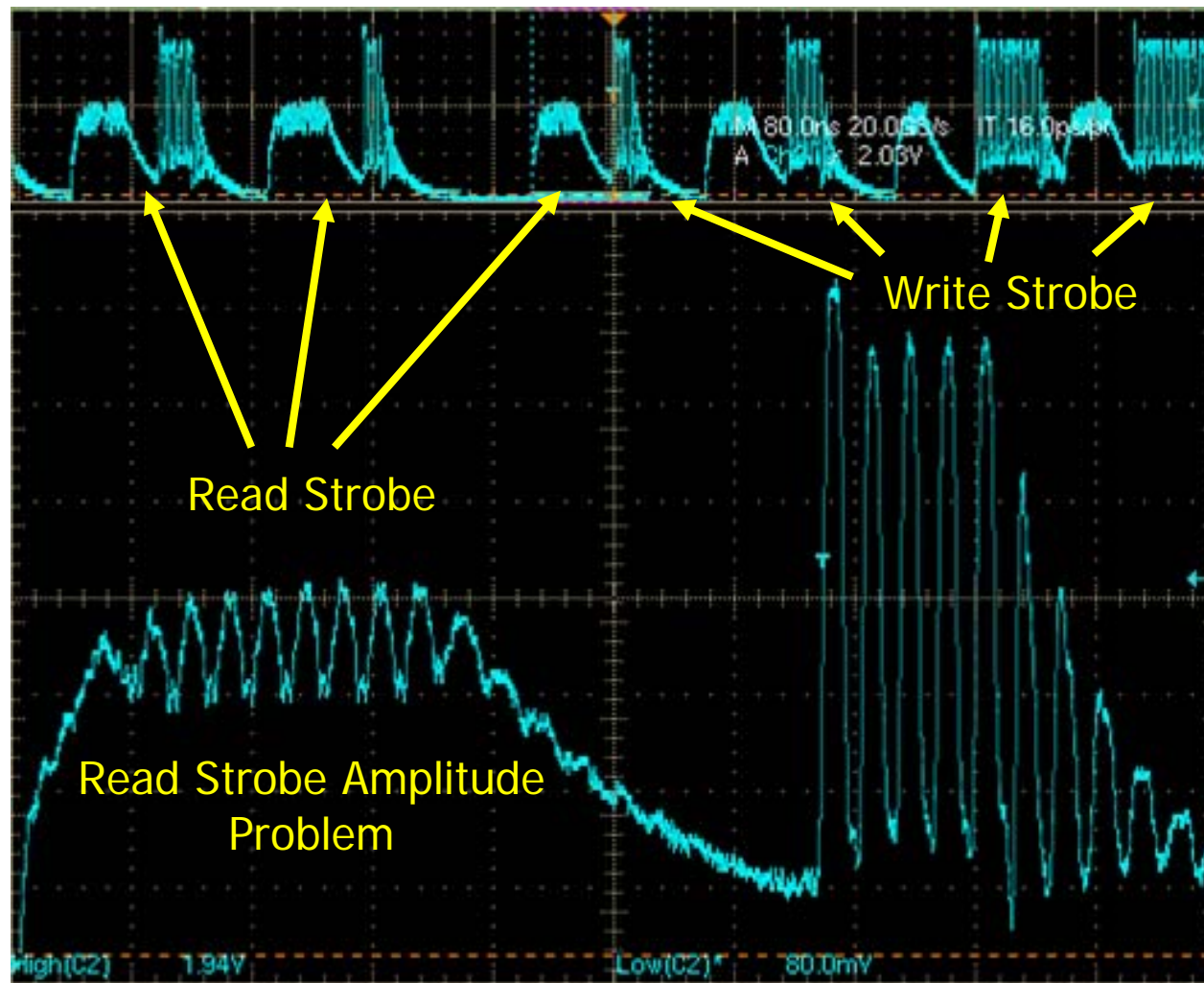
TLA BNC
Cables

iCapture: Logic Analyzer
integrated digital/analog probe



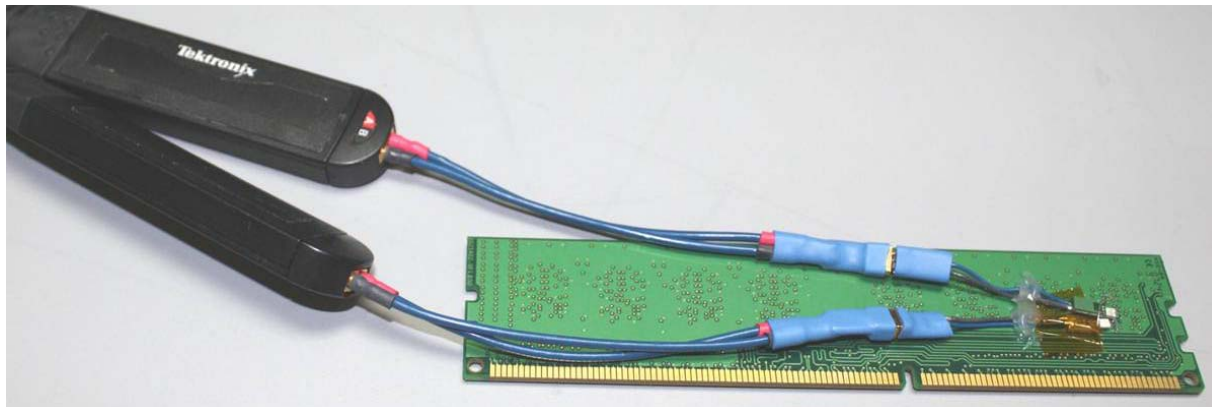
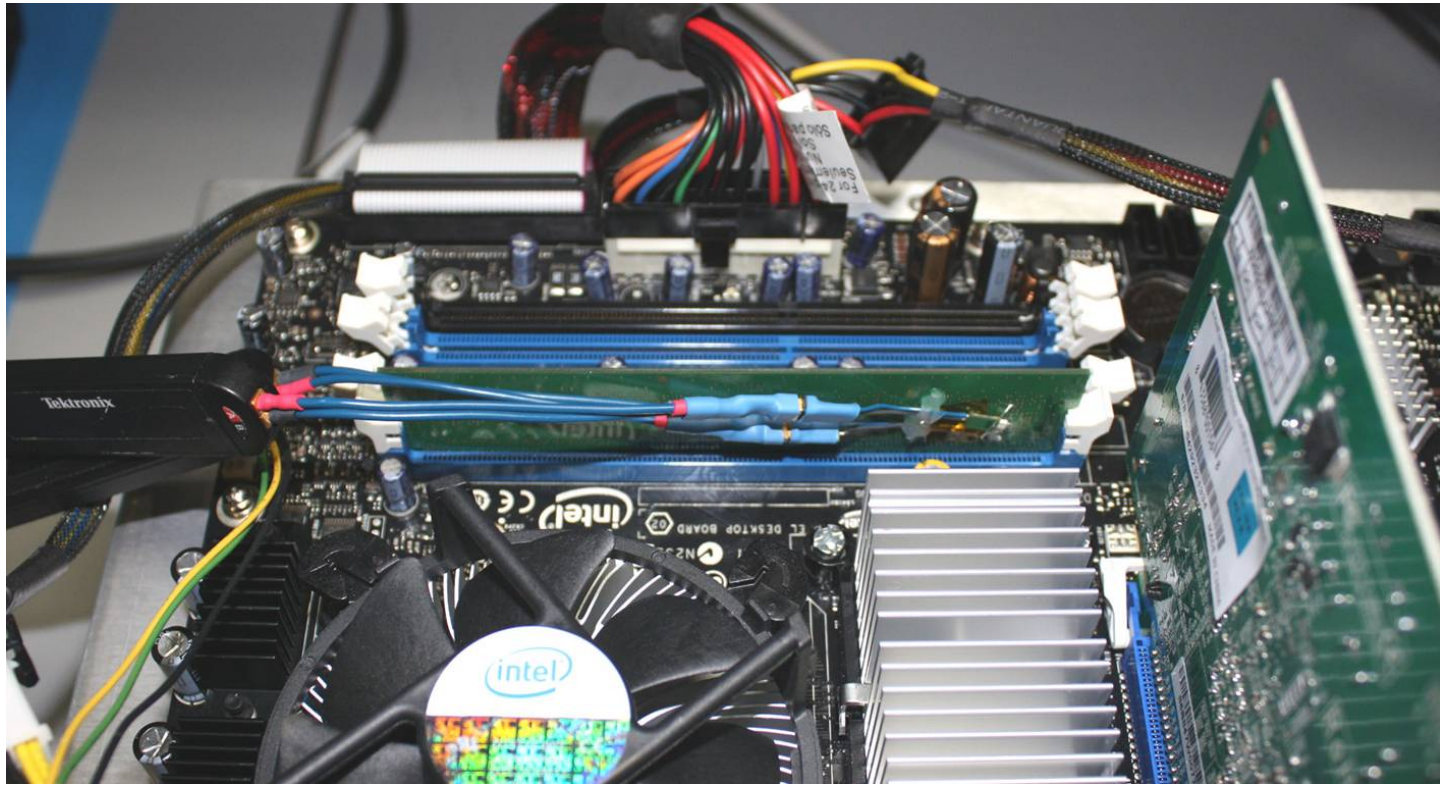
DDR3 DQS2 Strobe Waveform

Amplitude problem with Read strobe from DIMM



Logic analyzer probes used by the oscilloscope

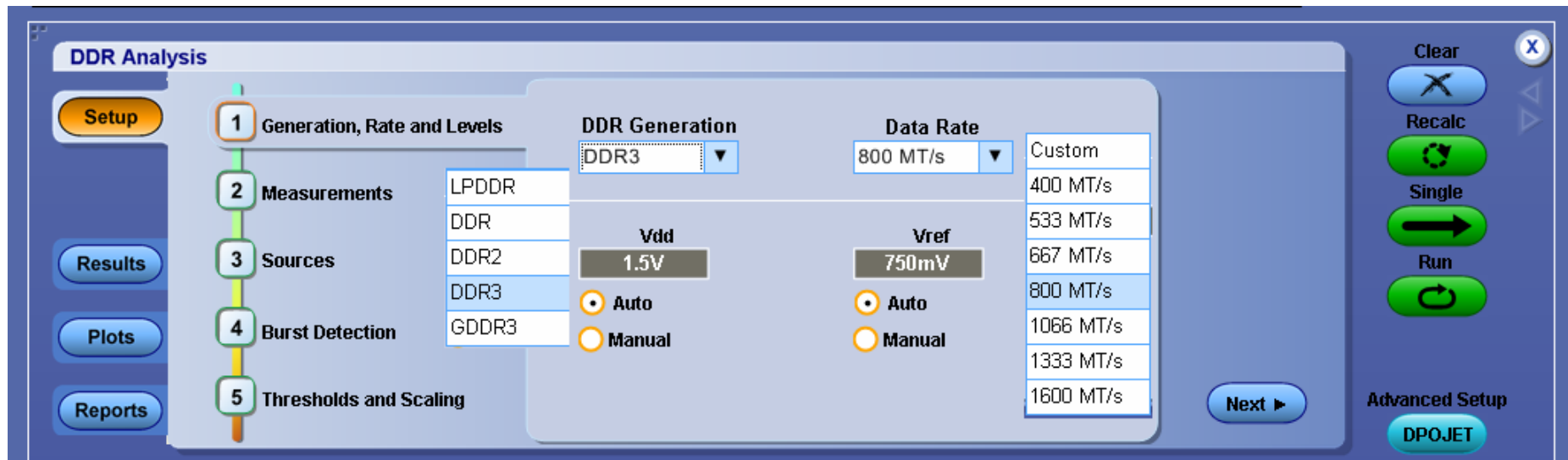
TriMode Probing for DSA/DPO70000 scopes



DDR memory validation wizard for DSA/DPO70000 series

Steps to completion:

1. Speed selection and Vref detection (automatic or manual)
2. Different types of measurements for different bursts
3. Chip Select Qualification to provide selective Read/Write Bursts
4. Detection of levels is automatic - or – customized
5. Threshold scaling



Measurements and configuration

- Compliance and analysis support
- Measurements on all edges and bursts
- JEDEC DDR measurements and serial data measurement library

The screenshot displays the Tektronix DDR Analysis software interface. The main window is titled "DDR Analysis" and features a sidebar with navigation buttons: Setup, Results, Plots, and Reports. A vertical progress bar on the left indicates the current step in the analysis process, with steps 1 through 5: 1. Generation, Rate and Levels (checked), 2. Measurements (highlighted), 3. Sources, 4. Burst Detection, and 5. Thresholds and Settings.

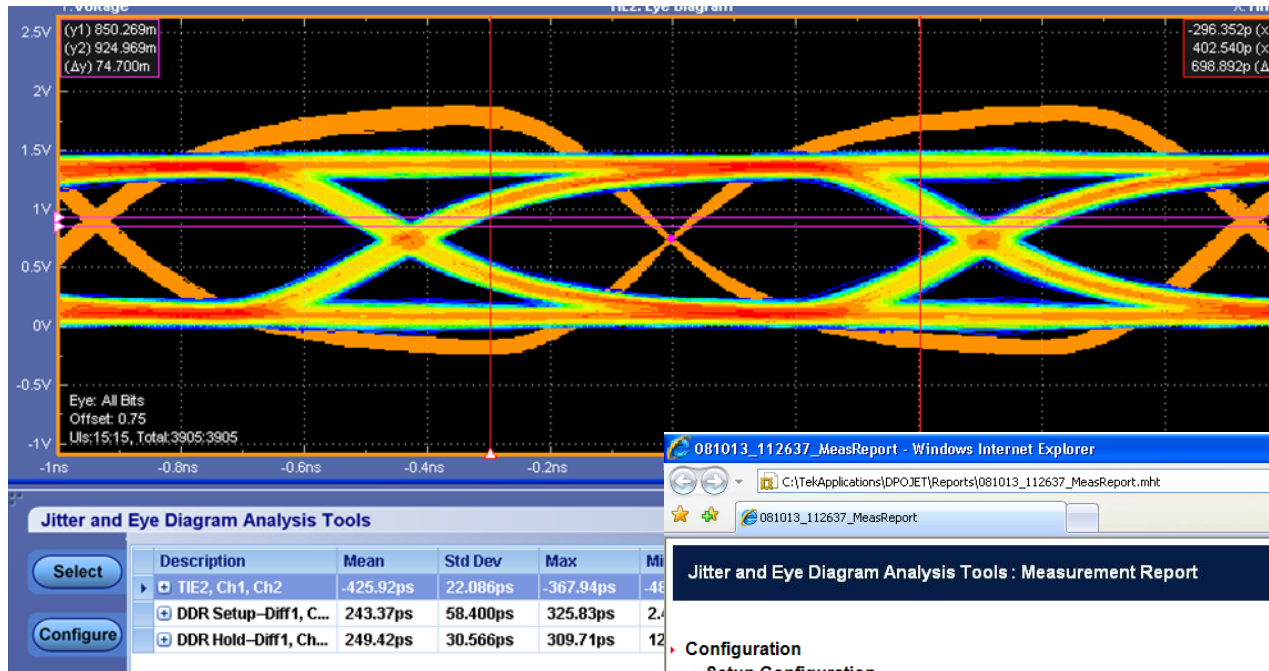
The central area shows the "Burst Detect Control" panel, which includes a dropdown menu for "Write Bursts" and a list of measurement items: Write Measure, Data Eye Width, tDH-Diff(ba), and tDQSH.

Below the main window, a smaller window titled "DDR Analysis" displays a table of measurement results. The table has columns for Description, Mean, Std Dev, Max, Min, p-p, Population, Max-cc, and Min-cc. The data is organized into sections for Data Eye Width, Ch1, and IDQSL, Ch1.

Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Data Eye Width, Ch...	1.7382ns	38.811ps	1.7839ns	1.6810ns	102.89ps	6	0.0000s	0.0000s
IDQSH, Ch1	1.8933ns	26.531ps	1.9553ns	1.7800ns	175.28ps	165	115.54ps	-96.488ps
High Limit				1.3130ns				
Low Limit								
Pass Fail				Fail				
Current Acquisition	1.8851ns	18.001ps	1.9208ns	1.8555ns	65.333ps	12	23.857ps	-27.857ps
IDQSL, Ch1	1.8530ns	26.073ps	1.9120ns	1.7875ns	124.50ps	246	79.167ps	-74.048ps
High Limit				1.3130ns				
Low Limit								
Pass Fail				Fail				

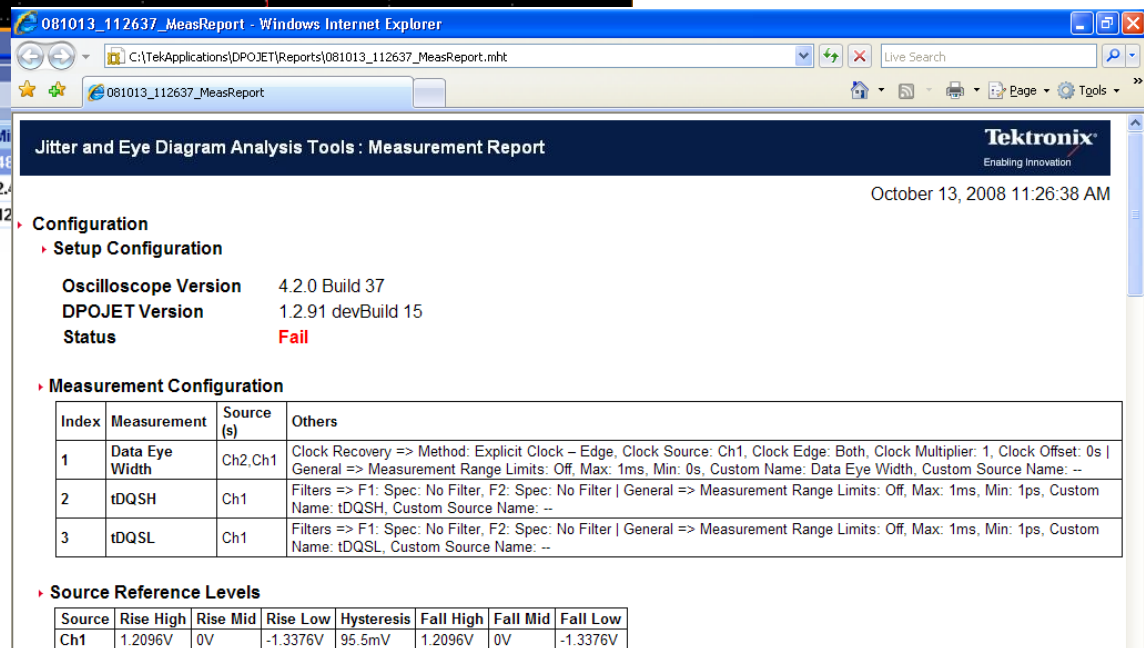
The interface also includes a "Clear" button and a "Recalc" button in the top right corner. The bottom right corner features a "Show Plots" button and a "DPOJET" button.

Analog Validation of DDR memory



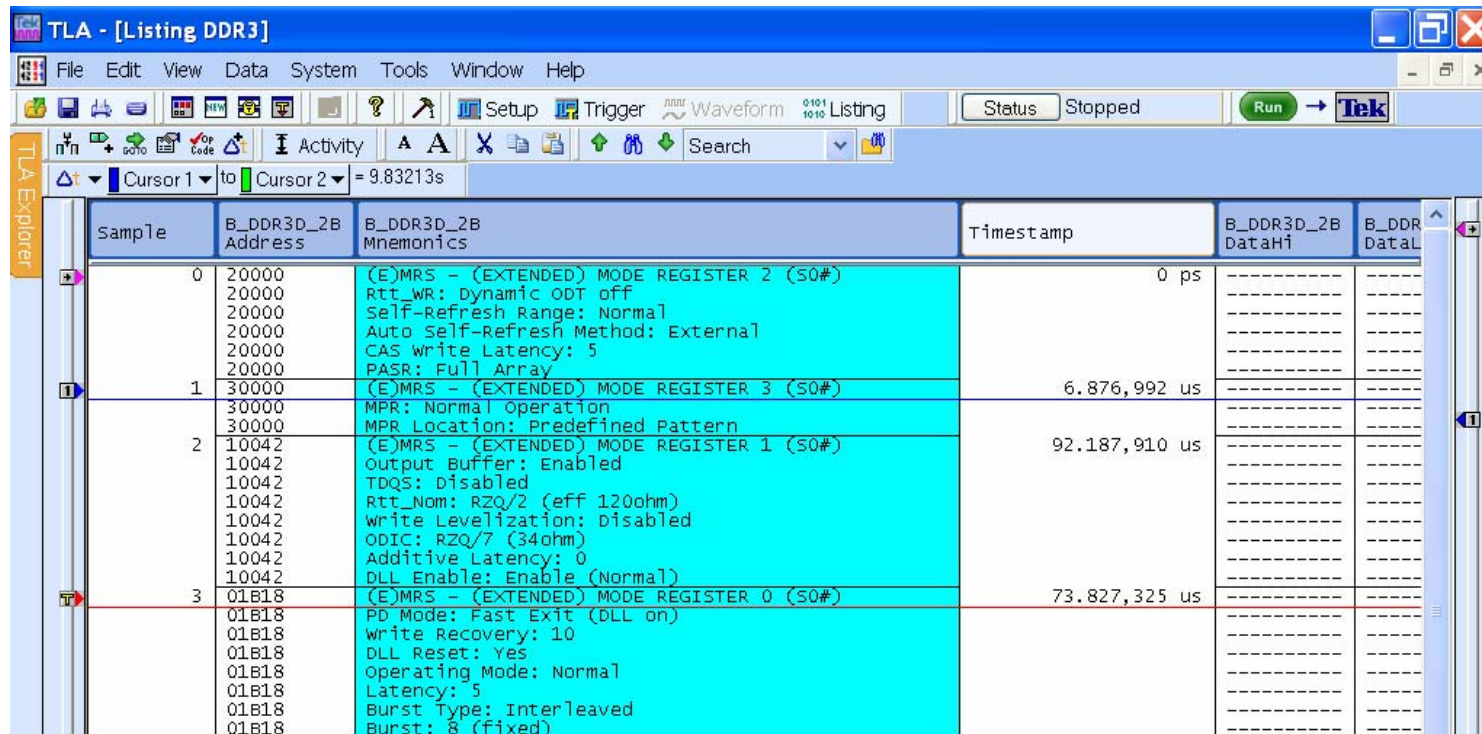
- Data Eye Diagram with Strobe information
- Quickly switch to DPOJET for powerful debug and analysis capabilities

- Complete Measurement Report
- Waveform screenshots, eye diagram, and detailed setup information



Mode Register Analysis

Only 4 MRS Commands Captured at Power-on



TLA - [Listing DDR3]

File Edit View Data System Tools Window Help

Status Stopped Run Tek

Cursor 1 to Cursor 2 = 9.83213s

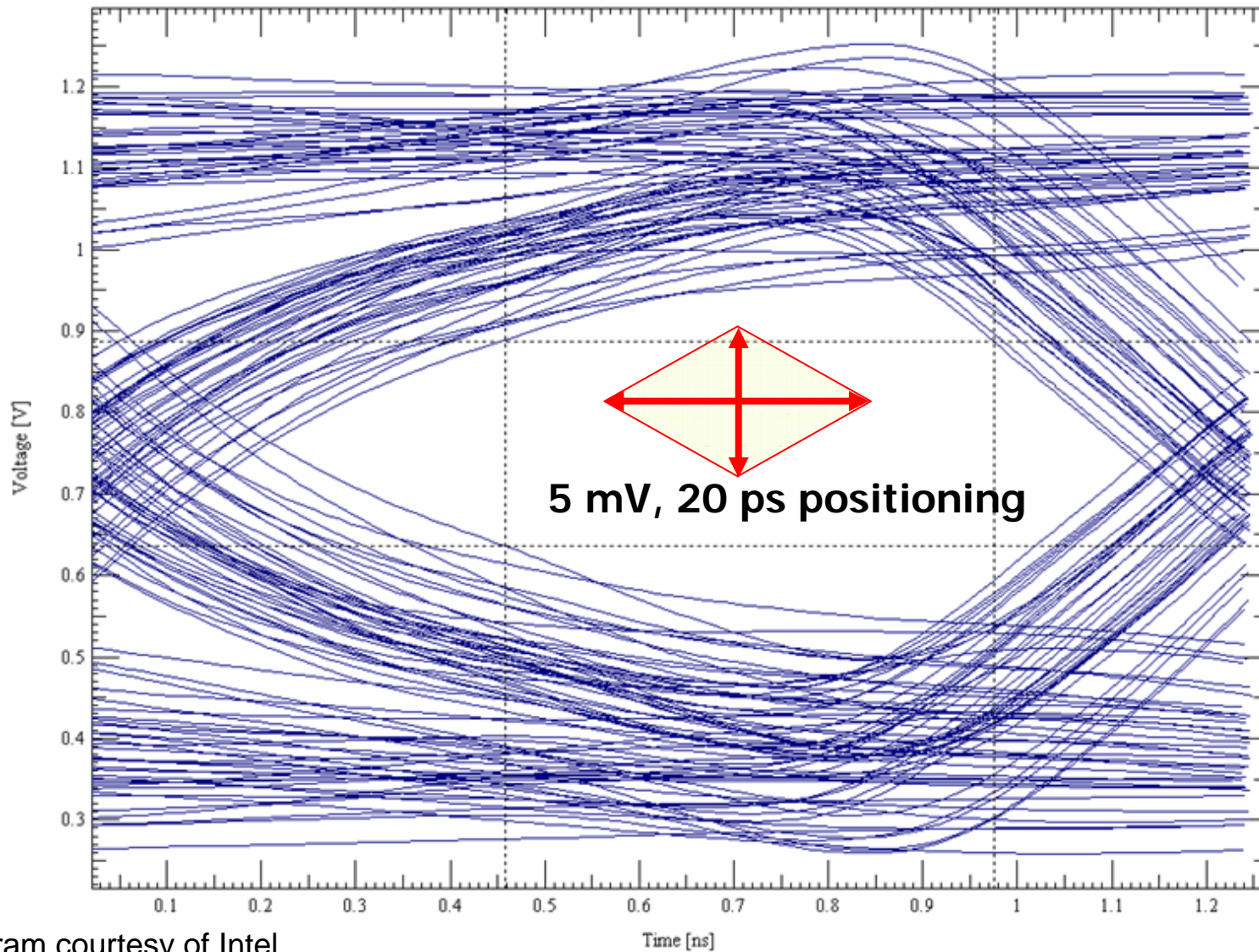
Sample	B_DDR3D_2B Address	B_DDR3D_2B Mnemonics	Timestamp	B_DDR3D_2B DataHi	B_DDR3D_2B DataLo
0	20000	(E)MRS - (EXTENDED) MODE REGISTER 2 (S0#)	0 ps	-----	-----
	20000	Rtt_wR: Dynamic ODT off		-----	-----
	20000	Self-Refresh Range: Normal		-----	-----
	20000	Auto Self-Refresh Method: External		-----	-----
	20000	CAS Write Latency: 5		-----	-----
	20000	PASR: Full Array		-----	-----
1	30000	(E)MRS - (EXTENDED) MODE REGISTER 3 (S0#)	6.876,992 us	-----	-----
	30000	MPR: Normal Operation		-----	-----
	30000	MPR Location: Predefined Pattern		-----	-----
2	10042	(E)MRS - (EXTENDED) MODE REGISTER 1 (S0#)	92.187,910 us	-----	-----
	10042	Output Buffer: Enabled		-----	-----
	10042	TDQS: Disabled		-----	-----
	10042	Rtt_Nom: RZQ/2 (eff 120ohm)		-----	-----
	10042	Write Levelization: Disabled		-----	-----
	10042	ODIC: RZQ/7 (34ohm)		-----	-----
	10042	Additive Latency: 0		-----	-----
	10042	DLL Enable: Enable (Normal)		-----	-----
3	01B18	(E)MRS - (EXTENDED) MODE REGISTER 0 (S0#)	73.827,325 us	-----	-----
	01B18	PD Mode: Fast Exit (DLL on)		-----	-----
	01B18	Write Recovery: 10		-----	-----
	01B18	DLL Reset: Yes		-----	-----
	01B18	Operating Mode: Normal		-----	-----
	01B18	Latency: 5		-----	-----
	01B18	Burst Type: Interleaved		-----	-----
	01B18	Burst: 8 (fixed)		-----	-----

SDRAM MRS2, MRS3, MRS1 & MRS0 configured by the memory controller at power-on & reset

Logic analyzer selective storage captures only useful information

State Acquisition

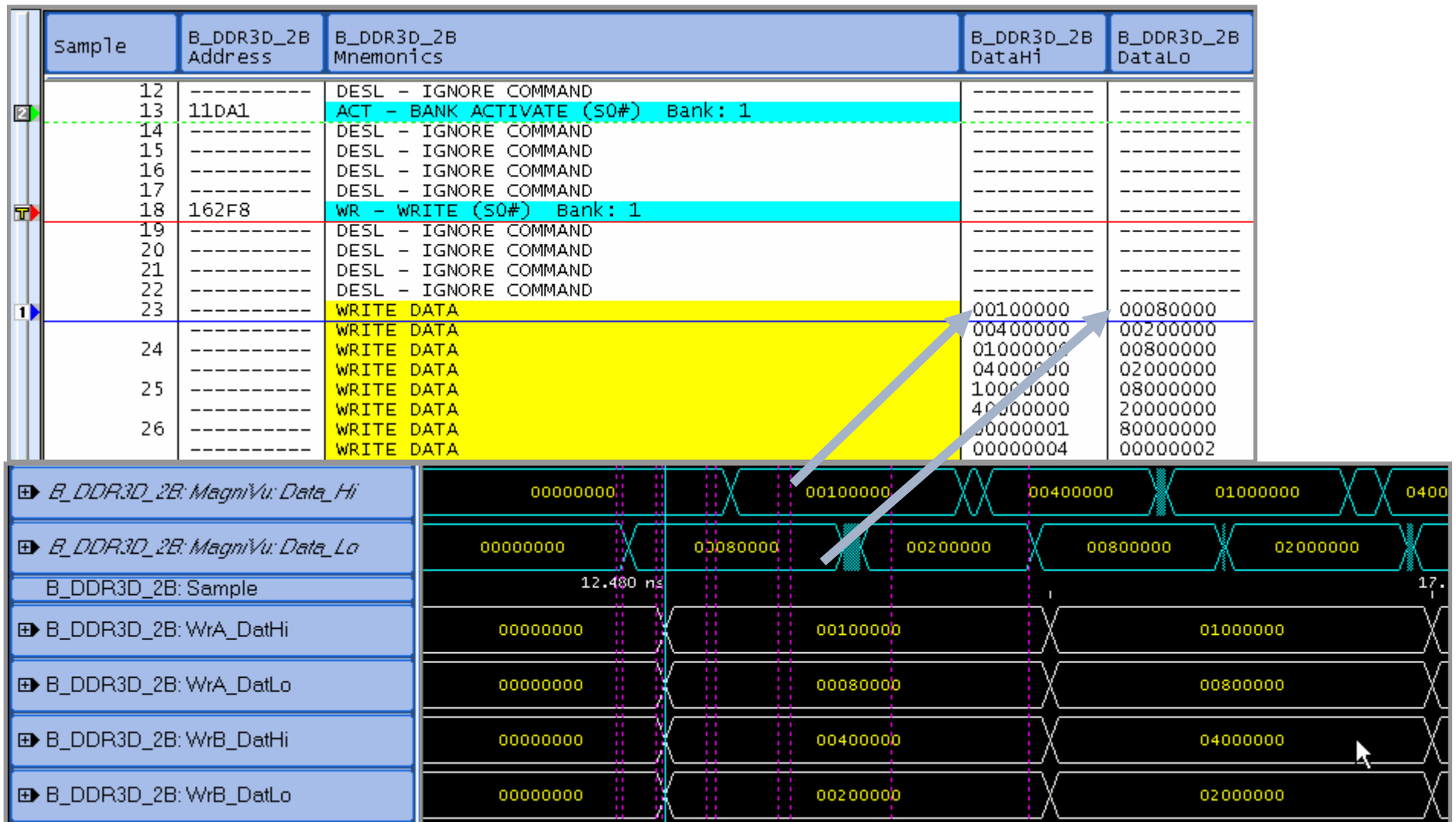
TLA7BB4 Data Valid Window: 200 mV, 240 ps (merged)



Eye diagram courtesy of Intel

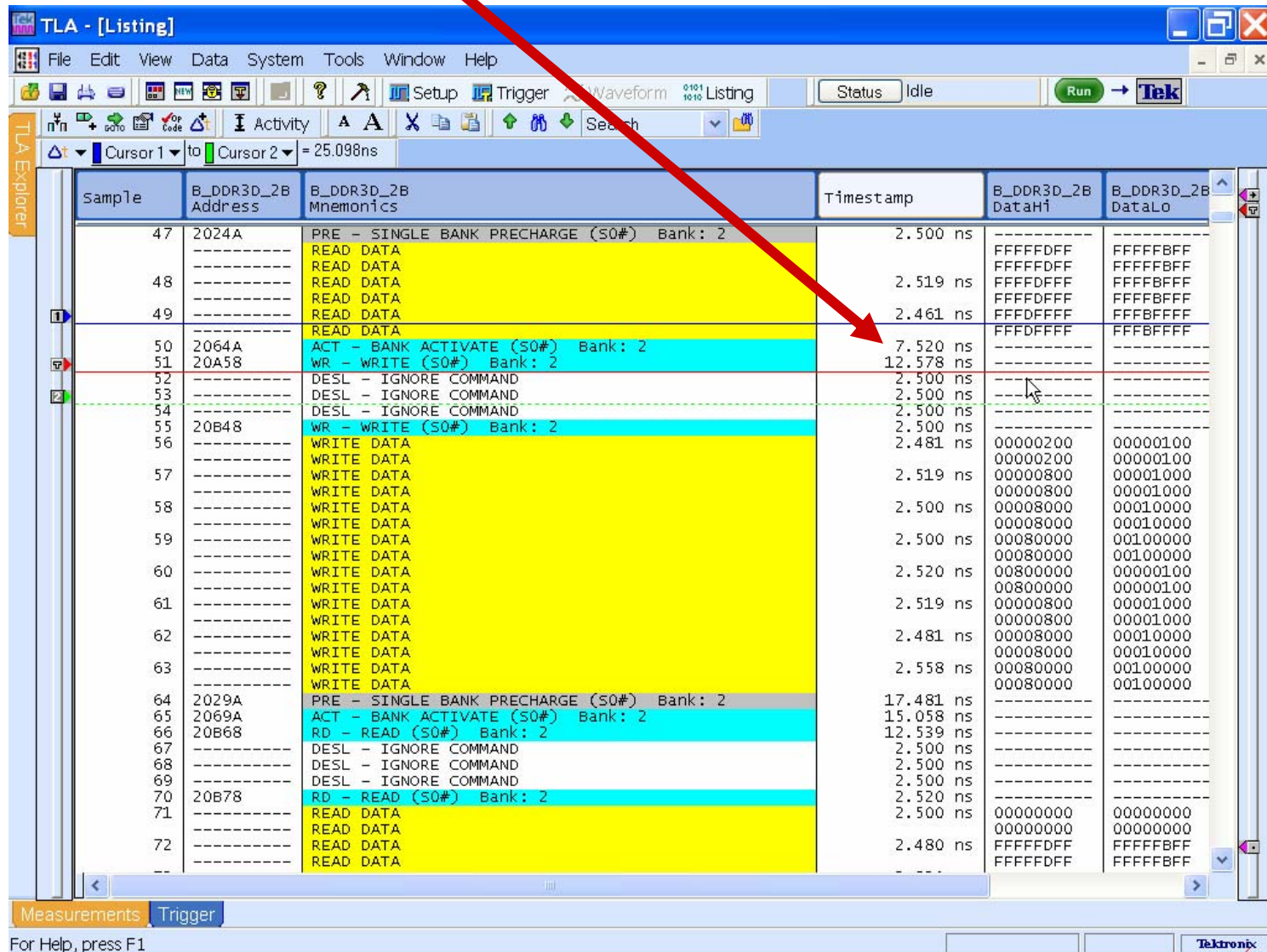
Write Data 64-bits Analysis

Verify state write data groups with MagniVu timing data



Selective Clocking Acquires More Useful Information

Notice Timestamp changes for DESL cycles not stored



Sample	B_DDR3D_2B Address	B_DDR3D_2B Mnemonics	Timestamp	B_DDR3D_2B DataHi	B_DDR3D_2B DataLo
47	2024A	PRE - SINGLE BANK PRECHARGE (S0#) Bank: 2	2.500 ns	-----	-----
48	-----	READ DATA	2.519 ns	FFFFDFFF	FFFFBFFF
49	-----	READ DATA	2.461 ns	FFFFDFFF	FFFFBFFF
50	2064A	ACT - BANK ACTIVATE (S0#) Bank: 2	7.520 ns	-----	-----
51	20A58	WR - WRITE (S0#) Bank: 2	12.578 ns	-----	-----
52	-----	DESL - IGNORE COMMAND	2.500 ns	-----	-----
53	-----	DESL - IGNORE COMMAND	2.500 ns	-----	-----
54	-----	DESL - IGNORE COMMAND	2.500 ns	-----	-----
55	20B48	WR - WRITE (S0#) Bank: 2	2.500 ns	-----	-----
56	-----	WRITE DATA	2.481 ns	00000200	00000100
57	-----	WRITE DATA	2.519 ns	00000200	00000100
58	-----	WRITE DATA	2.500 ns	00000800	00001000
59	-----	WRITE DATA	2.500 ns	00000800	00010000
60	-----	WRITE DATA	2.520 ns	00080000	00100000
61	-----	WRITE DATA	2.519 ns	00000800	00001000
62	-----	WRITE DATA	2.481 ns	00000800	00010000
63	-----	WRITE DATA	2.558 ns	00080000	00100000
64	2029A	PRE - SINGLE BANK PRECHARGE (S0#) Bank: 2	17.481 ns	-----	-----
65	2069A	ACT - BANK ACTIVATE (S0#) Bank: 2	15.058 ns	-----	-----
66	20B68	RD - READ (S0#) Bank: 2	12.539 ns	-----	-----
67	-----	DESL - IGNORE COMMAND	2.500 ns	-----	-----
68	-----	DESL - IGNORE COMMAND	2.500 ns	-----	-----
69	-----	DESL - IGNORE COMMAND	2.500 ns	-----	-----
70	20B78	RD - READ (S0#) Bank: 2	2.520 ns	-----	-----
71	-----	READ DATA	2.500 ns	00000000	00000000
72	-----	READ DATA	2.480 ns	FFFFFDFF	FFFFBFFF

Measurements Trigger

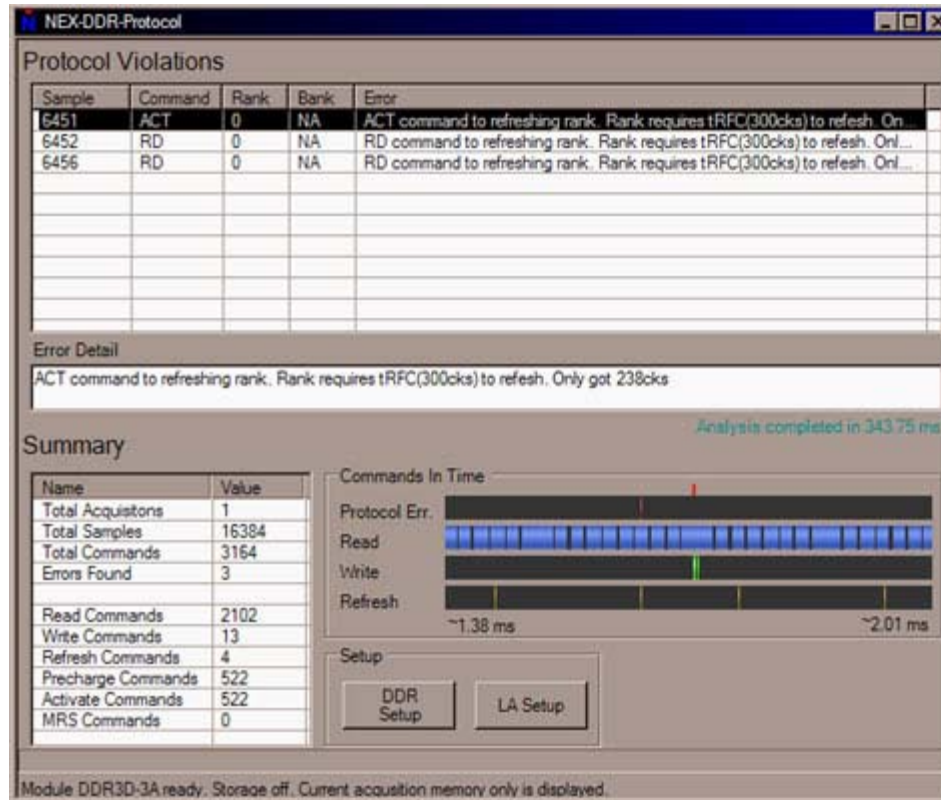
For Help, press F1

Nexus Protocol Violation Software

DDR3/DDR2 Protocol Checking



- Summary/Statistical Info.
- Bus/TLA Memory Utilization
- Quickly display problem areas in Listing & Waveform windows
- Customizable timing parameters
- Export data



Violation Reporting

Utilization
Summary of Data

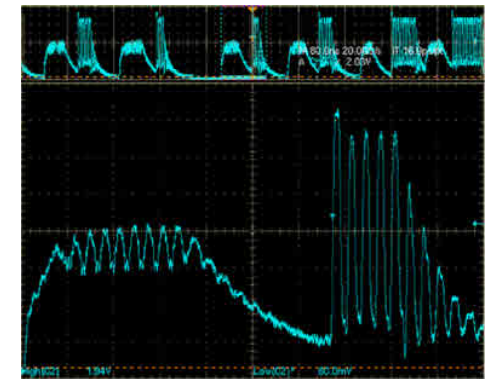
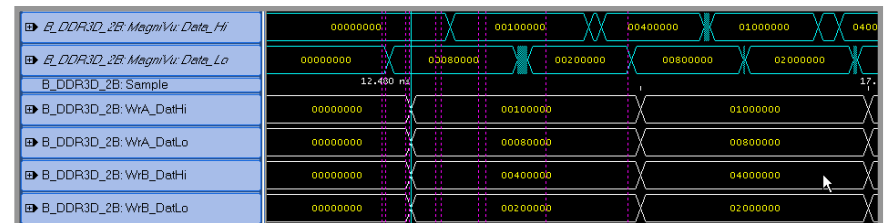
Memory System

Verification & Debug



- DDR/2/3 SDRAM
 - Initialization & mode register
 - Commands & read/write data
 - Waveforms
 - Protocol violation checking
- Selective clocking
 - Stores useful data in the TLA
 - Filters refresh & deselect cycles
- Pre-defined symbols for easy analysis & trigger setup
- Three simultaneous measurements through one probe
 - State acquisition
 - High-resolution 20 ps (50GS/s) MagniVu timing with TLA7BB4
 - Oscilloscope analog waveforms

Sample	B_DDR3D_2B Address	B_DDR3D_2B Mnemonics	B_DDR3D_2B DataHi	B_DDR3D_2B DataLo
12	-----	DESL - IGNORE COMMAND	-----	-----
13	110A1	ACT - BANK ACTIVATE (S0#) Bank: 1	-----	-----
14	-----	DESL - IGNORE COMMAND	-----	-----
15	-----	DESL - IGNORE COMMAND	-----	-----
16	-----	DESL - IGNORE COMMAND	-----	-----
17	-----	DESL - IGNORE COMMAND	-----	-----
18	162F8	WR - WRITE (S0#) Bank: 1	-----	-----
19	-----	DESL - IGNORE COMMAND	-----	-----
20	-----	DESL - IGNORE COMMAND	-----	-----
21	-----	DESL - IGNORE COMMAND	-----	-----
22	-----	DESL - IGNORE COMMAND	-----	-----
23	-----	WRITE DATA	00100000	00080000
24	-----	WRITE DATA	00400000	00200000
25	-----	WRITE DATA	01000000	00800000
26	-----	WRITE DATA	04000000	02000000
27	-----	WRITE DATA	10000000	08000000
28	-----	WRITE DATA	40000000	20000000
29	-----	WRITE DATA	80000001	80000000
30	-----	WRITE DATA	00000004	00000002





Agenda

- High Speed Serial Data Test Challenges
- PCI Express Digital Validation and Debug
- DDR Memory Validation and Debug
 - Probing
 - Acquisition
 - Analysis
- DDR2 Demo
- Summary

DDR2 Demo Setup

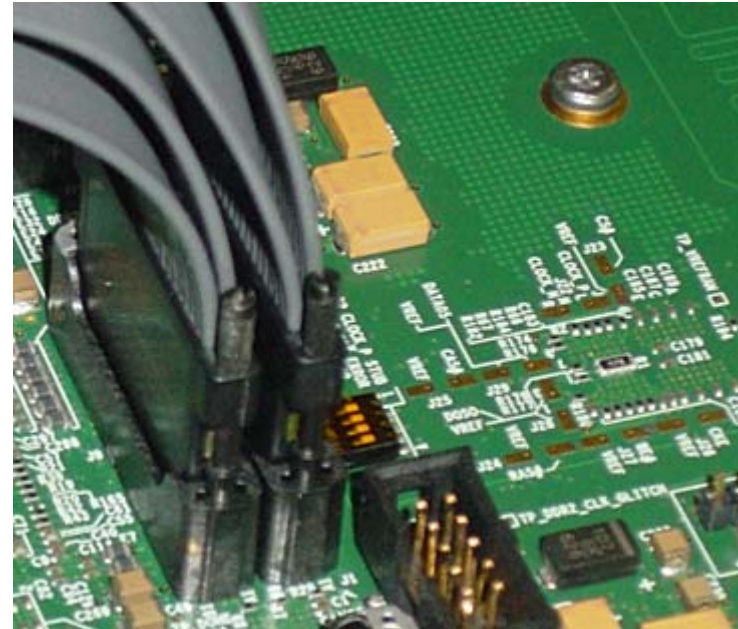
TLA7BB4, TLA7S16 & TLA7012 Logic Analyzer with second display



DDR2-533 & PCIe 2 development board

DDR2 Demo

- Mode Register Set
- Refresh Error
- Refresh Valid
- Read Data 123
- Read Data 123 Waveform View
- Write Trigger
- Selective Clocking



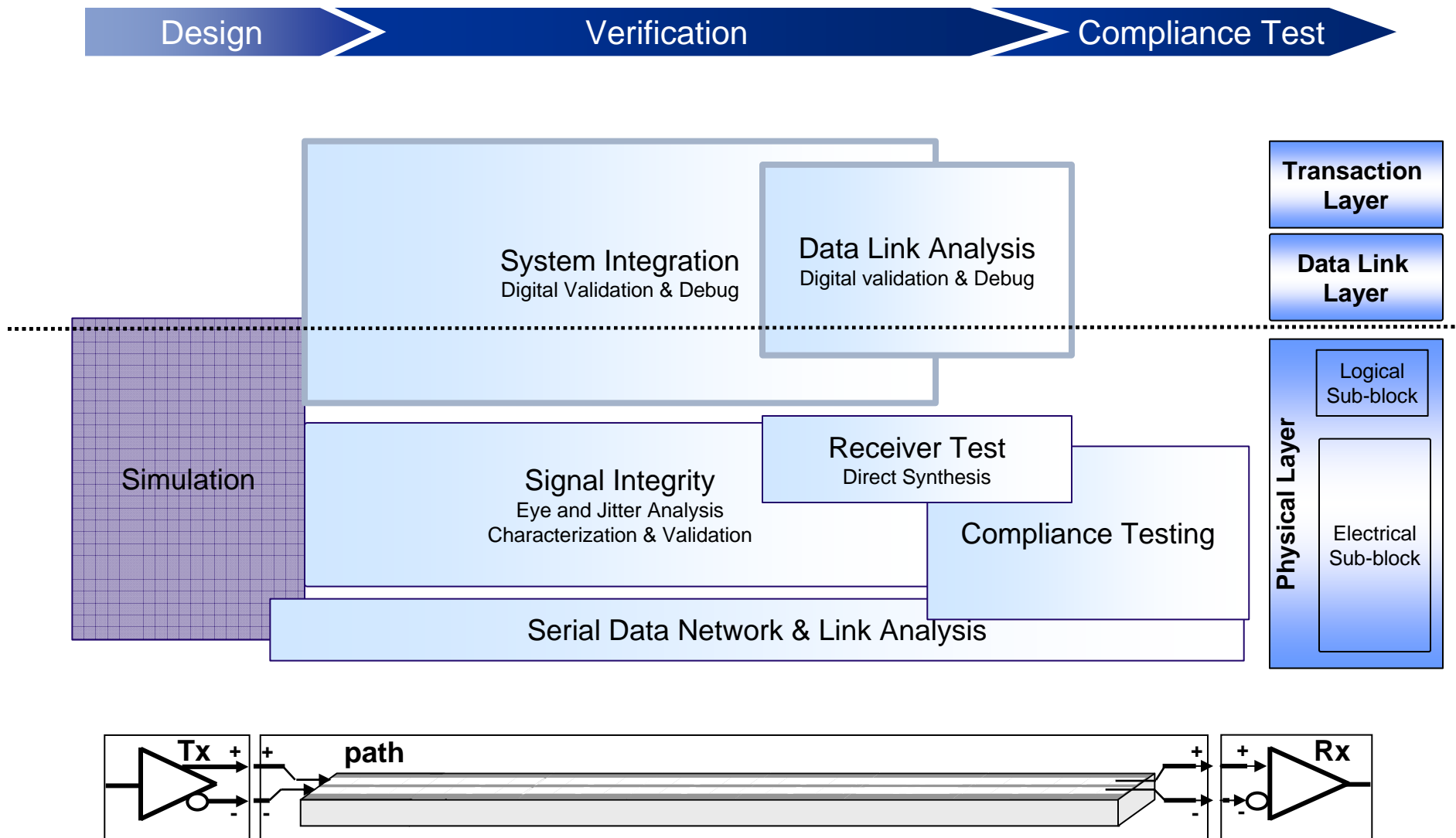
Direct probing DDR2-533 with two P6960 logic analyzer probes



Agenda

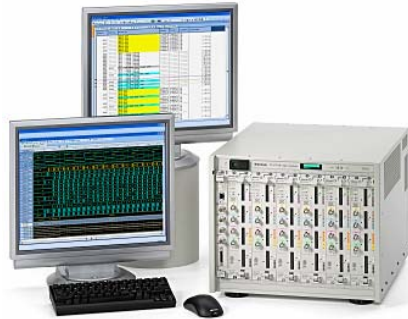
- High Speed Serial Data Test Challenges
- PCI Express Digital Validation and Debug
- DDR Memory Validation and Debug
 - Probing
 - Acquisition
 - Analysis
- DDR2 Demo
- Summary

High Speed Digital Test Challenges



High Speed Digital Verification & Debug

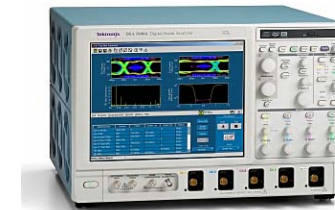
Protocols, Data, Signal Quality & Circuit Board Trace Quality



- Memory Protocols & Data
 - TLA7000 Logic Analyzers



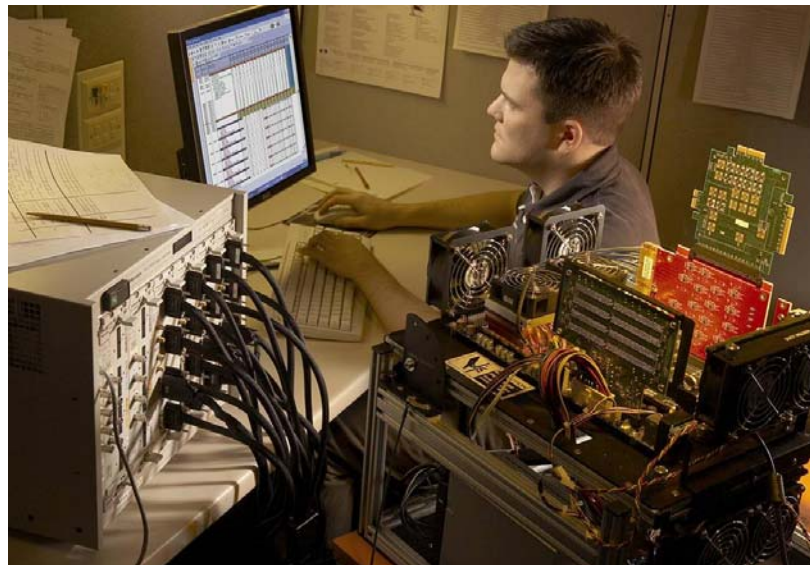
- Circuit Board Trace Quality
 - CSA8200 Sampling Oscilloscopes



- Signal Quality
 - DPO/DSA70000 Series Oscilloscopes

PCI Express Information

- Tektronix
 - www.tektronix.com/pci_express
- PCI Special Interest Group (PCI-SIG®)
 - www.pcisig.com
- PCI Express Test Procedures
 - www.pcisig.com/specifications/pciexpress/compliance/compliance_library



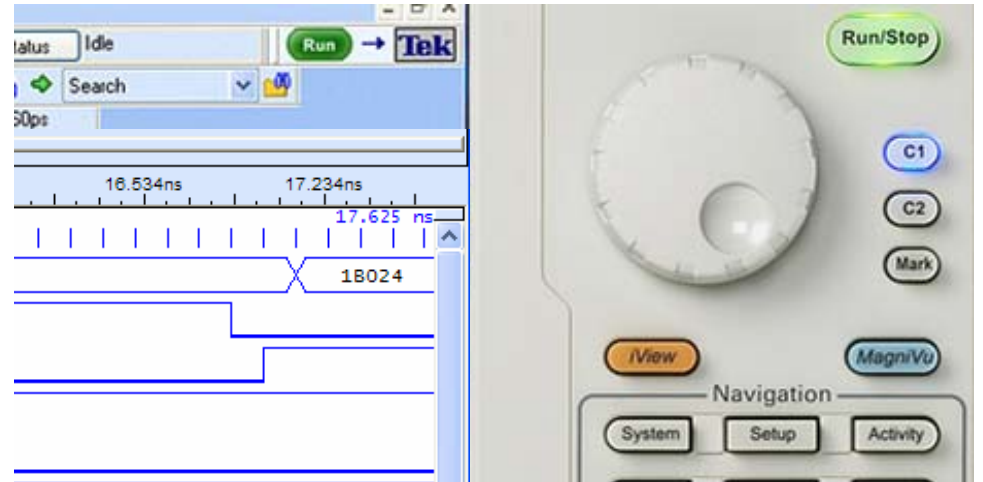
Memory Information

- Tektronix
 - www.tektronix.com/memory
- Nexus Technology
 - www.nexustechnology.com
- Memory Implementers Forum
 - www.memforum.org
- JEDEC
 - www.jedec.org



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