Mastering Validation and Debug of Digital Systems
Agenda

- High Speed Serial Data Test Challenges
- PCI Express® Digital Validation and Debug
- DDR Memory Validation and Debug
  - Probing
  - Acquisition
  - Analysis
- DDR2 Demo
- Summary
High Speed Serial Test Challenges

- Design Verification Compliance Test
- System Integration: Digital Validation & Debug
- Data Link Analysis: Digital validation & Debug
- Signal Integrity: Eye and Jitter Analysis, Characterization & Validation
- Receiver Test: Direct Synthesis
- Serial Data Network & Link Analysis

Diagram elements include:
- Simulation
- Transaction Layer
- Data Link Layer
- Logical Sub-block
- Electrical Sub-block
- Physical Layer

Signal path components:
- Tx
- Rx
- path
High Speed Serial Test Challenges

- Giga-bit data rates require higher performance instruments
  - Decreased timing budget: Faster timing resolution
  - Transmission line effects: Low loading

- Industry focus on reducing power consumption
  - Link width down configure for power savings and upconfigure when additional bandwidth is required
  - Electrical Idle Entry and Exit for power savings, design ease, and robustness

- Industry standards are defining stringent measurement and analysis requirements
Digital Validation & Debug

**Data Access - Probing**
- Requires reliable physical connectivity with minimal loading
  - Mid Bus Probes
  - Interposers
  - Instrument DIMMs
  - Direct probing to circuit board
- Requires maximum signal integrity

**Data Acquisition**
- Timing resolution high enough for thorough debugging
- Trigger state machine flexible enough to trigger only on relevant events
- Channel count scalable and high enough to capture all required signals
- Scalable and time correlated system for cross bus analysis

**Data Analysis**
- Verify and debug memory system operation
  - Data valid windows
  - Read/Write data operation
  - DDR commands and mode register initialization
- Quickly and easily identify protocol violations
- Analyze link training, power management, and advanced packet level decoding
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Example - PCI Express Protocol Stack

- **Transaction Layer**
  - Creates Request/Completion Transactions
  - Messaging
  - TLP Flow Control

- **Data Link Layer**
  - Flow control information
  - Data Integrity, Error Checking/Correction
  - Calculates/Check TLP Sequence Number
  - Calculate/Check CR

- **Physical Layer – Logical Sub Block**
  - Link Initialization and Training
  - Distribution of packet information over multiple lanes
  - Power management and link power state transitions

- **Physical Layer – Electrical Sub Block**
  - Transmitter Signal Quality and Ref Clock Testing
  - Receiver Testing
  - Interconnect Testing
  - PLL Loop BW
Primary PCIe 2.0 Digital Debug Challenges

Power management and link training continue to be the most difficult challenges

- **Power Up & Link Initialization**
  - Multi-lane systems (x1, x4, x8, x16)
  - PCIe 1.0 <-> PCIe 2.0 systems compatibility: Speed negotiation from 2.5Gb/s to 5.0Gb/s and 5.0Gb/s to 2.5Gb/s
  - Dynamic speed & link width changes

- **Active State Power Management**
  - Power Management: Electrical Idle Entry and Exit for power savings,
  - Dynamic link width and link speed changes depending on data transfer volume requirements

- **A PCIe Bus Remains Part of a Total System**
  - Critical cross bus dependencies increase with speed
  - Time-correlated visibility across multiple buses
  - Signal access across the entire system
Primary PCIe 2.0 Digital Debug Challenges

SUT device indicates it’s entering L0s

10 Fast Training Sets displayed (not all FTSs shown here). The SUT actually sent 22.

COM, SKP detected on all lanes and is re-aligned.
**PCI Express 2.0 – Power Management**

**ASPM Active State Power Management**

*Need for Lower Power Consumption and Longer Battery Life*

- **Power management**
  - Less energy consumption
  - Longer battery lifetime
  - Government regulations: EnergyStar®

- **PCIe 2.0 power management implementations**
  - Dynamic link width changes depending on current data transfer volume.
  - Dynamic link speed changes depending on data transfer requirements (2.5Gb/s <-> 5Gb/s)
  - Short term idle states of one or both direction of a link (L0s, L1)
    - L0s: autonomous Idle-state of a link for a very short time
    - L1: short term Idle-state initiated by a higher level protocol

*When a lane is in Idle, no Power is consumed by that lane*
Power Management Sequence (L0s-example)

- L0s Power management is being used more frequently in PCI Express designs
- L0s: autonomous Idle-state of one or both direction of a link for a very short time
  - Efficiency depends on how fast a system can enter and exit the L0s state.
  - L0s Exit Latency is measured by the number of “Fast Training Set’s” (FTS) packets required by the system, to exit the L0s state.
  - Number of FTS = 1…255 (~16nS…4µS)
- Past designs have exhibited failures during ASPM events, thus visibility of these events is critical to the debug engineer
How to Debug:

- Detect and quickly re-sync as the bus employs ASPM in order to acquire all packets as the link exits L0s

- Tektronix supports maximum visibility of these transitions
  - Typical sync within 12 FTS packets for both 2.5Gb and 5Gb
Multiple Analysis Options
Packet Decode and Multi-bus Correlation

- Packet Decode and Transaction support in the Listing Window
  - Complete decode of PCI Express Packets
  - Symbolic decode on a lane by lane basis
  - View Tx and Rx in a common listing window or lock listing windows for transaction support

- Quick insight to system problems- View all system buses in the waveform window
  - View all system buses correlated to the TLA common system timestamp
  - Correlate analog and digital waveforms
Correlate Cross Bus Data

Graphics Bus response:
TLP MWr to 15325EC0h

FSB issues a Memory Write to Address 15325EC0h
Complete System Digital Debug & Design Verification
PCI Express 2.0 Logic Analyzer Solution

- **Performance**
  - Auto detect 2.5Gb/s to 5.0Gb/s data rate change
  - Dynamically track link width Upconfigure/Downconfigure
  - World class ASPM support - L0s and L1 sync time

- **Visibility**
  - Correlate all system buses to the common TLA timestamp
  - Import scope waveforms for analog / digital correlation
  - See the data you want with HW and SW filtering 32M 8b/10b symbols per lane acquisition depth

- **Flexibility**
  - Backwards compatible to PCIe 1.x (data rate/footprint)
  - Acquire x1, x4, and x8 links in a single TLA7S16 module
  - Acquire x1 and x4 links in a single TLA7S08

- **Best Probing Solution**
  - Mid-bus or Interposer probing options at 5.0Gb/s
  - Minimal impact on probed signals
  - No need for multiple probes to support different routings
  - Easy access to SUTs with 6 foot cable length
  - C-springs are integrated with the retention mechanism
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# Memory Systems

Gigabit Data Rates

- **DDR/2/3 SDRAM**
  - Driven by increasing computer performance
  - Performance doubles every ~ 3 years

- Complex parallel bus
  - Fast clock speeds
  - Small data valid eyes
    - Small timing margins
    - Crosstalk, impedance & jitter

- Memory system verification is critical to reliable product operation

<table>
<thead>
<tr>
<th>SDRAM</th>
<th>Data Rate MT/S</th>
<th>Clock MHz</th>
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<td>DDR-266</td>
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<td>133</td>
<td>2.5</td>
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<td>DDR-333</td>
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<td>400</td>
<td>200</td>
<td>2.5</td>
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<td>DDR2-400</td>
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<td>200</td>
<td>1.8</td>
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<td>DDR2-533</td>
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<td>1.8</td>
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<td>334</td>
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<td>DDR3-1867</td>
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<td>933</td>
<td>1.5</td>
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</table>
Tektronix Platform Validation System
Complete System Visibility with Time Correlation

- Nexus Technology DDR3 NEXVu
- DDR3 Direct Probing
- QPI Bus
- PCI Express 2
- Electrical compliance test

TLA7000 Series Logic Analyzer with Nexus Memory Supports

DPO/DSA70000 Series Oscilloscope
DDR/2/3 Verification & Debug
Memory protocols & data

- Operations, Commands & Data
  - Memory initialization
    - Mode registers settings
  - Read & write data
    - Command sequences & timing
    - Data valid windows
    - Export read & write data to other tools
  - Time correlated memory operations
    - With oscilloscope waveforms
    - Other buses (QPI, FSB, PCI-Express 2, etc)

TLA7000 Series Logic Analyzers
with Nexus Memory Supports

Capture errors that cannot be captured or be seen by other logic analyzers with 20 ps high resolution timing
Logic Analyzer Probing
DDR/2/3 SDRAMs, DIMMs & SODIMMs

- Direct probing to circuit board
- Interposers
- NEXVu instrument DIMMs

240 pin unbuffered DDR3 DIMM NEXVu

Lowest probe loading in industry at <0.5pF
NEXVu: Instrumented DIMMs
JEDEC layout with measurements at the Memory IC pins

- Visibility of signals as seen by the memory chips
- Least signal integrity intrusive
- Logic analyzer connects above the normal DIMM height

Best measurement of the signal quality at the memory IC.

Signals are probed at the memory IC pins with an inner circuit board isolation resistors to reduce probe loading.
DDR3 240–pin UDIMM Signal Skew
No ECC

- Fly-by command/address/control bus with On-DIMM termination
- System level flight time compensation

Fly-by command/address/control bus

Read Data & Strobes

DQS0  DQS3  DQS4  DQS7

Tektronix®
Write Data Strobes Skew Analysis
Logic Analyzer MagniVu 20 ps (50 GS/s) timing resolution

1.27ns DQS6 to DQS0 skew captured with 20ps timing resolution

Oscilloscope timing performance on all logic analyzer channels all the time
Logic Analyzer Probes used by the Oscilloscope

iCapture: Logic Analyzer integrated digital/analog probe

TLA7016 & TLA7BB4s

Any Oscilloscope

TLA BNC Cables
DDR3 DQS2 Strobe Waveform

Amplitude problem with Read strobe from DIMM

Logic analyzer probes used by the oscilloscope
TriMode Probing for DSA/DPO70000 scopes
DDR memory validation wizard for DSA/DPO70000 series

Steps to completion:

1. Speed selection and Vref detection (automatic or manual)
2. Different types of measurements for different bursts
3. Chip Select Qualification to provide selective Read/Write Bursts
4. Detection of levels is automatic - or – customized
5. Threshold scaling
Measurements and configuration

- Compliance and analysis support
- Measurements on all edges and bursts
- JEDEC DDR measurements and serial data measurement library
Analog Validation of DDR memory

- Data Eye Diagram with Strobe information
- Quickly switch to DPOJET for powerful debug and analysis capabilities

- Complete Measurement Report
- Waveform screenshots, eye diagram, and detailed setup information
Mode Register Analysis
Only 4 MRS Commands Captured at Power-on

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<thead>
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<th>Sample</th>
<th>00000</th>
<th>00000</th>
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<th>00000</th>
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<td></td>
<td></td>
<td></td>
<td>0 ps</td>
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<td>02,827,215 us</td>
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</table>

SDRAM MRS2, MRS3, MRS1 & MRS0 configured by the memory controller at power-on & reset

Logic analyzer selective storage captures only useful information
State Acquisition
TLA7BB4 Data Valid Window: 200 mV, 240 ps (merged)

Eye diagram courtesy of Intel
Write Data 64-bits Analysis
Verify state write data groups with MagniVu timing data

<table>
<thead>
<tr>
<th>Sample</th>
<th>B_DDR3D_2B Address</th>
<th>B_DDR3D_2B Mnemonics</th>
<th>B_DDR3D_2B DataHi</th>
<th>B_DDR3D_2B DataLo</th>
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<tr>
<td>12</td>
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<td>DESL - IGNORE COMMAND</td>
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<td>11DA1</td>
<td>ACT - BANK ACTIVATE (SO#) Bank: 1</td>
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<td>14</td>
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<td>DESL - IGNORE COMMAND</td>
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<td>17</td>
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<td>18</td>
<td>162F8</td>
<td>WR - WRITE (SO#) Bank: 1</td>
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<td>WRITE DATA</td>
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<td>000000002</td>
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</table>
Selective Clocking Acquires More Useful Information

Notice Timestamp changes for DESL cycles not stored
Nexus Protocol Violation Software
DDR3/DDR2 Protocol Checking

- Summary/Statistical Info.
- Bus/TLA Memory Utilization
- Quickly display problem areas in Listing & Waveform windows
- Customizable timing parameters
- Export data
Memory System
Verification & Debug

- DDR/2/3 SDRAM
  - Initialization & mode register
  - Commands & read/write data
  - Waveforms
  - Protocol violation checking

- Selective clocking
  - Stores useful data in the TLA
  - Filters refresh & deselect cycles

- Pre-defined symbols for easy analysis & trigger setup

- Three simultaneous measurements through one probe
  - State acquisition
  - High-resolution 20 ps (50GS/s)

MagniVu timing with TLA7BB4
- Oscilloscope analog waveforms
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DDR2 Demo Setup

TLA7BB4, TLA7S16 & TLA7012 Logic Analyzer with second display

DDR2-533 & PCIe 2 development board
Direct probing DDR2-533 with two P6960 logic analyzer probes
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Digital Validation & Debug

Data Link Analysis
Digital validation & Debug

Receiver Test
Direct Synthesis

Compliance Testing

Serial Data Network & Link Analysis

Simulation

Signal Integrity
Eye and Jitter Analysis
Characterization & Validation

Transaction Layer

Data Link Layer

Logical Sub-block

Physical Layer

Electrical Sub-block

Tx + path + Rx
High Speed Digital Verification & Debug
Protocols, Data, Signal Quality & Circuit Board Trace Quality

- Memory Protocols & Data
  - TLA7000 Logic Analyzers

- Signal Quality
  - DPO/DSA70000 Series Oscilloscopes

- Circuit Board Trace Quality
  - CSA8200 Sampling Oscilloscopes
PCI Express Information

- Tektronix
  - www.tektronix.com/pci_express

- PCI Special Interest Group (PCI-SIG®)
  - www.pcisig.com

- PCI Express Test Procedures
  - www.pcisig.com/specifications/pciexpress/compliance/compliance_library
Memory Information

- Tektronix
  - www.tektronix.com/memory

- Nexus Technology
  - www.nexustechnology.com

- Memory Implementers Forum
  - www.memforum.org

- JEDEC
  - www.jedec.org
Thank You!

Contact your local Tektronix Account Manager for more information