DisplayPort™ 1.4 over Type-C Compliance Test Overview

What you need to know

eBOOK

Tektronix®

CONTENTS

DisplayPort Overview

DisplayPort (DP) is a newer standard originally developed to support the higher performance and flexibility requirements of personal computers. In addition to higher performance, it also provides a more robust and error-free digital A/V link. Because DisplayPort is packet based and leverages the signaling technology common in other modern high-speed data interfaces, it can be combined with other standards such as USB and Thunderbolt™.

DisplayPort™ is compatible with legacy display connections, making it the universal A/V video source connection. Connect your DisplayPort™ output to an existing HDMI™ TV or display using a simple and inexpensive DisplayPort™-to-HDMI™ adapter.

The next few pages will provide detailed information on test points, Transmitter (Tx) and Receiver (Rx) specifications, recommended DUT connections, calibration and test set-ups for the DisplayPort standard.

KEY FEATURES

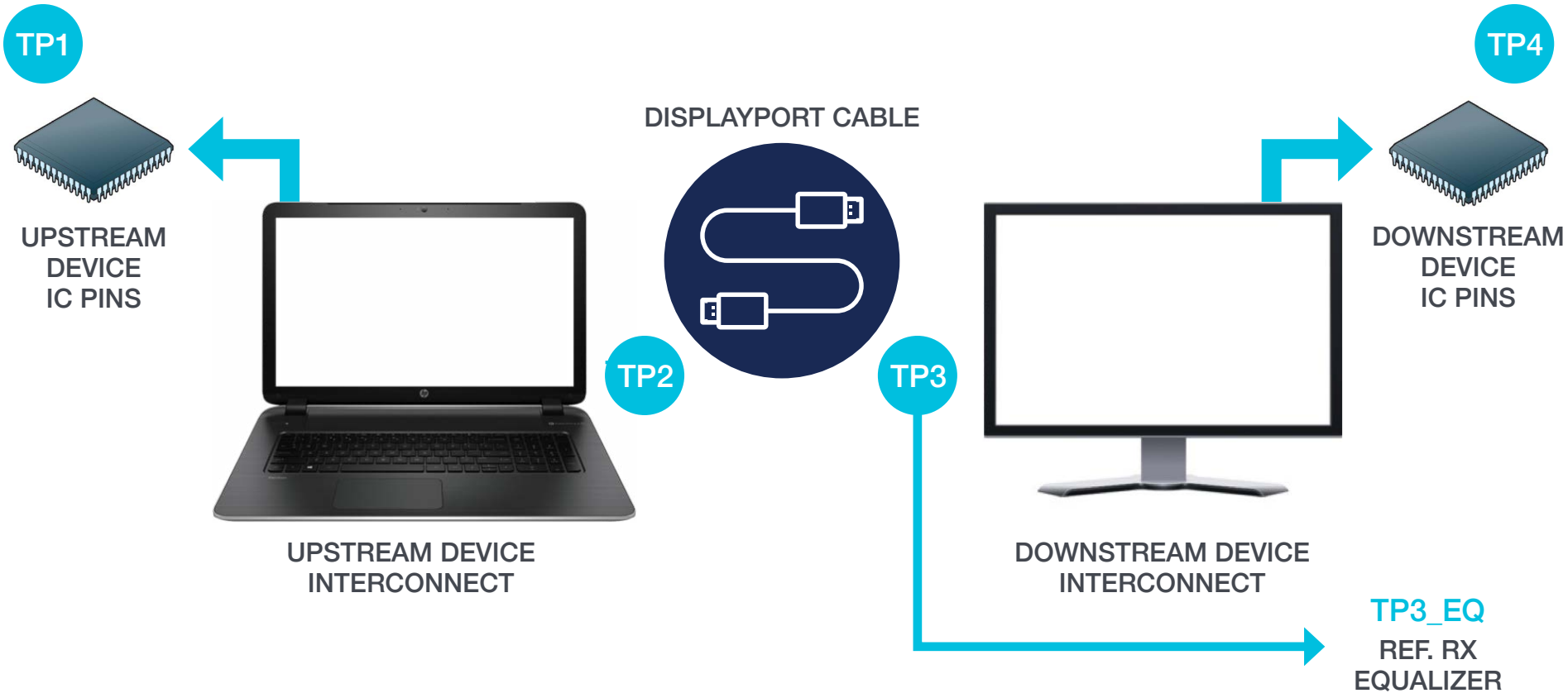
- 8K display and HDR support with the latest standard
- Multiple displays over a single connector
- Backward compatibility with HDMI, VGA, and DVI with simple adapters
- Supports HDMI™ 2.0 and previous versions
- Expanded capabilities to support latest audio trends and camera interfaces

ADVANTAGES

- Royalty Free
- MST
- 8K compress video with DP1.4
- DisplayPort to HDMI, DVI, VGA adapters
- Simpler cables
- Type-C connectivity

Test Point Definitions

TP1: at the pins of the transmitter device.
TP2: at the DP connector on the Source device.
TP3: at the DP connector on the Sink device.
TP3_EQ: TP3 using a defined cable model with equalizer applied.
TP4: at the pins of a receiving device.



Transmitter (Tx) Test Conditions

DisplayPort 1.4 specification introduces a new data rate - HBR3 and increases the highest operating data rate to 8.1Gbps. With design margins becoming more stringent, the DP 1.4 compliance tests undergo changes which are indicated in the table below for quick reference.

Test ID	RBR (1.62Gb/s)	HBR (2.7Gb/s)	HBR2 (5.4Gb/s)	HBR3 (8.1Gb/s)
3.1 Eye Diagram Test				
Test Point	TP2	TP2	TP3_Eq	TP3_Eq
Pattern	PRBS-7	PRBS-7	CP2520	CP2520 Pattern 3 (TPS4)
Swing/Pre-Emphasis /PostCursor2	2/0/0	2/0/0	Provided by DUT Owner for Passing Condition	Provided by DUT Owner for Passing Condition
SW Channel	NA	NA	Zero Length & Worst Case	Zero Length & Worst Case
SSC	ON - If DUT Supports	ON - If DUT Supports	ON - If DUT Supports	ON - If DUT Supports
Crosstalk Eye Limit Correction Values: Eye Height, Eye Width	NA	NA	14mV, 7ps	12mV, 5ps
3.2 Non-Pre-Emphasis Level				
Test Point	TP2	TP2	TP2	TP2
Pattern	PRBS-7	PRBS-7	80 Bit PLTPAT	80 Bit PLTPAT
Swing/Pre-Emphasis /PostCursor2	All/0/0	All/0/0	All/0/0	All/0/0
SSC	On if DUT Supports	On if DUT Supports	On if DUT Supports	On if DUT Supports
CTLE	No	No	Yes	Yes
DFE	No	No	No	Yes
3.3 Pre-Emphasis Level Maximum Differential Pk-Pk Output Voltage				
Test Point	TP2	TP2	TP2	TP2
Pattern	PRBS-7	PRBS-7	80 Bit PLTPAT	80 Bit PLTPAT
Swing/Pre-Emphasis /PostCursor2	All/All/0	All/All/0	All/All/0	All/All/0
SSC	On if DUT Supports	On if DUT Supports	On if DUT Supports	On if DUT Supports
3.4 Inter-pair Skew				
Bit Rate	Highest Bit Rate Supported			
Test Point	TP2			
Pattern	PRBS-7 or DUT dependent custom pattern			
Swing/Pre-Emphasis /PostCursor2	2/0/0			
SSC	On if DUT Supports	On if DUT Supports	On if DUT Supports	On if DUT Supports
3.11 Non-ISI Jitter				
Test Point	TP2	TP2	NA	NA
Pattern	PRBS-7	PRBS-7	NA	NA
Swing/Pre-Emphasis /PostCursor2	All/All/0	All/All/0	NA	NA
SSC	On and Off if DUT Supports	On and Off if DUT Supports	NA	NA

Transmitter (Tx) Test Conditions – continued

Test ID	RBR (1.62Gb/s)	HBR (2.7Gb/s)	HBR2 (5.4Gb/s)	HBR3 (8.1Gb/s)
3.12.1 Total (TJ) and Deterministic (DJ) Jitter				
Test Point	TP2	TP2	TP3_Eq	TP3_Eq
Pattern	PRBS-7	PRBS-7	2520 Bit HBR2 Compliance Eye Pattern	2520 Bit HBR3 Compliance Eye Pattern
Swing/Pre-Emphasis /PostCursor2	2/0/0	2/0/0	Provided by DUT Owner for Passing Condition	Provided by DUT Owner for Passing Condition
SW Channel	NA	NA	0 Length & Worst Case	0 Length & Worst Case
SSC	On and Off if DUT Supports	On and Off if DUT Supports	On and Off if DUT Supports	On and Off if DUT Supports
3.12.2 HBR2/HBR3 D10.2 TJ/RJ/DJ				
Test Point	NA	NA	TP3_eq	TP3_eq
Pattern	NA	NA	D10.2	D10.2
Swing/Pre-Emphasis /PostCursor2	NA	NA	Same Setting as Passing Eye/Jitter	Same Setting as Passing Eye/Jitter
SW Channel	NA	NA	0 Length & Worst Case	0 Length & Worst Case
SSC	NA	NA	On and Off if DUT Supports	On and Off if DUT Supports
CTLE	No	No	Yes	Yes
DFE	No	No	No	No
3.14 Main Link Frequency				
Test Point	TP2	TP2	TP2	TP2
Pattern	D10.2	D10.2	D10.2	D10.2
Swing/Pre-Emphasis /PostCursor2	2/0/0	2/0/0	2/0/0	2/0/0
SSC	On and Off if DUT Supports	On and Off if DUT Supports	On and Off if DUT Supports	On and Off if DUT Supports
3.15 SSC Modulation Frequency **3.16 SSC Modulation Deviation**	NA if SSC not supported	NA if SSC not supported	NA if SSC not supported	NA if SSC not supported
Test Point	TP2	TP2	TP3_Eq	TP3_Eq
Pattern	D10.2	D10.2	D10.2	D10.2
Swing/Pre-Emphasis /PostCursor2	2/0/0	2/0/0	2/0/0	2/0/0
SSC	On	On	On	On
3.18 Dual Mode TMDS Clock **3.19 Dual Mode Eye Diagram**				
Test Point	TP2			
Pattern	TMDS			
TMDS Clock Rate	Maximum TMDS Frequency Supported			

Recommended DUT Connections

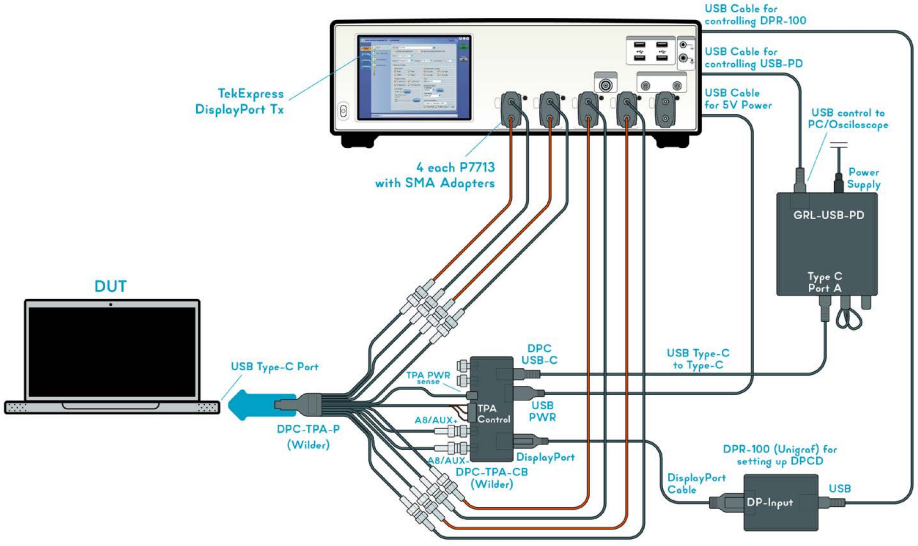
CONNECTION FOR DISPLAYPORT TYPE-C TESTING

The diagram to the right details the connection setup for DisplayPort Type-C testing. The setup requires a Alt-mode controller, DPR-100 and a Type-C fixture.

The table below outlines how data lanes are mapped to oscilloscope channels.

Oscilloscope Channel	Probe connection	Wilder Fixture pins
Channel 1	Channel 1 +	RX2+(USB SuperSpeed, Receiver 2 Pos/A11, Blue)
	Channel 1-	RX2-(USB SuperSpeed, Receiver 2 Neg/A10, Blue)
Channel 2	Channel 1 +	TX2+(USB SuperSpeed, Transmit 2 Pos/B2, Yellow)
	Channel 1-	TX2-(USB SuperSpeed, Transmit 2 Neg/B3, Yellow)
Channel 3	Channel 1 +	TX1+(USB SuperSpeed, Transmit 1 Pos/A2, White)
	Channel 1-	TX1-(USB SuperSpeed, Transmit 1 Neg/A3, White)
Channel 4	Channel 1 +	RX1+(USB SuperSpeed, Transmit 2 Pos/B11, Red)
	Channel 1-	RX1-(USB SuperSpeed, Transmit 2 Neg/B10, Red)

DISPLAYPORT TYPE-C TRANSMITTER TESTING SETUP



Recommended DUT Connections – continued

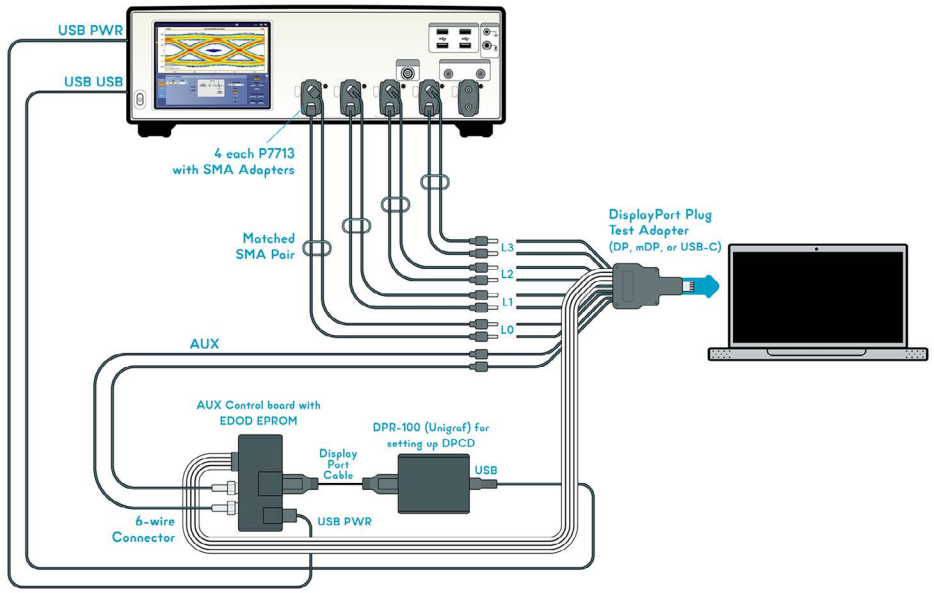
CONNECTION FOR STANDARD DISPLAYPORT TESTING

The connection diagram to the right details Standard DisplayPort Transmitter testing. The setup requires DPR-100 and a standard DisplayPort fixture fixture.

The table below shows how the data lanes are mapped to oscilloscope channels. The colors for the wilder fixture pins indicates the lanes on the fixture.

Oscilloscope Channel	Probe connection	Wilder Fixture pins
Channel 1	Channel 1 +	T0_P/R3_N – Positive White
	Channel 1-	T0_N/R3_P – Negative White
Channel 2	Channel 1 +	T1_P/R2_N – Positive Red
	Channel 1-	T1_N/R2_P – Negative Red
Channel 3	Channel 1 +	T2_P/R1_N – Positive Yellow
	Channel 1-	T2_N/R1_P – Negative Yellow
Channel 4	Channel 1 +	T3_P/R0_N – Positive Blue
	Channel 1-	T3_N/R0_P – Negative Blue

STANDARD DISPLAYPORT TRANSMITTER TESTING SETUP



Receiver Test Inputs

DisplayPort receiver testing involves calibration of jitter parameters before Jitter Tolerance (JTOL) testing. The CTS describes a calibration table for each data rate (RBR, HBR, HBR2 and HBR3). At each value of fixed SJ, the RJ is swept to arrive at a target TJ value.

JITTER COMPONENT SETTINGS

RBR

f(SJ) [MHz]	TJ(JTRBRrx) [mUI]	ISI [mUI]	RJ(RMS) [mUI]	Approximate SJ [mUI]
2	1648	570	8.1	981
10	778	570	8.1	111
20	747	570	8.1	80

HBR

f(SJ) [MHz]	TJ(JTHBRrx) [mUI]	ISI [mUI]	RJ(RMS) [mUI]	Approximate SJ_{SWEEP} [mUI]
2	1227	161	13.5	904
10	548	161	13.5	225
20	505	161	13.5	182
100	491	161	13.5	168

HBR2

f(SJ) [MHz]	TJ(JTHBR2rx) [mUI]	ISI [mUI]	RJ(RMS) [mUI]	Approximate SJ_{SWEEP} [mUI]	SJ_{FIXED} @ 297MHz [mUI]
2	1026	220	16.7	505	80
10	636	220	16.7	116	80
20	624	220	16.7	104	80
100	620	220	16.7	100	80

HBR3

f(SJ) [MHz]	TJ(JTHBR2rx) [mUI]	ISI [mUI]	RJ(RMS) [mUI]	Approximate SJ_{SWEEP} [mUI]	SJ_{FIXED} @ 297MHz [mUI]
2	620	240	13	1013	130
10	620	240	13	137	130
20	620	240	13	109	130
100	620	240	13	100	130

Receiver Test Inputs – continued

TEST PARAMETERS FOR BER MEASUREMENT

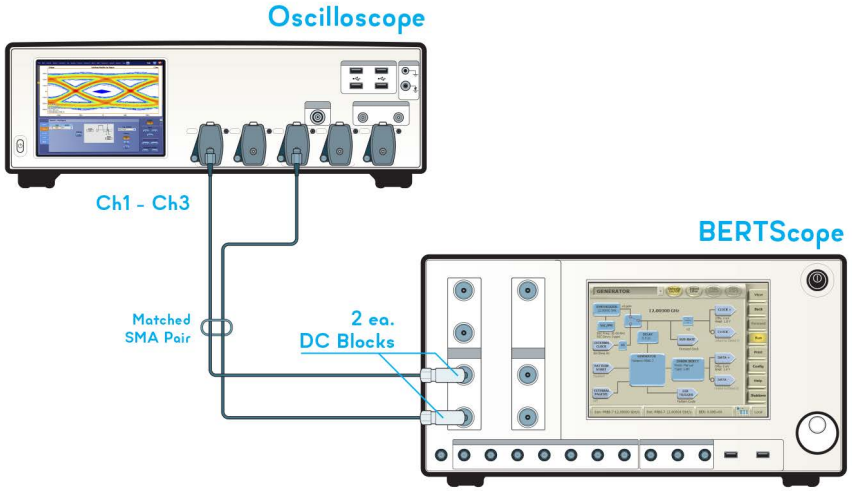
The table describes the number of seconds the stressed signal is outputted on a Bit Error Rate Tester into the DUT and the allowable number of bit errors at each jitter frequency. The DUT must allow access to DPCD registers in order for test setup to be able to read the bit error value.

Data Rate	Jitter Frequency	Number of Bits	Max Number of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR3 HBR2 HBR RBR	2MHz	10^{12}	1000	HBR3 = 123s HBR2 = 185s HBR = 370s RBR = 620s	0
HBR3 HBR2 HBR RBR	10MHz	10^{11}	100	HBR3 = 13s HBR2 = 19s HBR = 37s RBR = 62s	+350ppm +350ppm +350ppm
HBR3 HBR2 HBR RBR	20MHz	10^{11}	100	HBR3 = 13s HBR2 = 19s HBR = 37s RBR = 62s	0
HBR3 HBR2 HBR	100MHz	10^{11}	100	HBR3 = 13s HBR2 = 19s HBR = 37s	0
To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 1011 bits at HBR = 370ps/UI * 1011 UI = 37 seconds)					

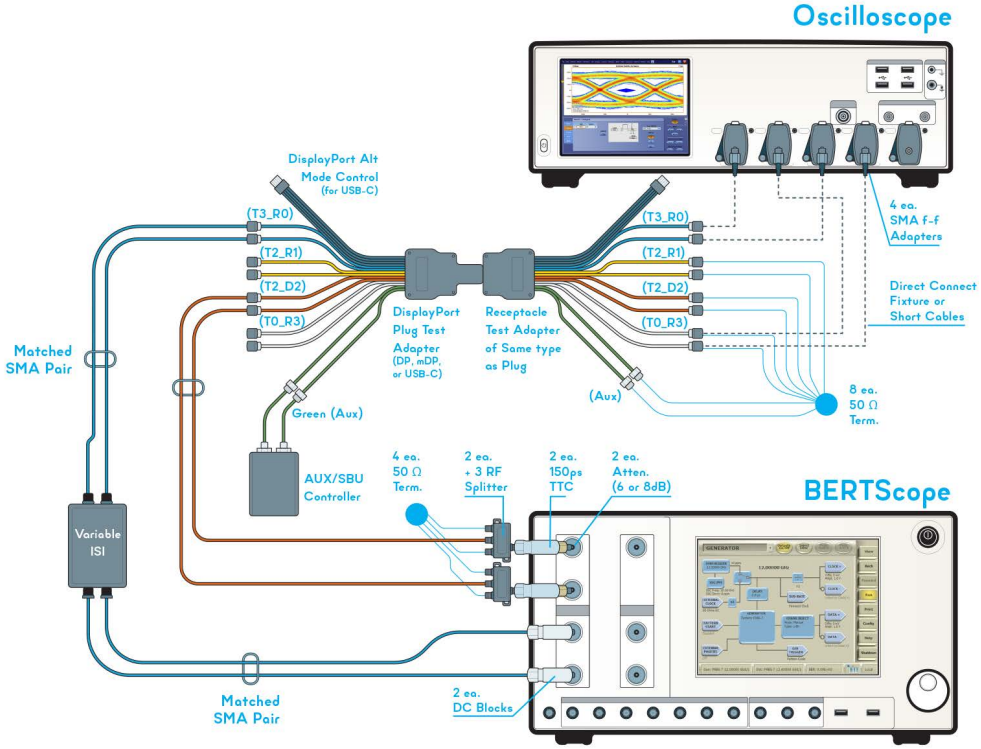
Calibration Setup for DisplayPort 1.4 Receiver (Rx)

Calibration is the first step in Receiver testing. The following DUT parameters are calibrated in the first step of calibration : ISI, RJ, SJ Fixed, SJ Sweep, Crosstalk and Eye Height. The calibration setup for TP1 and TP2 are different as shown in the setup below. Refer to **Tektronix MOI** for detailed test description.

CALIBRATION SETUP AT TP1



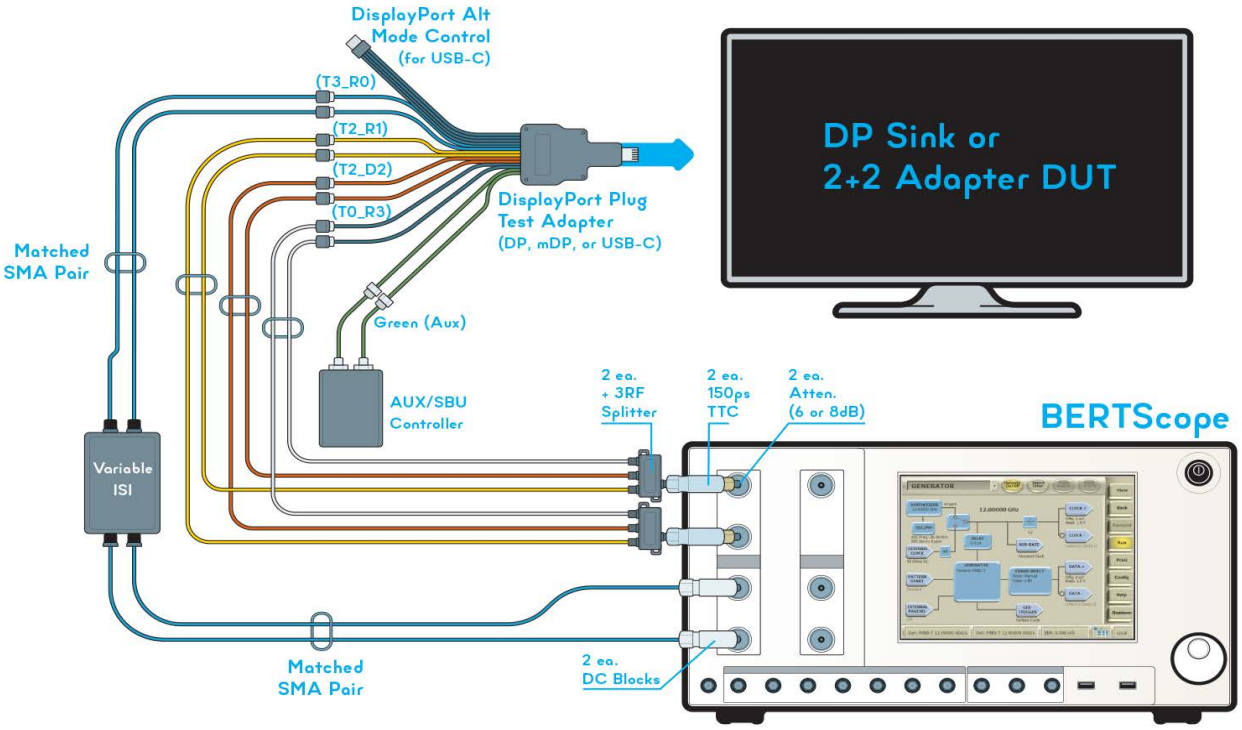
CALIBRATION SETUP AT TP2/TP3



Test Setup for DisplayPort 1.4 Receiver (Rx)

The BERTScope outputs stressed pattern as defined in specification with RJ, SJ, and ISI jitter injected. The error counter is initially cleared. The sink compliance tests are run for a specified time. If the Sink DUT supports aux communication, then after the specified test time, the error counter is read through by reading sink DPCD register.

DUT JITTER TOLERANCE COMPLIANCE TEST SETUP



Summary

As DisplayPort speed becomes faster and more complex with the emergence of the DP 1.4 standard, engineers are faced with new design challenges, shorter time-to-market windows, new standards specifications to understand and apply, and new compliance testing requirements.

Before you tackle testing and debug of your standard DisplayPort or Type-C DisplayPort device, here are some key questions to ask:

- How will you verify that actual transmitter or receiver margin meets design goals?
- How will you debug and perform repeatability testing when there are measurement failures?
- How will you test your device beyond compliance limits?
- Do test times matter to you in DisplayPort testing?
- Do you have the tools to automatically and quickly perform compliance testing at various corner conditions?
- Do you have the tools and expertise to configure, optimize and calibrate your entire test set up?
- Do you perform elaborate data mining on the DisplayPort results?

—

Don't waste your time.

Make sure your device passes the first time.

Historically, when a new generation of DisplayPort devices enters compliance testing, a significant percentage of them fail their first plugfest for PHY and link training compliance. Thus, it is vital to have a comprehensive test equipment and software solution in place prior to workshop testing. Tektronix's DisplayPort test and debug solution can easily guide you through compliance testing and debug before a plugfest to ensure your design meets the standards requirements with a high degree of confidence.

Need help in answering these questions?

Your Tektronix Account Manager will be happy to help, just give them a call.

To contact any of our worldwide offices for assistance please refer to the telephone numbers on the next page.

Find more valuable resources at TEK.COM

DisplayPortTM and the DisplayPortTM logo are trademarks owned by the Video Electronics Standards Association (VESA®) in the United States and other countries.

Tektronix products are covered by U.S. and foreign patents, issued and pending. Information in this publication supersedes that in all previously published material. Specification and price change privileges reserved. TEKTRONIX and TEK are registered trademarks of Tektronix, Inc. All other trade names referenced are the service marks, trademarks or registered trademarks of their respective companies.

11/2018 61W-61237-0

CONTACT INFORMATION:

Australia 1 800 709 465
Austria 00800 2255 4835
Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777
Belgium 00800 2255 4835
Brazil +55 (11) 3759 7627
Canada 1 800 833 9200
Central East Europe / Baltics +41 52 675 3777
Central Europe / Greece +41 52 675 3777
Denmark +45 80 88 1401
Finland +41 52 675 3777
France 00800 2255 4835
Germany 00800 2255 4835
Hong Kong 400 820 5835
India 000 800 650 1835
Indonesia 007 803 601 5249
Italy 00800 2255 4835
Japan 81 (3) 6714 3086
Luxembourg +41 52 675 3777
Malaysia 1 800 22 55835
Mexico, Central/South America and Caribbean 52 (55) 56 04 50 90
Middle East, Asia, and North Africa +41 52 675 3777
The Netherlands 00800 2255 4835
New Zealand 0800 800 238
Norway 800 16098
People's Republic of China 400 820 5835
Philippines 1 800 1601 0077
Poland +41 52 675 3777
Portugal 80 08 12370
Republic of Korea +82 2 6917 5000
Russia / CIS +7 (495) 6647564
Singapore 800 6011 473
South Africa +41 52 675 3777
Spain 00800 2255 4835
Sweden 00800 2255 4835
Switzerland 00800 2255 4835
Taiwan 886 (2) 2656 6688
Thailand 1 800 011 931
United Kingdom / Ireland 00800 2255 4835
USA 1 800 833 9200
Vietnam 12060128

Rev. 020916

Tektronix®