DDR Memory and Interface Design Trends

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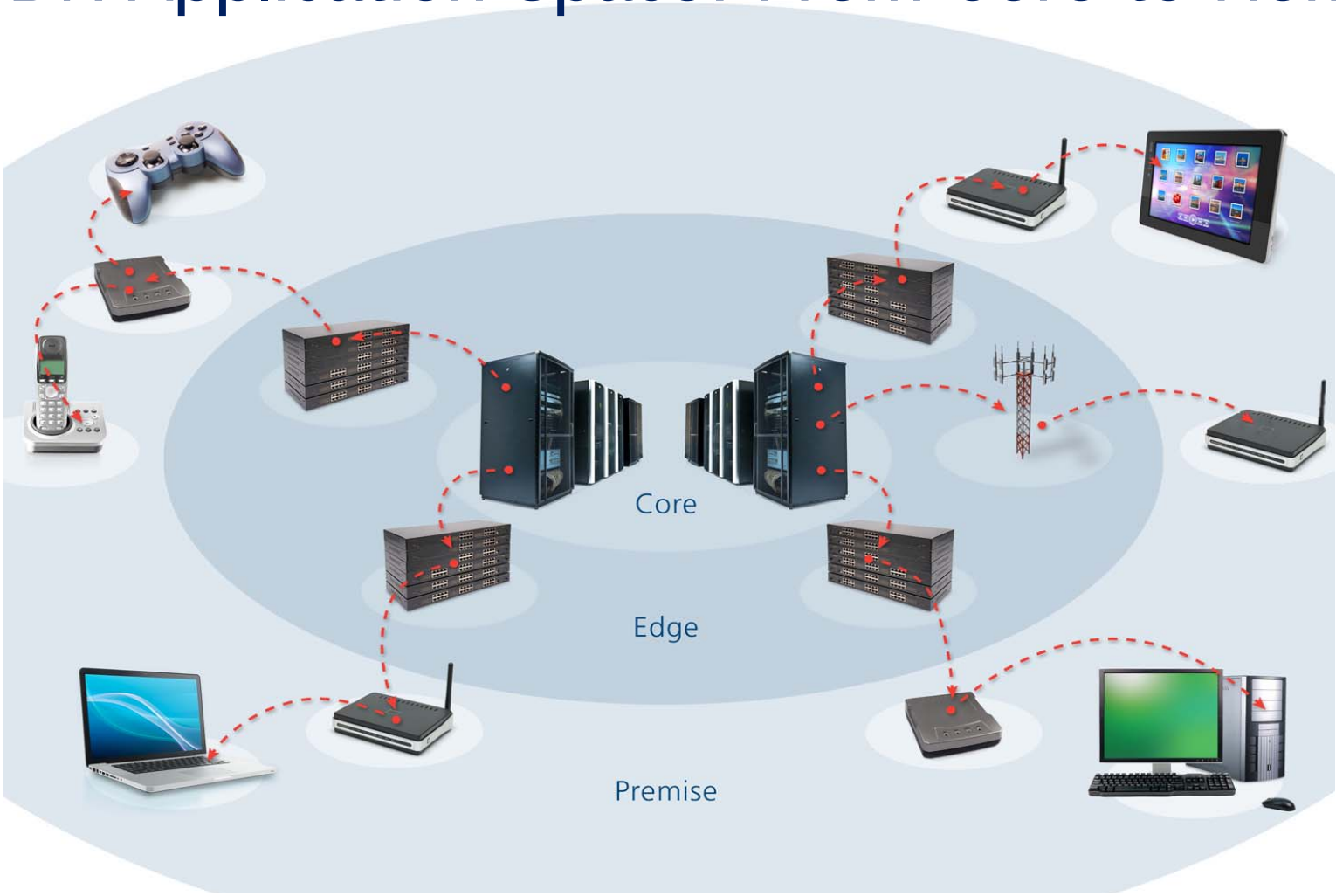
Agenda

- Variety in DDR Memory Types
- DDR Memory Trends
- Selecting DDR Memory
- DDR Memory Interface Design Considerations

Variety in DDR Memory Types

DDR Application Space: From Core to Home



- Server, Networking, and Storage Convergence: Companies and equipment are crossing segment borders
- Consumer and Personal Computing Convergence: Game consoles, PCs, and tablets—always on and connected
- Cloud Delivery: Software, information, and computing power—convenience and access for consumer devices

Value of DDR Memory from Market Eye

- Good Balance of High Density/Low Cost and Small Package/Fast Speed/Low Power
  - Flash offers high density and nonvolatility, but very slow write speeds
  - SRAM offers low standby power, high-speed operation, and requires no refresh, but costs increase due to large die sizes
  - Flash and SRAM have relatively large packages due to many address and data pins

Variety in DDR Memory Types

- DDR Series (Standard DRAM)
  - SDRAM/DDR/DDR2/DDR3/(DDR4)
- Mobile LPDRAM (Low Power – for Cell Phones)
  - LPSDRAM/LPDDR/LPDDR2/(LPDDR3)
- Special Purpose
  - Reduced latency DRAM (RLDRAM® Memory); short ^{t}RC for networking
  - Hybrid memory cube (HMC); super-high bandwidth
  - Wide I/O; low power, high bandwidth
- Other DRAM
  - GDDR3/GDDR5 (graphics cards)
  - FCRAM (game consoles)
  - XDR (game consoles)

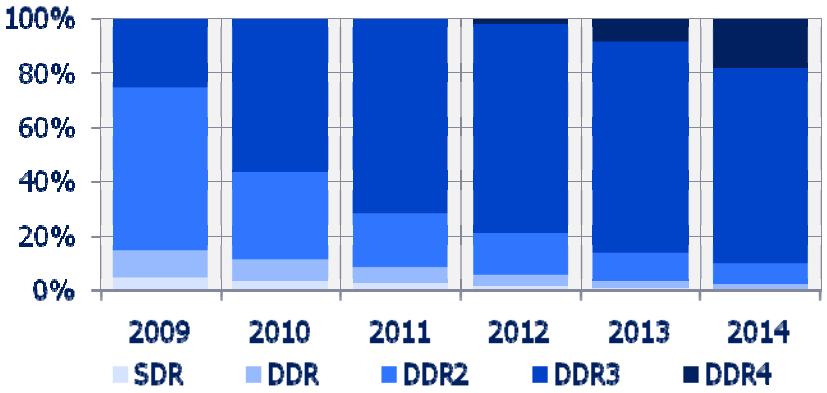
DDR Memory Spec Comparison

DRAM Type	Max Bandwidth	Data Bus Width	Operating Frequency	Supply Voltage	I/O Voltage
SDR	166 Mb/s	x4/x8/x16	0–166 MHz	3.3V	3.3V
DDR	400 Mbps	x4/x8/x16	83–200 MHz	2.5V	2.5V
DDR2	1066 Mb/s	x4/x8/x16	125–533 MHz	1.8V	1.8V
DDR3	2133 Mb/s	x4/x8/x16/(x32)	200–1066 MHz	1.5V/1.35V	1.5V/1.35V
DDR4	Mb/s	x4/x8/x16	400–1600 MHz	1.2V & 2.5V	1.2V
Mobile LPDRAM	133 Mb/s	x16/x32	0–133 MHz	1.8V	1.8V/1.2V
LPDDR	400 Mb/s	x16/x32	0–166 MHz	1.8V	1.8V/1.2V
LPDDR2	1066 Mb/s	x8/x16/x32	10–533 MHz	1.2V & 1.8V	1.2V
LPDDR3	2133 Mb/s	x8/x16/x32	200–1066 MHz	1.2V & 1.8V	1.0V
GDDR3	1.6 Gb/s	x32	200–800 MHz	1.8V/2.0V	1.8V/2.0V
GDDR5	5.0 Gb/s	x32	200–800 MHz	1.8V/2.0V	1.8V/2.0V
RLDRAM 2	1066 Mb/s	x18/x36	175–533 MHz	1.8V & 2.5V	1.8V/1.5V
RLDRAM 3	2133 Mb/s	x18/x36	TBD–1066 MHz	1.35V & 2.5V	1.2V

Leading with New Interfaces: **DDR4**

Optimized for Power and Performance

DDR4 Market Introduction



Potential DDR4 Lead Applications

Servers

- Best solution for high-density DIMMs
- Significant power reduction

Notebooks

- Further power savings due to 1.2V supply
- Increased performance to address future applications

Tablet PCs

- Ideal application for low-power features
- Fast adoption due to the variety of controller vendors

Source: Gartner 4Q'10

The Next Major Standard

DDR4 introduction expected in 2012

- Main interest: Power-sensitive applications

Key improvements over DDR3

- Higher bandwidth: Up to 3.2 Gb/s
- Power consumption: 1.2V offers significant improvement
- High density: 128GB in single-stack, single-load packages

Ideal memory for a variety of applications

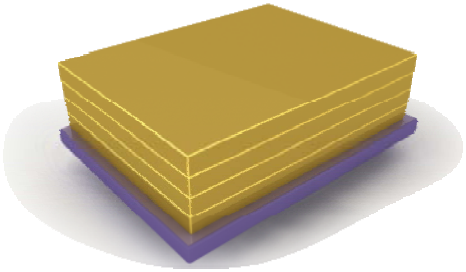
- Servers: Ideal technology for power and performance benefits
- Tablet PCs: Important low-voltage benefits
- Notebooks: Fast introduction expected

Commitment

Micron is fully committed to DDR4 introduction

Micron's Hybrid Memory Cube

Worldwide Announcement – February 11, 2011



Micron's Newest Memory Innovation

We've combined fast logic process technology and advanced DRAM design to create an entirely new category we're calling **Hybrid Memory Cube (HMC)** technology.
The end result is a high-bandwidth, high-density, low-energy memory system that's unlike anything on the market today.

The Real Difference is in the Cube

HMC will provide a revolutionary performance shift that will enrich next-generation networking and enable exaflop-scale supercomputing:

- **Increased Bandwidth** — Today, HMC prototypes are exhibiting 10X the bandwidth of a DDR3-1600 module. The performance gap will widen.
- **Power Reductions** — HMC is exponentially more efficient than current memory, using only a fraction of the energy per bit consumed in traditional solutions.
- **Smaller Physical Systems** — HMC's stacked architecture uses almost 90% less space than today's RDIMMs, enabling many different topology implementations.

Introducing: **RLDRAM3**

The best low-latency DRAM gets better

- Unprecedented performance for high-end networking
- Comparable to SRAM access time at superior cost and density
- Easy transition path from RL2 platforms
- High interest from customers and key enablers

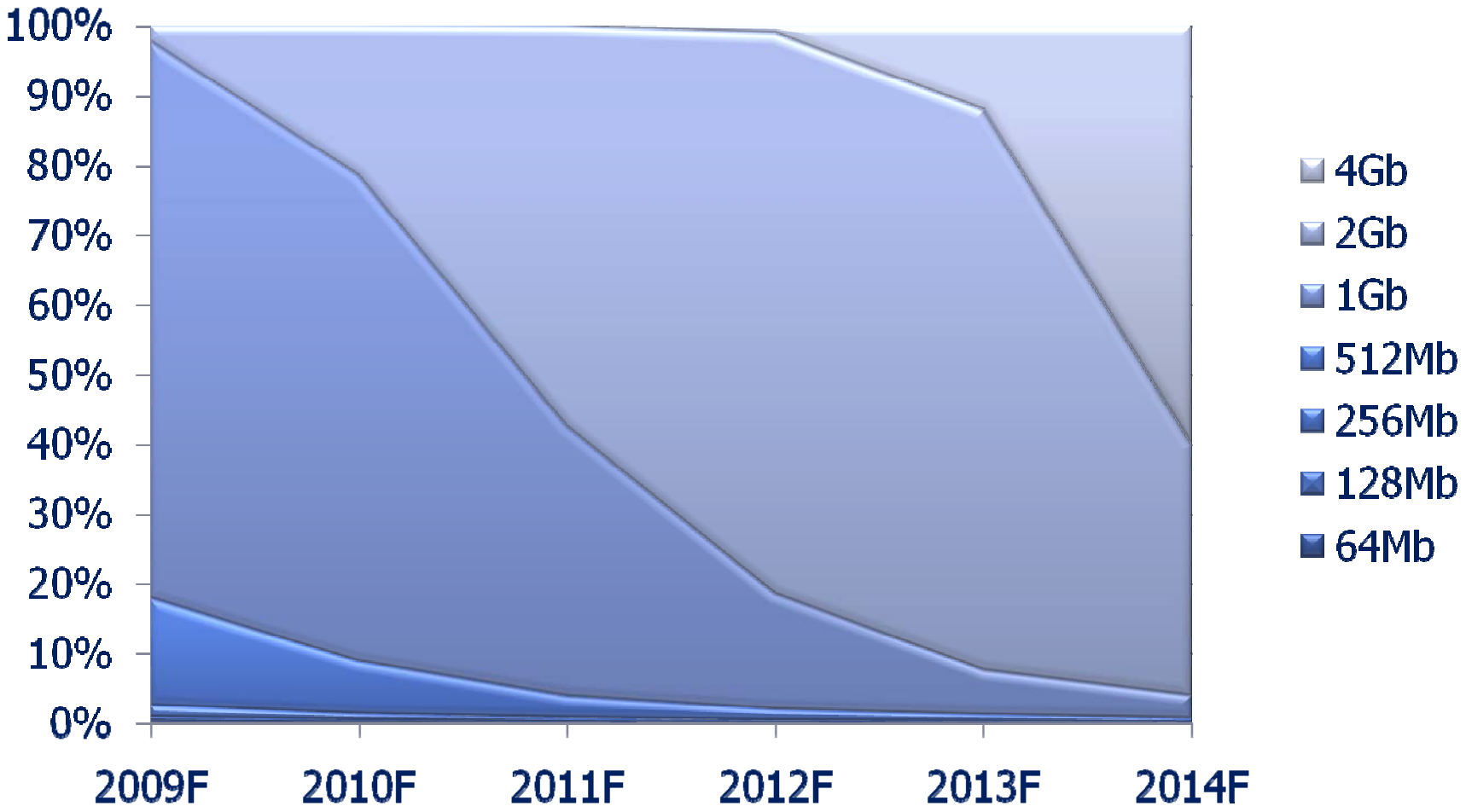
Extending success of RLDRAM 2 with RLDRAM 3

- Improved performance:
  - Random access time down to 10ns WRITE and 2.5ns READ
  - Doubled sustainable bandwidth of 2133 Gb/s
  - Power efficiency and high memory density
- Memory densities of 576Mb and 1.1Gb

DDR Memory Trends

DRAM Density Trends

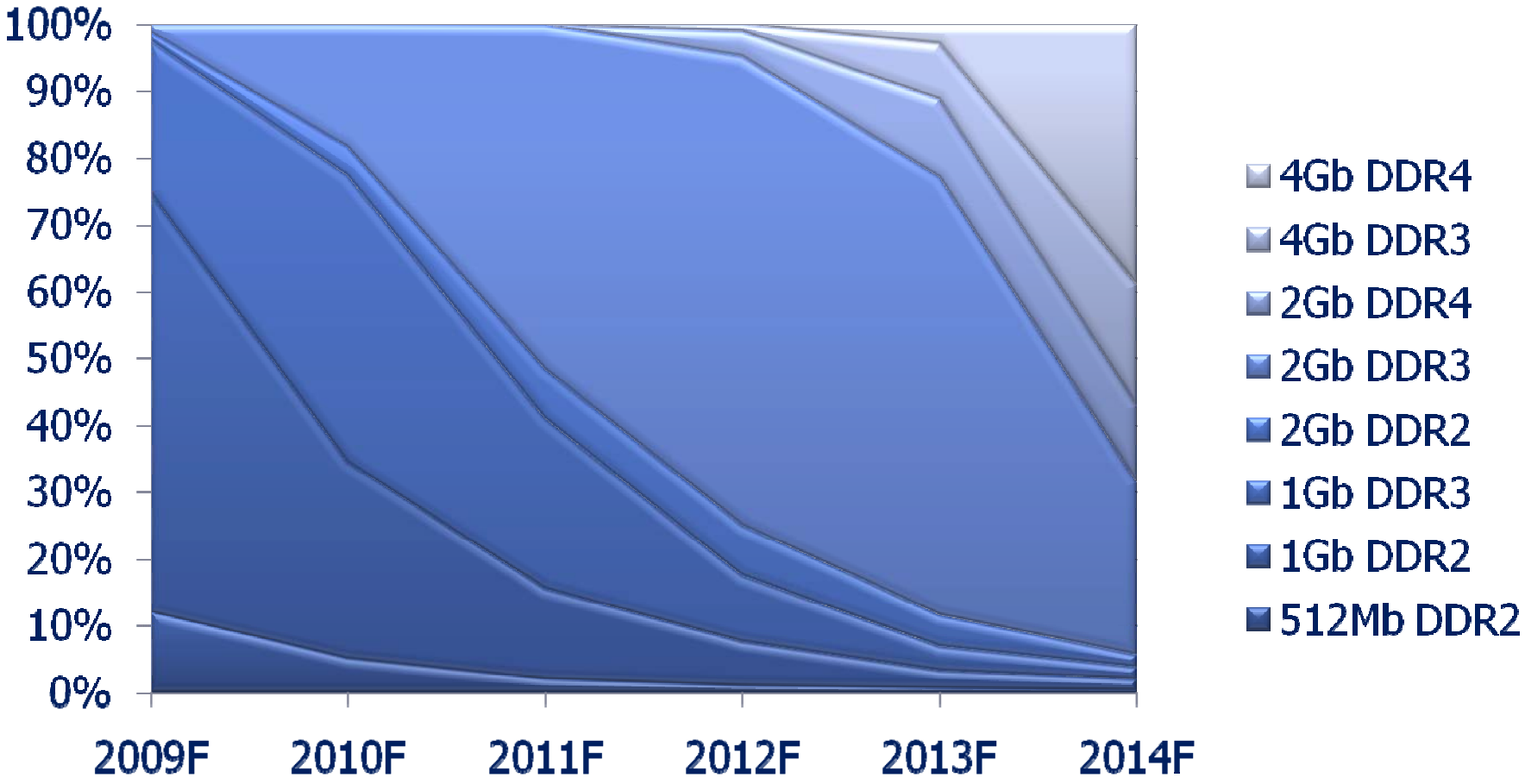
All Technologies



Source: Gartner 1Q10

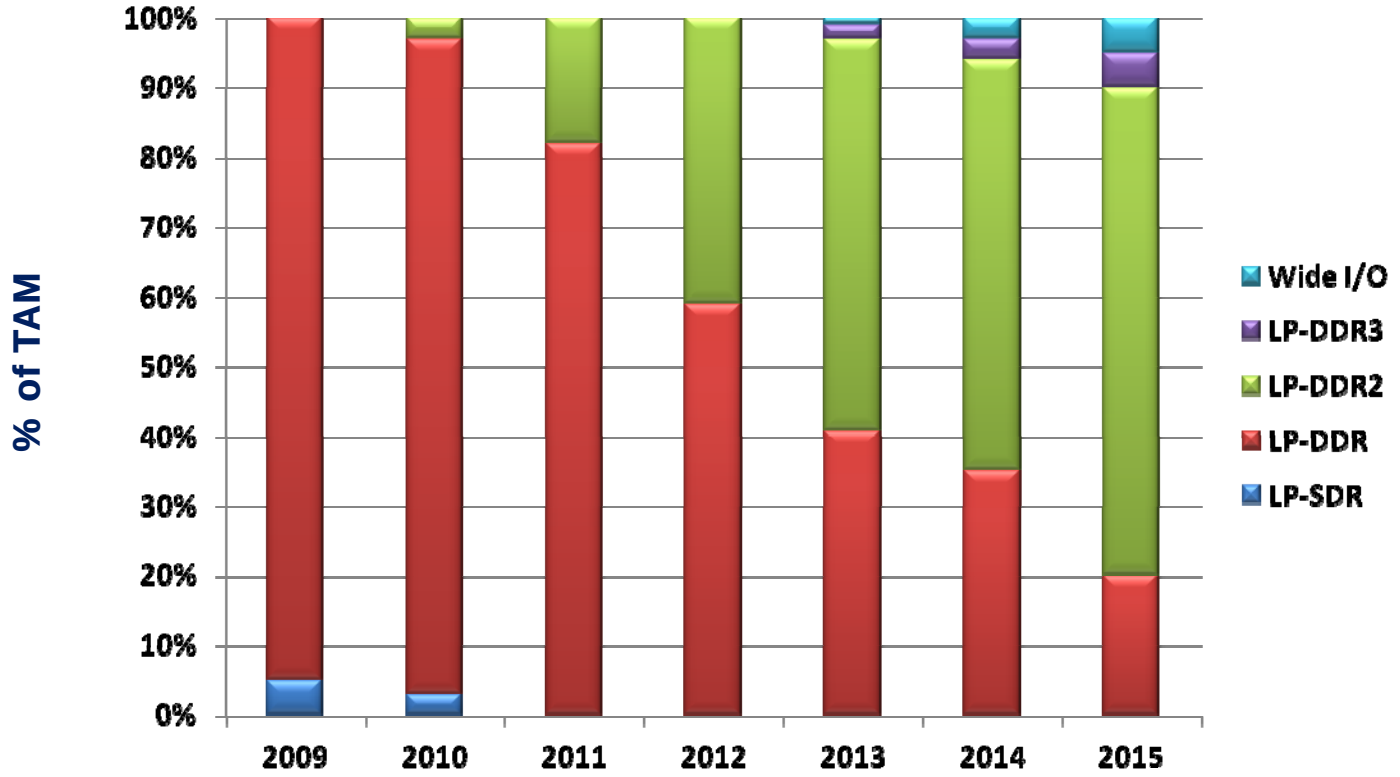
DRAM Technology Trends

Major Products



Source: Gartner 1Q10

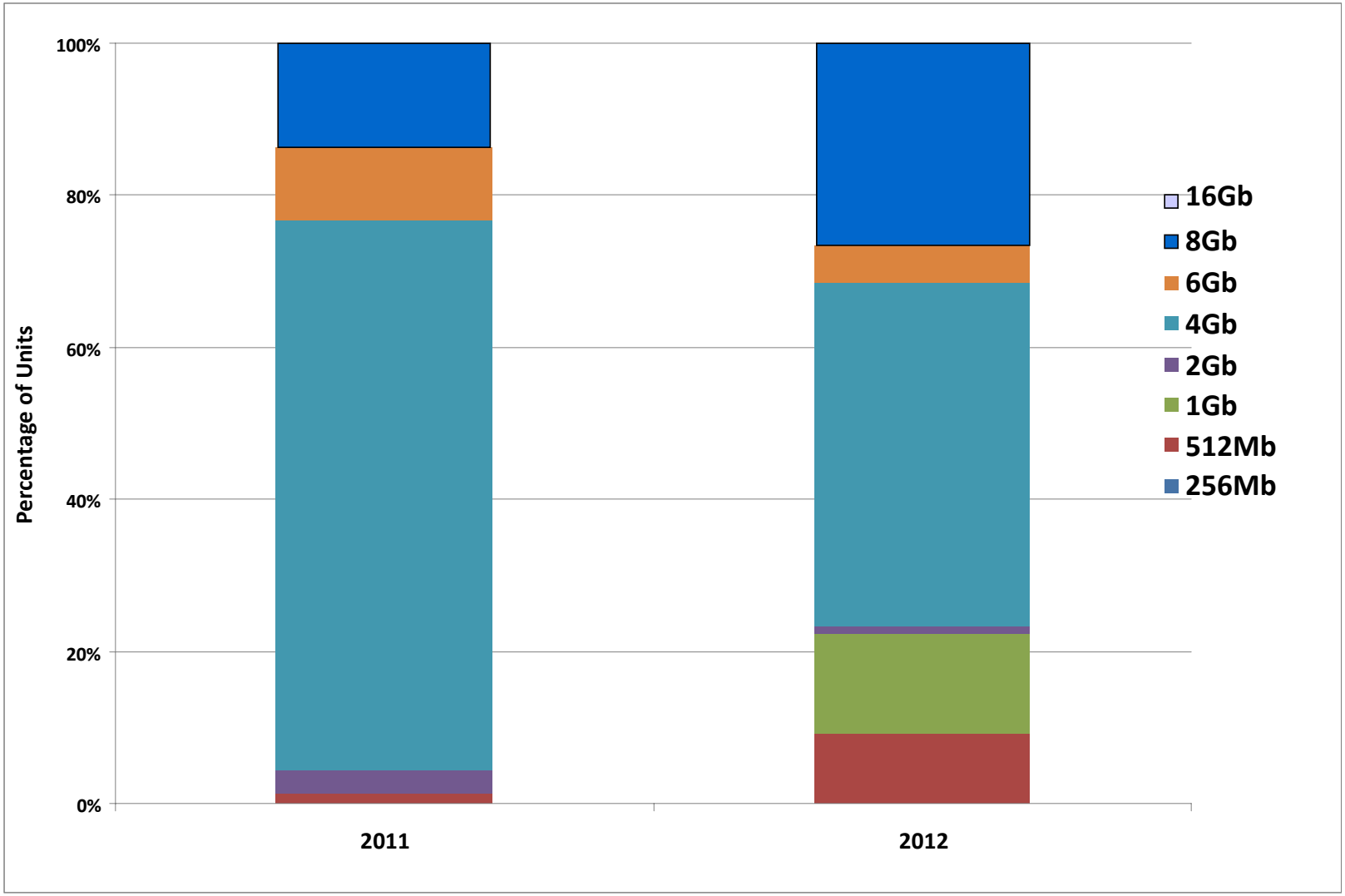
LPDRAM Technology Trends



- Increased LPDDR2 adoption starting in 2011
- Wide I/O and LPDDR3 introduction planned for 2013

Source: Micron Marketing

LPDDR2 Density Trends – Handsets



Source: Micron Marketing

Selecting DDR Memory

How to Select DDR Memory

System Requirements

- Bandwidth
- Density
- Power consumption
- Size/board area
- Cost

Clarify the System Requirements First!

DDR Selection

- Data bus width
- Operating frequency
- Technology
  - Interface
  - Voltage
  - Operating mode
- Package
- Market trends

DDR Memory Recommendations

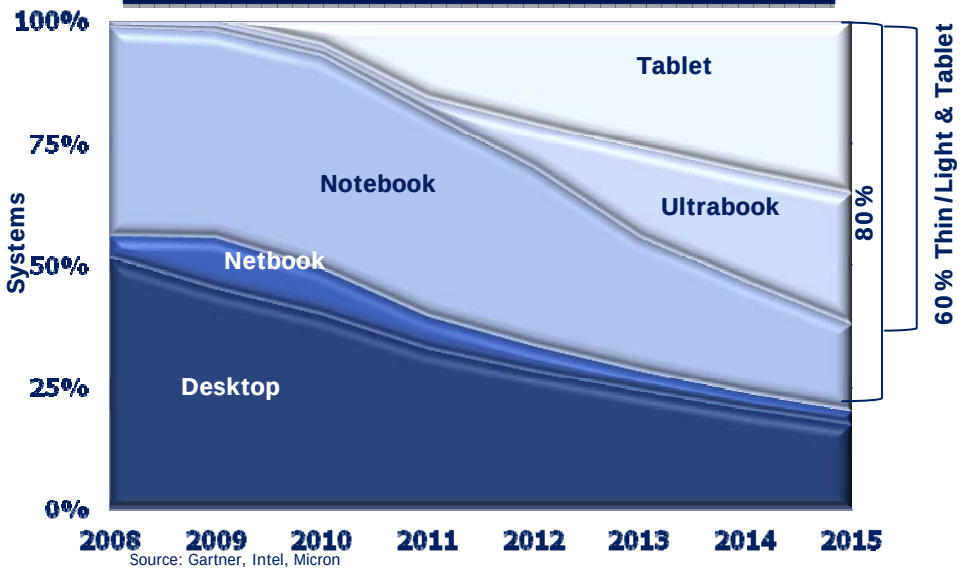
- Commodity DDR: DDR3 in 2011–12
  - Cost-effective (density/performance) solution for most applications
  - Legacy DDR (SDRAM, DDR, DDR2) for low-density/low-speed applications; consider market availability and pricing
- Low-Power DDR: LPDDR/LPDDR2 in 2011–12
  - For highly power-sensitive applications
- Special Purpose: RLDRAM, HMC
  - For extensive, performance-driven applications (latency/bandwidth)

LPDRAM and Commodity DRAM Serving Different Market Requirements

	LPDRAM	Commodity DRAM
Performance	x32 enables systems to support high bandwidth in point-to-point applications.	x4, x8, and x16 are lower cost and support higher-density configurations. High performance supported through high clock rate, which adds power.
Form factor	Edge bond pads allow for stacked die in MCP and PoP packaging, enabling compact form factors.	Center bond pads offer highest performance and lowest cost.
DRAM power	Ultra-low standby power enabled by on-die power management and long refresh rates.	I_{DD} specifications are geared toward moderate standby power, providing the highest yields and lowest cost.
System power	Lack of DLL allows for system power management. System can enter/exit power-down modes and throttle or stop the clock.	DLL required for high performance, which inhibits system power savings.
	Optimized for battery life and portability—low power is the primary feature	**Optimized for cost and performance—cost is the primary feature**

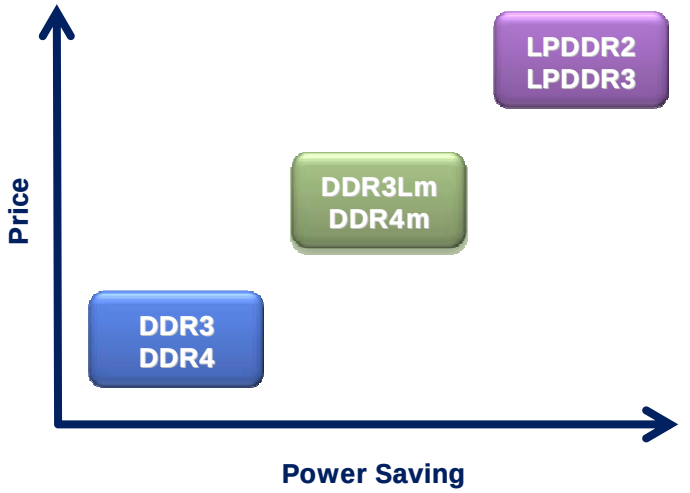
Micron's solution in the middle : M-Class

Market Trend



Source: Gartner, Intel, Micron

Price vs. Power Savings



DRAM Solutions: DDR3Lm / DDR4m

- Thin & Light drives future DRAM requirements
- DDR3Lm / DDR4m products optimized for new applications Ultrabook and Tablet
  - Power saving to extend battery life (stand-by / IDD6)
  - High density solution for small from factors (DDP / x32)

DDR Memory
Interface Design Considerations

DDR Interface Design Considerations

- DQ Driver Impedance Matching
  - Select the proper driver strength to match the system size
  - Point-to-point systems need a weak driver
  - DDR2 off-chip driver calibration (OCD) is not recommended; ZQ self calibration in DDR3 provides greater precision
- Clock Domain Boundary
  - At high frequencies, the clock period is smaller and signals may cross the clock domain boundary in a large system, then require an alignment in the initialization sequence

DDR Interface Design Considerations

- On Die Termination (ODT) Use
  - ODT is almost a MUST for better signal integrity in high-frequency operation, but it consumes power
  - Choose termination resistance carefully to balance power consumption, signal swing, and reflection
  - If ODT is not used, carefully design to cancel or reduce the signal reflection using symmetrical T-branches or a dumping resistor, for example

Signal Grouping and Routing Considerations

- CLK
  - DDR memory timing reference
    - Route carefully to avoid catching noise or distortion
  - Differential clock (except in SDR and Mobile LPRAM)
    - Treat as a differential pair
  - Address/command signals are latched by CLK
    - ^{t}PD matching is required to meet the setup/hold spec
    - Address/command signals are single-ended, so velocity compensation against CLK is required
  - ^{t}DQSS spec
    - DQS is required to stay within (±) ¼ clock.

Signal Grouping and Routing Considerations

- DQS, DQ, DM
  - DQS is used for latching data (DQ, DM)
    - Glitch-free operation is required for DQS; route carefully to prevent unnecessary noise or crosstalk
  - DQS is a differential signal for better timing margins (except in DDR)
    - Treat as a differential pair
  - Match traces within byte lanes in routing (8 DQ, DM, DQS, DQS#)
    - Ensure reduced timing skew

Signal Grouping and Routing Considerations

- Address, Command
  - Frequency is one-half of DQ, except for LPDDR2, which uses DDR address/command input
  - In large systems, loading becomes quite heavy; special consideration is required for both signal integrity and timing
    - 2T timing can be used except for CS# and CKE (not applicable for LPDDR2)
  - DDR3 has a write-leveling feature to enable fly-by address commands—clock topology for high-speed operation in a high-loading condition

Summary

- Make your system competitive
  - Select the right DDR memory device and design it in properly

Thank you !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