E2

DDR Memory Trends and Design Considerations

Yoshitomo Asakura
Senior Manager, Technical Marketing
DRAM Solution Group
Micron Japan, Ltd.

©2011 Micron Technology, Inc.

Agenda

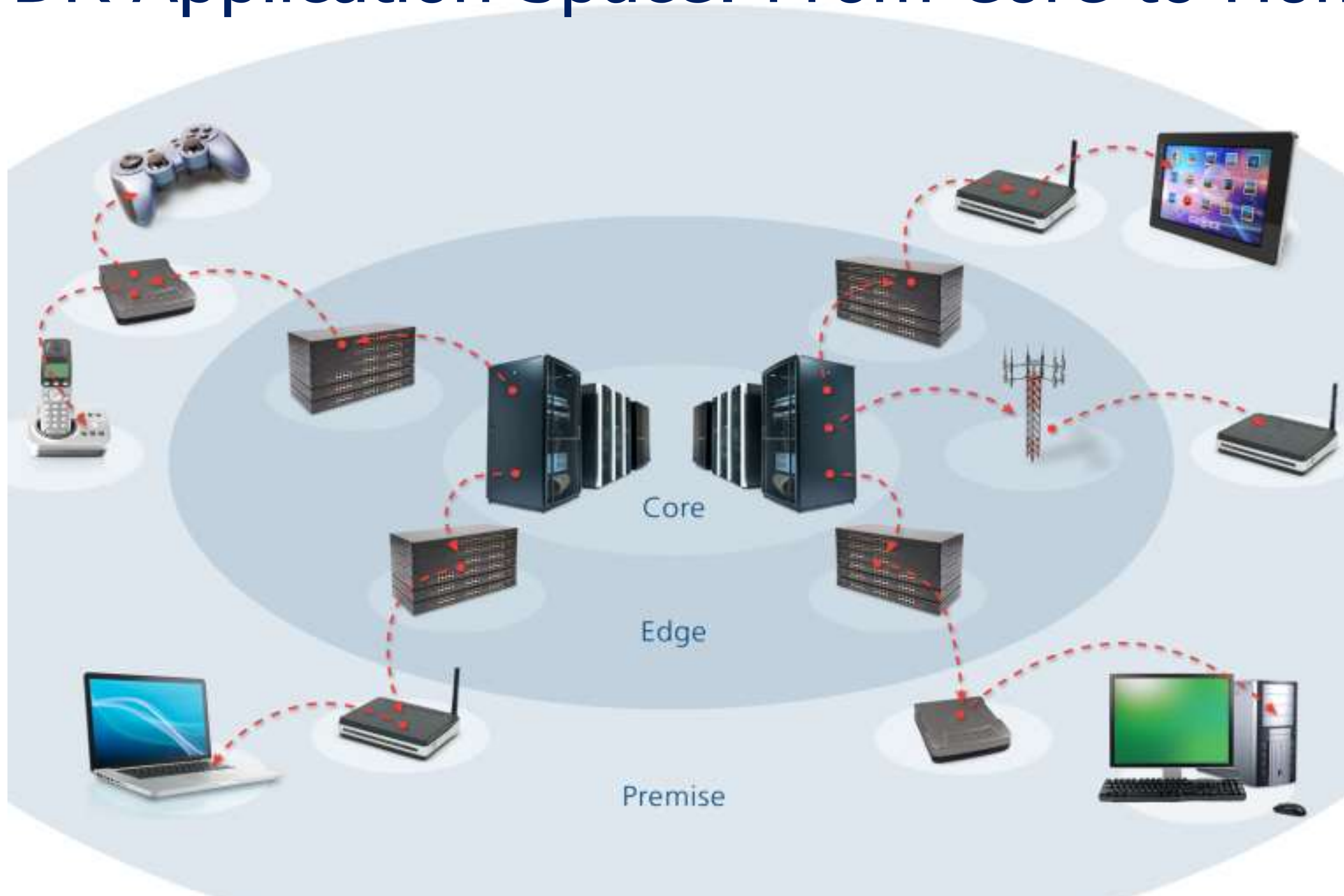
- Variety of DDR Memories
- DDR Memory Trends
- Selecting a DDR Memory for Your Application
- DDR Memory Design Considerations
  - Performance
  - Signaling, Board Layout, and Routing

©2011 Micron Technology, Inc.

Variety of DDR Memories

©2011 Micron Technology, Inc.

DDR Application Space: From Core to Home



- Server, Networking, and Storage Convergence: Companies and equipment are crossing segment borders
- Consumer and Personal Computing Convergence: Game consoles, PCs, and tablets—always on and connected
- Cloud Delivery: Software, information, and computing power—convenience and access for consumer devices

Value of DDR Memories from Market Eye

- **Good Balance of High Density/Low Cost and Small Package/High Speed/Low Power**
  - Flash offers high density and nonvolatility, but very slow write speeds
  - SRAM offers low standby power, high-speed operation, and requires no refresh, but costs increase due to large die sizes
  - Flash and SRAM have relatively large packages due to many address and data pins
  - Emerging memories (MRAM, PCRAM, ReRAM etc.) offer relatively high speed and nonvolatility, but density scaling has not yet been established in order to replace DDR and Flash

©2011 Micron Technology, Inc.

Variety of DDR Memories

- DDR Series (Standard DRAM)
  - SDRAM/DDR/DDR2/DDR3/(DDR4)
- Mobile LPDRAM (Low Power – for Cell Phones)
  - LPSDRAM/LPDDR/LPDDR2/(LPDDR3)
  - Wide I/O
- Special Purpose
  - Reduced latency DRAM (RLDRAM® Memory); short ^{t}RC for networking
  - Hybrid memory cube (HMC); super-high bandwidth
- Other DRAM
  - GDDR3/GDDR5 (graphics cards)
  - FCRAM (game consoles)
  - XDR (game consoles)

©2011 Micron Technology, Inc.

DDR Memory Spec Comparison

DRAM Type	Max Bandwidth	Data Bus Width	Operating Frequency	Supply Voltage	I/O Voltage
SDR	166 Mb/s	x4/x8/x16	0–166 MHz	3.3V	3.3V
DDR	400 Mbps	x4/x8/x16	83–200 MHz	2.5V	2.5V
DDR2	1066 Mb/s	x4/x8/x16	125–533 MHz	1.8V	1.8V
DDR3	2133 Mb/s	x4/x8/x16/(x32)	200–1066 MHz	1.5V/1.35V	1.5V/1.35V
DDR4	3200Mb/s	x4/x8/x16	400–1600 MHz	1.2V & 2.5V	1.2V
Mobile LPDRAM	133 Mb/s	x16/x32	0–133 MHz	1.8V	1.8V/1.2V
LPDDR	400 Mb/s	x16/x32	0–166 MHz	1.8V	1.8V/1.2V
LPDDR2	1066 Mb/s	x8/x16/x32	10–533 MHz	1.2V & 1.8V	1.2V
LPDDR3	2133 Mb/s	x8/x16/x32	200–1066 MHz	1.2V & 1.8V	1.0V
GDDR3	1.6 Gb/s	x32	200–800 MHz	1.8V/1.5V	1.8V/1.5V
GDDR5	5.0 Gb/s	x32	200–800 MHz	1.5V/1.35V	1.5V/1.35V
RLDRAM 2	1066 Mb/s	x18/x36	175–533 MHz	1.8V & 2.5V	1.8V/1.5V
RLDRAM 3	2133 Mb/s	x18/x36	TBD–1066 MHz	1.35V & 2.5V	1.2V

©2011 Micron Technology, Inc.

Micron Announces Fully Functional DDR4 DRAM Module

- It is expected that the enterprise and micro-server markets will take full advantage of the new features and specifications designed into DDR4
- The fast-growing ultrathin client and tablet markets will also benefit from new opportunities enabled by the power savings and performance features of Micron's DDR4

Micron's 30-nanometer (nm) technology, the 4-gigabit (Gb) DDR4 x8 part is the first piece of what is expected to be the industry's most complete portfolio of DDR4-based modules, which will include RDIMMs, LRDIMMs, 3DS, SODIMMs and UDIMMs (standard and ECC)

©2012 Micron Technology, Inc.

HMC Consortium

- **Mission:**
  To promote widespread adoption and acceptance of an industry standard serial interface and protocol for the Hybrid Memory Cube
- Hybridmemorycube.org
  - Weekly working group meetings among Developers
  - Adopter group preparing to received initial draft specification
  - Over 90 Adopter Agreement inquiries submitted to date
- HMC Consortium specification release available early to Adopters
  - Only Adopters see first draft and subsequent revisions prior to public launch
  - Draft scheduled for release to Adopters June 2012
  - Public release targeted for December 2012
- Log into hybridmemorycube.org to become an Adopter and join the conversation

http://www.hybridmemorycube.org/

Hybrid Memory Cube
CONSORTIUM

Home | About Us | The Technology | Membership | Contact Us | News | Login

"With HMC's ground-breaking memory technology and our IP and turnkey design capabilities we can enable a new level of system performance and integration." - Naveed Sherwani, President & CEO of Open-Silicon

- Discover The Technology
- Review the FAQ
- Learn How To Participate

About the Technology

Hybrid Memory Cube (HMC) represents an entirely new category of high performance memory, delivering unprecedented system performance and bandwidth. Learn More

About the Consortium

The HMC Consortium is a working group made up of industry leaders who build, design-in, or enable Hybrid Memory Cube (HMC) memory technology. The group works to innovate and expand the capabilities of the next generation of memory-based solutions. Learn More

News

Announcing the HMC Consortium

View All HMC News

© 2011 Hybrid Memory Cube Consortium

ALTERA. IBM Micron® Microsoft

Open-Silicon SAMSUNG XILINX®

Introducing: **RLDRAM3**

The best low-latency DRAM gets better

- Unprecedented performance for high-end networking
- Comparable to SRAM access time at superior cost and density
- Easy transition path from RLDRAM 2 platforms
- High interest from customers and key enablers

Extending success of RLDRAM 2 with RLDRAM 3

- Improved performance:
  - Random access time down to 10ns WRITE and 2.5ns READ
  - Doubled sustainable bandwidth of 2133 Gb/s
  - Power efficiency and high memory density
- Memory densities of 576Mb and 1.1Gb

©2011 Micron Technology, Inc.

DDR Memory Trends

©2011 Micron Technology, Inc.

DRAM Density & Architecture Transition

All Technologies

100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

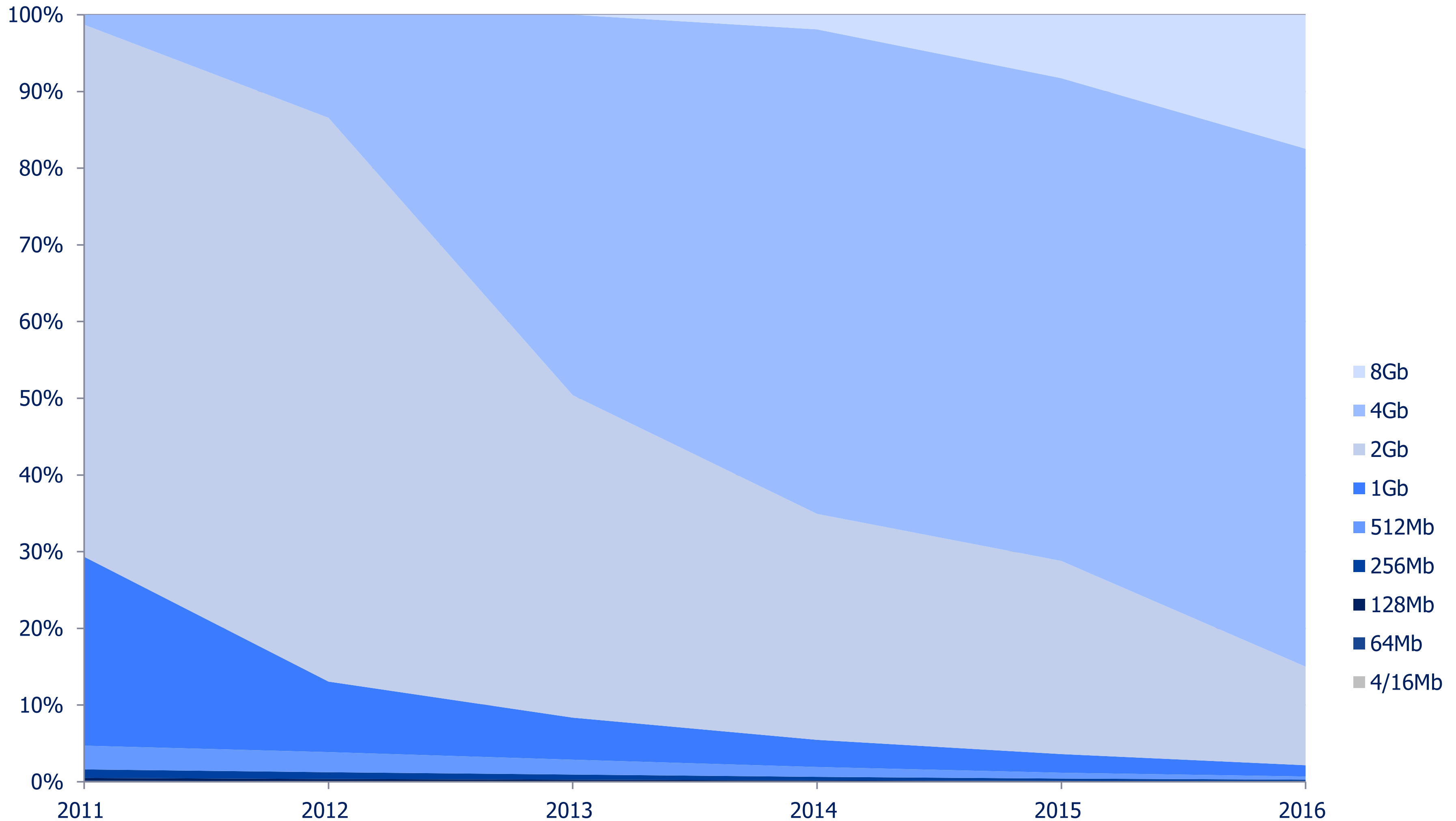
2011 2012 2013 2014 2015 2016

DDR4
DDR3
Mobile DRAM
DDR2
Graphic
SDR
DDR

Source: iSuppli - DRAM Q1 2012 Market Tracker Database

DRAM Density & Architecture Transition

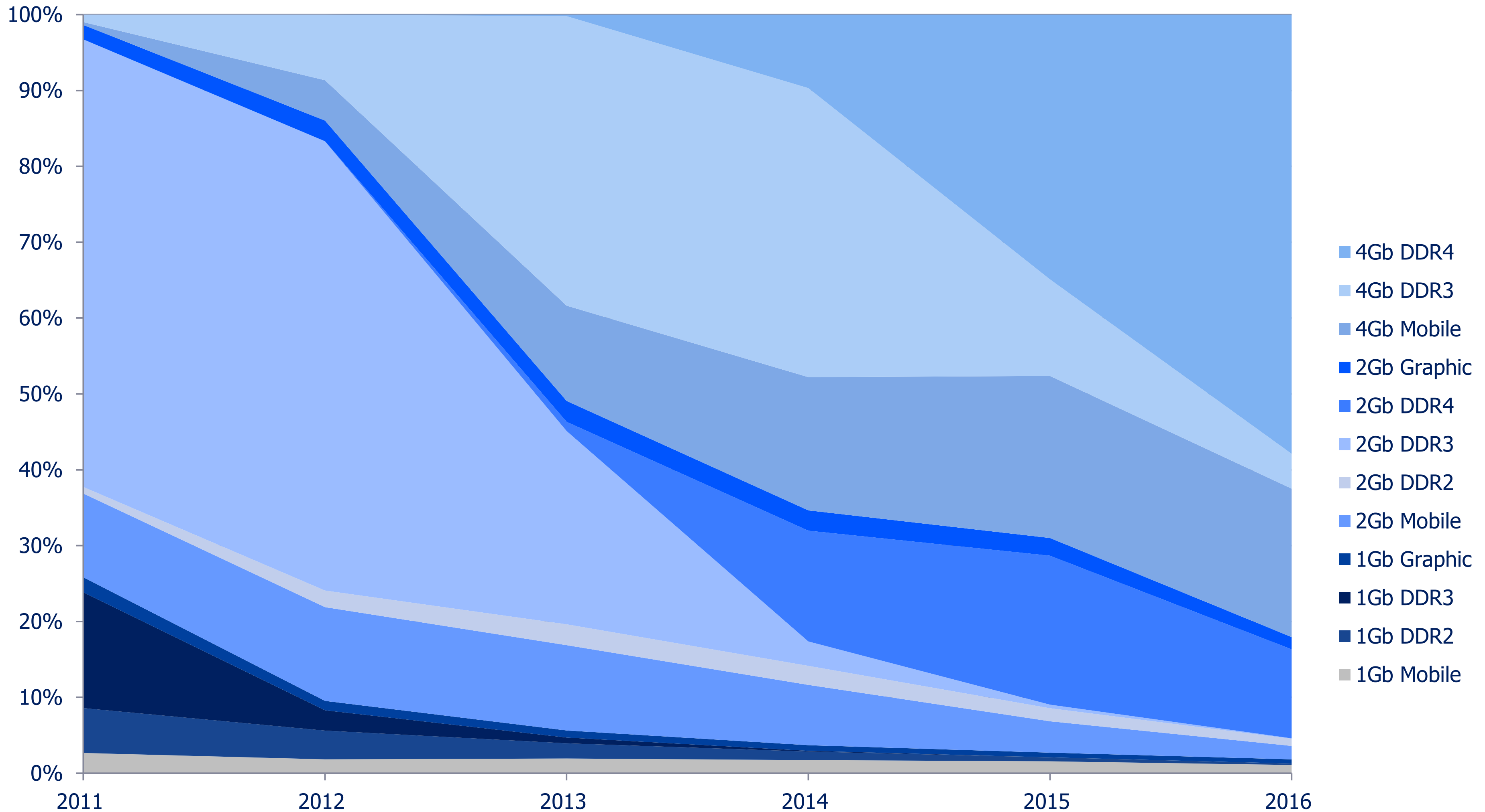
All Densities



Source: iSuppli - DRAM Q1 2012 Market Tracker Database

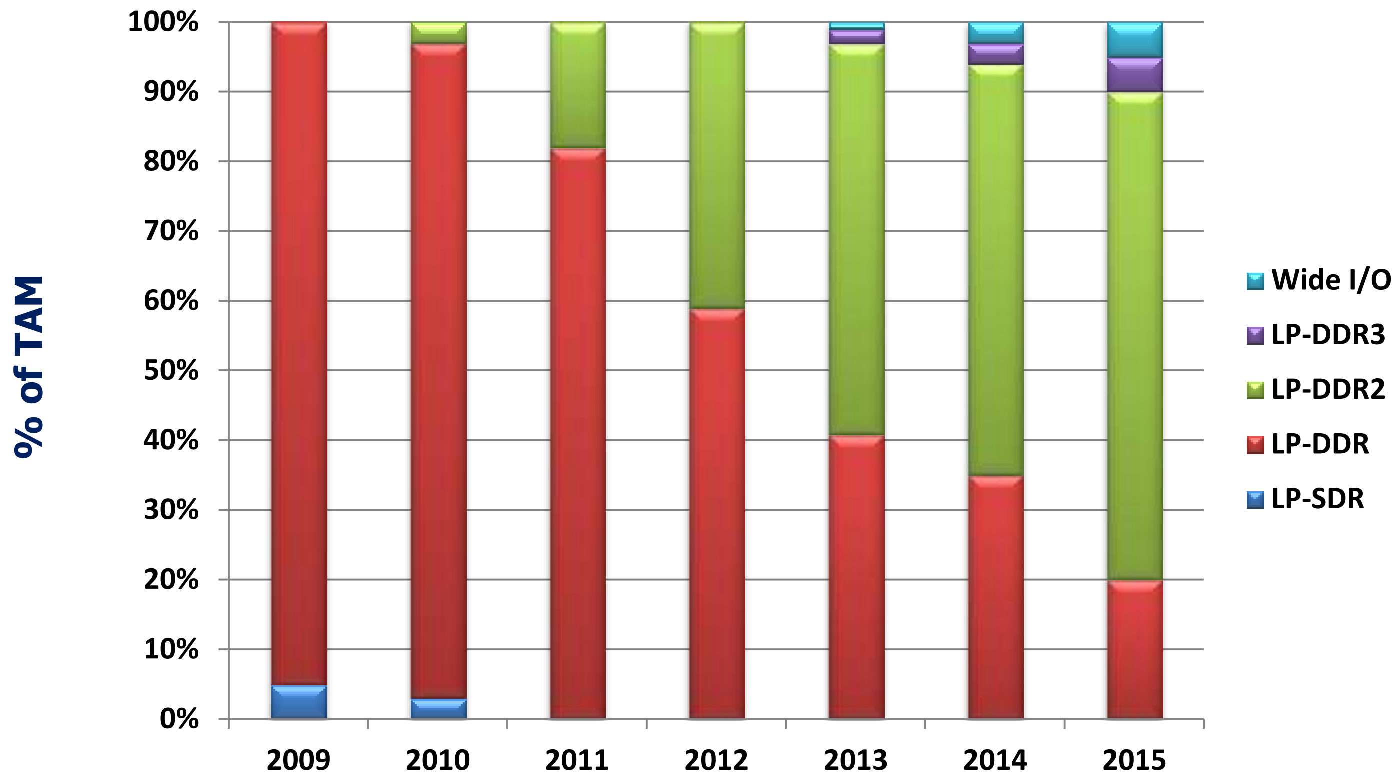
DRAM Density & Architecture Transition

Major Products



Source: iSuppli - DRAM Q1 2012 Market Tracker Database

LPDRAM Technology Trends



- Increased LPDDR2 adoption starting in 2011
- Wide I/O and LPDDR3 introduction planned for 2013

Source: Micron Marketing

Selecting a DDR Memory for Your Application

©2011 Micron Technology, Inc.

How to Select DDR Memory

System Requirements

- Bandwidth
- Density
- Power consumption
- Size/board area
- Cost

Clarify the System Requirements First!

DDR Selection

- Data bus width
- Operating frequency
- Technology
  - Interface
  - Voltage
  - Operating mode
- Package
- Market trends

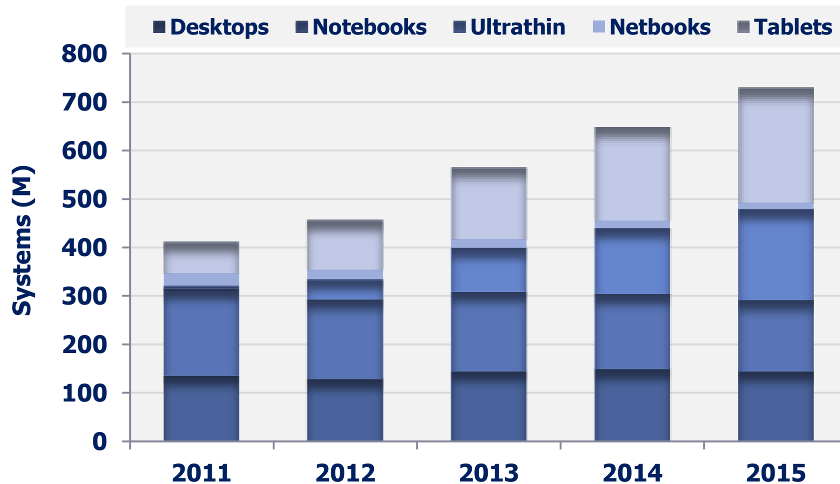
DDR Memory Recommendations

- Commodity DDR: DDR3 in 2012–13
  - Cost-effective (density/performance) solution for most applications
  - Legacy DDR (SDRAM, DDR, DDR2) for low-density/low-speed applications; consider market availability and pricing
- Low-Power DDR: LPDDR/LPDDR2 in 2012–13
  - For highly power-sensitive applications
- Special Purpose: RLDRAM, HMC
  - For extensive, performance-driven applications (latency/bandwidth)

©2011 Micron Technology, Inc.

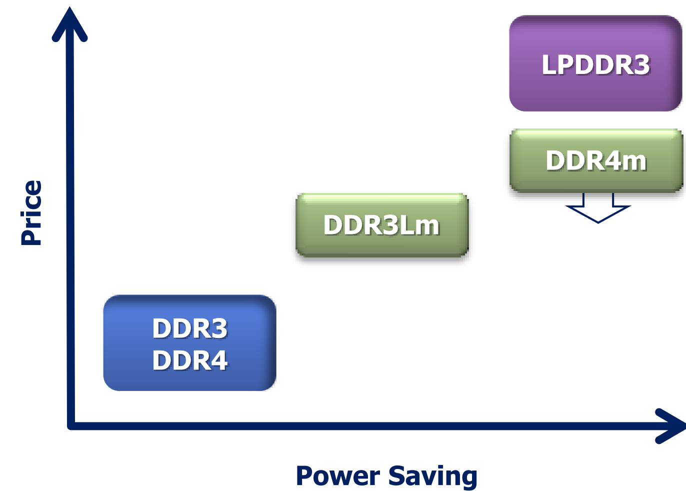
Innovative Solution for Ultrathin Market

Market Trend



Source: Gartner, Intel, Micron

Price vs. Power Savings



DRAM Solutions

Full Product Portfolio

- DDR3 / DDR4 → Optimized for cost and performance - cost is primary feature
- LPDDR3 → Optimized for battery life and portability - low power is primary feature
- DDR3Lm / DDR4m → Extended battery life while keeping cost competitive

Market Introduction Status

- DDR3Lm design wins with 42nm products shipping in volume
- DDR3Lm sampling of 30nm started with volume available in CQ3'12
- DDR4(m) sampling of 30nm late 3Q'12
- LPDDR3 sampling of 30nm late 4Q'12

DDR Memory
Design Considerations – Performance

©2011 Micron Technology, Inc.

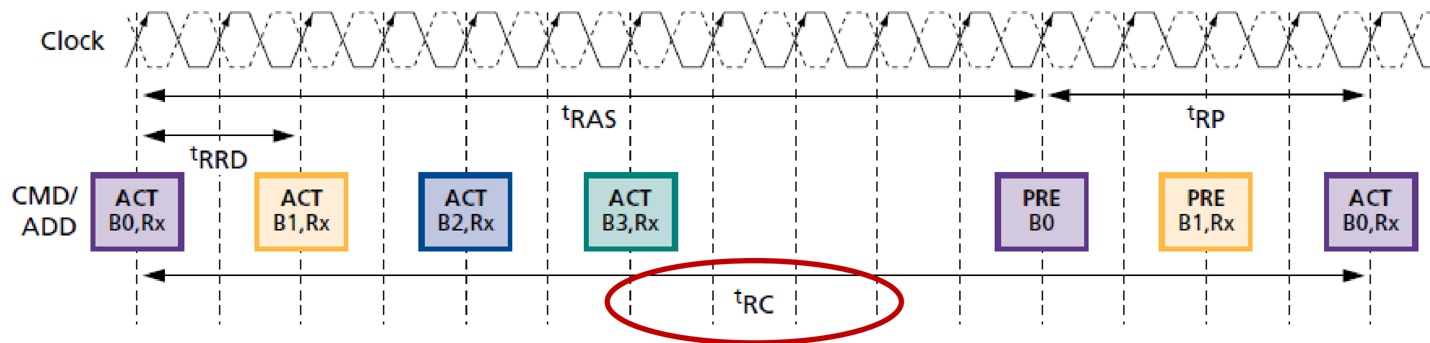
Design Considerations – Performance

- These days, DDR controller IPs are widely available; therefore interfacing DDR memories is getting easier
- But if the target is a high-performance system, designers of system and DDR memory interfaces should know about the DRAM performance constraint
  - Random Access Constraints
  - Power Bussing Constraints
  - Common Data Bus Constraints
  - Data Strobe Preamble/Postamble Constraints
  - Minimum Burst Length Constraints
  - Refresh Overhead Constraints

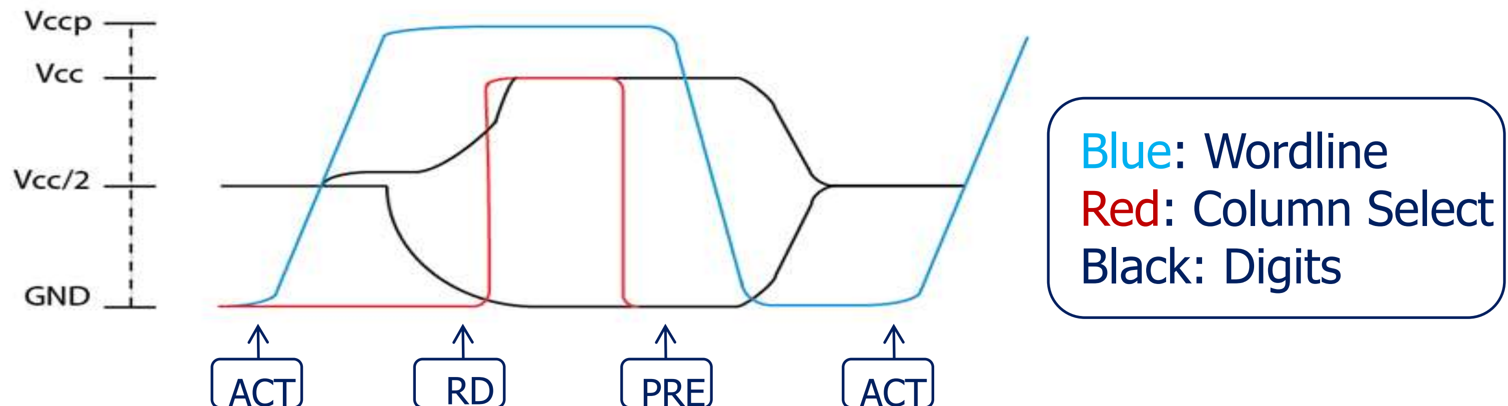
©2011 Micron Technology, Inc.

Random Access Constraint

- ^{t}RC – Activate-to-Activate Delay Within the Same Bank

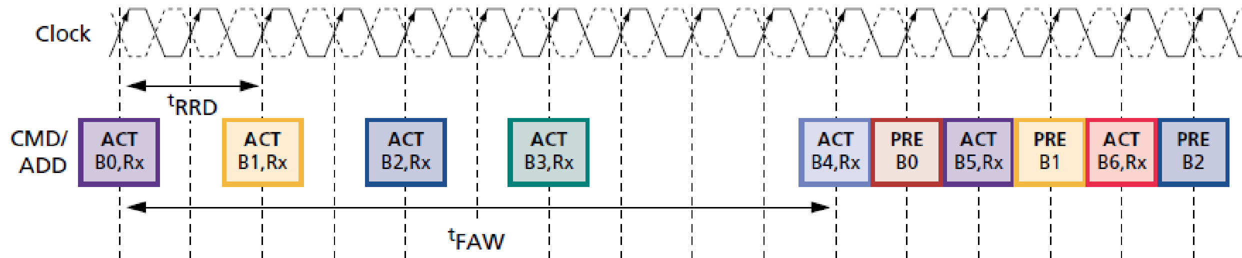


  - Product of DRAM 1T-1C Architecture – All DRAM have this constraint
    - Row Opens -> Stored Charge Dumps on Digit Line -> Sense Amp Fires -> Row Closes

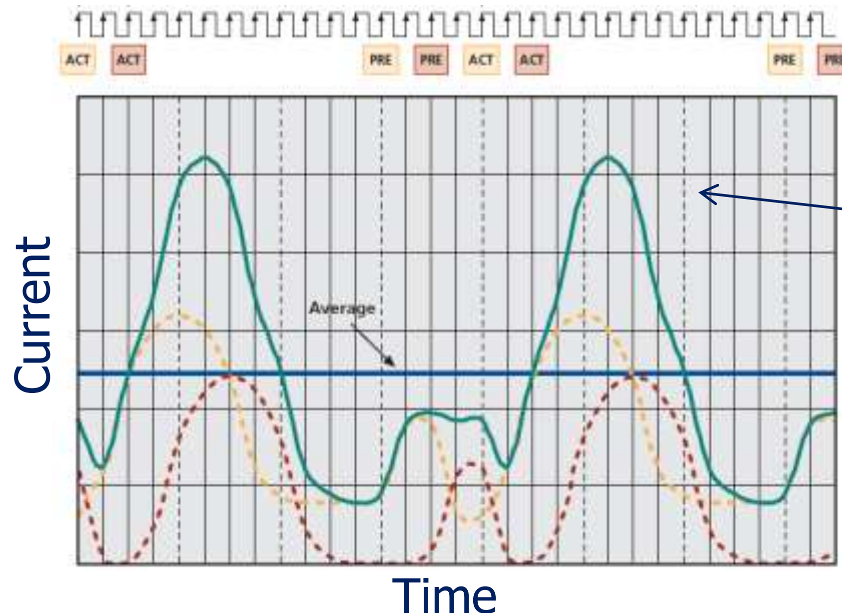


Power Busing Constraints

- ^{t}FAW – Four Bank Activate Window



  - Introduced with 8-bank architecture in DDR2
  - Spec dictated by DRAM power busing constraints



ACTIVATE Commands Cause Large Current Spikes

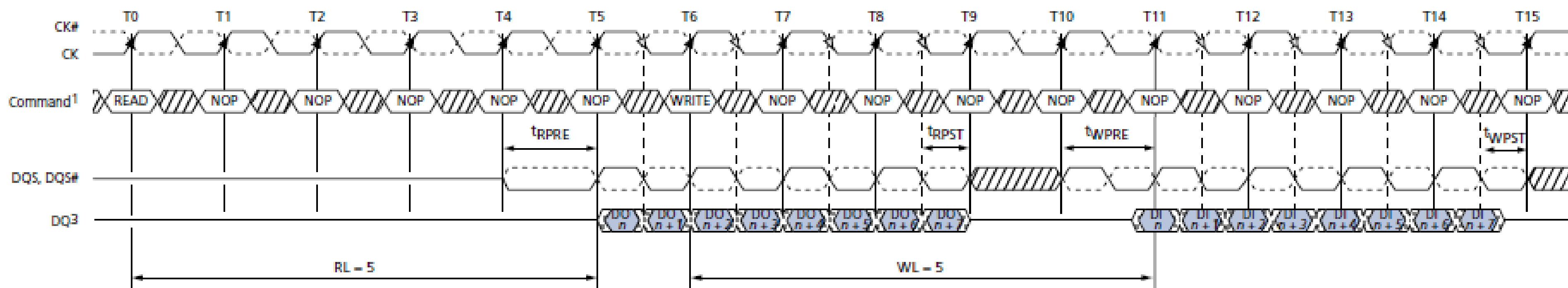
Micron Confidential | ©2011 Micron Technology, Inc.

Common Data Bus Constraints

- Common I/O beneficial in reducing pin count
- DDR3 internal input/output is same physical bus
  - Reduces die size
  - Introduces ^{t}WTR spec to avoid contention
    - Ensures data has been fully written to array and internal data bus is available to have READ data on it

Data Strobe Preamble/Postamble Constraints

- SSTL-based strobes require preamble and postamble
  - Necessary for input data buffer on and off timing
  - WRITE: ^tWPRE, ^tWPST/READ: ^tRPRE, ^tRPST
- DDR3 ^tWPRE spec requires a HIGH-to-LOW transition
  - Adds one extra clock of latency during READ-to-WRITE



- DDR3 ^tRPRE and ^tRPST add latency with dual-rank systems
  - One to two NOPs required to avoid contention on shared DQS signal

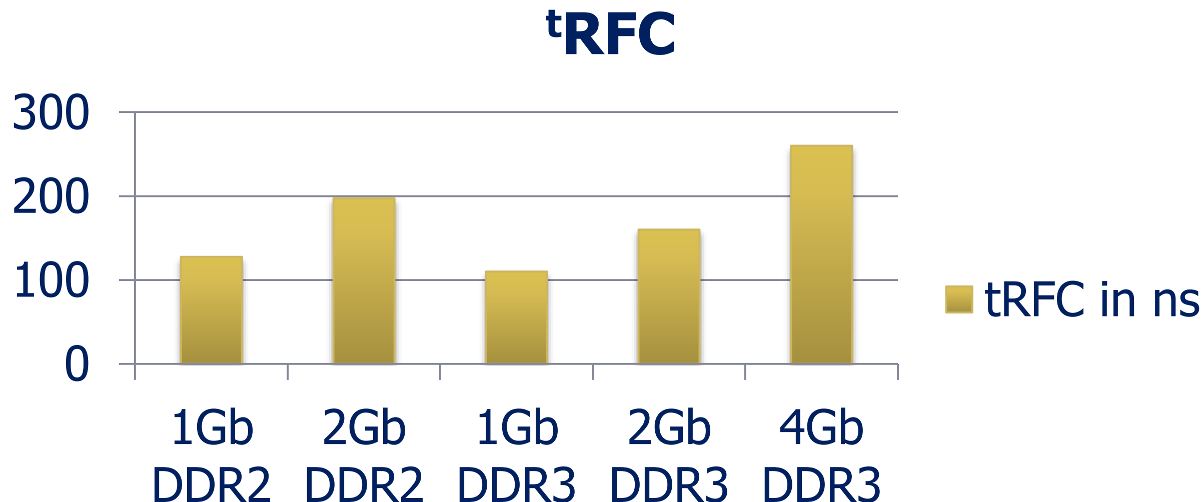
Minimum Burst Length Constraints

- Core architecture of commodity DRAM same for generations
  - Based on ~5ns column cycle time
    - Keeps DRAM architecture simple and economic
  - Each successive DRAM family requires longer MIN burst lengths
    - SDRAM: BL1 / DDR: BL2 / DDR2: BL4 / DDR3: BL8
  - Significant delays if desired MIN burst length lower than DRAM MIN burst length

©2011 Micron Technology, Inc.

Refresh Overhead

- All DRAM subject to some level of refresh overhead
  - Spec typically 64ms < 95˚C
  - Commodity DRAM refreshes all banks with single refresh command
    - Addresses are "Don't Care"
    - Subject to ^{t}RFC – Only NOPs issued during this time
  - ^{t}RFC spec increasing with larger densities to maintain 8K refresh count



©2011 Micron Technology, Inc.

DDR Memory Design Considerations – Board Layout and Routing

©2011 Micron Technology, Inc.

Design Considerations – Board Layout/Routing

- Avoid crossing splits (return path discontinuities) in reference planes
- Minimize intersymbol interference (ISI) by keeping impedances matched
- Minimize crosstalk by isolating sensitive bits, such as strobes
- Maintain references for a given signal, whether it be V_{DD}, V_{DDQ}, or V_{SS}
  - High-speed signals should be referenced to V_{SS}

Design Considerations – Power Supplies

Supply	Minimum	Nominal	Max	Purpose
V_{DD}/V_{DDQ}	1.425V	1.5V	1.575V	DDR3
V_{DD}/V_{DDQ}	1.28V	1.35V	1.42V	DDR3L
V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	Differential Input Buffer Reference

- V_{REF} Recommendations
  - Low current draw allows for generation with precision resistor divider
  - Design traces as short and wide as possible from source to DDR
    - Provides lowest possible inductance and minimizes noise
  - Place 0.1uF decoupling cap as close as possible for each V_{REF} ball
    - Place between V_{REF} and input signals reference plane
    - Short traces reduce inductance of net
  - Maintain at least 15–25 mil clearance from V_{REF} to adjacent traces to prevent coupling

©2011 Micron Technology, Inc.

Design Considerations – Power Supplies

- Decoupling V_{DD} and V_{DDQ}
  - On-board power supplies typically switching regulators that include large amount of bulk capacitance
    - Additional low-frequency decoupling generally not required
      - Additional bulk cap might be a good idea if DDR is a long distance from supply and inductance of plane causes unacceptable voltage droops
  - Decoupling high-frequency power supply noise recommendation
    - Place a 0.2–1.0uF cap at the following locations for each supply to minimize distance (and associated inductance)
    - Adjacent die can share caps

Design Considerations – Power Supplies

- V_{TT} Recommendations
  - External supply used if terminating command and address signals
  - Nominal value equivalent to V_{REF}
    - Must track variations of V_{REF}
  - Generate by a regulator that can sink and source reasonable amounts of current while maintaining tight voltage tolerance
  - Place one 1.0uF decoupling cap for every 4 signals terminated to V_{TT}
    - Place cap between V_{TT} and the input signals reference plane
    - Place as close as possible to terminating resistors to minimize inductance
  - V_{TT} island surface trace length should be at least 150 mil (250 mil preferred)

©2011 Micron Technology, Inc.

Design Considerations – Signaling

- DQ Driver Impedance Matching
  - Select the proper driver strength to match the system size
  - Point-to-point systems need a weak driver
  - DDR2 off-chip driver calibration (OCD) is not recommended; ZQ self calibration in DDR3 provides greater precision
- Clock Domain Boundary
  - At high frequencies, the clock period is smaller and signals may cross the clock domain boundary in a large system, then require an alignment in the initialization sequence

©2011 Micron Technology, Inc.

Design Considerations – Signaling

- On-Die Termination (ODT)
  - ODT is almost a MUST for better signal integrity in high-frequency operation, but it consumes power
  - Choose termination resistance carefully to balance power consumption, signal swing, and reflection
  - If ODT is not used, carefully design to cancel or reduce the signal reflection using symmetrical T-branches or a dumping resistor, for example

©2011 Micron Technology, Inc.

Design Considerations – Signaling

- Address, Command
  - Frequency is one-half of DQ, except for LPDDR2, which uses DDR address/command input
  - In large systems, loading becomes quite heavy; special consideration is required for both signal integrity and timing
    - 2T timing can be used except for CS# and CKE (not applicable for LPDDR2)
  - DDR3 has a write-leveling feature to enable fly-by address commands—clock topology for high-speed operation in a high-loading condition

©2011 Micron Technology, Inc.

Design Considerations – Signaling

- CLK
  - DDR memory timing reference
    - Route carefully to avoid catching noise or distortion
  - Differential clock (except in SDR and Mobile LPRAM)
    - Treat as a differential pair
  - Address/command signals are latched by CLK
    - ^{t}PD matching is required to meet the setup/hold spec
    - Address/command signals are single-ended, so velocity compensation against CLK is required
  - ^{t}DQSS spec
    - DQS is required to stay within (±) ¼ clock

©2011 Micron Technology, Inc.

Design Considerations – Signaling

- DQS, DQ, DM
  - DQS is used for latching data (DQ, DM)
    - Intermittent operation but glitch-free operation is required for DQS; route carefully to prevent unnecessary noise or crosstalk
  - DQS is a differential signal for better timing margins (except in DDR)
    - Treat as a differential pair
  - Match traces within byte lanes in routing (8 DQ, DM, DQS, DQS#)
    - Ensure reduced timing skew

©2011 Micron Technology, Inc.

Summary

- Make your system competitive
  - Select the right DDR memory device and design it in properly

Thank you !

©2011 Micron Technology, Inc.

Micron®
Focused on Memory | Engineered for Innovation