Application Note

Electronic Package Fault Isolation Using TDR

Introduction 1
TDR Fundamentals 1
TDR Multiple Reflection Effects 3
TDR Resolution and Rise Time 4
TDR Measurements of "Splits" and "Stubs" 5
TDR Probing and Fixturing 5
Using Good Measurement Practices 7
Failure Analysis Goals and Methods 8
Signature Analysis 9
Comparative Analysis 9
Additional Considerations for Package Open Failure Analysis 10
Signal-to-Ground Short Failures 12
Plane-to-Plane Short 13
Plane-to-Plane Short Text Example 13
Summary, Conclusions and Future Work 14
References 15

Introduction

Time Domain Reflectometry (TDR) measurement methodology is increasing in importance as a non-destructive method for fault location in electronic packages [1-4]. The visual nature of TDR makes it a very natural technology that can assist with fault location in BGA packages, which typically have complex interweaving layouts that make standard failure analysis techniques, such as acoustic imaging and X-ray, less effective and more difficult to utilize [5].

In this paper, we will discuss the use of TDR for non-destructive package failure analysis and fault isolation work. We will analyze in detail the TDR impedance deconvolution algorithm as applicable to electronic packaging fault location work, focusing on the opportunities that impedance deconvolution and the resulting true impedance profile opens up for such work. We will discuss the place of TDR in the overall failure analysis process, and present examples of proper fault isolation techniques.

TDR Fundamentals

TDR was initially developed for fault location of long electrical systems such as cables. Currently, high-performance TDR instruments, coupled with add-on analysis tools, are commonly used as the tool of choice for failure analysis and signal integrity characterization of board, package, socket, connector and cable interconnects. Such high-end TDR equipment is currently available from two manufacturers - Agilent and Tektronix.

Figure 1. TDR instruments from Agilent and Tektronix

Based on the TDR impedance measurements, the designer can perform signal integrity analysis of the system interconnect, and the digital system performance can be predicted accurately. A failure analyst can use TDR impedance measurements to locate an interconnect fault more accurately and quickly, allowing the analyst to focus on understanding the physics of the failure at this failure location. A typical system required for such work will consist of a TDR oscilloscope, a probing or fixturing setup (for example, from Cascade Microtech), and analysis software, such as IConnect® from TDA Systems.

Figure 2. A typical failure analysis setup includes a TDR instrument, a probing or fixturing setup, and analysis software

The TDR instrument is a very wide bandwidth equivalent sampling oscilloscope (18-20 Ghz or even more) with an internal step generator. It is connected to the Device Under Test (DUT) via cables, probes and fixtures. It delivers a fast rise time to the DUT, and based on the reflection from the DUT the failure analyst can perform the fault isolation analysis of the DUT.

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This application note was published in EDFAS Microelectronic Failure Analysis Desk Reference, 5th edition (2004).

TDR is very similar to X-ray and acoustic imaging techniques in that it sends the signal to the DUT and looks at the reflection to obtain the information about the DUT. The difference between X-ray or acoustic imaging and TDR is in the type of signal and the type of propagation media for the signal. X-ray and acoustic imaging use X-ray and acoustic stimuli correspondingly, propagating through the free space to the DUT, whereas TDR uses fast-electrical-step stimulus, delivered to each trace in the DUT via electrical cables, probes, and fixtures.

Table 1. Comparison between TDR, SAM and X-Ray failure analysis techniques

	TDR	SAM	X-ray
Stimulus type	Electric	Acoustic	X-ray
Stimulus delivery medium	Electrical wires	Water	Air
Direct contact required?	Yes, signal and ground	No	No
Output presented for analysis	Package trace reflection profile	Optical image	Optical image
Ability to locate failures between package or board layers	Good	Poor	Poor

A direct electrical contact between the TDR instrument and the DUT is required to perform the measurement. In addition, not only the signal, but also the ground contact must be provided in order for the TDR signal to provide meaningful information about the DUT. Without a good ground contact, the TDR signal will not have a good current ground return path, and the TDR picture will be extremely hard to interpret.

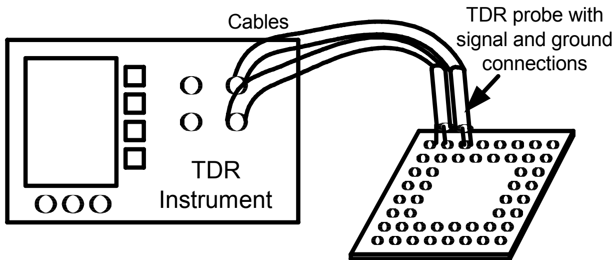


Figure 3. TDR is connected to the DUT via cables, probes and fixtures. A direct electrical contact to the DUT is required for both signal and ground pins of the TDR probe

Because of the wide bandwidth of the oscilloscope, and to ensure that this bandwidth and fast rise time can be delivered to the DUT, one must use high-quality cables, probes, and fixtures, since these cables, probes and fixtures can significantly degrade the rise time of the instrument, reduce the resolution, and decrease the impedance measurement accuracy.

A typical TDR oscilloscope block diagram is shown in Figure 4 below. The fast-step-stimulus waveform is delivered to the DUT via electrical cable, probe, and fixture interconnects. One way to think of the incident TDR step is as a wave front propagating through the interconnect and reflecting back from the discontinuities. The superposition of all the wave fronts, reflected from all discontinuities, is what is displayed on a TDR oscilloscope.

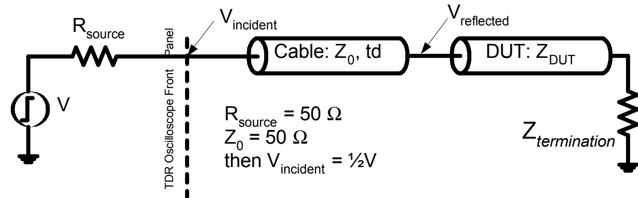


Figure 4. TDR oscilloscope equivalent circuit

The waveform reflected from the DUT is delayed by two electrical lengths of the interconnect between the DUT to the TDR oscilloscope, and superimposed with the incident waveform at the TDR sampling head (Figure 5). The incident waveform amplitude at the DUT is typically half the original stimulus amplitude (V) at the TDR source. The smaller DUT incident waveform amplitude is due to the resistive divider effect between the 50 Ohm resistance of the source and 50 Ohm impedance of the coaxial cables connecting the TDR sampling head and the DUT.

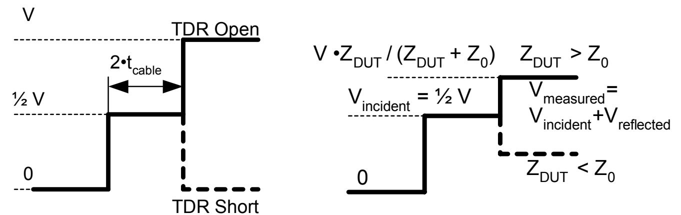


Figure 5. The incident waveform is delayed by twice the length of the interconnect between the DUT and the TDR oscilloscope, and is divided in half by the resistor divider effect between resistance of the TDR source and resistance of the interconnect to the DUT

Equivalent resistance of the TDR source R_{source} defines the characteristic impedance of the measurement system. Since R_{source} is 50 Ohm for high-performance TDR instruments available today, using non-50 Ohm cables and probes can produce confusing results. Unlike with a regular oscilloscope, no active probes or resistor divider probes are allowed for use with TDR.

TDR does not provide an optical image of the package, but rather an electrical signature of the trace in the package. Because of the nature of the information that TDR provides, it is important to be aware of typical TDR signatures that correspond to simple package failures, such as a short or an open connection (Figure 6).

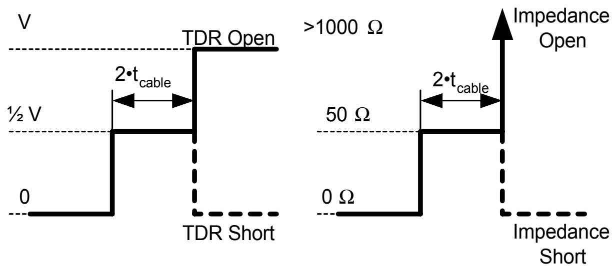


Figure 6. Open and short connection TDR and impedance profile signatures. V is the full voltage amplitude of the TDR step source; t_{cable} is the electrical length of the cable and probe interconnecting the TDR oscilloscope and the DUT

Note that everything in TDR is round trip delay. This applies not only to the cable, probe and fixture interconnecting the TDR oscilloscope to the DUT, but also to all delay measurements on the DUT itself. In order to obtain an accurate delay readout, the designer has to divide the measured delay by 2.

After the round trip delay of the cable, the voltage reflected from the DUT arrives back to the oscilloscope and is added to the incident voltage on the oscilloscope to produce the measured voltage values. The oscilloscope then converts these voltage values into the values for reflection coefficient and impedance. It is the impedance and delay that the failure analyst is most interested in, and the accuracy and resolution of the impedance and delay measurements is what determines the accuracy of fault isolation.

The faster the rise time that the TDR interconnect can deliver to the package under test, the smaller the size of the discontinuities that can be resolved with a TDR oscilloscope. Available TDR instrumentation provides very fast rise times; reflected signal rise times of the order of 25-35 ps can be observed at the TDR oscilloscope. However, poor quality cabling and fixturing can quickly degrade the TDR instrumentation rise time and decrease the instrument resolution.

It is important to wear good personal ESD protection when working with high-performance TDR oscilloscopes. TDR instruments are ESD-sensitive, high-precision and high frequency instruments. Personal ESD protection (e.g., anti-static strap connected to the instrument) will protect the instrument while maintaining its performance. Add-on ESD modules in the signal path will degrade the rise time of the instrument and degrade its resolution. It is also important to discharge possible charge accumulated on your probe or cable before making the connection to the DUT.

In addition to measuring impedance, the TDR oscilloscope is capable of providing L, C and R signatures for the DUT. For example, an experienced TDR user can, without difficulty, recognize a "dip" in a TDR waveform as a shunt capacitance, and a "spike" as a series inductance. Any L and C combination can also be represented as shown in Figure 7.

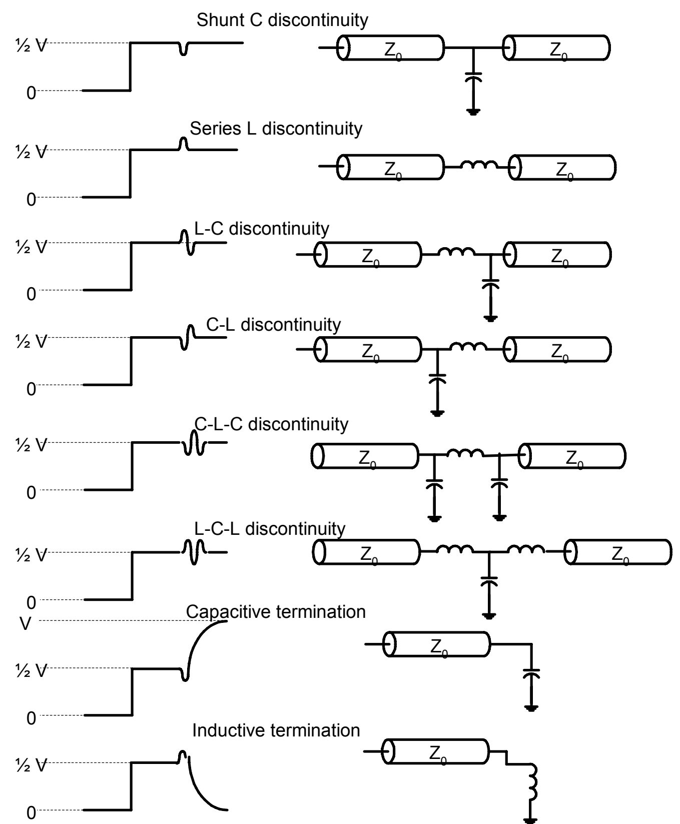


Figure 7. Visual lumped (LCR) interconnect analysis using TDR

A series C or a shunt L, however, will represent a high-pass filter for the TDR signal, and the resulting reflection from the elements beyond such series C or shunt L can not be interpreted without prior knowledge of the DUT topology.

Additional information about TDR measurement technology and TDR oscilloscopes can be found in references [6] through [8].

TDR Multiple Reflection Effects

One of the limitations of TDR is the effect of multiple reflections, which is present in multi-segment interconnect structures, such as an electrical package. The accuracy of the DUT signature observed at the TDR oscilloscope is dependent on the assumption that at each point in the DUT, the incident signal amplitude equals the original signal amplitude at the probe-to-DUT interface. In reality, however, at each impedance discontinuity, a portion of the TDR incident signal propagating through the DUT is reflected back, and only a portion of this signal is transmitted to the next discontinuity in the DUT. In addition, the signal reflected back to the scope may re-reflect and again arrive at the next discontinuity at the DUT. These so called "ghost" reflections are illustrated on the lattice diagram in Figure 8.

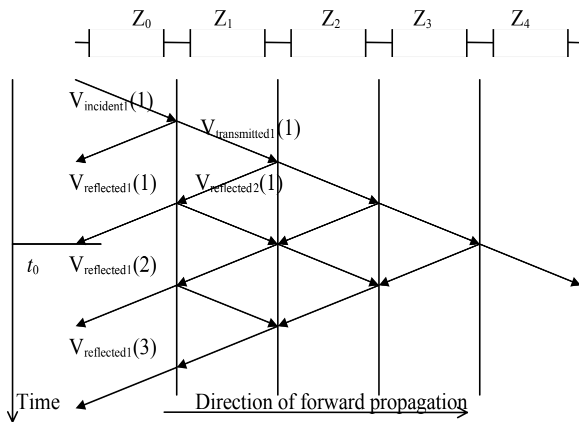


Figure 8. Lattice diagram of TDR waveform propagating through a DUT with multiple impedance discontinuities

As a result of these re-reflections, the signature of the DUT becomes less clear, and additional processing is required using the impedance deconvolution algorithm ([9] and [10]), which is currently not available in TDR oscilloscopes. The impedance deconvolution algorithm deconvolves the multiple reflections from the TDR waveform and provides the true-impedance-profile for the DUT, significantly improving the clarity of the DUT signature and simplifying further analysis of the TDR data.

For example, if a failure analysis technician were looking for an open failure in an electrical package, TDR data by itself would not have been sufficient to locate the position of the failure (Figure 9) as there appears to be multiple potential fault locations. The true-impedance-profile provides an exact location of the open in the DUT whereas the TDR waveform by itself provides confusing information about the location of this open. In addition, the impedance profile, being an exact signature of the DUT, is relatively easy to correlate to different layers in a BGA package. Such correlation is practically impossible with a TDR waveform alone.

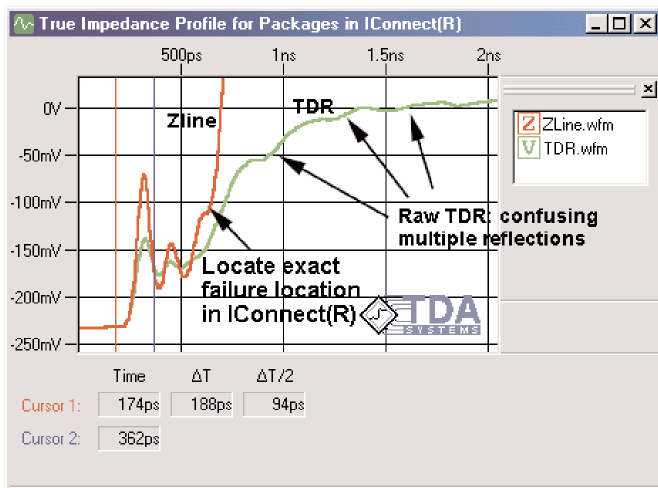


Figure 9. True-impedance-profile vs. the raw TDR waveform for a BGA package. The true-impedance-profile provides much more accurate information about the failure location

An additional advantage that the true-impedance-profile provides is that it is very easy to evaluate capacitance or inductance of an impedance profile segment using the following equations:

$$C = \frac{1}{2} \cdot \int_{t_1}^{t_2} \frac{1}{Z(t)} dt \qquad L = \frac{1}{2} \cdot \int_{t_1}^{t_2} Z(t) dt \qquad (1)$$

The type of discontinuity (inductive or capacitive) that we observe in the impedance profile, can also be easily identified – "dips" in the impedance profile correspond to the capacitive discontinuity, and "peaks" correspond to inductive discontinuity. Being able to estimate the value of capacitance or inductance for any given segment can be a significant help in understanding which package segment is being analyzed and in locating the failure more accurately.

Before discussing package failure analysis techniques using TDR in further detail, it is imperative to note the importance of obtaining a good quality TDR measurement and a clean impedance profile. Without a good TDR measurement for the DUT and the reference, the true-impedance-profile is likely to be computed incorrectly, and both TDR data for the DUT and the true-impedance-profile will provide a confusing picture.

TDR Resolution and Rise time

The issues of TDR resolution are often misunderstood or misrepresented, because the TDR resolution is believed to be completely governed by the following rule of thumb. Two small discontinuities, such as two vias in a PCB, can still be resolved as two separate ones, as long as they are separated by at least ½ the TDR rise time:

$t_{separate}$ a_1 a_2

To resolve a_1 and a_2 as separate discontinuities: $t_{separate} > t_{TDR_risetime}/2$ (10a)

t_{single} a_1

a_1 is not observed if $t_{single} << t_{TDR_risetime}$ ($t_{single} < t_{TDR_risetime}$ / 10) (10b)

Figures 10a and 10b. TDR resolution rules of thumb

If these two vias are not separated by half the TDR rise time as it reaches the vias, they will be shown by TDR as a single discontinuity. Assuming we use good cables, probes, fixtures, and we can deliver the full 30-40ps rise time of the instrument to the discontinuities in question, the minimal physical separation between these vias will be 15-20ps. For FR4 board material with dielectric constant ε_r=4, this results in 2.5-3mm (0.1") resolution. Often this number (or other similar calculation) is quoted as the TDR resolution limit.

However, in real-life situation, the designer typically is looking to observe or characterize a single discontinuity, such as a single via, or a single bondwire in a package, rather than several of such vias or bond-wires! In this case, the above rule is totally irrelevant, and TDR can allow the designer to observe discontinuities of 1/10 to 1/5 of the TDR rise time, bringing the numbers above to 5ps or less than 1mm (25milliinches) range (Figure 10b).

Furthermore, there are well-developed relative TDR procedures for observing and characterizing even smaller discontinuities, such as the golden device comparisons for failure analysis [1-4].

In addition, faster TDR modules are available from Picosecond Pulse Labs, which makes it easier to resolve some of the finer discontinuities and faults.

Figure 11. Picosecond Pulse Labs fast TDR add-on module

TDR Measurements of "Splits" and "Stubs"

If the package trace under test splits into two or more directions, the TDR instrument shows the sum of all reflection from all the N legs in the split, but cannot separate which reflection came from which leg in the split. This means the failure location in case of the traces with splits or stubs can be extremely challenging.

If the splits are of the same impedance and delay (as sometimes is the case in a "star" interconnect topology), they can be simply represented by transmission lines running in parallel, and the impedance measured by the TDR oscilloscope equals Z_1 / N, with the delay of each trace being equal to the delay measured by TDR (Figure 12).

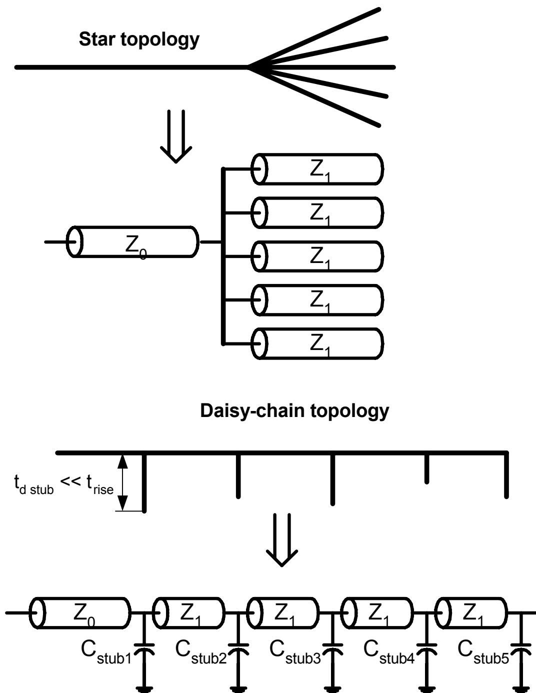


Figure 12. Taking TDR measurements of splits in a star topology and stubs in a daisy-chain topology

In case of a stub (which often takes place in a daisy chain configuration), if the length of each stub on the main bus is much shorter than the rise time of the signal propagating through the bus, the stub can be treated as lumped capacitances loading the main bus, thus simplifying the measurement problem.

TDR Probing and Fixturing

TDR is delivered to the DUT via electrical cable, probe, and fixture interconnects. The quality of these interconnects is the key to obtaining a good measurement. As noted before, poor quality cabling and probes can degrade the TDR rise time and decrease the resolution of the instrument. In addition, when computing the impedance profile, it is necessary to have a clean reference short or open waveform; without a good reference, we are not likely to get a clear signature of the DUT. Because of these factors, good quality microwave probes and cables are required to obtain a good quality TDR measurement.

Fixtures, probes, and probing stations for package failure analysis work are available from various manufacturers. A full-featured failure analysis probing station can provide easy viewing and access to the package with a probe, and enable a failure analyst to perform at-temperature analysis of the package failures.

TDR cables and probes will degrade the rise time of the signal measured on the TDR oscilloscope approximately as follows:

$$t_{measured} = \sqrt{t_{TDR}^2 + 2 \cdot \left(\frac{0.35}{f_{3dB}}\right)^2} \qquad (2)$$

where t_{TDR} is the rise time measured on the TDR scope with no cable connected, and f_{3dB} is the 3dB bandwidth of the cable and probe. The factor of 2 in this equation is due to the fact that the signal has to take a roundtrip through the cable before it is observed and measured on the oscilloscope. Specifying a cable with a 3dB bandwidth (f_{3dB}) of about 10 Ghz for the scope with its own rise time of 30ps, will result in the rise time at the cable end of about 58ps. Specifying 3dB bandwidth of 17.5 Ghz will give the rise time end of the cable of about 40ps.

In an application where the TDR cable length can be limited to less than 2 ft, requesting a "lowest-loss" flexible cable from your favorite high quality low cost coaxial cable manufacturer would be sufficient. If you are working with a 3-4 ft cable, however, or require full resolution and rise time that the oscilloscope can offer, you will have to work with a high-end microwave cable manufacturer. Semi rigid cables can provide better performance than flexible ones, but are more difficult to use. SMA connector is commonly used in TDR cables, since it provides acceptable performance, and can be mated directly to the 3.5mm connector found on 20Ghz TDR sampling modules. For even faster rise time, a higher bandwidth microwave connector, such as 2.92mm or even 2.4mm may be required[1].

When using a probe for taking a TDR measurement on a package, the designer has to define a ground location near the signal location. If such ground location is not available, or if the spacing from signal to ground varies widely across the PCB, the designer may have to use a probe which has a long ground wire, or a variable length wire. For a probe with a long ground wire, the parasitic inductance will be very large, and will not allow the designer to obtain a good quality TDR measurement. Variable length ground wires, and variable pitch (signal-to-ground spacing) probes do not provide sufficient measurement repeatability, and will not provide accurate impedance measurement results or signal integrity interconnect models.

In many cases, a simple, inexpensive and convenient TDR probe can be obtained by using a 3 inch length of semi-rigid coaxial cable with an SMA connector, exposing the center conductor of such cable, and either using the sleeve of the semi-rigid coax as the ground contact, or attaching a ground wire. Using different diameter coax will result in different probe pitch, and making the center and ground conductors shorter or longer can provide the right trade-off between convenience of use and performance[2]. Such probes are also available commercially, Figure 13.

Figure 13. TDA Systems QuickTDR™ probe supported by Cascade Microtech EZProbe™ positioner. The spacing between signal and ground in the tip of the probe is extremely small to ensure best performance

A package fixture may be used to conveniently provide a connection to the balls or contact pads of the package. Such fixture must also ensure contact for the signal connection, and it also must provide a ground plane to allow accurate impedance measurement. (Figure 14). An automated version of such fixture may be even more beneficial for high-throughput fault isolation work.

A homemade version of the same fixture can be also made. However, the designer of such a fixture needs to ensure both good low-inductance connection to the signal pins and a good ground connection, such as provided in a commercial fixture shown on Figure 14.

[1]3.5mm connector is specified to operate to a 26.5 Ghz, whereas a typical SMA is rated to 12.5 or 18 Ghz. 2.92 mm connector is specified to 40 Ghz, and 2.4mm to 50 Ghz.

[2]However, a ground lead that is 10mm long will probably produce a 10nH parasitic inductance and pretty much destroy the measurement accuracy.

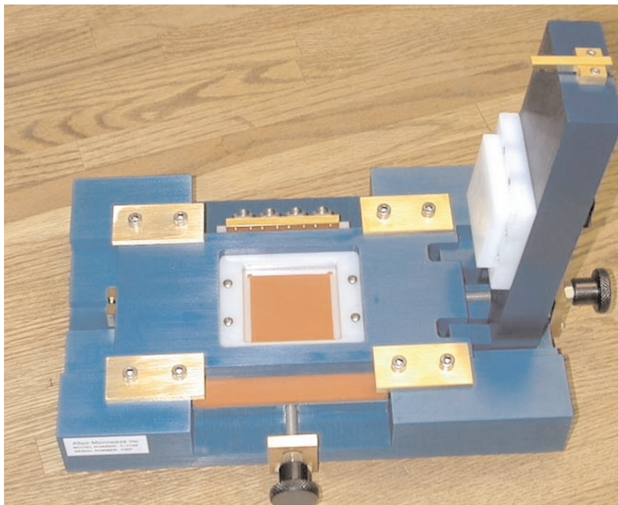
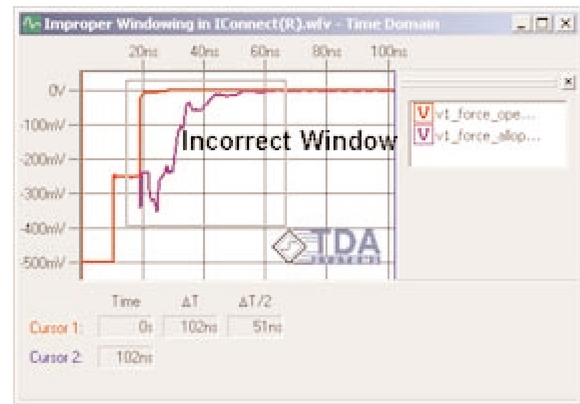


Figure 14. Altair Microwave BGA package probing fixture provides a high-frequency connection for four pins of the package simultaneously. The body of the fixture serves as the ground plane

Using Good Measurement Practices

To obtain good quality impedance, signal integrity modeling, and failure analysis data, it is important to follow general good measurement practices when using a TDR oscilloscope. The instrument should be turned on and its internal temperature should be allowed to stabilize for 20-30 minutes before performing any measurements. Calibration, compensation and normalization for the instrument must be performed regularly, as specified by the instrument manufacturer. The internal instrument temperature must be within the specified range from the calibration points for the given instrument.

To maximize the resolution of the scope, particularly in the time axis, it is important to zoom in on the DUT - but at the same time to allow a window that is sufficiently long to include all the reflections related to the DUT. A window that is too short may prevent the designer from obtaining complete and accurate information about the DUT. When the designer intends to perform true impedance profile analysis, as implemented in IConnect TDR software, it is also important to window out the transition related to the sampling head to the cable interface, and focus on the DUT portion of the waveform, so as to ensure that the impedance deconvolution algorithm, discussed above, could perform correctly.



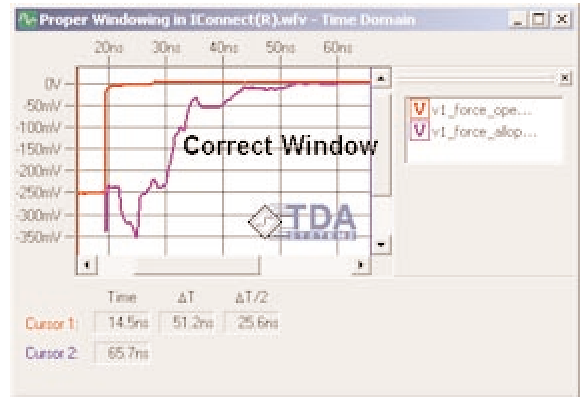


Figure 15. Proper windowing of the TDR waveform for further analysis in IConnect TDR software. The properly windowed waveform will exclude the first transition, corresponding to the interface between the TDR sampling head to the cable, but will keep the window sufficiently long to allow all the reflections corresponding to the DUT, to be included in the window

It is critical to use a torque wrench when mating any two connectors in your probing, cabling and fixturing setup. Such torque wrenches ensure a repeatable connection between the connectors, thus providing better measurement repeatability. These torque wrenches are available from most TDR manufacturers and many microwave component suppliers. It is also important to clean the RF connectors used in the probing / fixturing setup with isopropyl alcohol and lint free swab.

Failure Analysis Goals and Methods

The goal and the task of the failure analyst is to determine whether there is a possible connection failure in the given package trace, and what the exact position was when the failure occurred. Once the position of the failure is determined, further analysis can be performed to determine the physical cause and the nature of the failure, possibly with destructive analysis methods. Thus, in this scenario TDR is a fault isolation or a fault locator technique, allowing the failure analyst to quickly find the failure, and analyze it using other, possibly destructive, analysis techniques.

For example, the following picture illustrates how TDR was used to locate a short in a package.

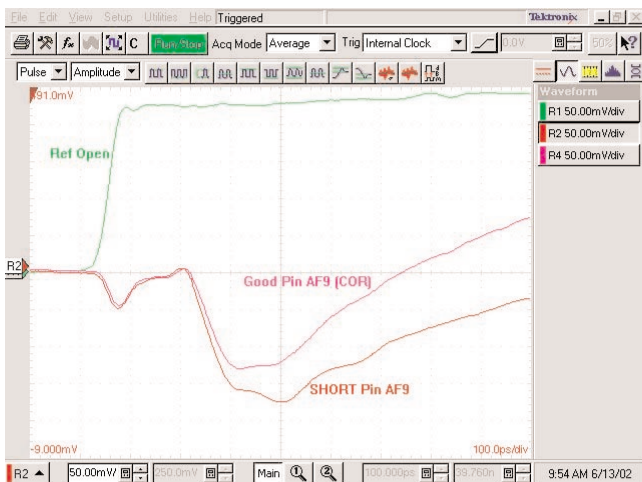


Figure 16. TDR result showing I/O short (AF9 and AE8) in a package

And the picture that follows shows an X-ray image of the same short failure.

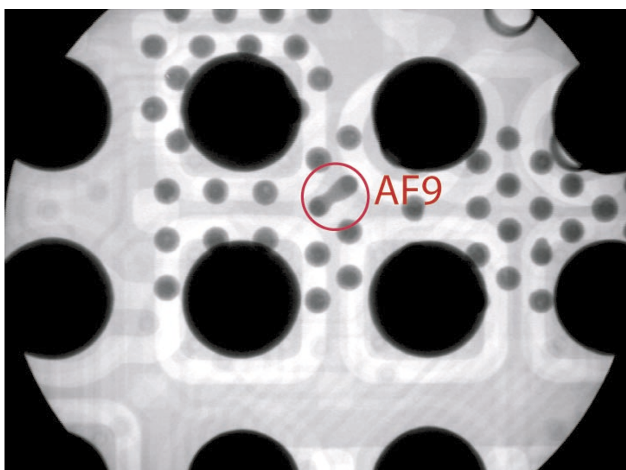


Figure 17. X-ray image of two solder bump shorts

The following four pictures are additional examples of TDR open signatures in a package, a short signature in a die, and corresponding optical images.

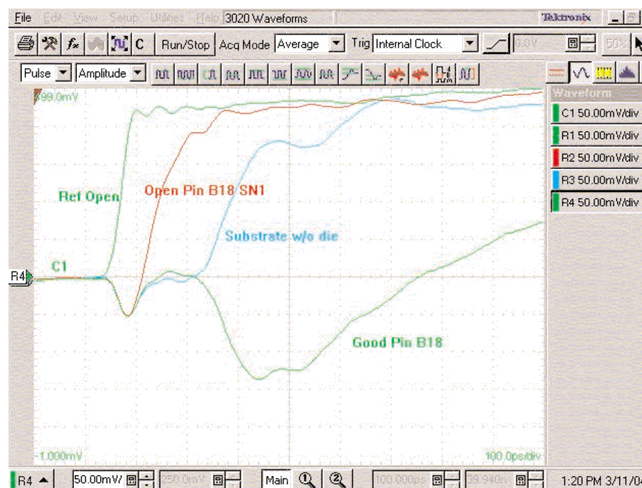


Figure 18. TDR result showing an open in the package substrate

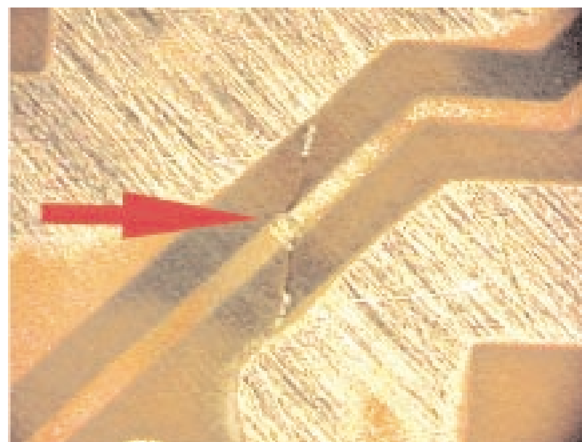


Figure 19. Optical image showing a broken trace in the package substrate

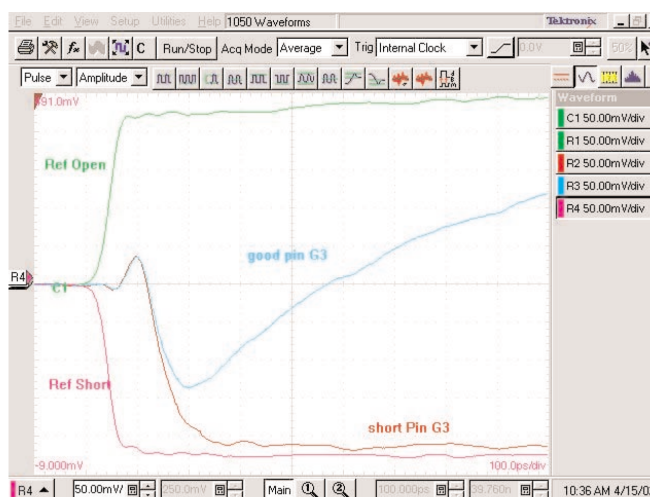


Figure 20. TDR result showing I/O short in the die

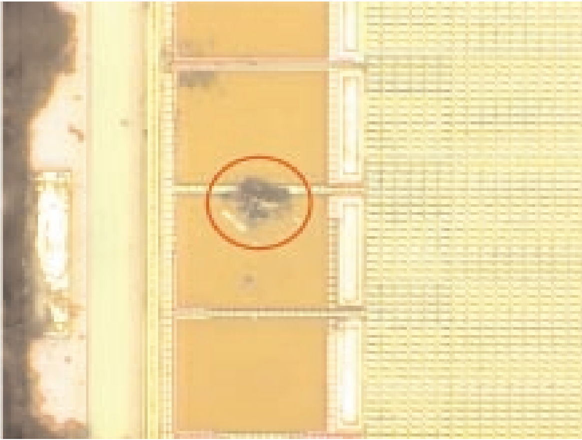


Figure 21. Optical photo of an EOS short in the die on pin G3

Typical approaches that can be used to determine whether there is a failure present are signature analysis, where the package trace true-impedance-profile data is analyzed for known failure signatures, and comparative analysis, where the package trace data is compared to the data of a trace in a known good package. Both approaches will be applied to the true-impedance-profile data obtained from the TDR using the impedance deconvolution algorithm as it is implemented in TDA Systems' IConnect® software.

As Figure 9 on page 4 indicates, the true-impedance-profile provides a much clearer picture of the failure type, and also enables the user to easily determine the exact position of the failure in an electrical sense, i.e., in terms of electrical length of the interconnect in picoseconds. Additional analysis must be performed to determine the physical location (in millimeters or milli-inches) of the failure with the goal of locating the package element that is failing. The true-impedance-profile provides the user with a way to correlate the TDR data to the specific layers in the package, as well as provide an estimate of a constant that would allow the user to convert the electrical length in picoseconds into physical lengths in mils.

Signature Analysis

In the true-impedance-profile, open and short failures can be easily identified as 0 Ohm or very low impedance readout for the short and very high (1000 Ohms or more) impedance readout for the open (Figure 6, Page 3). The exact electrical position of a short or an open can be easily identified in the true-impedance-profile, even in the presence of multiple reflections, as previously described.

In the following example (Figure 22), the known good BGA package (ZlineGood.wfm) was analyzed alongside a suspect package (ZlineBad.wfm). The fixture-impedance-profile (ZlineFixture.wfm) is shown for reference. The known good package impedance profile ends with a large capacitive dip, corresponding to the input package capacitance. An open failure is clearly observed in the BGA package at about 80 ps inside the package (160 ps roundtrip delay).

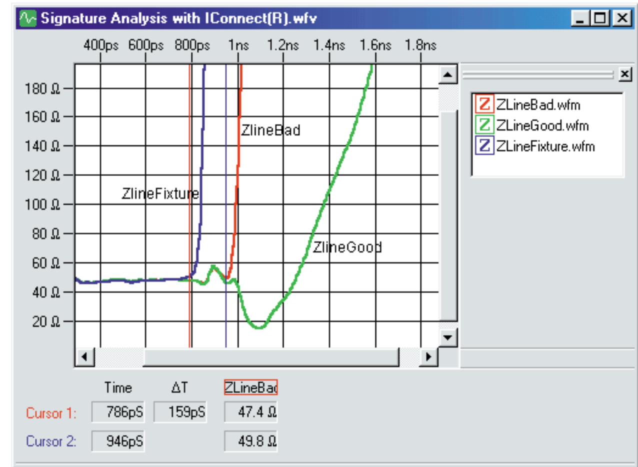


Figure 22. Signature analysis of a BGA package failure using the true-impedance-profile in IConnect

So called "soft" failures, i.e., partly shorted or partly open leads, can also be identified using the signature analysis, but their impedance profile and TDR signatures must be identified beforehand. The only alternative to knowing the soft failure signature beforehand is to observe the changes in capacitance of the known good device compared to the failing device.

TDR has specific signatures for the open and short connections, as shown in Figure 6, and can also be used for identifying the failures. However, in multi-segment structures, such as BGA packages, the exact location of the failure can be difficult to determine because of the multiple reflection effects. This is why we want to emphasize the importance of using the true impedance profile when performing fault isolation on electronic packages.

Comparative Analysis

Comparative package failure analysis, as the name implies, relies on comparison of the known good waveform to the suspect waveform. Even though some discrepancy between different measurements may still be observed due to measurement repeatability, comparative analysis utilizing the true-impedance-profile waveforms, computed using IConnect, yields very quick and intuitive results.

Consider the following example. In Figure 22, the package failure is identified as an open failure. In Figure 23, the analysis is continued by comparing the failed waveform to the package substrate waveform only, without connection to the die. The challenge is to determine what package component is failing based on this comparative analysis. Because the failed impedance profile waveform overlays directly over the substrate waveform, it is easy to deduce that the likely

failure source is the broken connection between the package and the die. Again, the large capacitive dip is due to the input capacitance of the die.

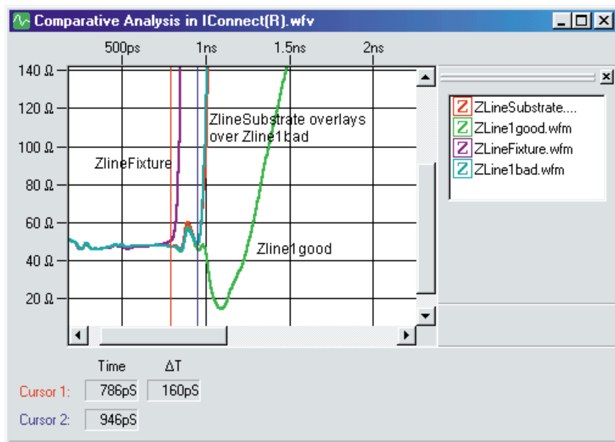


Figure 23. Comparative analysis for a BGA package. The bad impedance profile waveform clearly indicates an open failure signature. Comparing it to the package substrate waveform only without connection to the die, allows pin-pointing the likely failure source - a broken connection to the die

Based on this analysis, a failure analyst can focus on the connection to the die area, and use additional failure analysis techniques to determine the physics of the failure.

Thus, in comparative analysis at the very least we need to have a known good device. For a typical package, one of the key impedance profile features differentiating an open fault in the package or bondwire from an open fault in the die itself is a dip in the impedance profile corresponding to ***an input die capacitance*** and presenting itself shortly before the open impedance signature. The presence of this characteristic dip in the impedance profile indicates a good connection to the die, whereas its absence indicates a problem in the package structure. Such a capacitive signature can be observed much more readily on the impedance profile waveform than on a raw TDR waveform. An additional known good bare package substrate can also be useful in identifying the exact location of the failure.

An important issue when performing comparative analysis is measurement repeatability. Following good general measurement practices, such as:

· maintaining TDR instrument calibration

· keeping the instrument well-warmed in a lab with constant ambient temperature

· maintaining the probe or cable position and spacing between the probe signal and ground during the measurement

will enable the analyst to minimize any non-repeatability errors. However, a failure analyst must be aware that small differences between different impedance profiles may actually result from measurement non-repeatability, rather than failures in the package under test.

For example, because of the differences between the good package impedance profile (ZlineGood.wfm) and bad package impedance profile (ZlineBad.wfm) in the outlined region of Figure 24, a failure analyst may view the differences between the good and bad waveforms in the selected region as the cause for the failure observed in the later portion of the impedance profile. However, because we are working with the impedance profile and not the TDR waveform, any effect of the reflections in the selected region on the rest of the impedance profile waveform is minimal. With that in mind, the differences between the two impedance profiles are too small to be viewed as the cause of the failure. And, one can comfortably conclude that the failure occurred in the later portion of the package (in this case, again, it is a failure of the package-to-die connection.)

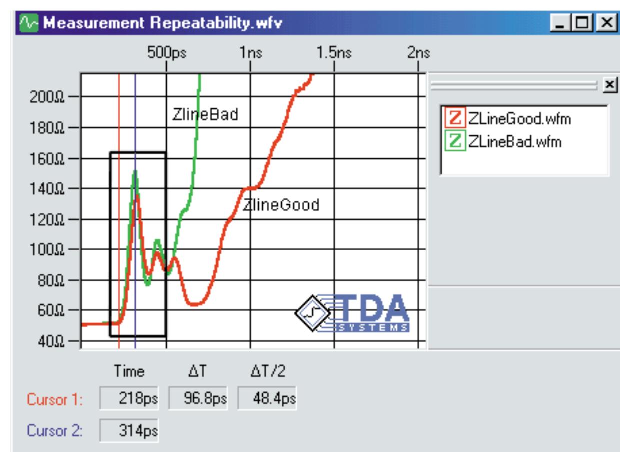


Figure 24. Measurement repeatability considerations

Additional Considerations for Package Open Failure Analysis

The true-impedance-profile is very powerful because it opens up other interesting venues for FA on electronic packages. For example, because the true-impedance-profile represents an exact signature of the DUT, one can now analyze the package impedance profile and quite easily correlate it to the physical layers in the BGA package, which can be observed in the package layout or drawing.

Consider the following two package samples with the following simplified trace layouts in Figure 25. The two packages are quite similar, except that the trace leading to the via connecting the package trace to the die is significantly longer for package 1. Both of these packages were analyzed with a TDR instrument and an impedance profile in IConnect. In both cases a good package sample and a sample with a failure of the connection between the package trace and the die has been analyzed.

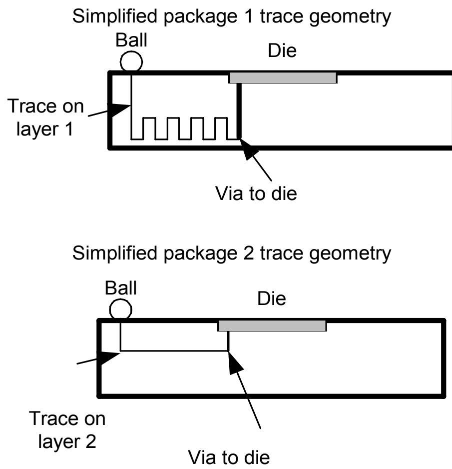


Figure 25. Sample package trace geometries used for correlation to the impedance profiles

The impedance profile enables a simple correlation to the package geometry (Figure 26). In package 1, the known good waveform (Zline1good.wfm) shows a segment with inductive behavior (estimated to be about 2nH in inductance), correlating to the long package trace, then a short segment correlating to the via, and then a segment correlating to the input capacitance of the die. When the connection to the die is broken, the corresponding waveform (Zline1bad.wfm) still shows the long trace in the package, but does not go into the capacitance of the die (estimated to be 800fF). Finally, the shorter second package trace correlates to the shorter section in the impedance profile waveform (Zline2good.wfm), whereas for the failed trace in package 2, the impedance profile goes up to high impedance at a much earlier point. The estimates for the inductance of the trace and input capacitance of the die match the expected numbers well, which provides further confirmation for the accuracy of the analysis of the failure type and location.

Once the correlation from the physical package structure to the impedance profile waveform has been determined, the location of the fault in the package can be found easily.

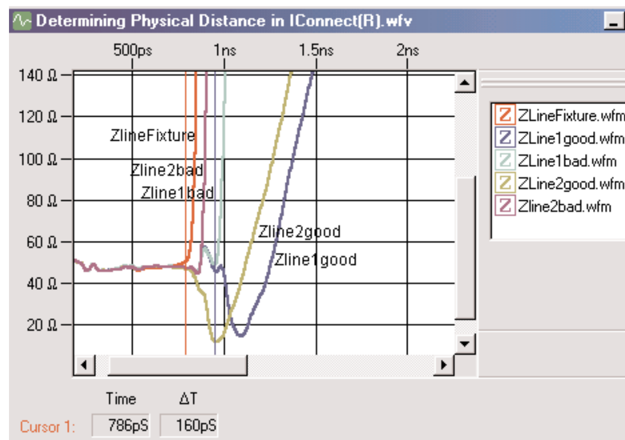


Figure 26. Layer correlation and distance analysis in IConnect based on the impedance profiles of two packages with similar layouts

In addition, since the overall physical length of the package trace can be quickly found from the package layout, and the impedance profile provides exact information about the electrical length of the package trace, this correspondence can provide a reasonably good estimate of the physical location of the failure. For example, if the package layout software gives a reading for the overall package trace length of l_{total} meters, and the true-impedance-profile shows that the package length is $t_{d\ total}$ seconds, then the average relative velocity of propagation through the package can be estimated as:

$$V_{prop\ average} = \frac{l_{total}}{t_{d\ total}} \cdot \frac{1}{V_C} \qquad (3)$$

where V_C is the speed of light. For example, the difference between the length of the traces in package 1 and package 2 is 45 ps (90 ps roundtrip). Based on the layout file data, the corresponding physical length is 10 mm, which provides an estimated relative velocity of propagation of 4.5 ps/mm, or 0.74 the speed of light.

In addition, if a correlation between an electrical position in seconds to the physical position in meters needs to be estimated, it can be done using the following equation:

$$l = t_d \cdot \frac{l_{total}}{t_{d\ total}} \qquad (4)$$

Using equation (4), one can estimate the relative position of the failure within a layer, if it is suspected that the failure actually occurred within a layer.

One can extend the computation above to determine the average dielectric constant ε_r through the package using the following equation:

$$V_{prop\ average} = \frac{V_c}{\sqrt{\varepsilon_{r\ average}}} \qquad (5)$$

where V_{prop} average is the average signal propagation velocity through the package, V_c is the speed of light in vacuum. We can rewrite this equation as:

$$\varepsilon_{r\ average} = \left(\frac{V_c}{V_{prop\ average}} \right)^2 \qquad (6)$$

Now, the computed ε_r value can be entered into the software, and the results can be displayed as impedance vs. physical length (millimeters, inches, or feet).

Clearly, equations (3) through (6) are only estimates. The propagation velocity will vary through the different layers in the package. To get a more accurate value for the propagation velocity one needs to do extensive characterization of the package substrate material, as well as other characteristics. Such characterization is very time consuming and requires that special test structures be laid out on the material under test ([11, 12]). Because of such complexity, the exact data about the velocity of propagation through the separate package layers is rarely available to a failure analyst. A much easier approach is to correlate the layers in the package to the segments in the true-impedance-profile and use equation (3) to estimate the propagation velocity in each layer. However, sufficient resolution of the TDR instrument is required to resolve the layers, which can be on the order of 10 ps or less in length.

An attractive approach for a failure analyst could be to model the package under test, and then attempt to predict the TDR waveform of the package trace via SPICE or full-wave circuit simulations. The problem with this approach is, again, that the properties of the package material must be known with a reasonably high level of accuracy in order to ensure that the simulation predicts the TDR waveform correctly, unless the package model has been directly extracted from TDR measurement.

Signal-to-Ground Short Failures

Experiments have demonstrated that a signal to ground plane short can be located relatively easily using the same techniques as those used for locating an open fault. Since the trace has a certain amount of characteristic impedance, a short failure will clearly exhibit itself on the true impedance profile, as a rapid decrease in impedance until this impedance reaches zero Ohm.

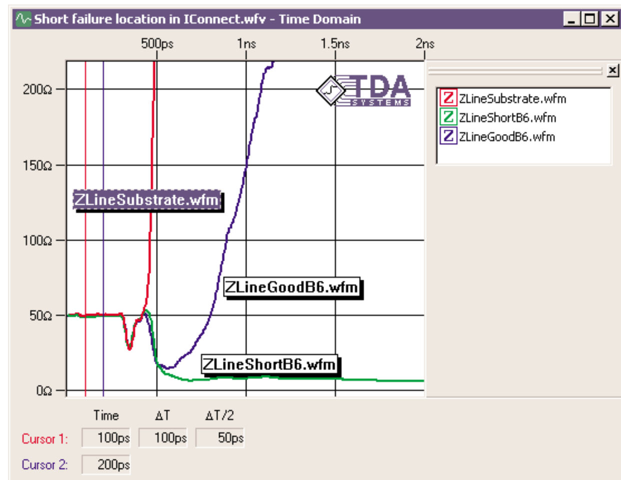


Figure 27. Locating a signal to plane short failure using the impedance profile signature. By comparing the short waveform (ZlineShortB6.wfm) to the substrate waveform (ZlineSubstrate.wfm), one easily concludes that the short is located near the connection to the die

Since in Figure 27 we can observe that the short waveform goes towards zero Ohm right where the bare package substrate waveforms goes into an open (high impedance), and right before the good device waveform goes to the die capacitance, we conclude that the short is located at or near the connection to the die.

In this example, the electrical length is 63ps, and the physical length is 8.7mm, which gives an average propagation velocity of 7.24ps/mm or 0.138mm/ps. Using this number, and knowing that the speed of light in vacuum is 0.305 mm/ps, we obtain the average ε_r of 4.9. Then, one can display the data in the software as impedance versus physical time.

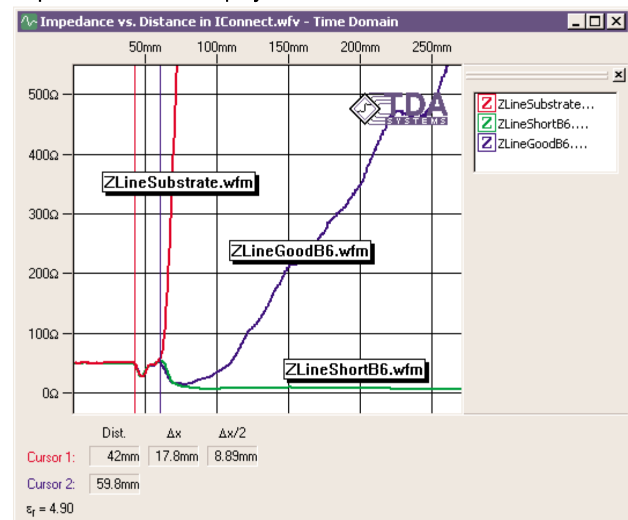


Figure 28. Impedance vs. distance in IConnect TDR software. The fault occurred about 63ps or 14mm inside the package

The actual dielectric constant (ε_r) for the substrate has been measured to be 4.2 at 1 MHz, which comes from the material property data provided by the substrate vendor. Using ε_r=4.2 to recalculate the physical length, the measured total length of the trace is 9.4 mm, which is very close the actual CAD layout length of 8.7 mm (~8% error). It is a very good correlation, considering that the ε_r would be higher at higher frequency for the TDR measurement, and that we are looking for the average ε_r through the whole package. The localized ε_r variations, non-homogeneity, effects of different conductor shape, all contribute to the difference between the vendor supplied ε_r and the measured value. However, the overall correlation we observe is considered to be quite good.

Plane-to-Plane Short

Locating a plane-to-plane short, such as ground plane to power plane short, is a more difficult task. In the case of a signal trace, the characteristic impedance of such a trace is normally in the range of 30 to 80 Ohms, and observing the change from this range to zero Ohm in the impedance profile waveform is relatively easy. The power plane, however, presents much lower impedance to the TDR signal, typically on the order of less than 0.5-2 Ohm, and the change from that impedance to zero does not always allow the failure analyst to use the impedance profile effectively to find the exact location of the short between the planes using either time or distance.

In this paper, however, we propose two comparative techniques for plane-to-plane short location, both based on secondary information in the TDR data. One technique looks for the difference in the secondary reflections in the TDR waveform, and can be performed with the raw TDR data or using the true impedance profile. The second technique looks at the inductance of the current return path, which can be computed using IConnect software, based on the JEDEC standard described in [13, 14]. Smaller inductance indicates a shorter distance to the short, and by comparing the failing device measurement to that of the good device and a shorted package substrate, one can determine the relative position of the short failure. For both techniques, repeating the measurements multiple times to ensure good repeatability is key to finding a fault.

Plane-to-Plane Short Test Example

Consider the following simple test board example (Figure 29):

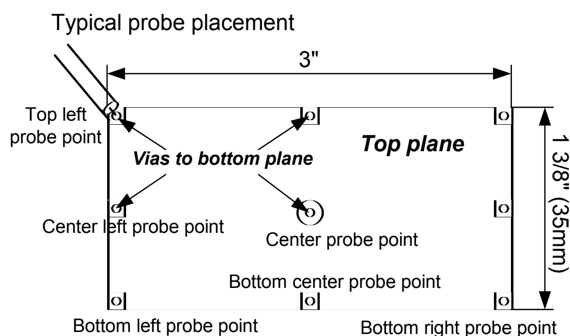


Figure 29. Test board for plane-to-plane short failure location. The board consists of two planes that can be probed with TDR at multiple locations at one side of the board and shorted at another side

This test board consists of two planes, which have via probe points at multiple locations on the board. Using these vias, the failure analyst can perform TDR measurements of the two planes on one side of the board, while at the same time shorting the planes at the other side and attempting to locate the position of the short. The board is about twice the size of a typical BGA package, which makes it an easier test case. The following table summarizes the expected closeness of the shorted probe point to the top left probe point, where the TDR signal is applied, based on visual analysis of the board.

	Left	*Center*	*Right*
Top	X	2	6
Center	1	4	7
Bottom	3	5	8

Table 2. Physical closeness of short point to the top left probe point (closest, 1 to farthest, 8), based on visual analysis

We applied signal every time at the same location (top left probe point), while creating a short between the planes by connecting the via from the bottom plane to the top plane contact. We shorted the two planes together at each of the remaining probe point locations and acquired the corresponding TDR waveform (Figure 30).

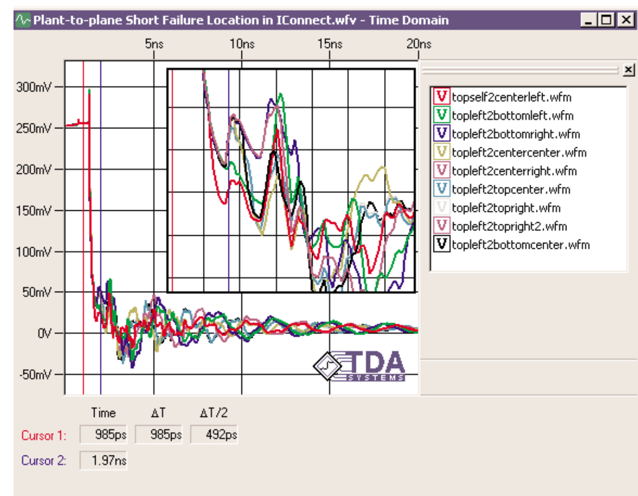


Figure 30. Locating plane-to-plane short on the test board. The fault location is based on the secondary TDR measurements, such as secondary reflection delay and inductance measurement

As one can see from Figure 30, there is little delay between the different waveforms. The inset, however, demonstrates, that the waveforms do exhibit a difference in position and waveshape. If a failure analyst tried to analyze this difference and determine which short is closer to the point where the TDR signal is applied, the following order could be established as shown in Table 3 (from closest short to the probe point to the farthest).

	Left	*Center*	*Right*
Top	X	4	5
Center	1	3	7
Bottom	2	6	8

Table 3. Electrical closeness of short point to the top left probe point (closest, 1 to farthest, 8), based on TDR measurement

By comparing these results with the expected results from Table 2, a failure analyst can observe a good correlation. The only questionable result is that the center top probe point comes after the center point. The difference between the two waveforms corresponding to those probe points, however, is small, and can be attributed to measurement repeatability issues.

To confirm our conclusions, we compute the total inductance of the plane for each measurement in IConnect software. This measurement is a good figure of merit for the current return path through the plane, which, in turn, is a good indicator of where the short may have occurred.

The following table summarizes the inductance data, listing the shorted probe point inductance measurements from the smallest to the largest. All the inductance measurements have been in 2-4 nH range.

	Left	*Center*	*Right*
Top	X	3	4
Center	1	5	7
Bottom	6	2	8

Table 4. Electrical closeness of short probe point to the top left probe point (from smallest inductance, 1 to largest, 8), based on inductance measurements in IConnect TDR software

Again, the center point and the bottom left point are outliers, but otherwise this table correlates well to the Table 2 of expected physical closeness.

These "outliers," or incorrect data points, may come from some minor details and changes in the current return path between the planes. Vias and other plane openings, such as those on the test board in question can affect this return path. All these issues indicate that the failure analyst must apply these techniques to plane-to-plane short analysis with the good understanding of the TDR measurement technique, and must study the layout and structure of the package carefully. Repeated measurements may be necessary in order to prove the actual location of the short.

As a final note, additional analysis using triangulation (making TDR measurements from three different points on the plane) would enable even easier location of the position of the short between the planes.

Summary, Conclusions and Future Work

In this paper, we discussed TDR measurement technology as it applies to the failure analysis of electronic packaging. We analyzed the impedance deconvolution algorithm, and demonstrated the advantages that the true-impedance-profile (resulting from applying this algorithm to the TDR data), provides for a package failure analyst over a simple TDR data set, for both signature and comparative package failure analysis. Additional analyses were presented, which can be performed on the true-impedance-profile, and that can further simplify the location of the failures in electronic packaging.

We have analyzed the application of the TDR measurement techniques and the true impedance profile to finding the location of signal-to-ground and plane-to-plane shorts in electronic packages. Locating a signal-to-ground short has been shown to present little difficulty over a comparable open fault locating task. Plane-to-plane shorts, however, present additional challenges, which require more attention to the repeatability and accuracy of the measurements. However, with the true impedance profile and plane inductance analyses, the claim of impossibility of locating a plane-to-plane short is effectively challenged in this paper.

For future work, more automated fixturing is required, which would enable the failure analyst to increase the throughput and locate more failures with less time invested. Faster rise time TDR modules can produce better resolution results and allow the analyst to locate the failure even more easily.

References

1. C. Odegard and C. Lambert, Comparative TDR Analysis as a Packaging FA Tool, – Proceedings from the 25th International Symposium for Testing and Failure Analysis (ISTFA), 1999

2. D. Bethke, W. Seifert, TDR Analysis of Advanced Microprocessors, – Proceedings from the 26th International Symposium for Testing and Failure Analysis, 2000

3. D.A. Smolyansky, Electronic Package Failure Analysis Using TDR, – Proceedings from the 26th International Symposium for Testing and Failure Analysis, 2000 (TDA Systems application note PKFA-0700)

4. D.A. Smolyansky, D. Staab, P. Tan, Signal Trace and Power Plane Shorts Fault Isolation Using TDR, – Proceedings from the 27th International Symposium for Testing and Failure Analysis, 2001 (TDA Systems application note PKSH-0102)

5. P. Viswanadham, P. Singh, Failure Modes and Mechanisms in Electronic packages, – Chapman and Hall (1998)

6. TDR Impedance Measurements: A Foundation for Signal Integrity, – Tektronix Application Note 55W-14601-0

7. Agilent High Precision Time Domain Reflectometry, – Agilent Application Note 1304-7

8. D.A. Smolyansky, TDR Testing Primer, – Printed Circuit Design Magazine, March 2002 (TDA Systems application note TDRP-0402)

9. L.A. Hayden, V.K. Tripathi, Characterization and modeling of multiple line interconnections from TDR measurements, – IEEE Transactions on Microwave Theory and Techniques, Vol. 42, September 1994, pp.1737-1743

10. C.–W. Hsue, T.-W. Pan, Reconstruction of Nonuniform Transmission Lines from Time-Domain Reflectometry, – IEEE Transactions on Microwave Theory and Techniques, Vol 45, No. 1, January 1997, pp. 32-38

11. D.A. Rudy, J.P. Mendelsohn, P.J. Muniz, Measurement of RF Dielectric Properties with Series Resonant Microstrip Elements, – Microwave Journal, March 1998, pp. 22-39

12. D. I. Amey, S.J. Horowitz, Tests Characterize High-Frequency Material Properties" – Microwaves and RF, August 1997

13. Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters, – JEDEC Publication #123, JC-15 Committee, October 1995

14. D.A. Smolyansky, TDR Techniques for Characterization and Modeling of Electronic Packaging, – High Density Interconnect Magazine, March 2001, Part 1 of 2 (TDA Systems application note PKGM-0101)

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© 2004 TDA Systems, Inc. All Rights Reserved
4000 Kruse Way Pl. #2-300, Lake Oswego, OR 97035 USA
Telephone: (503) 246-2272 Fax: (503) 246-2282
E-mail: info@tdasystems.com Web site: www.tdasystems.com

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