Tektronix

Enterprise Computing
HSS Standards Overview

Agenda

- 25GAUI-C2M
- SFP+
- SAS
- SATA
- USB

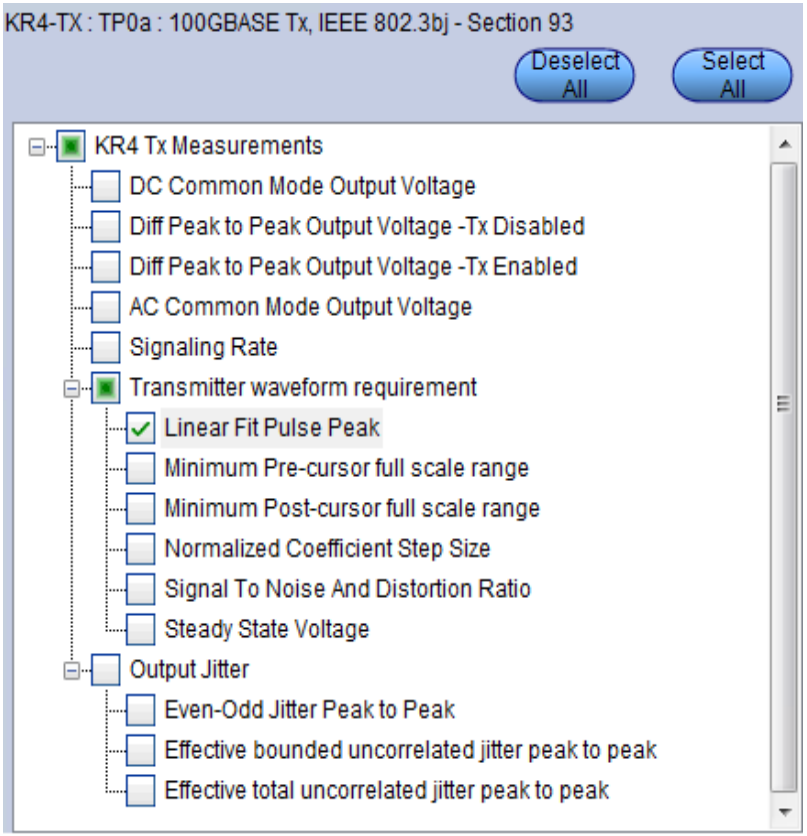
25GAUI

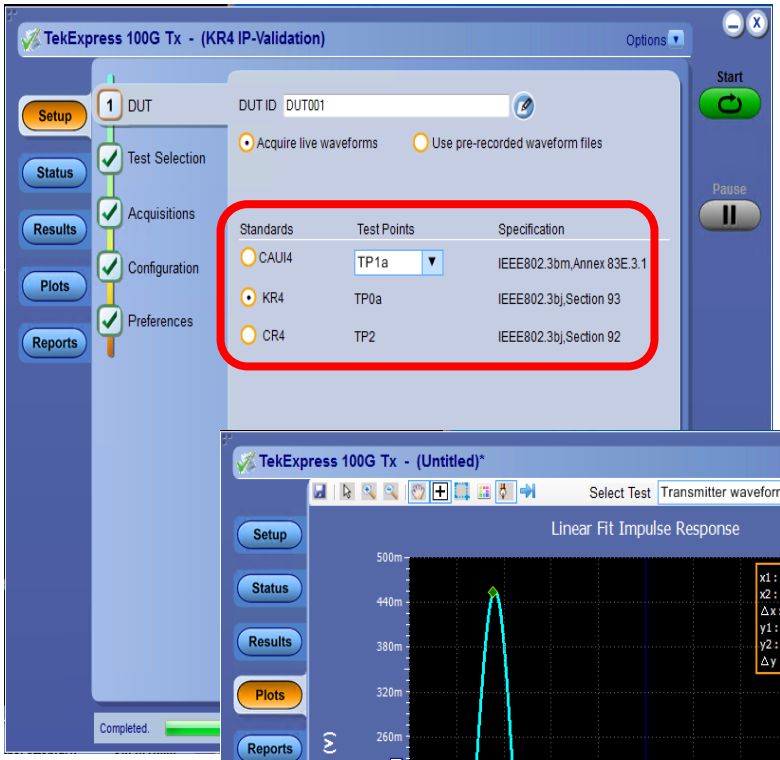
25GAUI Technology overview

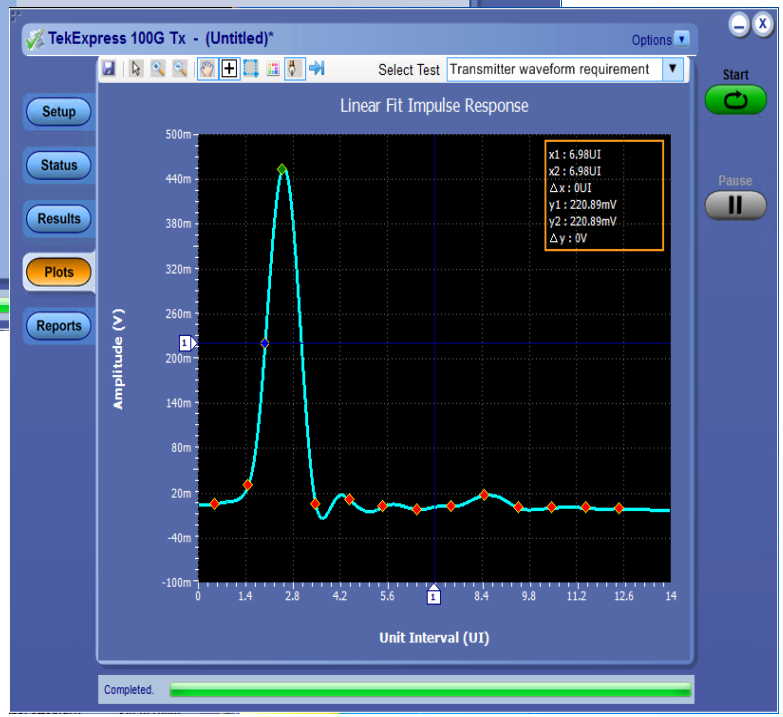
- Chip-to-Module 25G Attachment Unit Interface (25GAUI-C2M)
- Defined in 802.3by -2016
- Data Rate at 25.78125Gbps, single lane
- Key Chip vender- Intel(XXV Series) and Mellanox(ConnectX-4/5)
- Electrical Spec is the same as 100G CAUI-4 in 802.3-2015
- Connector SFP28
- Cabling- Copper(CR) or Optics(SR/LR)

CAUI4/25GAUI Compliance

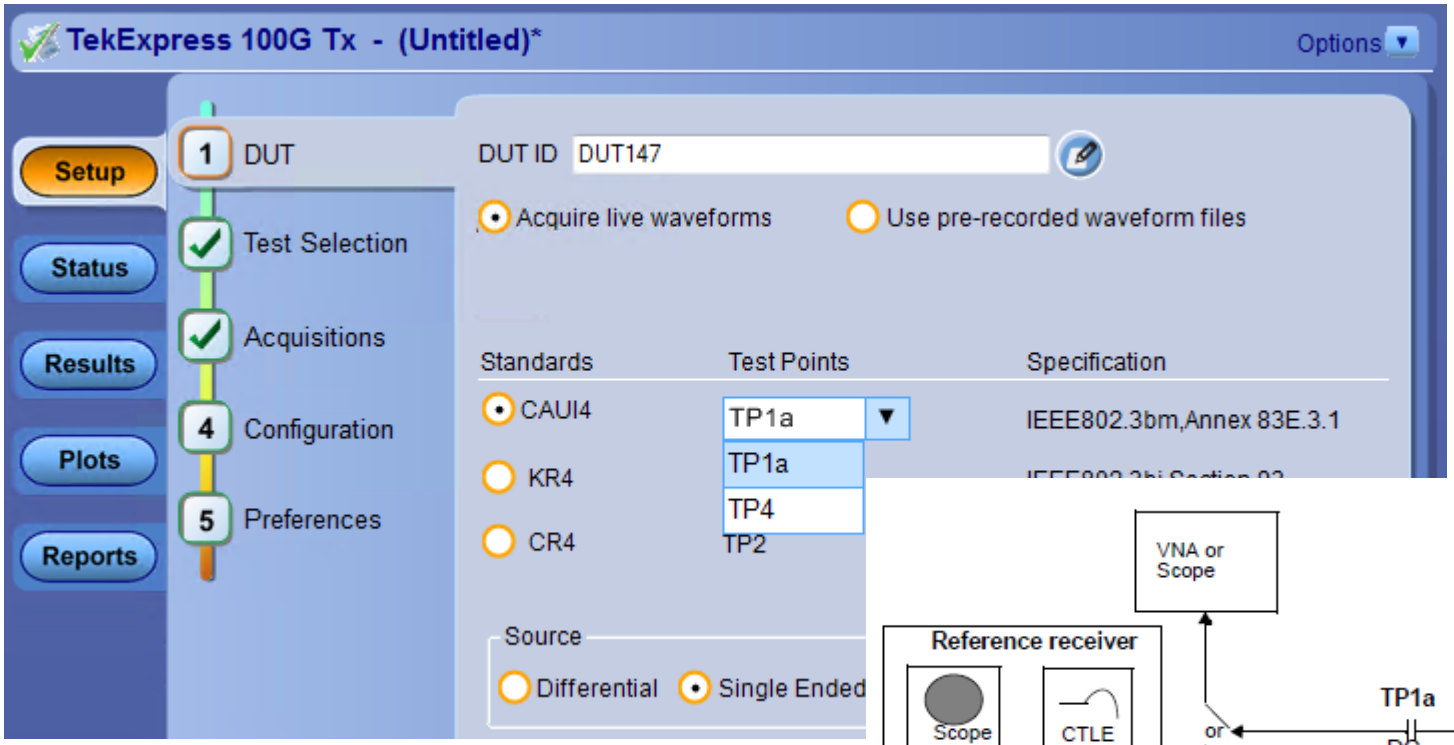
- Launched at OFC 2016, Tektronix introduces the most comprehensive 100G compliance tool set to date.







Test Point



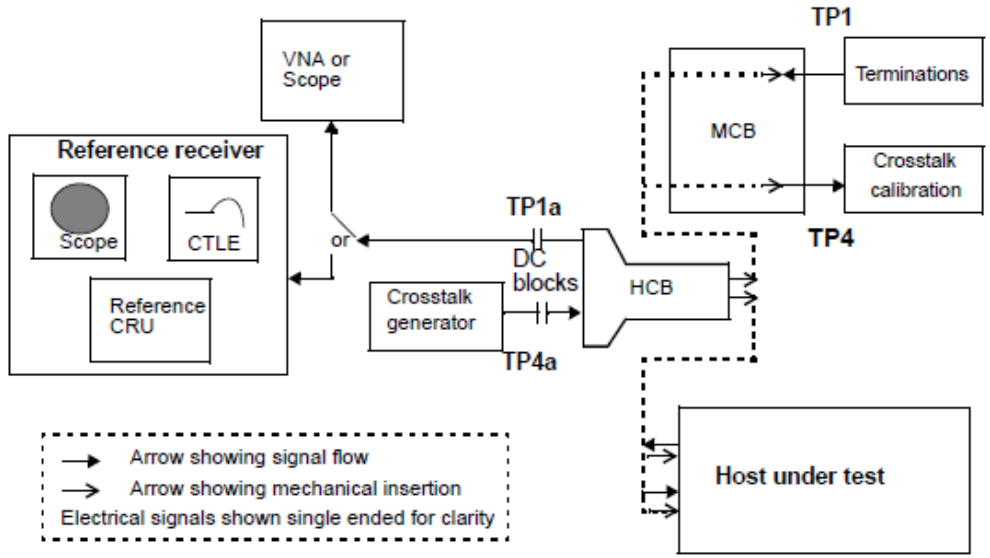


Figure 83E–9—Example host output test configuration

- TP1a: Host Tx Validation
- TP4a: NEXT Calibration
- SFP28/QSFP28 Fixture

Measurements Items

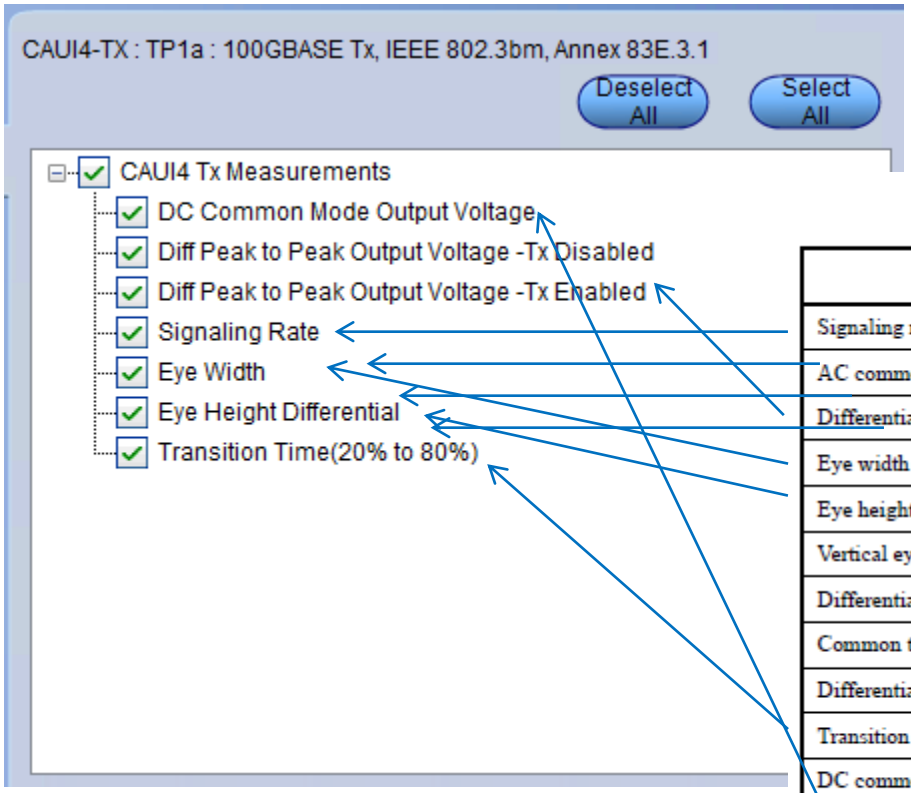


Table 83E–3—CAUI-4 module output characteristics (at TP4)

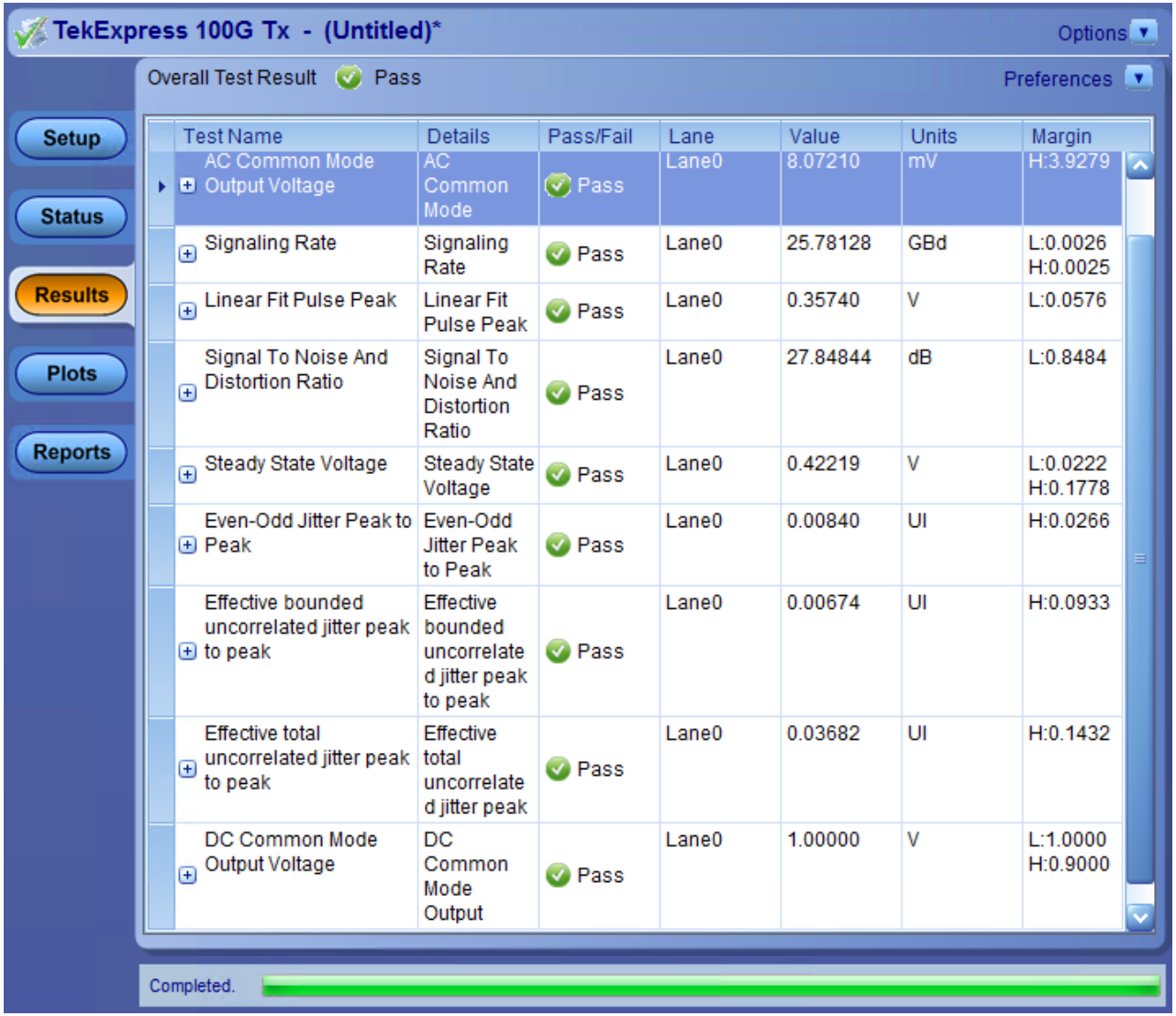
Parameter	Reference	Value	Units
Signaling rate per lane (range) ✓	83E.3.1.1	25.78125 ± 100 ppm	GBd
AC common-mode output voltage (max, RMS) ✓	83E.3.1.2	17.5	mV
Differential output voltage (max) ✓	83E.3.1.2	900	mV
Eye width (min) ✓	83E.3.2.1	0.57	UI
Eye height, differential (min) ✓	83E.3.2.1	228	mV
Vertical eye closure (max) ✓	83E.4.2.1	5.5	dB
Differential output return loss (min)	83E.3.1.3	Equation (83E–2)	dB
Common to differential mode conversion return loss (min)	83E.3.1.3	Equation (83E–3)	dB
Differential termination mismatch (max)	83E.3.1.4	10	%
Transition time (min, 20% to 80%) ✓	83E.3.1.5	12	ps
DC common mode voltage (min)[a] ✓	83E.3.1.2	–350	mV
DC common mode voltage (max)[a] ✓	83E.3.1.2	2850	mV

[a]DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage.

- The eye height and width have very specific population and extrapolation requirements. These are followed to the letter in the CAUI4 module.

Run Results

- Margin and test details are provided on a measurement by measurement basis.
- All Analysis is performed on post processed acquired and saved waveforms. Re-Run of measurements w/o DUT is an option



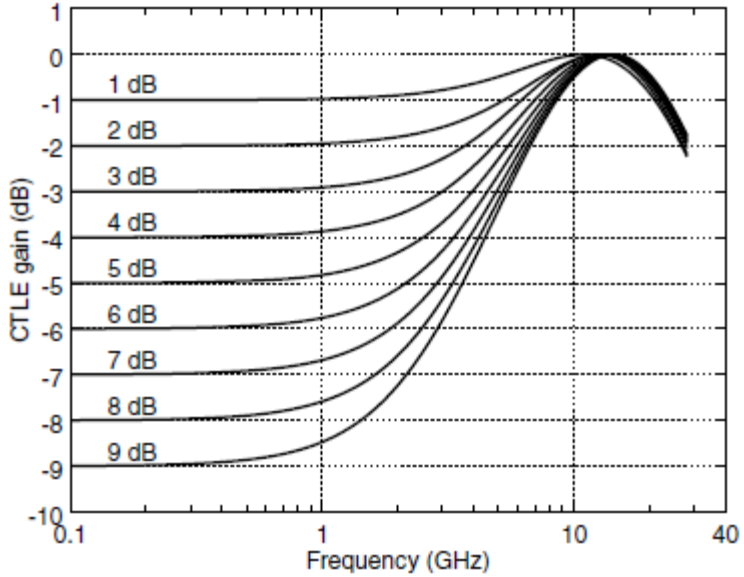
Test Name	Details	Pass/Fail	Lane	Value	Units	Margin
AC Common Mode Output Voltage	AC Common Mode	Pass	Lane0	8.07210	mV	H:3.9279
Signaling Rate	Signaling Rate	Pass	Lane0	25.78128	GBd	L:0.0026 H:0.0025
Linear Fit Pulse Peak	Linear Fit Pulse Peak	Pass	Lane0	0.35740	V	L:0.0576
Signal To Noise And Distortion Ratio	Signal To Noise And Distortion Ratio	Pass	Lane0	27.84844	dB	L:0.8484
Steady State Voltage	Steady State Voltage	Pass	Lane0	0.42219	V	L:0.0222 H:0.1778
Even-Odd Jitter Peak to Peak	Even-Odd Jitter Peak to Peak	Pass	Lane0	0.00840	UI	H:0.0266
Effective bounded uncorrelated jitter peak to peak	Effective bounded uncorrelated jitter peak to peak	Pass	Lane0	0.00674	UI	H:0.0933
Effective total uncorrelated jitter peak to peak	Effective total uncorrelated jitter peak	Pass	Lane0	0.03682	UI	H:0.1432
DC Common Mode Output Voltage	DC Common Mode Output	Pass	Lane0	1.00000	V	L:1.0000 H:0.9000

AUIx CTLE EH/EW Measurements

- Auto-indexing of CAUI4 CTLE's across the same acquisition indicates the optimum equalizer setting for Tx analysis.

Table 83E–2—Reference CTLE coefficients

Peaking (dB)	G	$\frac{P_1}{2\pi}$	$\frac{P_2}{2\pi}$	$\frac{Z_1}{2\pi}$
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099
3	0.70795	15.6	14.1	5.676
4	0.63096	15.6	14.1	4.9601
5	0.56234	15.6	14.1	4.358
6	0.50119	15.6	14.1	3.844
7	0.44668	15.6	14.1	3.399
8	0.39811	15.6	14.1	3.012
9	0.35481	15.6	14.1	2.672



CTLE Table			
CTLE Details	Eye Height (mV)	Eye Width (UI)	Eye Area (mV*UI)
CTLE_3dB.flt	306.174492219	0.686647528495	210.233958370
CTLE_4dB.flt	267.098617750	0.665374694316	177.720661137
CTLE_5dB.flt	223.408751846	0.643380134595	143.736752832
CTLE_6dB.flt	185.008694089	0.615838493614	113.935475473
CTLE_7dB.flt	153.567849476	0.594839176019	91.3481730454
CTLE_8dB.flt	124.297296866	0.573819046395	71.3241563572
CTLE_9dB.flt	99.1453613163	0.546318948738	54.1649895666

Back to Summary Table

Report Generation

- Full MHTML or PDF rendering of test reports.

Tektronix

TekExpress 100G Tx

Test Report CR4-TX (TP2)

Setup Information			
DUT ID	DUT147	Master Scope Information	DPO77002SX , PQ100011
Date/Time	2016-05-03 16:02:44	Master Scope F/W Version	10.2.0 devBuild 6
TekExpress Version	100GTx 0.0.0.130 (Evaluation Version) Framework: 4.0.5.248	Master Scope SPC Status	INIT
Specification Version	IEEE 802.3bj, Section 92	Extension-1 Scope Information	DPO77002SX , PQ100013
Compliance Mode	True	Extension-1 Scope F/W Version	10.2.0 devBuild 6
Execution Mode	Live	Extension-1 Scope SPC Status	INIT
Overall Test Result	Pass		
Overall Execution Time	0:04:57		
DUT COMMENT:	100G Tx CR4		

Test Name Summary Table	
DC Common Mode Output Voltage	Pass
Diff Peak to Peak Output Voltage -Tx Enabled	Pass
AC Common Mode Output Voltage	Pass
Signaling Rate	Pass
Linear Fit Pulse Peak	Pass
Signal To Noise And Distortion Ratio	Pass
Steady State Voltage	Pass
Even-Odd Jitter Peak to Peak	Pass
Effective total uncorrelated jitter peak to peak	Pass
Effective bounded uncorrelated jitter peak to peak	Pass

DC Common Mode Output Voltage

Measurement Details	Lane	Iteration	Measured Value	Test Result	Margin	Low Limit	High Limit	Units	Comments
DC Common Mode Output Voltage	Lane0	0	1.00000	Pass	L:1.0000 H:0.9000	0	1.9	V	N.A
COMMENTS	DC Common Mode Output Voltage is measured using multimeter								

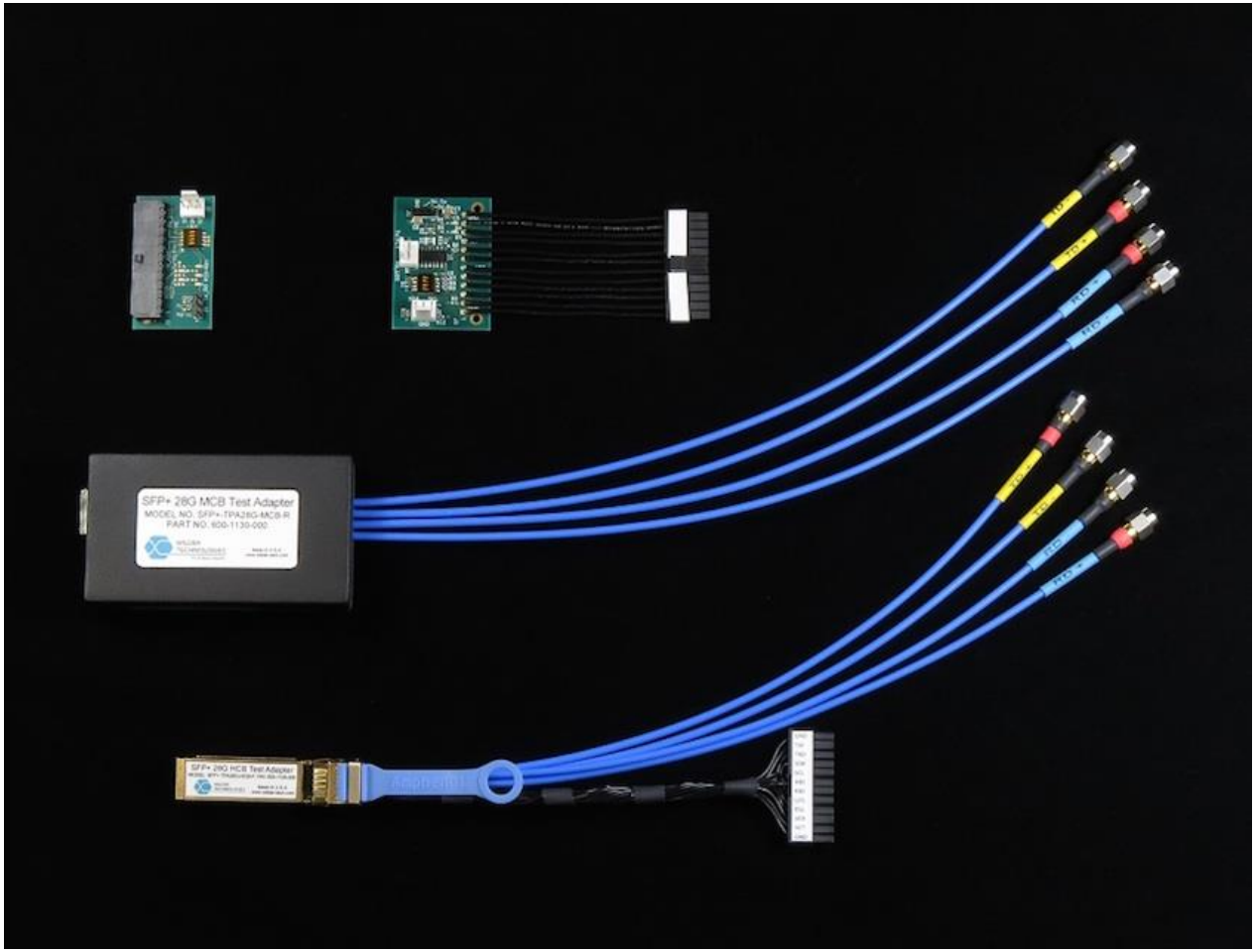
Back to Summary Table

Diff Peak to Peak Output Voltage -Tx Enabled

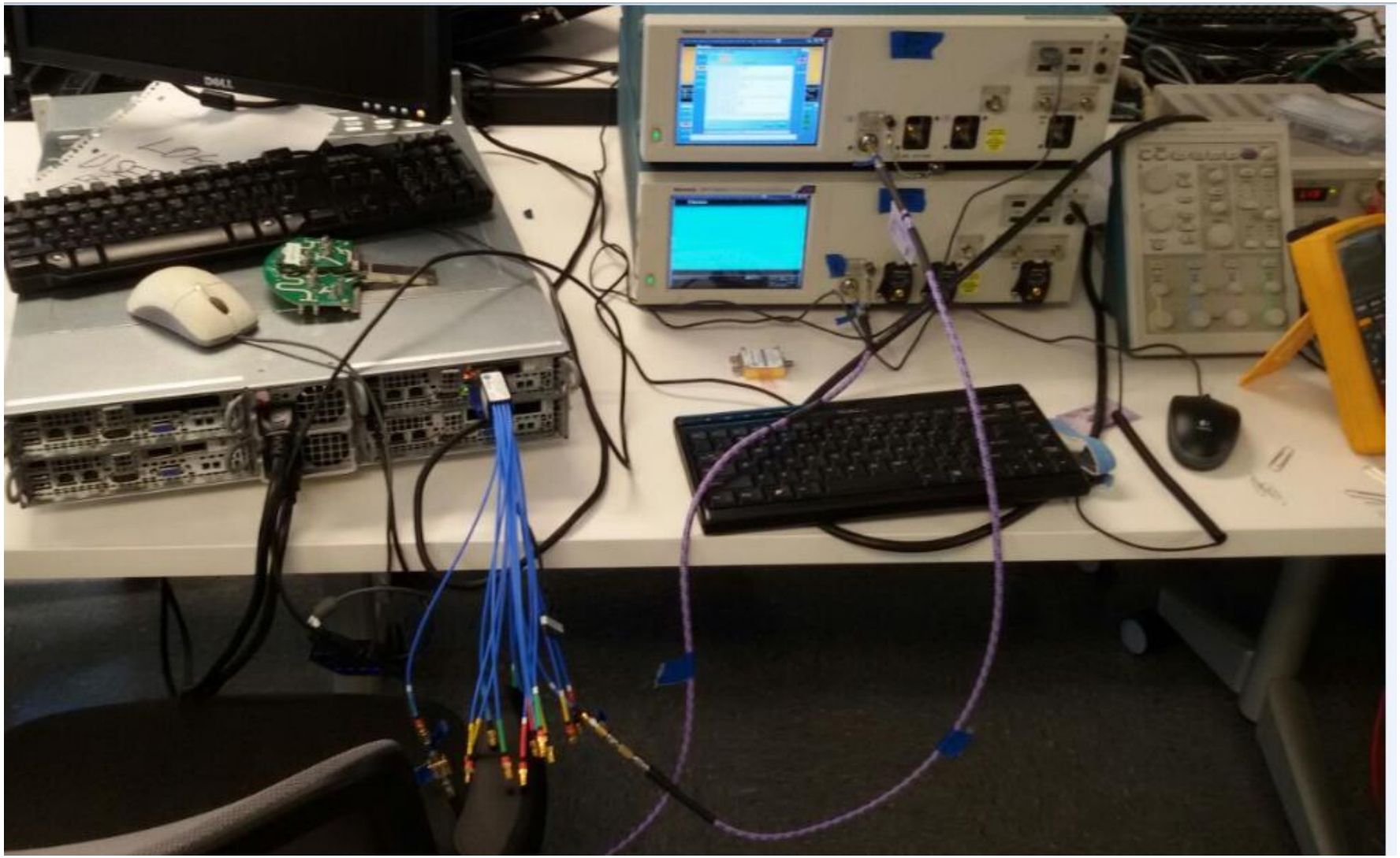
Measurement Details	Lane	Iteration	Measured Value	Test Result	Margin	Low Limit	High Limit	Units	Comments
Diff Peak to Peak Output Voltage -Tx Enabled	Lane0	0	949.72940	Pass	H:250.2706	N.A	1200	mV	N.A
COMMENTS	Pattern type PRBS9								

DPOJET 100G-TXE plugin measurements

SFP28 Fixture



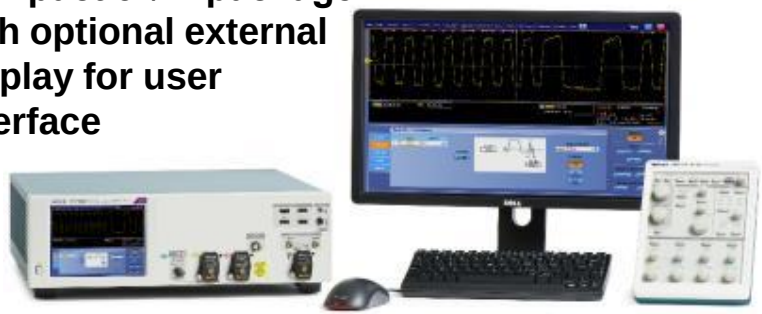
Tx Electrical Interop &Validation



70KSX Scalable Performance

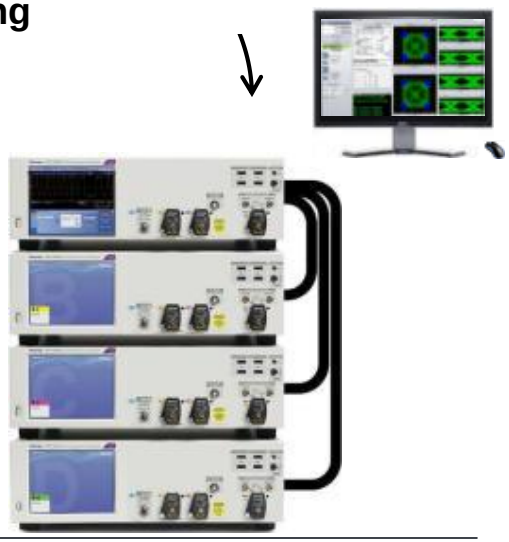
- Compact instrument for increased configuration flexibility
- UltraSync high performance synchronization for multi-unit configurations

Compact 5 ¼” package with optional external display for user interface



Additional performance using multiple units

Configuration flexibility with precisely-synchronized timing



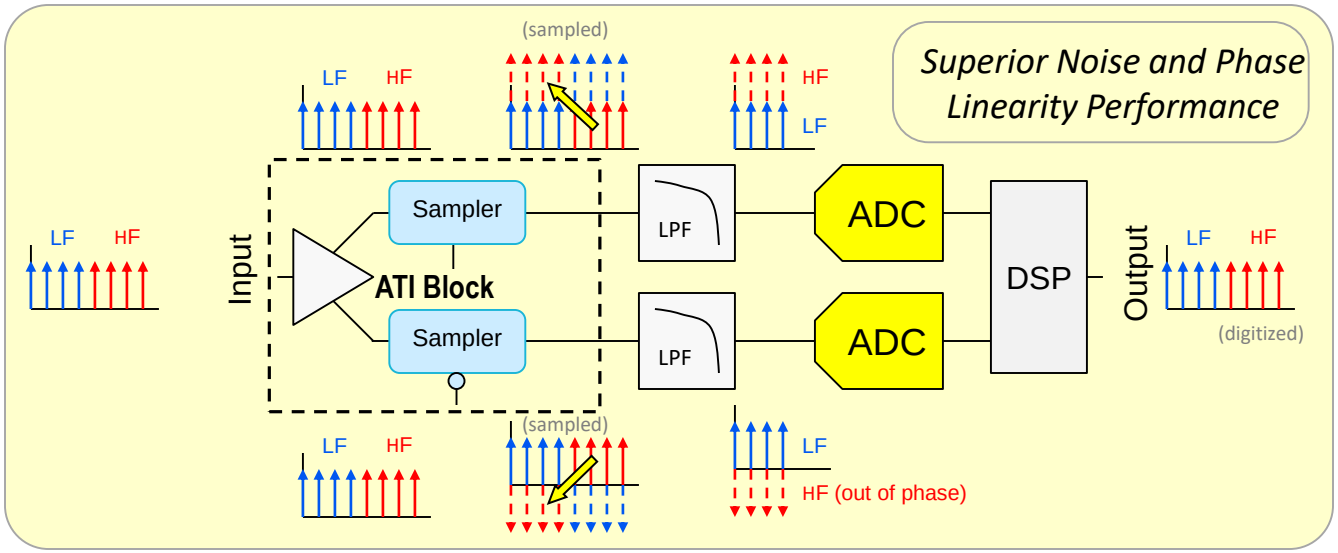
UltraSync High Performance Synchronization & Control bus

- 12.5 GHz Sample Clock Reference
- Coordinated Trigger
- High speed data path
- 2X 70GHz channels
- 4X 33GHz channels

Comparing Methods: Tek Acquisition Advantage

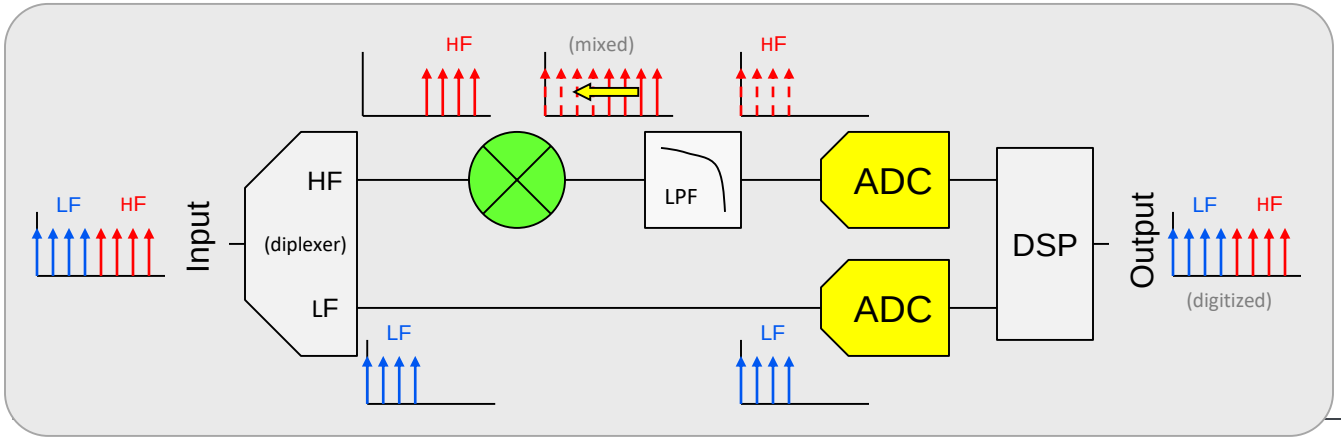
Superior Noise Performance for High-Bandwidth Data Converters

Tektronix Architectural Innovation



- ✓ **Improved SNR**
  - Each ADC sees full spectrum
  - Signal reconstruction involves *averaging* → improves SNR and Phase Linearity
- ✓ **Signal-path symmetry**
- ✓ **Patented architecture**

Asymetric Frequency Interleaving

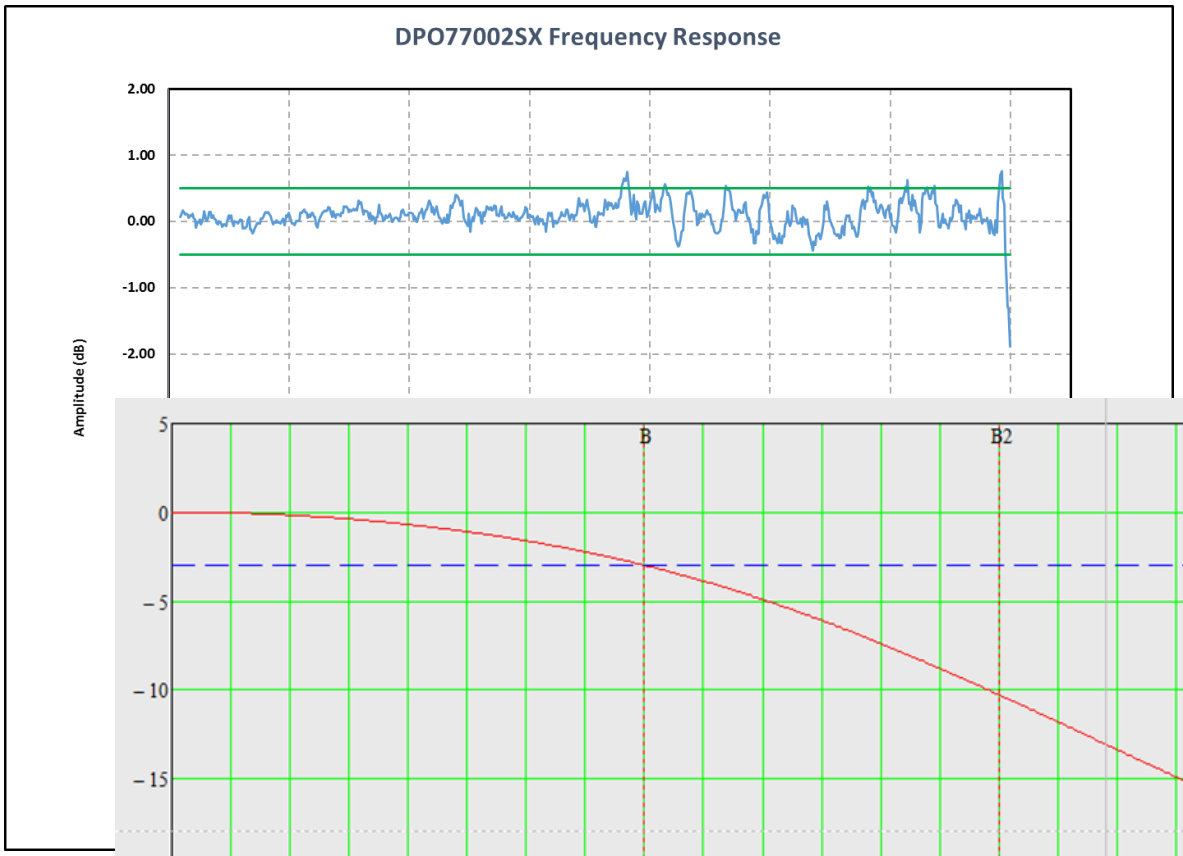


- Each ADC sees **half** spectrum
- Signal reconstruction involves *summation* → no improvement in SNR

Tektronix DPO77002SX Frequency Response

Flat intermodulation overlap zone offers the cleanest, low noise acquisition system available today.

Bandwidth to 70GHz can be channel modeled in DSP to map precisely to the 40G Bessel Thompson response required by OIF-CEI physical layer measurements today.

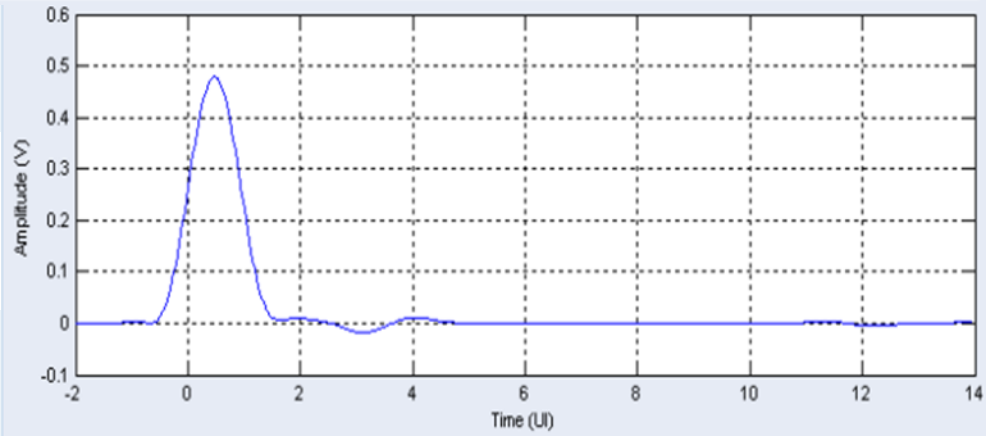


Tektronix DPO77002SX SNDR

Results

SNDR :	34.2744	dB	Peak :	477.8255	mV
Sigma_e:	7.7356	mV	Sigma_n:	5.0488	mV

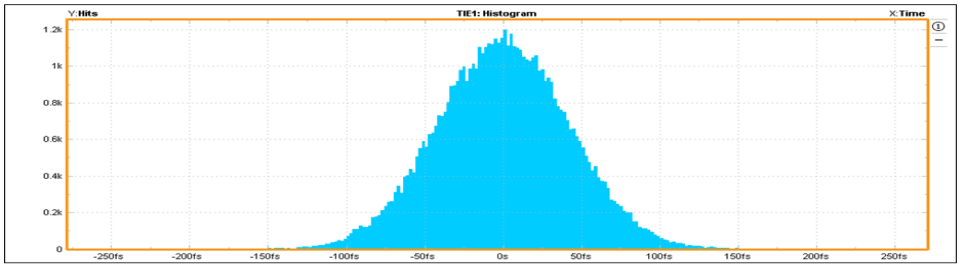
$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right) dB$$

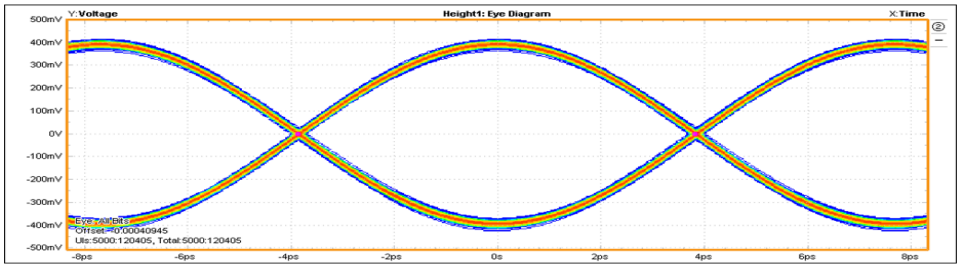


- The ATI acquisition architecture (low noise, flat phase response, high bandwidth with flat magnitude response) offers a unique ability to perform the 100G and forward looking 400G Signal to Noise and Distortion Ratio (SNDR) computations, with a level of precision only found in a similar bandwidth Sampling Oscilloscopes.

Tektronix 100G/400G Signal Acquisition Systems

Equivalent Time Signal Acquisition • Real Time Signal Acquisition Software Control and Analysis





Real Time

- Multi channel time synchronized operation.
- Advanced analysis CTLE/DFE and Complex Math.
- Complex modulation analysis tools.
- Unprecedented jitter noise floor.
  - ~ 40fs RMS clock jitter (64 GHz clock)
  - <125fs jitter noise floor (64Gbps PRBS)

Measurement Results

Hide Current Aquisitions | Summary View

Description	Mean	Std Dev	Max	Min
TIE1, Math4	4.4985as	41.903fs	159.37fs	-167.66fs
Current Acquisition	4.4985as	41.903fs	159.37fs	-167.66fs
Height1, Math4	729.78mV	0.0000V	729.78mV	729.78mV
Current Acquisition	729.78mV	0.0000V	729.78mV	729.78mV
TJ@BER1, Math4	573.74fs	0.0000s	573.74fs	573.74fs
Current Acquisition	573.74fs	0.0000s	573.74fs	573.74fs
RJ–δδ1, Math4	38.441fs	0.0000s	38.441fs	38.441fs
Current Acquisition	38.441fs	0.0000s	38.441fs	38.441fs
DJ–δδ1, Math4	35.570fs	0.0000s	35.570fs	35.570fs
Current Acquisition	35.570fs	0.0000s	35.570fs	35.570fs
Width@BER1, Math4	14.811ps	0.0000s	14.811ps	14.811ps
Current Acquisition	14.811ps	0.0000s	14.811ps	14.811ps
PJ1, Math4	80.938fs	0.0000s	80.938fs	80.938fs
Current Acquisition	80.938fs	0.0000s	80.938fs	80.938fs
DJ1, Math4	83.367fs	0.0000s	83.367fs	83.367fs
Current Acquisition	83.367fs	0.0000s	83.367fs	83.367fs
RJ1, Math4	38.441fs	0.0000s	38.441fs	38.441fs
Current Acquisition	38.441fs	0.0000s	38.441fs	38.441fs
DDJ1, Math4	0.0000s	0.0000s	0.0000s	0.0000s
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s

Source Reference Levels

Source	Autoset Method	Rise High	Rise Mid	Rise Low
Ch1	Auto	70.16mV	400uV	-69.36mV
Ch2	Auto	-44.04mV	-114.6mV	-185.16mV
Ch3	Auto	1V	0V	-1V
Ch4	Auto	1V	0V	-1V
Math1	Auto	1V	0V	-1V
Math2	Auto	-80.697mV	-302mV	-523.31mV
Math3	Auto	209.4mV	982.61uV	-207.43mV
Math4	Auto(Low-High(full wfm))	308.9mV	-409.45uV	-309.72mV
Ref1	Auto	1V	0V	-1V
Ref2	Auto	1V	0V	-1V
Ref3	Auto	1V	0V	-1V
Ref4	Auto	1V	0V	-1V

Miscellaneous Settings

	Gating	Qualify	Population
State	Cursors	Off	Off
Source	--	--	--
Size	--	--	--

Pattern Length

Source	Data Rate	Pattern Type	Pattern Length
MATH4	130.00Gb/s	Repeating	2UI

25GAUI Receiver Testing Challenge

- EW/EH at 10E-15
- Reference CTLE 1dB/2dB
- PLL corner Freq 10MHZ, slope 20dD/decade
- Calibration Pattern PRBS9
- Required Scope 3dB BW 33GHZ,
  with 4th BT filter

Table 83E–6—Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI

[a]Total Jitter at BER of 10^{-15}
[b]Random Jitter at BER of 10^{-15}
[c]As defined in 92.8.3.8.1

Table 83E–5—Host stressed input parameters

Parameter	Value
Eye width	0.57 UI
Applied pk-pk sinusoidal jitter	Table 88–13
Eye height	228 mV

Table 88–13—Applied sinusoidal jitter

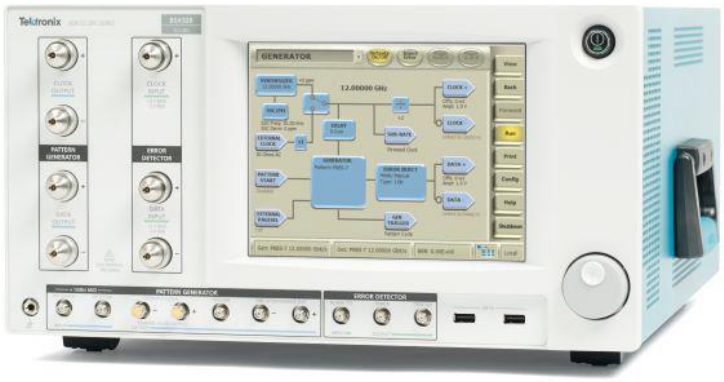
Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 100$ kHz	Not specified
100 kHz $< f \leq$ 10 MHz	$5 \times 10^5 / f$
10 MHz $< f <$ 10 LB[a]	0.05

[a]LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

Tektronix 25GAUI Receiver Testing Solution

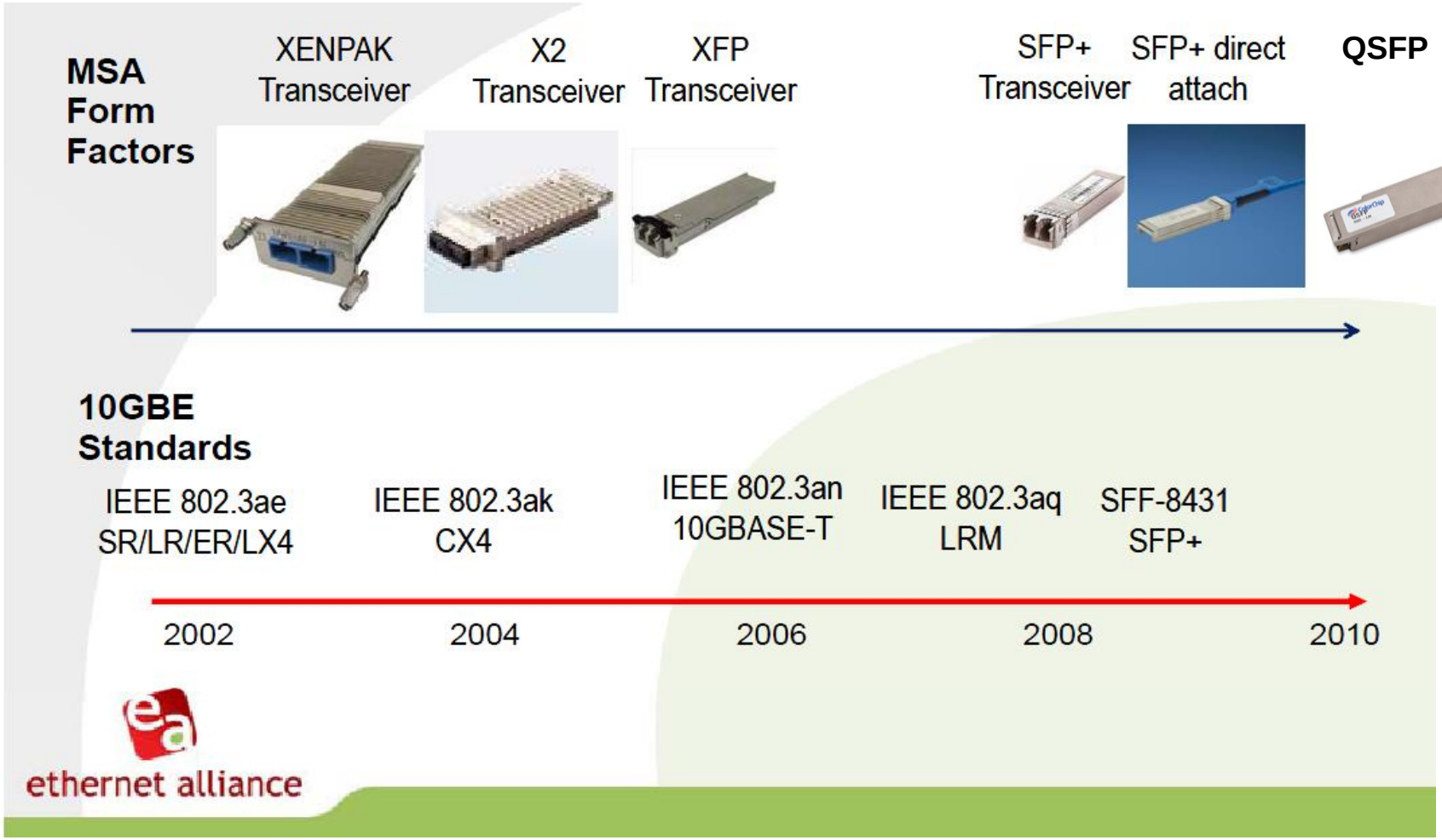
- BSX320, with Stress & TXEQ
- CR286A
- DPO77004SX Scope(recommended)

  or MSO73304DX (minimum)
- ISI Board (optional)
- SFP28 Host and Module Fixture



SFP+ QSFP+ Technology and Related Testing Challenges

10Gigabit Ethernet Interface Evolution



Source : Ethernet Alliance

SFF-8431 SFP+/SFF-8635 QSFP+ Technology overview

- SFP+ is a next-generation hot-pluggable, small footprint, serial-to-serial multi-rate optical transceiver for 8.5GbE to 11.1GbE Datacom and Storage Area Networks (SAN) applications.
- SFF-8635 QSFP+ 10 Gb/s 4X Pluggable Transceiver Solution (QSFP10)
- SFP+ technology moved the clock and data recovery units out of the module and onto the line card – Reducing size drastically
- As a result, the modules are smaller, consume less power, allow increased port density, and are less expensive compared to XFP.
- High density capable Up to 48 ports in a rack
- Low power per port - Host Port power < 1 W and Low Latency

TWDPc Measurement Definitions

- TWDPc
  - **T**ransmitter **W**aveform **D**ispersion **P**enalty for **C**opper
  - *Defined as a measure of the deterministic dispersion penalty due to a particular transmitter with reference channel and a well-characterized receiver.*
  - The fiber optics concept has been extended to quantify channel performance of high speed copper links “10GSFP+Cu”
  - Critical for performance
  - Requires a special algorithm
  - ClariPhy has IP rights for this algorithm
- Test Specification Requirements for TWDPc
  - 7 measurement samples per unit interval
  - Causes worst-case 0.24 dB TWDPc over 30 measurements

SFP-TX Host Transmitter Measurements

- 15 Defined Measurements for Host Tx Compliance

SL No.	Measuremnts	Signal Type Recommended	Limit			
			Min	Target	Max	Units
Host Transmitter output electrical Specifications:						
1	Single Ended Output Voltage Range	PRBS31	-0.3		4	V
2	Output AC Common Mode voltage (RMS)	PRBS31			15	mV(RMS)
Host Transmitter Jitter and Eye Mask specifications						
3	Crosstalk source rise/fall time (20%-80%) (Tr, Tf)	8180		34		ps
4	Crosstalk source amplitude (p-p differential)	8180		1000		mV
5	Signal rise/fall time (20%-80%) (Tr, Tf)	8180	34			ps
6	Total Jitter (p-p) (Tj)	PRBS31			0.28	UI(p-p)
7	Data Dependent Jitter (p-p) (DDJ)	PRBS9			0.1	UI(p-p)
8	Data Dependent Pulse Width Shrinkage (p-p) (DDPWS)	PRBS9			0.055	UI(p-p)
9	Uncorrelated Jitter (RMS) (UJ)	PRBS9			0.023	UI(p-p)
10	Transmitter Qsq	8180	50			
11	Eye mask hit ratio(Mask hit ratio of 5×10-5)	PRBS31	X1=0.12UI, X2=0.33UI, Y1=95mV, Y2=350mV			
Host Transmitter output specifications for Cu (SFP+ host supporting direct						
12	Voltage Modulation Amplitude (p-p)	8180	300			mV
13	Transmitter Qsq Output AC Common Mode voltage	8180	63.1			
14	Output AC Common Mode Voltage	PRBS31			12	mV(RMS)
15	Host Output TWDPc *	PRBS9			10.7	dBe

SFP-TX Module Transmitter Measurements

- 10 Defined Measurements for Tx Module Compliance

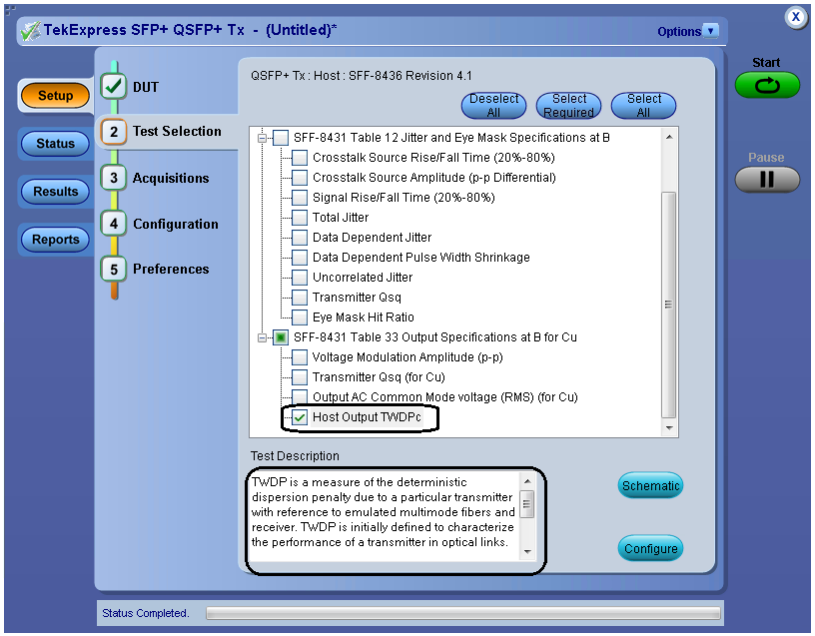
SL No.	Measuremnts	Signal Type Recommended	Limit			
			Min	Target	Max	Units
Module Transmitter Input electrical Specifications:						
1	AC common mode voltage tolerance	PRBS31	15			mV
2	Single Ended Input Voltage Tolerance	PRBS31	-0.3		4	V
Module Transmitter Jitter and Eye Mask specifications						
3	Crosstalk source rise/fall time (20%-80%) (Tr, Tf)	8180		34		ps
4	Crosstalk source amplitude (p-p differential)	8180		1000		mV
5	Output AC Common Mode Voltage	PRBS31			15	mV(RMS)
6	Total Jitter (p-p) (Tj)	PRBS31			0.28	UI(p-p)
7	Data Dependent Jitter (p-p) (DDJ)	PRBS9		0.1		UI(p-p)
8	Data Dependent Pulse Width Shrinkage (p-p) (DDPWS)	PRBS9		0.055		UI(p-p)
9	Uncorrelated Jitter (RMS) (UJ)	PRBS9		0.023		UI(RMS)
10	Eye mask hit ratio(Mask hit ratio of 5×10-5)	PRBS31	X1=0.12UI, X2=0.33UI, Y1=95mV, Y2=350mV			

Tektronix SFP-TX – Automation Part

- Operates on Tektronix DPO/DSA70000C/DX Series Oscilloscopes
- Automate setup & quickly generate reports
- Meets Compliance needs of SFF-8431/SFF-8635

- User defined mode supports PRBS7, PRBS11, PRBS15,PRBS20 & PRBS23 in addition to patterns supported in Compliance mode including PRBS9, PRBS31 and 8180.

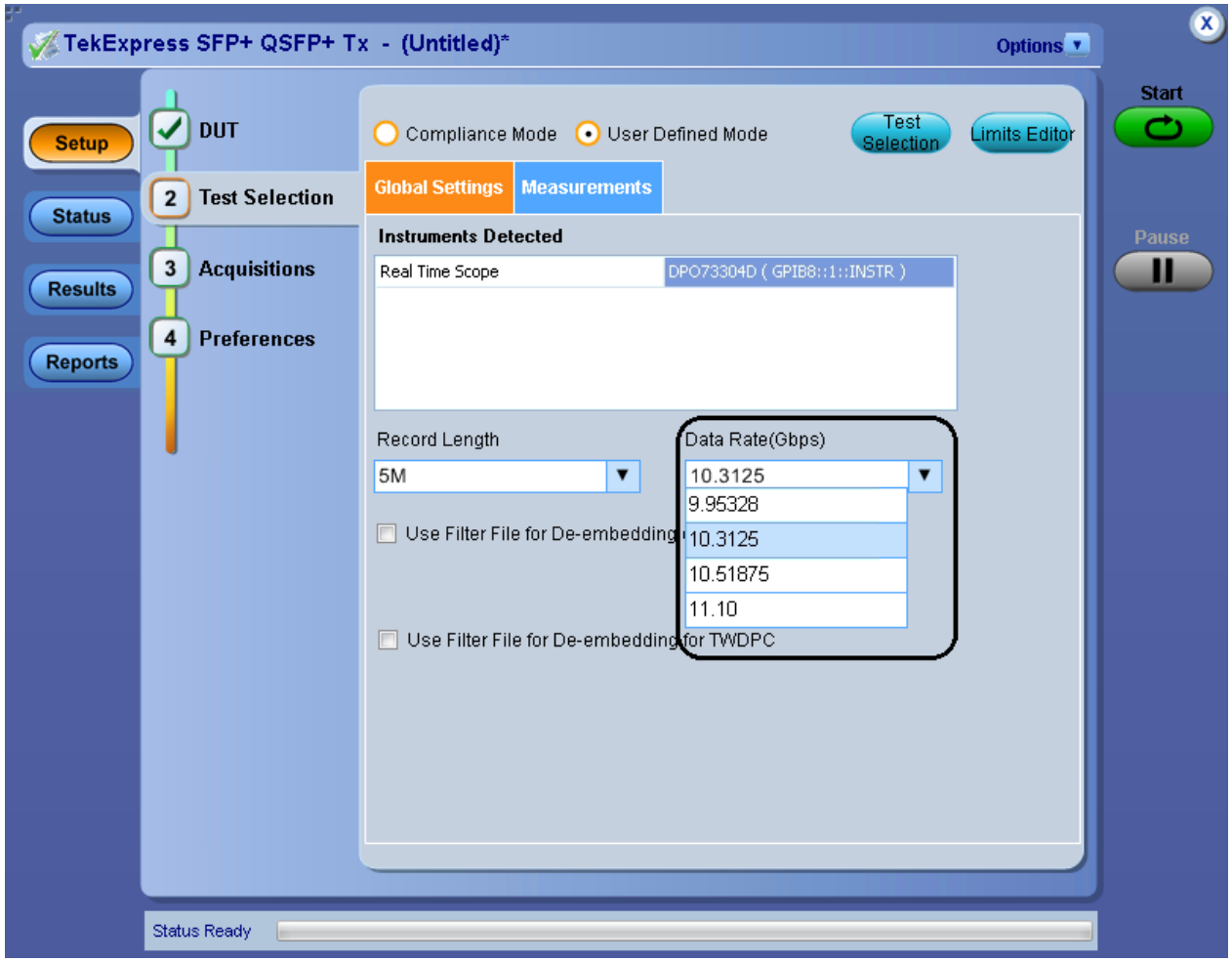
Tektronix SFP-WDP Option – TWDPc Measurement



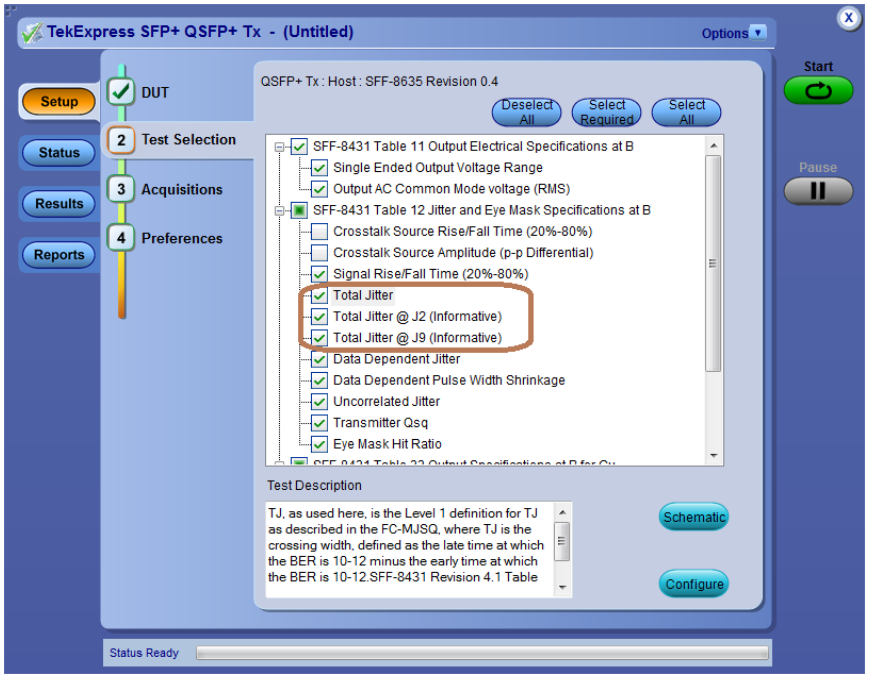
- Operates on Tektronix DPO/DSA70000C/DX Series Oscilloscopes
- Perform Transmitter Waveform Dispersion Penalty measurement with simple setup and test execution
- Ideal for high sample rate acquisition
  - 100GS/sec setting available on DPO/DSA70000C/D

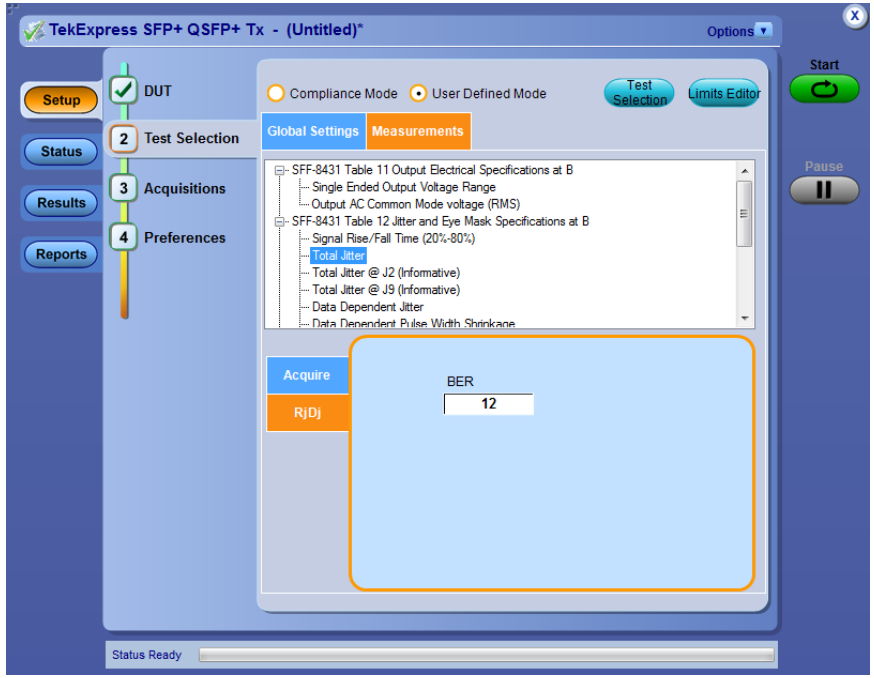
Tektronix SFP-TX Option – Multiple Data Rate Support

- Tektronix application supports multiple data rates including 9.95328Gbps, 10.3125 Gbps,10.51875 Gbps and 11.10 Gbps.



Tektronix SFP-TX Option – J2 & J9 Support





- SFP-TX allows users to enter BER value of in the range of BER e^–2 to –18,providing them the flexibility to calculate Total Jitter at various BER values.
- J2 & J9 measurements are part of other 10G standards like 40GBASE-CR4 and XLPPI.

Reporting and Documentation

Summary-reporting capability in .mht (HTML) format with pass/fail

Tektronix
Enabling Innovation

TekExpress QSFP+

Host Test Report

Setup Information	
DUT ID : DUT001	**TekExpress Version SFP+/QSFP+ :** 3.0.0.79
Spec Version : SFF-8635 Revision 0.4	**Scope Model :** MSO71604C
Date/Time : 2013-06-12 18:07:47.083000	**FW Version :** 6.7.4 Build 3
Compliance Mode : True	**DPOJet Version :** "6.0.1 Build 8"
Overall Execution Time : 0:01:40	**Scope Serial Number :** B130223
Overall Test Result : Pass	**Calibration Status :** PASS
DUT Comment : General Comment - QSFP + Transmitter Host DUT	

Test Name:Summary Table	Overall Result
Signal Rise/Fall Time (20%-80%)	Pass
Uncorrelated Jitter	Pass

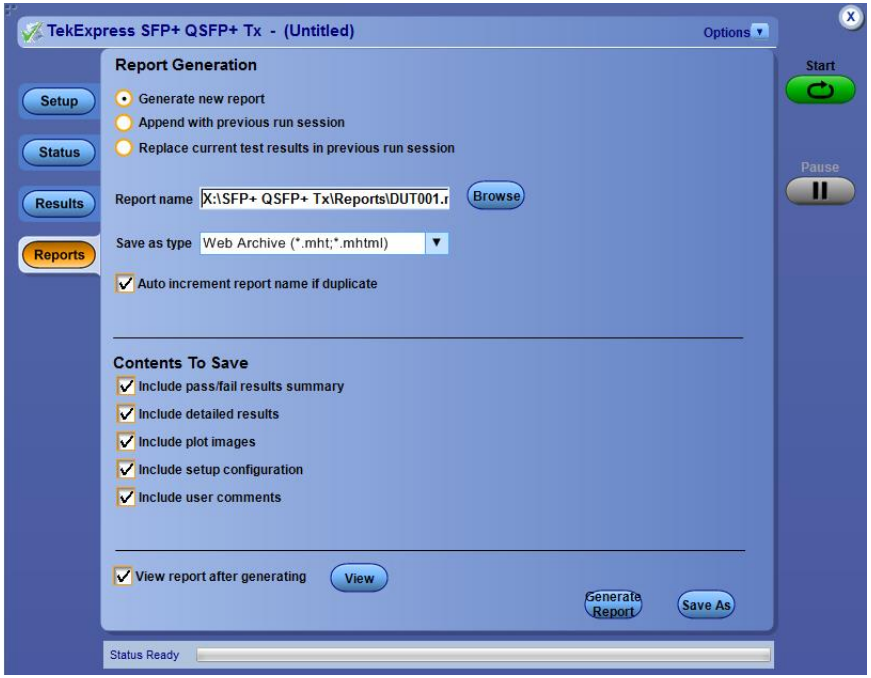
Signal Rise/Fall Time (20%-80%)

Lane Name	Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
Lane0	Signal Rise/Fall Time (20%-80%) RiseTime	52.7845	ps	Pass	18.7845	34.0	N.A	Signal Type :8180
Lane0	Signal Rise/Fall Time (20%-80%) FallTime	47.1486	ps	Pass	13.1486	34.0	N.A	

Back To Summary Table

Uncorrelated Jitter

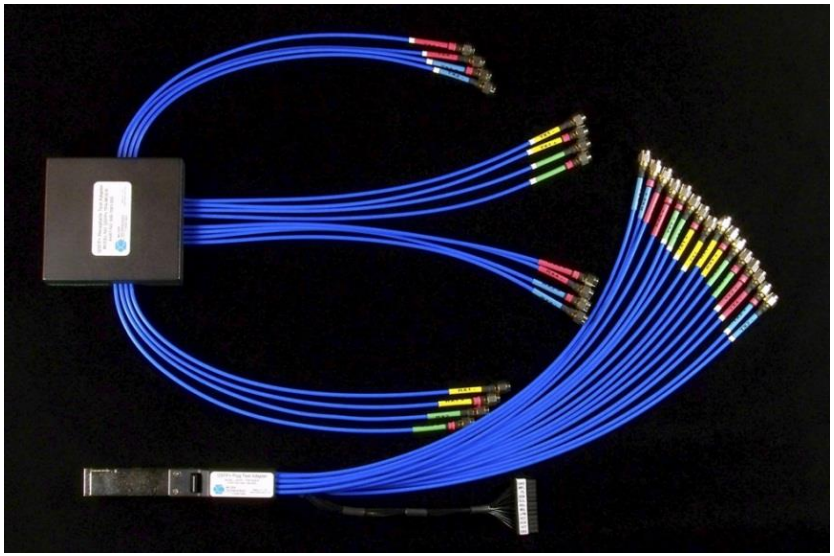
Lane Name	Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
Lane0	Uncorrelated Jitter	0.004	UI	Pass	0.019	N.A	0.023	Signal Type :PRBS9

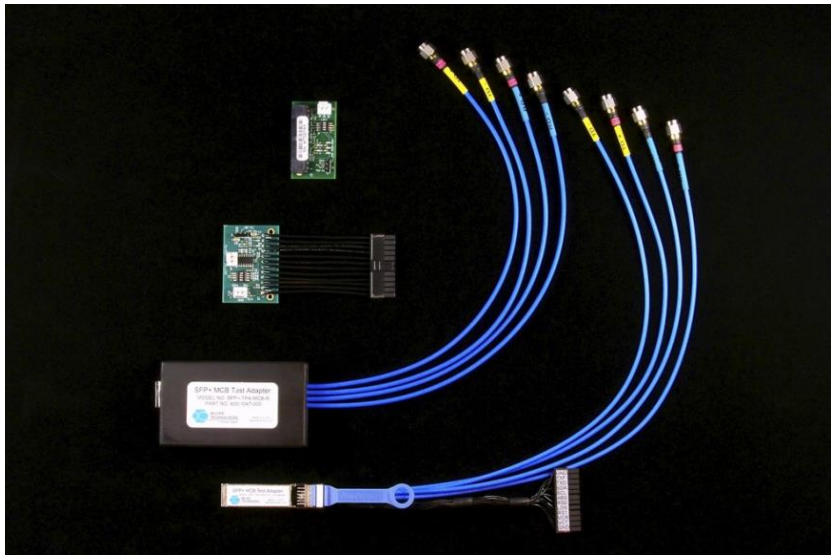


- Detailed report includes
  - Measurement results:
    - Test configuration details, waveform plots, and margin analysis
  - Test Setup details:
    - Calibration status, oscilloscope model, probe model, software version, date, execution time etc.

- Flexible report configuration provides options like auto increment, appending etc.

QSFP+ SFP+ Fixture





SFP-TX, WDP Recommended Test Equipment

- SFF-8431/SFF-8635 SFP+ provides 10.3125 Gb/second connections with the minimum rise time requirement of 34 psec
- DPO/DSA/MSO71604C/D 16GHz Oscilloscope (24.5 psec Rt)
- DPO/DSA/MSO72004C/D 20GHz Oscilloscope (18psec Rt)
  - >16GHz Oscilloscope will meet rise time requirements of SFF-8431/SFF-8635 SFP+ signal
  - Option SFP-WDP requires 100GS/sec Sample Rate

Oscilloscope	Software	Fixture
DPO/DSA/MSO 16-33 GHz scope*	SFP-TX, SFP-WDP & DJA	HCB and MCB

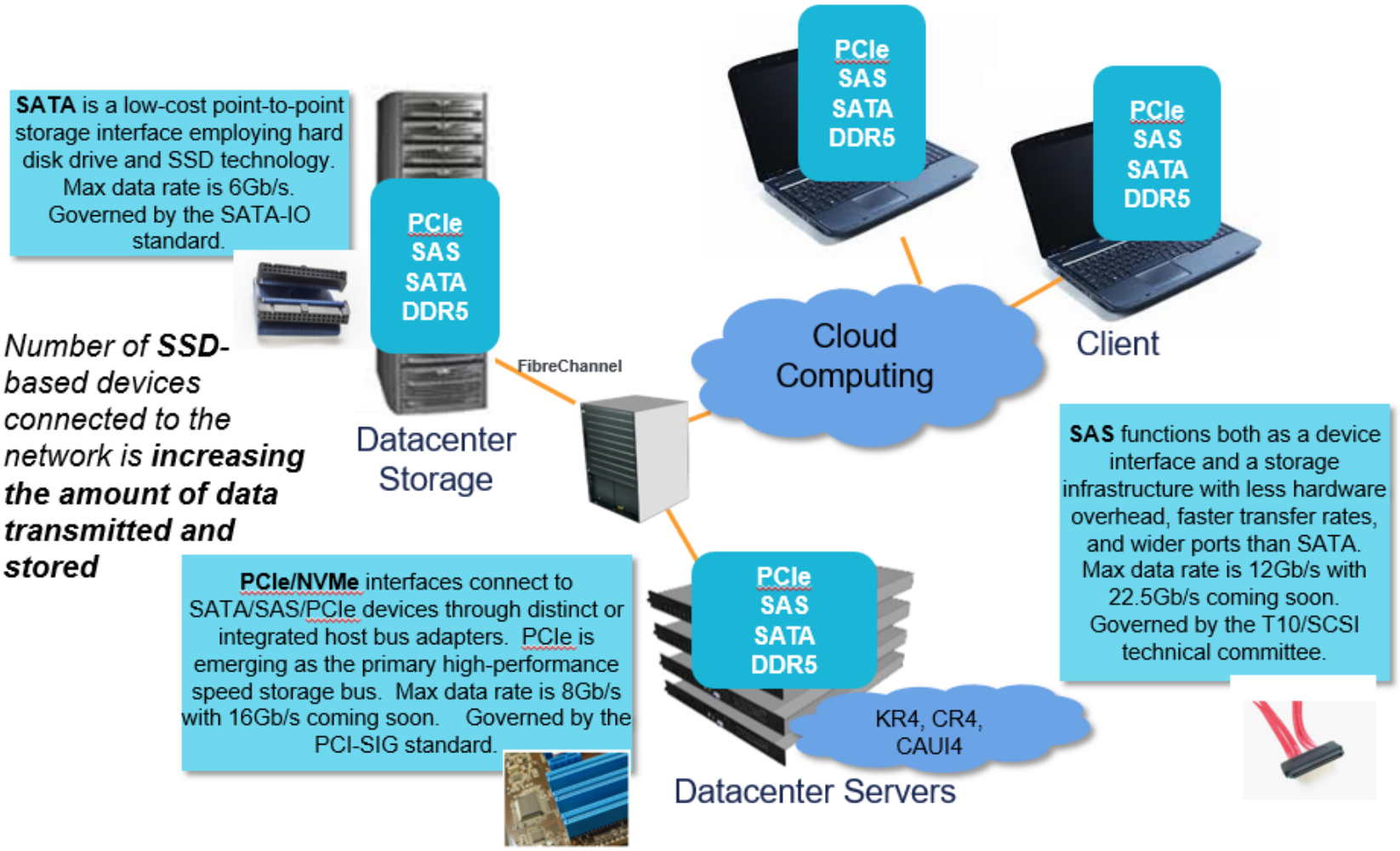
*SFP-WDP requires "C" & "D" series scopes with BW greater than equal to 16GHz

Tektronix Ethernet Solution – Information

- Tektronix has strong portfolio of products and solution in Ethernet Space – RT Scope, Sampling scope, BERTScope and Optametra products
- TDSET3 – Available since 2003 with, ET3 is widely used solution across industry
- 10GBASE-T/NBASE-T Compliance solution is the only “One Box” solution available in the market
- SFP-TX & SFP-WDP provides comprehensive solution for SFP+ & QSFP+, Tektronix is first to market
- 10GBASE-KR - 802.3ap™-2007 – We now have a Compliance, Debug and Decode Solution
- FC-16G – Fiber Channel 16G Compliance and Debug solution available on RT Scopes
- 10GBASE-KR and SFP+ RX MOI are available on BERT Scope

SAS

Server/Storage Technology Overview



Today's Storage Market?

- 3
  - Manufacturers of Hard Disk Drive
  - WD, Seagate, Toshiba
- 5
  - # of manufacturers of NAND flash chips for SSDs
  - Toshiba/WD, Intel/Micron, Samsung, SK Hynix, Powerchip
- 161
  - # of SSD Makers

Making a solid-state disk drive is much easier than manufacturing a magnetic hard disk drive. Mainly, *you just have to buy flash chips and assemble them with a controller from your own design or acquired from an outside company .*

It's not a lot of investment and that's why many small Asian firms entered into this activity. The key differentiators are not the chips, available from several sources and evolving in parallel, always smaller an smaller. *The main component is the controller, each one using different algorithms to manage the complex way of reading and above all writing flash chips*.

Source: Storagenewsletter.com

Key Information about SAS Standard

- SAS—Serial-attached SCSI. SAS-1 = 3Gb/s, SAS-2 = 6Gb/s, SAS-3 = 12Gb/s
- Key attributes/requirements of SAS-4
  - 22.5 Gb/s (Fbaud)
    - 2x data throughput from 12 Gb/s SAS3
    - **33GHz scope BW guideline**
    - **Reed Solomon FEC coding (30/26) required** to achieve 1E-15 BER corrected BER, based on 1E-6 uncorrected BER
  - Table 55 (was Table 45 for SAS3) uses pre-emphasis coefficients to characterize the **signal integrity of the transmitted signal**
  - Maintains compatibility w/ SAS3 installed base
    - Multiplexed interfaces provide multiple data paths, enhanced **redundancy & availability**
    - **Same JTF requirements as 12 Gb/s SAS (f_{JTF} = 2.6MHz with SSC support)**
    - Transmitter training comparable for 12 Gb/s and 22.5 Gb/s (SPL-4)
    - Maintains support for OOB signals if SATA is supported
- SAS4
  - New/updated connector definitions including SFF-8639 (U.2)
  - Longer scrambler for improved training capabilities (same as PCIe)
  - **Test channels (-30dB end-to-end, not including package)**

Testing Challenges in SAS Tx

- Understanding and implementing measurement algorithms such as Table 45/55 and WDP/SASEYEOPENING is difficult
- Interoperability issues stemming from SSC/coupled power supply switching noise
- How to overcome -30dB channel loss required by SAS4?
- Optimizing equalization settings for Tx compliance
- Automation is required due to test duration and complexity

SAS Table 55 (was Table 45 for SAS3)

SAS Table 55/45 specifies Tx Characterization, i.e. how the output changes with increase, decrease, or hold using pre-emphasis coefficients

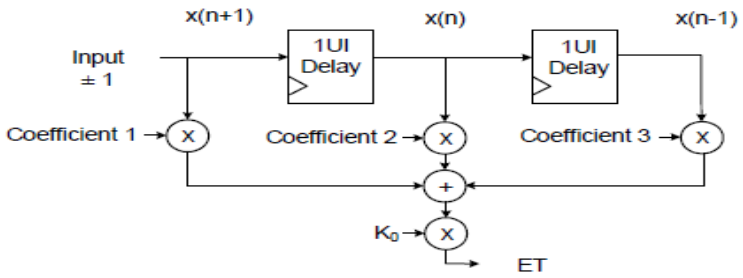
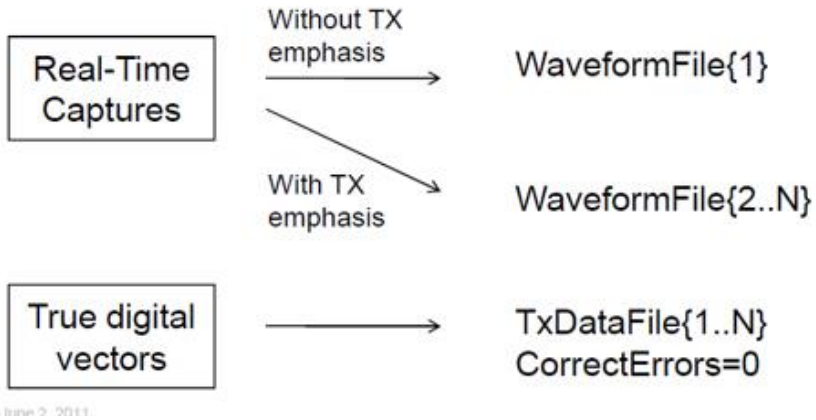


Figure 137 — 12 Gbit/s reference transmitter

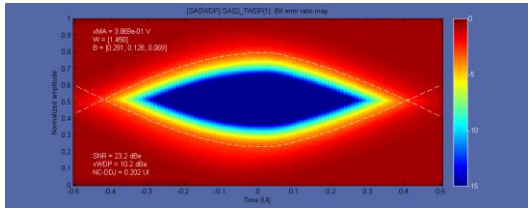
Procedure:

1. Select Interconnect point closest to TX
2. Set TX to transmit IDLE sequence with no de-emphasis
3. Capture data sequence
4. Step Tx Emphasis
5. Provide data to SAS Eye Opening



SAS WDP/SASEYEOPENING Measurement

- WDP stands for Waveform Dispersion Penalty
- SASWDP is a MATLAB program specified by the T10/SAS standard and can be employed by test instrument tools for 1.5 - 6 Gb/s operation
- Key SASWDP attributes:
  - **Data must be periodic**
  - Data and pattern must be properly aligned
  - Has built-in clock recovery. Can be challenging with closed eye.



- SASWDP replaced by SASEYEOpening for SAS3 12G speed
- Details on SASEyeOpening measurement:
  - **Not sensitive to pattern. Can extract information from close eye also.**
  - Computes the eye opening due to DDJ, after a perfect 3-tap DFE.
  - Outputs information about each of the DFE's 3-taps compensation

SAS Rx Calibration and Test Procedure for SAS3/4

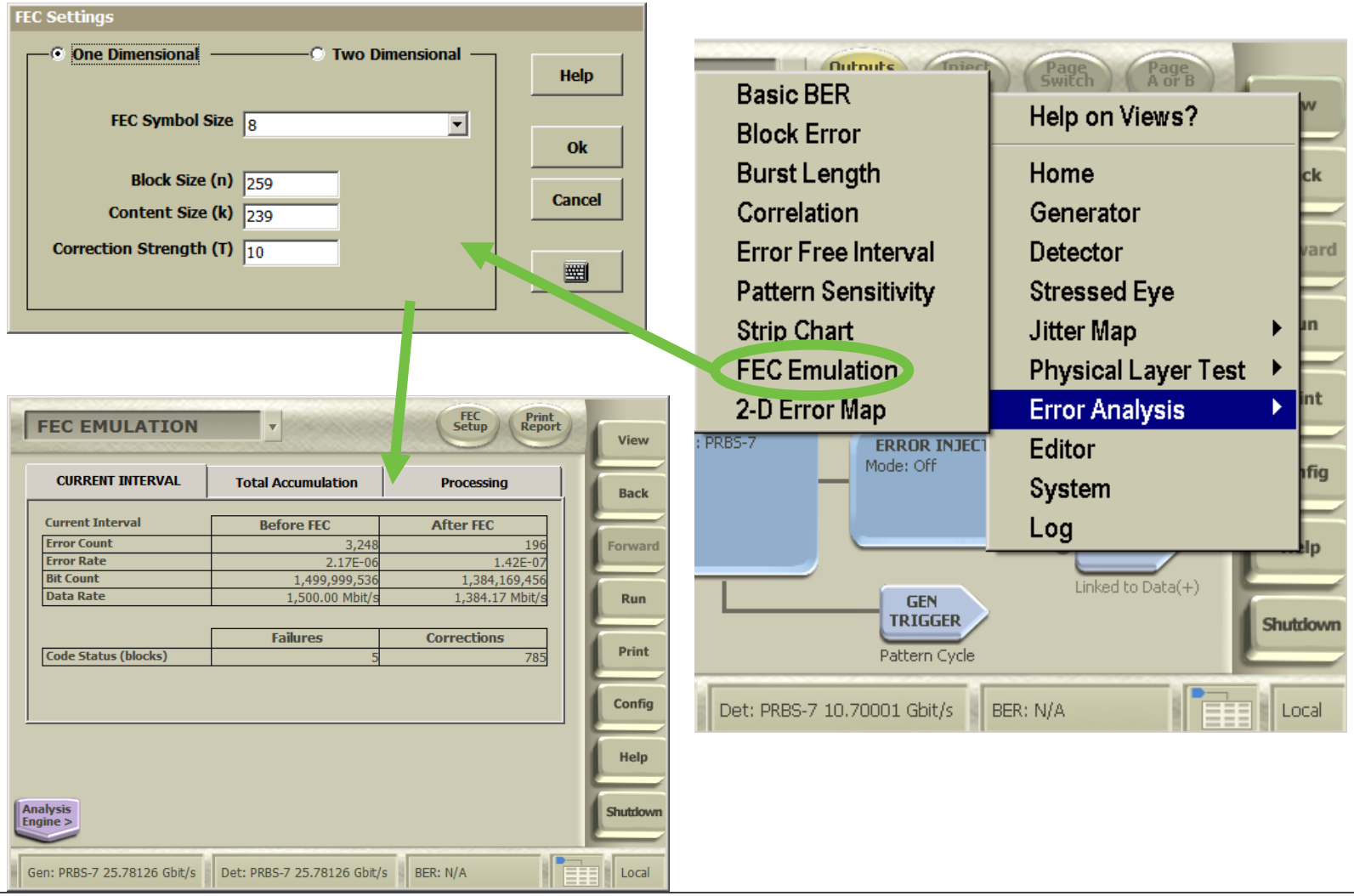
SAS3

1. Calibrate ISI for Vpp, eye opening, cal coefficients per standard
2. Calibrate crosstalk source for noise peak-to-peak
3. Apply ISI and crosstalk to DUT
4. Run live traffic
5. Load training patterns and **train Rx/Tx**
6. Configure RJ
7. Configure SJ
8. Configure BERT to transmit **CJTPAT**
9. Ensure that Rx DUT has BER less than 1E-12 with level of 95%

SAS4

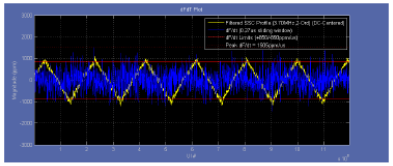
1. Run live traffic
2. Ensure test equipment complies with signal specs such as Vpp, impedance, rise/fall, UUGJ, UBHPJ, DCD, and TJ
3. Calibrate channel to be compliant to worst-case standards (-30dB at 11.25GHz)
4. Load training patterns and **train Rx/Tx**
5. Configure SJ
6. Configure BERT to transmit **PRBS31**
7. Ensure that Rx DUT has BER less than 1E-6 with level of 95%
8. If desired, confirm BER of 1E-15 using **FEC**

SAS4 Error Location Analysis: FEC Emulation

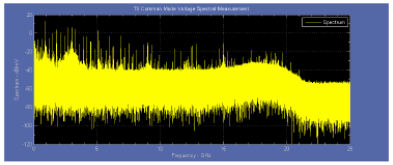


Tek Guidance for SAS4 Solutions

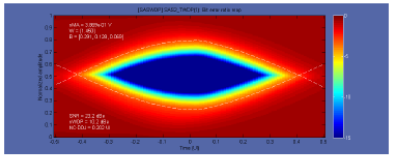
- Receiver Test
  - BSX BERTScope (integrated TXEQ) w/ support for 22.5Gbs SAS Rx & LinkEQ
- Transmitter Test
  - SAS4 min BW requirements at 33GHz dictate use of either DPO73304DX or DPS75004SX solution
  - SAS4 solution based on DPOJET



Comprehensive SSC Analysis Tools



Transmitter Spectral Profile for Common Mode Analysis



SAS-2 Waveform Dispersion Penalty (WDP measurement)

SATA

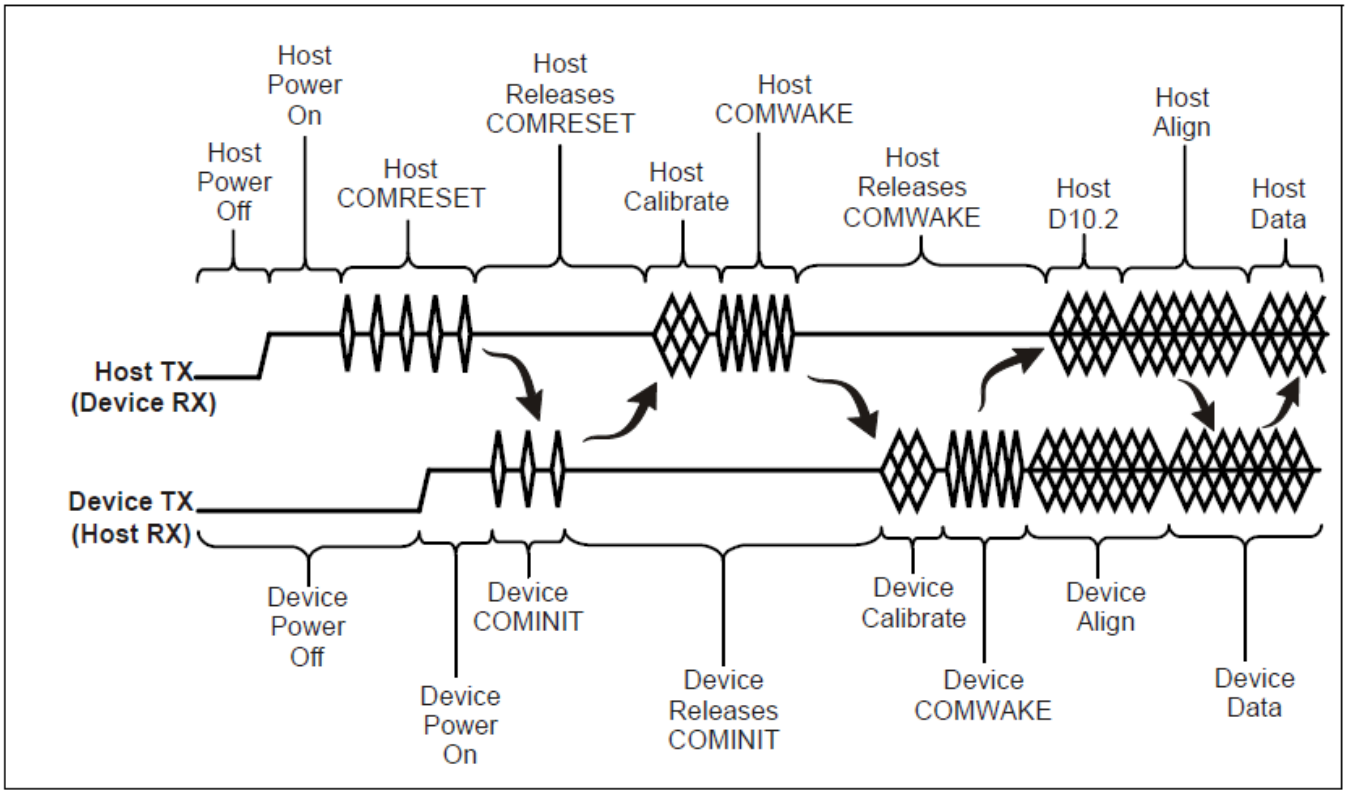
SATA 3.2 Specification

6GB/S DATA SPEEDS

- **SATA Express:**
  - Includes both SATA and PCIe signaling
  - Hosts supports both SATA or PCIe storage device.
  - With PCIe transfer rates of up to 2 GB/s (2 lanes of PCIe 3.0), compared with today's SATA technology at 0.6 GB/ (due to encoding)
- **M.2:**
  - SATA revision 3.2 also incorporates the M.2 form factor, enabling small form-factor M.2 SATA SSDs suitable for thin devices such as tablets and notebooks.
- Additional features of the SATA-IO Revision 3.2 Specification include:
  - microSSD–standard for embedded solid state drives (SSDs) that enables developers to produce single-chip SATA implementations for embedded storage applications.
  - Universal Storage Module (USM)– enables removable and expandable storage for consumer electronic devices. SATA revision 3.2 introduces USM Slim, which reduces module thickness, allowing smaller removable storage solutions.
  - DevSleep– the lowest level of power management yet, where the drive is almost completely shut down, meeting the requirements of new always on, always connected mobile devices such as Ultrabooks™.

Initiating BIST-L/BIST-T Mode

BELOW IS HOST/DEVICE HANDSHAKE/TRAINING SEQUENCE

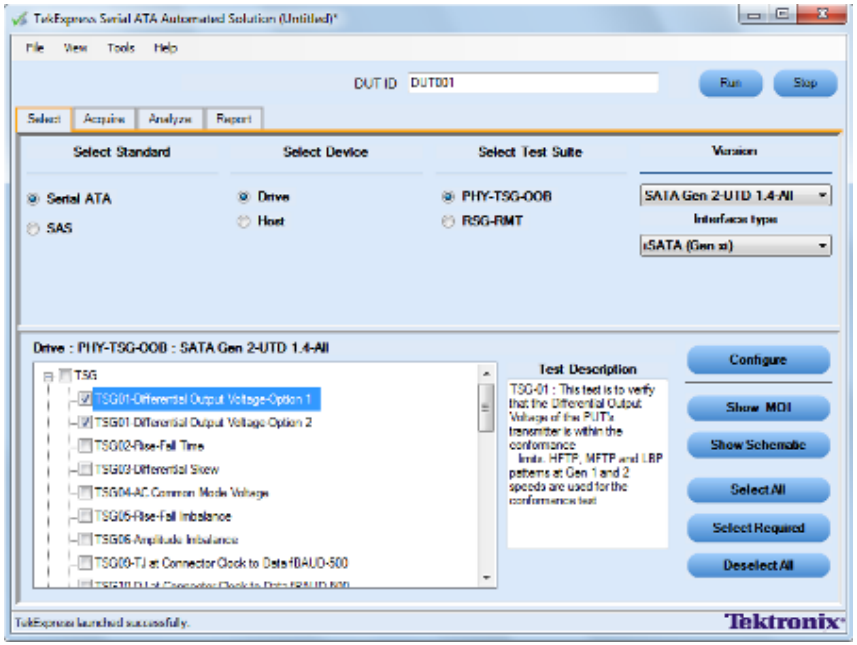


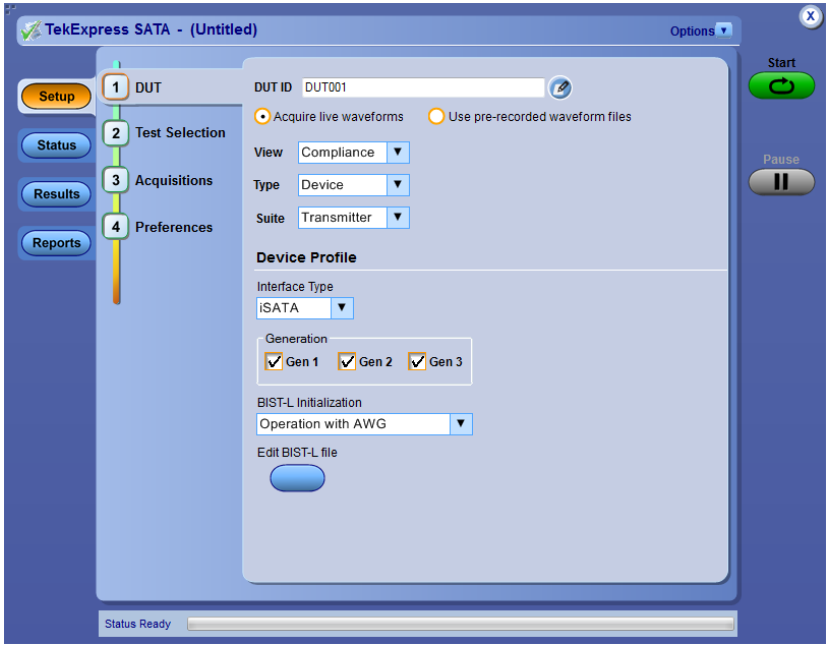
SATA PHY Test Summary

- SATA 3.2 spec and UTD 1.5.0
- Updated measurements
  - Focus on mobile/direct attach form factors (Uhost)
- BIST-L critical to SATA testing
  - Host controllers more difficult
  - BIST-L library continually updated per latest chipsets
- Compliance Interconnect Channel (CIC) central to Gen3 testing
  - Models worst-case channel for far-end Tx measurements and ISI for Rx
  - No CIC for Gen3u Host
- TekExpress Automated software simplifies setup and testing
  - SATA-TSG for PHY/TSG/OOB

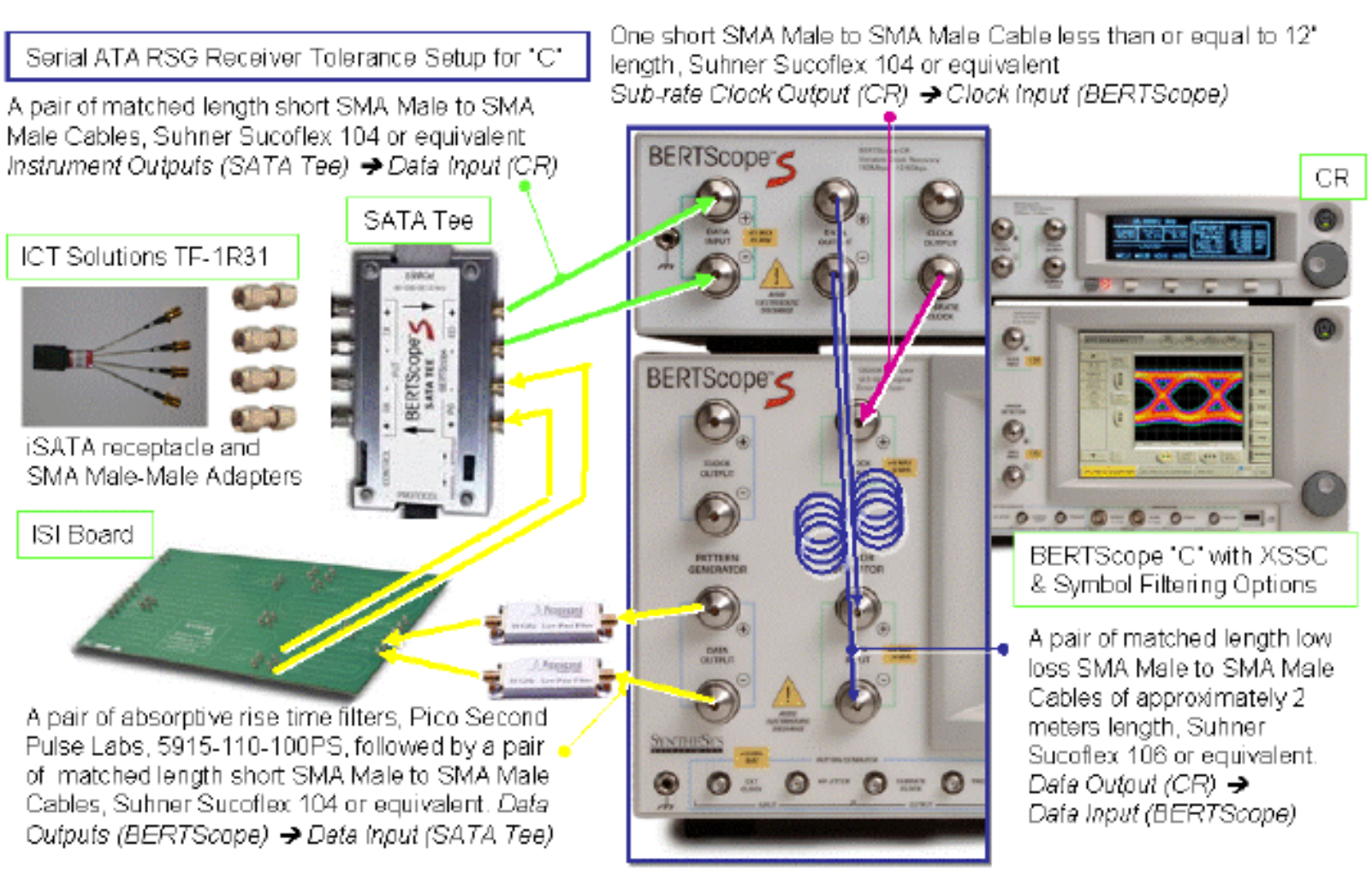
SATA Transmitter Test Solution

- TekExpress SATA-TSG software
- Recommend BW 16GHZ for SATA3

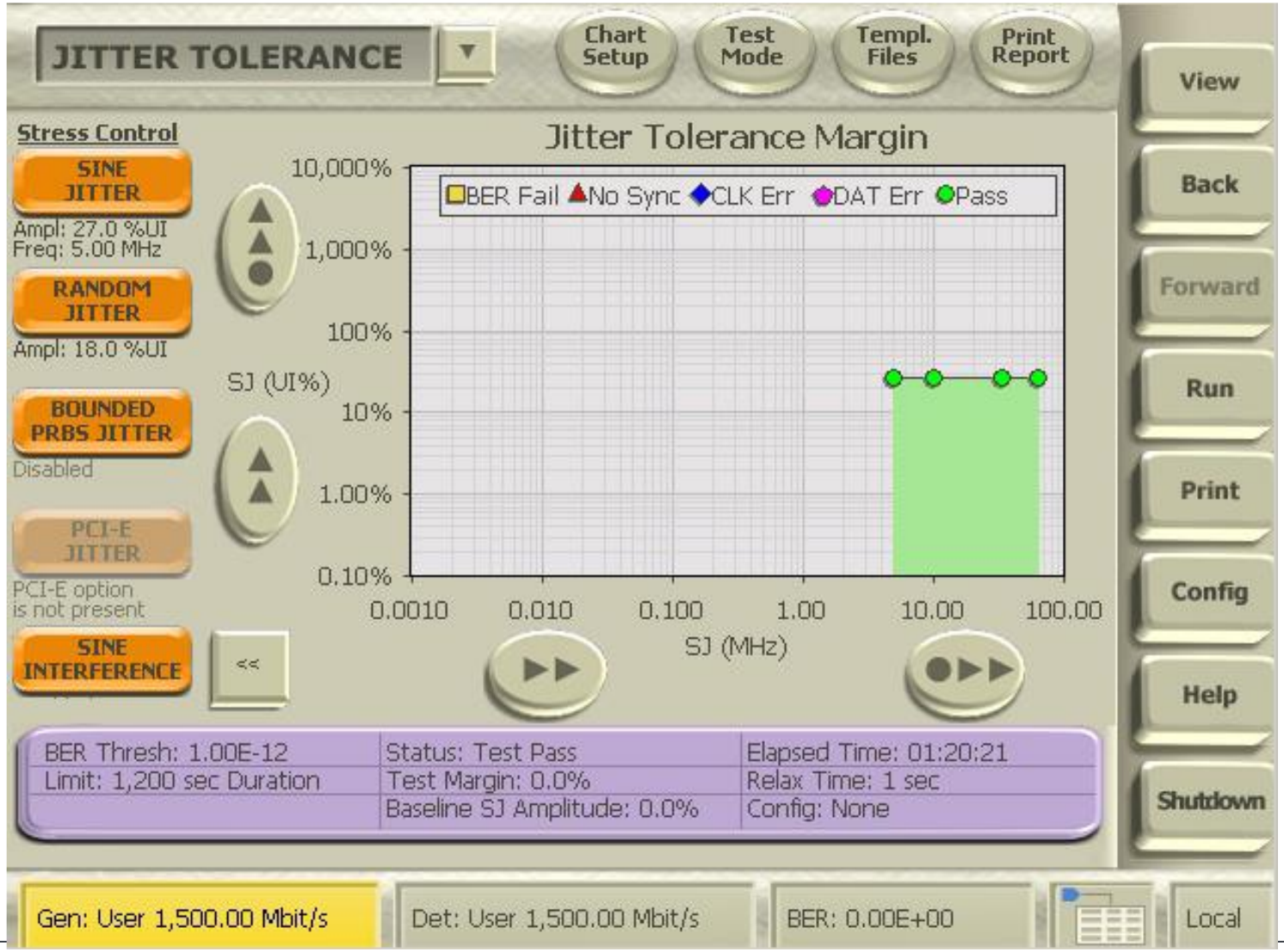




SATA Receiver Testing - BertScope



Jitter Tolerance



USB

What Does Type-C Mean to You?

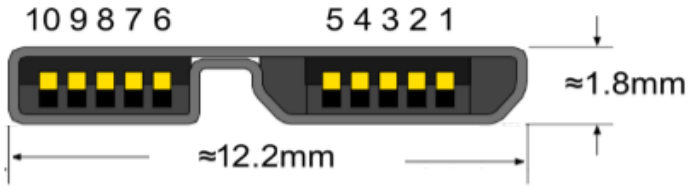
Power Delivery	More **Power** with USB Power Delivery (100 W)
Type-C	More **Flexibility** with new reversible USB Type-C connector
Alternate Mode	More **Protocols** (Display Port, Thunderbolt, HDMI, etc.)
USB IF	More **Speed** with USB 3.1 (10 Gbit/s)

Source: USB-IF

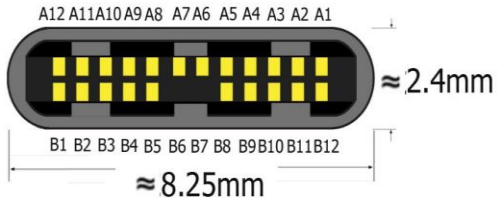
Type-C Comparison *(USB-C)*

- Rounded, reversible, flip-able
- ~25% less width vs.µB
- Signaling
  - Two SS differential pairs
  - Vbus power
  - Configuration Channel (CC)
  - USB 2.0 differential pair
  - Sideband Use (SBU)
  - Plug power (Vconn)

Micro B Plug



Type-C Plug



A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2			VCONN	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

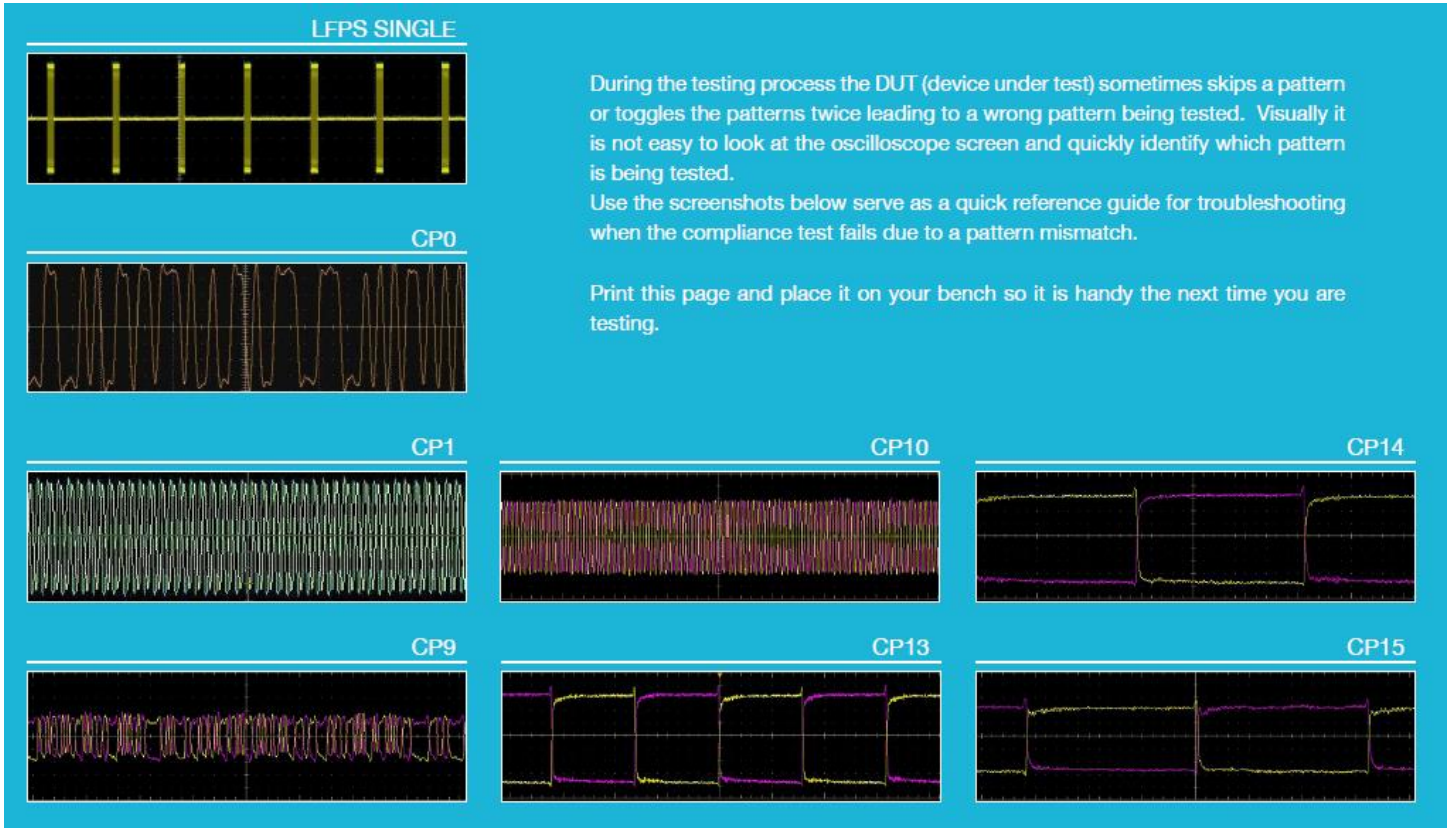
USB 3.1 Comparison of Gen1 vs. Gen2

USB 3.1	Gen1	Gen2
Data Rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b
Target Channel	3m/2m + Host/Device channels (-17dB, 2.5 GHz)	1m + board ref channels (-23dB, 5 GHz)
LTSSM	LFPS, TSEQ, TS1, TS2	LFPSPlus, SCD, TSEQ, TS1, TS2,
Reference Tx EQ	De-emphasis	3-tap (Preshoot/De-emphasis)
Reference Rx EQ	CTLE	CTLE + 1-tap DFE
JTF Bandwidth	4.9 MHz	7.5 MHz
Eye Height (TP1)	100 mV	70 mV
TJ@BER	132 ps (0.66 UI)	67.1 ps (0.671 UI)
Backwards Compatibility	Y	Y
Connector	Std. A, Micro, Type-C	Std. A, Micro, Type-C

USB 3.1 Transmitter Measurement Overview

USB Type-C Gen1			
Measurements	Sigtest v.3.2.11.2	DPOJET	Compliance Pattern
Jitter budget(RJ,DJ and TJ)	Yes	Yes	CP0, CP1
Eye diagram	Yes	Yes	CP0
Width@BER – 10E-12	Yes	Yes	CP0
SSC deviation	No	Yes	CP1
SSC modulation rate	No	Yes	CP1
Differential pk-pk voltage	No	Yes	CP0
LFPS	Yes	Yes	NA
USB Type-C Gen2			
Measurements	Sigtest v.4.0.23.1	DPOJET	Compliance Pattern
Jitter budget(RJ,DJ and TJ)	Yes	Yes	CP9, CP10
Eye diagram	Yes	Yes	CP9
Width@BER – 10 E-6	Yes	Yes	CP9
Height@BER – 10E-6	No	Yes	CP9
SSC deviation	Yes	Yes	CP10
SSC modulation rate	Yes	Yes	CP10
Differential pk-pk voltage	No	Yes	CP9
Tx Equalization (Preshoot & De-emphasis)	Yes	Yes	CP13, 14,15
LFPS	Yes	Yes	NA

Compliance Test Pattern

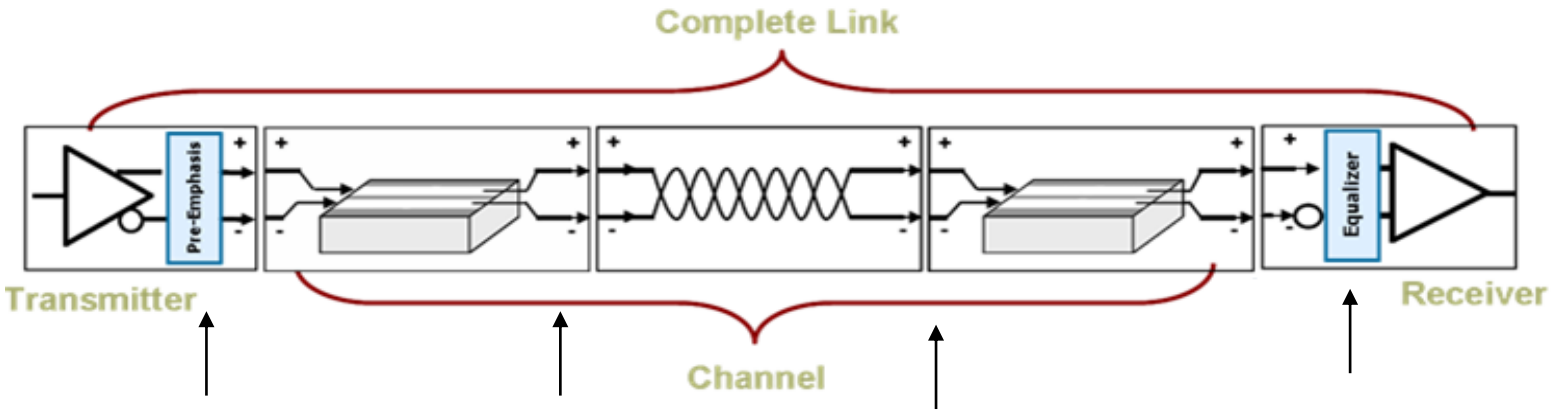


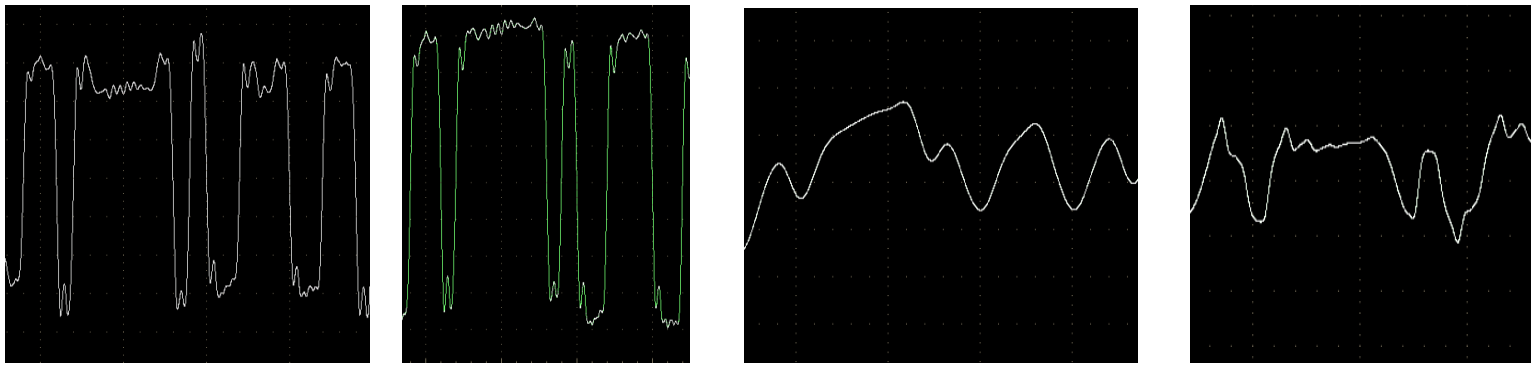
Typical Steps Involved to Run Tx Tests

1. Connect DUT to scope via test fixture
2. Transmit CP10 (clock) & measure $2x10^6$ consecutive UI
   - This step used to measure RJ
3. Repeat with CP9 (scrambled data pattern
   - Will combine RJ (step 2) with DJ to extrapolate TJ (step
4. Post-process the waveforms with the compliance channel, the reference CTLE, & jitter transfer function
   - Channels are S-Parameter-based and are embedded into captured waveform
5. Accumulate jitter to 10^{-6} BER

Spec	Min	Max	Units
Eye Height	70	1200	mV
Dj @ 10^{-6} BER		0.530	UI
Rj @ 10^{-6} BER		0.094	UI
Tj @ 10^{-6} BER		0.671	UI

End-to-End PHY Validation





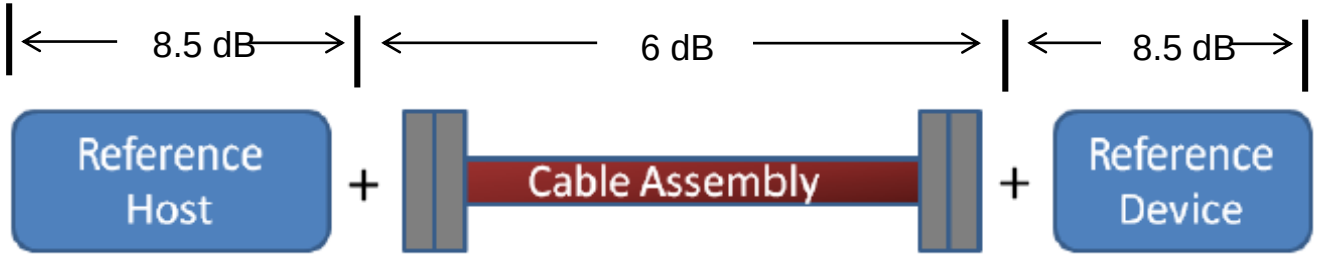
TP0 – Near End

Measurements are specified at TP1

TP1 – Far End

New Channel Budget – USB 3.1 Gen2 Type-C

- Target 23 dB @ 5 GHz loss budget (die-to-die)
- Equal channel allocation for host/device
- Tx EQ settings (normative)
  - 2.2 dB Preshoot and -3.1 dB De-emphasis
  - Requires additional compliance patterns (CP13, 14 &15) for Tx testing
- Host or device loss that exceeds 8.5 dB may require repeater
  - Need end-to-end training -> link aware repeaters



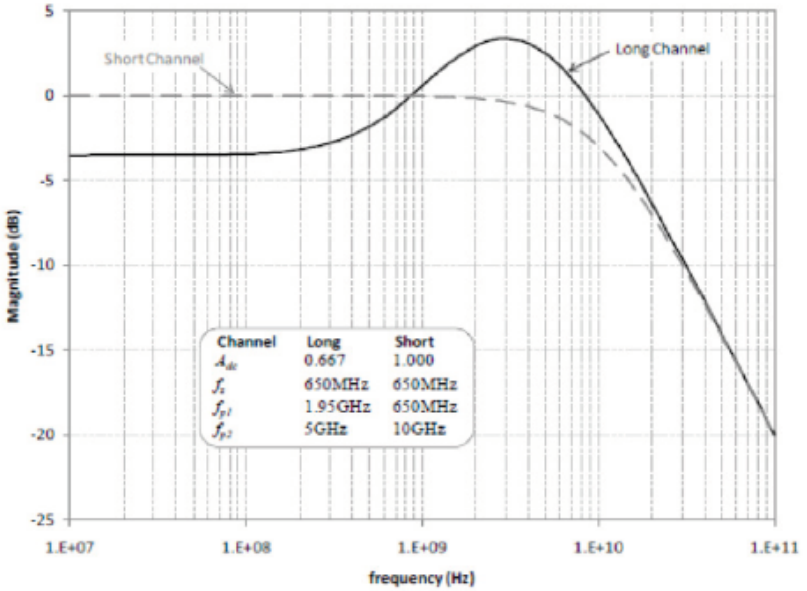
Reference Receiver Equalizer – Gen1

USB 3.1 allows the use of receiver equalization to meet system timing and voltage margins. For long cables and channels the eye at the Rx is closed, and there is no meaningful eye without first applying an equalization function. The Rx equalizer may be required to adapt to different channel losses using the Rx EQ training period. The exact Rx equalizer and training method is implementation specific.

The equation for the continuous time linear equalizer (CTLE) used to develop the specification is the compliance Rx EQ transfer function described below.

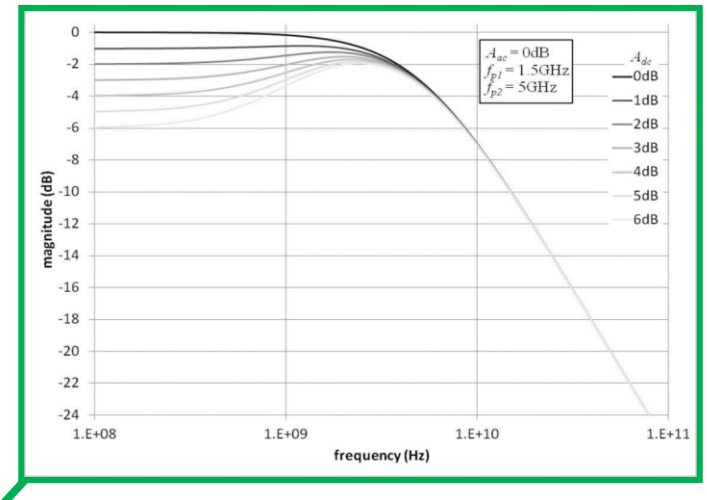
$$H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

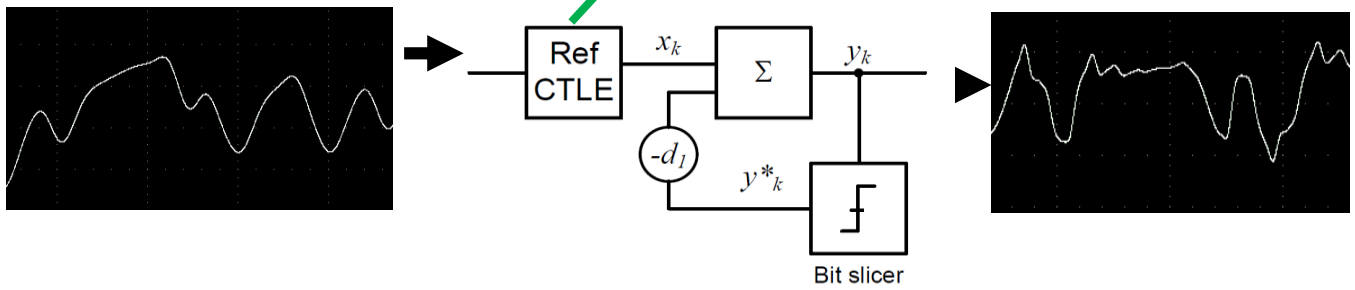
where A_{dc} is the DC gain
$\omega_z = 2\pi f_z$ is the zero frequency
$\omega_{p1} = 2\pi f_{p1}$ is the first pole frequency
$\omega_{p2} = 2\pi f_{p2}$ is the second pole frequency



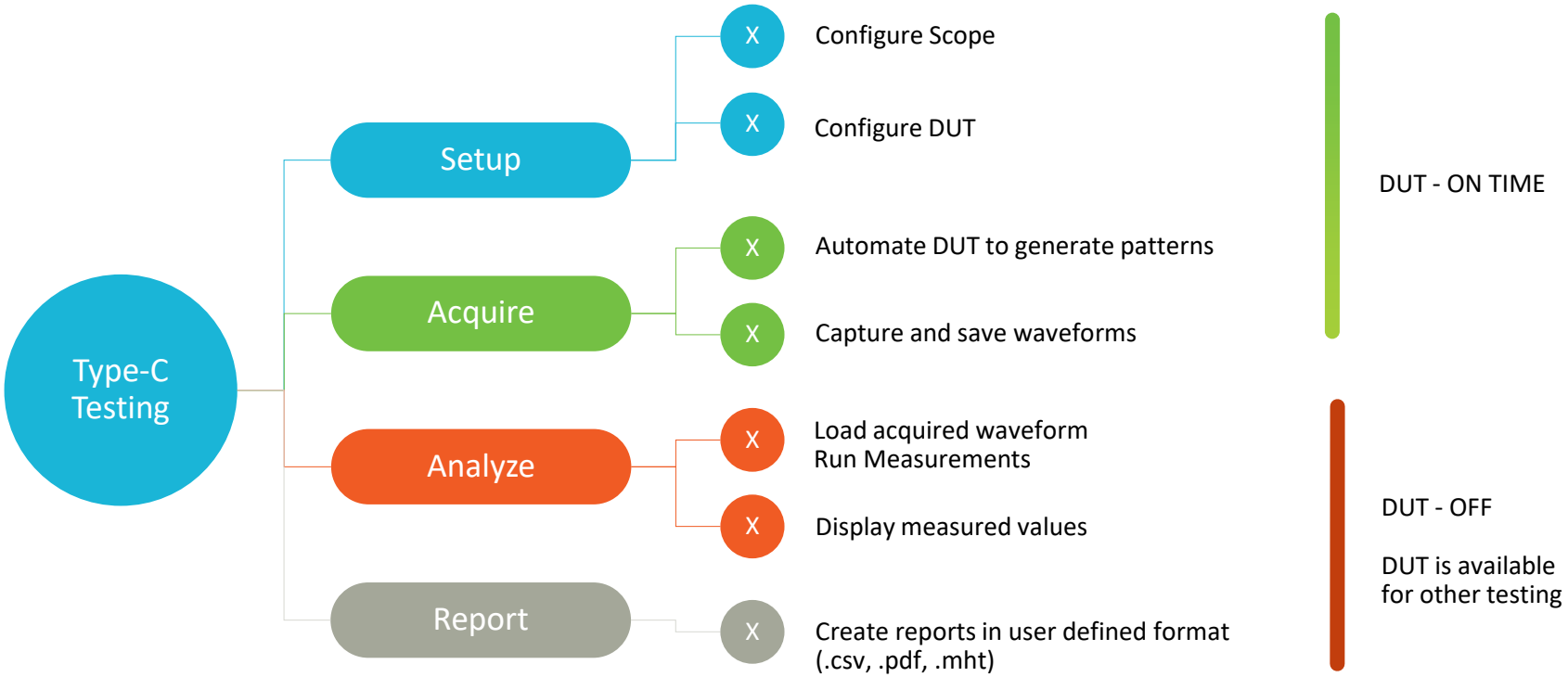
Reference Receiver Equalizer – Gen2

- Far End (TP1) Eye closed
- Need to open eye with EQ
- Adaptation only for Rx
  - No back channel Tx negotiation
- Iterate through multiple CTLE gain settings + 1-tap DFE



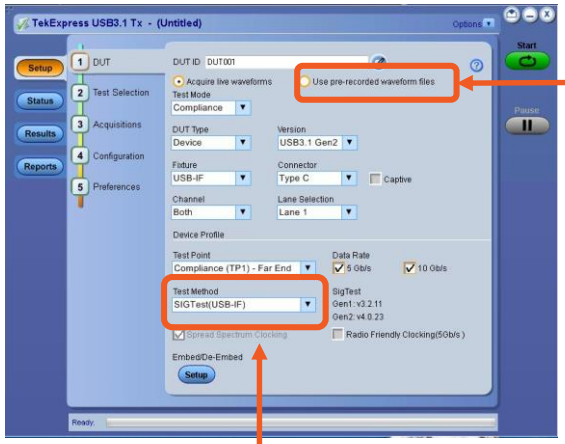


Tx Testing Workflow



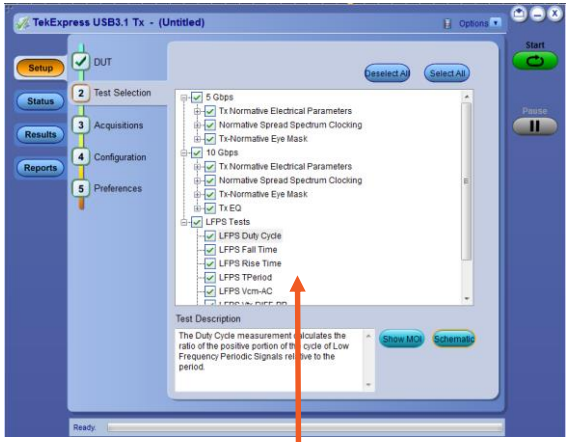
USB Automated Compliance Tools

USER DEFINED LIMITS, OFFLINE ANALYSIS, DPOJET & SIG-TEST SUPPORT



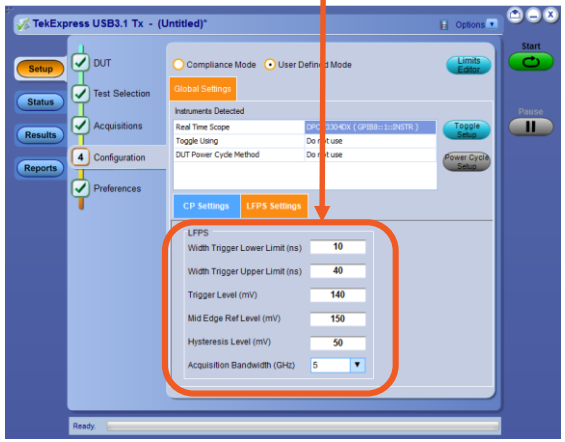
Offline Analysis

Measurements using both Sig-Test & DPOJET



Test selection panel showing Gen1, Gen2 and LFPS tests

User editable parameters



How do I Debug Compliance Failures?

3 EASY STEPS:

- Manually setup standard specific measurement and analyze
- Vary measurement parameters and monitor behavior
- Add different plots to get deep insight into DUT characteristics

SOLUTION:

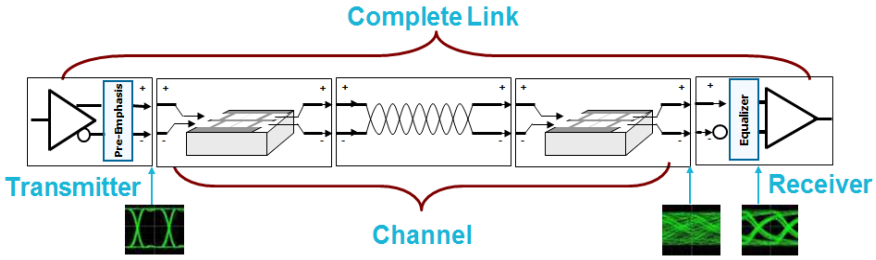
- Standard Specific Modules and measurement analysis on single acquisition
- Comprehensive Measurements for
  - Jitter Analysis, Noise & Margin Analysis
  - Eye Diagram with BER Contour
  - Multiple plots like Bath Tub Curve etc.
  - Amplitude, Timing and Frequency Analysis

Eye Height – Transmitter Eye Mask									
Measurement Details	Lane	Channel	Generation	Method	Measured Value	Test Result	Margin	Low Limit	High Limit
Eye Height – Transmitter Eye Mask	Lane1	Short	Gen1	DPOJET	358.769 mV	Pass	258.769 mV & 841.231 mV	100.0 mV	1.2 V
Eye Height – Transmitter Eye Mask	Lane1	Short	Gen1	SigTest	349.847 mV	Pass	249.847 mV & 850.153 mV	100.0 mV	1.2 V
Eye Height – Transmitter Eye Mask	Lane1	Long	Gen1	DPOJET	68.565 mV	Fail	–31.435 mV & 1.131 V	100.0 mV	1.2 V
Eye Height – Transmitter Eye Mask	Lane1	Long	Gen1	SigTest	66.401 mV	Fail	–33.599 mV & 1.134 V	100.0 mV	1.2 V
COMMENTS	USB 3.1 Specification, Rev 1.0, Table 6–19								

How do I Analyze Channel Loss?

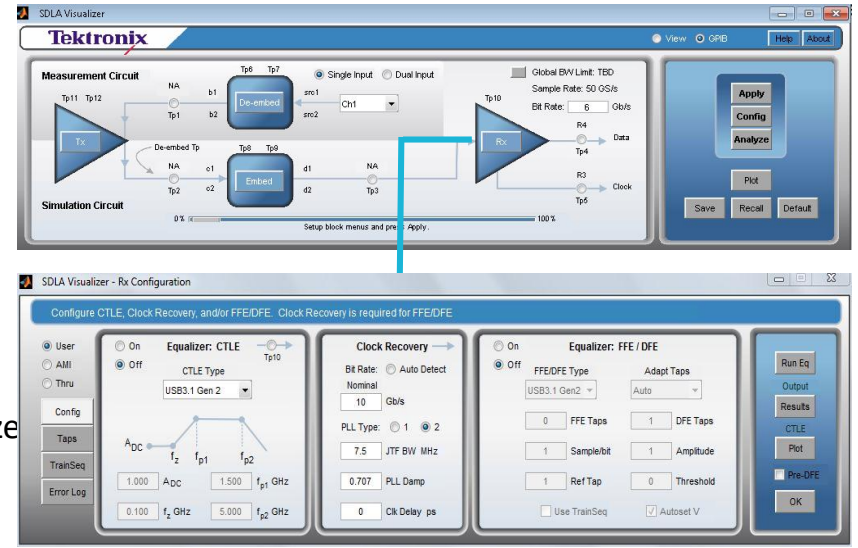
PROBLEMS WITH CHANNEL BEHAVIOR

- Inability to probe at required location in signal path
- Reflections, cross-coupling, fixture losses, cable effects
- Closed eye analysis
- Standards mandate eye analysis at various test points



SOLUTION:

- Enables virtual probing through test points
- Remove the effects of the cables, probes and fixtures
- Open a closed eye
- Model each block through different techniques and visualize each test point in the block using plots



USB-IF Fixtures

USB3ET FOR TYPEA/MICROB @ 5GBPS

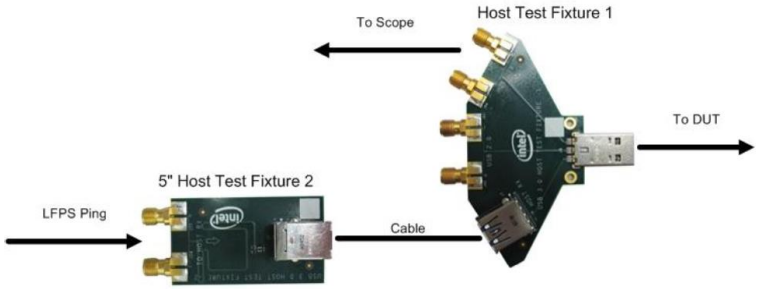


Figure 6: Host Tx Test Topology

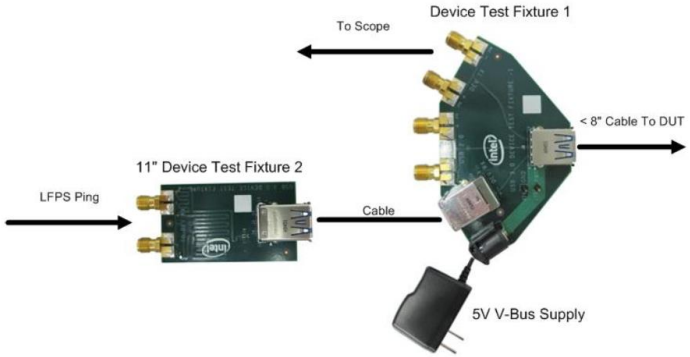
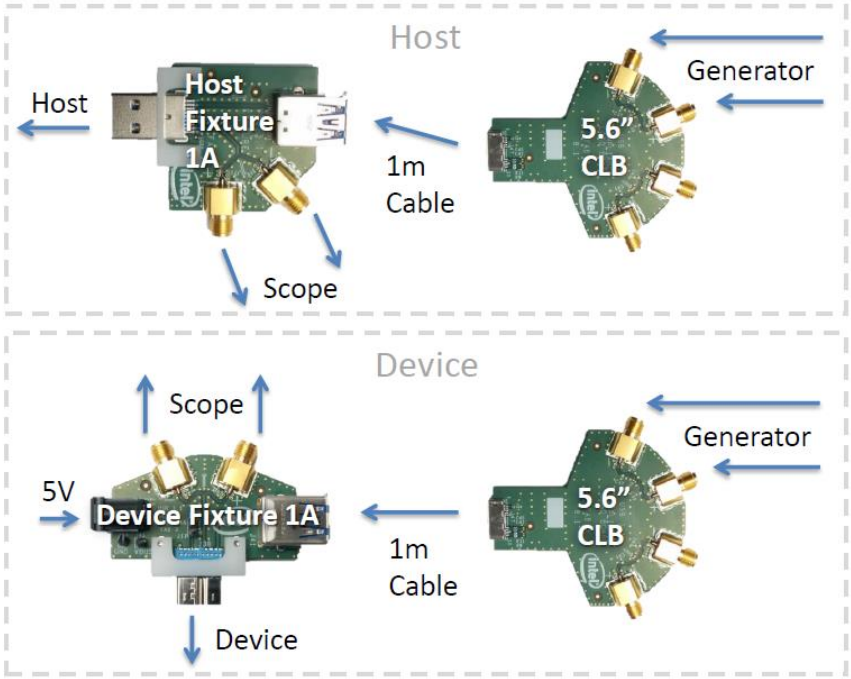
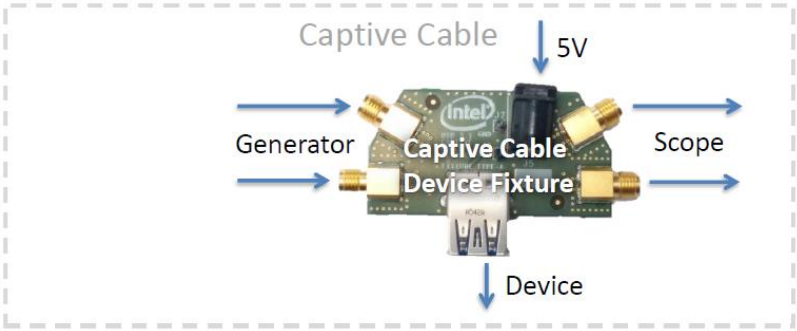


Figure 5: Device Tx Test Topology

USB-IF Fixtures

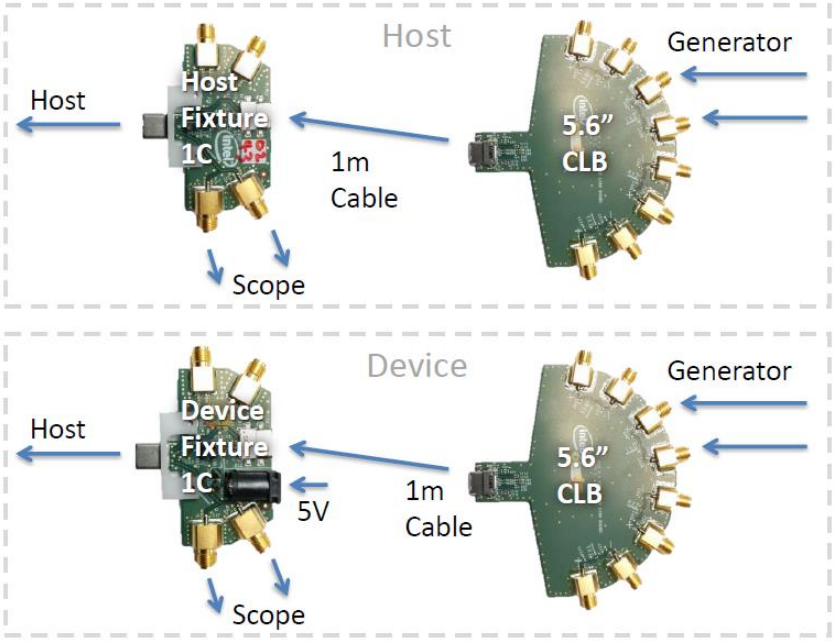
USB31AET FOR TYPEA/MICROB @10G/5GBPS

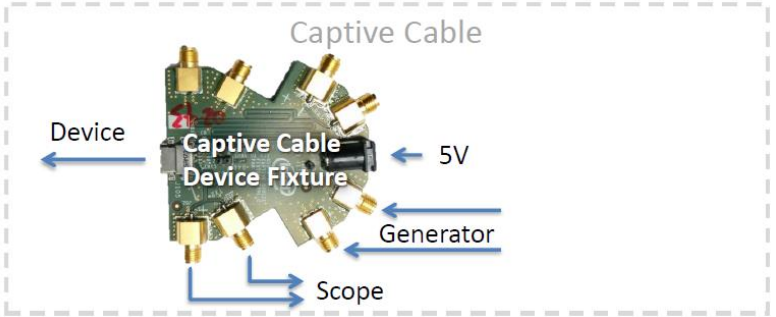




USB-IF Fixtures

USB31CET FOR TYPEC @10G/5GBPS

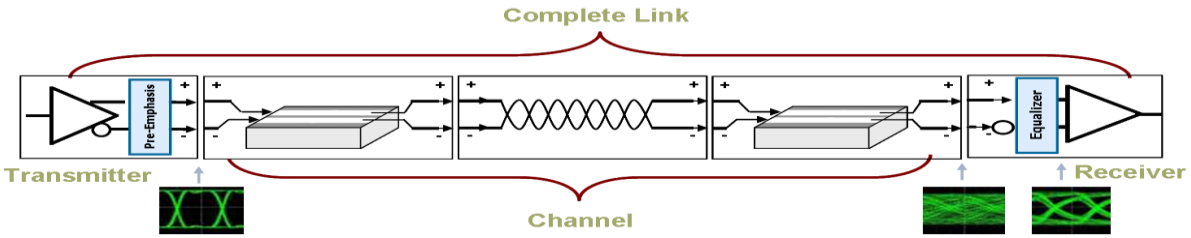




USB 3.1 Rx Testing Overview

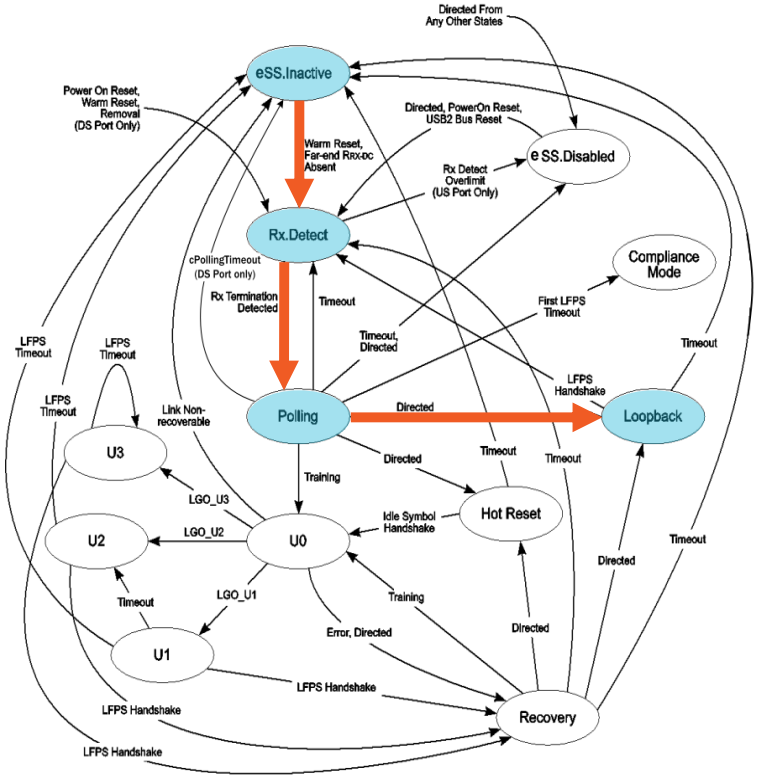
A jitter tolerance test is required for certification, though debug and characterization capabilities are needed to ensure that receivers will work in real world conditions

- Send specific test data patterns to the device-under-test (DUT) through a known channel (fixtures and cables)
- Add a specific “recipe” of stresses and de-emphasis
- Command the DUT into loopback mode (far-end retimed)
- Return “echoed” data to a BERT
- Detected errors are inferred to be a result of bad DUT receiver decisions



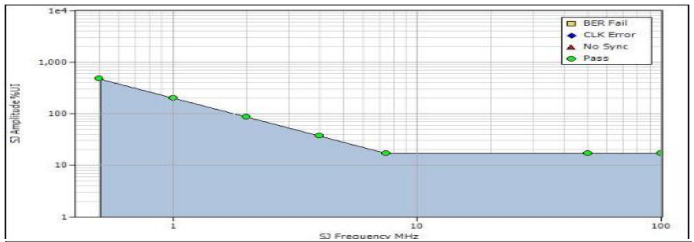
Getting a DUT Into Loopback Mode

- Basic Overview
  - DUT starts in Power-off, or test fixture un-plugged
  - At device power-on or hot plug, BERT sends LFPS signaling
  - Device responds by going from LFPS.Polling to training sequence
    - Handshaking sequence between DUT and BERT: TSEQ > TS1 > TS2
    - TS2 sequence from BERT sets loopback bit to force DUT into loopback for Rx testing



Rx Tolerance Test Overview (JTOL)

- Nine Test Points (USB3.1 Gen2)
- SSC Clocking is enabled
- BER Test is performed at 10^{-10}
- Preshoot/De-emphasis enabled
- Stress verified by TJ/Eye Height
- Each SJ term in the table is tested one at a time after the device is in loopback mode



MHZ	Test	Template	Bits	Errors	BER	Status	Margin
0.50	476.00%	476.00%	3.00e010	0	0.00e000	Passed	0.00%
1.00	203.00%	203.00%	3.00e010	0	0.00e000	Passed	0.00%
2.00	87.00%	87.00%	3.00e010	0	0.00e000	Passed	0.00%
4.00	37.00%	37.00%	3.00e010	0	0.00e000	Passed	0.00%
7.50	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
50.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
100.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%

Frequency	SJ	RJ
500kHz	476ps	1.308ps RMS
1MHz	203ps	1.308ps RMS
2MHz	87ps	1.308ps RMS
4MHz	37ps	1.308ps RMS
7.5MHz	17ps	1.308ps RMS
15MHz	17ps	1.308ps RMS
30MHz	17ps	1.308ps RMS
50MHz	17ps	1.308ps RMS
100MHz	17ps	1.308ps RMS

USB Solutions Portfolio

70K Series Scopes

- USB TX Analysis (DPOJET)
- Automated USB TX

BERTScope

- Automated USB RX

Technology

TX

- USB 3.1
  Gen 1 - 5 Gbps
  Gen 2 - 10 Gbps

RX

- USB @ 20G

5K/7K Series Scopes

- USB 2
  TX & RX
- SR – USB
  Protocol Decode
- USB - PD

USB-IF Logo Certification

TEKTRONIX APPROVED GOLD TEST SUITES AT USB-IF WORKSHOPS

- USB 3.1 Gen2 Tx & Rx – USBIF Approved Gold Test Suite
- USB 3.1 Gen1 Tx & Rx – USBIF Approved Gold Test Suite
- USB 2.0 – USBIF Approved Gold Test Suite
- USB PD – USBIF Approved Gold Test Suite

	USB Performance Only	USB Performance + USB Power Delivery
Original USB		
SuperSpeed USB		
SuperSpeed USB 10Gbps