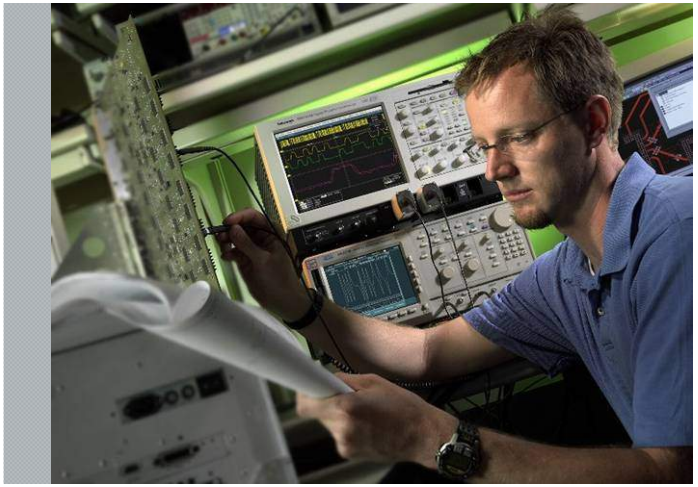
计算机，通讯以及嵌入式系统
调试以及验证解决方案



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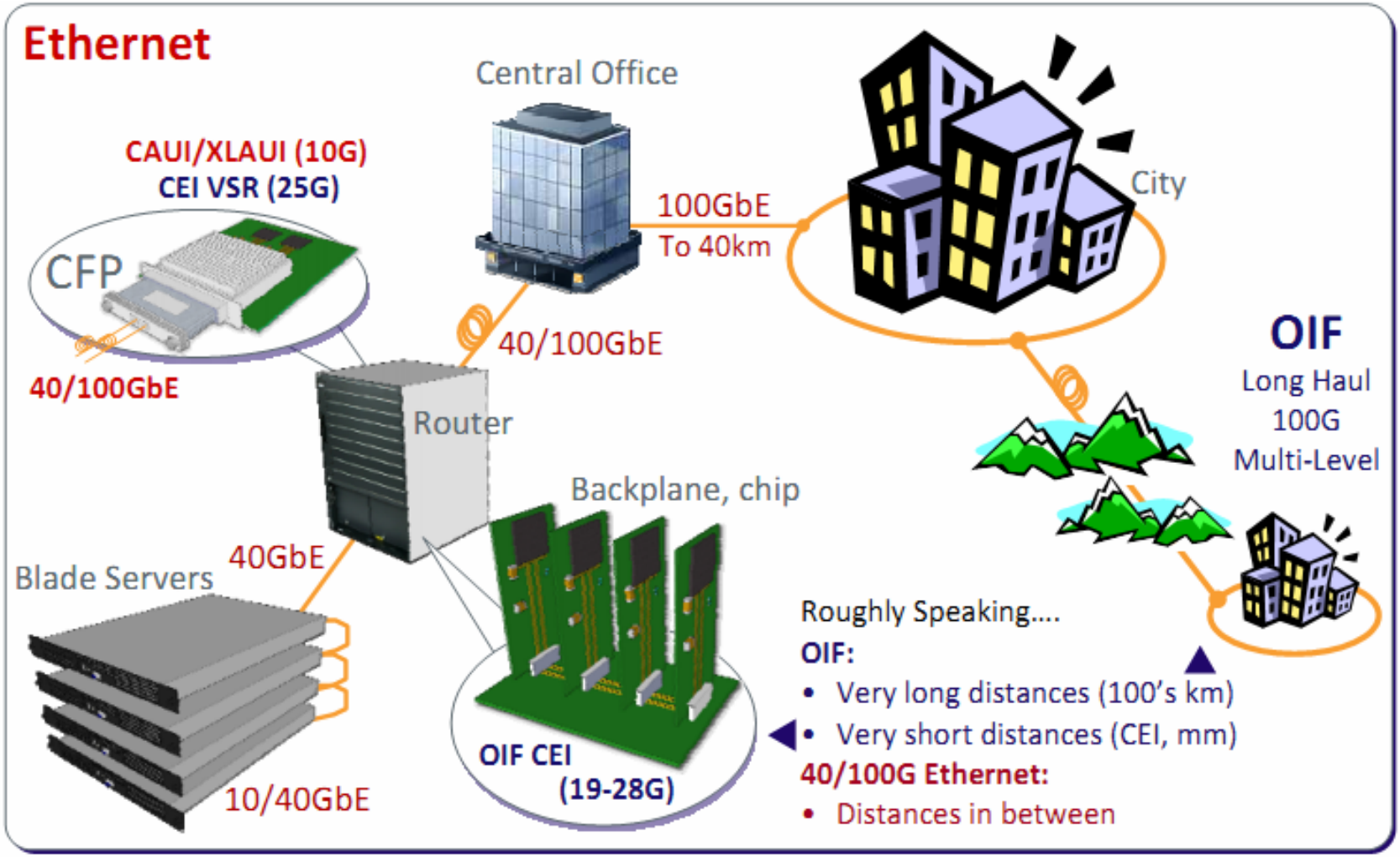
网络通信产品的发展趋势



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计算机产品的发展趋势

PCI EXPRESS

SERIAL ATA

HDMI

ddr3 A JEDEC STANDARD

DisplayPort

IEEE GbE

USB3.0 5Gbps

PCIE 3.0 8Gbps

SAS 3.0　12Gbps

行业/技术/市场趋势

- 接口从低速并行技术转向高速串行技术
- 数据速率继续提高:
  3 ⇒ 6 ⇒ 10 ⇒ 12 Gb/s
- 行业标准化，实现即插即用互连
- 消费电子成为更大的推动因素

对测试测量的影响

- 千兆位数据速率需要性能更高的产品
- 行业标准提出了严格的测量和分析要求
- 测试整个系统，包括发射机、接收机和传输路径或电缆
- 要求广泛的产品系列及提高一致性测试的自动化程度
- 测试测量在标准机构中发挥着关键作用

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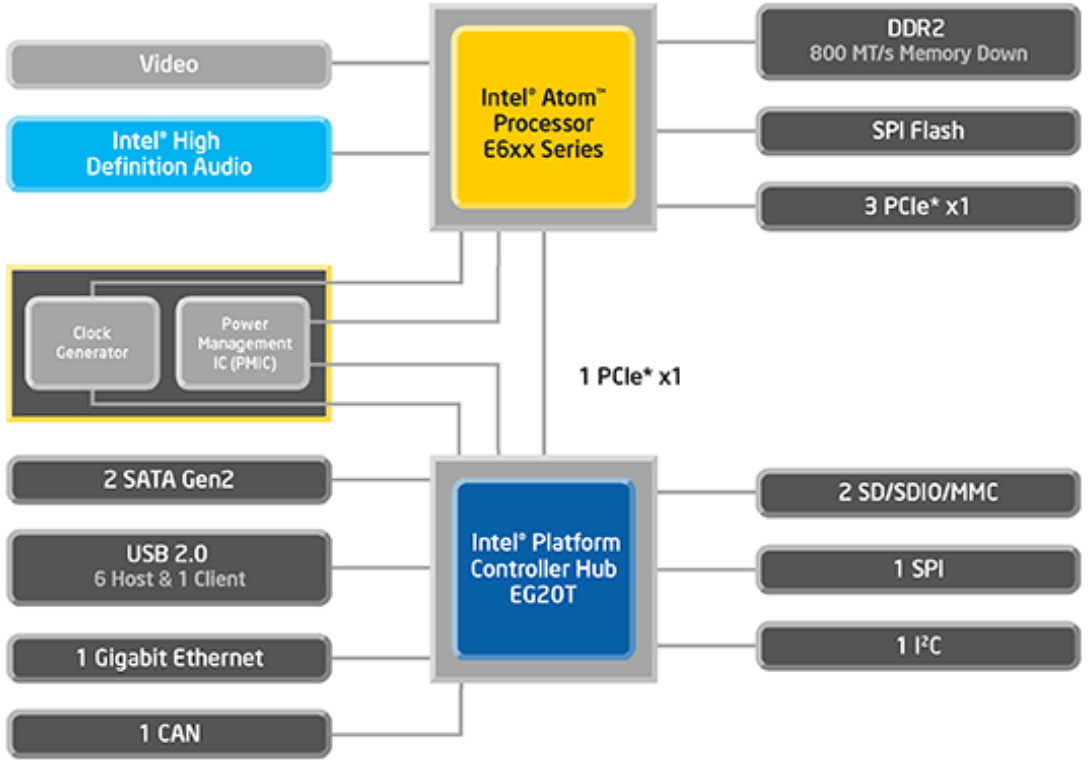
嵌入式系统

- 串行总线
  - USB2.0
  - Ethernet
  - I2C & I2S
  - SPI
  - DDR & LPDDR
  - SDIO & MMC
  - PCIe
  - TCON (LVDS/DP)
- ADC/DAC/Codec编解码
- Tx/Rx & WLAN
- 电池与开关电源管理



Intel英特尔®凌动™处理器

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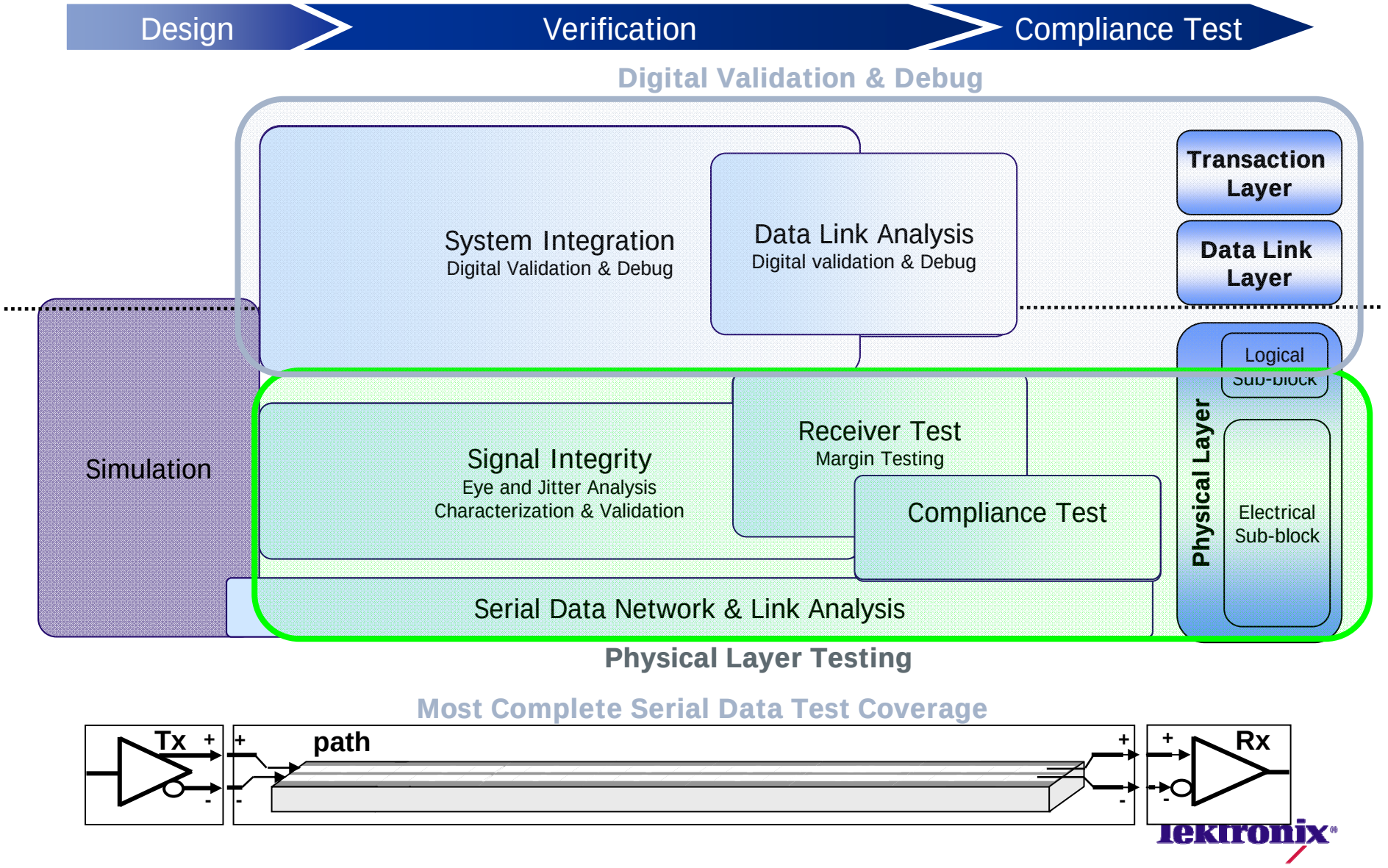
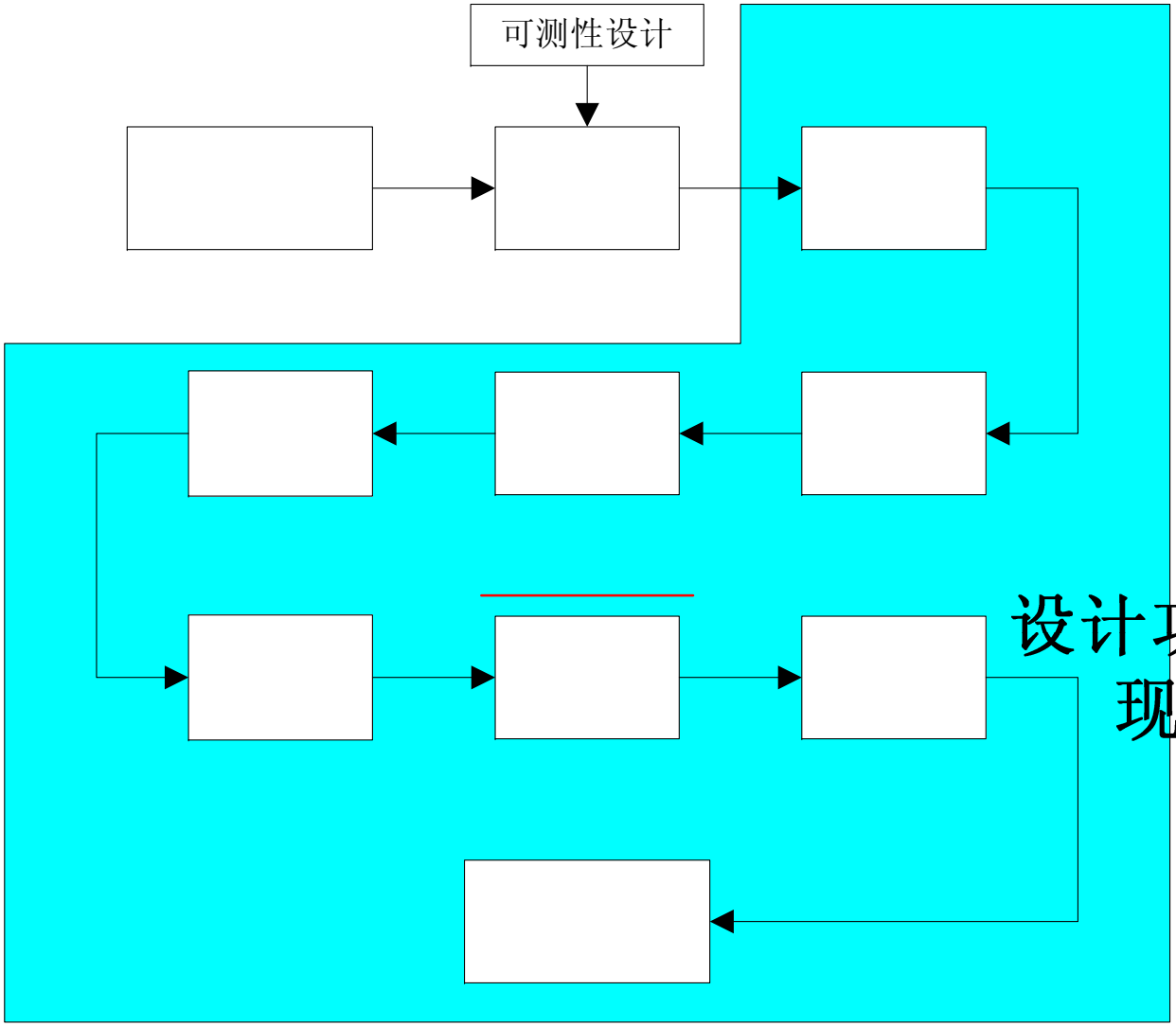
高速数字系统测试验证解决方案



设计流程概览

- 每一步都很重要，将会对以后的步骤产生深远的影响



设计功能及实现原理

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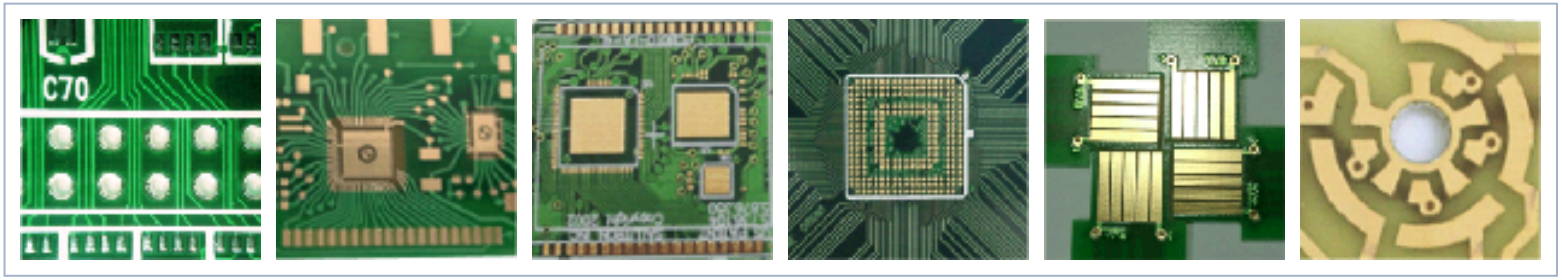
内部总线互连能力

高速互连的测试和验证



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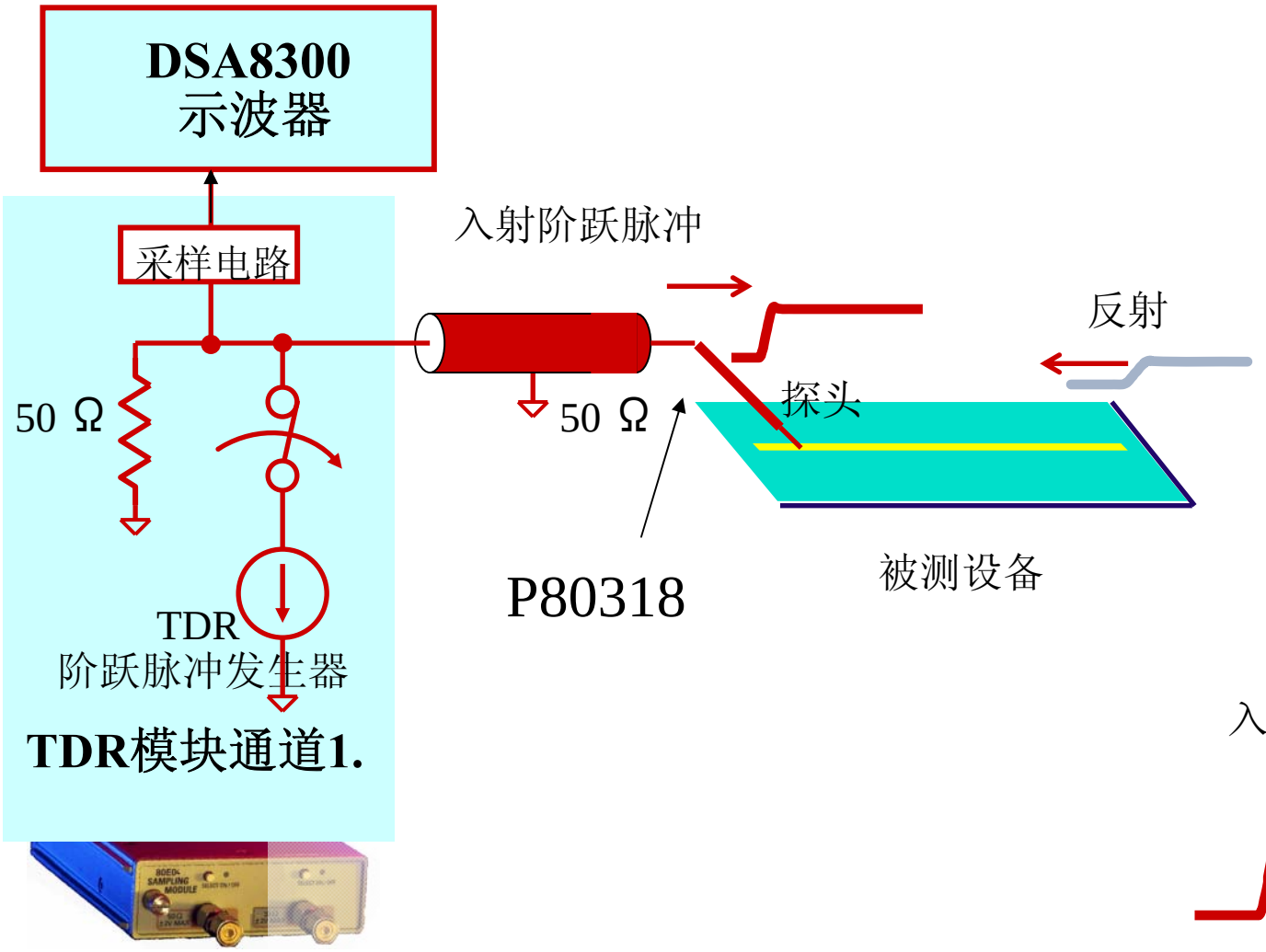
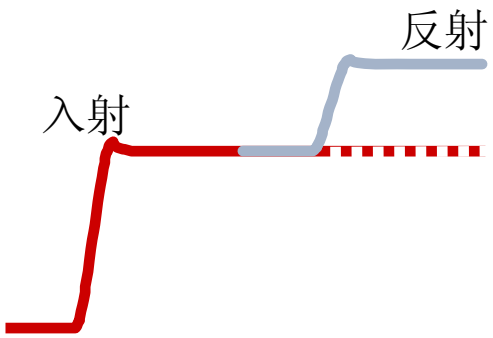
TDR概述及原理——典型系统



结果是入射值和反射值之和:



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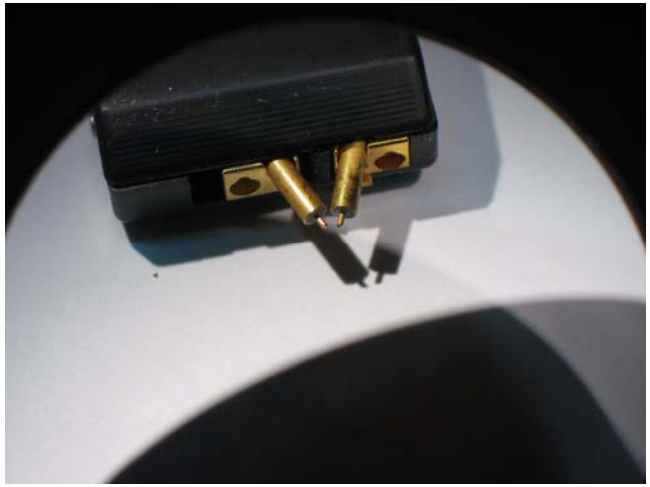
高带宽差分TDR探头是测试关键

- **P80318 – 18GHz 100 Ω 手持式TDR阻抗测量探头**
  - **0.5mm to 4.2mm可调间距探头尖**
  - **FR4材质PCB最小2.5 mm (0.1 in.) 间距分辨**
  - **与80A02模块一起使用时提供EOS/ESD 保护功能**
- **专门优化用于差分TDR/TDT测量**
- **P80318X – 18GHz 100 Ω 手持式TDR差分阻抗测量附加探头**
  - **用于主要探头需要维护时的替代品,确保生产时间**



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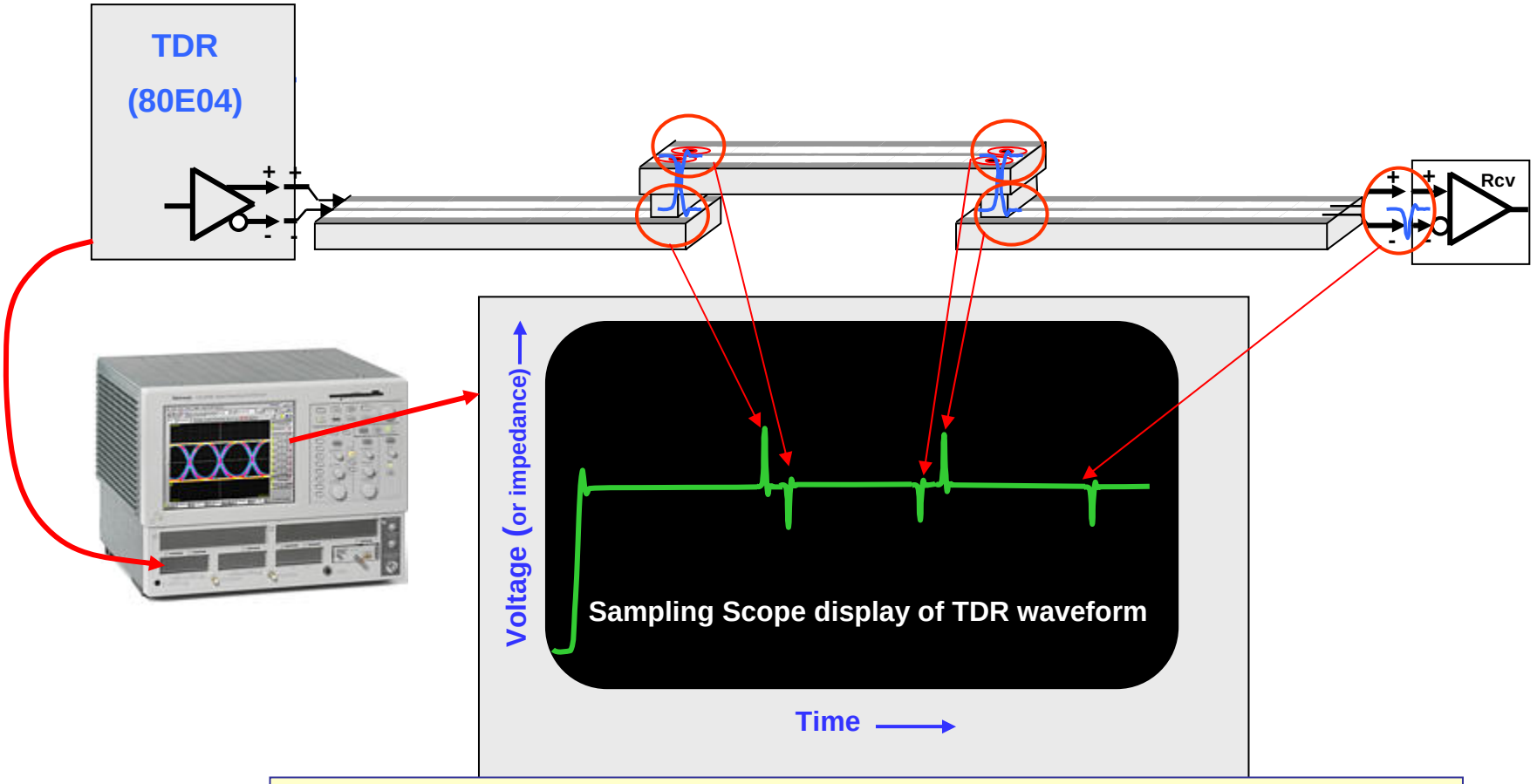
TDR在信号完整性SI(Signal Integrity)中的应用——**Reflection(反射)**



- *TDR on an Equivalent Time scope is used to measure the quality of the serial data interconncet: A step is generated and returning reflections are sampled (**it's like radar for serial data cables and boards**)*

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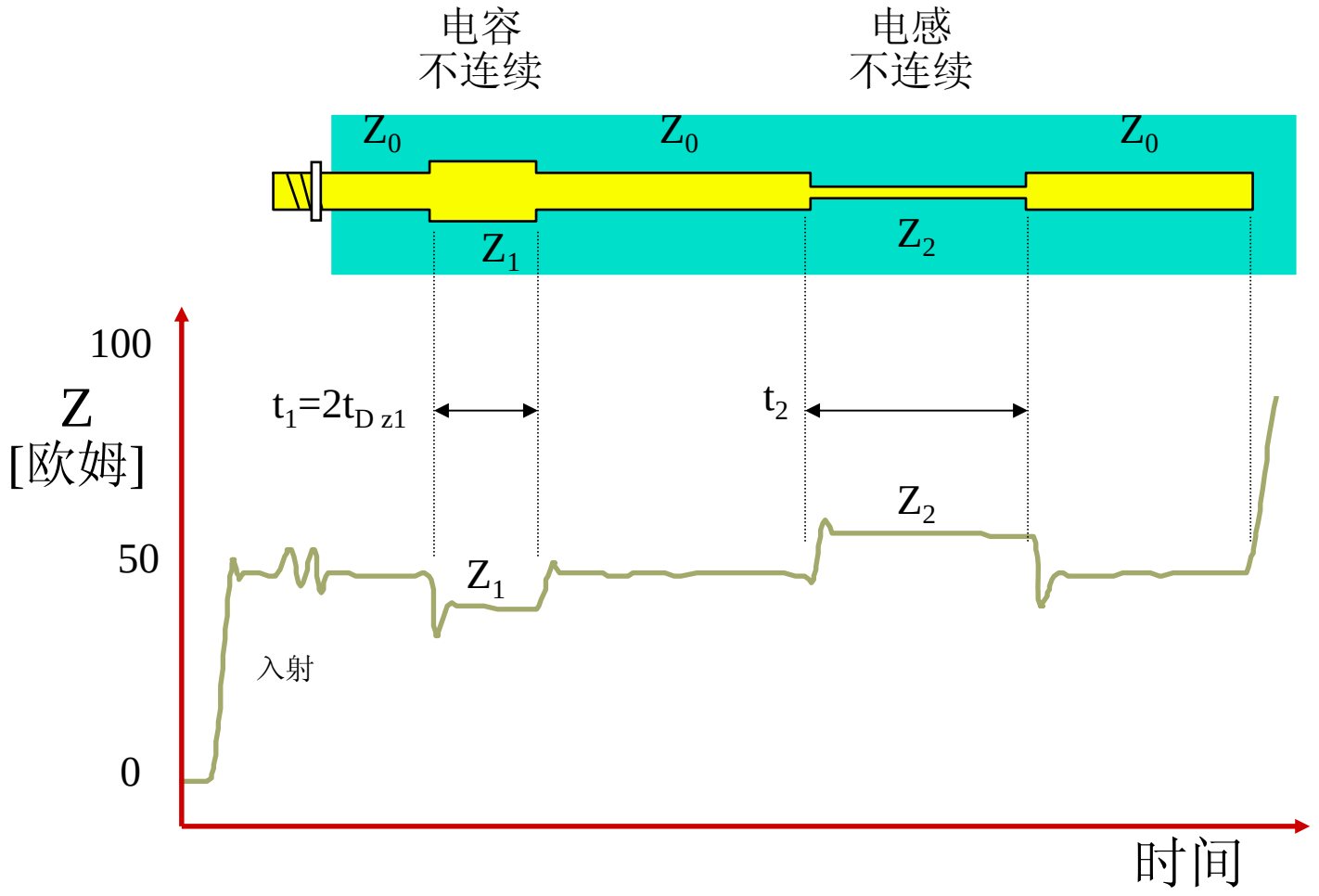
TDR概述及原理－更加复杂的走线



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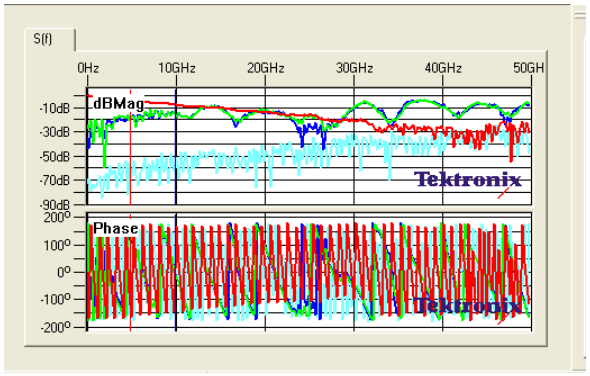
IConnect软件－信号完整性和S参数自动测量软件

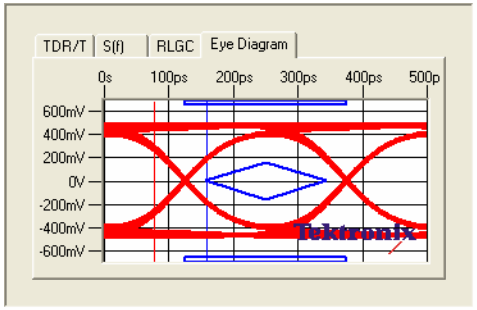
性能

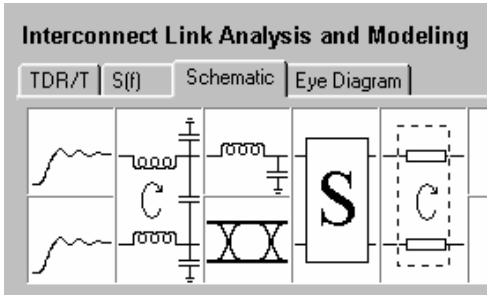
- 高达70dB的动态范围
- 改善了阻抗测量精度和分辨率(Z-Line)
- 1M 记录长度，可以在更高频率测量长互连



高效，简单

- 自动程序，最大限度地减少错误，降低测试时间
- 为制造应用提供了命令行界面
- 全面的互连链路分析功能
- 自动提取SPICE模型，集成式分析功能，并支持仿真模型
- 在几分钟内、而不是几个小时内完成分析任务





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第二部分：基本功能验证(模拟数字部分)

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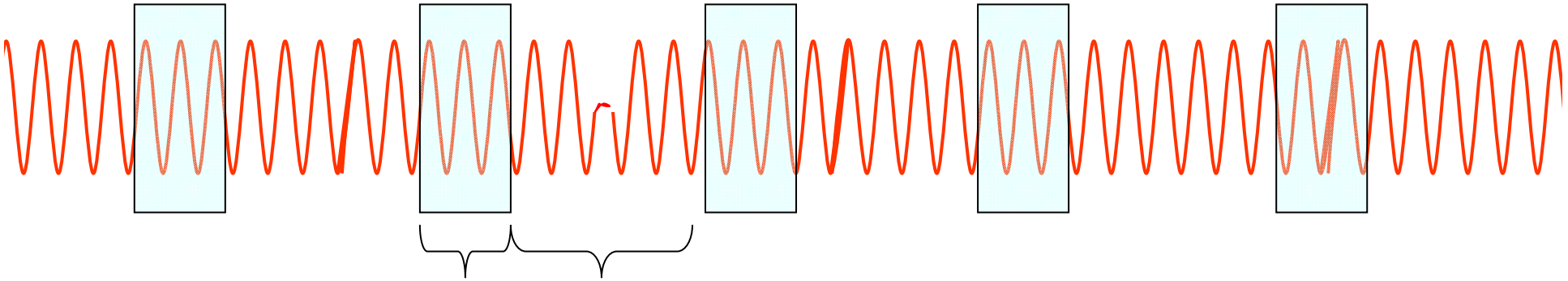
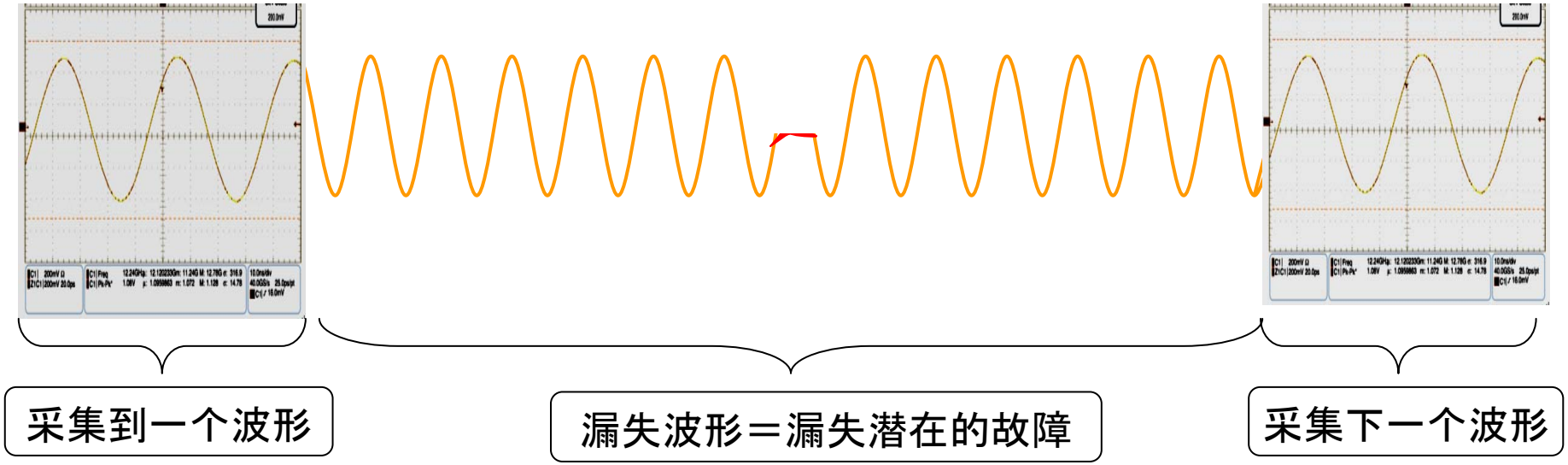
示波器波形捕获率：每一秒采集多少个波形





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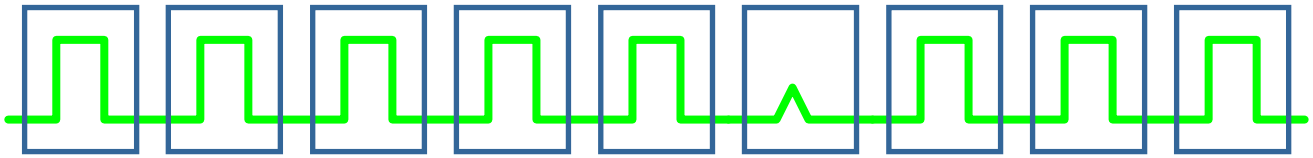
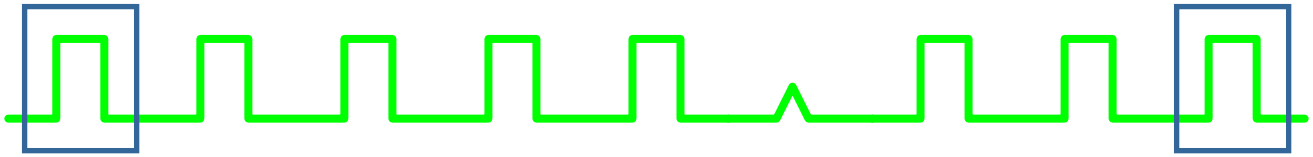
波形捕获率对测试结果的影响

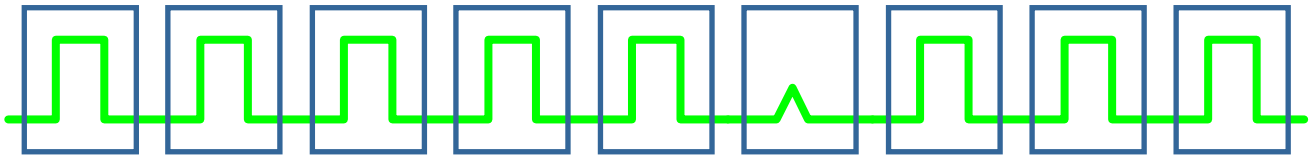
模拟实时



数字存储



DPX 技术



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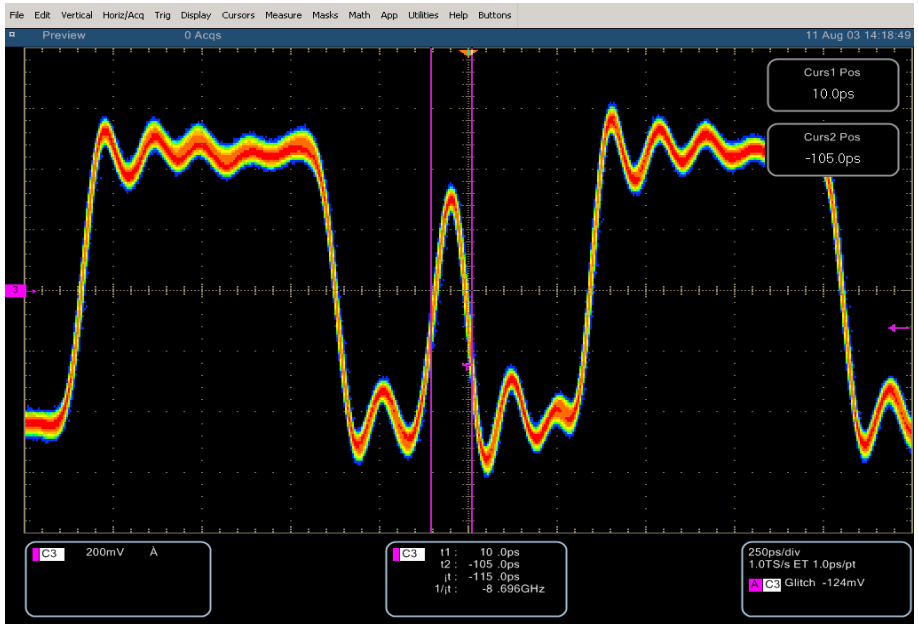
Productivity

DPO的效率——触发系统

- 触发系统——最快定位电路特定行为的工具
- 好的工程师使用长内存——DPO当然提供；聪明的工程师使用触发——泰克使您更聪明

- 完美的Pinpoint™触发系统，可以几乎没有限制地定义条件，捕获最快的瞬变信号



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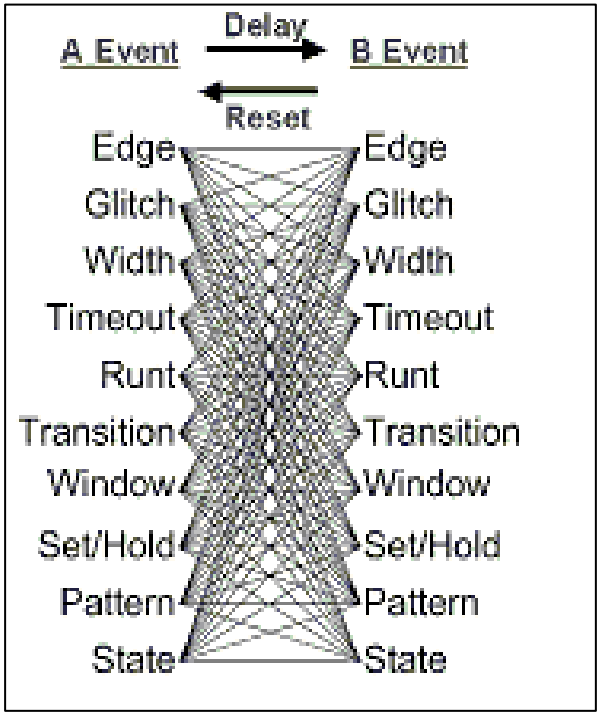
Productivity

DPO的效率——触发系统

- 使用顶级的触发技术
  - 在所有触发方式下使用最新一代SiGe技术，性能全面超过业界其它产品
- 广泛使用于泰克中高端示波器的Pinpoint™触发系统
  - 九大类触发模式灵敏度可高达9GHz
- Pinpoint™ 触发系统
  - 业界最完善的触发系统
  - 唯一完善的双触发系统

Virtually Unlimited Trigger Combinations
Plus Comm & Serial



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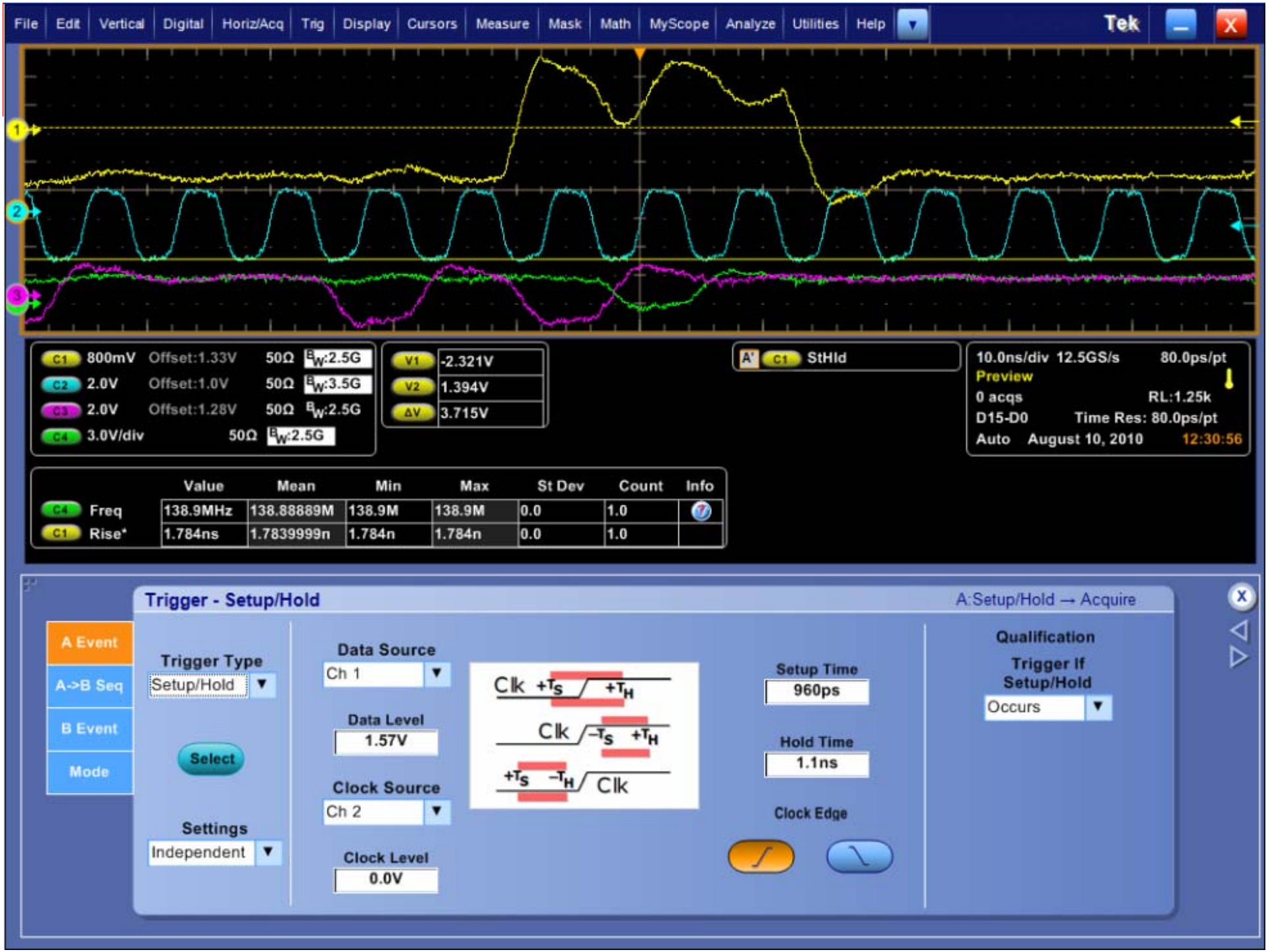
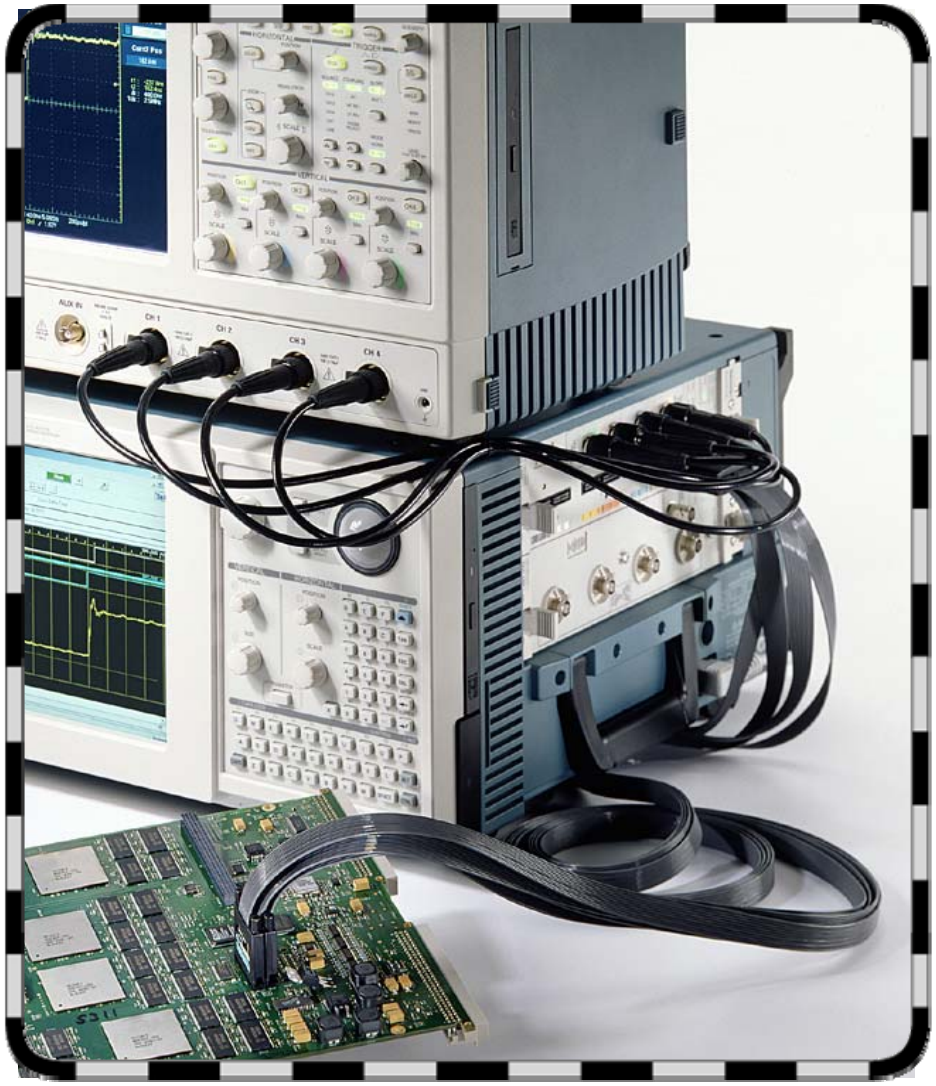
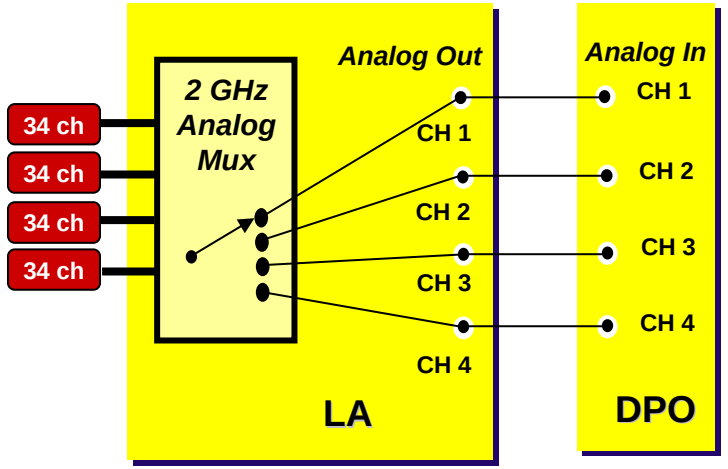

File
Edit
Vertical
Digital
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
C1 800mV Offset:1.33V 50Ω BW:2.5G
C2 2.0V Offset:1.0V 50Ω BW:3.5G
C3 2.0V Offset:1.28V 50Ω BW:2.5G
C4 3.0V/div 50Ω BW:2.5G
V1 -2.321V
V2 1.394V
ΔV 3.715V
A' C1 StHld
10.0ns/div 12.5GS/s 80.0ps/pt
Preview
0 acqs RL:1.25k
D15-D0 Time Res: 80.0ps/pt
Auto August 10, 2010 12:30:56
Value Mean Min Max St Dev Count Info
C4 Freq 138.9MHz 138.88889M 138.9M 138.9M 0.0 1.0
C1 Rise* 1.784ns 1.7839999n 1.784n 1.784n 0.0 1.0
Trigger - Setup/Hold
A:Setup/Hold → Acquire
A Event
A->B Seq
B Event
Mode
Trigger Type
Setup/Hold
Select
Settings
Independent
Data Source
Ch 1
Data Level
1.57V
Clock Source
Ch 2
Clock Level
0.0V
Clk +TS +TH
Clk -TS +TH
+TS -TH Clk
Setup Time
960ps
Hold Time
1.1ns
Clock Edge
Qualification
Trigger If Setup/Hold
Occurs

全新的信号完整性调试理念-模拟数字联合调试

新



- 单LA探头连接信号，同时测量信号模拟、逻辑特性
- LA探头所有通道模拟带宽指标2~3 GHz
- LA中136通道任意4路可以输出到外部示波器



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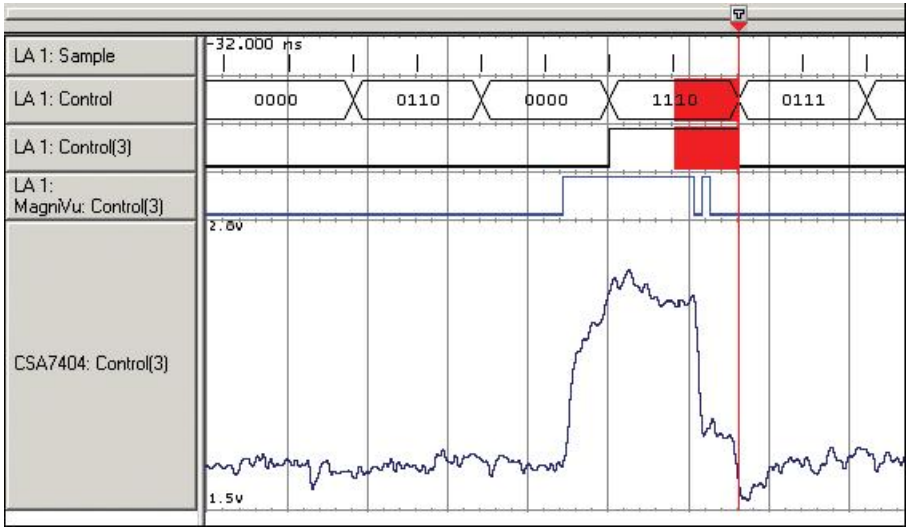
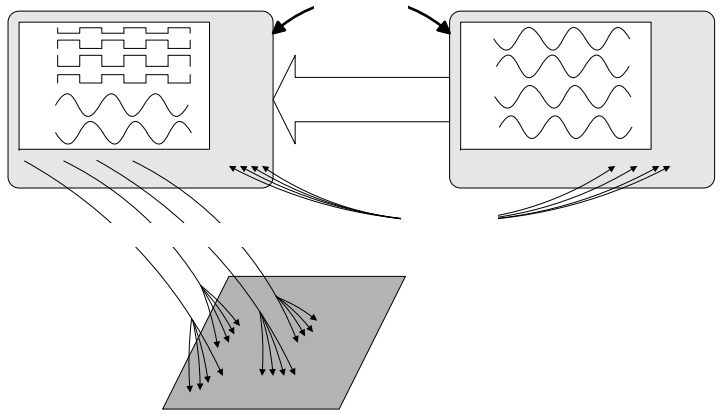
模拟、数字联合调试方案

- 毛刺捕获技术
  - 实时动态监控信号中的异常逻辑
  - 高亮标注
  - 准确定位异常发生时刻、位置
- iView
  - 将逻辑分析仪和示波器无缝连接为一套测试系统
  - 在逻辑分析仪屏幕上显示自动时间对齐后的同一信号模拟和数字的波形
  - 通过逻辑分析仪对示波器的触发控制，准确定位信号异常时的模拟采集





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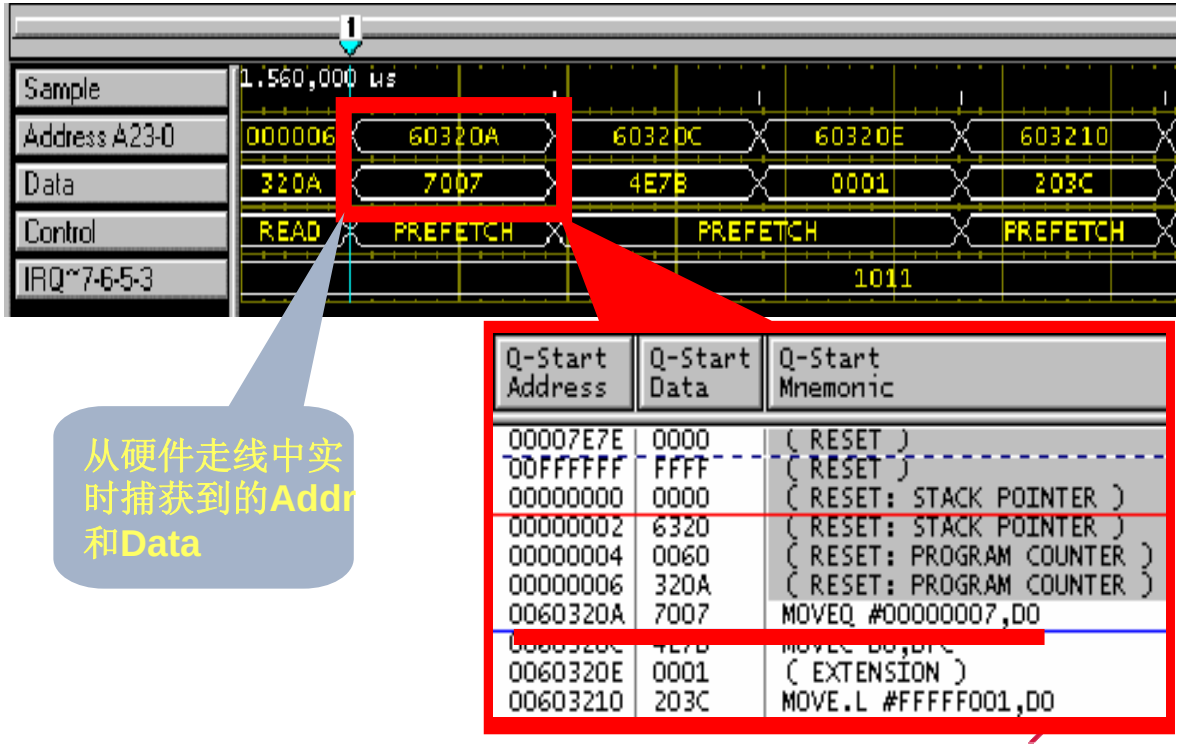
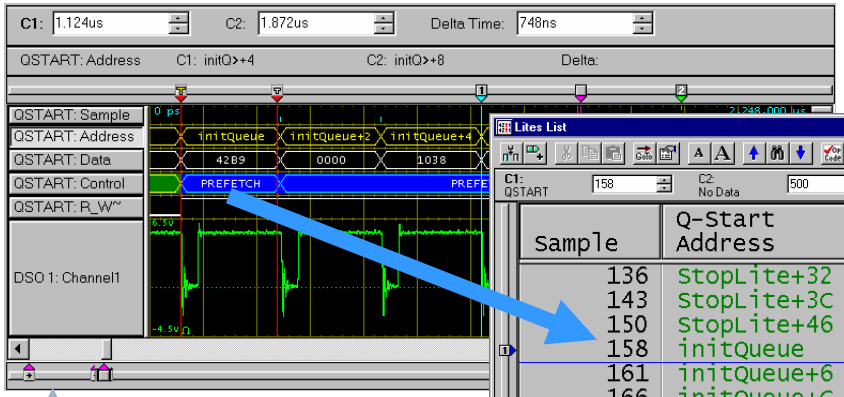
嵌入式软件调试和验证

- 捕获、分析和显示实时软件执行的过程以及定位问题的根源
- TLA可以将软件执行和其他的系统事件联系起来
  - 总线协议事件: IEEE-1394, USB,LVDS etc.
  - 硬件事件: Interrupts, DMA cycles, Suspend,etc.
- TLA不会影响嵌入式软件实时的运行

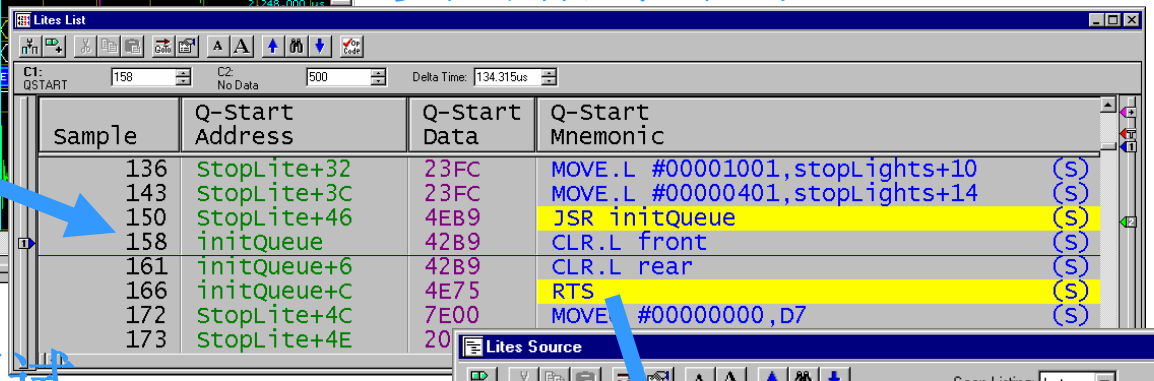


TLA嵌入式系统方案

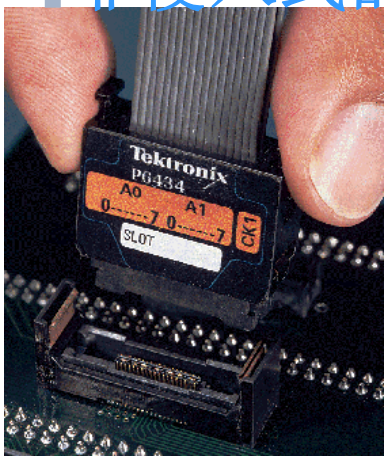
实时硬件信号探测

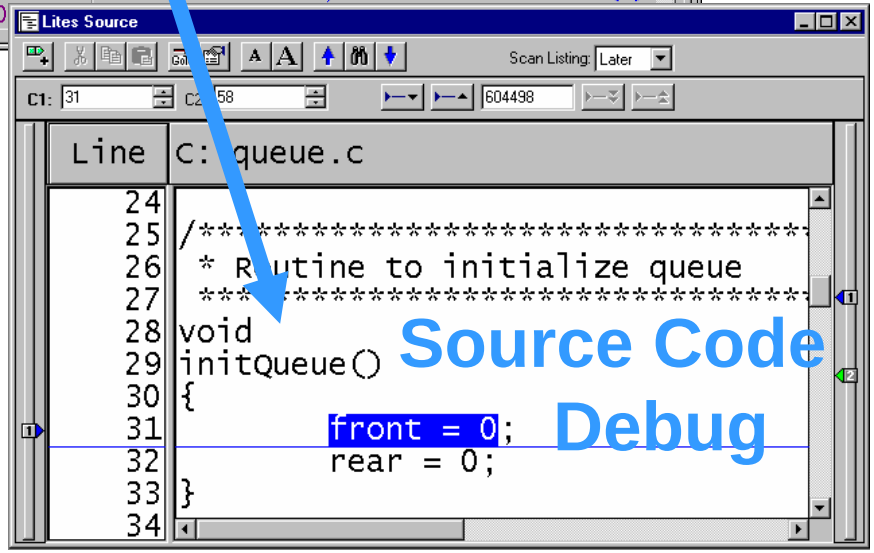


实时指令跟踪



非侵入式的调试





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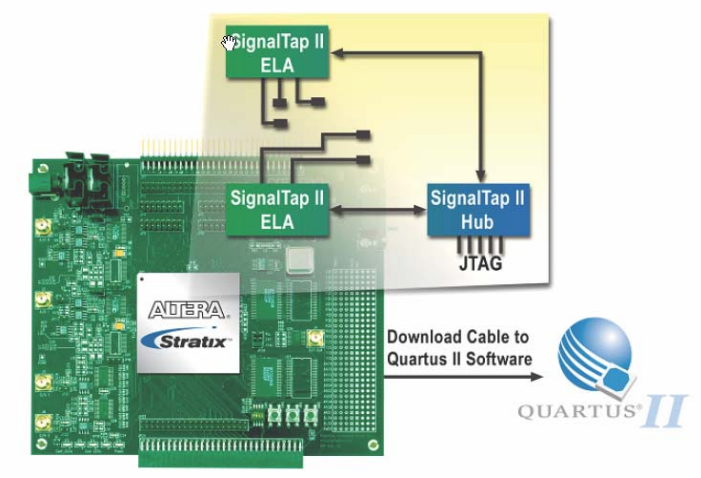
In-Circuit FPGA Debug Methods

- Embedded Logic Analyzer
  - Logic analyzer functionality is inserted in design
    - Has triggering and trace storage resources
    - Uses FPGA memory
  - Examples:
    - SignalTap® II (Altera)
    - ChipScope™ ILA (Xilinx)
    - CLAM® (Actel)



- External Logic Analyzer
  - Use a full-feature logic analyzer
    - Route internal signals to FPGA pins and observe with TLA Series logic analyzer
    - Make use of programmability of FPGA

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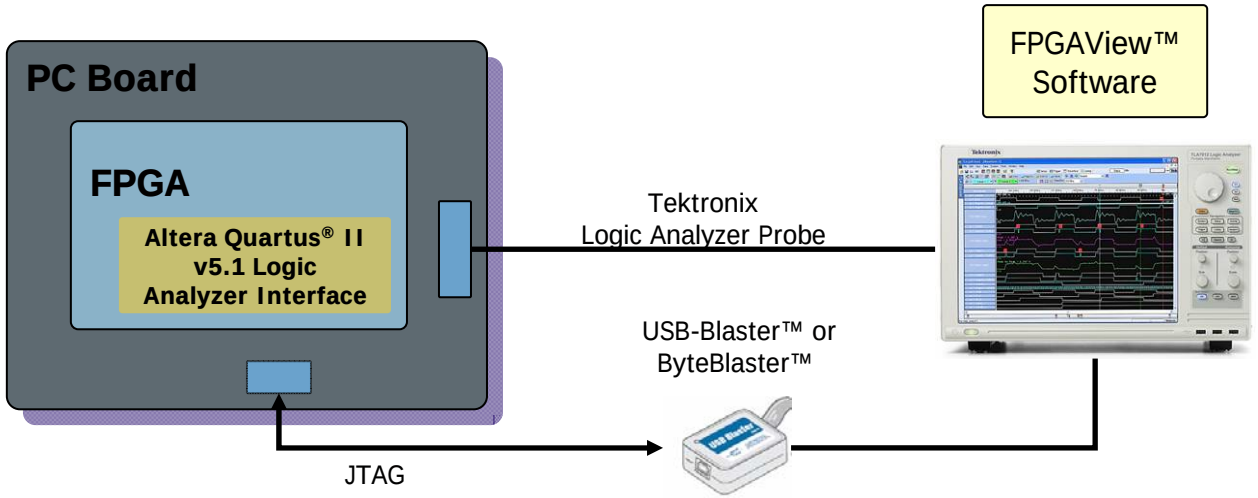
Real-Time Logic Debug Solution for Altera FPGAs

Overview

- Software package developed by First Silicon Solutions (www.fs2.com)
  - Supports Altera FPGA devices
  - Runs on Windows 2000 and Windows XP machines

Function	Solution
Multiplexer	Altera Quartus® II v5.1
Control Software	FS2 FPGAView™
Logic Analyzer	Tektronix TLA Series Logic Analyzer, running v4.3 or later
JTAG Cable	Altera USB-Blaster™ or ByteBlaster™
Operating System	Windows® 2000 and Windows® XP



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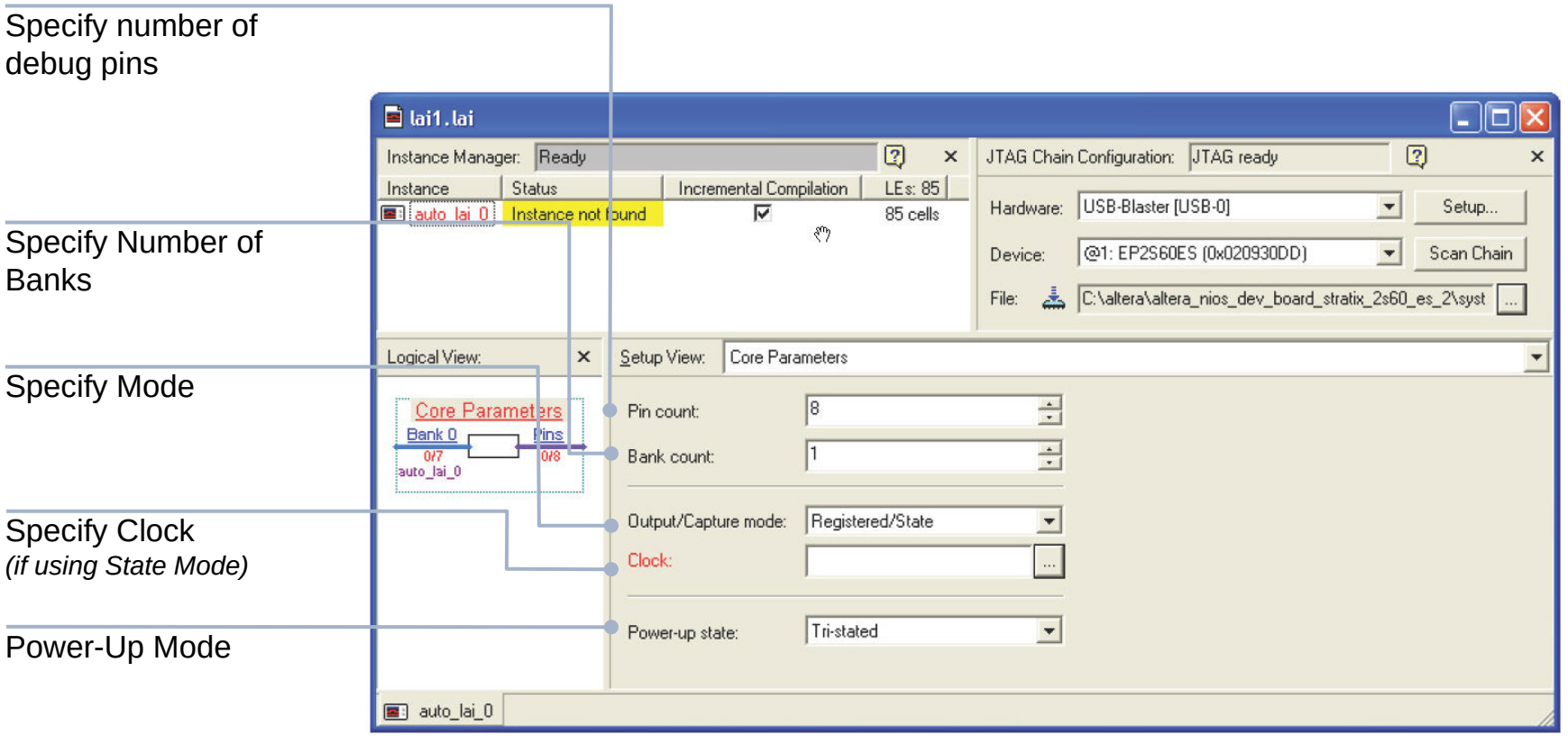
Using FPGAView

Step 1 – Create the Logic Analyzer Interface

- Use Altera Quartus II Logic Analyzer Interface Editor to define and insert Logic Analyzer Interface
  - Available in all editions of Quartus II, including free Web Edition



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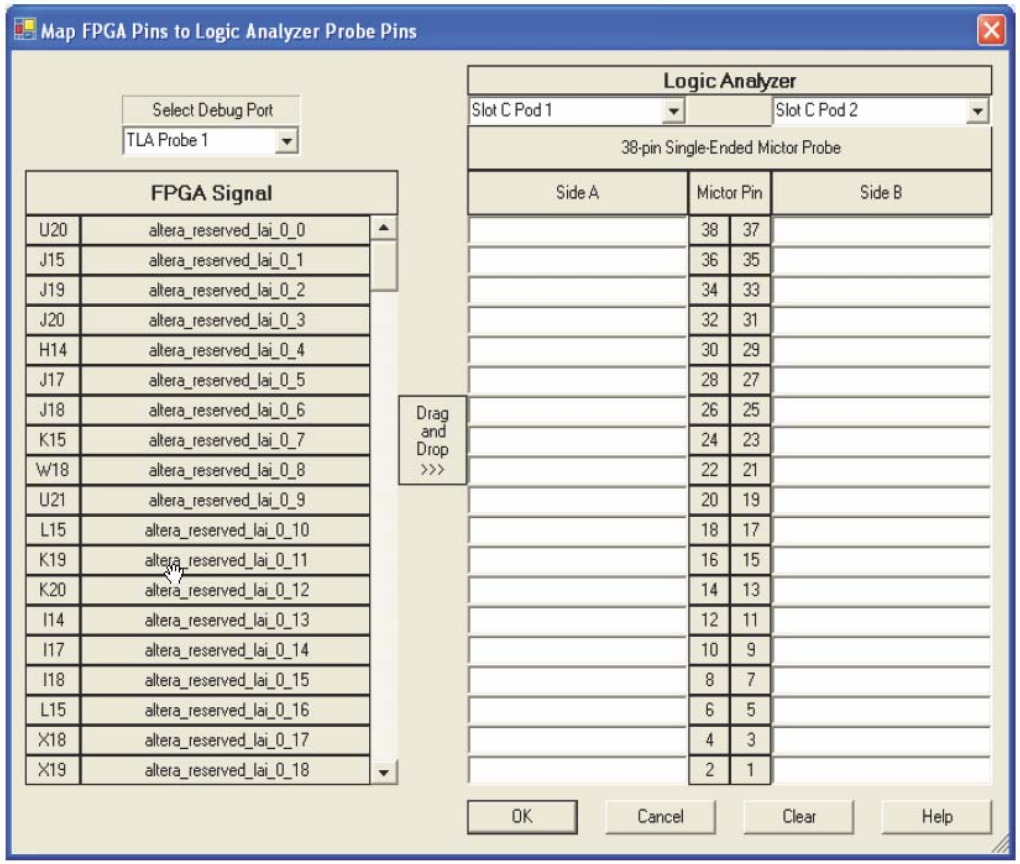
Using FPGAView

Step 3 – Map FPGA Pins to Logic Analyzer

- Use FPGAView to “connect” FPGA pins to logic analyzer
  - Enables automatic channel name updating
  - Drag & Drop operation
  - Supports multiple LAIs / FPGAs / TLA modules

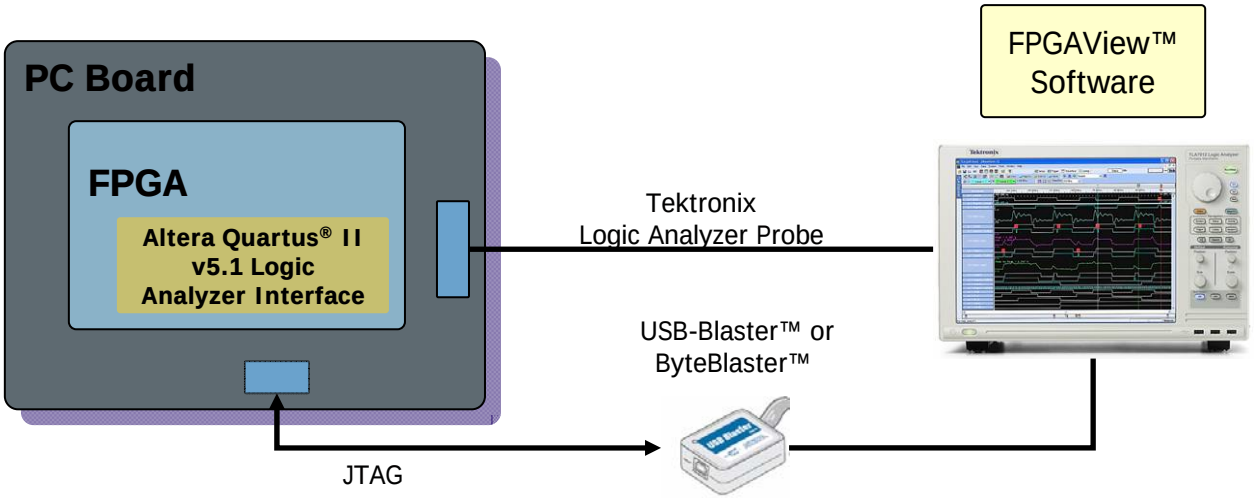


Real-Time Logic Debug Solution for Altera FPGAs

Summary

- FPGAView Configurations
  - One Year Use and Support License
  - Three Year Support License (perpetual use)

Function	Solution
Multiplexer	Altera Quartus® II v5.1
Control Software	FS2 FPGAView™
Logic Analyzer	Tektronix TLA Series Logic Analyzer, running v4.3 or later
JTAG Cable	Altera USB-Blaster™ or ByteBlaster™
Operating System	Windows® 2000 and Windows® XP



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MSO70000 高性能混合信号示波器

Real Time
20 GH

ogic Analyzer
& iCapture

MSO70000

目前世界上唯一的高性能混合信号示波器

Tektronix

MSO70000 高性能混合信号示波器

业内领先的配有高性能数字通道的实时示波器

高性能

▪33G带宽模拟通道
4个通道

▪80ps 数字定时分辨率

▪20 ps模拟定时分辨率

▪深存储

▪对于模拟和数字通道全部为250M/ch

▪16 数字通道
连同4个模拟通道组成的采集系统

iCapture™ 同时进行模拟数字时间相关调试

▪事件触发能力
隔离定位偶发的故障

▪新数字逻辑探头
提供高信号保证度以及最小的负载

集成了并行总线、I2C、SPI解码功能

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MSO5000系列，同时支持数字和模拟调试

- 同类最优秀的探头负荷
  - 超低输入电容 (3.9pF)
  - 输入阻抗大：10MOhm
  - 内部RC电路的突破和改进
  - 高电压动态范围：1GHz,300Vrms
- 每台示波器标配4根探头
  - TPP0500：500MHz (350/500MHz型号标配）
  - TPP1000：1GHz （1/2GHz型号标配）
  - 性能高，使用方便，节省额外购买探头成本
- 多个地线连接， 包括
  - 6英寸地线
  - 接地引线短弹簧夹

有源探头的性能，
无源探头的简便。

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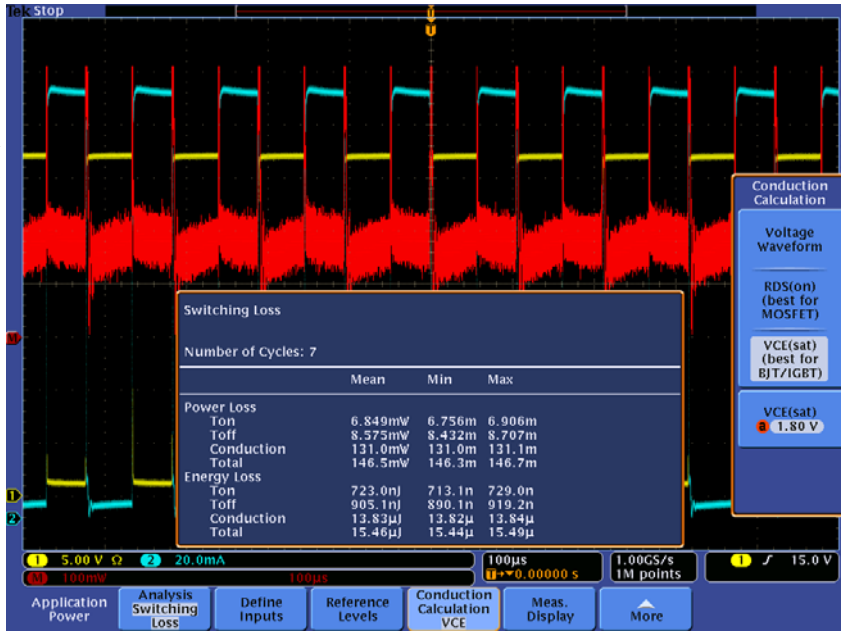
单板或者系统开关电源测量解决方案

- DPOPWR能耗测量分析方案
  - 提供业内最完整、最丰富的能耗测试方案
  - 功率质量
  - 开关损耗测量
  - 安全工作区谐波分析
  - 纹波测量
  - PWM调制分析
  - 变压器磁特性分析



- 丰富的探头系统
  - 高压探头
    - 浮地、共地探头
    - 最高电压20000V
  - 高精度电流探头
    - 最高精度200uA
    - 最大测试电流750A

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第三部分：一致性分析以及验证

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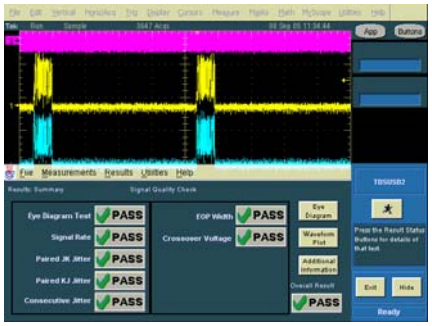
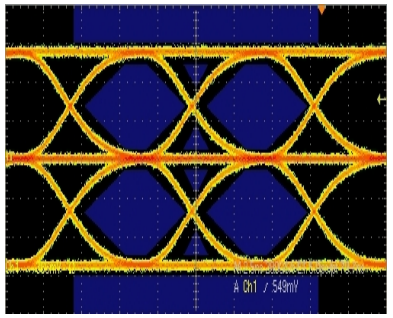
以太网与USB一致性测试、极限/模板测试

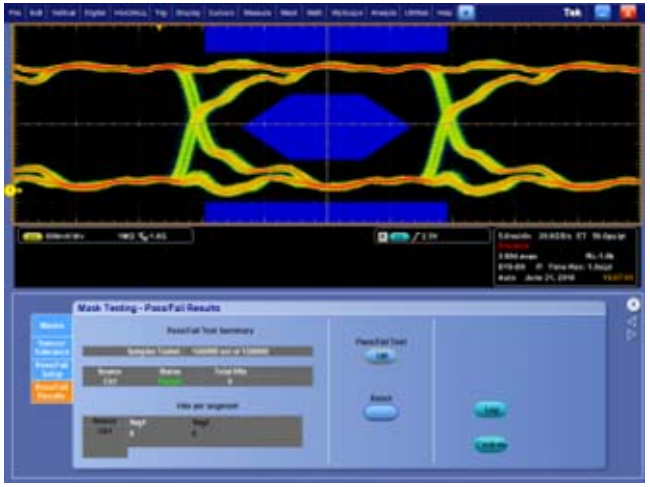
- 以太网与USB2.0串行一致性测试
  - 选项ET3:
  - 选项USB: 低速, 全速, 高速USB2.0 总线
- 极限测试 (选项LT)
  - 设置水平极限和垂直极限，从源波形进行极限测试
- 模板测试 (选项MTM)
  - 常用电信标准和串行标准模板测试
  - 用户自定义模板，测试自定义信号
- 应用
  - 合格/不合格测试
  - 电信或串行标准信号检定



USB 2.0 一致性测试



以太网一致性测试



串行总线与通讯眼图模板测试

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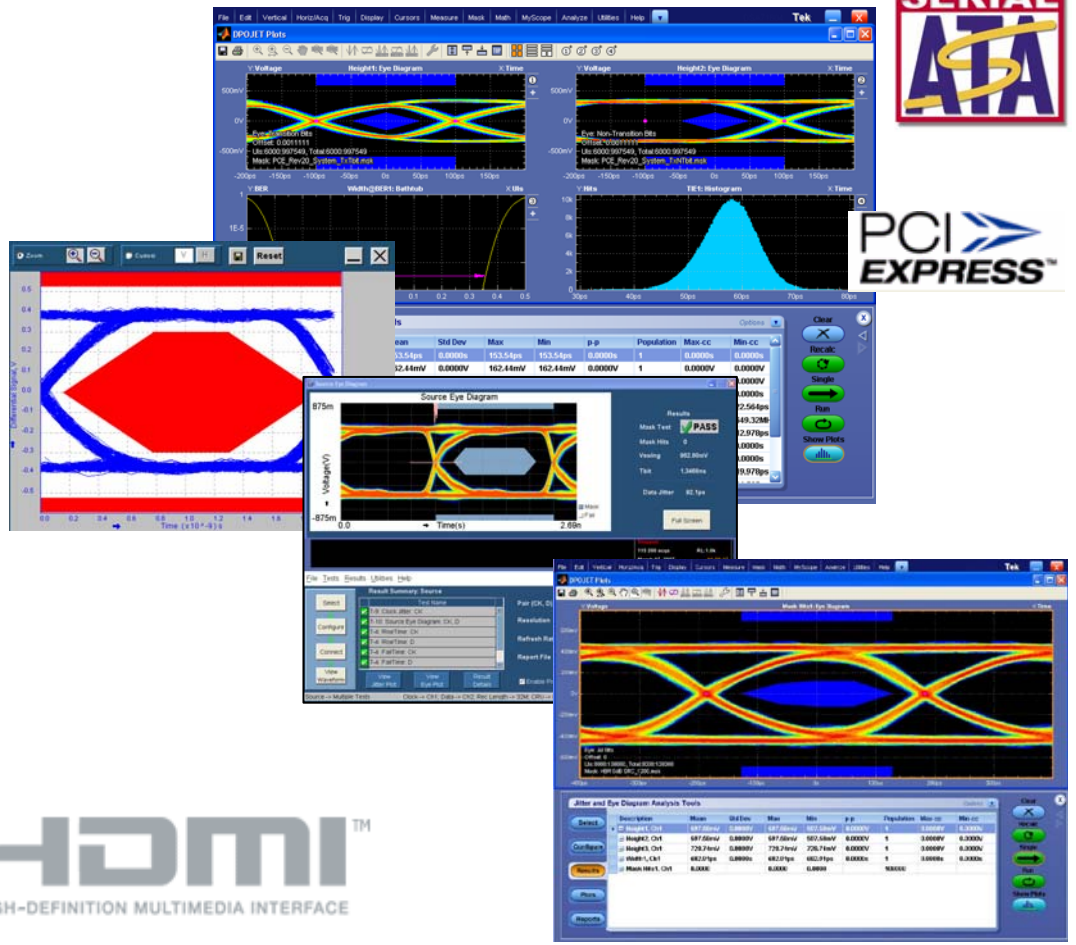
Tektronix提供计算机、通信行业一致性测试标准支持

- PCIExpress Gen 2/Gen 3
- DisplayPort
- HDMI
- SATAII/III
- DDR2/3
- Ethernet
- USB
- WiMedia
- Inifiband
- FiberChannel
- XAUI
- USB3.0



SERIAL ATA

PCI EXPRESS

HDMI
HIGH-DEFINITION MULTIMEDIA INTERFACE

DisplayPort

HI-SPEED USB

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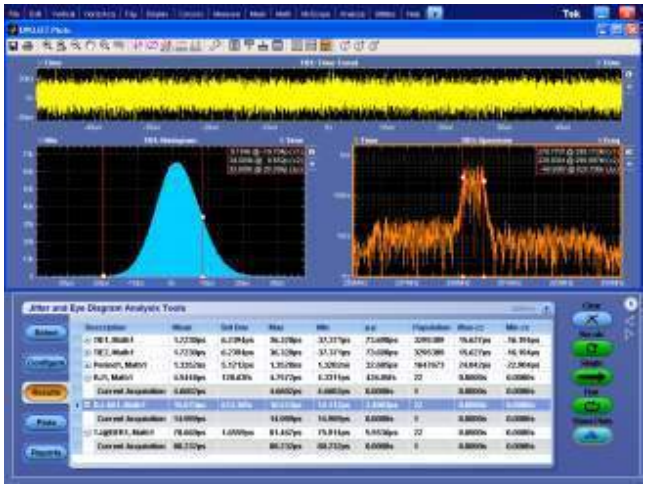
抖动、眼图测量

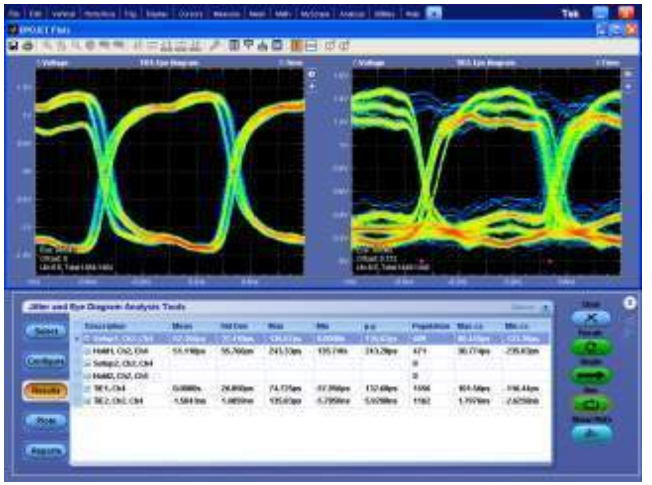
- 抖动/眼图分析
  - 单键向导，简化设置
  - 眼图模板测试
  - 通过/失败测试
  - 随机性/确定性抖动隔离
  - 支持特定标准一致性测试软件包，如DDR和USB



高级DPOJET 抖动、眼图测量软件

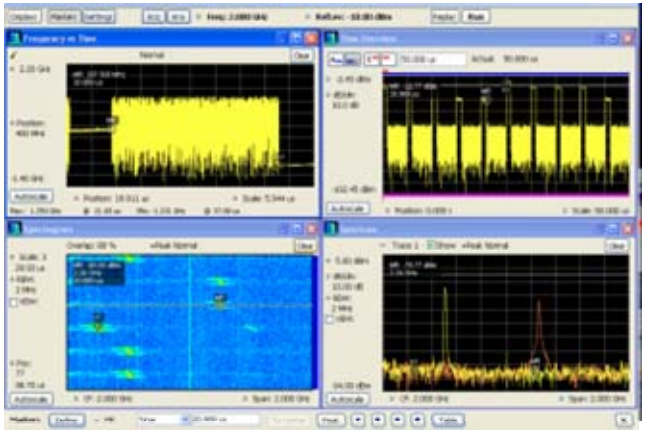
DDR/SDRAM/FLASH内存总线检测调试、频域分析软件

- DDR存储器分析 (选项DDRA)
  - 支持DDR1, DDR2, LPDDR, LPDDR2测试
  - 自动分离读和写
  - 增强DPOJET，提供DDR分析
- 应用
  - 检定DDR存储器总线



DDR内存总线检测与调试

- SignalVuTM，进行RF分析
  - 选项SVE/SVM/SVO/SVP/SVT
  - 分析宽带RF信号
- 应用
  - 宽带RF分析



频域与调制域分析

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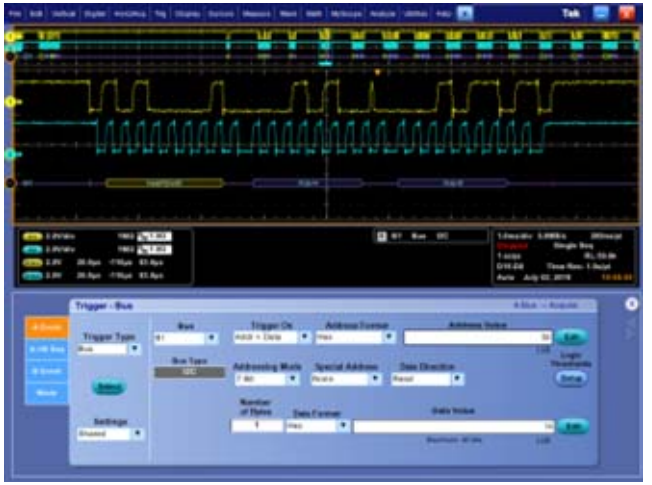
串行总线触发与解码

- 支持常用的行业标准嵌入式串行总线
  - I2C, SPI, RS-232/422/485/UART, USB2.0
  - CAN/LIN
- 在现与总线信号时间对准的总线波形中或在带时间标记的协议事件表中显示解码后的值，总线波在时间上与总线信号
- 在行业标准总线上触发数据包级信息
  - 包头
  - 包尾
  - 数据标ID
  - 地址
  - 数据
- 最高同时对16条总线进行解码



加快串行总线和嵌入式系统调试速度

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第四部分：新的挑战－接收端容限测试

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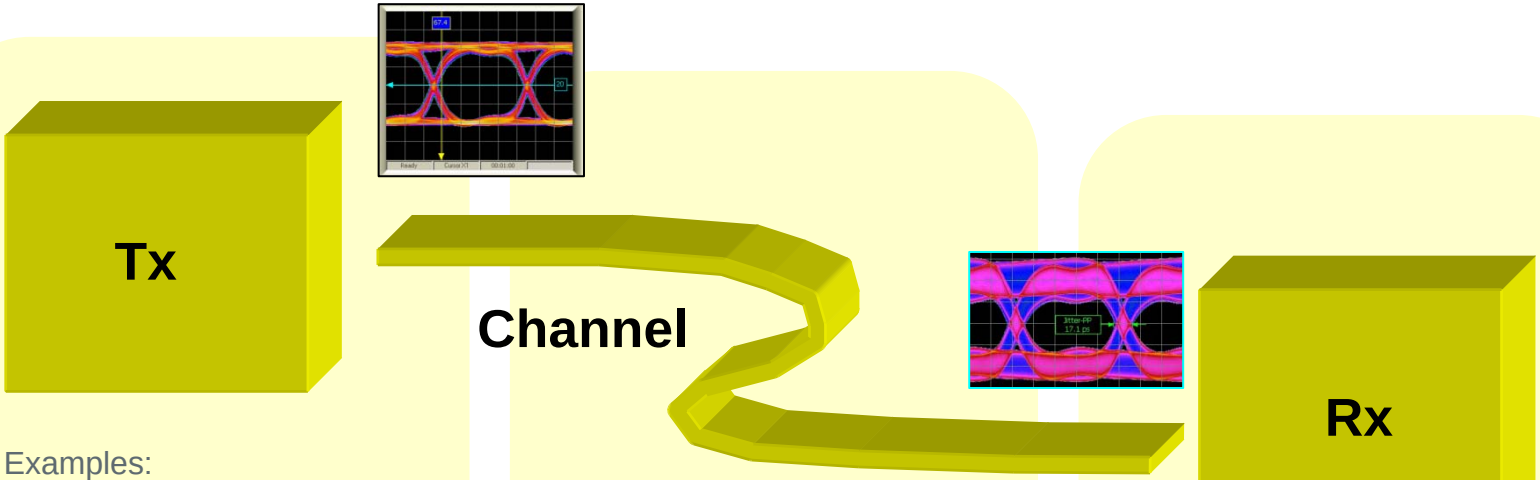
Components of generic communications link



Examples:
- Optical Transceivers (SFP, XFP etc.)
- SERDES chips
- Satellite uplink
- Backplane drivers

Examples:
- Optical Fibre with amplifiers
- High Speed Backplanes
- Circuit Boards
- Coax cables

Examples:
- Optical Transceivers
- SERDES chips
- SERDES

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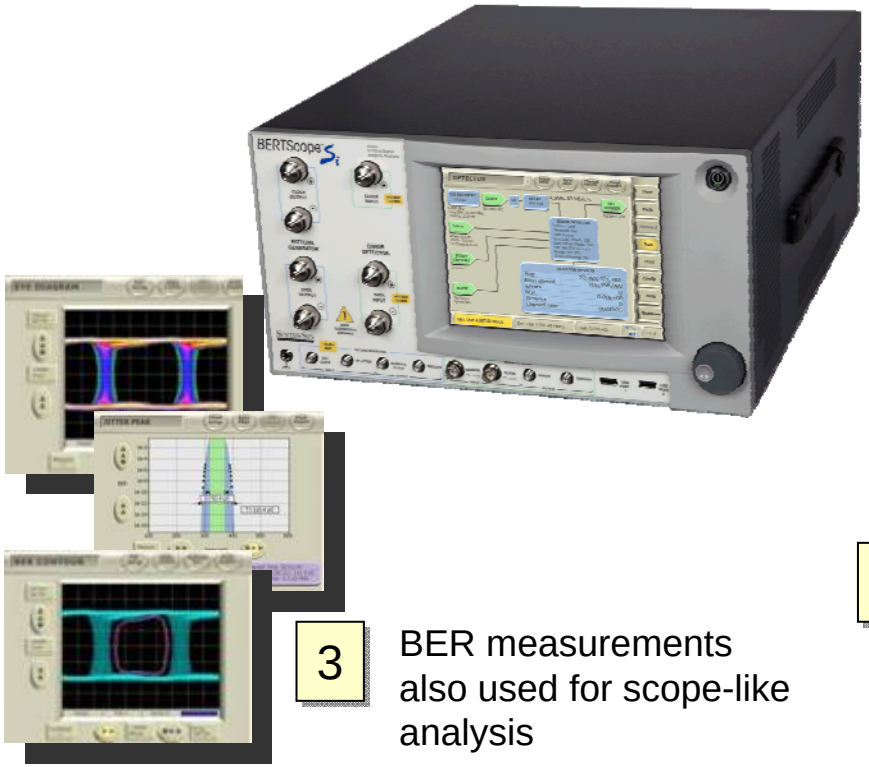
接收端容限测试

A Combination BERT and Scope for Computer Bus and Communications Serial Data Applications

1 Pattern Generator (with optional Stress) sends bits, e.g. a PRBS pattern

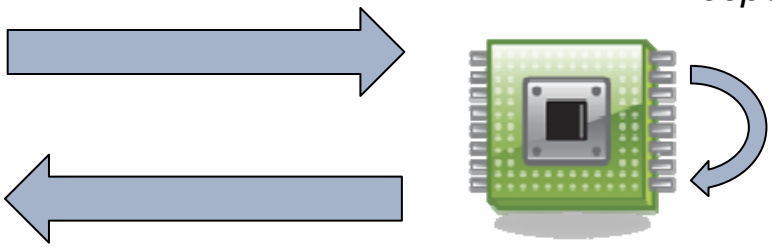


3 BER measurements also used for scope-like analysis

A Typical Receiver Test Setup

From Stressed Pattern Generator

loopback



To Error Detector

Device Under Test (DUT)

2 Bits come back from DUT to Error Detector and compared to expected pattern for Bit Error Ratio (BER) measurement.

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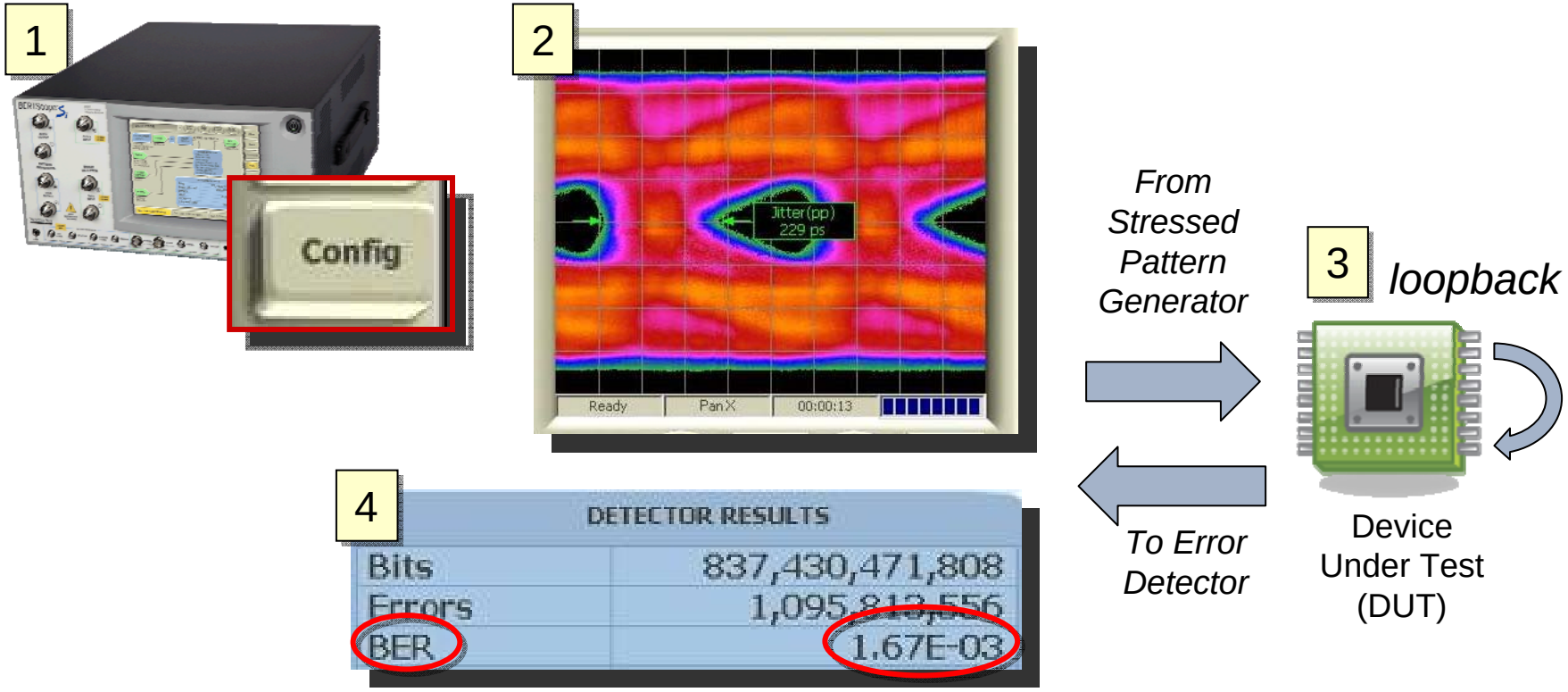
Start Testing Quickly



1. Recall stressed eye configuration
2. Apply stressed eye signal to DUT's receiver
3. DUT loops received bits back to BERTScope Error Detector
4. BERTScope counts any errors

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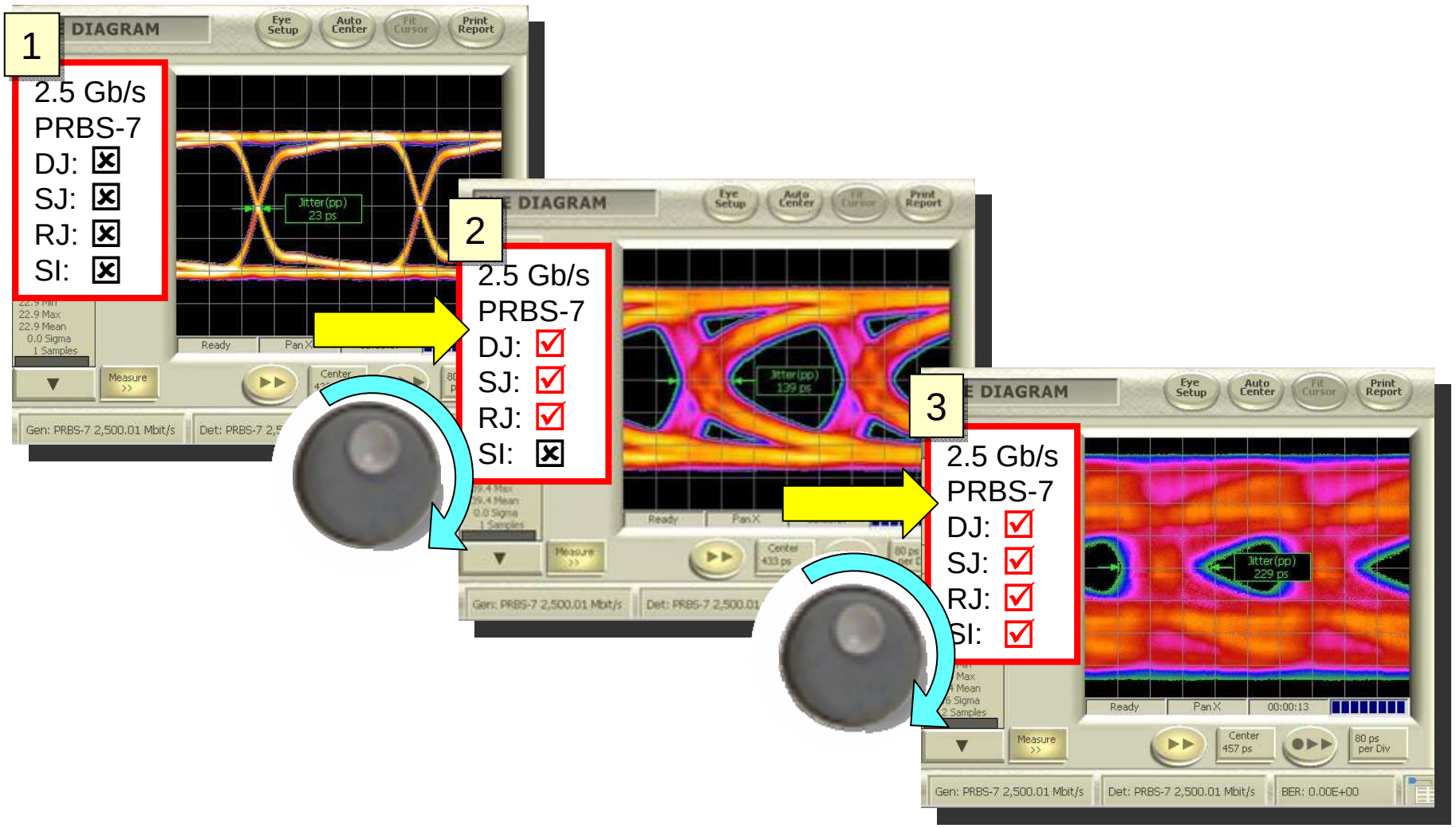
Dynamically change Data Rate, Stress, Pattern



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Which Standards Use Stressed Eye Receiver Jitter Tolerance Testing?

	Sinusoidal Jitter	Random Jitter	Bounded Uncorrelated Jitter (PRBS)	Sinusoidal Interference	Data-Dependent Jitter from ISI	Vertical closure from ISI
SONET/SDH*	✔					
OIF CEI	✔	✔	✔	✔	✔	✔
XFP	✔	✔	(proposed)		✔	✔
1x/2x/4x Fibre Channel	✔	✔	✔		✔	✔
XAUI	✔	✔			✔	✔
10 GbE (4-lane optical, 10 GBase-LX4)	✔	✔			✔	✔
10 GbE (802.3ae) & 10 G Fibre Channel (both Serial)	✔			✔	**	✔
Serial-ATA II	✔	✔		✔	✔	✔

* SONET/SDH also require jitter transfer & jitter generation testing

** Minimal due to use of linear phase filter.

◯ Inferred as component that is part of DJ recipe

Table also available on Anatomy of an Eye Diagram Poster
www.bertscope.com

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总结

- 全新的数字电路调试、测试理念，时域、逻辑域时间相关联合测试
- 创新的仪器实际构架，能够快速发现问题、定位问题，提高调试效率
- 丰富的测量、分析平台
- 丰富完整的工业标准测试
- 完整的测量测试平台，包含各种调试用仪器

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