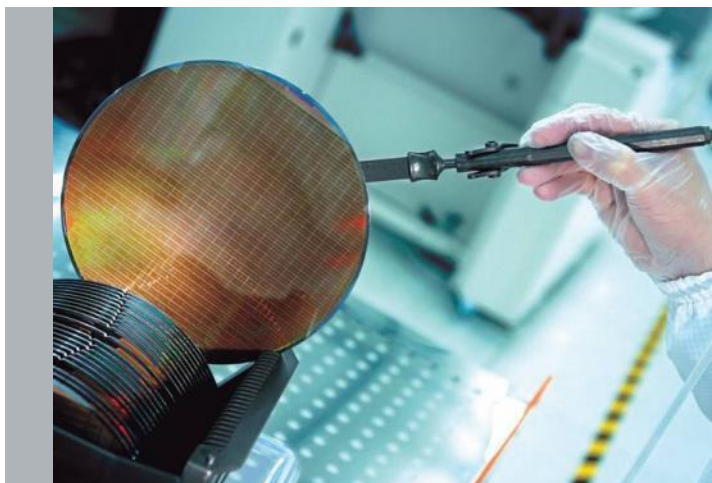


高速串行测试方案介绍

泰克华南区技术支持工程师 余岚



Tektronix[®]

High-Speed Serial Data Test Solutions

Design

Verification

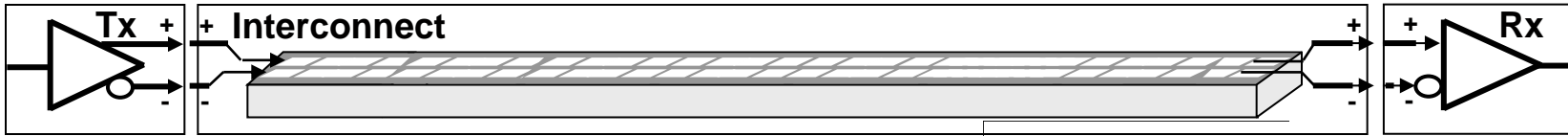
Compliance Test



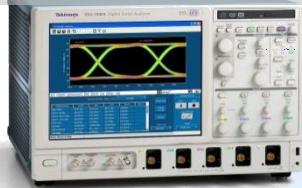
GbE DisplayPort

HDMI™

MHL ...



Real-time Scopes



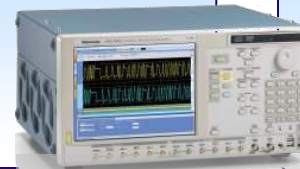
System Integration
Digital Validation & Debug

Logic Analyzers



Transmitter Testing

Receiver Test
Margin
Testing



Arbitrary Waveform Generator

Probing
Fixtures



Interconnect Test

Sampling Scopes

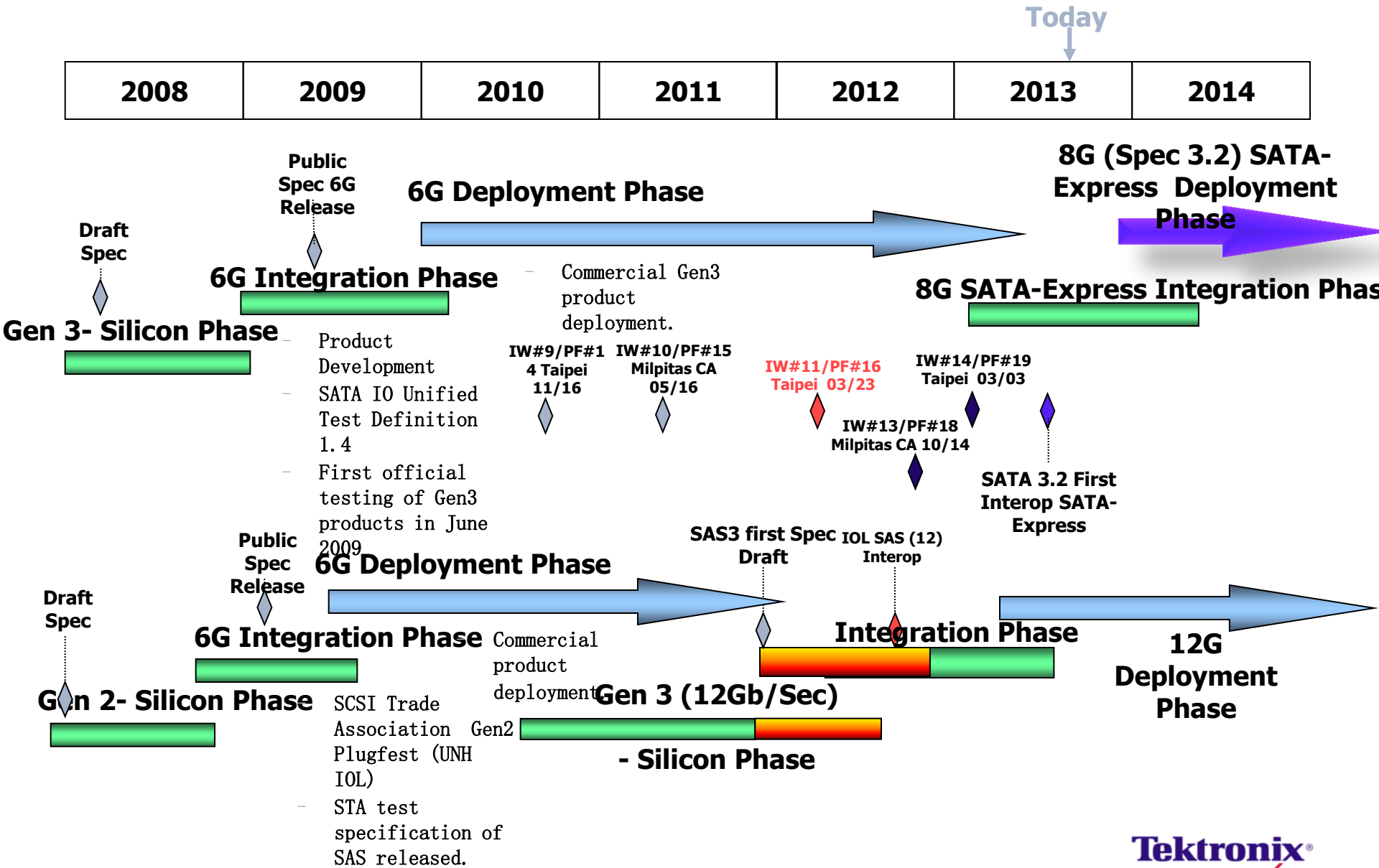


Compliance Test

Compliance Test Software



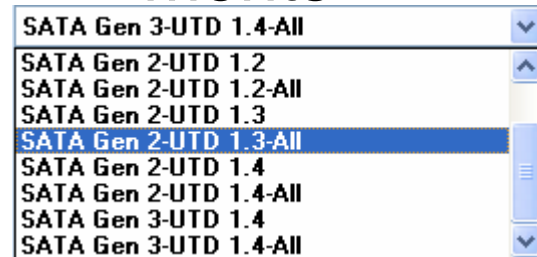
Storage Timelines and Solutions Development



SATA UTD 1.4 TSG/PHY/OOB Measurements

Drive : PHY-TSG-OOB SATA Gen 3-UTD 1.4-All

Select	Test Name
<input checked="" type="checkbox"/>	Informative-df/dt Measurement
<input checked="" type="checkbox"/>	Informative-Eye diagrams
<input checked="" type="checkbox"/>	OOB01-OOB Signal Detection Threshold
<input checked="" type="checkbox"/>	OOB02-UI During OOB Signaling
<input checked="" type="checkbox"/>	OOB03-COMINIT_RESET and COMWAKE Transmit Burst Length
<input checked="" type="checkbox"/>	OOB04-COMINIT_RESET Transmit Gap Length
<input checked="" type="checkbox"/>	OOB05-COMWAKE Transmit Gap Length
<input checked="" type="checkbox"/>	OOB06-COMWAKE Gap Detection Windows
<input checked="" type="checkbox"/>	OOB07-COMINIT Gap Detection Windows
<input checked="" type="checkbox"/>	PHY01-Unit Interval
<input checked="" type="checkbox"/>	PHY02-Frequency Long Term Stability
<input checked="" type="checkbox"/>	PHY03-Spread-Spectrum Modulation Frequency
<input checked="" type="checkbox"/>	PHY04-Spread-Spectrum Modulation Deviation
<input checked="" type="checkbox"/>	TSG01-Differential Output Voltage-Option 1
<input checked="" type="checkbox"/>	TSG01-Differential Output Voltage-Option 2
<input checked="" type="checkbox"/>	TSG02-Rise-Fall Time
<input checked="" type="checkbox"/>	TSG03-Differential Skew
<input checked="" type="checkbox"/>	TSG04-AC Common Mode Voltage
<input checked="" type="checkbox"/>	TSG05-Rise-Fall Imbalance
<input checked="" type="checkbox"/>	TSG06-Amplitude Imbalance
<input checked="" type="checkbox"/>	TSG09-TJ at Connector, Clock to Data, fBAUD-500
<input checked="" type="checkbox"/>	TSG10-DJ at Connector, Clock to Data, fBAUD-500
<input checked="" type="checkbox"/>	TSG11-TJ at Connector, Clock to Data, fBAUD-500
<input checked="" type="checkbox"/>	TSG12-DJ at Connector, Clock to Data, fBAUD-500
<input checked="" type="checkbox"/>	TSG13-Transmit Jitter
<input checked="" type="checkbox"/>	TSG14-TX Maximum Differential Voltage Amplitude
<input checked="" type="checkbox"/>	TSG15-TX Minimum Differential Voltage Amplitude
<input checked="" type="checkbox"/>	TSG16-Tx AC Common Mode Voltage



- Different test program and degrees of regression testing user selectable.
- Debug and diagnostic tools (Informative measurements)
- Updated SATA Gen3 measurements
 - **New OOB patterns**
 - TSG ECN additions

SATA/SAS TSB/PHY/OOB



Select Standard	Select Device	Select Test Suite	Version
<input type="radio"/> Serial ATA	<input checked="" type="radio"/> Drive	<input checked="" type="radio"/> PHY-TSG-00B	SAS 2.0
<input checked="" type="radio"/> SAS		<input type="radio"/> Rx-Tx	

Drive : PHY-TSG-00B SAS 2.0

Select	Test Name
<input checked="" type="checkbox"/>	Test 5.2.4 - TX SSC DFDT (Informative)
<input checked="" type="checkbox"/>	Test 5.3.1 - TX Physical Link Rate Long Term Stability
<input checked="" type="checkbox"/>	Test 5.3.2 - TX Common Mode RMS Voltage Limit
<input checked="" type="checkbox"/>	Test 5.3.3 - TX Common Mode Spectrum
<input checked="" type="checkbox"/>	Test 5.3.4 - TX Peak-to-Peak Voltage
<input type="checkbox"/>	Test 5.3.5 - TX VMA and EQ
<input checked="" type="checkbox"/>	Test 5.3.6 - TX Rise and Fall Times
<input checked="" type="checkbox"/>	Test 5.3.7 - TX Random Jitter (RJ)
<input checked="" type="checkbox"/>	Test 5.3.8 - TX Total Jitter (TJ)
<input checked="" type="checkbox"/>	Test 5.3.9 - TX Waveform Distortion Penalty (WDP)

Configure

Show MOI

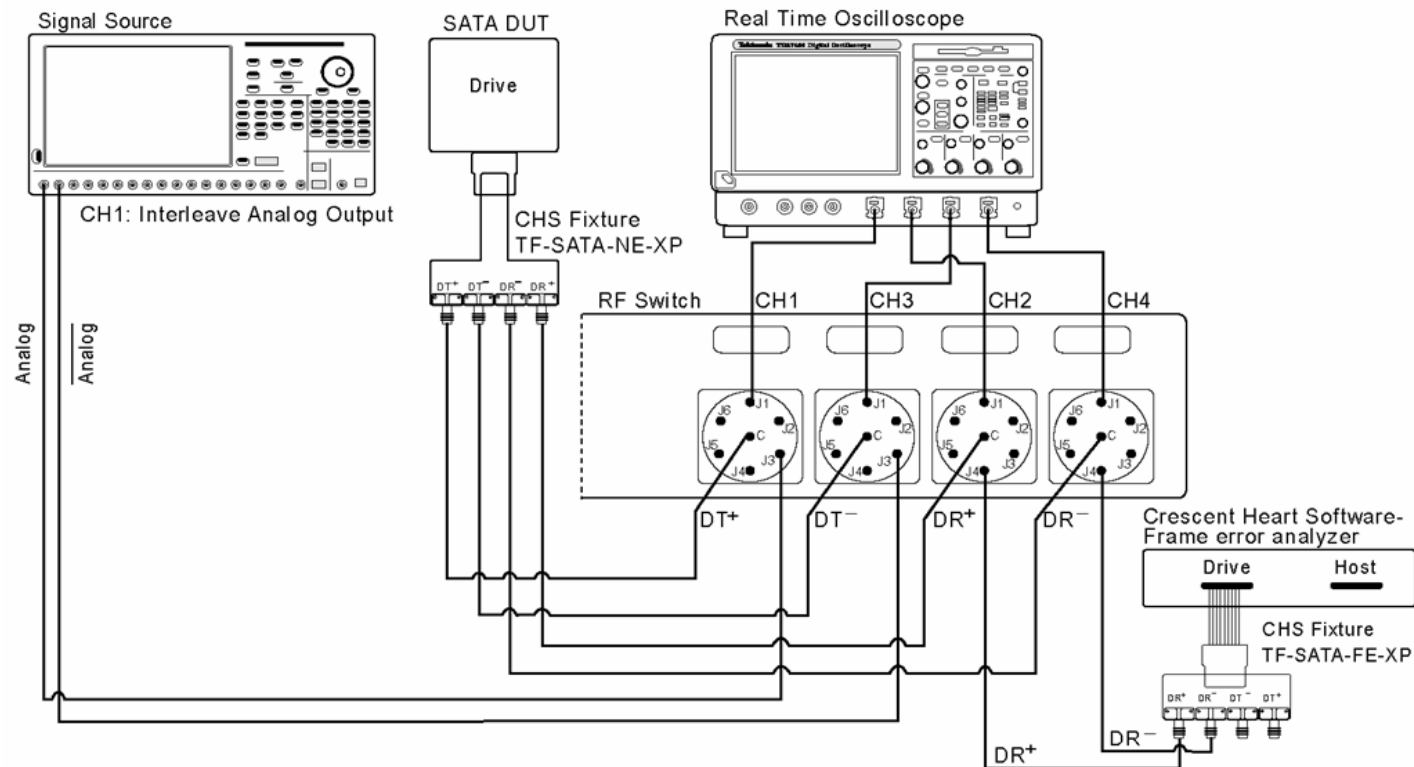
Show Schematic

Select All

Select Required

Deselect All

SATA/SAS TSG/PHY/OOB test connection

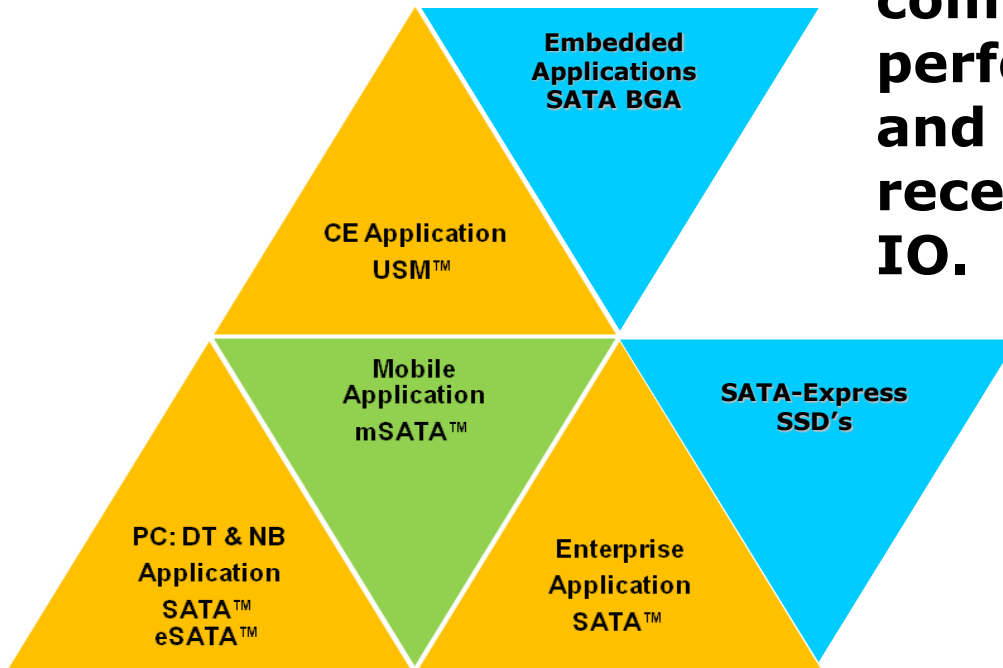


SATA/SAS: test Report

Test Name	Test Details			Low Limit	Measured Value	High Limit	Margin	Units	Test Result
	Pattern Name	Interface Speed	Measurement Details						
Test 5.2.1-TX SSC Modulation Type	HFTP	6.0Gb/s	Center-spread SAS	-NA-	SSC ON	-NA-	-NA-	-NA-	Pass
Test 5.2.2-TX SSC Modulation Frequency	HFTP	6.0Gb/s	SSC Modulation Frequency	>= 30	30.0000	<= 33	0 , 3	KHz	Pass
	HFTP	6.0Gb/s	Min SSC Modulation Frequency	>= 30	29.9992	<= 33	Informative		Informative
	HFTP	6.0Gb/s	Max SSC Modulation Frequency	>= 30	30.0011	<= 33	Informative		Informative
Test 5.2.3-TX SSC Modulation Deviation and Balance	HFTP	6.0Gb/s	Max Deviation	-NA-	-2199.6500	-NA-	-NA-	ppm	Informative
	HFTP	6.0Gb/s	Min Deviation	-NA-	2200.0074	-NA-	-NA-		Informative
	HFTP	6.0Gb/s	Avg Deviation	>= -350	0.1787	<= 350	350.1787, 349.8213		Pass
	HFTP	6.0Gb/s	Deviation asymmetry	-	0.3574	<= 288	287.6426		Pass
Test 5.2.4-TX SSC DFDT (Informative)	HFTP	6.0Gb/s	df/dt	>= -850	-380.3082	<= 850	Informative	ppm/us	Informative
Test 5.3.1-TX Physical Link Rate Long Term Stability	HFTP	6.0Gb/s	Mean Period	> -100	-2.1050	< 100	Informative	ppm	Informative
	HFTP	6.0Gb/s	Min Period	> -100	2200.0074	< 100	Informative		Informative
	HFTP	6.0Gb/s	Max Period	> -100	-2199.6501	< 100	Informative		Informative
Test 5.3.2-TX Common Mode RMS Voltage Limit	CJTPat-Gen 2	6.0Gb/s	Common-mode RMS voltage at IT (mV)-SAS 2.0	-	42.9927	< 30	12.9927	mV	Fail
Test 5.3.3-TX Common Mode Spectrum	CJTPat-Gen 2	6.0Gb/s	Common-mode spectrum (dBmV) at 100MHz-SAS 2.0	-	-33.5589	< 12.7	46.2589	mV	Pass
	CJTPat-Gen 2	6.0Gb/s	Common-mode spectrum (dBmV) at first harmonic-SAS 2.0	-	16.7701	< 26	9.2299		Pass
	CJTPat-Gen 2	6.0Gb/s	Common-mode spectrum (dBmV) at second harmonic-SAS 2.0	-	-9.8586	< 30	39.8586		Pass
Test 5.3.4-TX Peak-to-Peak Voltage	D30.3-Gen 2	6.0Gb/s	Peak to Peak voltage (mVppd)-SAS 2.0	> 850	1240.0000	< 1200	390 , 40	mV	Fail
Test 5.3.5-TX VMA and EQ	D30.3-Gen 2	6.0Gb/s	Transmitter equalization (dB)-SAS 2.0	> 2	2.0684	< 4	Informative	dB	Pass
Test 5.3.6-TX Rise and Fall Times	D10.2	6.0 Gb/s	Rise time in ps	>= 41.6	55.7616	-	14.1616	ps	Pass
	D10.2	6.0 Gb/s	Fall time in ps	>= 41.6	55.3999	-	13.7999		Pass
Test 5.3.7-TX Random Jitter (RJ)	D24.3-Gen 2	6.0Gb/s	Rj before CIC	-	0.7069	<= 25	24.2931	ps	Pass
	D24.3-Gen 2	6.0Gb/s	Rj after CIC	-	0.5321	<= 25	24.4679		Pass

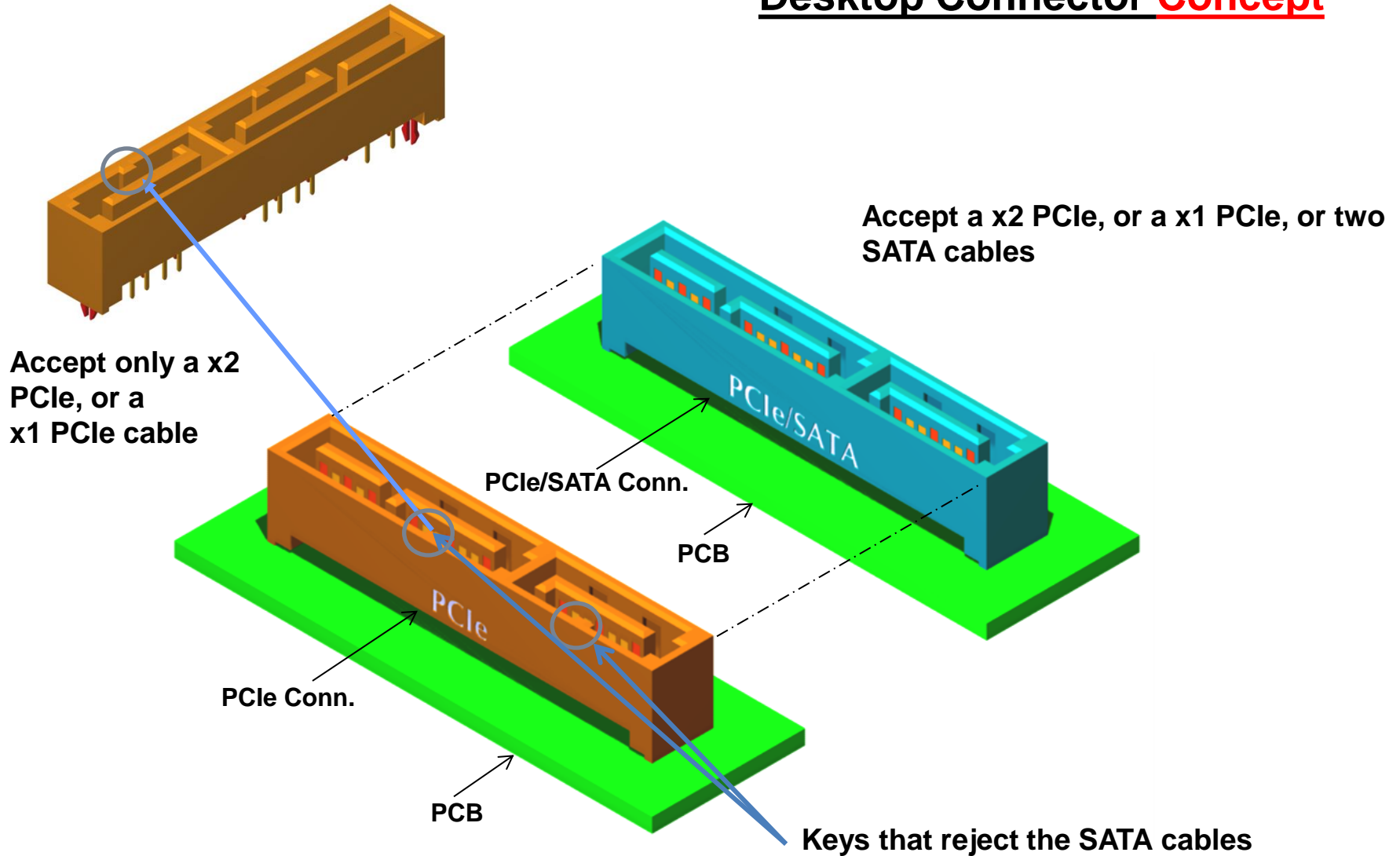
The SATA Ecosystem: Now

Today, SATA is expanding in specialized low power, compact and high performance areas with BGA and SATA-Express Solutions recently approved by SATA-IO.

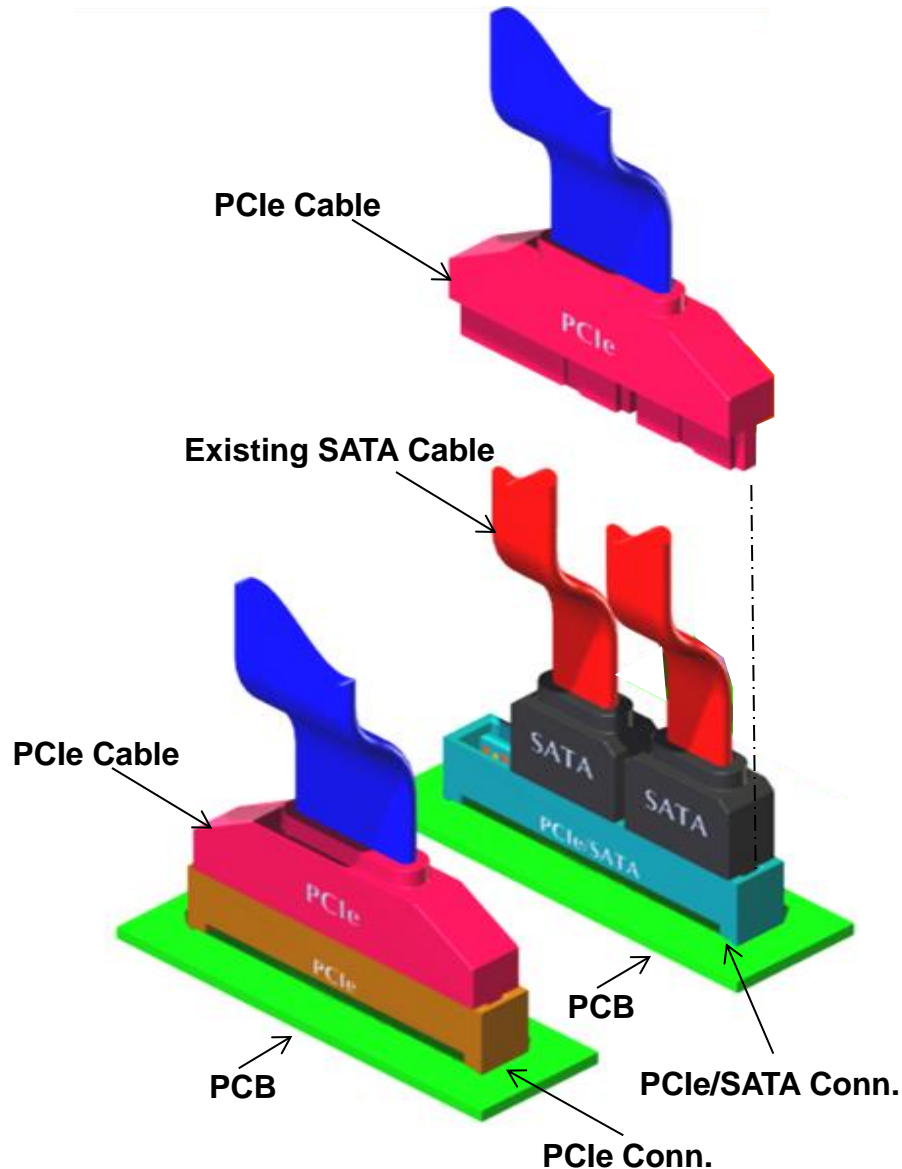


Enabling the New SATA Express Ecosystem

Desktop Connector Concept



Enabling the New SATA Express Ecosystem



Desktop Cables **Concept**

- SATA devices will coexist with next generation PCIe devices
- SATA cost/performance benefits
- Requires a connector that supports both PCIe and SATA
 - Allows a single motherboard (backplane) connector to support both interfaces
- HDD-compatible form factors to be defined for PCIe devices
 - Enables system-level mechanical compatibility
 - Preserves high-capacity storage

SATA-IO CabCon has been chartered to develop SATA compatible connectors and form factors for PCIe SSD/hybrid drives

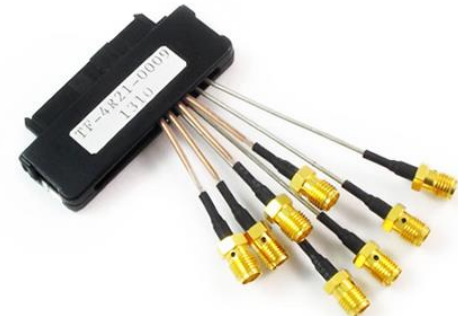
SATA Express Signal Access

- Recommend Luxshare-ICT Dual Port SAS fixtures (SFF-8482)
- Similar dimensions but different pinout
- For device testing use plug fixture (TF-4R21) to mate with SATAe plug
 - Both ports accessible (29 pin)
- For cable testing use receptacle fixture (TF-4P22) to mate with SATAe receptacle
 - Only port A is accessible (22 pin)

SAS Dual Port Plug Test Fixture



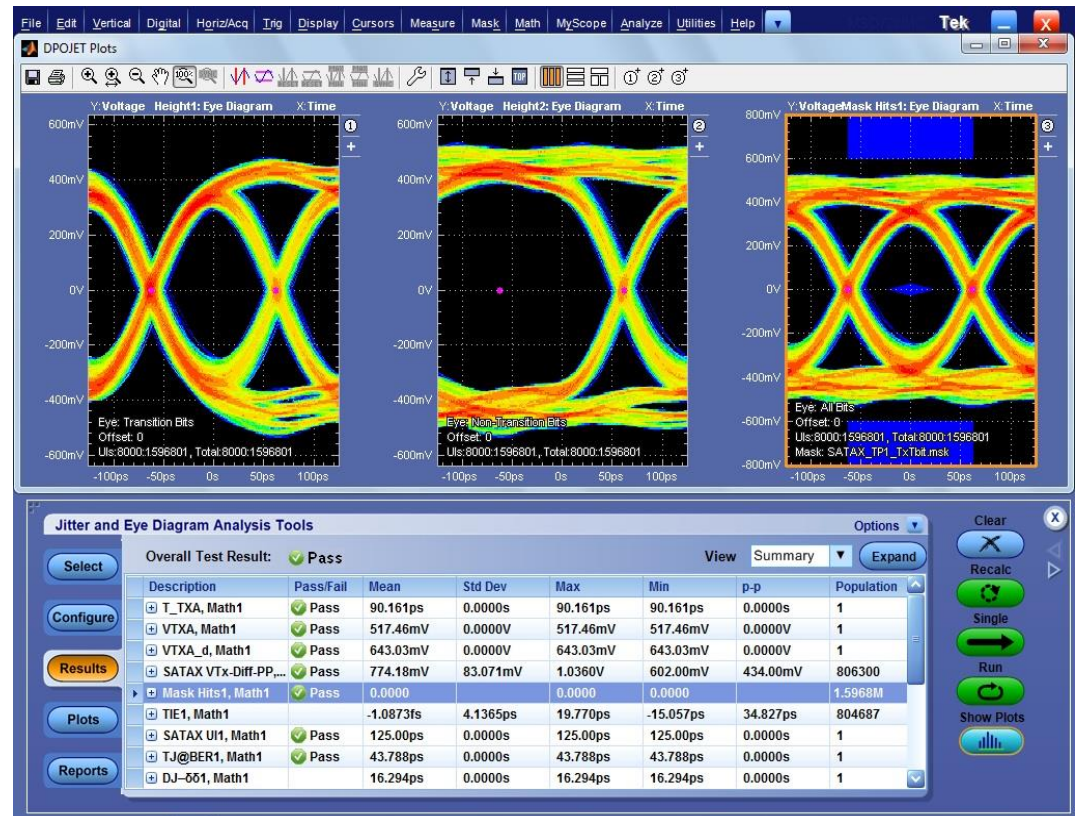
SAS Dual Port Receptacle Test Fixture



<http://www.luxshare-ict.com/>

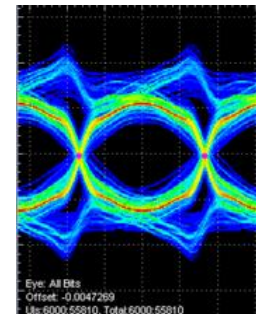
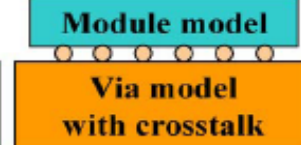
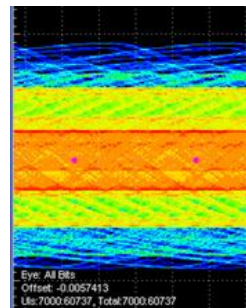
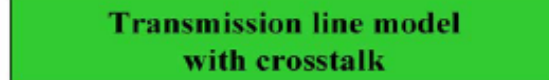
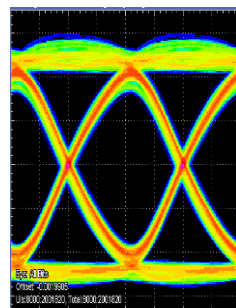
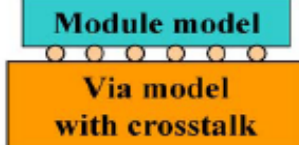
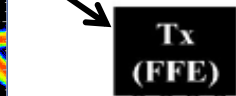
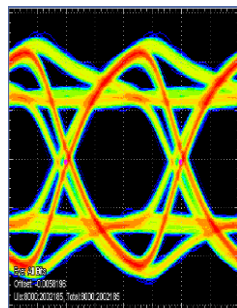
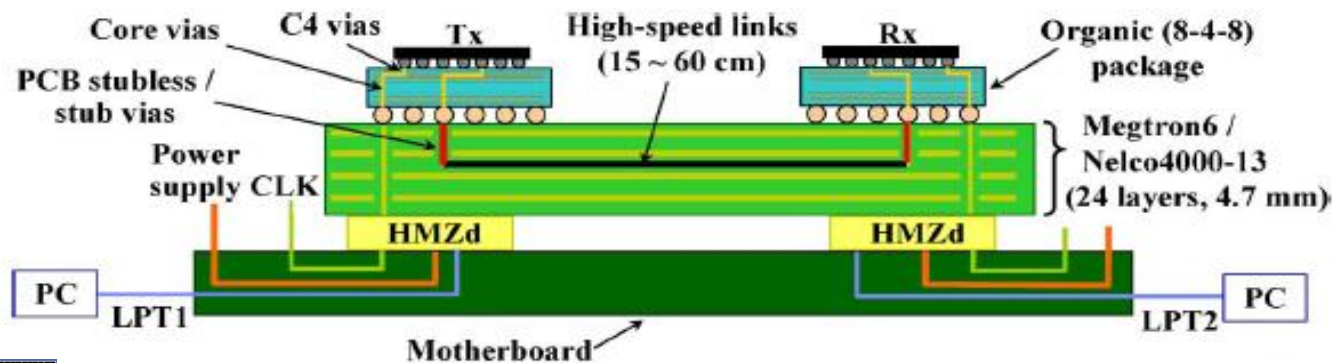
Tektronix Solutions for SATA Express Measurements

- DPOJET-based SATA Express setup (requires option PCE3)
- Support for Base/CEM spec measurements
- Supports all versions of PCI Express and includes SATA Express PLL configurations



12G+ Design Problem: 1000mV, FFE, Crosstalk, DFE, 50mV

- Crosstalk and signal loss problems are the largest design challenge today.
- Significant advances in high tap count Decision Feedback Equalization are key to operating at 12G+.



SAS-3 PHY Transmitter Solution

Group 1 – OOB Signaling

- 5.1.1 Maximum Noise During OOB Idle
- 5.1.2 OOB Burst Amplitude
- 5.1.3 OOB Offset Delta
- 5.1.4 OOB Common Mode Delta

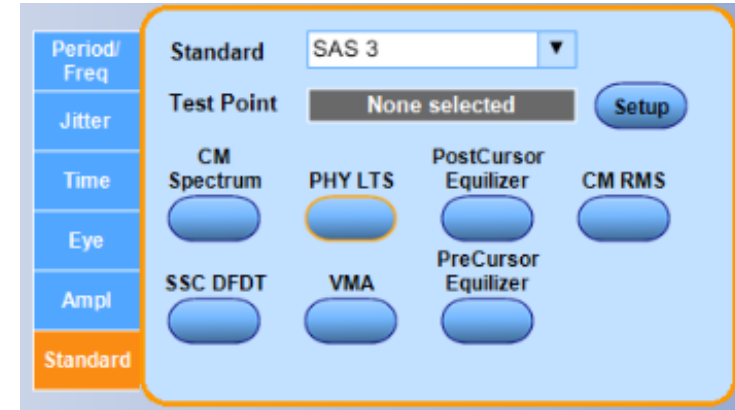
Group 2 – Spread Spectrum Clocking (SSC) Requirements

- 5.2.1 SSC Modulation Type
- 5.2.2 SSC Modulation Frequency
- 5.2.3 SSC Modulation Deviation
- 5.2.4 SSC Balance
- 5.2.5 SSC DFDT

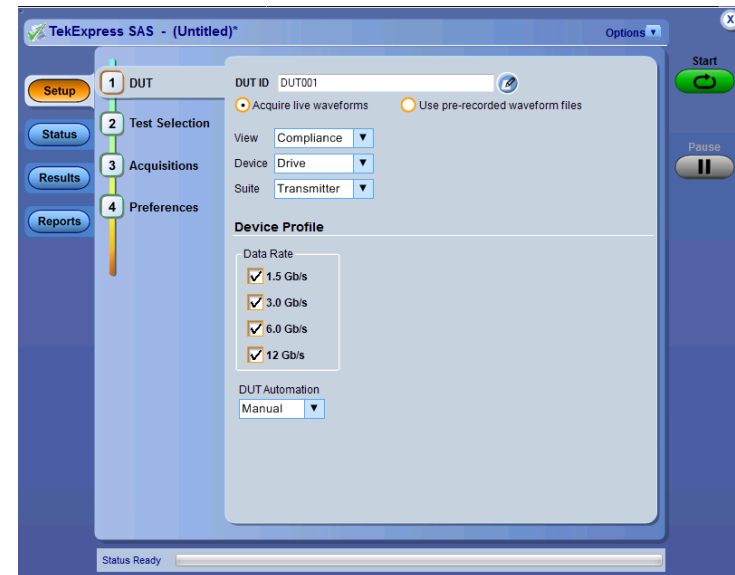
Group 3 – NRZ Data Signaling Requirements

- 5.3.1 Physical Link Rate Long Term Stability
- 5.3.2 Common Mode RMS Voltage Limit
- 5.3.3 Common Mode Spectrum
- 5.3.4 Peak to Peak Voltage
- 5.3.5 Voltage Modulation Amplitude (VMA)
- 5.3.6 Equalization
- 5.3.7 Rise Time
- 5.3.8 Fall Time
- 5.3.9 Random Jitter (RJ)
- 5.3.10 Total Jitter (TJ)
- 5.3.11 Waveform Distortion Penalty (WDP)
- 5.3.12 SAS3_EYEOPENING
- 5.3.13 Pre Cursor Equalization Ratio
- 5.3.14 Post Cursor Equalization Ratio
- 5.3.15 Transition Bit Voltage PK-PK (VHL)
- 5.3.16 Unit Interval

SAS-3 1.5/3/6/12 Gb/s Tx Test Software



TekExpress SAS3-TSG Automation Software



NEW Measurement for Crosstalk/ISI Evaluation

- SAS3_EYEOPENING* Measurement for accurate analysis of ISI and crosstalk effects
- Provides measure of relative vertical eye opening after reference equalization

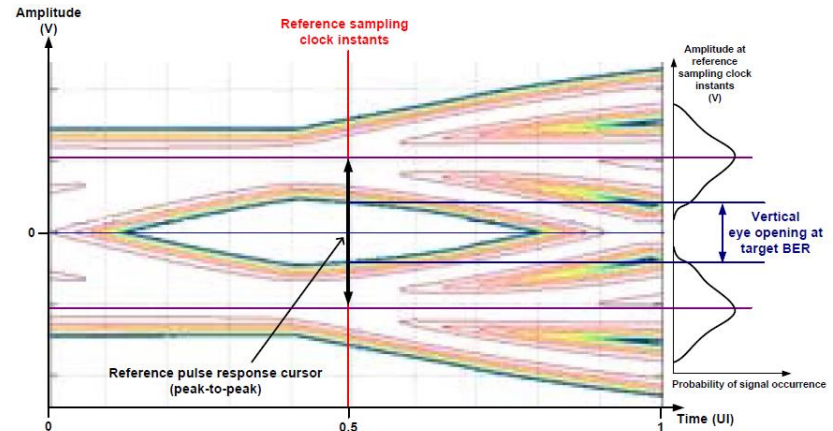
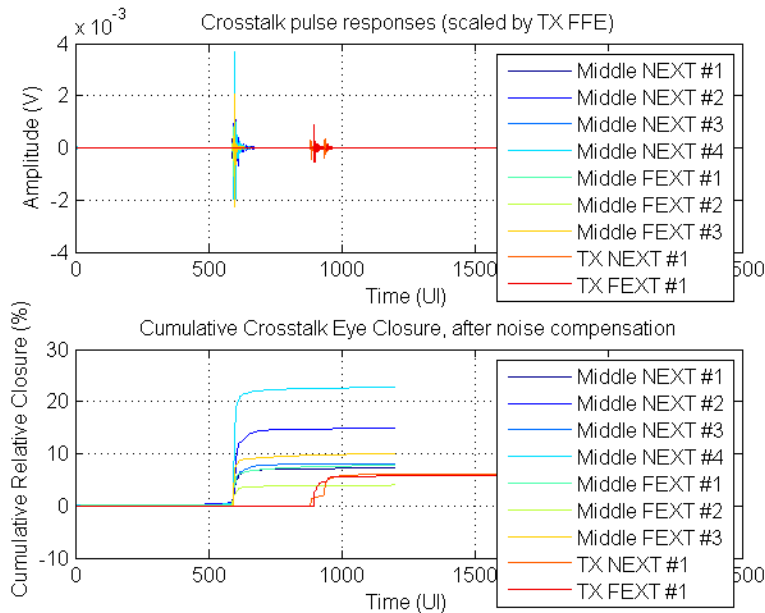
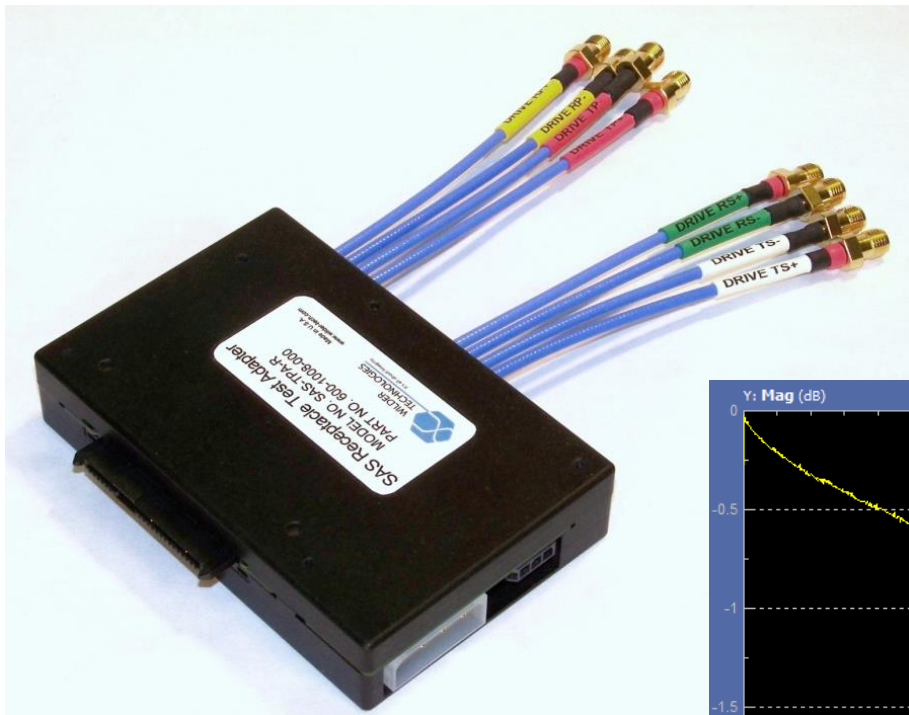


Figure Fe – Simulated Vertical eye opening and reference pulse response cursor

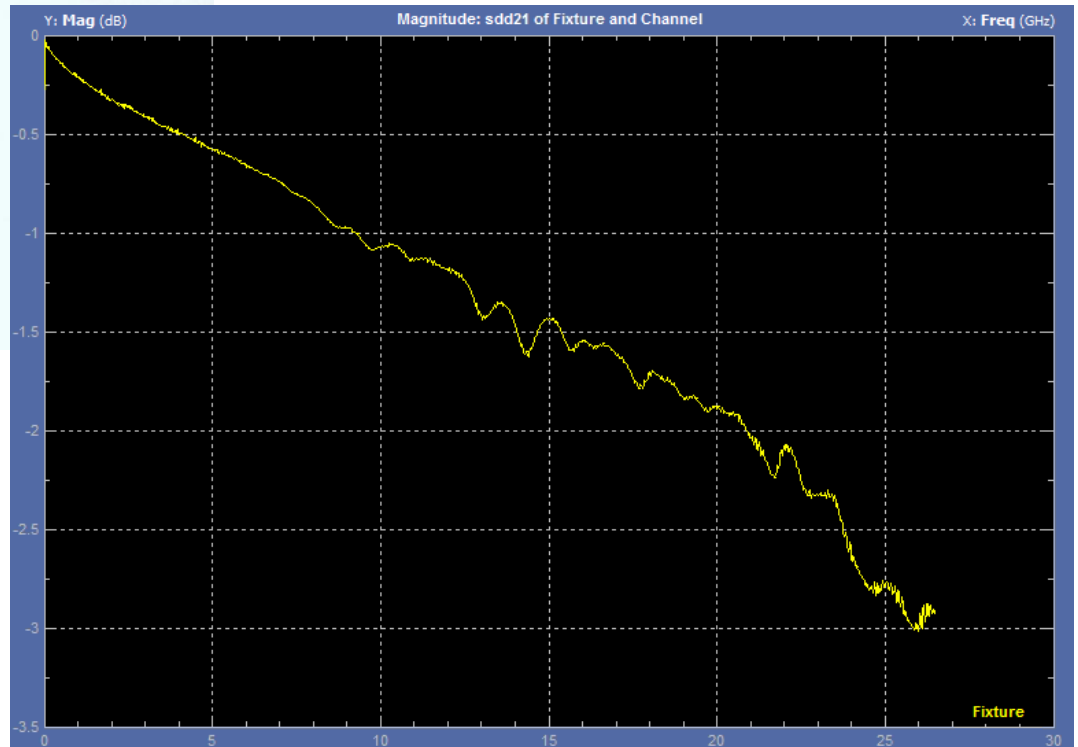
Source: 12-244r3

*Note, this measurement is similar to the SAS-2 Waveform Distortion Penalty (WDP) measurement but also includes Tx EQ in addition to DFE. The code was provided and distributed through the T10 Technical Committee and permission has been granted for Tektronix to reuse.

SAS Receptacle Test Adapter

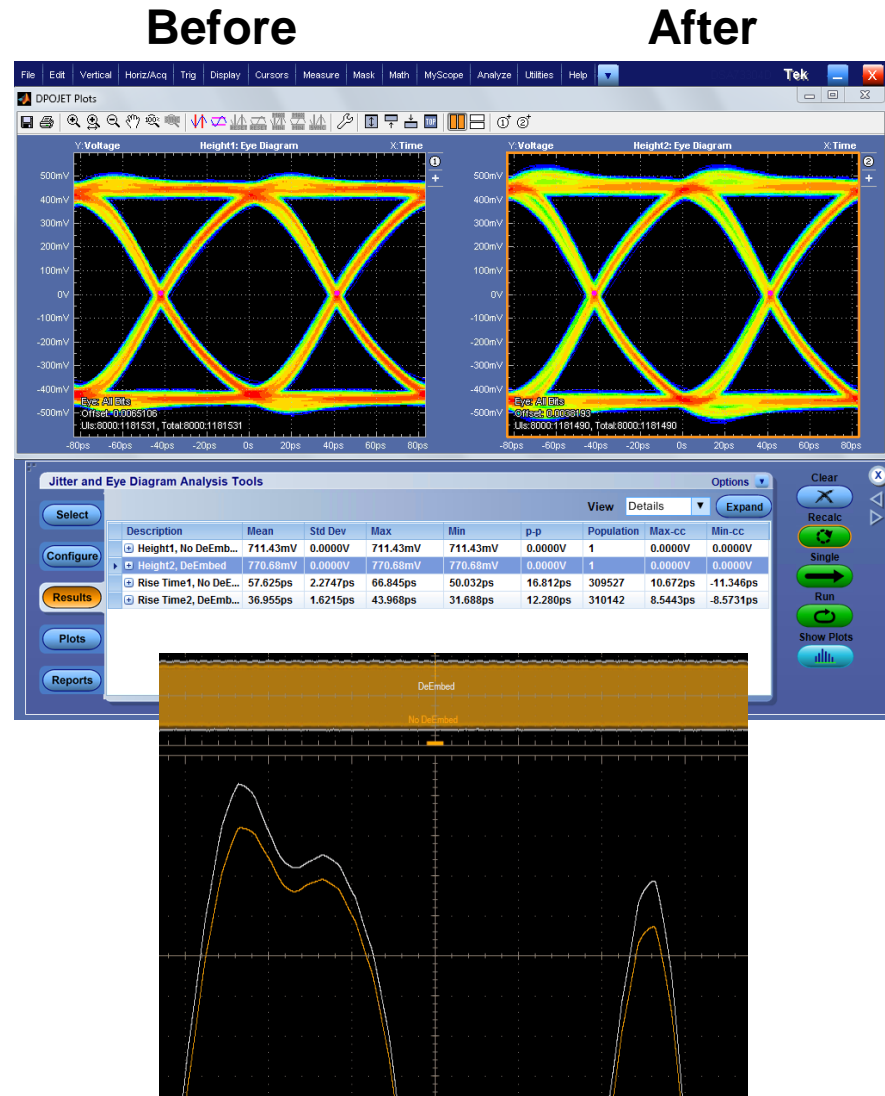


Sdd21 (1x Thru) => -3dB @26 GHz



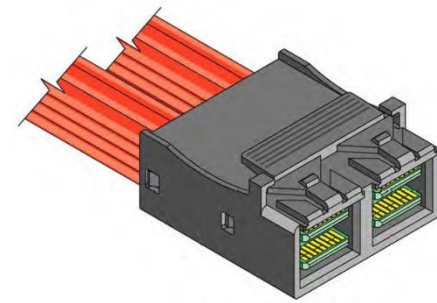
Test Fixture De-embedding

- Why de-embed?
 - Tx measurements referenced to die (ET)
 - Improve margin with removal of fixture effects
- S-Parameters acquired from calibration fixture or model extraction
- Use inverse response to compensate for loss

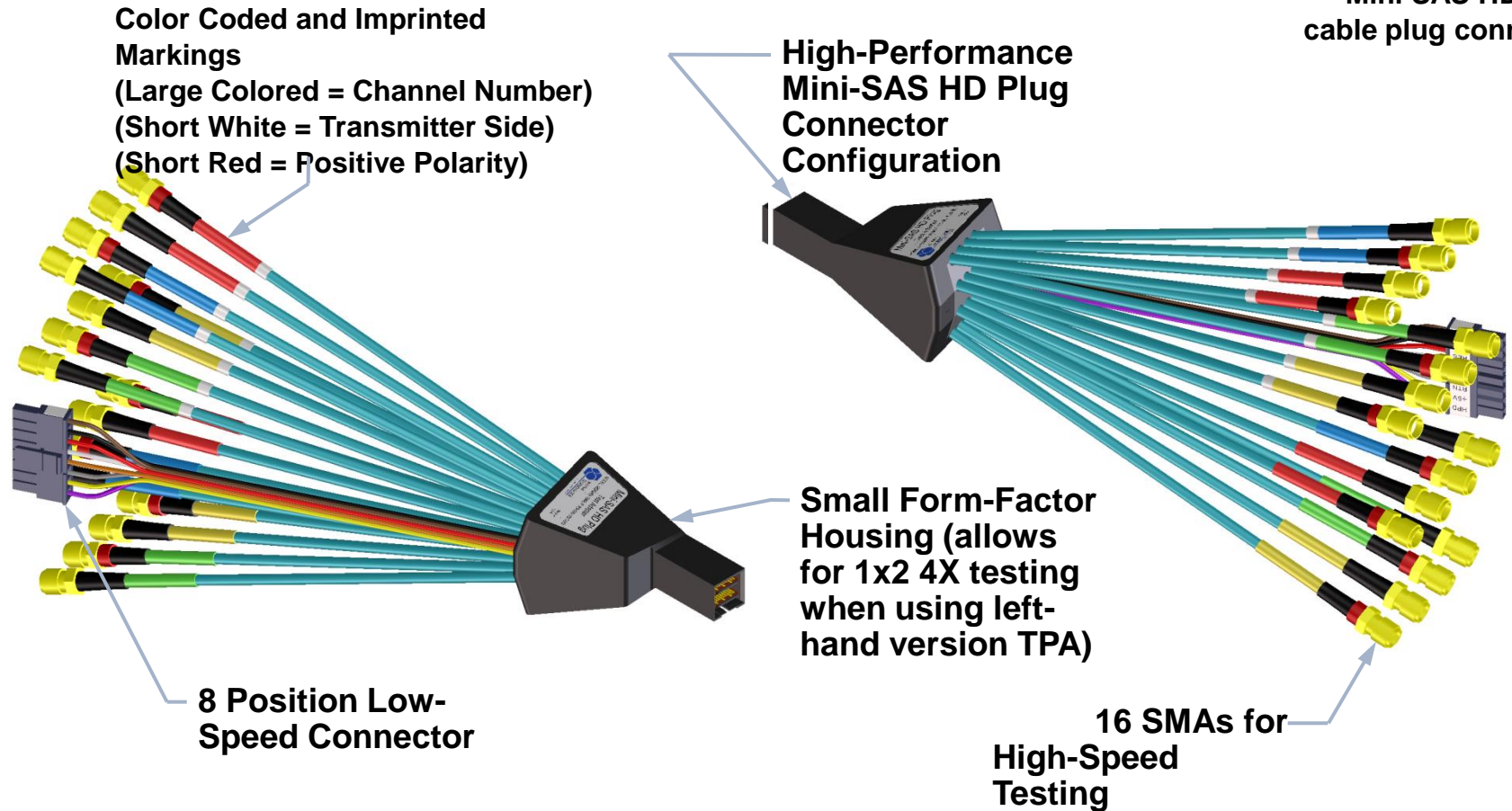


	Before De-Embed	After De-Embed
Eye Height	711 mV	770 mV
Rise Time	57	37

Mini-SAS HD Plug Test Adapters



Mini SAS HD 8i
cable plug connector



Color Coded and Imprinted
Markings
(Large Colored = Channel Number)
(Short White = Transmitter Side)
(Short Red = Positive Polarity)

High-Performance
Mini-SAS HD Plug
Connector
Configuration

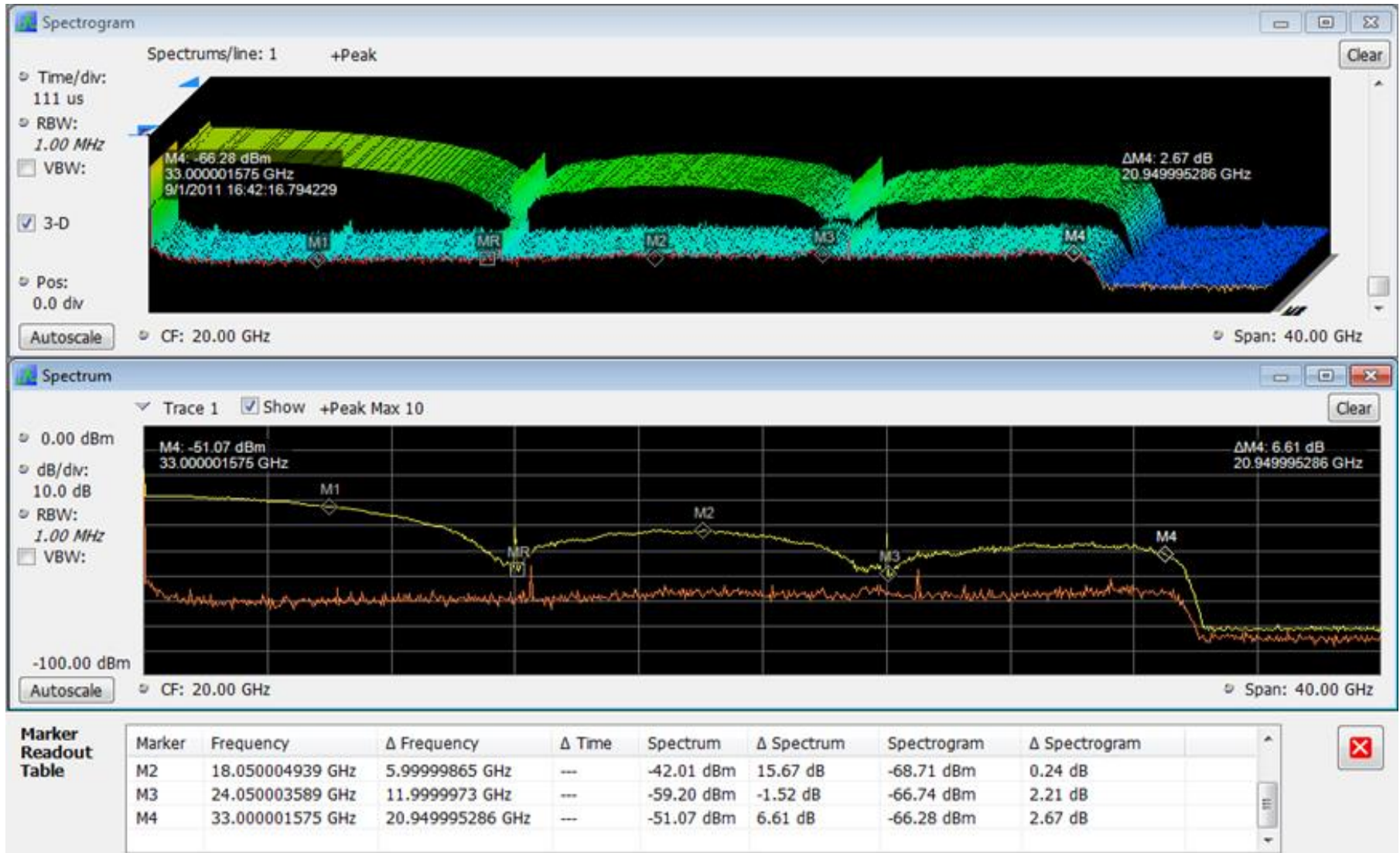
Small Form-Factor
Housing (allows
for 1x2 4X testing
when using left-
hand version TPA)

8 Position Low-
Speed Connector

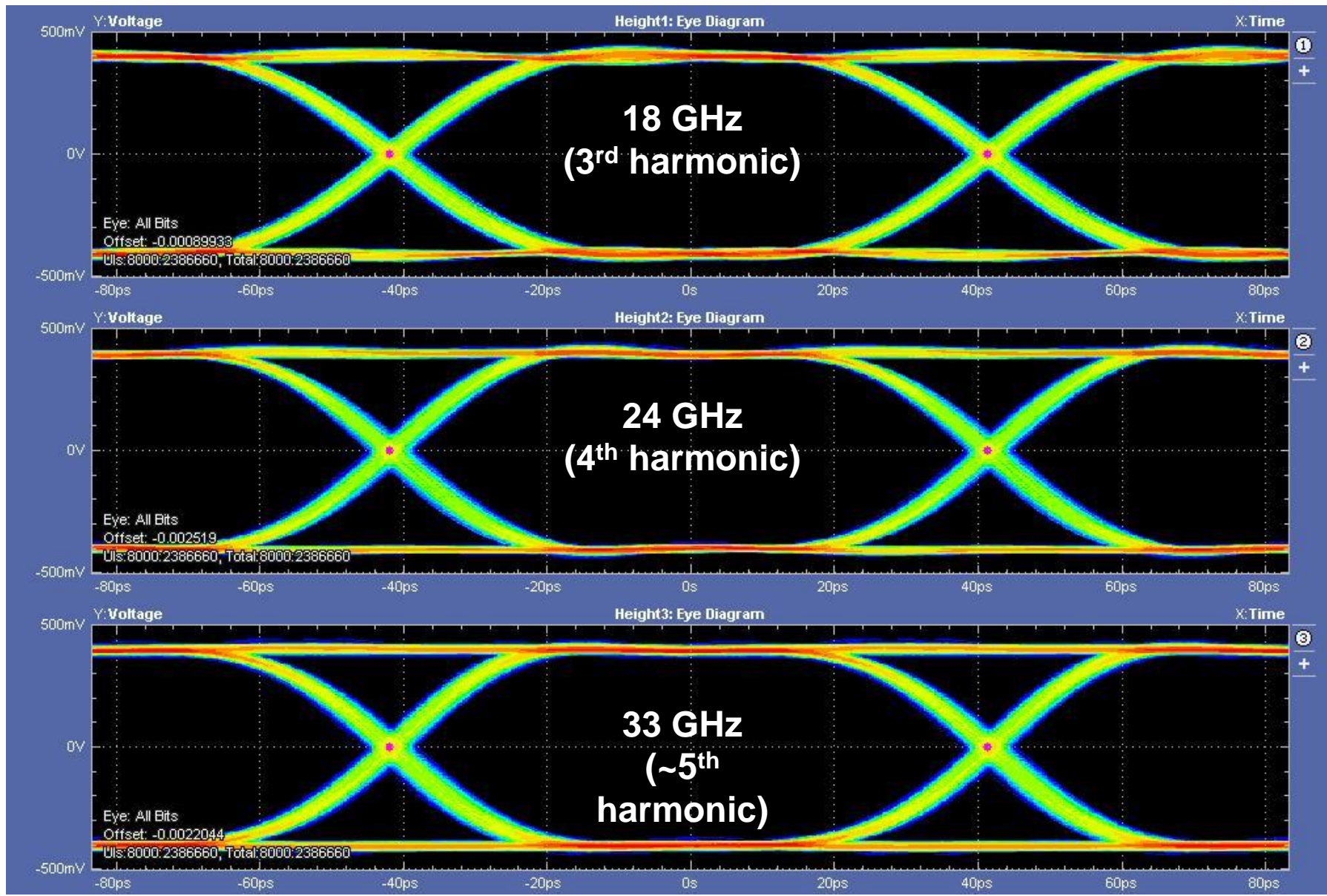
16 SMAs for
High-Speed
Testing

Bandwidth Considerations

SAS 12G NRZ Power Spectrum



12G PRBS from BERT (20ps 20-80% Tr)



Recommended Equipment

The following components are required for performing SAS12 Tx measurements

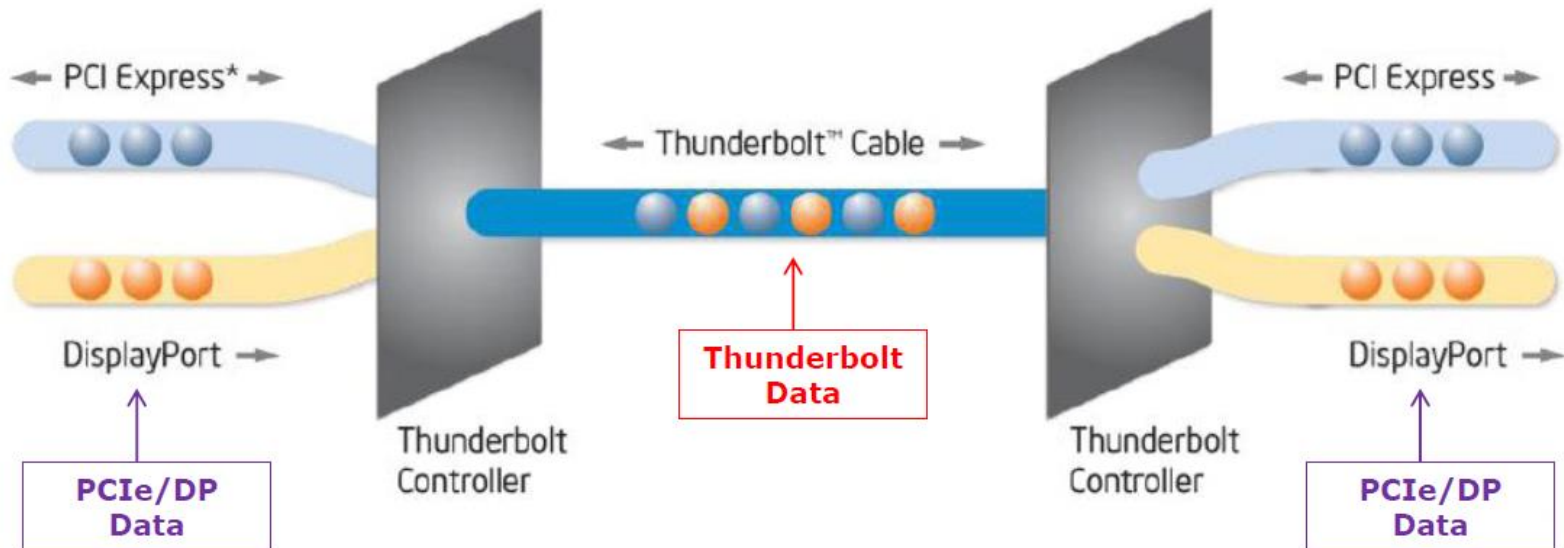
- DPO/MSO70K(C/D) Series Oscilloscope with Opt. 2XL or higher
 - 12.5 GHz or higher recommended for 1.5, 3, or 6 Gb/s
 - 20 GHz or higher recommended for 12 Gb/s
- DPOJET Advanced (DJA) - Prerequisite
- Option SAS3-TSG & SAS3-TSGW (required for WDP measurements)
- Test Fixtures:
 - TF-SAS-TPA-R SAS Gen3 Receptacle Adapter (drive form factor) or
 - TF-SASHD-TPA-R miniSASHD 12G SAS Receptacle (mini SAS HD 4i/x cables) or
 - Set of TF-SASHD-TPAR-P miniSASHD 12G SAS (Right Side) Plug and TF-SASHD-TPAL-P miniSASHD 12G SAS (Left Side) Plug (x8)
- PMCABLE1M or equivalent Phase Matched Cable Set (qty: 2)

Thunderbolt Overview

- High Speed Data Bus for PC's
 - Brought to market by Intel/Apple in 2011
 - Interoperable with DisplayPort
- Thunderbolt signaling is dual NRZ (64/66b Encoded)
 - 10.3125 Gb/s data rate
 - It utilizes SFP+ technology with 2 diff Tx and Rx pairs.



Thunderbolt

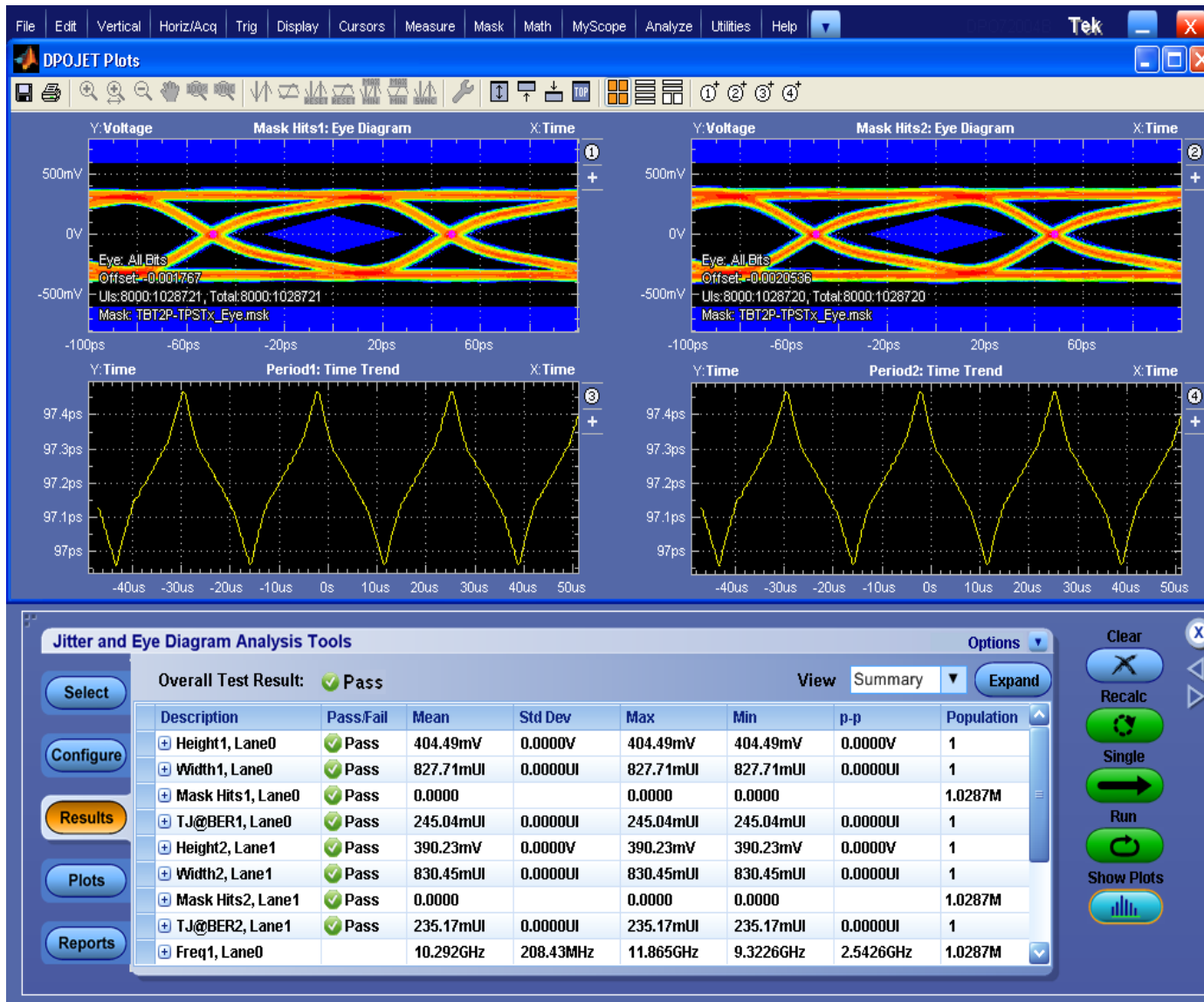


Thunderbolt Transmitter Test Overview

- All measurements are near end with Fixtures fully de-embed.
- Requires DisplayPort 1.2 conformance testing
- **Source Test Suite**
 - PHY1.1 – Transition Timing
 - PHY1.2 – Intra-Pair Skew
 - PHY1.3 – AC Common Mode RMS
 - PHY1.4 – AC Common Mode Peak
 - PHY1.5 – Eye Height
 - PHY1.6 – Eye Width
 - PHY1.7 – Max Differential Voltage
 - PHY1.8 – Total Jitter at 10-12 BER
 - PHY1.9 – Unit Interval
 - PHY1.10 – SSC Modulation Frequency
- **DUT Configuration**
 - 1. **Bit Rates: (DP1.2) + 10.3125Gb/sec**
 - 2. **Patterns: 8 1's8 0's, PRBS-9, PRBS-11 and PRBS-31**
 - 3. **SSC (Spread Spectrum): On/Off**

Thunderbolt Transmitter Testing

Fully supported in Tektronix's current solutions



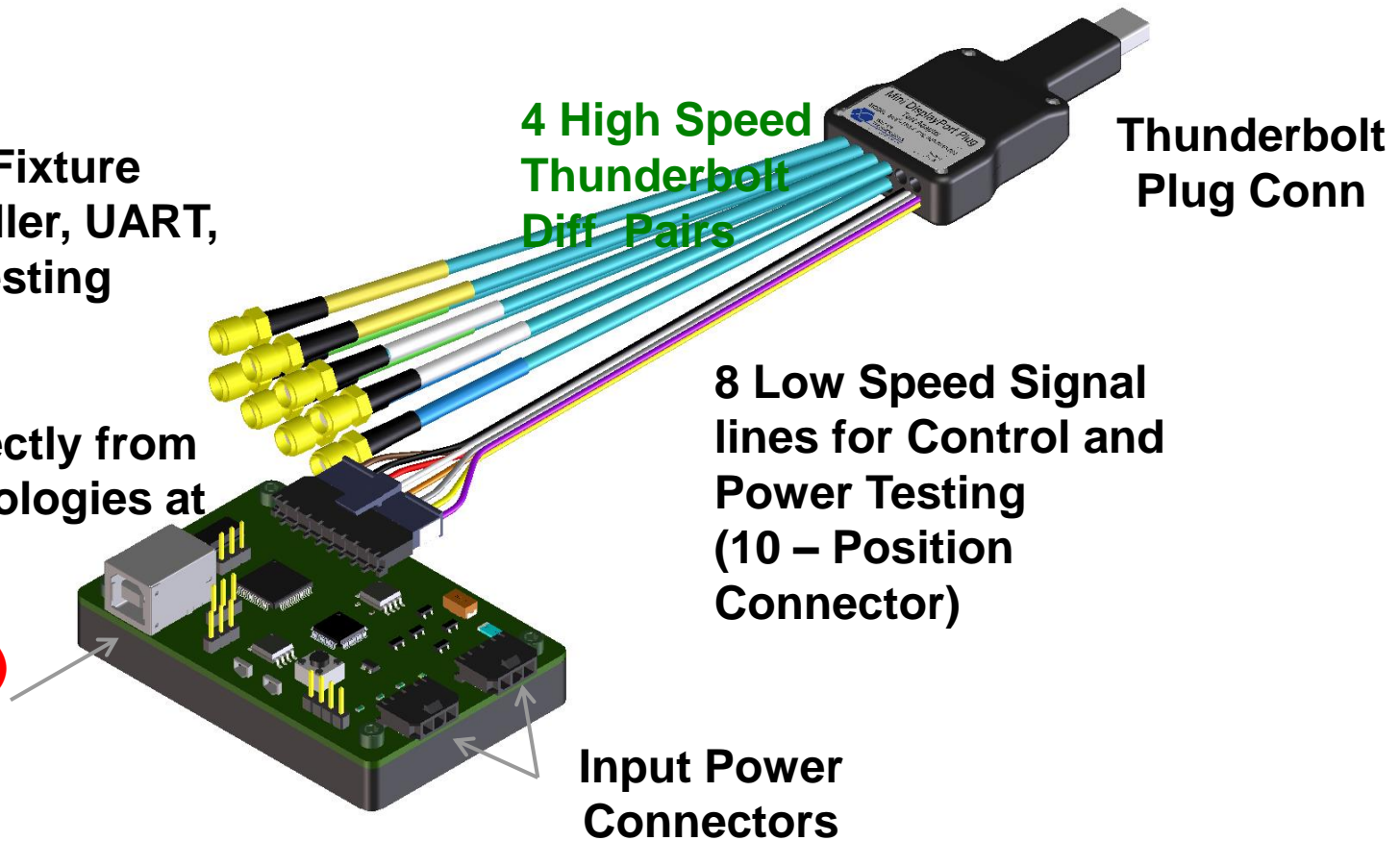
Thunderbolt Test Connectivity

- The Digital Port Micro is responsible for Test Pattern and general state control, as well as error polling in the DUT.

Thunderbolt Fixture
Micro Controller, UART,
and Power Testing
Board:

Available directly from
Wilder Technologies at
part number..

640-0503-000
(TBT-TPA-UH)
USB to PC
Connection
for Control



4 High Speed
Thunderbolt
Diff Pairs

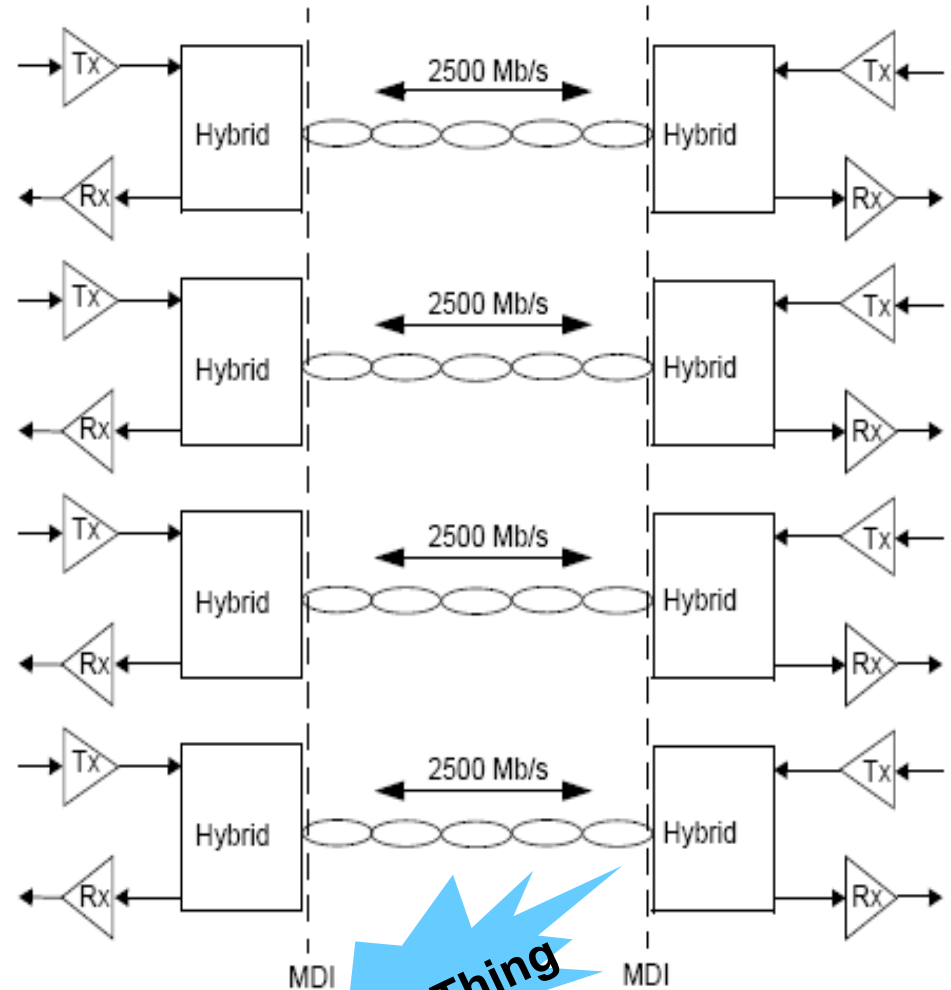
Thunderbolt
Plug Conn

8 Low Speed Signal
lines for Control and
Power Testing
(10 – Position
Connector)

Input Power
Connectors

10GBASE-T - Overview

- **10GBASE-T provides 10 gigabit/second connections over unshielded or shielded twisted pair cables, over distances up to 100 m. 2.5Gbps per lane (A, B, C & D)**
- **Baseband 16-level PAM signaling with a modulation rate of 800 Msymbols per second is used on each of the wire pairs.**
- **Supports full duplex operation only**
- **Compatibility of Auto Negotiation enabled to also operate 10/100/1000 BASE-T**
- **Supports a BER of less than or equal to $10E-12$ on all supported distances and Classes**
- **Provides a cost advantage over fiber**



Next Big Thing

XGbT – 10GBASE-T 发送端测试

	Measurement	Test Mode	XGbT Features / Notes	Does XGbT cover this measurement?
1	Maximum output droop	Sub clause 55.5.3.1, Test Mode 6	Flexibility to test beyond compliance – XGbT provides the flexibility to perform testing beyond what is specified in IEEE standard 802.3an-2006. It helps users to analyze their PHY in addition to compliance tests.	Yes
2	Transmitter timing jitter – Master	Sub clause 55.5.3.3, Test Mode 2	Measure Jitter down to just few picoseconds. Software Filters are designed and applied on the acquired data automatically while performing measurements.	Yes
3	Transmit clock frequency	Sub clause 55.5.3.5, Test Mode 2	Exact value PPM for measured clock frequency is provided	Yes
4.	Transmitter timing jitter – Slave	Sub clause 55.5.3.3, Test Mode 1 and Mode 3	Measure Jitter down to just few picoseconds. Software filters are designed and applied on the acquired data automatically while performing measurements.	Yes
5	Transmitter linearity	Sub clause 55.5.3.2, Test Mode 4. Tones 1-5	Spectral Features of the scope are used to perform the measurement, a methodology that is unique to Tektronix and approved by UNH-IOL	Yes
6	Transmitter power spectral density (PSD) and power level	Sub clause 55.5.3.4, Test Mode 5	Spectral Features of the scope are used to perform the measurement, a methodology that is unique to Tektronix and approved by UNH-IOL	Yes
7.	Return Loss	Sub clause 55.8.2.1, Test Mode 5	Return Loss is not part of XGbT solution for now, however it will finally be released in next version. For time gap arrangement please request product line for Return Loss utility	Yes**

Transmitter Power Spectral Density (PSD) and Power Level

发送端功率谱密度及功率值

- 目的：确保发送端功率谱密度和功率值满足规范要求。
- 功率值应在3.2dBm~5.2dBm范围内
功率谱密度曲线应介于规范要求的上下限曲线之间。
- 需进入Test Mode 5
- IEEE 标准 802.3an-2006, 55.5.3.4条目。
- Test Mode 5:
正常操作模式



TF-XGbT Test Fixture

- The XGbT test fixture provides easy access to the 10GBASE-T Electrical signals to perform conformance testing and device characterization as described in of IEEE 802.3an-2006 sub-clause 55.5.3 & 55.8.2.1. This fixture is used with the Tektronix's XGbT- 10GBASE-T Automation Solution to provide fast and accurate design debugging and validation. XGbT fixture covers all seven measurements including Jitter Slave and MDI Return Loss



Fig 1: XGbT Test Fixture main board

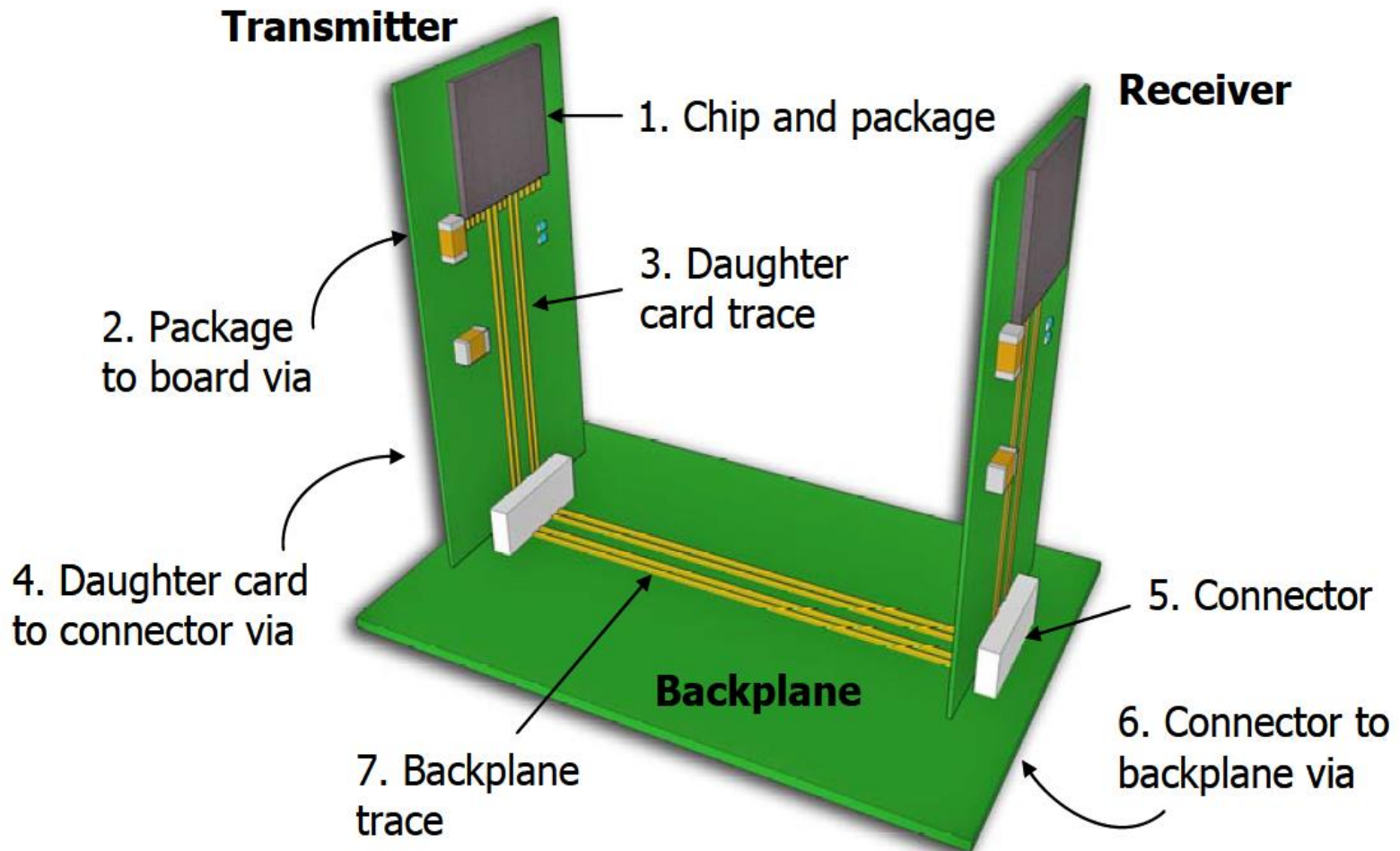


Fig 2: Calibration Board



Figure 3: RJ45 Shielded Patch cord

10G-KR Typical Backplane Ethernet

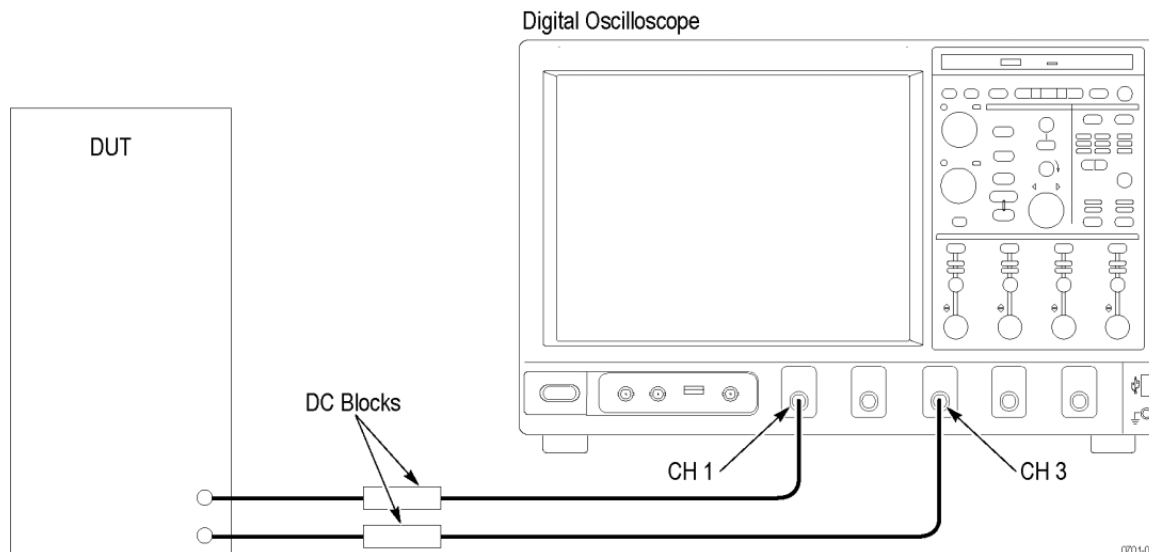
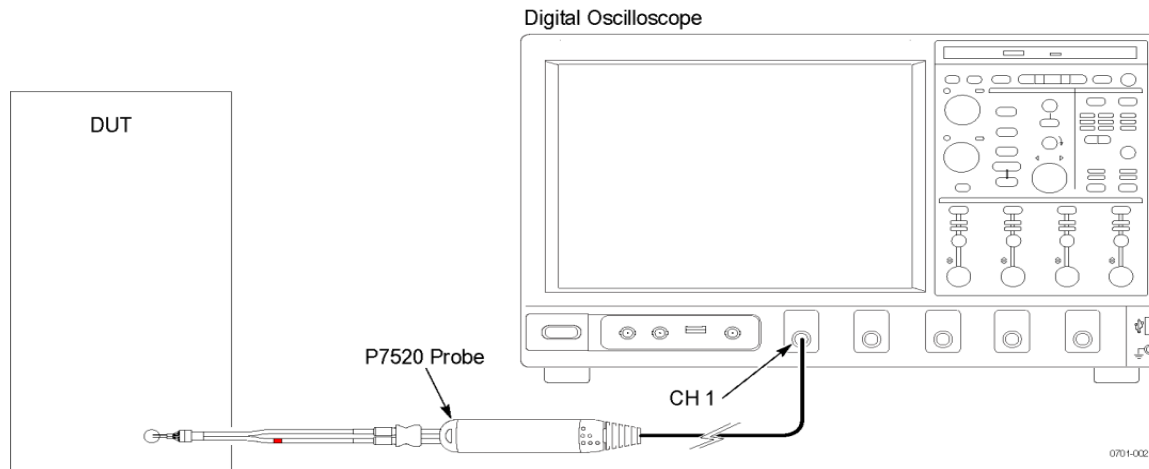


10G-KR自动化测试软件

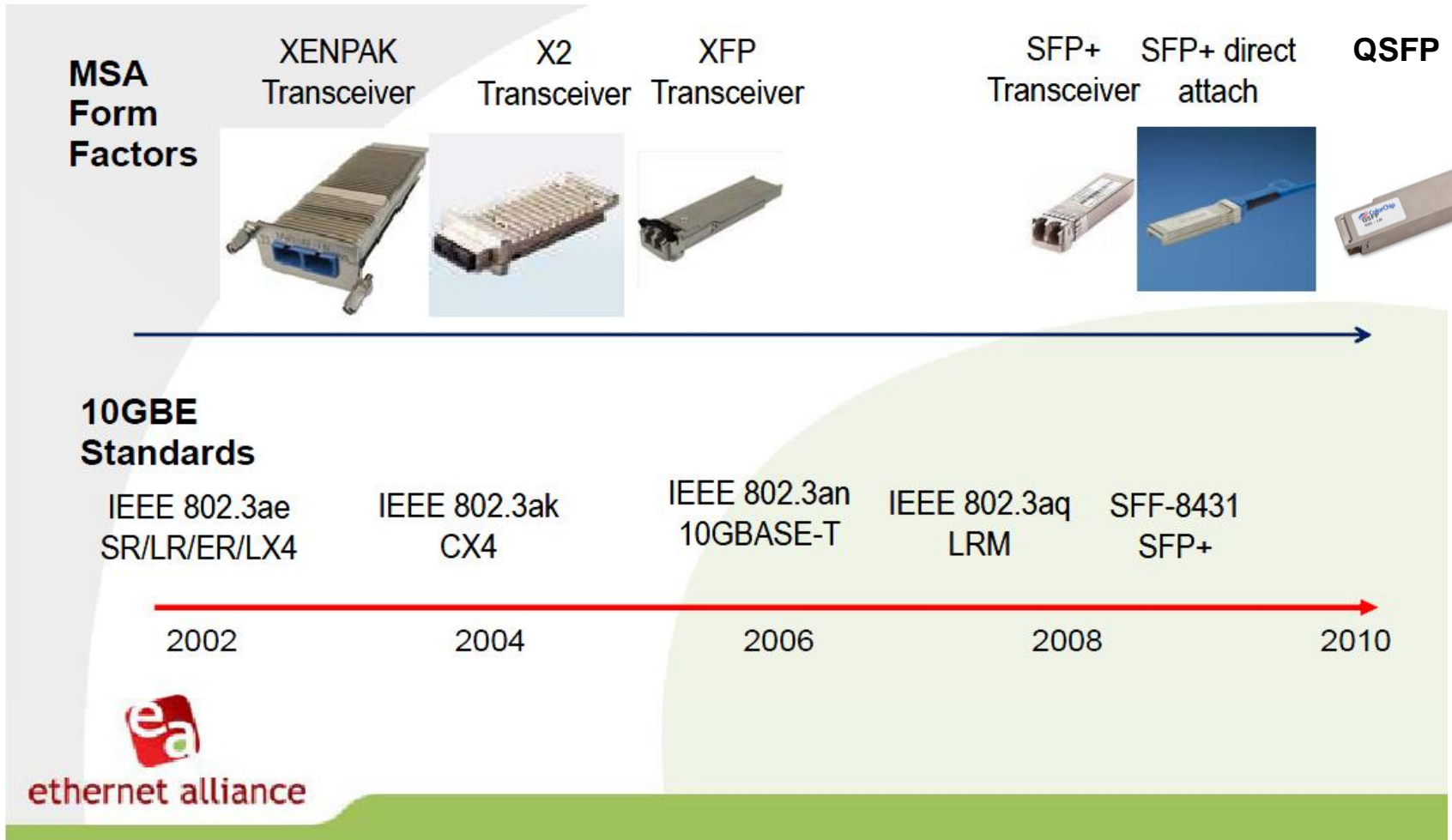
The screenshot displays the TekExpress 10G-KR (Evaluation Version) software interface. The main window title is "TekExpress 10G-KR (Evaluation Version) - (Untitled)*". The interface is divided into several sections:

- Left Panel:** Contains navigation buttons for "Setup", "Status", "Results", and "Reports". A vertical progress indicator shows the current step is "2 Test Selection", with "DUT", "Acquisitions", and "Preferences" also marked as completed.
- Top Panel:** Shows "Device : Source : CTS 0.9" and control buttons for "Deselect All", "Select Required", and "Select All".
- Test Selection List:** A list of tests under the "10GKR" category, all of which are checked. The first test, "Test 72.7.1.3_Signaling speed", is highlighted in blue. A green box highlights the first seven tests in the list.
 - 10GKR
 - Test 72.7.1.3_Signaling speed
 - Test 72.7.1.4_Differential peak-to-peak output voltage (max)
 - Test 72.6.5_Differential peak-peak output voltage (max) with Tx disa
 - Test 72.7.1.4_Common-mode voltage limits
 - Test 72.7.1.7_Transition time
 - Test 72.7.1.8_Max output jitter (peak-peak)
 - Test 72.7.1.10_Transmitter output waveform characteristics
 - Test 72.7.1.11a_Output waveform coefficient update
 - Test 72.7.1.11b_Output waveform coefficient status
- Test Description:** A text area containing the description: "The 10GBASE-KR signaling speed shall be 10.3125 GBd ± 100 ppm." Buttons for "Schematic" and "Configure" are located to the right of the text area.
- Right Panel:** Contains "Start" and "Pause" buttons.
- Bottom Panel:** Shows the "Tektronix" logo and a "Status Ready" indicator.

Testing connection for 10G-KR



10Gigabit Ethernet Interface Evolution



Source : Ethernet Alliance

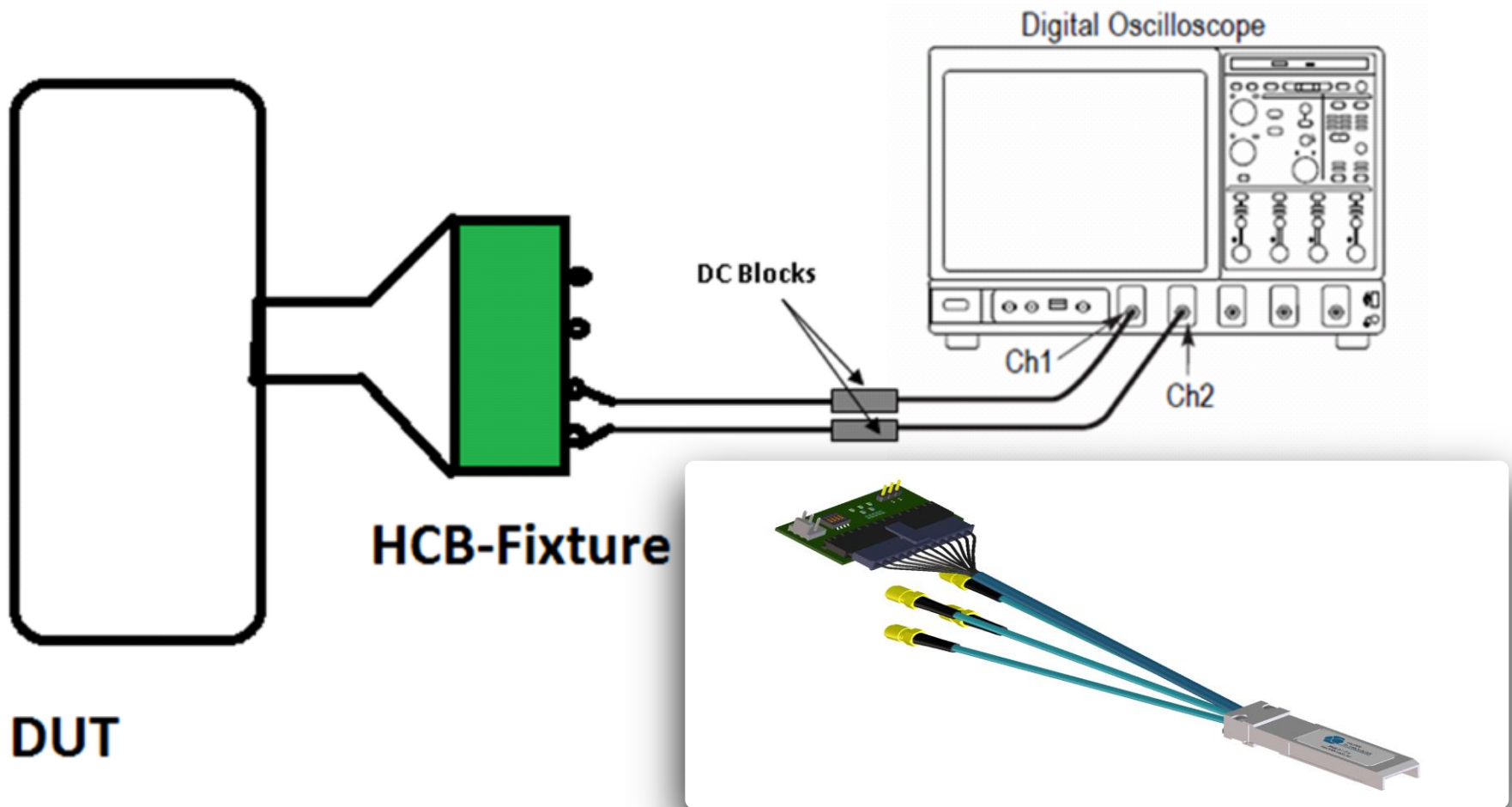
Next Big Thing
SFF-8431
SFP+

Tektronix SFP-TX – Automation & DPOJET Option

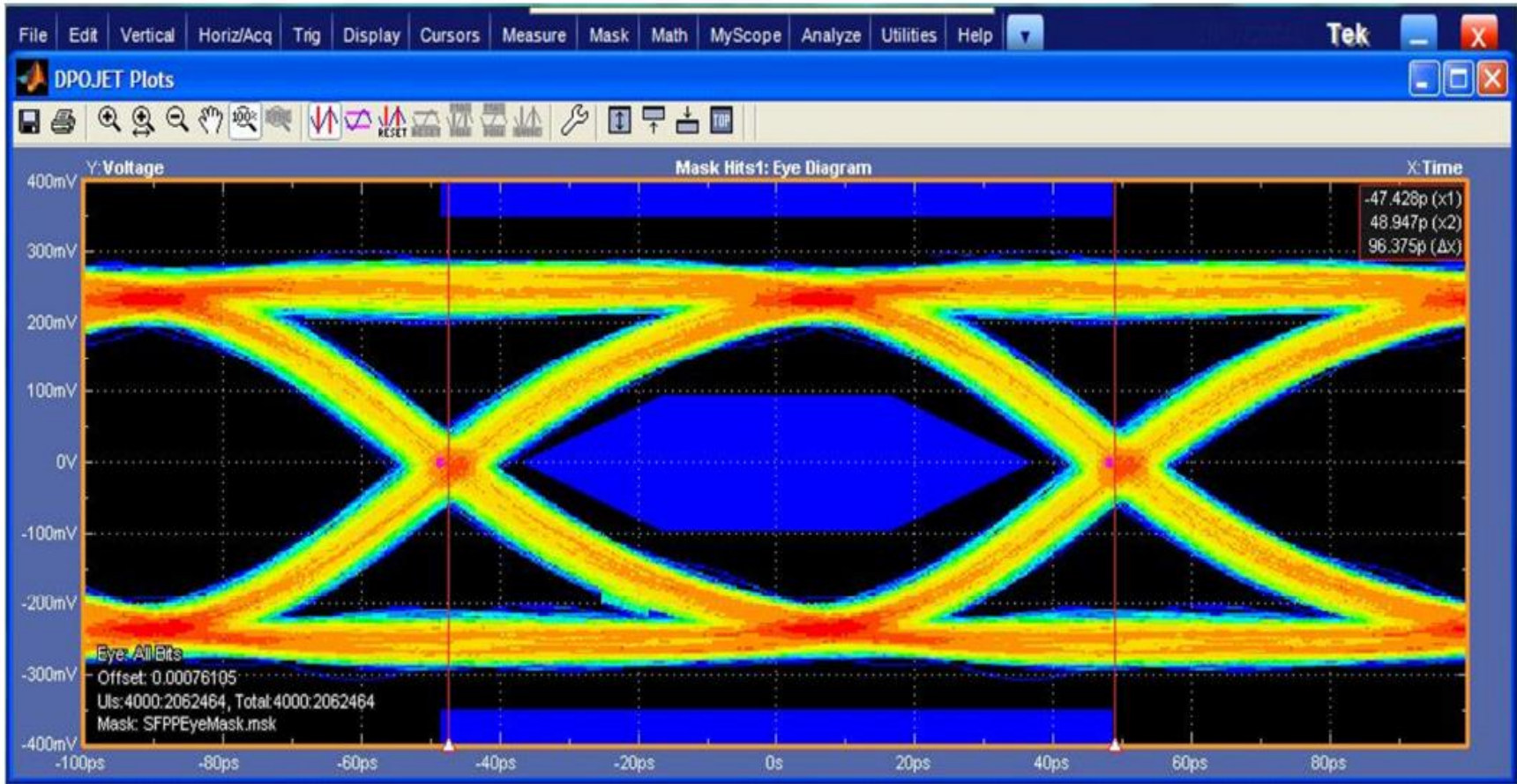
SL No.	Measuremnts	Signal Type Recommended	Limit			
			Min	Target	Max	Units
Host Transmitter output electrical Specifications:						
1	Single Ended Output Voltage Range	PRBS31	-0.3		4	V
2	Output AC Common Mode voltage (RMS)	PRBS31			15	mV(RMS)
Host Transmitter Jitter and Eye Mask specifications						
3	Crosstalk source rise/fall time (20%-80%) (Tr, Tf)	8180		34		ps
4	Crosstalk source amplitude (p-p differential)	8180		1000		mV
5	Signal rise/fall time (20%-80%) (Tr, Tf)	8180	34			ps
6	Total Jitter (p-p) (Tj)	PRBS31			0.28	UI(p-p)
7	Data Dependent Jitter (p-p) (DDJ)	PRBS9			0.1	UI(p-p)
8	Data Dependent Pulse Width Shrinkage (p-p) (DDPWS)	PRBS9			0.055	UI(p-p)
9	Uncorrelated Jitter (RMS) (UJ)	PRBS9			0.023	UI(p-p)
10	Transmitter Qsq	8180	50			
11	Eye mask hit ratio(Mask hit ratio of 5x10-5)	PRBS31	X1=0.12UI, X2=0.33UI, Y1=95mV, Y2=350mV			
Host Transmitter output specifications for Cu (SFP+ host supporting direct						
12	Voltage Modulation Amplitude (p-p)	8180	300			mV
13	Transmitter Qsq Output AC Common Mode voltage	8180	63.1			
14	Output AC Common Mode Voltage	PRBS31			12	mV(RMS)
15	Host Output TWDPc	PRBS9			10.7	dBc

The image displays two screenshots of the Tektronix software interface. The top screenshot shows a signal waveform with a menu open, highlighting the 'Jitter and Eye Analysis (DPOJET)' option. The bottom screenshot shows the 'TekExpress SFP+ Tx - (Untitled)' configuration window. This window includes a 'Test Selection' list with various test items checked, such as 'SFF-8431 Table 11 Output Electrical Specifications at B', 'Crosstalk Source Rise/Fall Time (20%-80%)', and 'Eye Mask Hit Ratio'. A 'Test Description' section at the bottom provides details on how the rise/fall time is measured.

SFP test connection

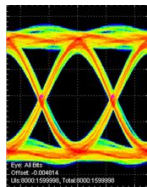


SFP Eye Mask hit ratio :less than 5E10-5

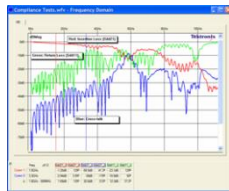


Add-In Card (CEM Spec) Tx Testing

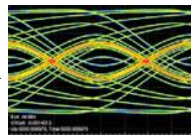
- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements



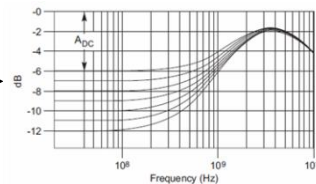
Signal Acquired from Compliance Board



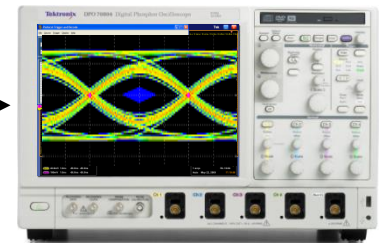
Embed Compliance Channel and Package



Closed Eye due to the Channel



Apply CTLE + DFE

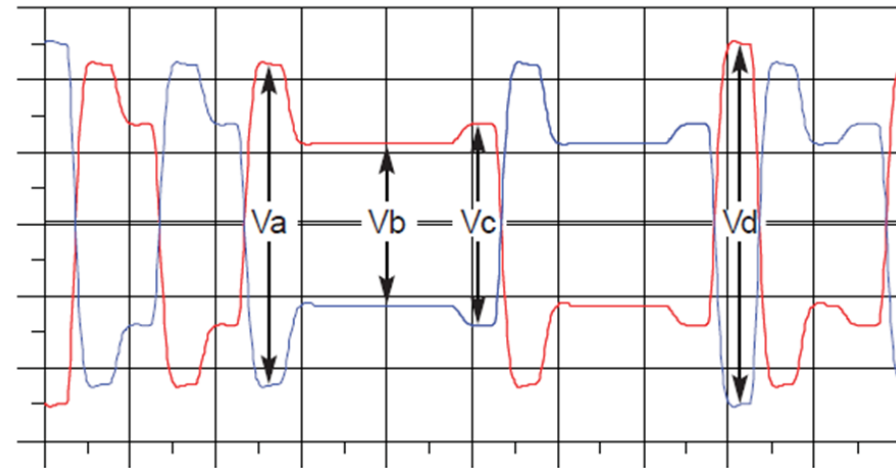


Open Eye for Measurements

Compliance Patterns

- Once in compliance mode, bursts of 100MHz clock can be used to cycle through various settings of compliance patterns to perform, Jitter, voltage, timing measurements.

Data Rate	Preshoot	De-emphasis
2.5 GT/s,		-3.5 dB
5.0 GT/s,		-3.5 dB
5.0 GT/s,		-6.0 dB
8.0 GT/s,	P0 = 0.0	-6.0±1.5dB
8.0 GT/s,	P1 = 0.0	-3.5±1.5dB
8.0 GT/s,	P2 = 0.0	-4.4±1.5dB
8.0 GT/s,	P3 = 0.0	-2.5±1dB
8.0 GT/s,	P4 = 0.0	0.0dB
8.0 GT/s,	P5 = 1.9±1dB	0.0dB
8.0 GT/s,	P6 = 1.9±1dB	0.0dB
8.0 GT/s,	P7 = 1.9±1dB	-6.0±1.5dB
8.0 GT/s,	P8 = 1.9±1dB	-3.5±1dB
8.0 GT/s,	P9 = 1.9±1dB	0.0dB
8.0 GT/s,	P10 = 1.9±1dB	Test Max Boost Limit

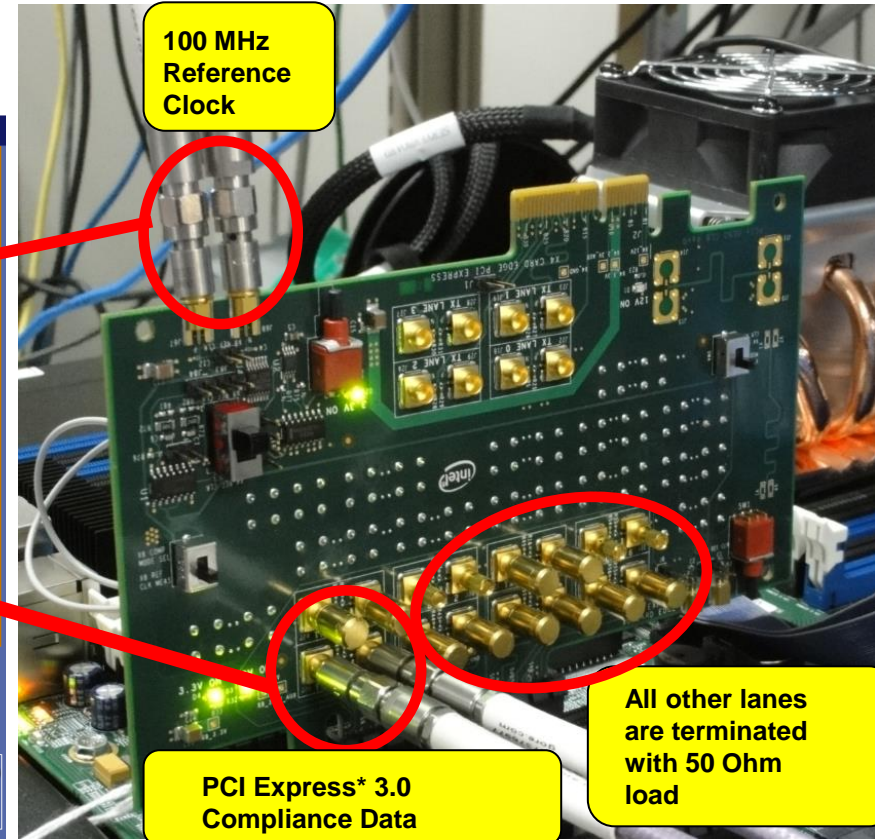
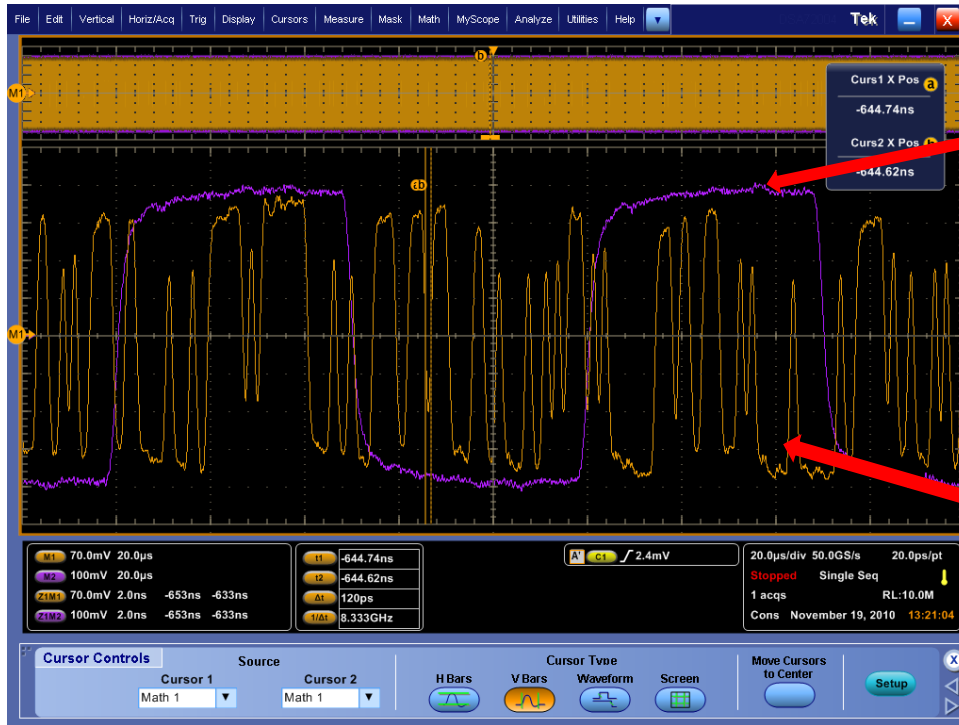


$$\text{De-emphasis} = 20\log_{10} V_b/V_a$$

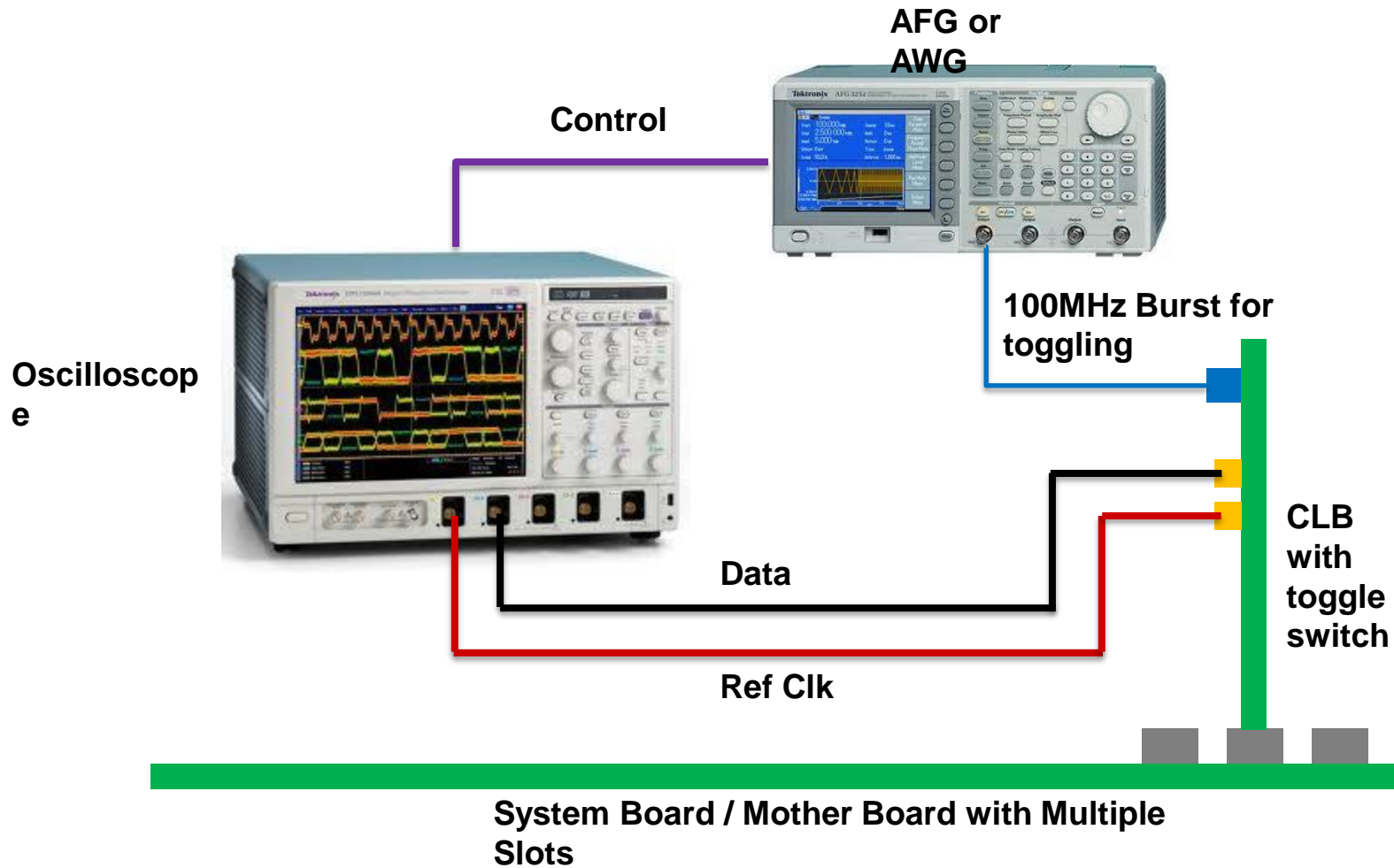
$$\text{Preshoot} = 20\log_{10} V_c/V_b$$

$$\text{Boost} = 20\log_{10} V_d/V_b$$

PCIe Dual-Port TX Measurement Example for System



Automated DUT Control



TekExpress Automation for Tx Compliance - Setup

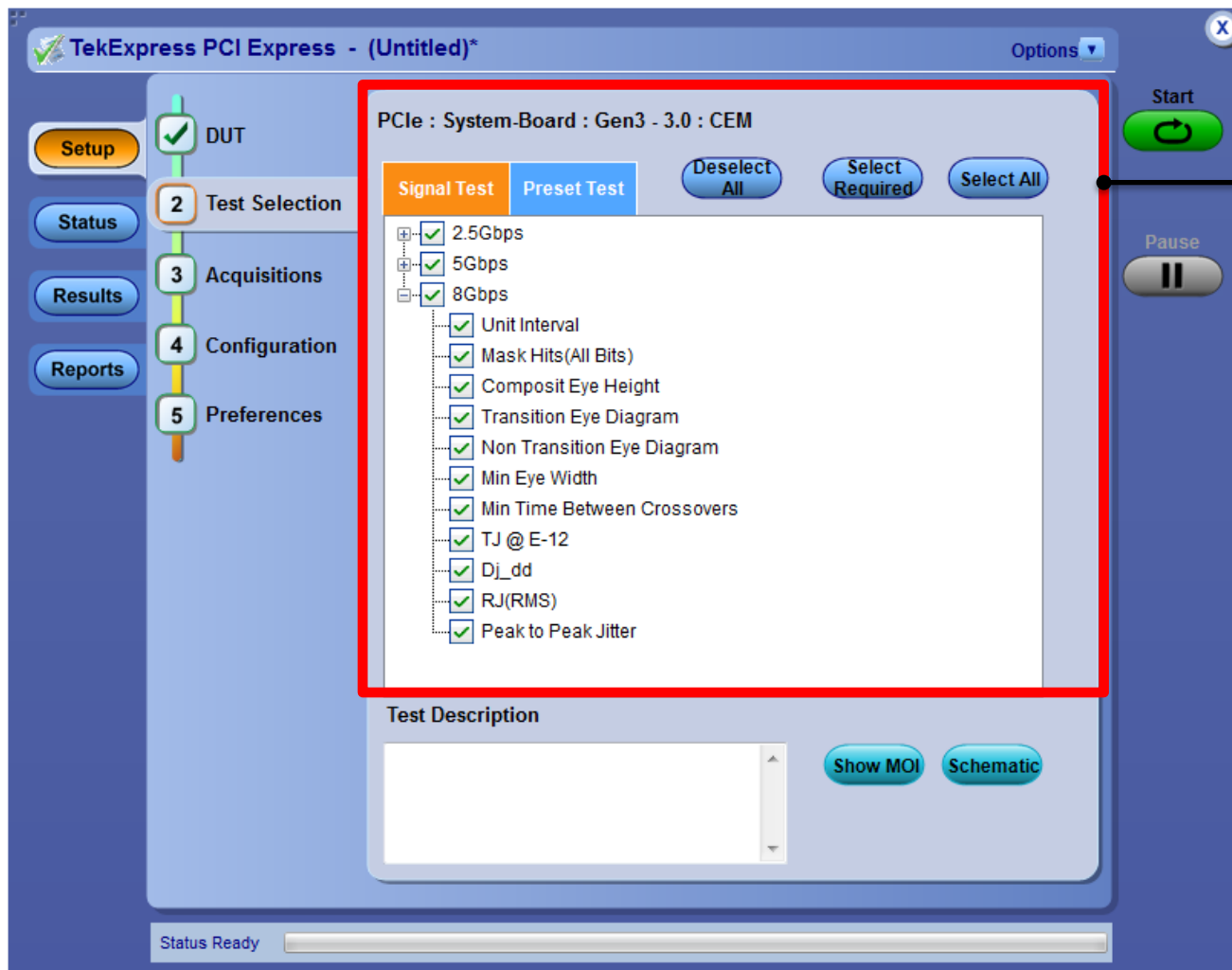
The screenshot shows the TekExpress PCI Express software interface. On the left, a navigation pane includes buttons for Setup, Status, Results, and Reports, and a vertical progress indicator with steps 1 (DUT), Test Selection, Acquisitions, Configuration, and 5 (Preferences). The main area is divided into several sections:

- DUT Section:** DUT ID: DUT001, Slot Number: 01. Radio buttons for "Acquire live waveforms" (selected) and "Use pre-recorded waveform files".
- SigTest Mode:** Compliance (dropdown).
- Version/Specification/Device Type:** Gen3 - 3.0, CEM, Add-In-Card.
- Device Profile:**
 - Data Rates: 2.5 Gb/s, 5 Gb/s, 8 Gb/s (all checked).
 - Transmitter Equalization: 3.5 dB, 6 dB (both checked).
 - Link Analysis: Setup button.
 - Presets: Selected Presets for Signal Quality (P0-P10).
 - Voltage Swing: Full Swing (selected), Reduced Swing.
 - SSC: On (selected), Off.
 - Cross Talk: CrossTalk (Interleaved) (selected), Non CrossTalk (Non Interleaved).
- Link Width:** 16 Lanes, Lanes button.
- Selected Test Lanes:** L0, L03, L07, L11, L15.
- Automated DUT Control:** Checked, Setup button.
- Signal Validation:** Prompt me if Signal Check Fails (dropdown).
- Perform Pattern Decoding:** Checked.

On the right side of the interface, there are Start and Pause buttons. Four callout boxes point to specific features:

- Run Analysis on Live or Pre-Recorded Data:** Points to the radio buttons for waveform acquisition.
- Type of test / device selection:** Points to the Version, Specification, and Device Type dropdowns.
- Test selection:** Points to the SigTest Mode dropdown.
- Automate DUT control:** Points to the Automated DUT Control checkbox and button.

TekExpress Automation for Tx Compliance – Test



TekExpress Automation for Tx Compliance – Reports

TekExpress PCI Express - (Untitled)* Options ▾

Overall Test Result ✔ Pass Preferences ▾

Signal Test Preset Test

Setup
Status
Results
Reports

Description	Details	Generation	Pass/Fail	Value	Margin
▶ Lane0			✔ Pass		
[-] Unit Interval	Mean Unit Interval	8Gbps P07	✔ Pass	125.0090 ps	L: 0.0465 ps H: 0.0235 ps
	High Limit		✔ Pass	125.0325	
	Low Limit		✔ Pass	124.9625	
[+] Mask Hits(All Bits)	Mask Hits	8Gbps P07	✔ Pass	0.0000 hits	H: 0.0000 hits
[+] Composit Eye Height	Composit Eye Height	8Gbps P07	✔ Pass	105.7689 mV	L: 71.7689 mV
[+] Transition Eye Diagram	Min Transition Eye Height	8Gbps P07	Informative	107.2269 mV	N.A
[+] Transition Eye Diagram	Min Transition Voltage	8Gbps P07	✔ Pass	-0.1264 mV	L: 599.8736 mV
[+] Transition Eye Diagram	Max Transition	8Gbps P07	✔ Pass	0.1289 mV	H: 599.8711 mV
[+] Transition Eye Diagram	Min Transition Top Margin	8Gbps P07	✔ Pass	0.0259 mV	L: 0.0259 mV
[+] Transition Eye Diagram	Min Transition Bottom Margin	8Gbps P07	✔ Pass	-0.0314 mV	H: 0.0314 mV
[+] Transition Eye Diagram	Transition Eye Mask Hits	8Gbps P07	✔ Pass	0.0000 hits	H: 0.0000 hits
[+] Non Transition Eye Diagram	Min Non Transition Eye Height	8Gbps P07	Informative	112.3181 mV	N.A
[+] Non Transition Eye Diagram	Min Non Transition	8Gbps P07	✔ Pass	-0.1274 mV	L: 599.8726 mV

Status Completed. Start

Pause Clear

TekExpress Automation for Tx Compliance – Reports



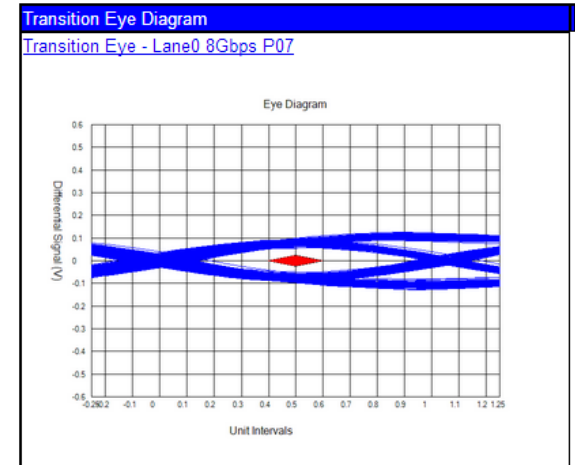
Add-In-Card Test Report

Setup Information	
DUT ID : DUT001	DPOJET Version : 6.0.1 Build 8
Date/Time : 2013-06-10 17:28:45	Scope Model : DPO73304D
Device Type : PCIe	Scope Serial Number : B241123
TekExpress Version : PCI Express:2.0.0.66 (Beta_Build) Framework:3.0.0.16_RevD	SPC, FactoryCalibration : PASS:PASS
Spec Version : Gen3 - 3.0	Scope FW Version : 6.7.4 Build 3
SigTest Version : 3_2_0	Probe1 Model : TCA292D
Slot Number : 01	Probe1 Serial Number : N/A
Overall Execution Time : 0:03:21	Probe2 Model : TCA292D
Overall Test Result : Pass	Probe2 Serial Number : N/A
	Probe3 Model : TCA292D
	Probe3 Serial Number : N/A
	Probe4 Model : TCA292D
	Probe4 Serial Number : N/A
	Signal Source Model : AFG3252
	Signal Source Serial Number : C010899
DUT Comment :DUT001	

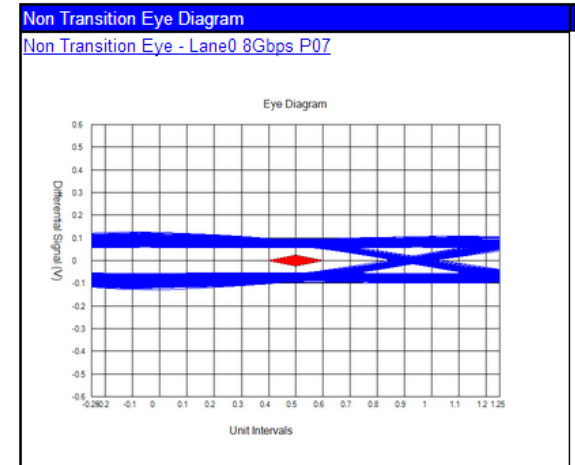
Test Name:Summary Table	
Unit Interval	Pass
Mask Hits(All Bits)	Pass
Composit Eye Height	Pass
Transition Eye Diagram	Pass
Non Transition Eye Diagram	Pass
Min Eye Width	Informative
Min Time Between Crossovers	Informative
mhtml:file://X:\PCI Express\Reports\DUT081_mht#TJ @ E-12	Pass
Dj_dd	Informative
RJ(RMS)	Pass
Peak to Peak Jitter	Informative

Unit Interval									
Measurement Details	Lane Name	DataRate	Equalization	Measured Value	Test Result	Margin	Low Limit	High Limit	Comments
Mean Unit Interval	Lane0	8Gbps	P07	125.0090 ps	Pass	L: 0.0465 ps H: 0.0235 ps	124.9625	125.0325	

[Back To Summary Table](#)

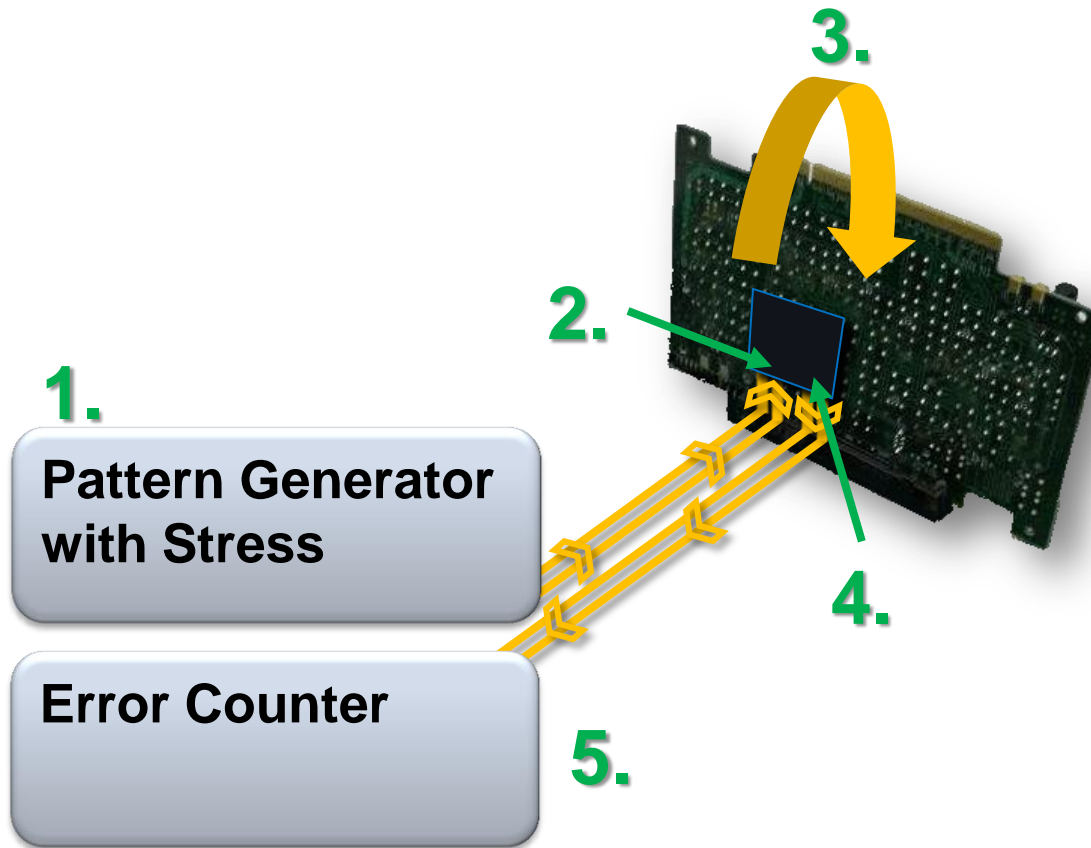


[Back To Summary Table](#)



[Back To Summary Table](#)

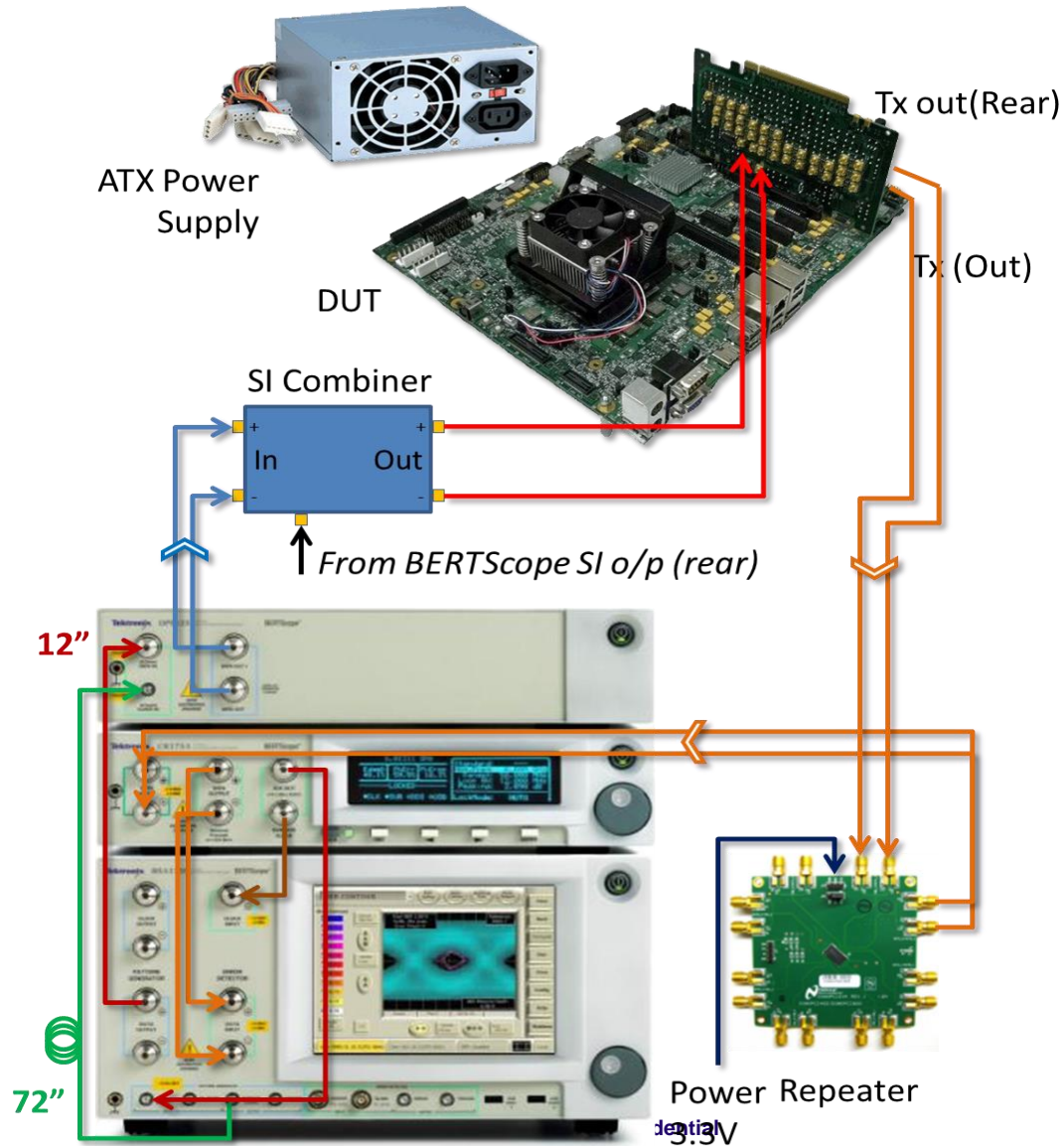
Basic Receiver Testing



At the simplest level, receiver testing is composed of:

1. Send **impaired signal** to the receiver under test
2. The **receiver decides** whether the incoming bits are a one or a zero
3. The chip **loops back** the bit stream to the transmitter
4. The **transmitter sends out** exactly the bits it received
5. An **error counter** compares the bits to the expected signal and looks for mistakes (errors)

RX Measurement Example for Host



USB 3.0 Key Considerations

- Receiver Testing Now Required
 - Jitter tolerance
 - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel Considerations
 - Need to consider transmission line effects
 - Software channel emulation for early designs
- New Challenges
 - 12" Long Host Channel
 - Closed Eye at Rx
 - Equalization
 - De-emphasis at Tx
 - Continuous Time Linear Equalizer (CTLE) at Rx

6 Physical Layer

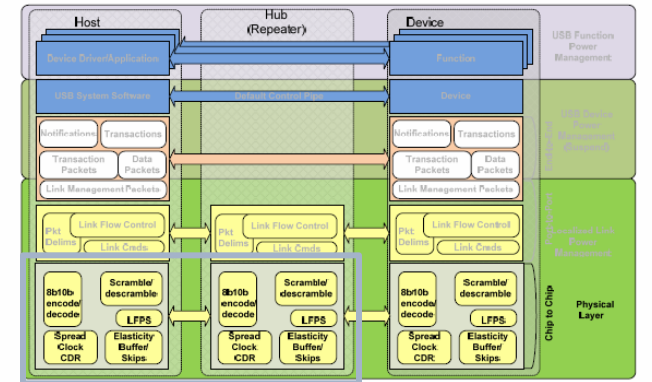
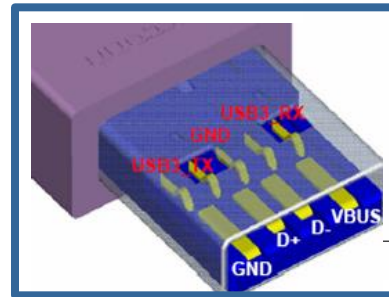
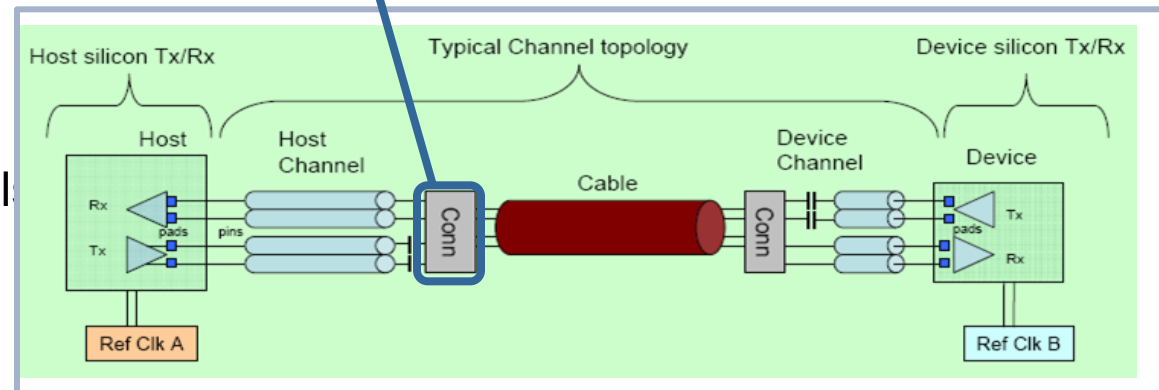


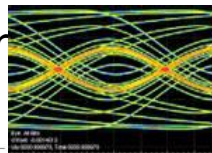
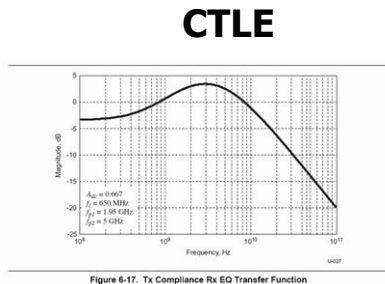
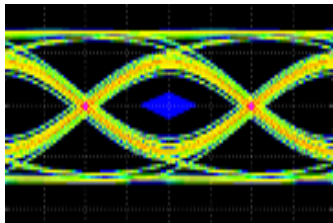
Figure 6-1. Super Speed Block Diagram: Physical



Source: USB 3.0 Rev 1.0 Specification

USB 3.0 Compliance Test Configuration

- USB 3.0 is a closed eye specification
 - Reference channel is embedded and CTLE is applied
- USB 3.0 Reference Channels
 - Host Reference Channel
 - 11" back panel is applied for device testing
 - Device Reference Channel
 - 5" device channel is applied for host testing
 - 3 Meter Reference Cable
 - Used for host and device (except captive devices) testing in addition to reference channels
- USB 3.0 Reference Equalizer
 - Attenuates the low frequency part of the signal to open the



part of the signal to open the

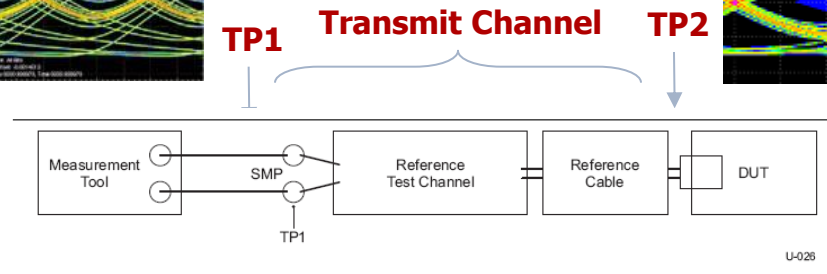
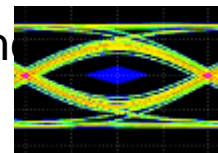


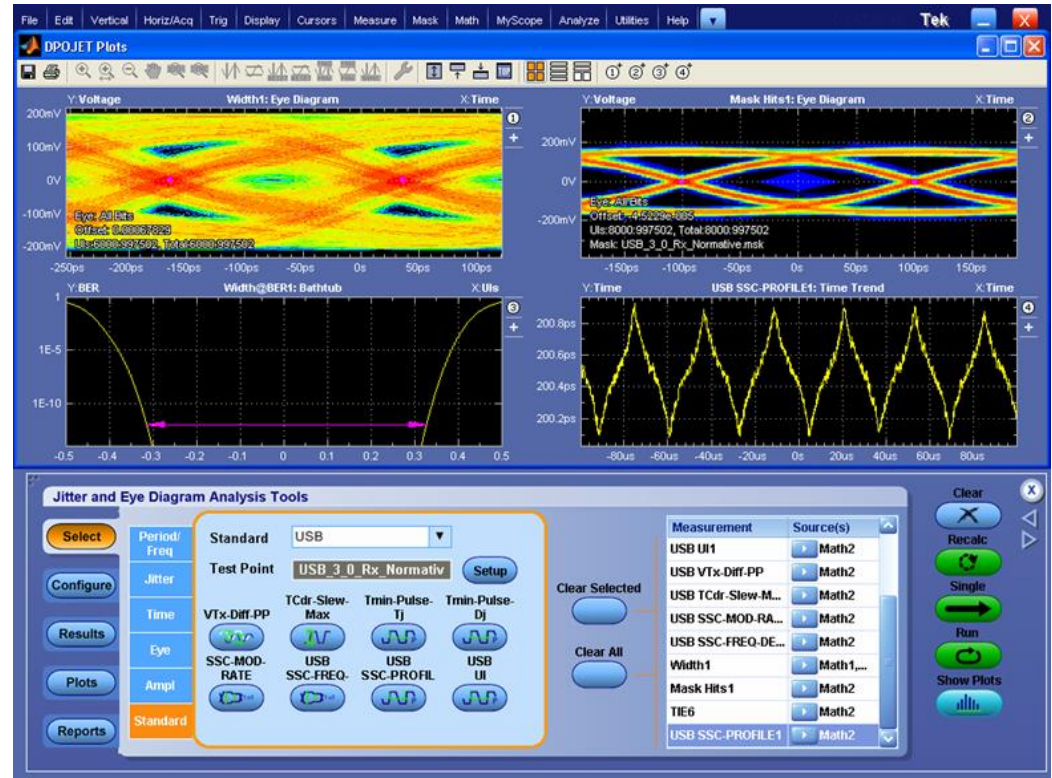
Figure 6-14. Tx Normative Setup with Reference Channel

USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
 - Eye Height
 - Pk to Pk Differential Voltage
 - RJ
 - DJ
 - TJ
 - Slew Rate

- Low Frequency Periodic Signaling (LFPS)
 - Pk to Pk Differential Voltage
 - Rise / Fall Time
 - AC Common Mode
 - tBurst
 - tRepeat
 - tPeriod

- SSC
 - Modulation Rate
 - Deviation



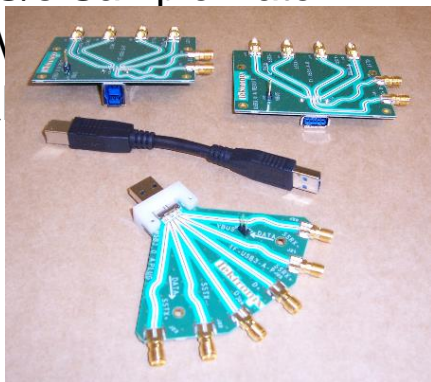
Complete USB 3.0 Transmitter Solution

DPO/DSA70000 Series Oscilloscopes

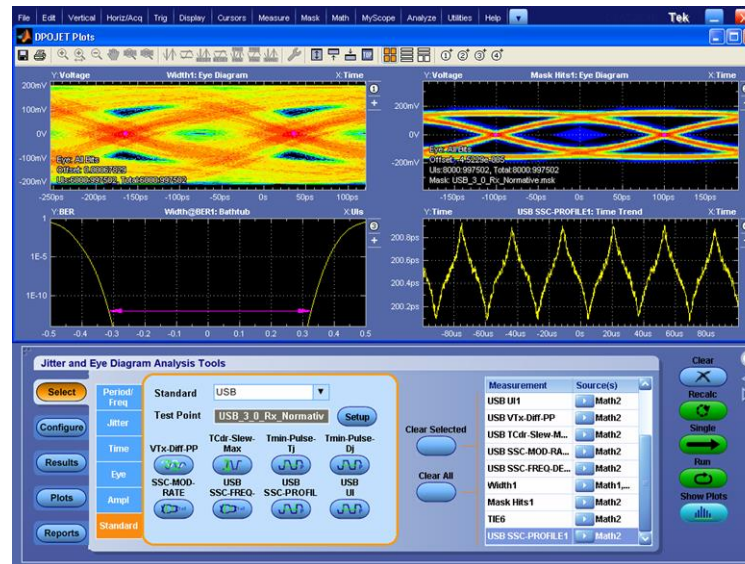
- Go Beyond Compliance Testing
 - Debug Suite with DPOJET
 - SDLA for Channel Modeling
 - Tektronix Super Speed USB Fixtures

- Automation software for characterization and compliance
 - TekExpress with option USB-TX (includes option USB3)

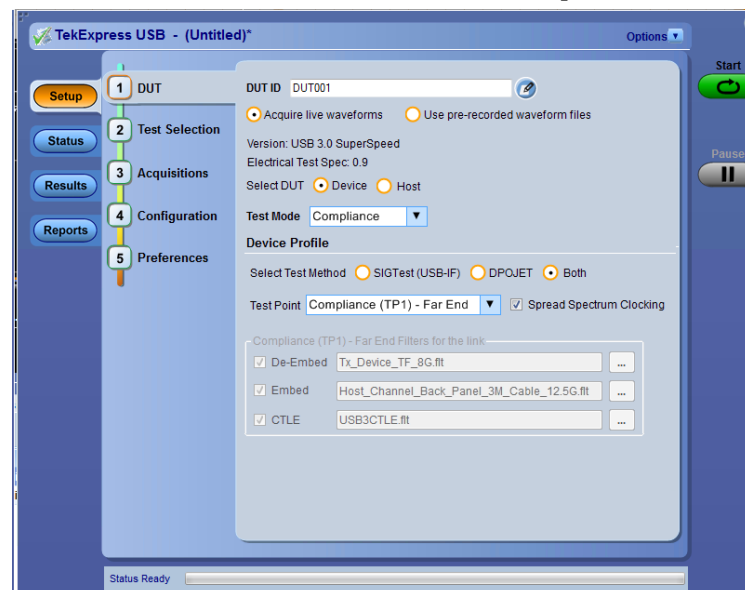
- Recommended Scope
 - 12.5 GHz Real-Time Scope
 - 50 GS/s Sample Rate
 - P7313SM (Optional)



Opt. USB3

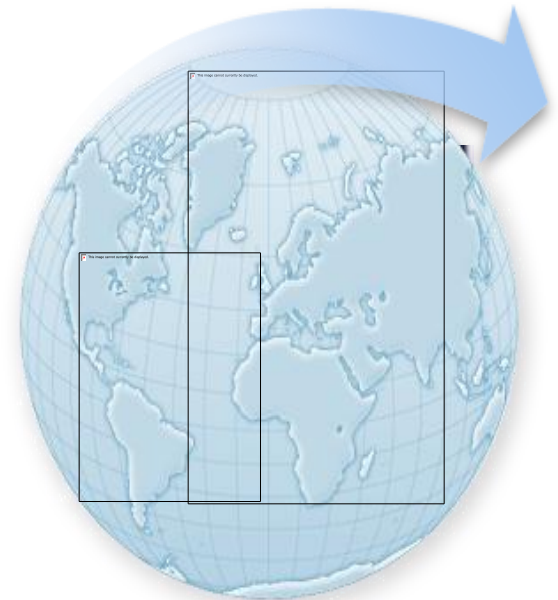


Opt. USB-TX



Increasing Serial Data Bandwidth

- **USB 2.0, 480 Mb/s (2000)**
 - Shift from slower, wide, parallel buses to narrow, high speed serial bus
 - 40x faster data rate, support for new connectors & charging
- **USB 3.0, 5 Gb/s (2008)**
 - ~10x faster data rate over 3 meter cable
 - Faster edges, 'closed eye' architecture
- **USB 3.0, 10 Gb/s (2013)**
 - 2x faster data rate over 1 meter cable
 - 'Scaled' SuperSpeed implementation



Transmitter Validation Example - DPOJET

- Recall DPOJET SSP setups

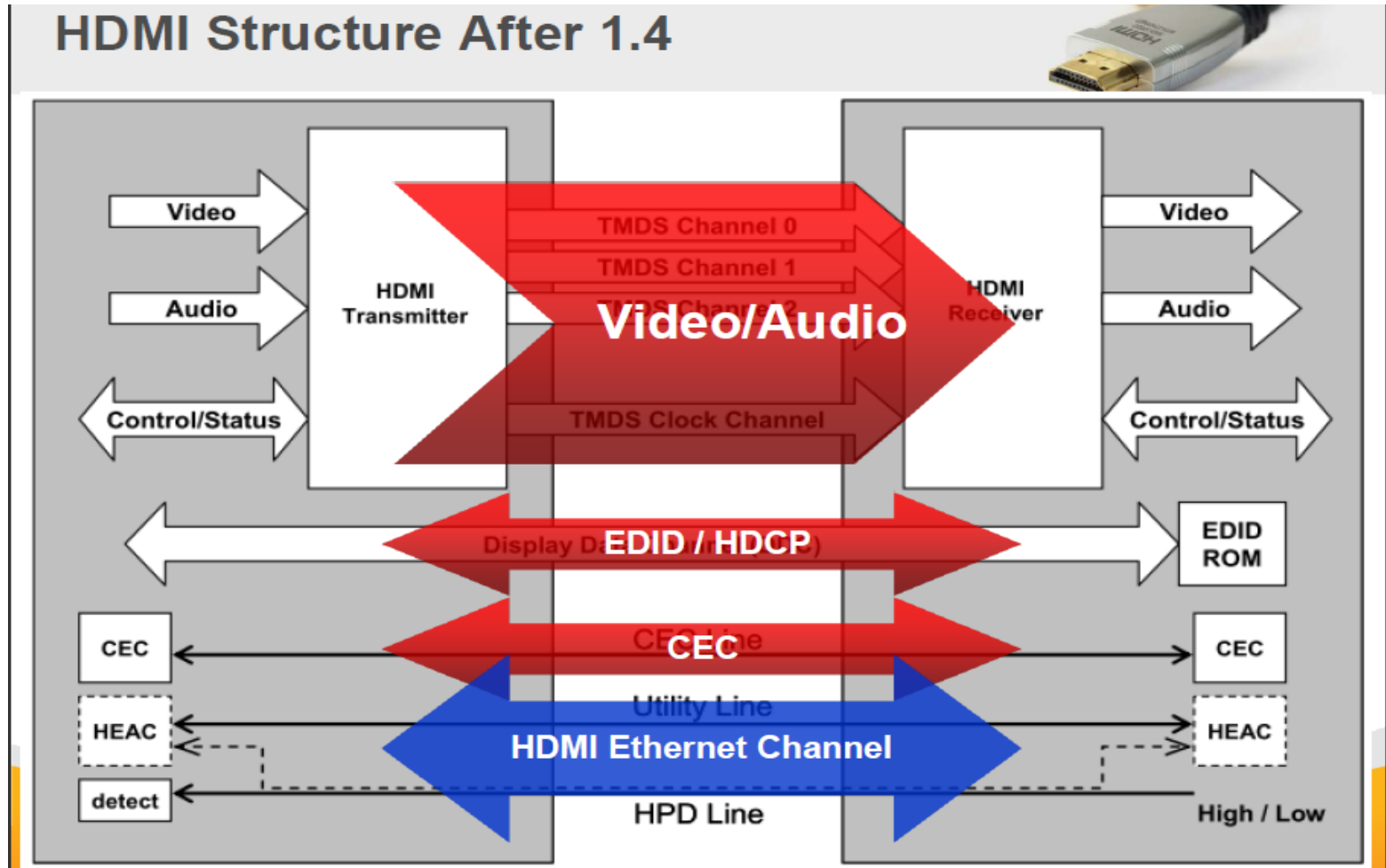
The screenshot displays the Tektronix DPOJET software interface, divided into several key sections:

- Configuration Panel (Top Left):** Shows the 'Jitter and Eye Diagram Analysis Tools' window. The 'Standard' is set to 'USB'. The 'Test Point' is 'USB3_Device_CP0_Nor'. Various jitter and eye diagram parameters are visible, such as 'VTx-Diff-PP', 'TCdr-Slew-Max', and 'SSC-FREQ-DEV-MAX'.
- Measurement List (Top Right):** A table listing measurements and their sources:

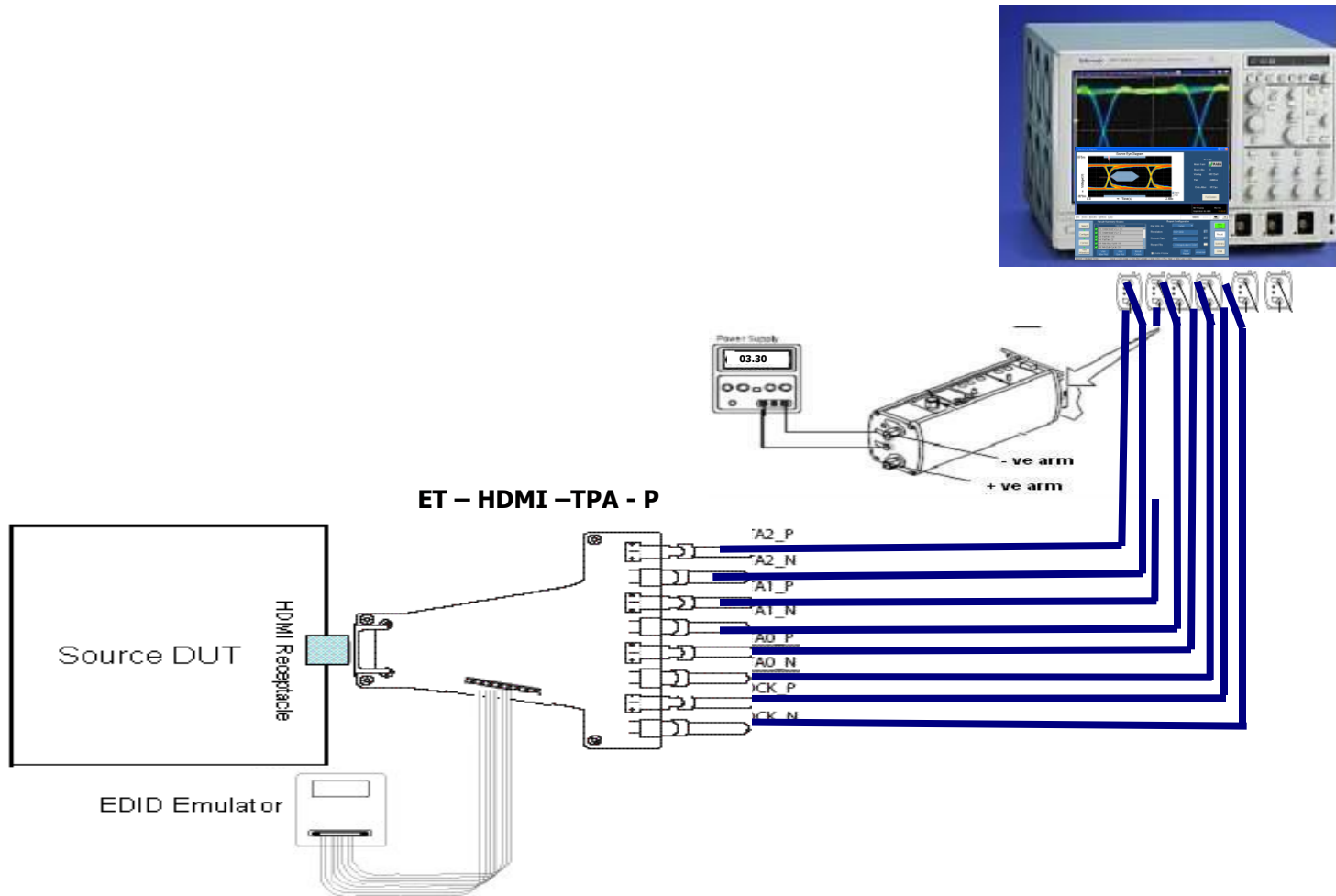
Measurement	Source(s)
TJ@BER1	Math2
DJ-δδ1	Math1
Eye Height	Math2
USB UI1	Math1
USB VTx-Diff-PP	Math1
De-emphasis	Math1
Preshoot	Math1
Eye Height afterCh...	Math3
- Analysis Plots (Middle):** Three eye diagrams are shown side-by-side. The left plot is the 'Eye: All Bits' with an offset of 0.0037279. The middle plot is the 'Eye: All Bits' with an offset of 0.0037279. The right plot is the 'Eye: All Bits' with an offset of 0.0077441 and a mask applied: 'Mask: USB_3_0_SSP_Rx_Normative.msk'.
- Results Table (Bottom):** A table showing the overall test results for various parameters:

Description	Pass/Fail	Mean	Std Dev	Max	Min	p-p	Population
TJ@BER1, Math2	Pass	55.784ps	0.0000s	55.784ps	55.784ps	0.0000s	1
DJ-δδ1, Math1	Pass	2.8399ps	0.0000s	2.8399ps	2.8399ps	0.0000s	1
Eye Height, Math2	Pass	78.470mV	0.0000V	78.470mV	78.470mV	0.0000V	1
USB UI1, Math1	Pass	100.00ps	0.0000s	100.00ps	100.00ps	0.0000s	1
USB VTx-Diff-PP, M...	Pass	823.92mV	41.718mV	956.63mV	708.63mV	248.00mV	499887
De-emphasis, Math1	Pass	1.3244	74.023m	1.5882	907.24m	680.93m	44430
Preshoot, Math1	Pass	1.3608	47.502m	1.5759	1.1950	380.90m	43907
Eye Height afterCh...	Pass	0.0000V	0.0000V	0.0000V	0.0000V	0.0000V	1
Mask Hits1, Math2	Pass	0.0000	0.0000	0.0000	0.0000	0.0000V	989277

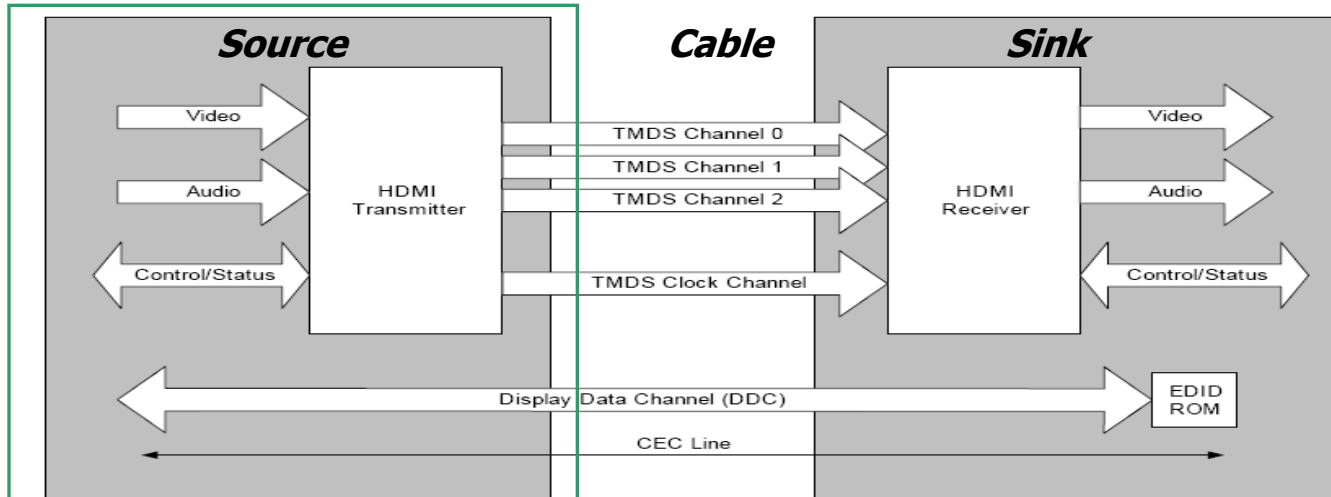
HDMI Basics



HDMI 测试方案-源端

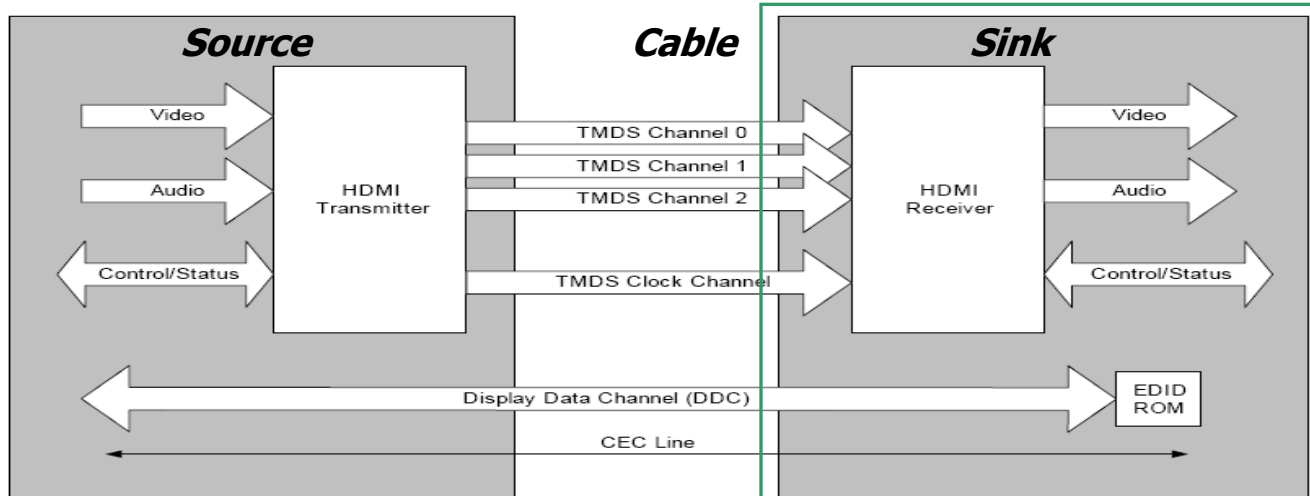


HDMI Source Testing



- Rise/Fall Time
 - Inter-pair Skew
 - Clock Duty Cycle
 - Clock Jitter
 - Eye Diagram
- } Differential
- Voltage VL
 - Intra-pair Skew
- } Single-ended

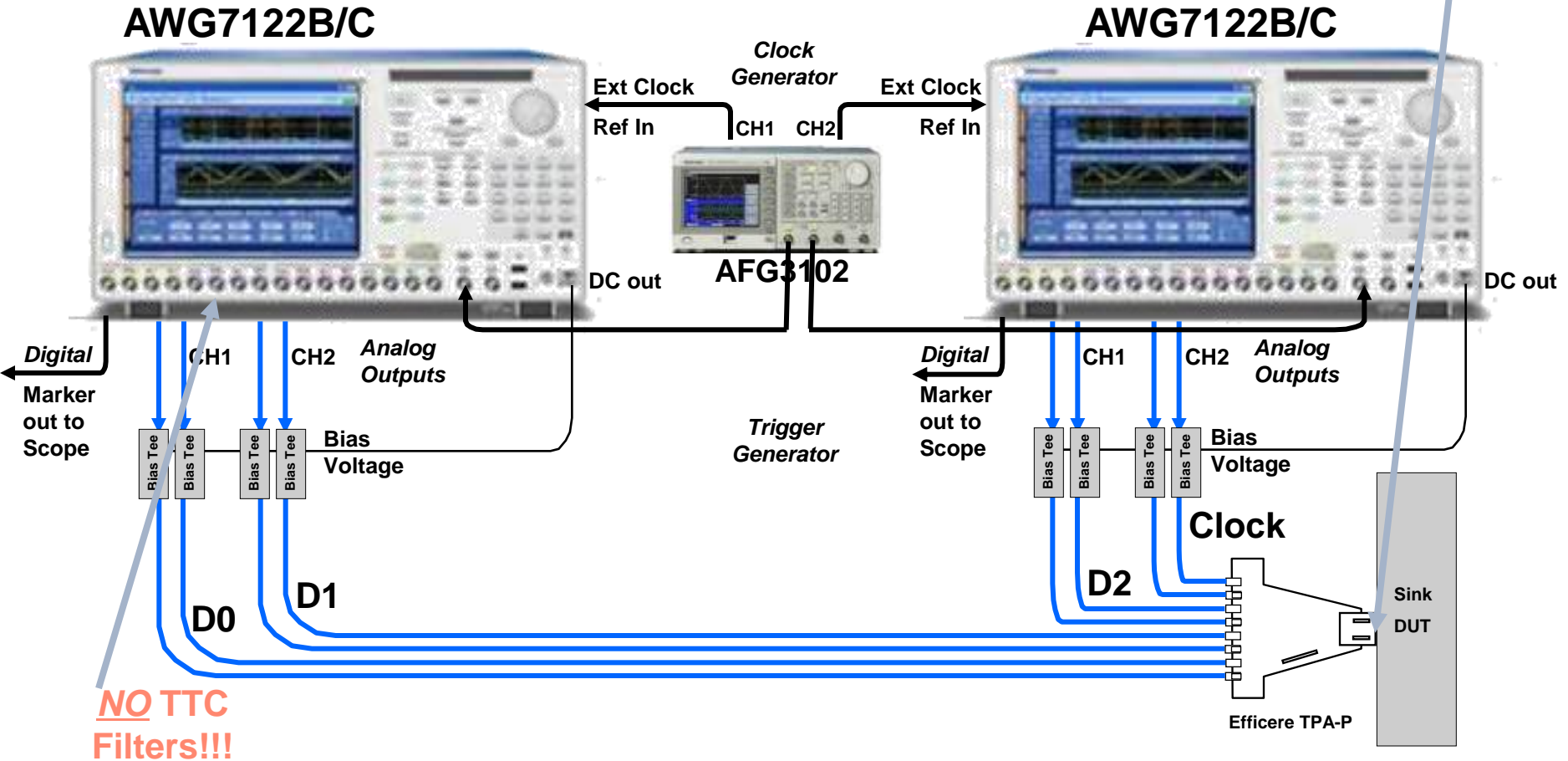
HDMI Sink Testing



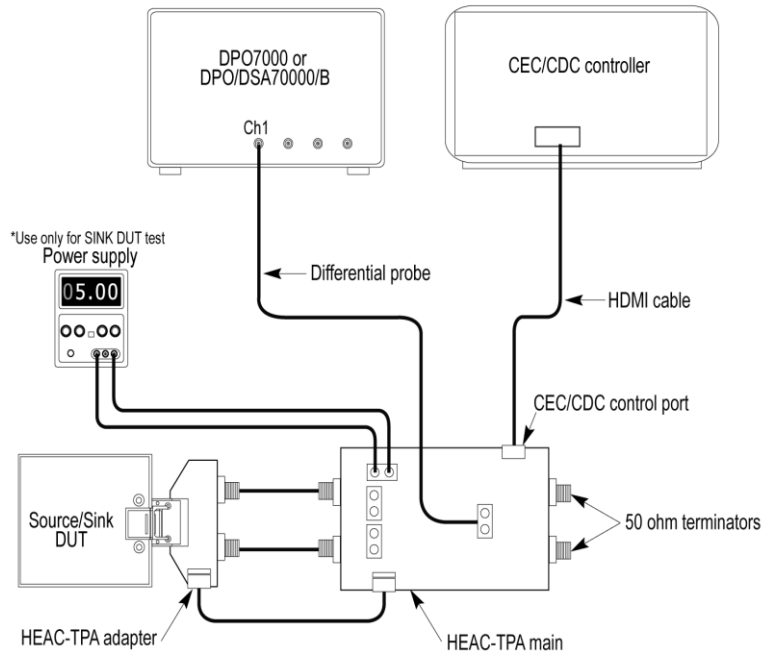
- **Jitter Tolerance**
- **Min/Max Differential Swing**
- **Intra-Pair Skew**
- **Differential Impedance**

HDMI 测试方案-接收端(TV/Monitor)

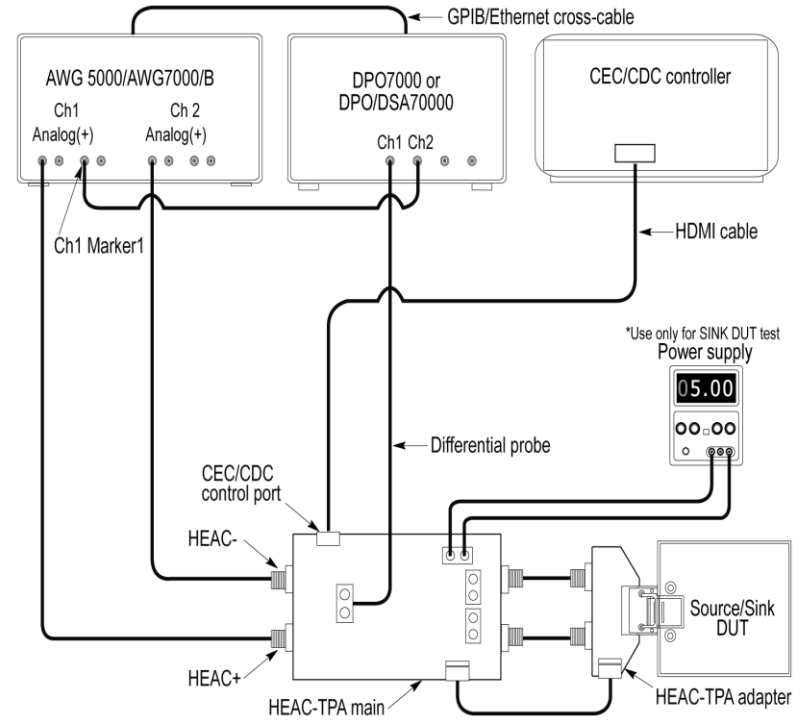
NO Cable Emulator!!!



HDMI 1.4 HEAC Solution Configuration



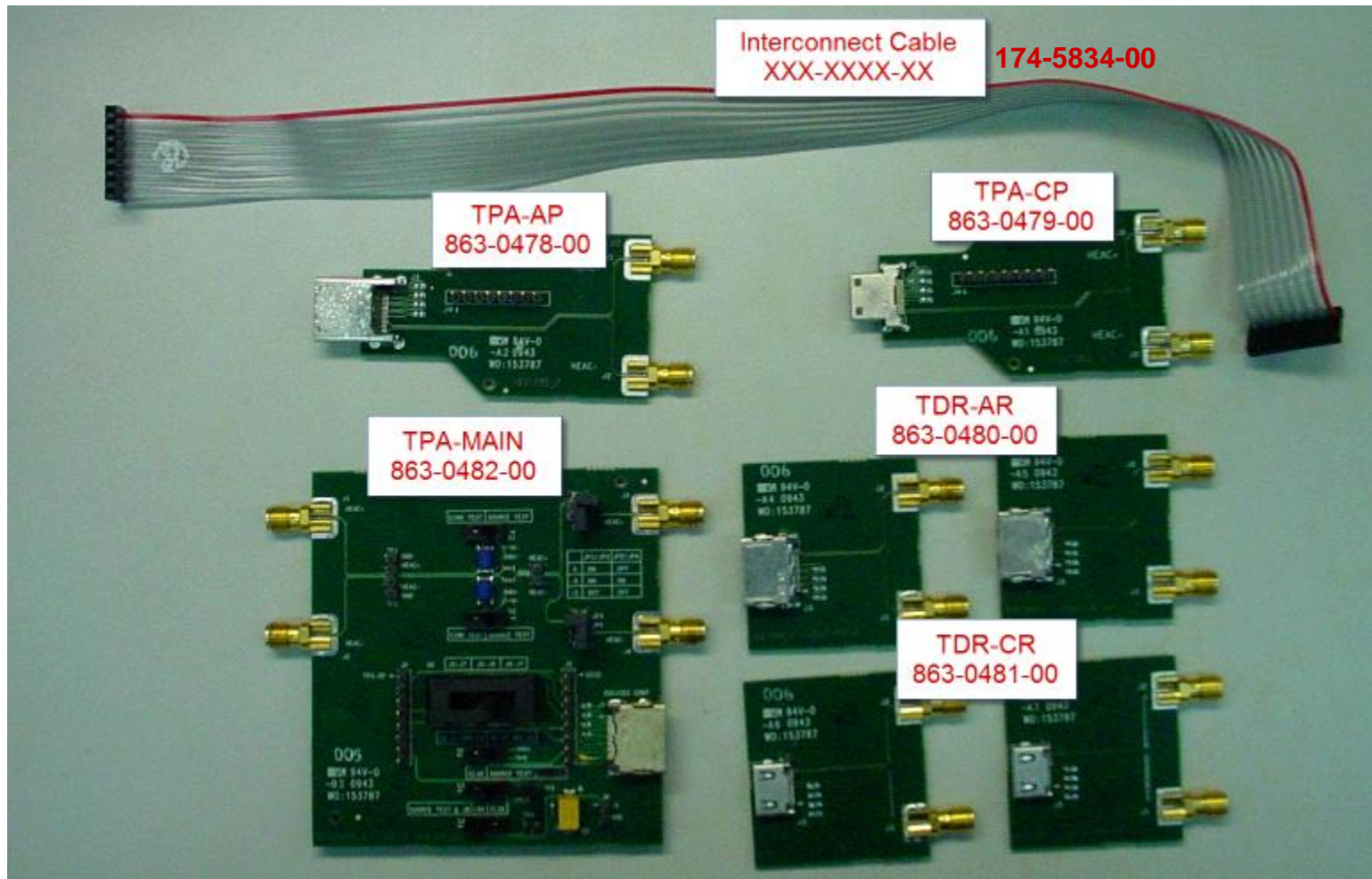
Tx Test Setup



Rx Test Setup

Tektronix HDMI 1.4a Test Solutions

HEAC Fixtures



HEAC Software

TekExpress HEAC Automated Solution (Evaluation Version) (Untitled)*

File View Tools Help

DUT ID: Run Stop

Select Acquire Analyze Report

Select Device

HEAC-Transmitter
 HEAC-Receiver

Select Test Suite

Differential-Rx
 CommonMode-Rx
 SingleMode-Rx

Version

CTS 1.4

DUT IP Address

Auto Detect MAC Address

HEAC-Receiver : Differential-Rx CTS 1.4

Select	Test Name
<input checked="" type="checkbox"/>	Receiver Performance - Nominal Response
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Amplitude
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Clock Frequency
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Common mode
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Signal Source Impedance
<input checked="" type="checkbox"/>	5.16 Receiver Performance - Worst Case Cable

Test Description

This optional test verifies the receiver capability to respond to nominal amplitude, clock frequency and

Configure

Show Schematic

Select All

Deselect All

TekExpress launched successfully.

Tektronix

Proposed HDMI 2.0 features-Not finalized

- Uses same Cat 2 Cable and HDMI 1.4b connector
- Support 4K 2K 4:4:4 60 Hz – 594Mhz
- Support 4K 2K 4:2:0 – 297Mhz
- Direct Attach device support
- Low level Bit error rate testing
- Scrambling is likely to be introduced for rates >340Mcps.

Rise time Needs

Table 4-24 Source AC Characteristics at TP1

Item	Value
Rise time / fall time (20%-80%)	<u>if attached Sink supports < 340MHz</u> <u>75psec ≤ Rise time / fall time</u> <u>if attached Sink supports ≥ 340MHz and transmitted TMD5 Character Rate ≥ 340MHz</u> <u>42.5psec ≤ Data Rise time / Data fall time</u> <u>75psec ≤ Clock Rise time / Clock fall time</u>

Table 4-30 TP7 Direct Attach AC Characteristics at 6Gbps

Item	Value
Rise time / fall time (20%-80%)	<u>if attached Sink supports ≥ 340MHz and transmitted TMD5 Character Rate ≥ 340MHz</u> <u>42.5psec ≤ Data Rise time / Data fall time</u> <u>75psec ≤ Clock Rise time / Clock fall time</u>

- HDMI 1.4b, should be capable of measuring 75 psec, but no word about the System Rise time.
- **HDMI 2.0 should be capable of measuring 42.5 psec, but no word about System Rise time.**
- The Error contribution of RT measurement due to System and DUT generally not accounted when we refer to specification

What is the system bandwidth needed to measure 42.5 (20-80%)psec or less DUT Rise time

- System bandwidth should be around $(42.5/1.5) = 28$ psec
- Scope bandwidth of 16 Ghz and 16 Ghz DSP enhanced probe has System Rise time of about 23 psec. It can measure the DUT Rise time of 42.5 psec with error of 1%. And can measure DUT Rise time of 37 psec with error of 7%.
- We can indicate Pass or fail confidently only when the System band. width is close to 16 Ghz scope .
- Is it fact for all scope vender ??
 - Spec says it should not be less than 42.5psec.
 - Max Rise time is limited by Eye diagram slope.
 - Both scope and Probe rise time cannot be less or equal to the DUT rise time because it can measure the signal rise time accurately only if DUT RT is slower than system rise time by 1.5 X times.
- How it is handled in HDMI 1.4b today???
 - We recommend 8Ghz scope and 13 Ghz probe, then system rise time is 38 psec which is close 2X faster than 75 psec

Conclusion

- 16GHz BW scope will give 1% error and hence is recommended for HDMI 2.0 testing.
- HDMI 2.0 RT/FT (20%-80%) data signals is 42.5ps

HDMI 2.0 Source Testing-Advanced information



Source Testing 1.4b Vs 2.0

Eye Diagram test is changed

Rest of the tests is same

1.4b CTS test is a pre-requisite for HDMI 2.0

Min 8GHz scope to 16GHz scope

Fixtures and Probes

Likely Source Electrical tests

Test ID HF1-1: Source TMDS Electrical – 340-600Mcsc – V_L

Test ID HF1-2: Source TMDS Electrical – 340-600Mcsc – T_{RISE} , T_{FALL}

Test ID HF1-3: Source TMDS Electrical – 340-600Mcsc – Inter-Pair Skew

Test ID HF1-4: Source TMDS Electrical – 340-600Mcsc – Intra-Pair Skew

Test ID HF1-5: Source TMDS Electrical – 340-600Mcsc – Differential Voltage

Test ID HF1-6: Source TMDS Electrical – 340-600Mcsc – Clock Duty Cycle

Test ID HF1-7: Source TMDS Electrical – 340-600Mcsc – Clock Jitter

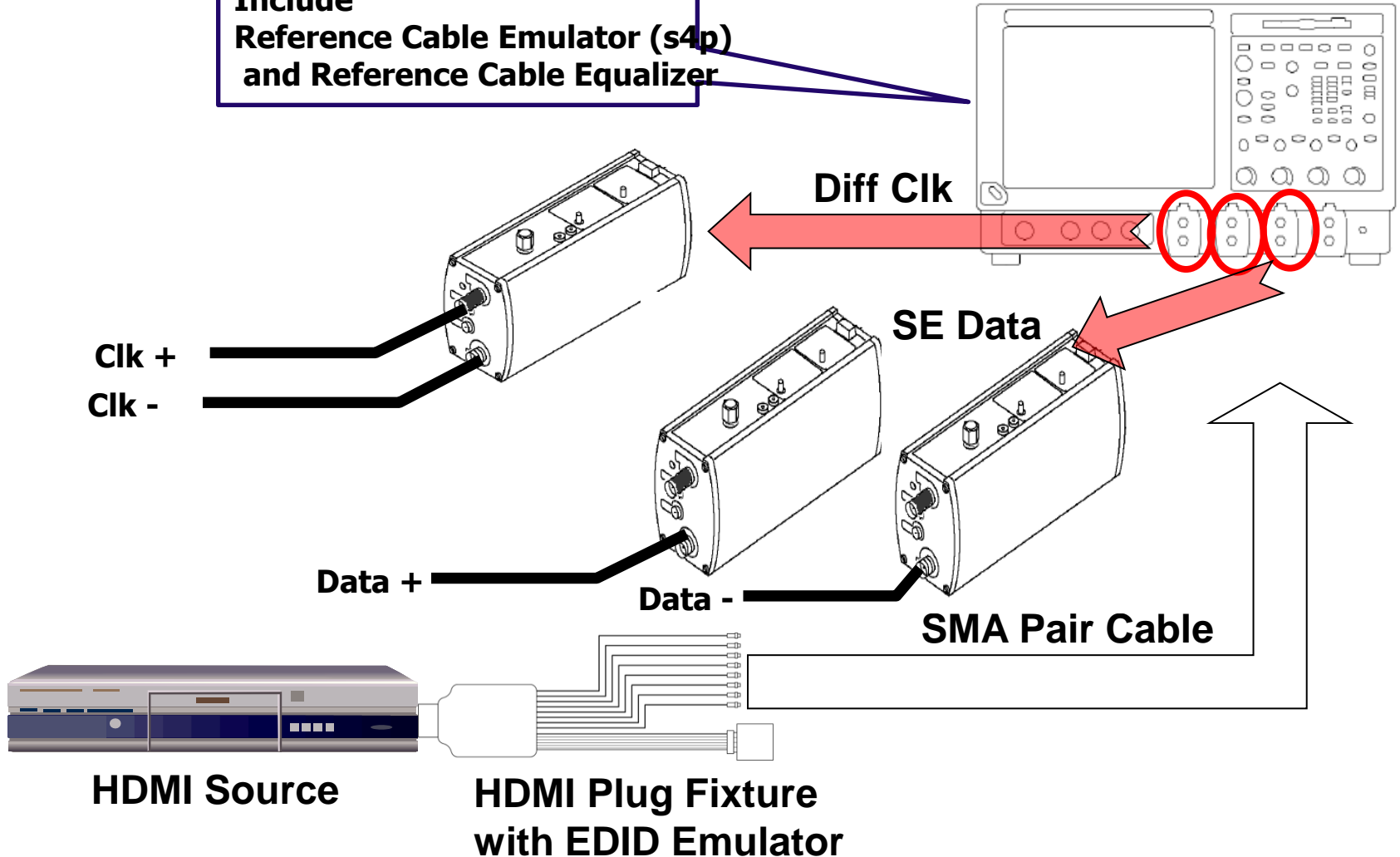
Test ID HF1-8: Source TMDS Electrical – 340-600Mcsc – Data Eye Diagram

Test ID HF1-9: Source TMDS Electrical – 340-600Mcsc – Differential Impedance

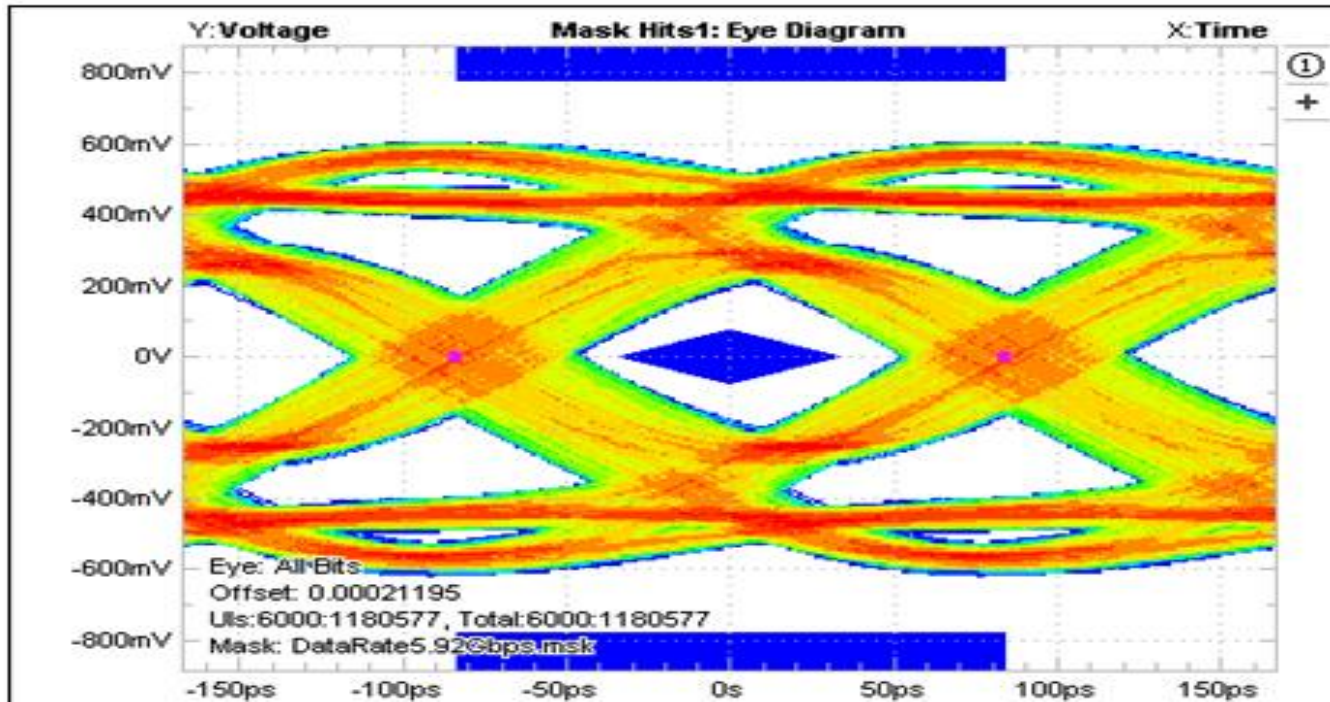
Source Eye Diagram Test

Tektronix Oscilloscope
DPO/DSA/MSO7000 Series
≥ 16GHz

Include
Reference Cable Emulator (s4p)
and Reference Cable Equalizer



TP2 Source Eye for HDMI 2.0 6G signal



Single End Input eye rendered at Tek lab

HDMI 2.0 Tx Compliance Software

TekExpress HDM - (Untitled)

Options

Start

Setup

1 DUT

DUT ID: DUT001

Device: HDM Physical Layer Solution

Suite: Source

Version: CTS 2.0

Acquire live waveforms

Use pre-recorded waveform files

View: Compliance

Device Profile

Termination Source: Internal

VTerm (V): 3.3

Diff Probe Attenuation (x): 12.5

SE Probe Attenuation (x): 2.5

TBIT: 0.0

Recalc TBIT

Number of Lanes to Test: 3 Lanes

Selected Test Lanes: ClockD0D1

Status Ready

TekExpress HDM - (Untitled)

Options

Start

Setup

2 Test Selection

HDM Physical Layer Solution : Source : CTS 2.0

Deselect All

Select All

- Differential
 - 1.2 TMDS TRise TFall
 - 1.3 TMDS Inter-Pair Skew
 - 1.5 TMDS ClockDutyCycle
 - 1.6 TMDS Clock Jitter
- Single Ended
 - 1.1 TMDS V Low
 - 1.4 TMDS Intra-Pair Skew
 - 1.7 TMDS DataEyeDiagram

Test Description

TMDS Rise Time and Fall Time measurement

Show MOI

Schematic

Configure

Status Ready

TekExpress HDM - (Untitled)

Options

Start

Setup

Status

Results

Reports

Test Status

Log View

Test Name	Acquisition	Acquire Status	Analysis Status
Clock			
1.2 TMDS TRise TFall	Short Record-length for Rise Fall	To be started	
1.5 TMDS ClockDutyCycle	Short Record-length for Clock Duty Cycle	To be started	
1.6 TMDS Clock Jitter	Short Record-length for Clock Jitter	To be started	
D0			
1.1 TMDS V Low	Short Record-length for VLow	To be started	
1.4 TMDS Intra-Pair Skew	Short Record-length for Intra-Pair Skew	To be started	
1.7 TMDS DataEyeDiagram	Short Record-length for Data Eye Diagram	To be started	
D1			
1.2 TMDS TRise TFall	Short Record-length for Rise Fall	To be started	
1.3 TMDS Inter-Pair Skew	Short Record-length for Inter-Pair Skew	To be started	
1.1 TMDS V Low	Short Record-length for VLow	To be started	
1.4 TMDS Intra-Pair Skew	Short Record-length for Intra-Pair Skew	To be started	
1.7 TMDS DataEyeDiagram	Short Record-length for Data Eye Diagram	To be started	

Status Ready

TekExpress HDM - (Test Results)

Options

Start

Setup

Status

Results

Reports

Overall Test Result

Test Name	Details	TBit	Value	Units	Pass/Fail	Margin
1.2 TMDS TRise TFall	Clock Rise Time	168.3498 ps	38.7089	ps	Fail	-36.2911
1.2 TMDS TRise TFall	Clock Fall Time	168.3498 ps	38.1015	ps	Fail	-36.8985
1.5 TMDS ClockDutyCycle	Maximum Duty Cycle	168.3498 ps	50.01	%	Pass	-9.99
1.5 TMDS ClockDutyCycle	Minimum Duty Cycle	168.3498 ps	49.99	%	Pass	9.99
1.6 TMDS Clock Jitter	TMDS Clock Jitter	168.3498 ps	40.1239	ps	Pass	-1.9635
1.6 TMDS Clock Jitter	TMDS VSwing	168.3498 ps	64.7812	mV	Fail	-335.22 & 1135.22
1.1 TMDS V Low	TMDS VLow for	168.3498 ps	3.2822	V	Fail	0.9822 & -0.1822
1.1 TMDS V Low	TMDS VLow for	168.3498 ps	3.1738	V	Fail	0.8738 & -0.0738
1.4 TMDS Intra-Pair Skew	TMDS Intra-Pair Skew for Clock	168.3498 ps	9.7096	ps	Pass	-15.5429
D0						Fail
1.2 TMDS TRise TFall	D0 Rise Time	168.3498 ps	60.6379	ps	Pass	18.1379
1.2 TMDS TRise TFall	D0 Fall Time	168.3498 ps	58.5778	ps	Pass	16.0778
1.1 TMDS V Low	TMDS VLow for	168.3498 ps	3.1720	V	Fail	0.8720 & -0.2720

Status Ready

Tektronix HDMI Protocol Analyzer

TEK-PGY HDMI/MHL Protocol Analysis solution - Beta

Mode: **HDMI** (selected), MHL

Displays:

- Image Viewer
- Protocol Viewer
- Bus Viewer
- Event Viewer
- Data Packet Viewer

List Of Tests:

- Source Protocol Tests
 - 7-16 Legal Codes
 - 7-17 Basic Protocol
 - 7-18 Extended Control Period
 - 7-19 Packet Types
- Source video
- Source audio
 - 7-28 IEC 60958/IEC 61937
 - 7-29 ACR
 - 7-30 Audio Sample Packet Jitter
 - 7-31 Audio InfoFrame
 - 7-32 Audio Sample Packet Layout
- Source interoperability with DVI

Buttons: Select, Configure, View, Capture, Clear All, Select All, Run (Single, Repetitive, No Acq), Analyze, Export, Report

Version: 0.8.0

TEK-PGY HDMI/MHL Protocol Analysis solution - Beta

Signal Source:

- Oscilloscope
- Wfm Files
- P/A/V Binary File

Signal Assignment:

Clock	CH1
Data 0	CH2
Data 1	CH3
Data 2	CH4

Video Format:

Pixel Encoding: RGB

Bits Per Pixel: 24 Bits

Format: 3D-Side by Side

(2) - 720x480 @ 60 Hz

Source_CN: Not Specified

Non CEA Format | AVI Supported

Audio Sample Frequency: 32 kHz

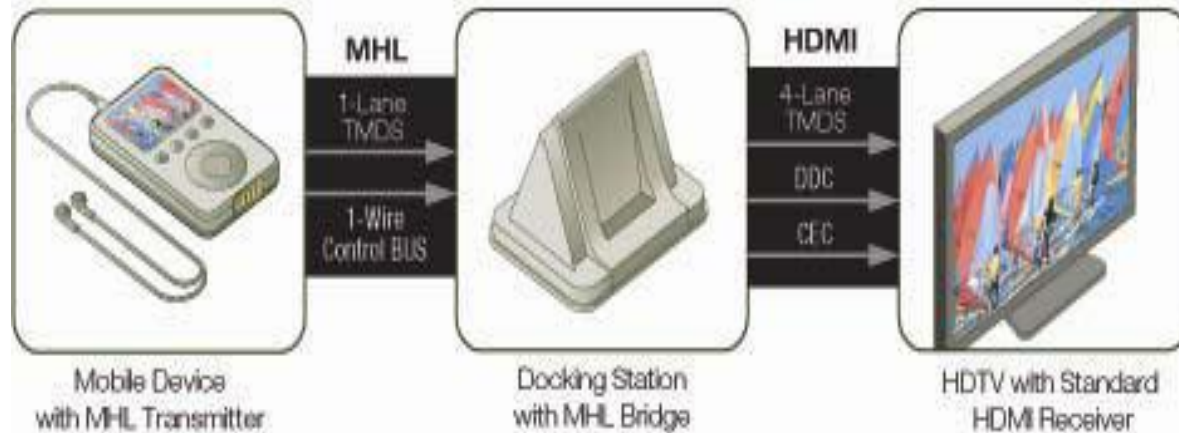
Channel Inversion:

- Invert Data 0
- Invert Data 1
- Invert Data 2

Buttons: Select, Configure, View, Capture, Run (Single, Repetitive, No Acq), Analyze, Export, Report

Version: 0.8.0

MHL Introduction



Source: MHL.org

- **Mobile HD Link (MHL) technology is a low pin count HD audio and video interface that connects portable electronics devices such as mobile phones, digital cameras, camcorders and portable media players, to HDTVs.**
- **The technology allows mobile devices to output digital 1080 Full HD resolution via the existing mobile connector without the real estate and cost of another dedicated video connector.**
- **Together with an MHL-to-HDMI bridge, the MHL-enabled mobile device becomes a fully compliant HDMI source and can connect to the television's standard HDMI input port.**

MHL Introduction

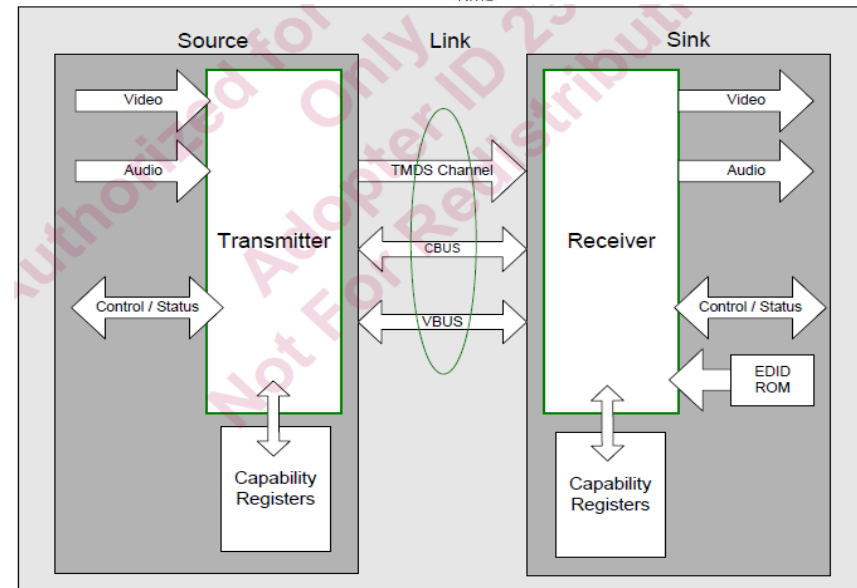
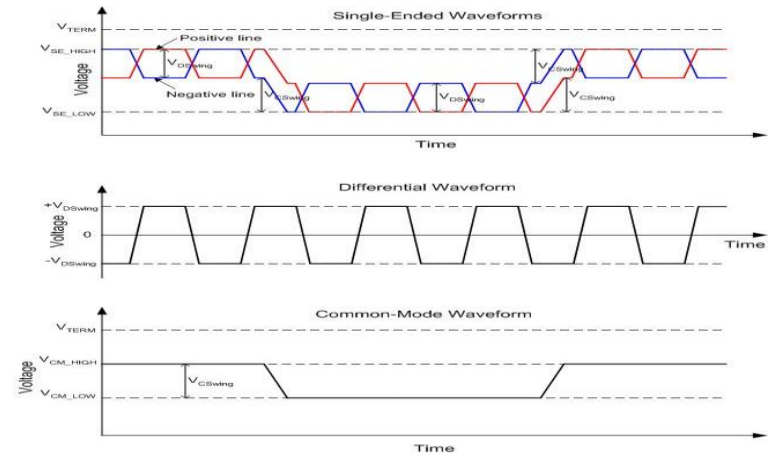
- MHL Consortium was formed in Sept 2009 with the following founding members:
 - NOKIA
 - SAMSUNG
 - Silicon Image
 - Sony
 - Toshiba
- The Specification 1.1 version was announced in Q12011 , Specification 1.2 in Dec 2011, Specification 2.0 in Feb 2012 and Specification 2.1 NOW.

The Consortium released CTS 1.1 version in June 2011, CTS 1.2 in Jan 2012, CTS 2.0 in Sept 2012 and CTS 2.1 is just announced.

COMPLETE TEKTRONIX SOLUTION APPROVED in CTS1.1 , CTS 1.2 , CTS 2.0 and CTS 2.1 solution

- Tektronix is a Contributor adopter and actively involved in defining the CTS 2.1.

MHL Customer Presentation



Source: MHL 1.2 specification document

Tektronix MHL 2.1 Tx Solution with Direct Attach test support

The screenshot displays the TekExpress MHL software interface. The main window is titled "TekExpress MHL - (Untitled)*" and includes an "Options" dropdown in the top right corner. On the left side, there is a vertical navigation menu with four items: "1 DUT", "2 Test Selection" (marked with a green checkmark), "3 Acquisitions", and "4 Preferences". Below this menu are four buttons: "Setup", "Status", "Results", and "Reports".

The main configuration area contains the following fields and options:

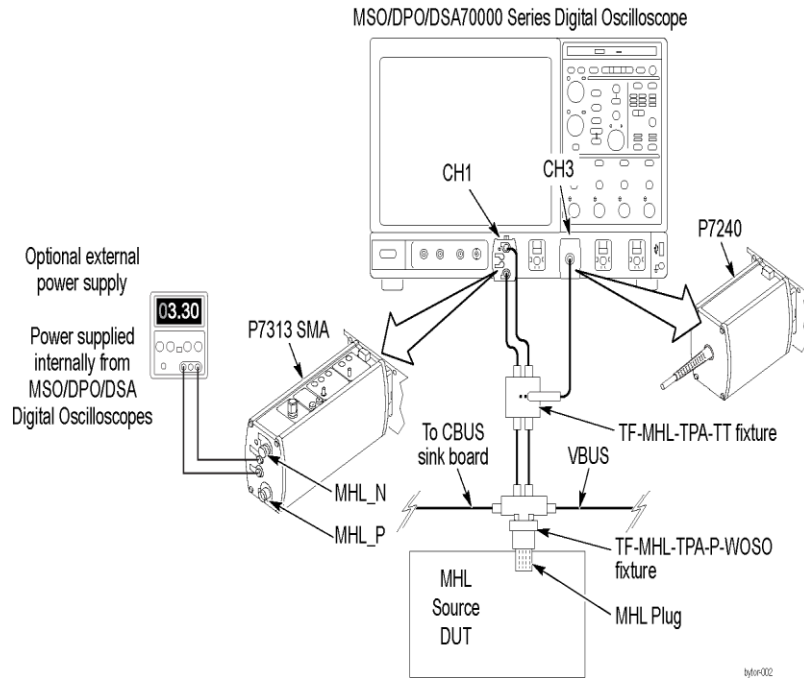
- DUT ID:** DUT001
- Device:** MHL Physical Layer Solution
- Suite:** MHL Transmitter
- Version:** CTS 1.3/2.1
- Acquire live waveforms:** (Selected)
- Use pre-recorded waveform files:**
- View:** Compliance

The **Device Profile** section is divided into several sub-sections:

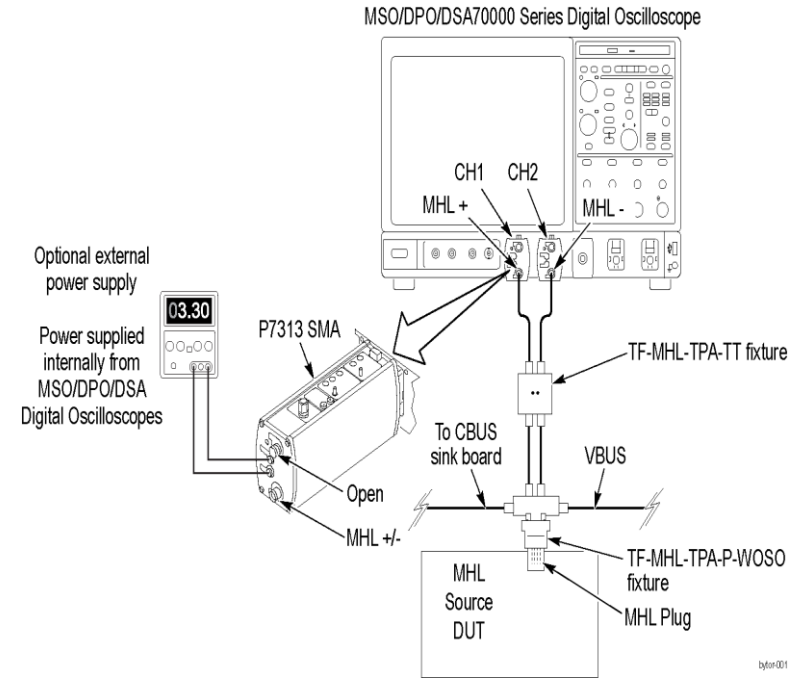
- Pixel Mode:** Both (Selected), Direct Attach
- Termination Source:** Internal
- 24 Bits:**
 - Low Data Rate (Gbps): 0.75
 - High Data Rate (Gbps): 2.22
- Packed Pixel:**
 - High Data Rate (Gbps): 2.97
- VTerm:**
 - Min (V): 3.135
 - Max (V): 3.465
- Compensation Factor:**
 - MHL+: 1.2
 - MHL-: 1.2
- Signal Threshold:**
 - Min(mv): 250

At the bottom left, the status bar shows "Status Ready". On the right side of the interface, there are three control buttons: "Start" (a green circular button with a refresh icon), "Pause" (a grey button with a pause icon), and a close button (an "X" icon).

Tektronix MHL Tx Setup



MHL Differential and CM Test Setup
7 tests



Single Ended and Intra Pair Skew Test Setup
3Tests

Also same setup is used for MHL Protocol Testing

**** C-Bus Sink and Source Board is needed for hand shaking and is available from Simplay Labs**

MHL 2.1 Compliance Software for Automated Tx Tests: Option MHD

The screenshot displays the TekExpress MHL software interface. The main window title is "TekExpress MHL - (Untitled)". On the left, a vertical navigation bar shows four steps: 1. DUT (checked), 2. Test Selection (highlighted), 3. Acquisitions, and 4. Preferences. Below this are buttons for "Setup", "Status", "Results", and "Reports".

The central panel is titled "MHL Physical Layer Solution : MHL Transmitter : CTS 1.3/2.1". It contains a tree view of test items, each with a checkmark:

- MHL Clock
 - 3.1.1.1 Standby Output Voltage-VOFF
 - 3.1.1.5 Common-mode Output Swing Voltage-V_CMSWING (Low)
 - 3.1.1.7 Common-mode Rise and Fall Times-TR_CM, TF_CM (High)
 - 3.1.1.10 MHL Clock Duty Cycle in Normal Mode (High)
 - 3.1.1.14 MHL Clock Duty Cycle in PackedPixel Mode (High)
 - 3.1.1.17 TP2 Clock Jitter in Normal Mode (Low, High)
 - 3.1.1.19 TP2 Clock Jitter in PackedPixel Mode (High)
- MHL Data
 - 3.1.1.2 Single-ended High Level Voltage-VSE_HIGH (Low)
 - 3.1.1.3 Single-ended Low Level Voltages-VSE_LOW (Low)
 - 3.1.1.4 Differential Output Swing Voltage-VDF_SWING (Low)
 - 3.1.1.6 Differential Rise and Fall Times-TR_DF, TF_DF (High)
 - 3.1.1.18 TP2 Eye Diagram in Normal Mode (Low, High)
 - 3.1.1.20 TP2 Eye Diagram in PackedPixel Mode (High)

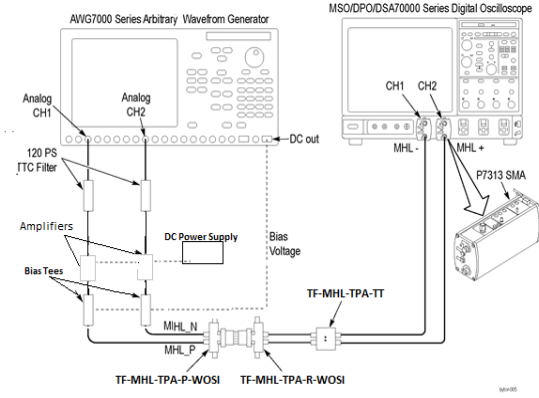
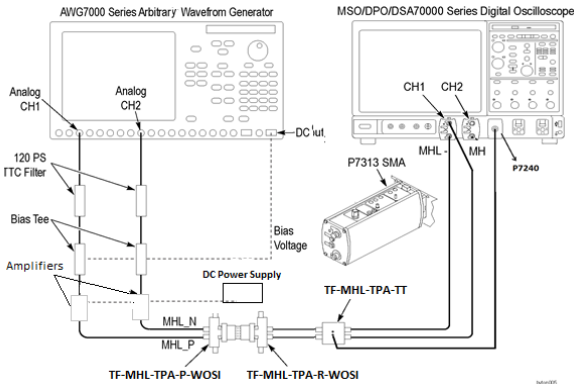
Buttons for "Deselect All" and "Select All" are located above the tree view. Below the tree view is a "Test Description" section with the text: "This test confirms that common-mode output voltage swing amplitude is within the specified limits when the source device operates in normal mode." To the right of the description are "Schematic" and "Configure" buttons.

On the right side of the interface, there are "Start" and "Pause" buttons. The "Start" button is green with a circular arrow icon, and the "Pause" button is grey with a double vertical bar icon. A "Status Ready" indicator is visible at the bottom left.

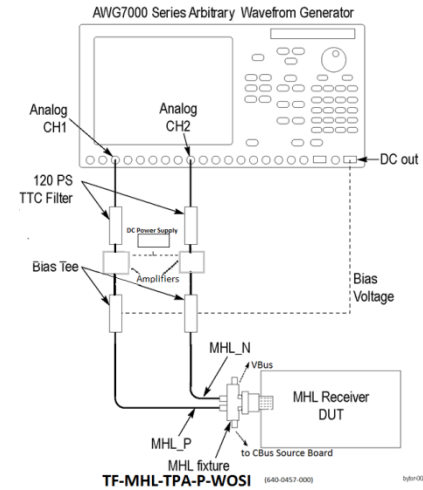
Tektronix MHL Solution Setup: Simple and Easy Sink and Dongle Min/Max Testing -2

Setup based on Direct Synthesis Capability of AWG7122C Series

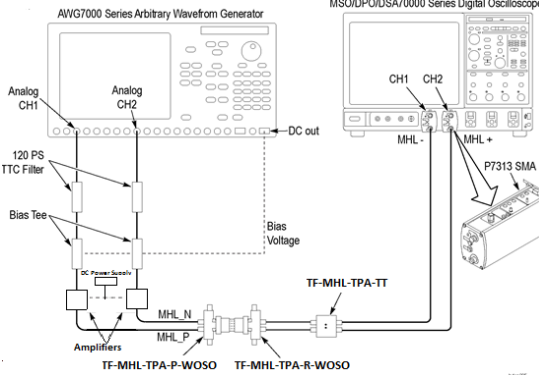
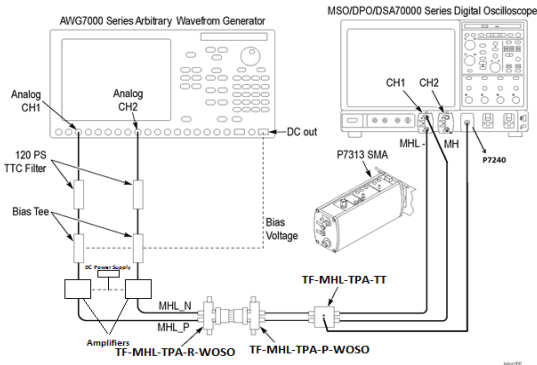
AWG Sink Min/Max Signal (CM,SE and Diff) Verification Using Real Time Oscilloscope



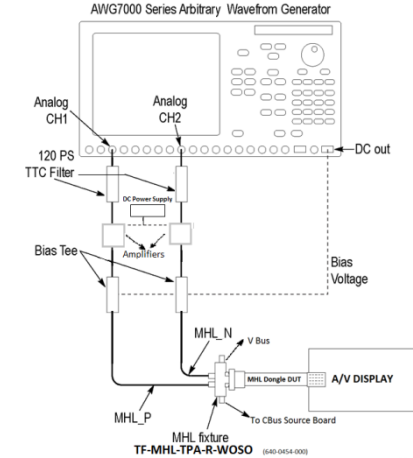
Test Setup for Sink Min/Max Tests



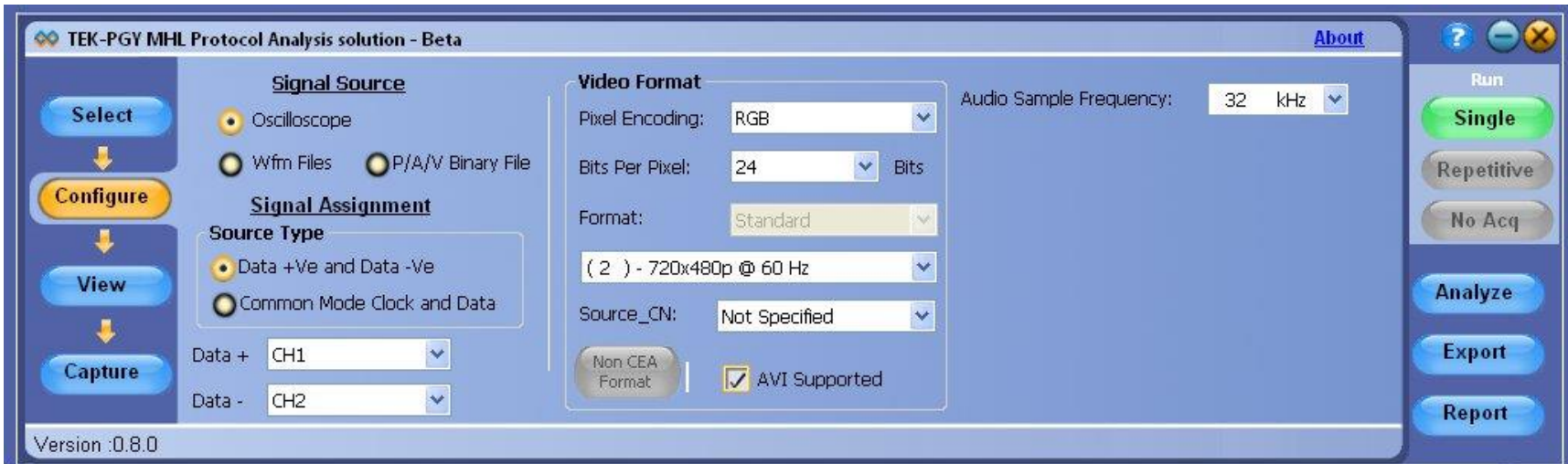
AWG Dongle Min/Max Signal (CM,SE and Diff) Verification Using Real Time Oscilloscope



Test Setup for Dongle Min/Max Tests

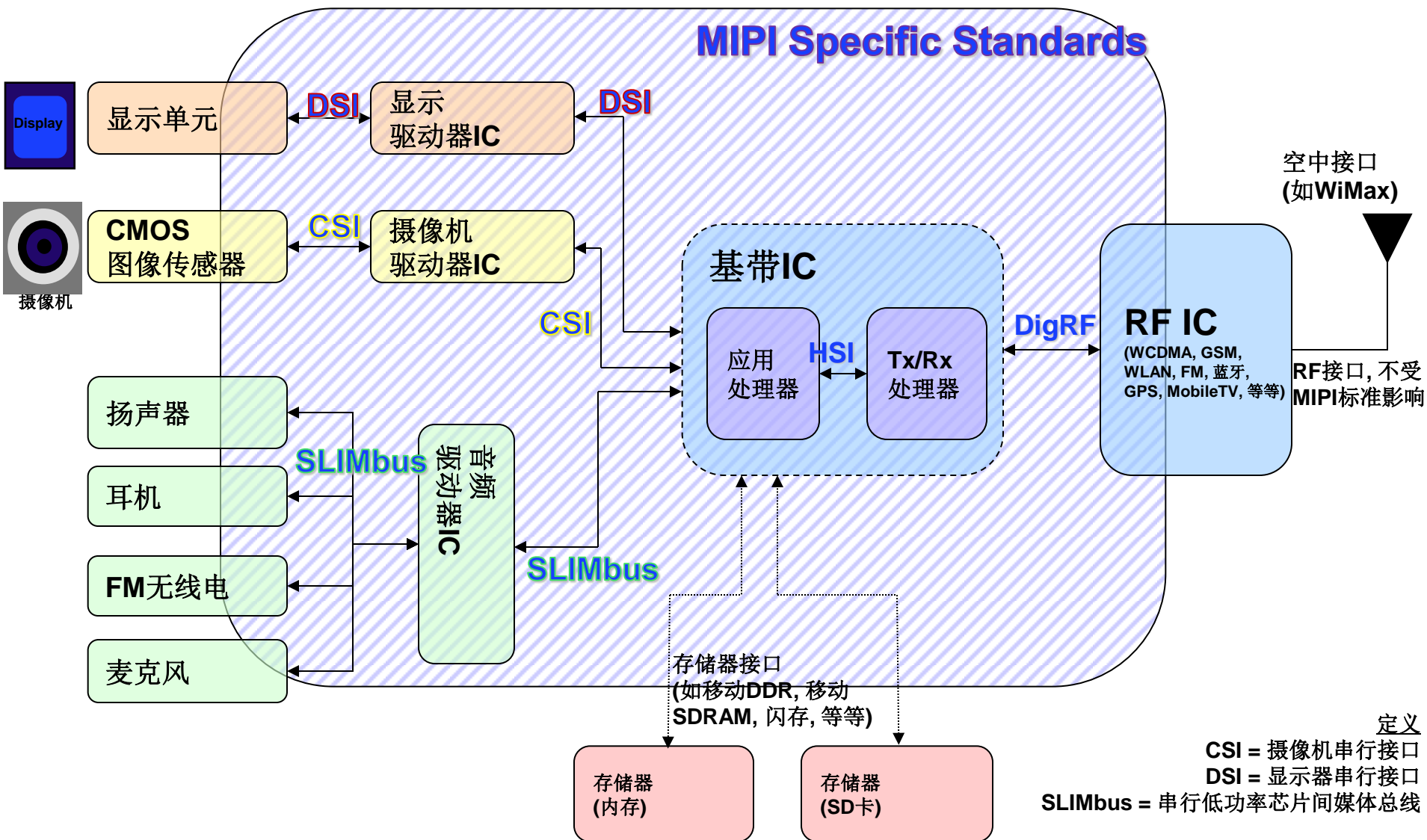


Tektronix MHL Protocol Analyzer



MIPI标准概述

移动终端方框图实例



D-PHY Tx测试解决方案 – 续

■ 示波器

- 推荐: **DPO7354或DPO/DSA/MSO70404/B**
 - 用来测量规范 $\pm 5\%$ 误差范围内的上升时间(150ps)
 - 如果不考虑上升时间的测试, 可以使用DPO7254

■ 探头

- 探头考虑因素

- 同时测量单端性能和差分性能
- 动态范围必须 $>1.2V$
- 探头衰减要达到最小
 - 1X最好, 2.5X或5X也行

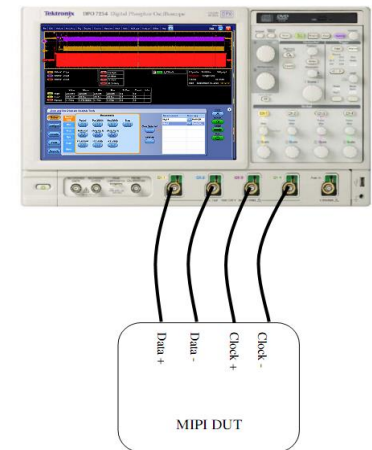
- 推荐:

- **DPO7000**采用四只**TAP3500**; **MSO/DPO/DSA70000/B**采用四只**P7240**
- (Ch1: D+), (Ch2: D-), (Ch3: Clk+), (Ch4: Clk-)
- TAP2500也适合低数据速率的DUT

- 也可以使用:

- 焊接式探头

- **DPO7000**采用**TDP3500**, **70000**系列采用**P73xx**
- (Ch1: D+, Gnd), (Ch2: D-, Gnd), (Ch3: Clk+ & Clk-)



New Opt.D-PHYTX

- Opt.D-PHYTX : D-PHY Automated Solution

- TekExpress option for Fully-Automated testing
- Automation similar to Opt.USB-TX
- Provides Conformance and Characterization Testing
- Based on D-PHY Base Spec v1.0 and UNH's Conformance Test Suite v0.98.
- Runs on DPO7000, DPO/DSA/MSO70000/B Series oscilloscopes

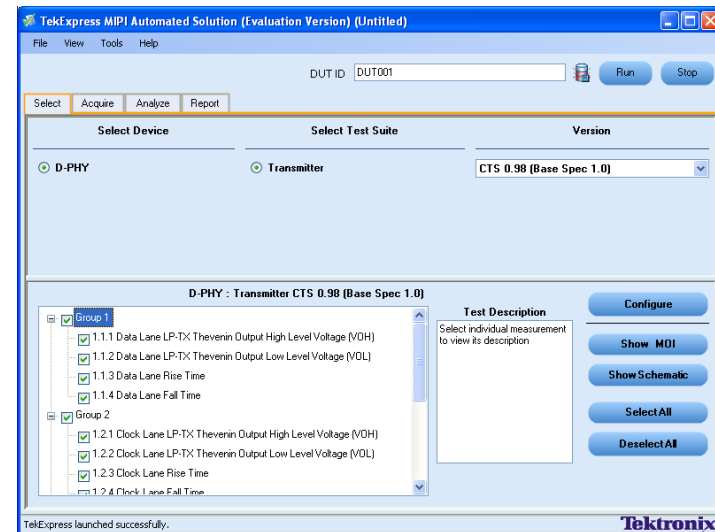
- Opt.TEKEXP is Pre-Requisite

- Differentiation

- Un-parallel Automation (Auto-Cursors/ Regions)
- For Conformance testing to Latest CTS (v0.98)
- Based on Latest Base spec (v1.0)

- Value proposition

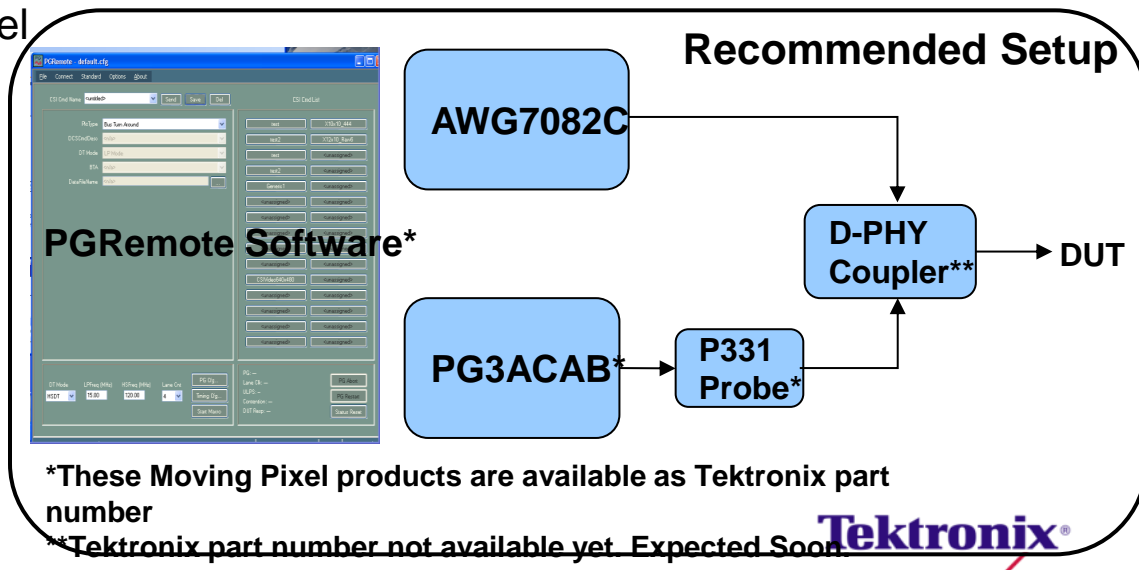
- Custom-limits/ Limits-Editing on the fly
- Test Reports
 - Zoom-in waveform captures at the Cursors/ Regions
 - Pass/Fail Summary with Margin details
- Tek 3.5GHz scope is the minimal configuration for accurate testing
 - i.e. unlike Agilent 4G scope at entry-level



D-PHY Rx : Test Solution Overview

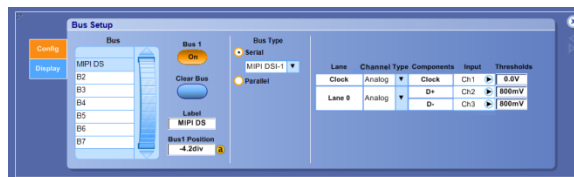
Simple, Quick, Easy and Re-usable

- 100% Coverage to Rx CTS
 - Meets all the requirements in UNH-IOL CTS document (v0.98)
- Quick and Easy setup
 - No complex VXI system, just stand alone instruments, and a probe.
- Cost effective solution
 - 70% Lower list price vs Competition
- Re-usable for Protocol tests
 - PG3A is the Only 4 channel solution for CSI & DSI test
- PG3A Pattern Generator
 - Controls clock and signaling to establish link with DUT
 - Adjusts voltage levels, packet type, etc to stress test receiver
- AWG7082C Generator
 - Adds jitter and interference to the D-PHY signals



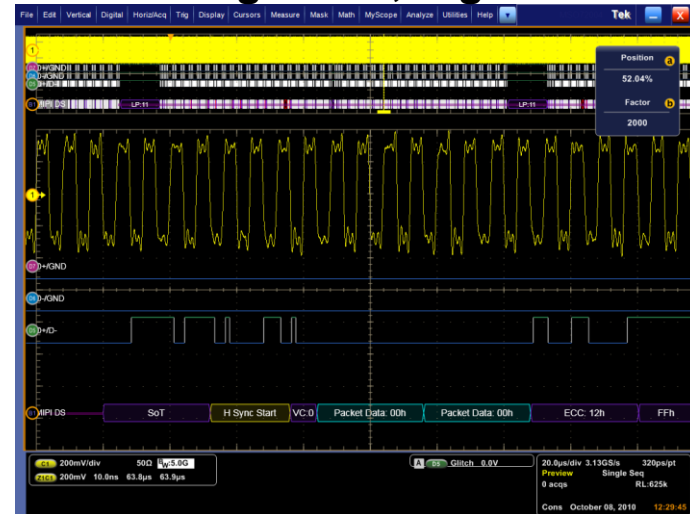
D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode Simultaneous Acquisition

- Probe using Analog, Digital or Mixed Channels
- Simultaneous probing of DSI & CSI using MSO channels
- Working on multi-lane support, using high performance MSO digital channels
- Supported on all 7KC, 70KC and MSO70K scopes. (**Win7-OS only**)
 - Option key bit #25
- Software installed as part of TekScope firmware v6.1.2.4 or later.
 - Browse to TekScope Menu --> Vertical --> Bus Setup --> Select Bus Type as Serial--> Select MIPI DSI or CSI from the drop down list.



Probe using Mixed Channels

Analog Clock, Digital Data

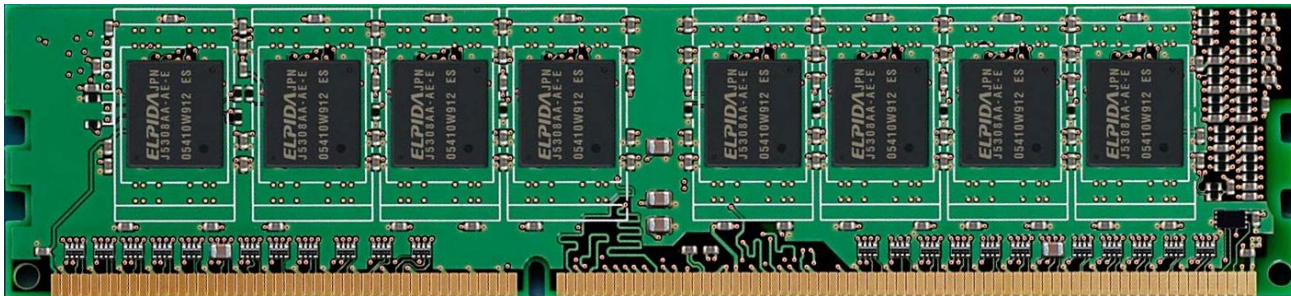


Digital Clock, Analog Data



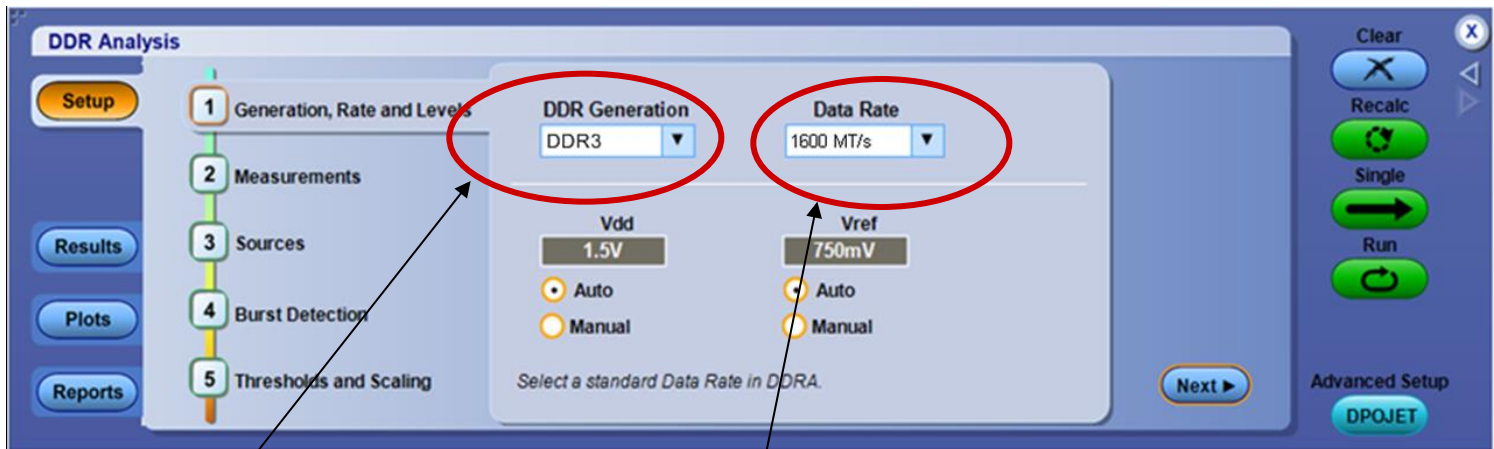
Memory Technology – Quick Overview

- DRAM - dominant memory technology
 - Computer system memory
 - Server, desktop, laptop
 - Dynamic, volatile memory, plug-in DIMMs
 - Embedded systems
 - Cell phones, printers, cars
 - Fixed memory configuration
 - DRAM driven by faster processors, faster data rates
 - DDR3 now available at 1600 (1.6Gb/s) data rates
 - DDR3 2000 emerging soon (overclocked)
- DRAM variants
 - LPDDR – Low Power DDR
 - Power savings for portable computing
 - GDDR – Graphic DDR
 - Optimized for Speed - faster access



Automated Test Setup

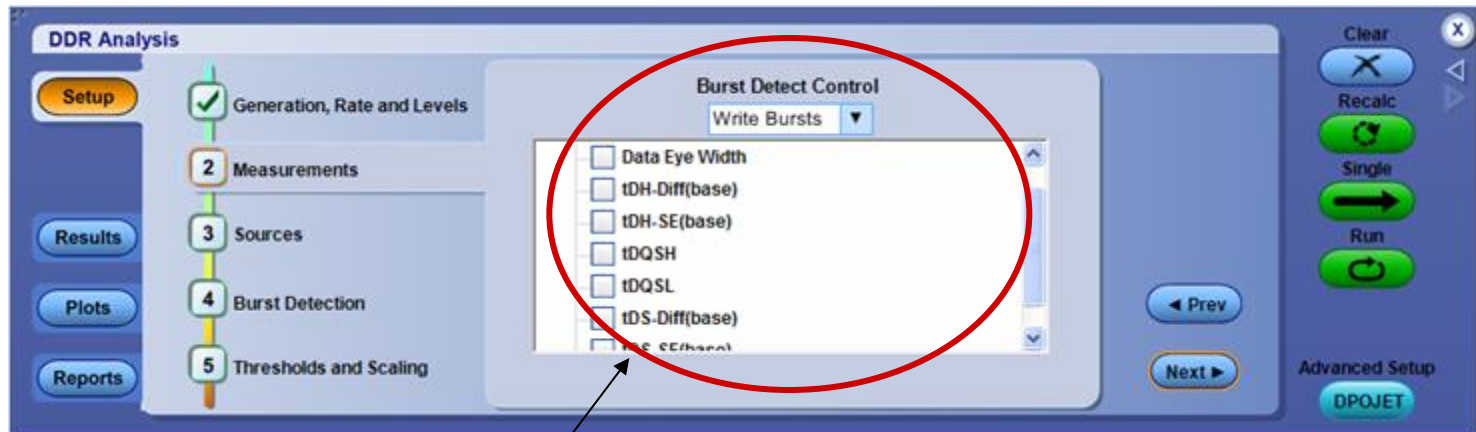
Step #1



Select DDR Generation

Select DDR Rate

Step #2



Choose measurements (Read / Write / CLK / Addr & Command)

Effective Reporting / Archiving

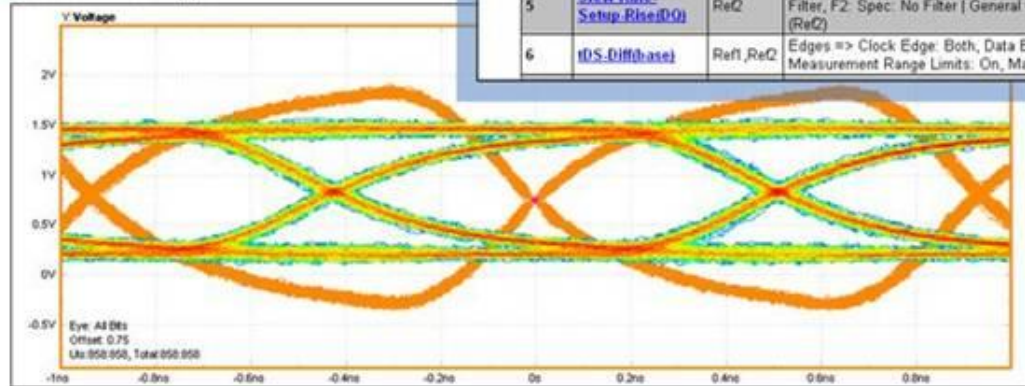
Measurement	tDOSH
Source1	DQS(Ref1)
	Value High Limit Low Limit Pass Fail
Min	928.86ps 1.8150ns 843.75ps Pass
Max	974.29ps 1.8150ns 843.75ps Pass

Pass/Fail Information

Measurement	tDOSL
Source1	DQS(Ref1)
	Value High Limit Low Limit Pass Fail
Min	900.00ps 1.8150ns 843.75ps Pass
Max	940.44ps 1.8150ns 843.75ps Pass

Plot Images

Measurement Plot(s)



Jitter and Eye Diagram Analysis Tools : Measurement Report

Enabling Innovation

October 16, 2009 10:17:54 AM

- Configuration
 - Setup Configuration

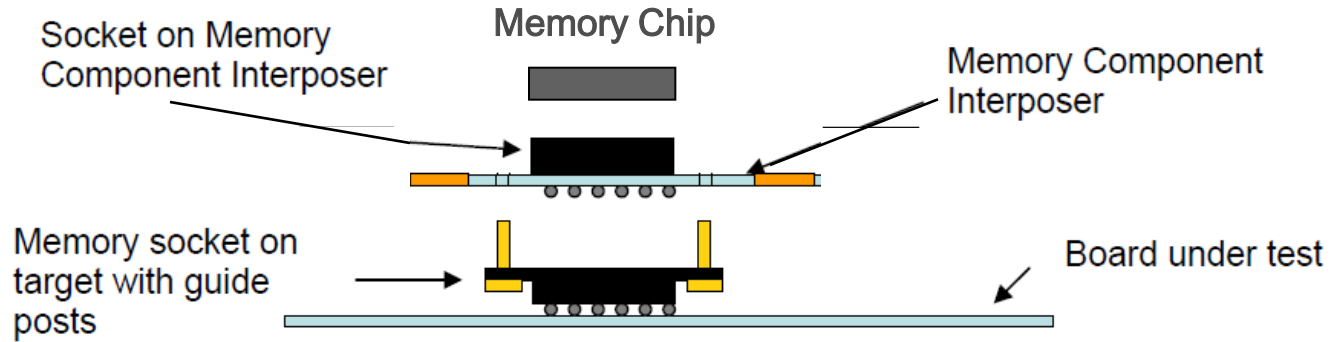
Oscilloscope Version 4.3.6 Build 5

DPOJET Version 2.4.0 Build 41

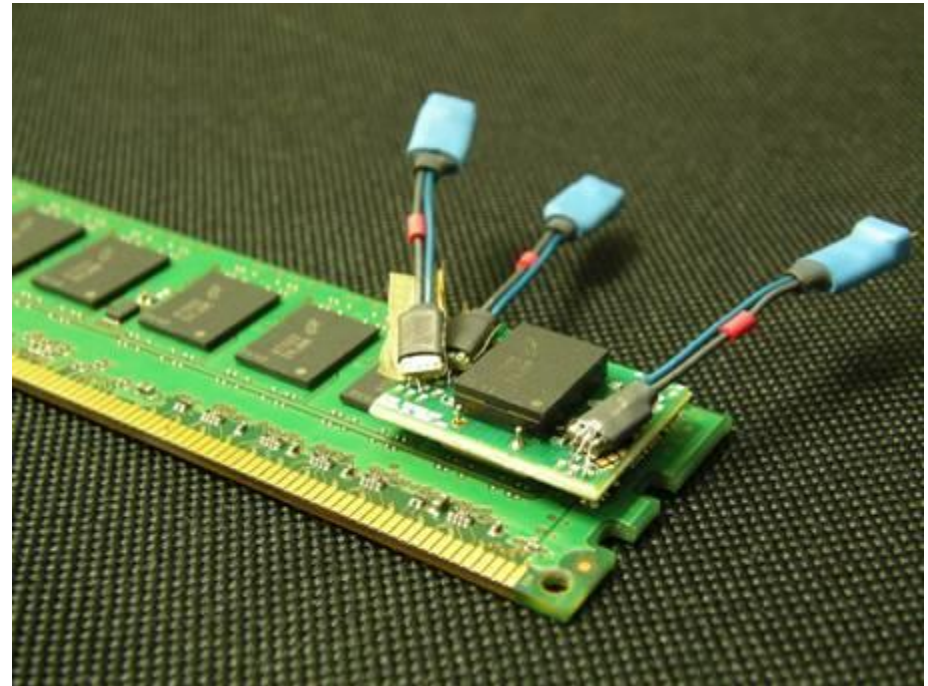
Status Pass
- Measurement Configuration

Index	Measurement	Source(s)	Others
1	Data Eye Height	ReQ,Ref1	Bit Config => Bit Type: All Bits Clock Recovery => Method: Explicit Clock - Edge, Clock Source: Ref1, Clock Edge: Both, Clock Multiplier: 1, Clock Offset Selection Type: Manual, Clock Offset: 469.04ps; Recalculation Type: When required General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(ReQ), DQS(Ref1)
2	Slew Rate Hold-Fall(DQ)	ReQ	Edges => From Level: High, To Level: Mid, Slew Rate Technique: DDRSlewrateTechnique Filters => F1: Spec: No Filter, F2: Spec: No Filter General => Measurement Range Limits: Off, Max: 0s, Min: 0s, Custom Source Name: DQ(ReQ)
3	Slew Rate Hold-Rise(DQ)	ReQ	Edges => From Level: Low, To Level: Mid, Slew Rate Technique: DDRSlewrateTechnique Filters => F1: Spec: No Filter, F2: Spec: No Filter General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(ReQ)
4	Slew Rate Setup-Fall(DQ)	ReQ	Edges => From Level: Mid, To Level: Low, Slew Rate Technique: DDRSlewrateTechnique Filters => F1: Spec: No Filter, F2: Spec: No Filter General => Measurement Range Limits: Off, Max: 0s, Min: 0s, Custom Source Name: DQ(ReQ)
5	Slew Rate Setup-Rise(DQ)	ReQ	Edges => From Level: Mid, To Level: High, Slew Rate Technique: DDRSlewrateTechnique Filters => F1: Spec: No Filter, F2: Spec: No Filter General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(ReQ)
6	tDS-Diff(base)	Ref1,ReQ	Edges => Clock Edge: Both, Data Edge: Both Filters => F1: Spec: No Filter, F2: Spec: No Filter General => Measurement Range Limits: On, Max: 938ps, Min: 0s, Custom Source Name: DQS(Ref1), DQ(ReQ)

Installation Process



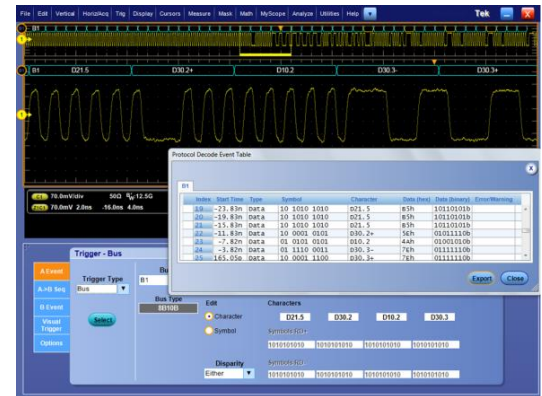
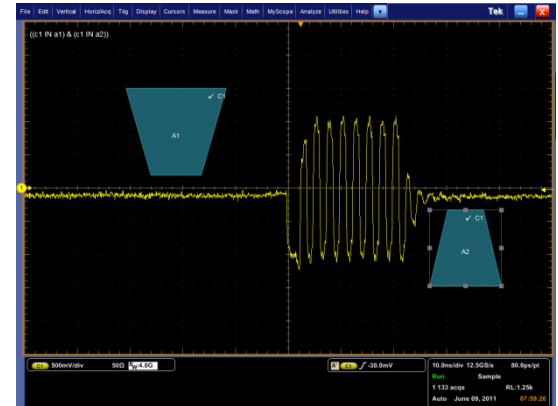
BGA Chip Interposer for Oscilloscopes



- Available in socket and solder-in versions
 - Socket design allows for multiple chip exchanges
 - Solder-in best for single use
- Recommended probes: P7500 Series
 - P7504, P7506, P7508, P7513A
 - 020-3022-00 TriMode solder tips for Nexus Interposer

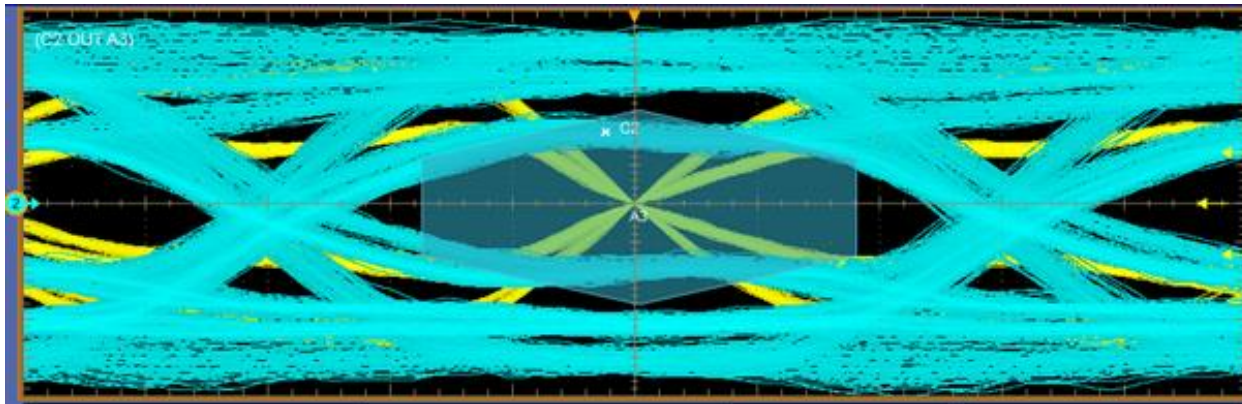
Visual Trigger and Serial Decode

- Next generation designs have less margin and additional analysis must be done to pinpoint in on pattern dependent issues
 - **NEW!** Visual Trigger qualifies hard to define trigger events
 - 8 customizable shapes for capture of real signal behaviors
- Electrical and Logic layer are merging and requires simultaneous analog and protocol views
 - **NEW!** 8b/10b Serial Decode
 - Trigger or Search on decoded traffic
 - Compare to analog views to speed up time to answer



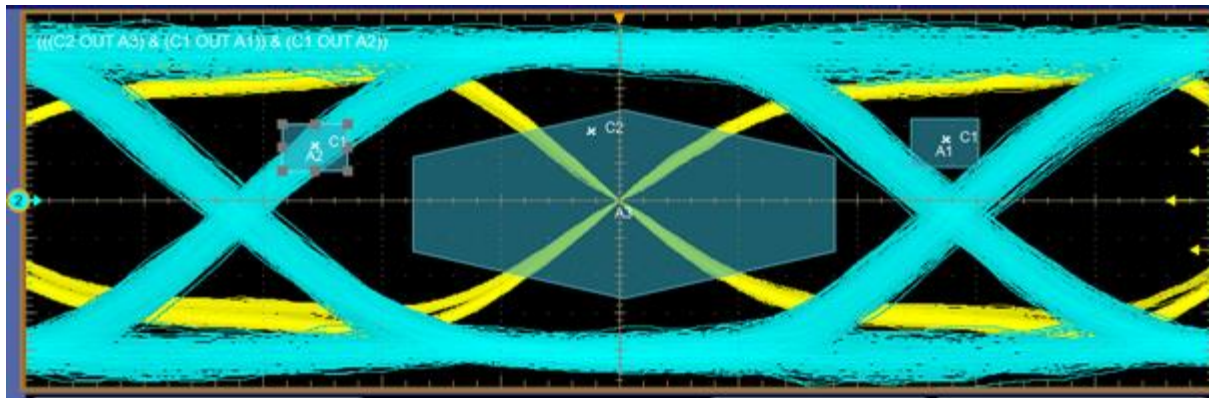
Triggering Techniques for Debugging DRAM

- **Challenge: Dual-Rank System**
 - **Need to Isolate & Measure a Single Rank**
 - **Difficult to isolate data bursts from one rank only**



Triggering Techniques for Debugging DRAM

- **‘Visual’ Trigger Used to Qualify One Rank**
 - Visual area (“keep-out” region) used to exclude low-amplitude signals
 - Eliminates lower-amplitude data bursts from rank 2



“After” gating with visual trigger

High-Speed Serial Data Test Solutions...

Design

Verification

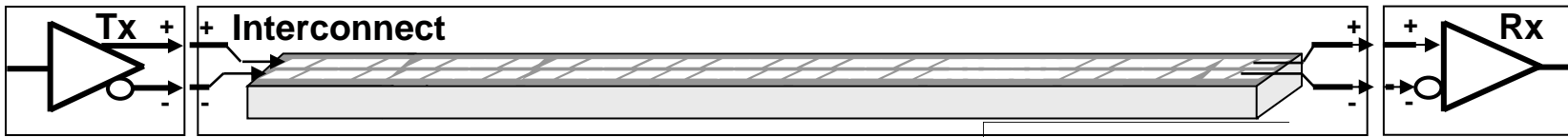
Compliance Test



GbE DisplayPort

HDMI™

MHL ...



Real-time Scopes



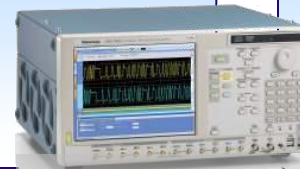
System Integration
Digital Validation & Debug

Logic Analyzers



Transmitter Testing

Receiver Test
Margin
Testing



Arbitrary Waveform Generator

Probing
Fixtures



Interconnect Test

Sampling Scopes



Compliance Test

Compliance Test Software

