# 高速串行测试方案介绍

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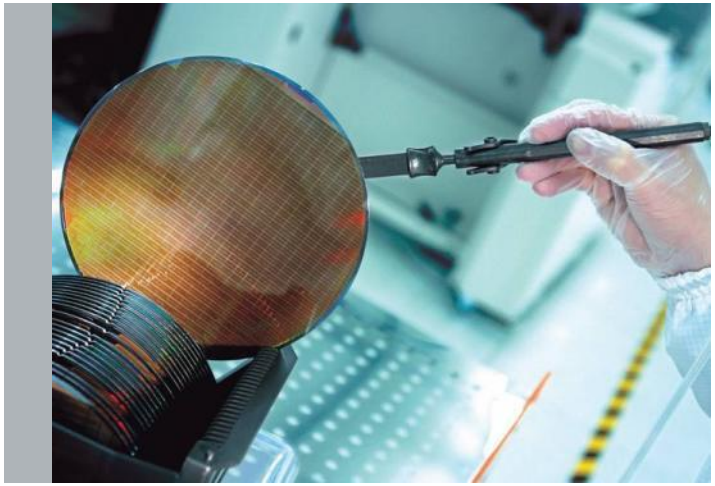

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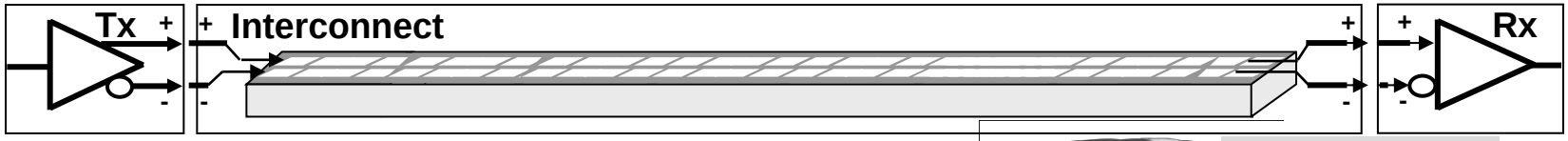
# High-Speed Serial Data Test Solutions

**Design** > **Verification** > **Compliance Test**

PCI EXPRESS · SERIAL ATA · SUPERSPEED USB · ddr3 · IEEE · GbE · DisplayPort · HDMI · MHL …



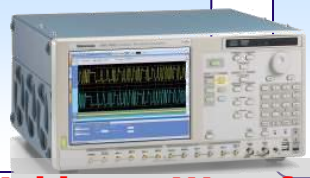

**System Integration**
**Digital Validation & Debug**

**Logic Analyzers**

**Real-time Scopes**

**Transmitter Testing**

**Receiver Test**
**Margin Testing**



**Arbitrary Waveform Generator**

**Probing Fixtures**

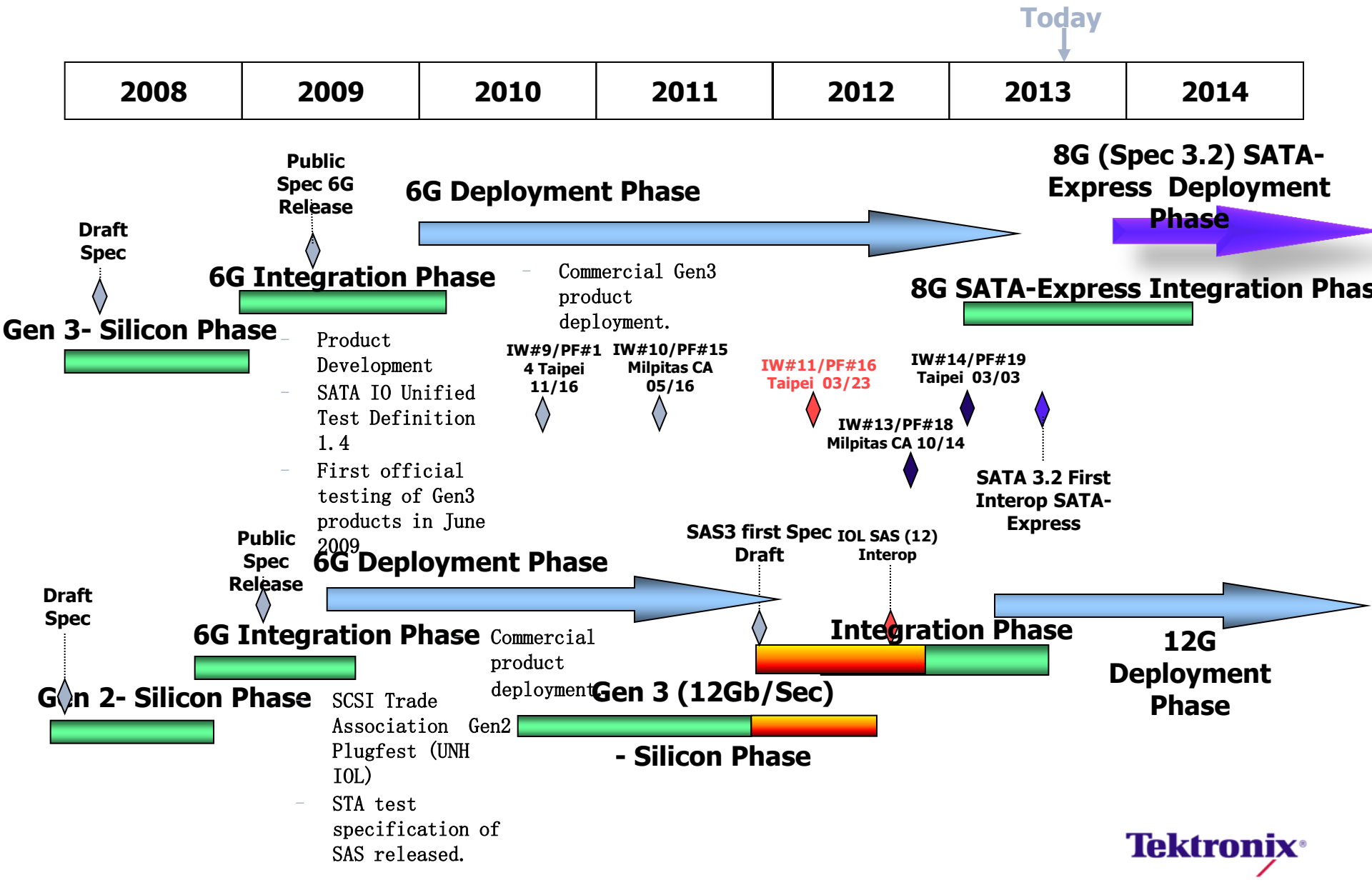
**Interconnect Test**

**Sampling Scopes**

**Compliance Test**

**Compliance Test Software**

# Storage Timelines and Solutions Development

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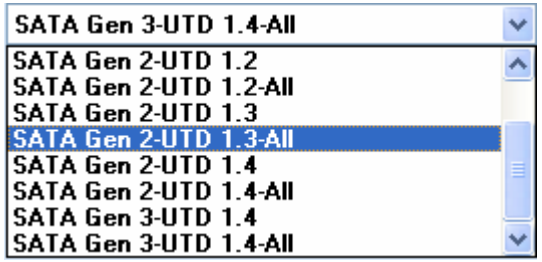
# SATA UTD 1.4 TSG/PHY/OOB Measurements

**Drive : PHY-TSG-OOB SATA Gen 3-UTD 1.4-All**

| Select | Test Name |
|---|---|
| ☑ | Informative-df/dt Measurement |
| ☑ | Informative-Eye diagrams |
| ☑ | OOB01-OOB Signal Detection Threshold |
| ☑ | OOB02-UI During OOB Signaling |
| ☑ | OOB03-COMINIT_RESET and COMWAKE Transmit Burst Length |
| ☑ | OOB04-COMINIT_RESET Transmit Gap Length |
| ☑ | OOB05-COMWAKE Transmit Gap Length |
| ☑ | OOB06-COMWAKE Gap Detection Windows |
| ☑ | OOB07-COMINIT Gap Detection Windows |
| ☑ | PHY01-Unit Interval |
| ☑ | PHY02-Frequency Long Term Stability |
| ☑ | PHY03-Spread-Spectrum Modulation Frequency |
| ☑ | PHY04-Spread-Spectrum Modulation Deviation |
| ☑ | TSG01-Differential Output Voltage-Option 1 |
| ☑ | TSG01-Differential Output Voltage-Option 2 |
| ☑ | TSG02-Rise-Fall Time |
| ☑ | TSG03-Differential Skew |
| ☑ | TSG04-AC Common Mode Voltage |
| ☑ | TSG05-Rise-Fall Imbalance |
| ☑ | TSG06-Amplitude Imbalance |
| ☑ | TSG09-TJ at Connector, Clock to Data, fBAUD-500 |
| ☑ | TSG10-DJ at Connector, Clock to Data, fBAUD-500 |
| ☑ | TSG11-TJ at Connector, Clock to Data, fBAUD-500 |
| ☑ | TSG12-DJ at Connector, Clock to Data, fBAUD-500 |
| ☑ | TSG13-Transmit Jitter |
| ☑ | TSG14-TX Maximum Differential Voltage Amplitude |
| ☑ | TSG15-TX Minimum Differential Voltage Amplitude |
| ☑ | TSG16-Tx AC Common Mode Voltage |




- Different test program and degrees of regression testing user selectable.
- Debug and diagnostic tools (Informative measurements)
- Updated SATA Gen3 measurements
  - **New OOB patterns**
  - TSG ECN additions

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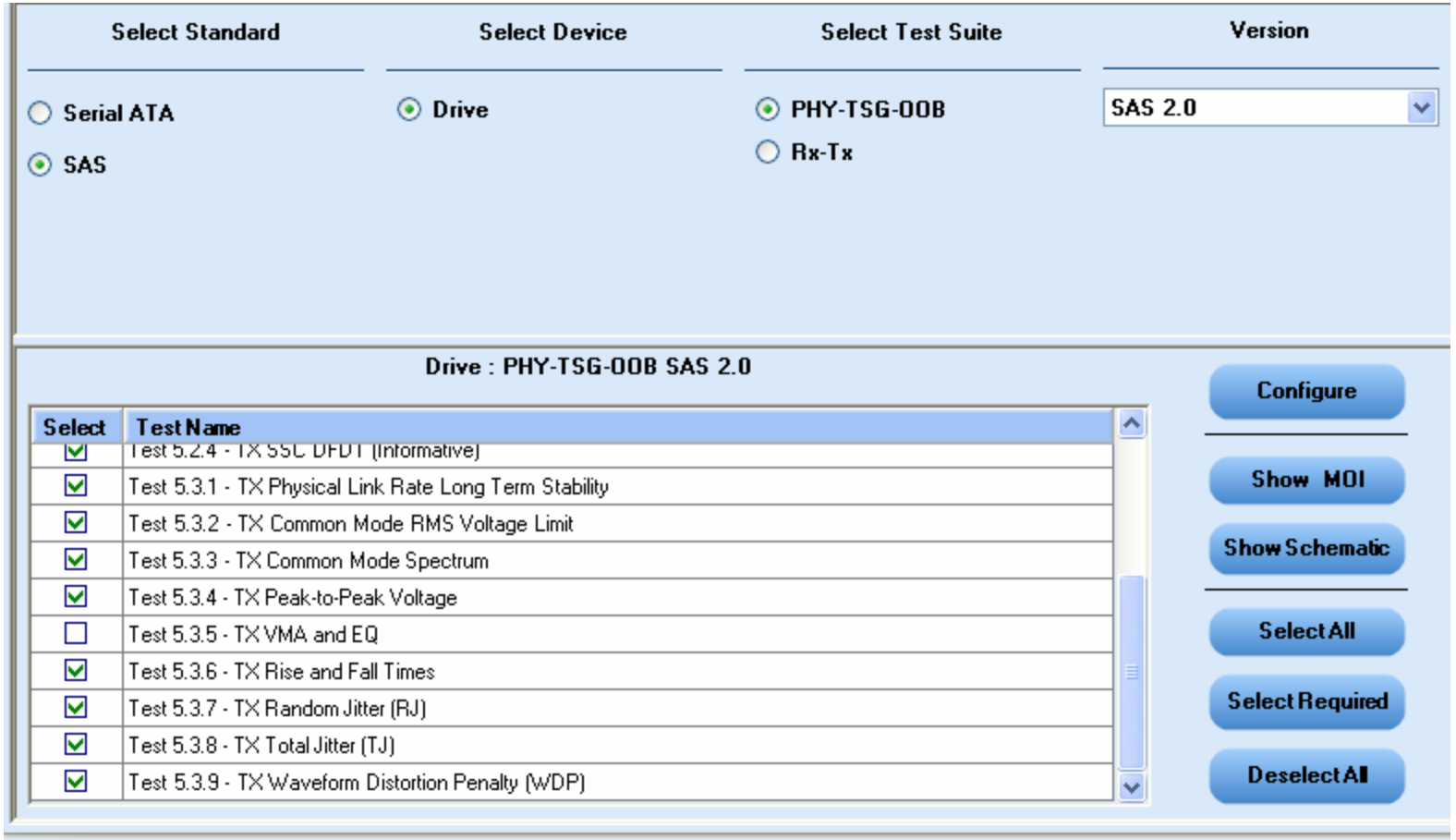
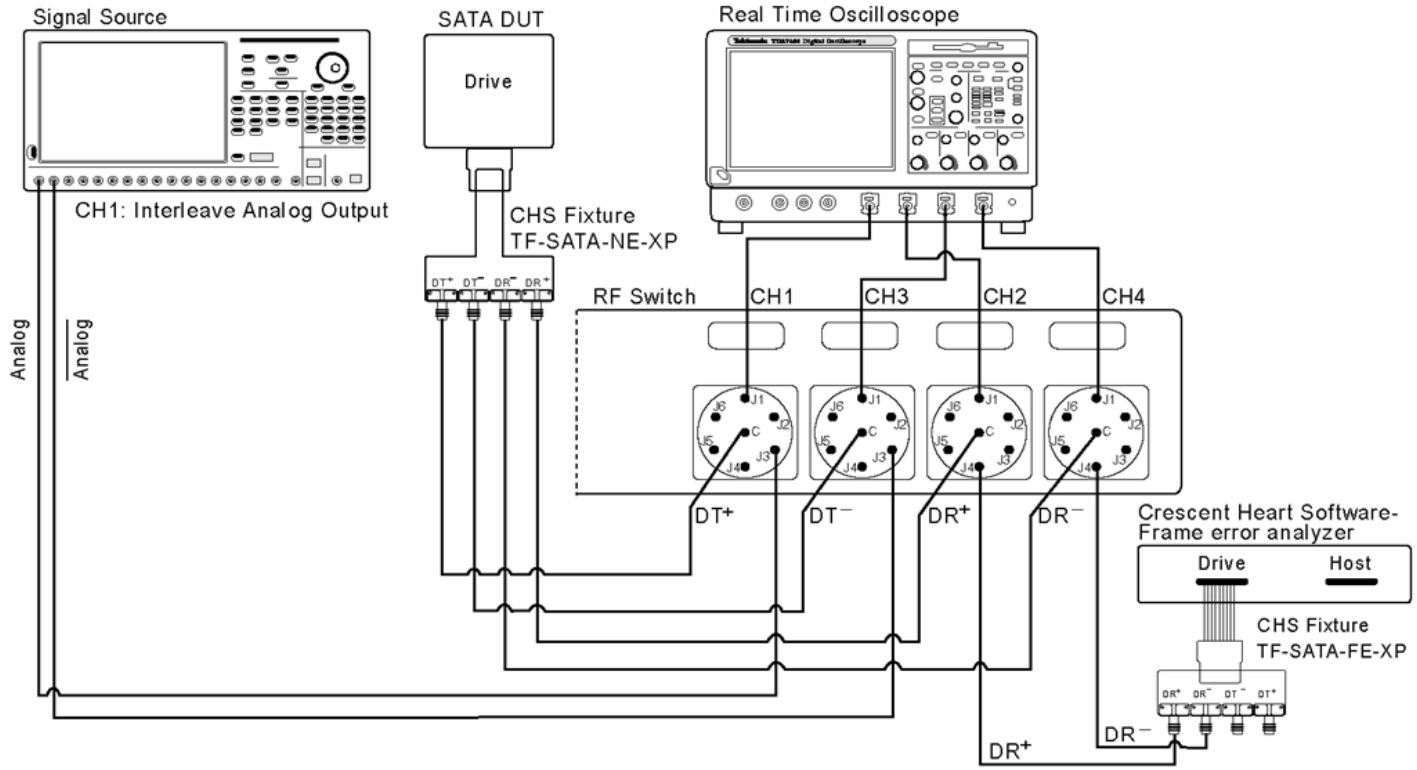
# SATA/SAS TSB/PHY/OOB



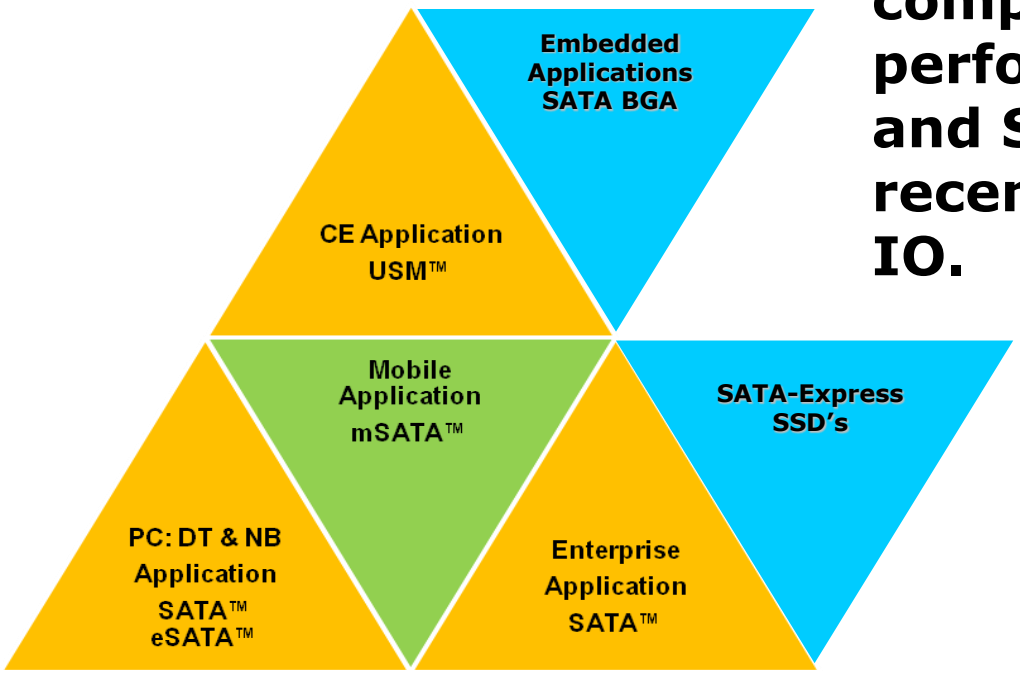
# SATA/SAS TSG/PHY/OOB test connection



# SATA/SAS: test Report

| Test Name | Test Details | | | Low Limit | Measured Value | High Limit | Margin | Units | Test Result |
|---|---|---|---|---|---|---|---|---|---|
| | Pattern Name | Interface Speed | Measurement Details | | | | | | |
| Test 5.2.1-TX SSC Modulation Type | HFTP | 6.0Gb/s | Center-spread SAS | -NA- | SSC ON | -NA- | -NA- | -NA- | Pass |
| Test 5.2.2-TX SSC Modulation Frequency | HFTP | 6.0Gb/s | SSC Modulation Frequency | >= 30 | 30.0000 | <= 33 | 0 , 3 | KHz | Pass |
| | HFTP | 6.0Gb/s | Min SSC Modulation Frequency | >= 30 | 29.9992 | <= 33 | Informative | | Informative |
| | HFTP | 6.0Gb/s | Max SSC Modulation Frequency | >= 30 | 30.0011 | <= 33 | Informative | | Informative |
| Test 5.2.3-TX SSC Modulation Deviation and Balance | HFTP | 6.0Gb/s | Max Deviation | -NA- | -2199.6500 | -NA- | -NA- | ppm | Informative |
| | HFTP | 6.0Gb/s | Min Deviation | -NA- | 2200.0074 | -NA- | -NA- | | Informative |
| | HFTP | 6.0Gb/s | Avg Deviation | >= -350 | 0.1787 | <= 350 | 350.1787, 349.8213 | | Pass |
| | HFTP | 6.0Gb/s | Deviation asymmetry | - | 0.3574 | <= 288 | 287.6426 | | Pass |
| Test 5.2.4-TX SSC DFDT (Informative) | HFTP | 6.0Gb/s | df/dt | >= -850 | -380.3082 | <= 850 | Informative | ppm/us | Informative |
| Test 5.3.1-TX Physical Link Rate Long Term Stability | HFTP | 6.0Gb/s | Mean Period | > -100 | -2.1050 | < 100 | Informative | ppm | Informative |
| | HFTP | 6.0Gb/s | Min Period | > -100 | 2200.0074 | < 100 | Informative | | Informative |
| | HFTP | 6.0Gb/s | Max Period | > -100 | -2199.6501 | < 100 | Informative | | Informative |
| Test 5.3.2-TX Common Mode RMS Voltage Limit | CJTPat-Gen 2 | 6.0Gb/s | Common-mode RMS voltage at IT (mV)-SAS 2.0 | - | 42.9927 | < 30 | 12.9927 | mV | Fail |
| Test 5.3.3-TX Common Mode Spectrum | CJTPat-Gen 2 | 6.0Gb/s | Common-mode spectrum (dBmV) at 100MHz-SAS 2.0 | - | -33.5589 | < 12.7 | 46.2589 | mV | Pass |
| | CJTPat-Gen 2 | 6.0Gb/s | Common-mode spectrum (dBmV) at first harmonic-SAS 2.0 | - | 16.7701 | < 26 | 9.2299 | | Pass |
| | CJTPat-Gen 2 | 6.0Gb/s | Common-mode spectrum (dBmV) at second harmonic-SAS 2.0 | - | -9.8586 | < 30 | 39.8586 | | Pass |
| Test 5.3.4-TX Peak-to-Peak Voltage | D30.3-Gen 2 | 6.0Gb/s | Peak to Peak voltage (mVppd)-SAS 2.0 | > 850 | 1240.0000 | < 1200 | 390 , 40 | mV | Fail |
| Test 5.3.5-TX VMA and EQ | D30.3-Gen 2 | 6.0Gb/s | Transmitter equalization (dB)-SAS 2.0 | > 2 | 2.0684 | < 4 | Informative | dB | Pass |
| Test 5.3.6-TX Rise and Fall Times | D10.2 | 6.0 Gb/s | Rise time in ps | >= 41.6 | 55.7616 | - | 14.1616 | ps | Pass |
| | D10.2 | 6.0 Gb/s | Fall time in ps | >= 41.6 | 55.3999 | - | 13.7999 | | Pass |
| Test 5.3.7-TX Random Jitter (RJ) | D24.3-Gen 2 | 6.0Gb/s | Rj before CIC | - | 0.7069 | <= 25 | 24.2931 | ps | Pass |
| | D24.3-Gen 2 | 6.0Gb/s | Rj after CIC | - | 0.5321 | <= 25 | 24.4679 | | Pass |

# The SATA Ecosystem: Now




**Today, SATA is expanding in specialized low power, compact and high performance areas with BGA and SATA-Express Solutions recently approved by SATA-IO.**

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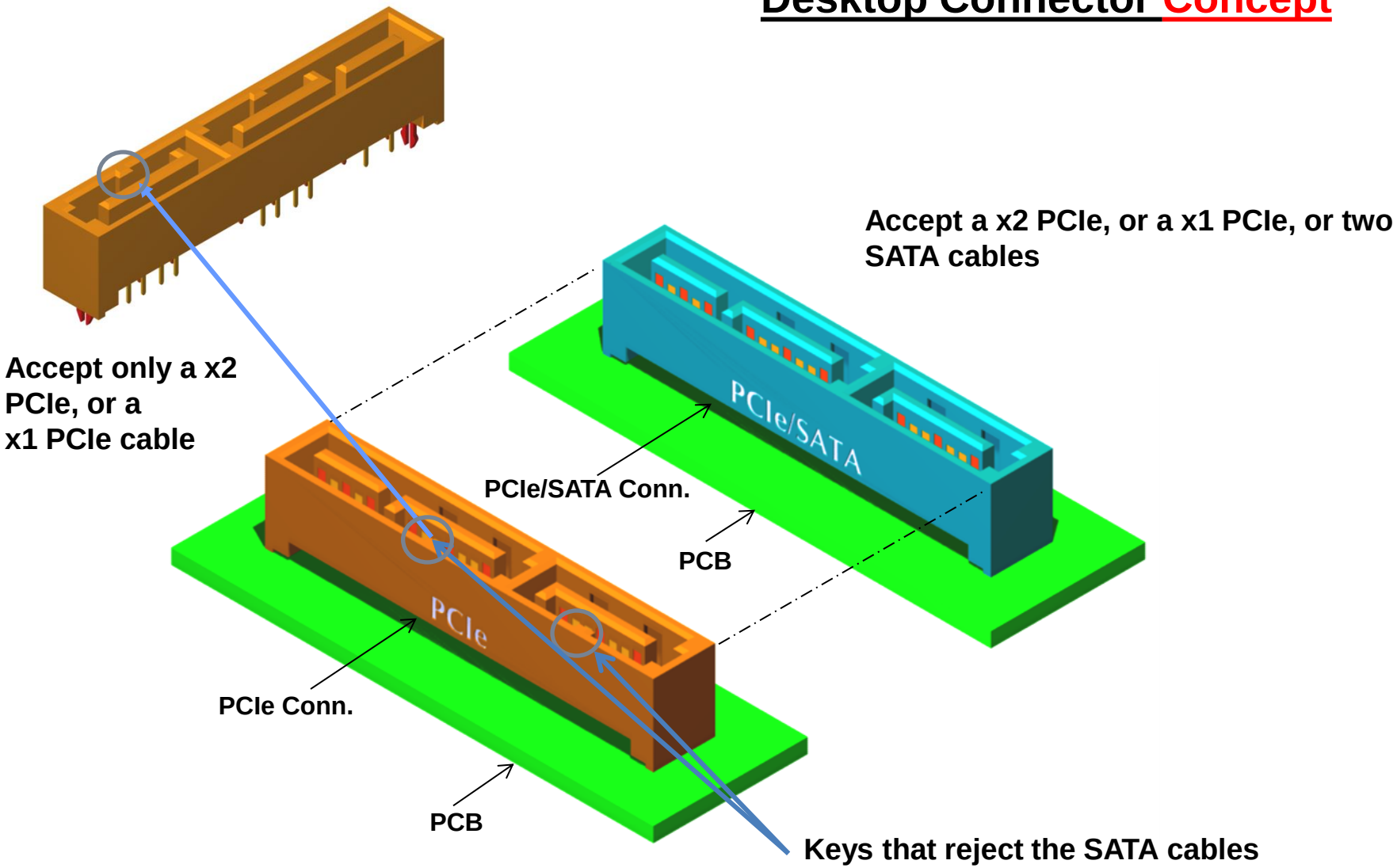
# Enabling the New SATA Express Ecosystem

## Desktop Connector Concept

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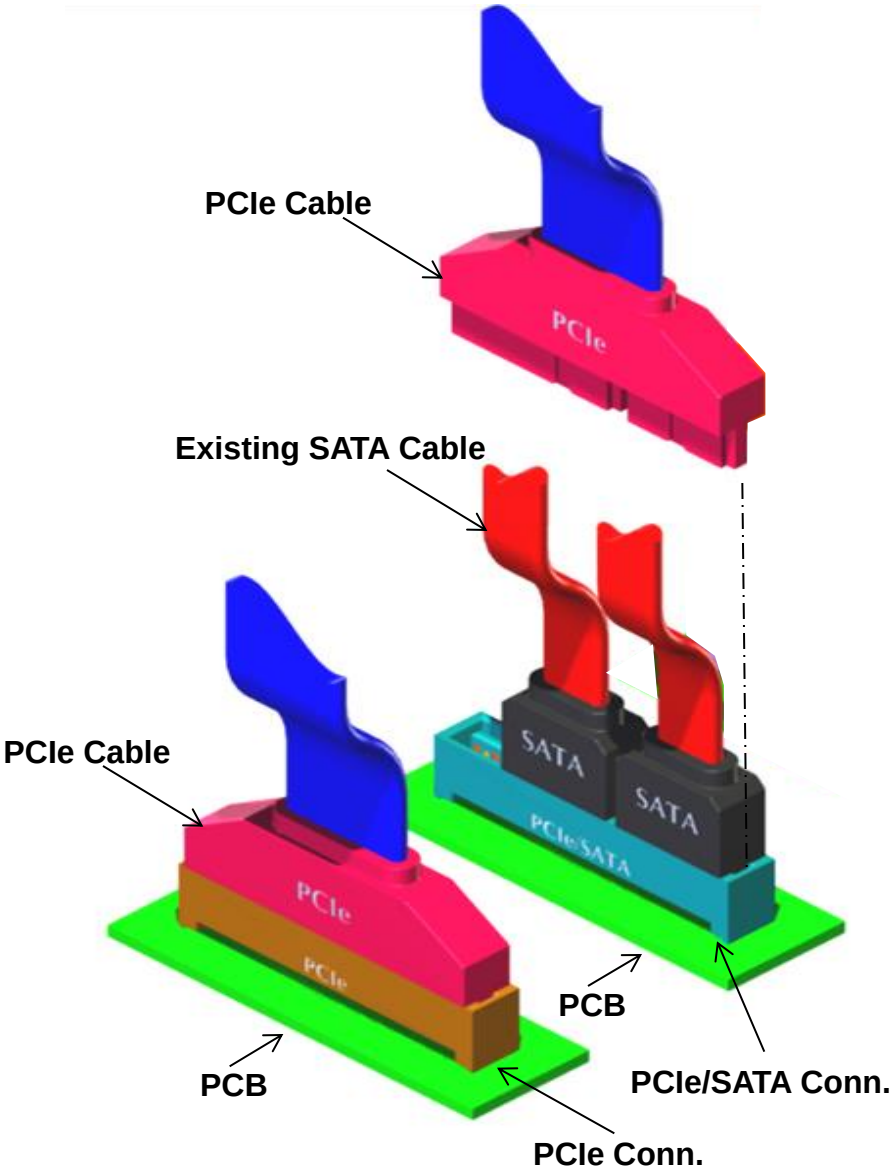
# Enabling the New SATA Express Ecosystem




## Desktop Cables Concept

- SATA devices will coexist with next generation PCIe devices
- SATA cost/performance benefits
- Requires a connector that supports both PCIe and SATA
  - Allows a single motherboard (backplane) connector to support both interfaces
- HDD-compatible form factors to be defined for PCIe devices
  - Enables system-level mechanical compatibility
  - Preserves high-capacity storage

**SATA-IO CabCon has been chartered to develop SATA compatible connectors and form factors for PCIe SSD/hybrid drives**

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# SATA Express Signal Access

- Recommend Luxshare-ICT Dual Port SAS fixtures (SFF-8482)
- Similar dimensions but different pinout
- For device testing use plug fixture (TF-4R21) to mate with SATAe plug
  - Both ports accessible (29 pin)
- For cable testing use receptacle fixture (TF-4P22) to mate with SATAe receptacle
  - Only port A is accessible (22 pin)

**SAS Dual Port Plug Test Fixture**

**SAS Dual Port Receptacle Test Fixture**

**http://www.luxshare-ict.com/**

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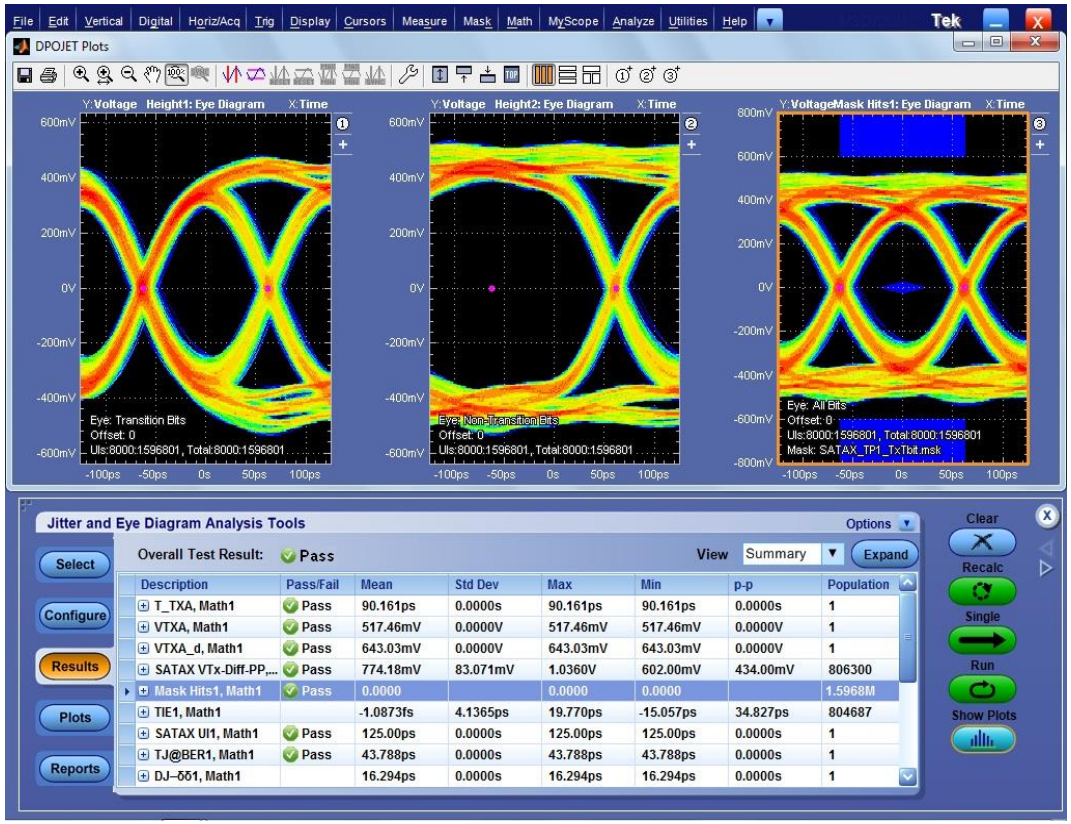
# Tektronix Solutions for SATA Express Measurements

- DPOJET-based SATA Express setup (requires option PCE3)
- Support for Base/CEM spec measurements
- Supports all versions of PCI Express and includes SATA Express PLL configurations

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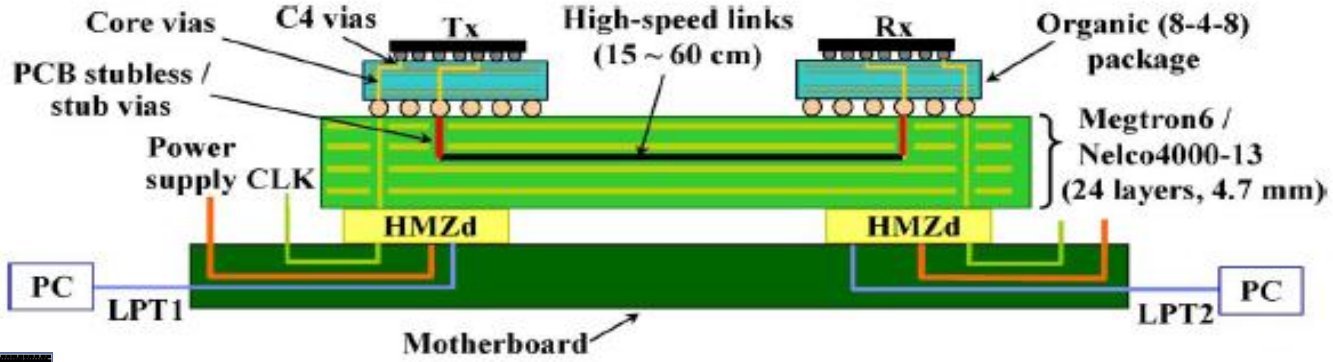
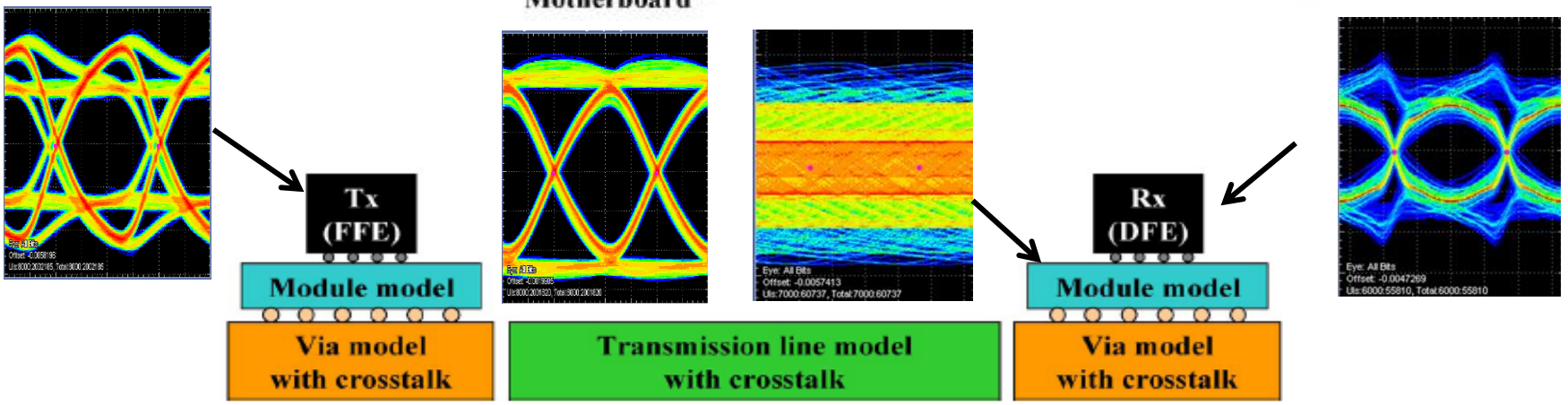
# 12G+ Design Problem:
## 1000mV, FFE, Crosstalk, DFE, 50mV

- **Crosstalk and signal loss problems are the largest design challenge today.**
- **Significant advances in high tap count Decision Feedback Equalization are key to operating at 12G+.**

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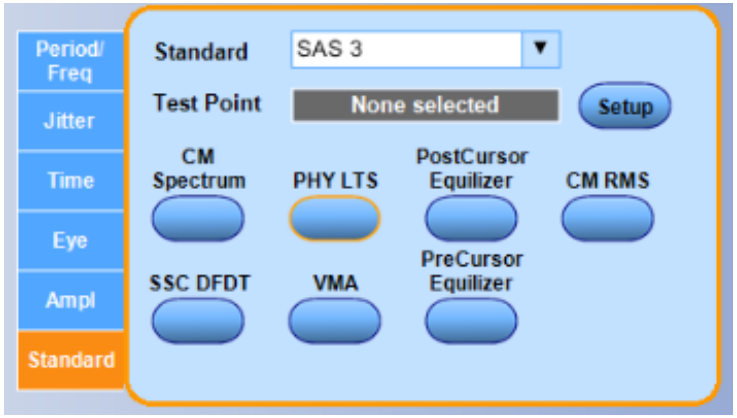
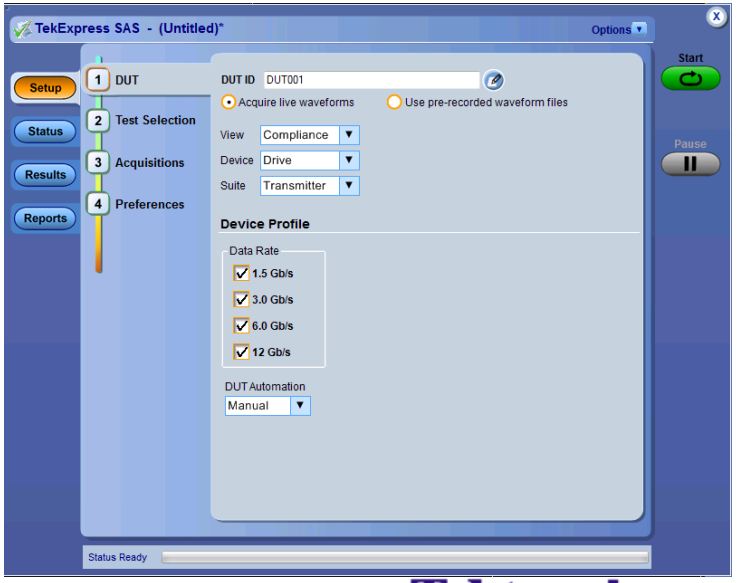
# SAS-3 PHY Transmitter Solution

| | |
|---|---|
| **Group 1 – OOB Signaling** | |
| 5.1.1 | Maximum Noise During OOB Idle |
| 5.1.2 | OOB Burst Amplitude |
| 5.1.3 | OOB Offset Delta |
| 5.1.4 | OOB Common Mode Delta |
| **Group 2 – Spread Spectrum Clocking (SSC) Requirements** | |
| 5.2.1 | SSC Modulation Type |
| 5.2.2 | SSC Modulation Frequency |
| 5.2.3 | SSC Modulation Deviation |
| 5.2.4 | SSC Balance |
| 5.2.5 | SSC DFDT |
| **Group 3 – NRZ Data Signaling Requirements** | |
| 5.3.1 | Physical Link Rate Long Term Stability |
| 5.3.2 | Common Mode RMS Voltage Limit |
| 5.3.3 | Common Mode Spectrum |
| 5.3.4 | Peak to Peak Voltage |
| 5.3.5 | Voltage Modulation Amplitude (VMA) |
| 5.3.6 | Equalization |
| 5.3.7 | Rise Time |
| 5.3.8 | Fall Time |
| 5.3.9 | Random Jitter (RJ) |
| 5.3.10 | Total Jitter (TJ) |
| 5.3.11 | Waveform Distortion Penalty (WDP) |
| 5.3.12 | SAS3_EYEOPENING |
| 5.3.13 | Pre Cursor Equalization Ratio |
| 5.3.14 | Post Cursor Equalization Ratio |
| 5.3.15 | Transition Bit Voltage PK-PK (VHL) |
| 5.3.16 | Unit Interval |

**SAS-3 1.5/3/6/12 Gb/s Tx Test Software**




**TekExpress SAS3-TSG Automation Softwa**

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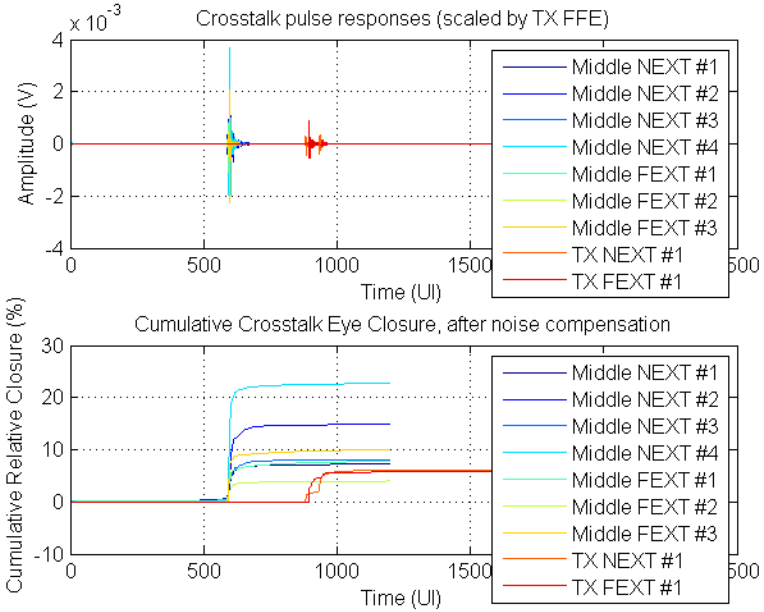
# NEW Measurement for Crosstalk/ISI Evaluation

- SAS3_EYEOPENING* Measurement for accurate analysis of ISI and crosstalk effects
- Provides measure of relative vertical eye opening after reference equalization



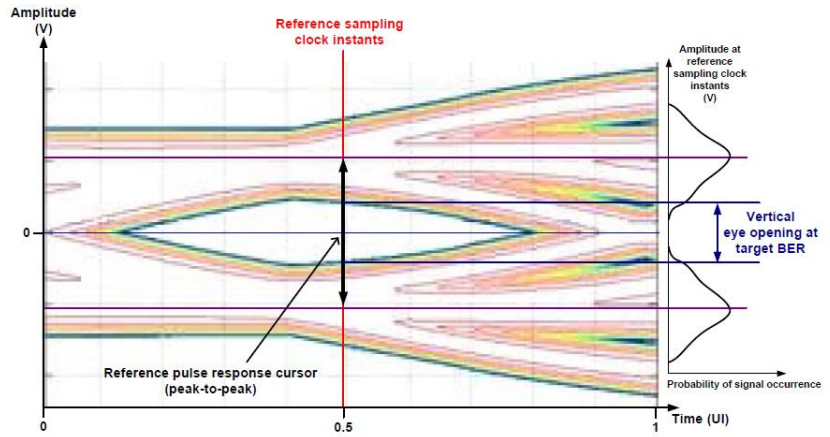




Figure Fe – Simulated Vertical eye opening and reference pulse response cursor

***Source:* 12-244r3**

*Note, this measurement is similar to the SAS-2 Waveform Distortion Penalty (WDP) measurement but also includes Tx EQ in addition to DFE. The code was provided and distributed through the T10 Technical Committee and permission has been granted for Tektronix to reuse.

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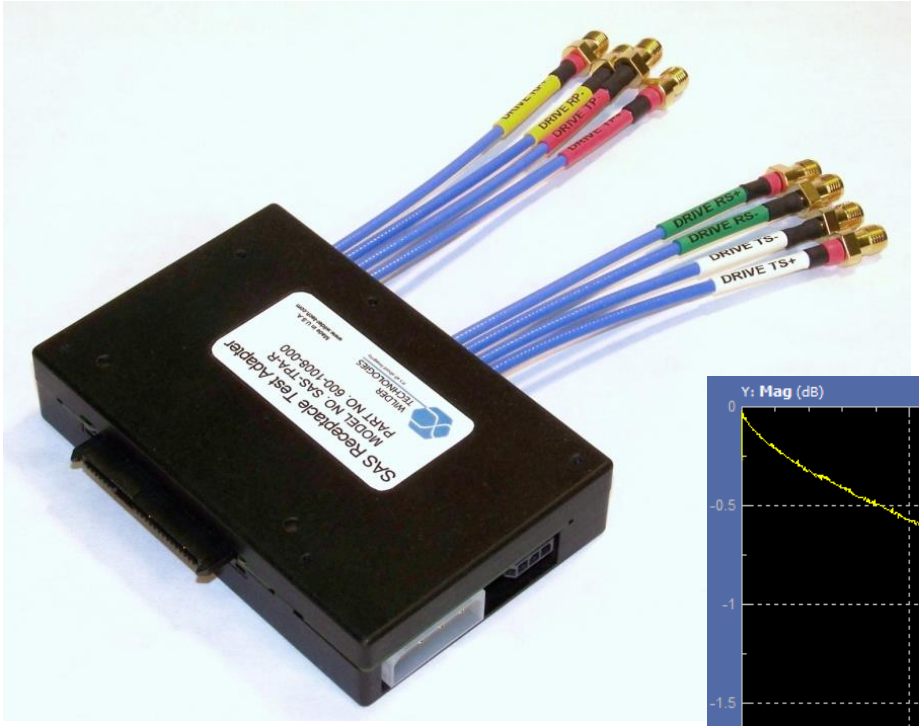
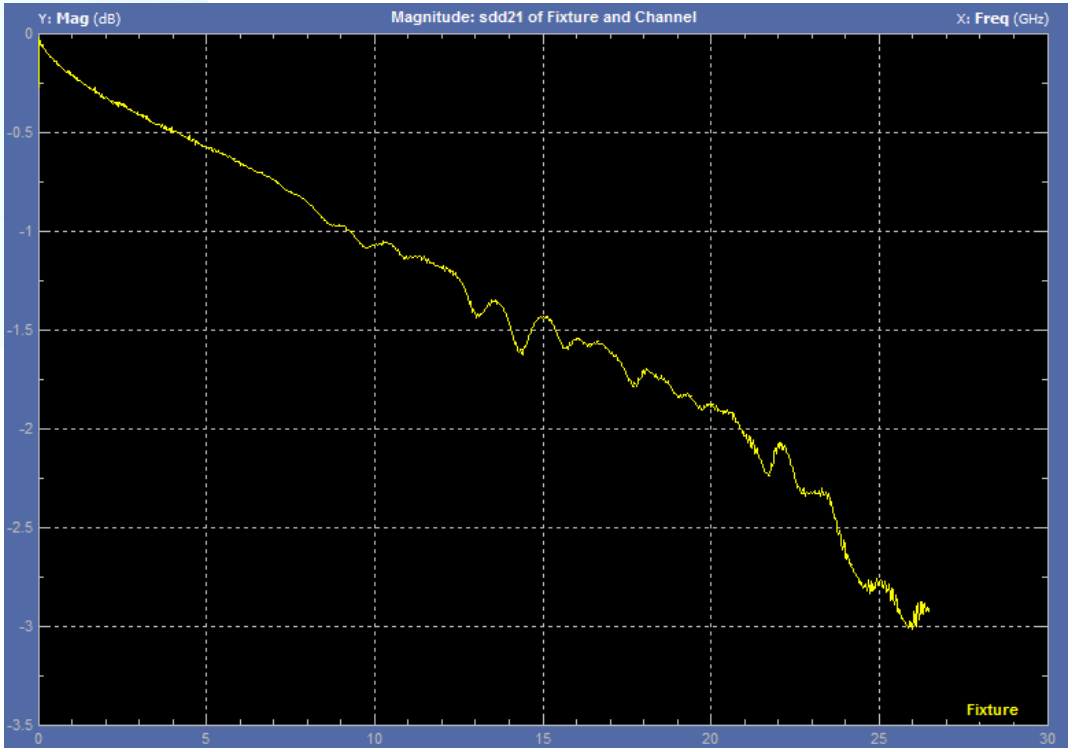
# SAS Receptacle Test Adapter




**Sdd21 (1x Thru) => -3dB@26 GHz**

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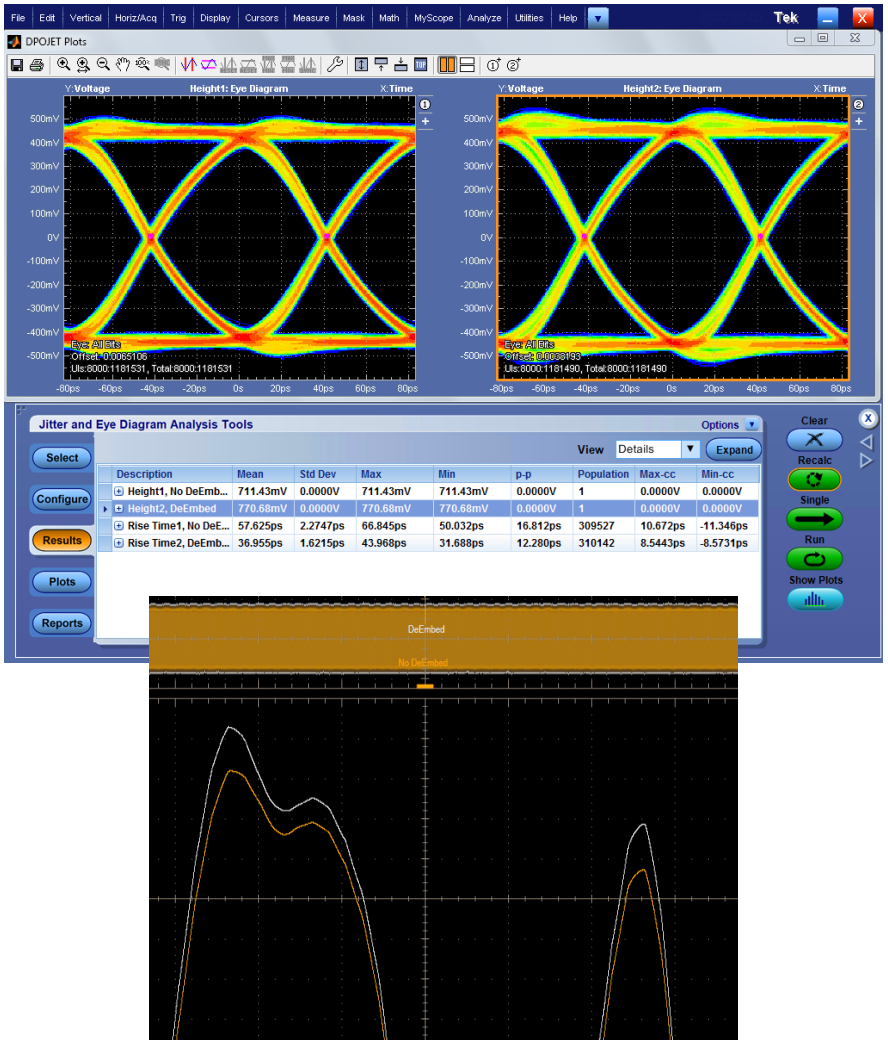
# Test Fixture De-embedding

- Why de-embed?
  - Tx measurements referenced to die (ET)
  - Improve margin with removal of fixture effects
- S-Parameters acquired from calibration fixture or model extraction
- Use inverse response to compensate for loss

| | Before De-Embed | After De-Embed |
|---|---|---|
| Eye Height | 711 mV | 770 mV |
| Rise Time | 57 | 37 |

**Before** **After**

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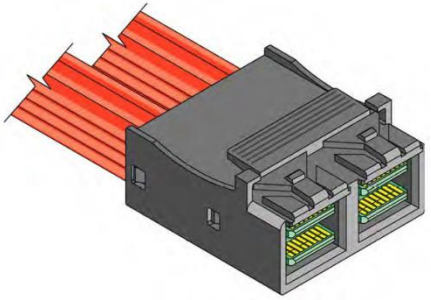
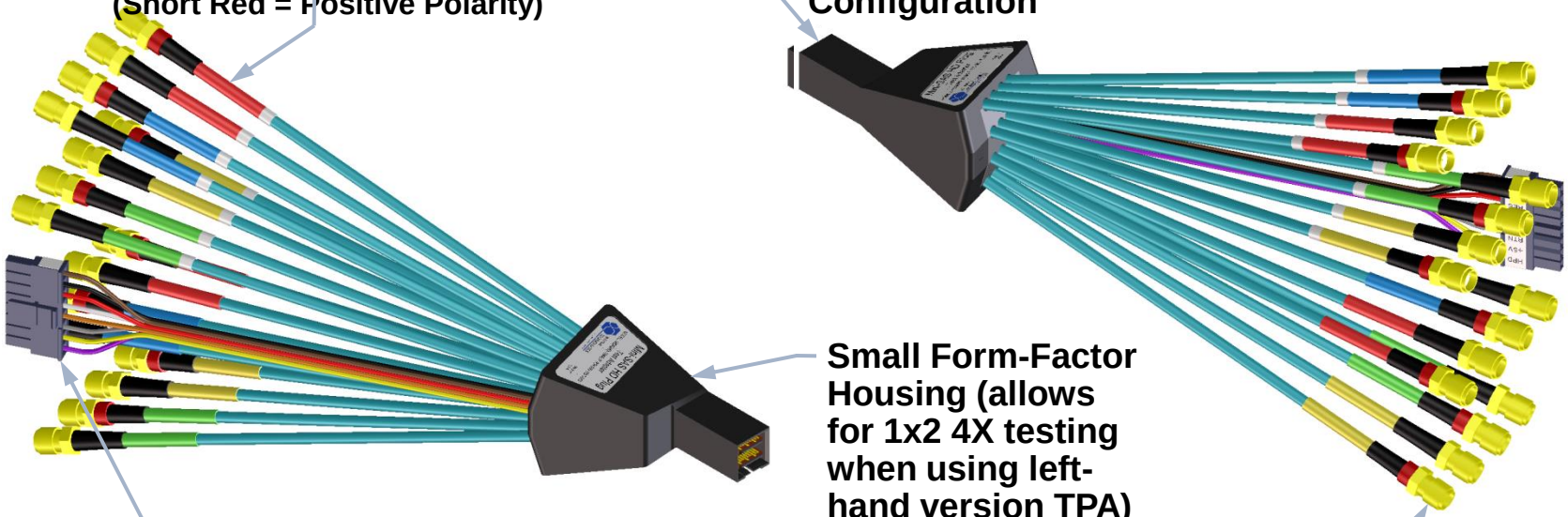
# Mini-SAS HD Plug Test Adapters



Mini SAS HD 8i
cable plug connector

Color Coded and Imprinted Markings
(Large Colored = Channel Number)
(Short White = Transmitter Side)
(Short Red = Positive Polarity)

High-Performance Mini-SAS HD Plug Connector Configuration



Small Form-Factor Housing (allows for 1x2 4X testing when using left-hand version TPA)

8 Position Low-Speed Connector

16 SMAs for High-Speed Testing

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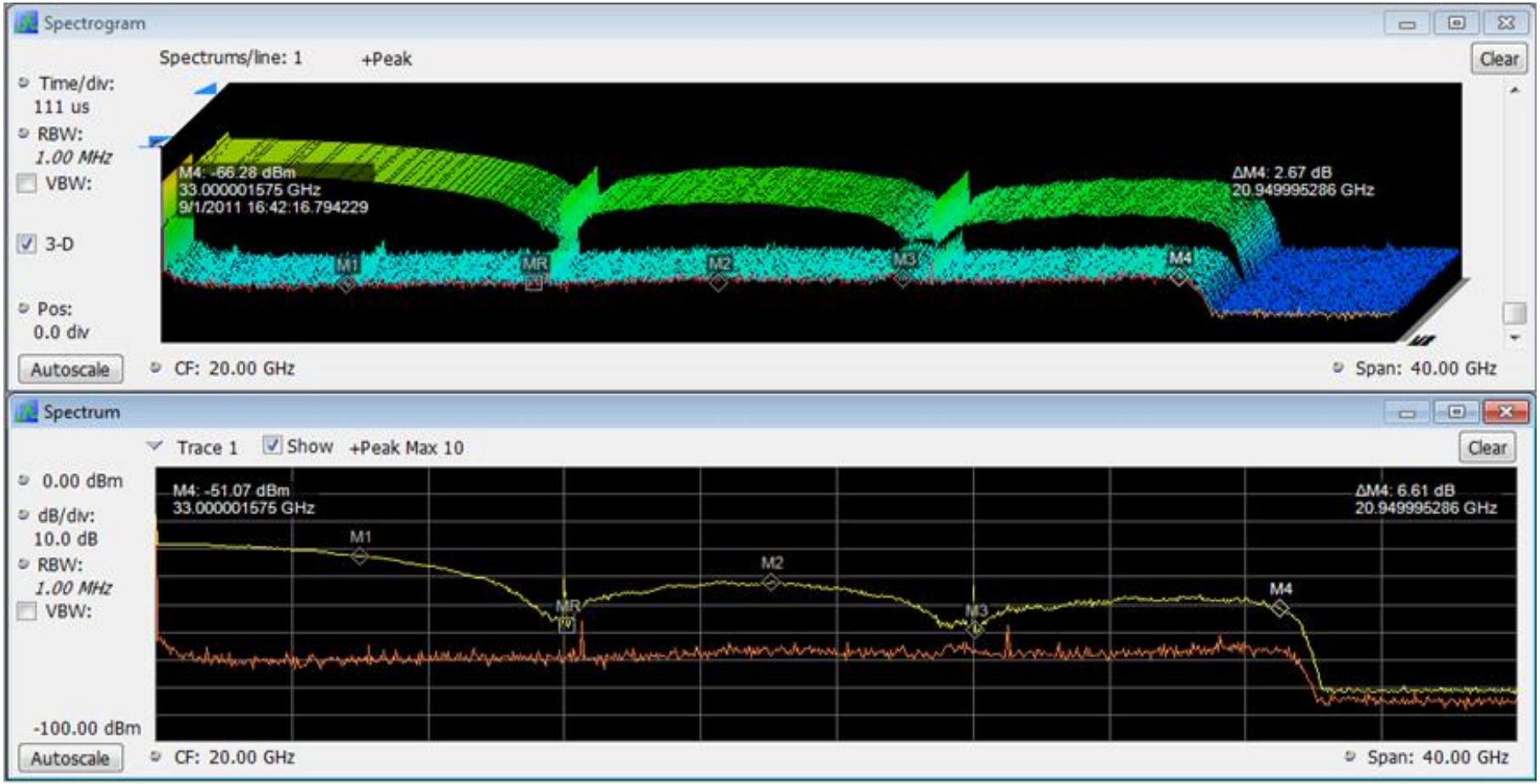
# Bandwidth Considerations

## SAS 12G NRZ Power Spectrum




**Marker Readout Table**

| Marker | Frequency | Δ Frequency | Δ Time | Spectrum | Δ Spectrum | Spectrogram | Δ Spectrogram |
|---|---|---|---|---|---|---|---|
| M2 | 18.050004939 GHz | 5.99999865 GHz | --- | -42.01 dBm | 15.67 dB | -68.71 dBm | 0.24 dB |
| M3 | 24.050003589 GHz | 11.9999973 GHz | --- | -59.20 dBm | -1.52 dB | -66.74 dBm | 2.21 dB |
| M4 | 33.000001575 GHz | 20.949995286 GHz | --- | -51.07 dBm | 6.61 dB | -66.28 dBm | 2.67 dB |

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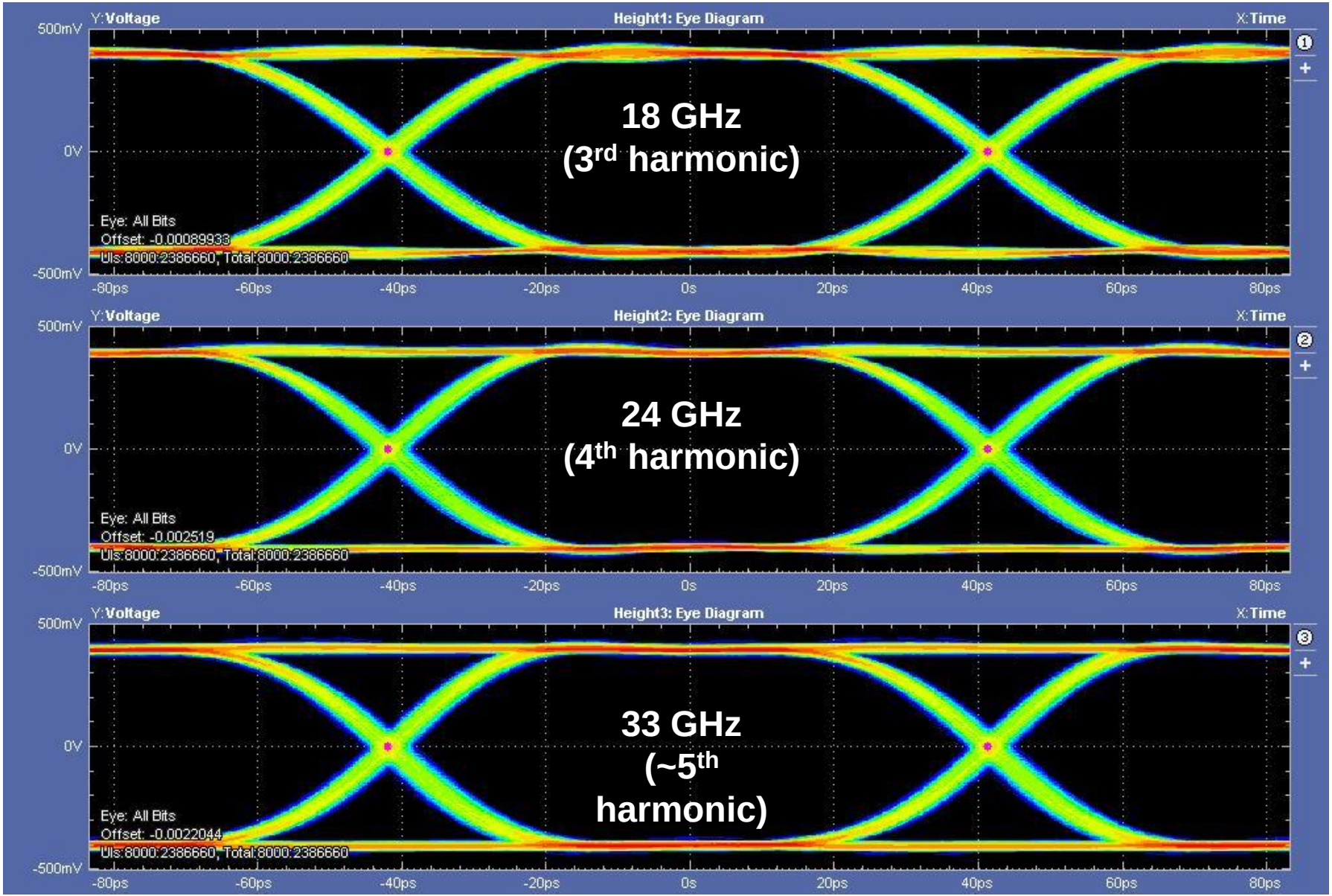
# 12G PRBS from BERT (20ps 20-80% Tr)



# Recommended Equipment

The following components are required for performing SAS12 Tx measurements

- DPO/MSO70K(C/D) Series Oscilloscope with Opt. 2XL or higher
  - 12.5 GHz or higher recommended for 1.5, 3, or 6 Gb/s
  - 20 GHz or higher recommended for 12 Gb/s
- DPOJET Advanced (DJA) - Prerequisite
- Option SAS3-TSG & SAS3-TSGW (required for WDP measurements)
- Test Fixtures:
  - TF-SAS-TPA-R SAS Gen3 Receptacle Adapter (drive form factor) or
  - TF-SASHD-TPA-R miniSASHD 12G SAS Receptacle (mini SAS HD 4i/x cables) or
  - Set of TF-SASHD-TPAR-P miniSASHD 12G SAS (Right Side) Plug and TF-SASHD-TPAL-P miniSASHD 12G SAS (Left Side) Plug (x8)
- PMCABLE1M or equivalent Phase  Matched Cable Set (qty: 2)

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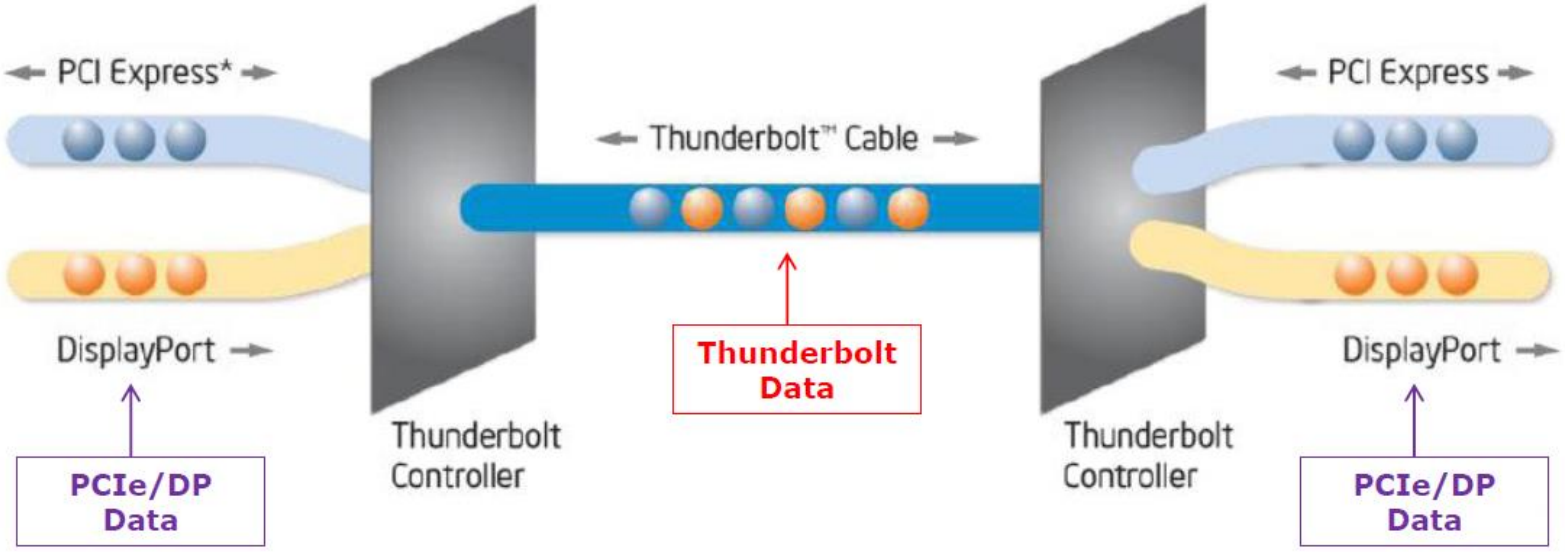
# Thunderbolt Overview

- High Speed Data Bus for PC's
  - Brought to market by Intel/Apple in 2011
  - Interoperable with DisplayPort
- Thunderbolt signaling is dual NRZ (64/66b Encoded)
  - 10.3125 Gb/s data rate
  - It utilizes SFP+ technology with 2 diff Tx and Rx pairs.

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# Thunderbolt Transmitter Test Overview

- All measurements are near end with Fixtures fully de-embed.
- Requires DisplayPort 1.2 conformance testing
- Source Test Suite
- PHY1.1 – Transition Timing
- PHY1.2 – Intra-Pair Skew
- PHY1.3 – AC Common Mode RMS
- PHY1.4 – AC Common Mode Peak
- PHY1.5 – Eye Height
- PHY1.6 – Eye Width
- PHY1.7 – Max Differential Voltage
- PHY1.8 – Total Jitter at 10-12 BER
- PHY1.9 – Unit Interval
- PHY1.10 – SSC Modulation Frequency

- **DUT Configuration**
  - **1. Bit Rates: (DP1.2) + 10.3125Gb/sec**
  - **2. Patterns: 8 1's8 0's, PRBS-9, PRBS-11 and PRBS-31**
  - **3. SSC (Spread Spectrum): On/Off**


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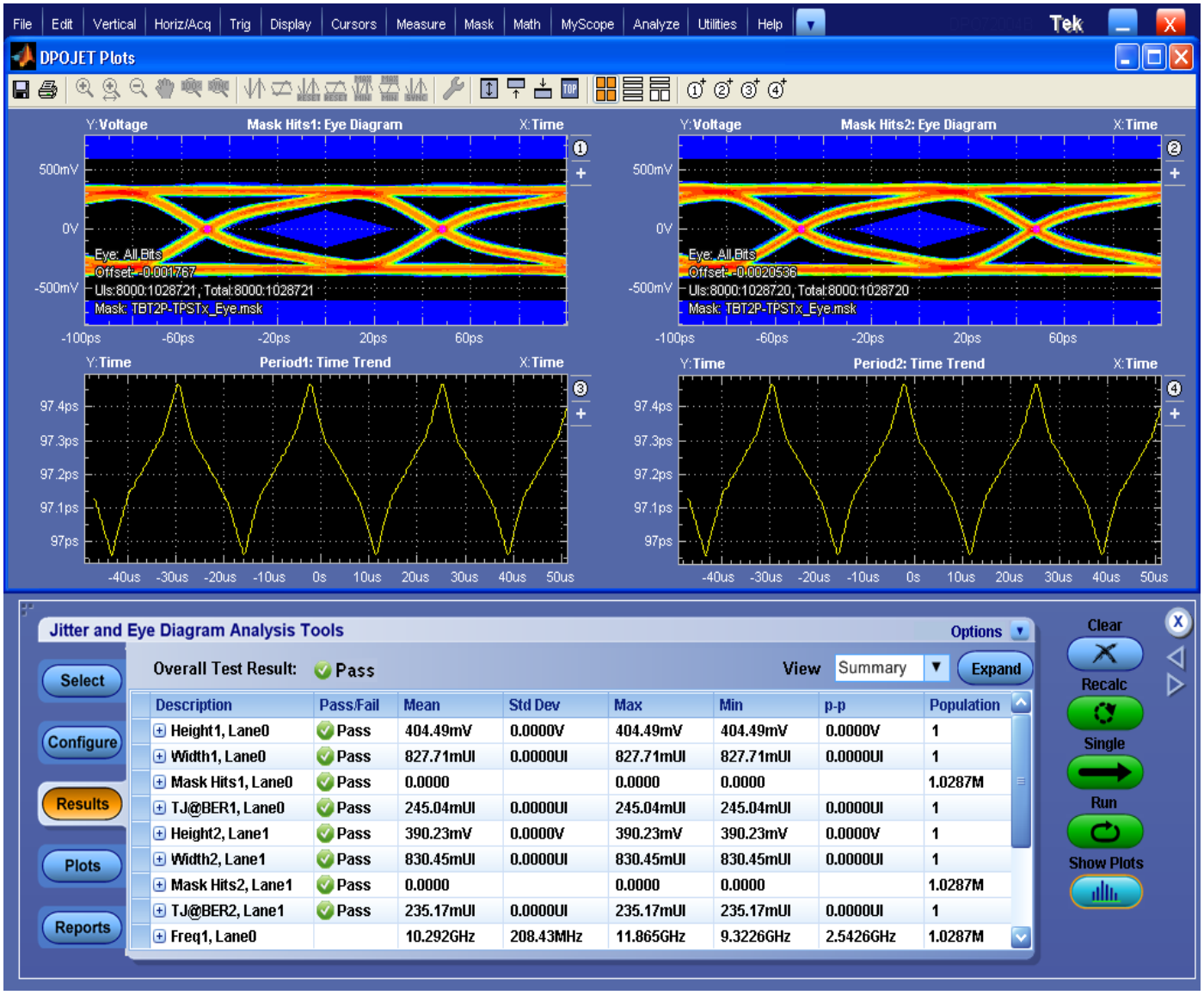
# Thunderbolt Transmitter Testing
# Fully supported in Tektronix's current solutions




Thunderbolt



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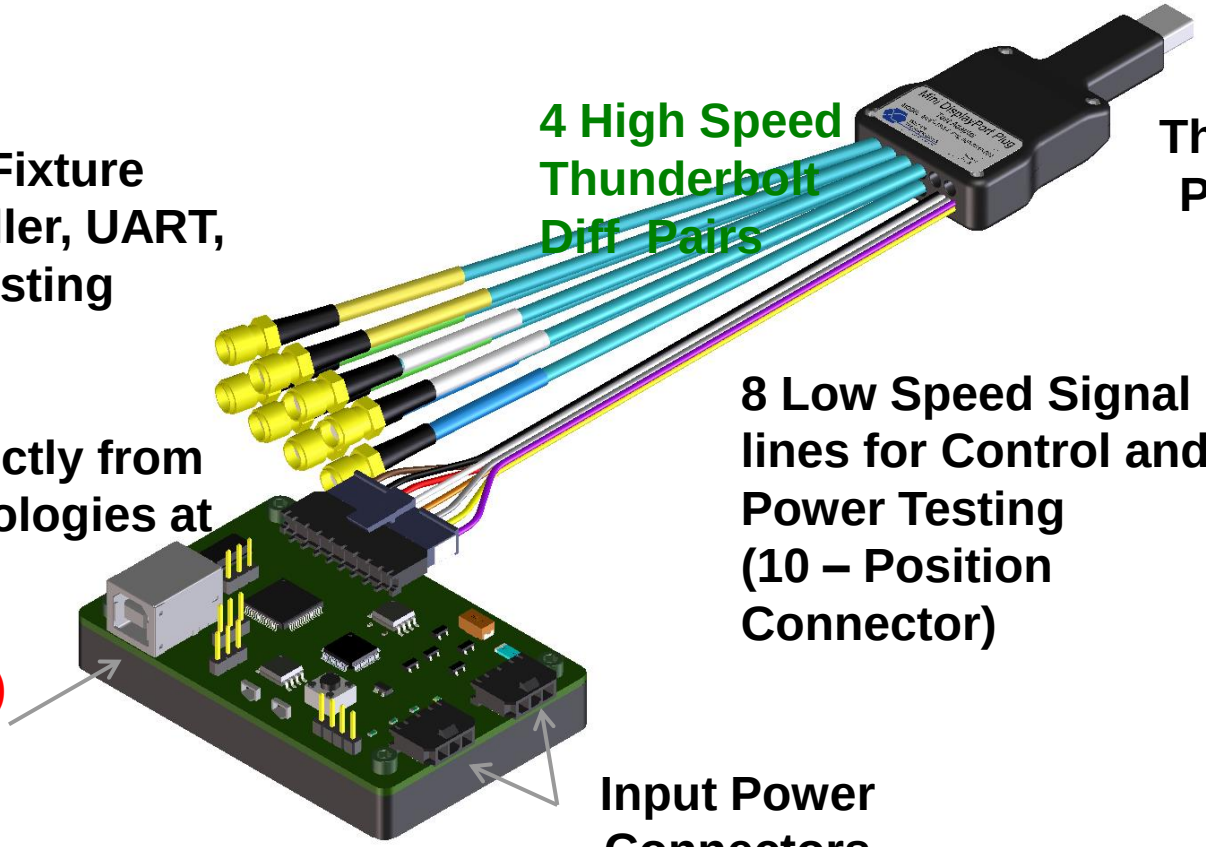
# Thunderbolt Test Connectivity

- **The Digital Port Micro is responsible for Test Pattern and general state control, as well as error polling in the DUT.**



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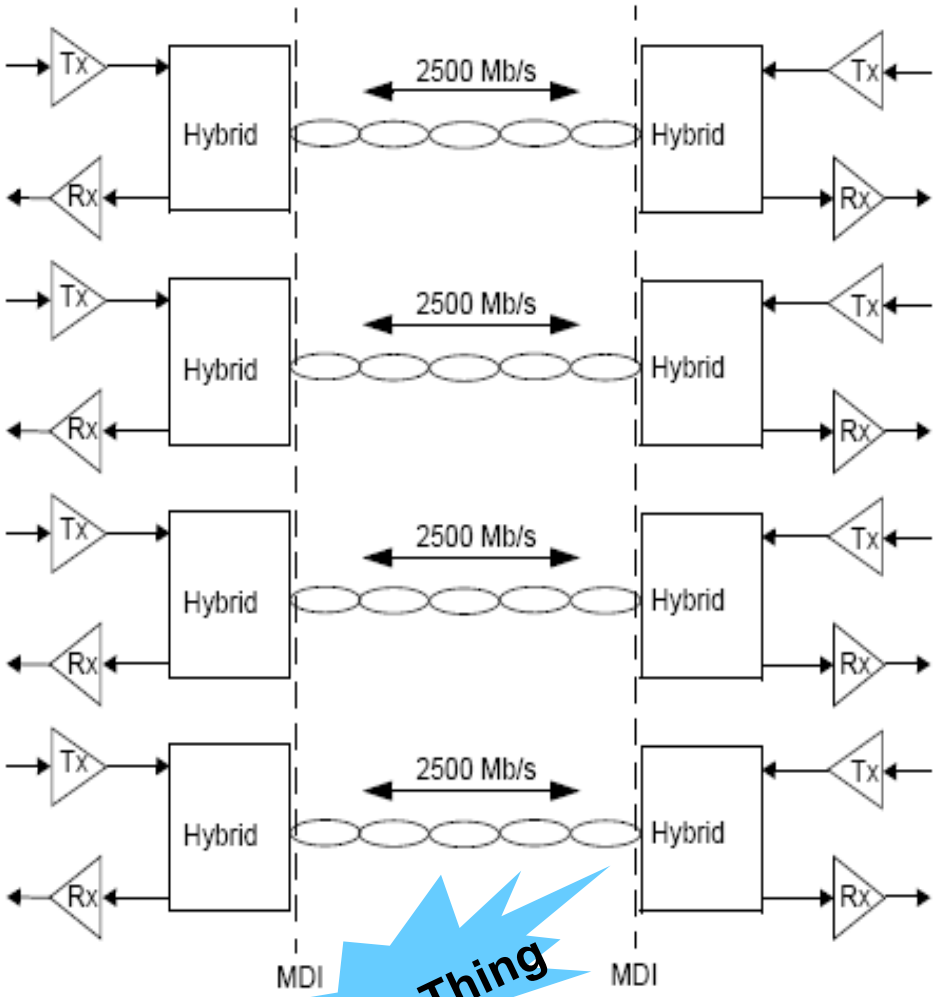
# 10GBASE-T - Overview

- 10GBASE-T provides 10 gigabit/second connections over unshielded or shielded twisted pair cables, over distances up to 100 m. 2.5Gbps per lane (A, B, C & D)
- Baseband 16-level PAM signaling with a modulation rate of 800 Msymbols per second is used on each of the wire pairs.
- Supports full duplex operation only
- Compatibility of Auto Negotiation enabled to also operate 10/100/1000 BASE-T
- Supports a BER of less than or equal to 10E-12 on all supported distances and Classes
- Provides a cost advantage over fiber



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# XGbT – 10GBASE-T 发送端测试

| | Measurement | Test Mode | XGbT Features / Notes | Does XGbT cover this measurement? |
|---|---|---|---|---|
| 1 | Maximum output droop | Sub clause 55.5.3.1, Test Mode 6 | Flexibility to test beyond compliance – XGbT provides the flexibility to perform testing beyond what is specified in IEEE standard 802.3an-2006. It helps users to analyze their PHY in addition to compliance tests. | Yes |
| 2 | Transmitter timing jitter – Master | Sub clause 55.5.3.3, Test Mode 2 | Measure Jitter down to just few picoseconds. Software Filters are designed and applied on the acquired data automatically while performing measurements. | Yes |
| 3 | Transmit clock frequency | Sub clause 55.5.3.5,Test Mode 2 | Exact value PPM for measured clock frequency is provided | Yes |
| 4. | Transmitter timing jitter – Slave | Sub clause 55.5.3.3, Test Mode 1 ans Mode 3 | Measure Jitter down to just few picoseconds. Software filters are designed and applied on the acquired data automatically while performing measurements. | Yes |
| 5 | Transmitter linearity | Sub clause 55.5.3.2, Test Mode 4. Tones 1-5 | Spectral Features of the scope are used to perform the measurement, a methodology that is unique to Tektronix and approved by UNH-IOL | Yes |
| 6 | Transmitter power spectral density (PSD) and power level | Sub clause 55.5.3.4, Test Mode 5 | Spectral Features of the scope are used to perform the measurement, a methodology that is unique to Tektronix and approved by UNH-IOL | Yes |
| 7. | Return Loss | Sub clause 55.8.2.1, Test Mode 5 | Return Loss is not part of XGbT solution for now, however it will finally be released in next version. For time gap arrangement please request product line for Return Loss utility | Yes** |

# Transmitter Power Spectral Density (PSD) and Power Level
# 发送端功率谱密度及功率值

- **目的**：确保发送端功率谱密度和功率值满足规范要求。
- 功率值应在3.2dBm~5.2dBm范围内

  功率谱密度曲线应介于规范要求的上下限曲线之间。
- 需进入Test Mode 5
- IEEE 标准 802.3an-2006, 55.5.3.4条目。
- Test Mode 5：

  正常操作模式




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# TF-XGbT Test Fixture

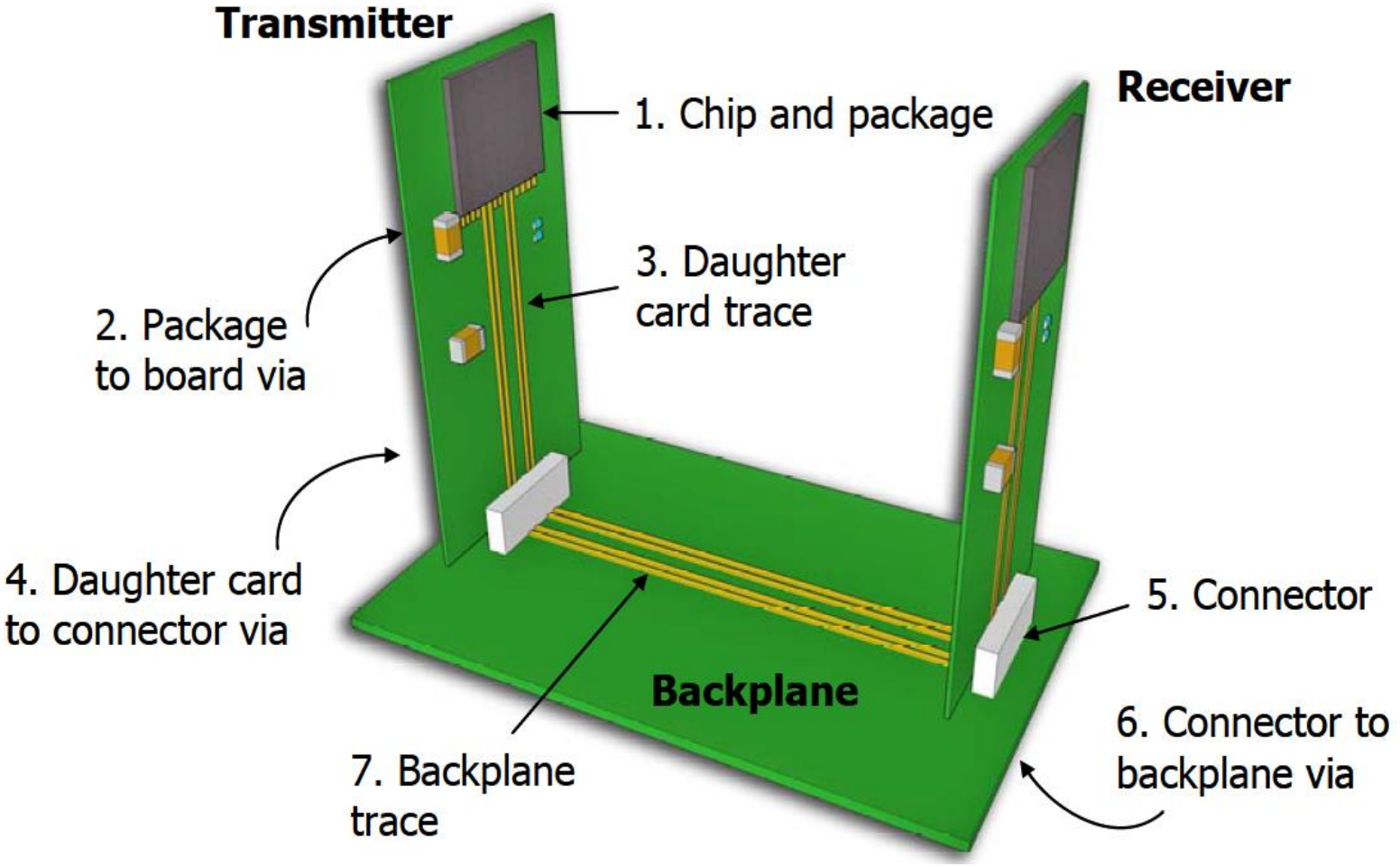
- The XGbT test fixture provides easy access to the 10GBASE-T Electrical signals to perform conformance testing and device characterization as described in of IEEE 802.3an-2006 sub-clause 55.5.3 & 55.8.2.1. This fixture is used with the Tektronix's XGbT- 10GBASE-T Automation Solution to provide fast and accurate design debugging and validation. XGbT fixture covers all seven measurements including Jitter Slave and MDI Return Loss


Fig 1: XGbT Test Fixture main board

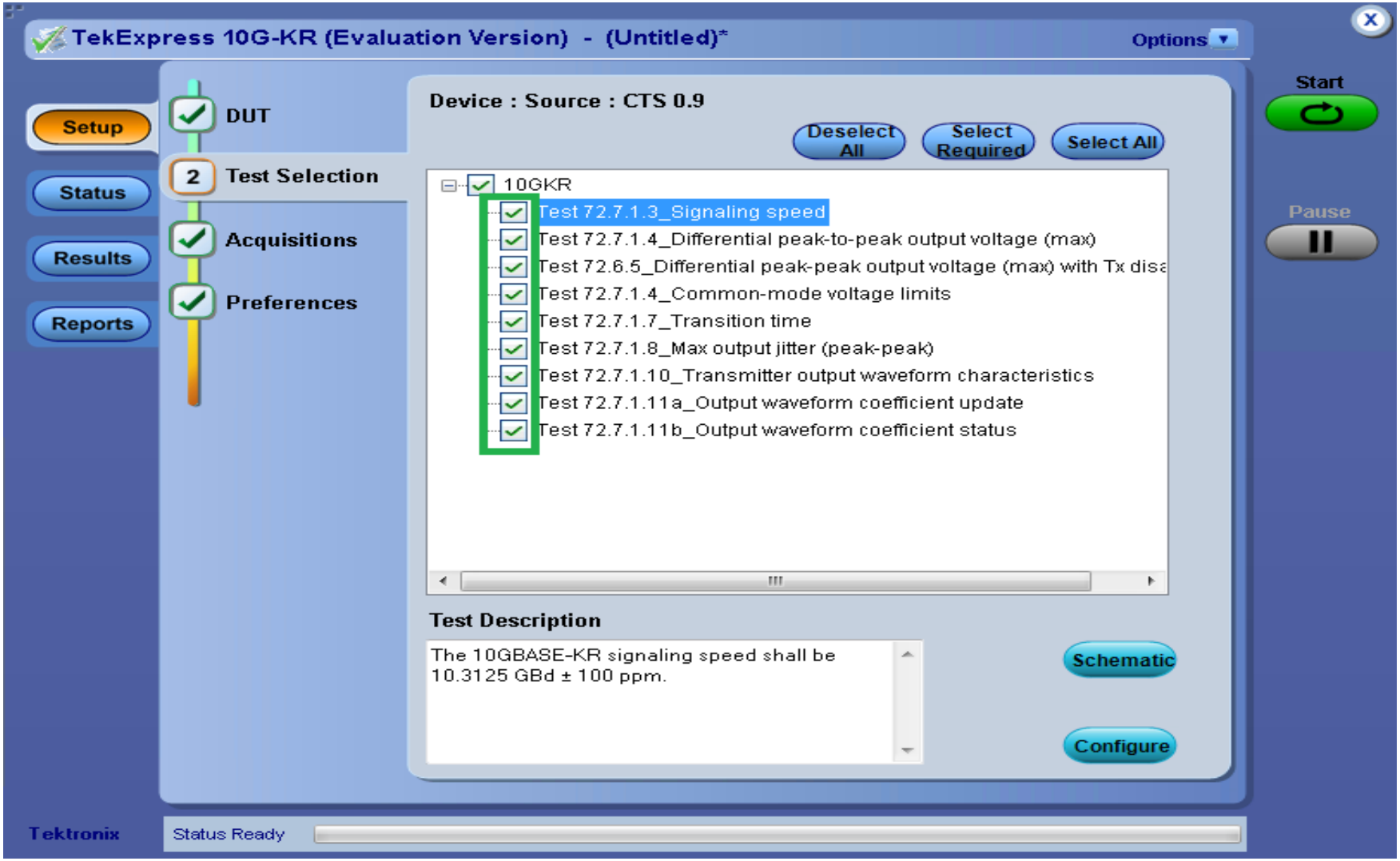

Fig 2: Calibration Board

Figure 3: RJ45 Shielded Patch cord

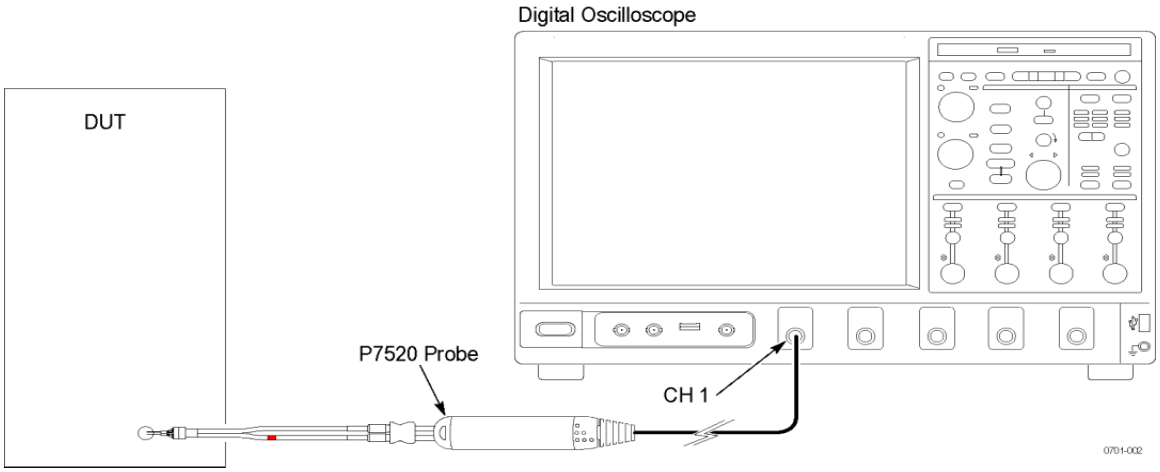
# 10G-KR Typical Backplane Ethernet

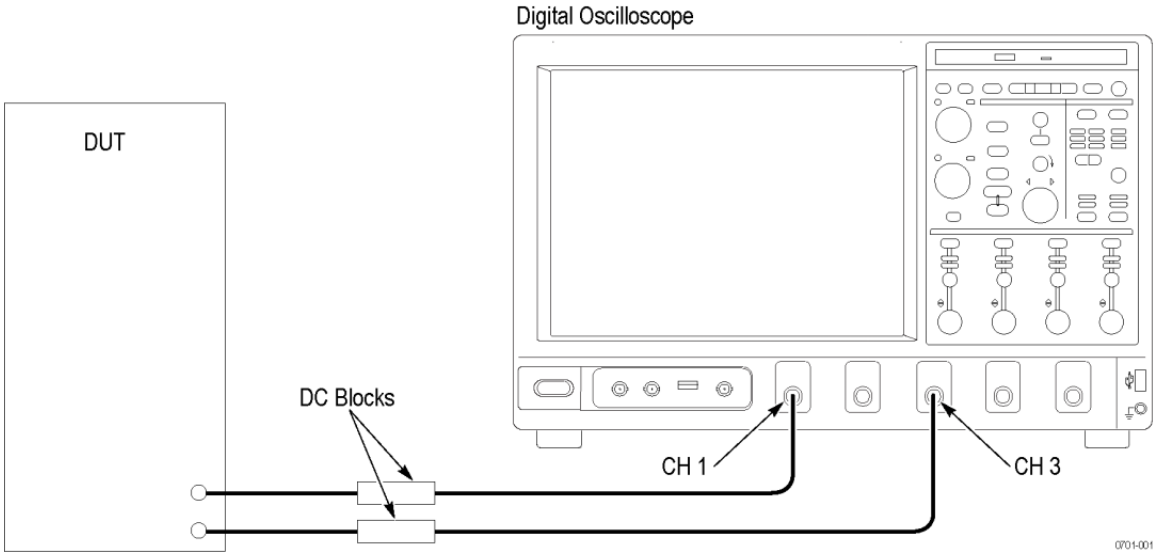


# 10G-KR自动化测试软件

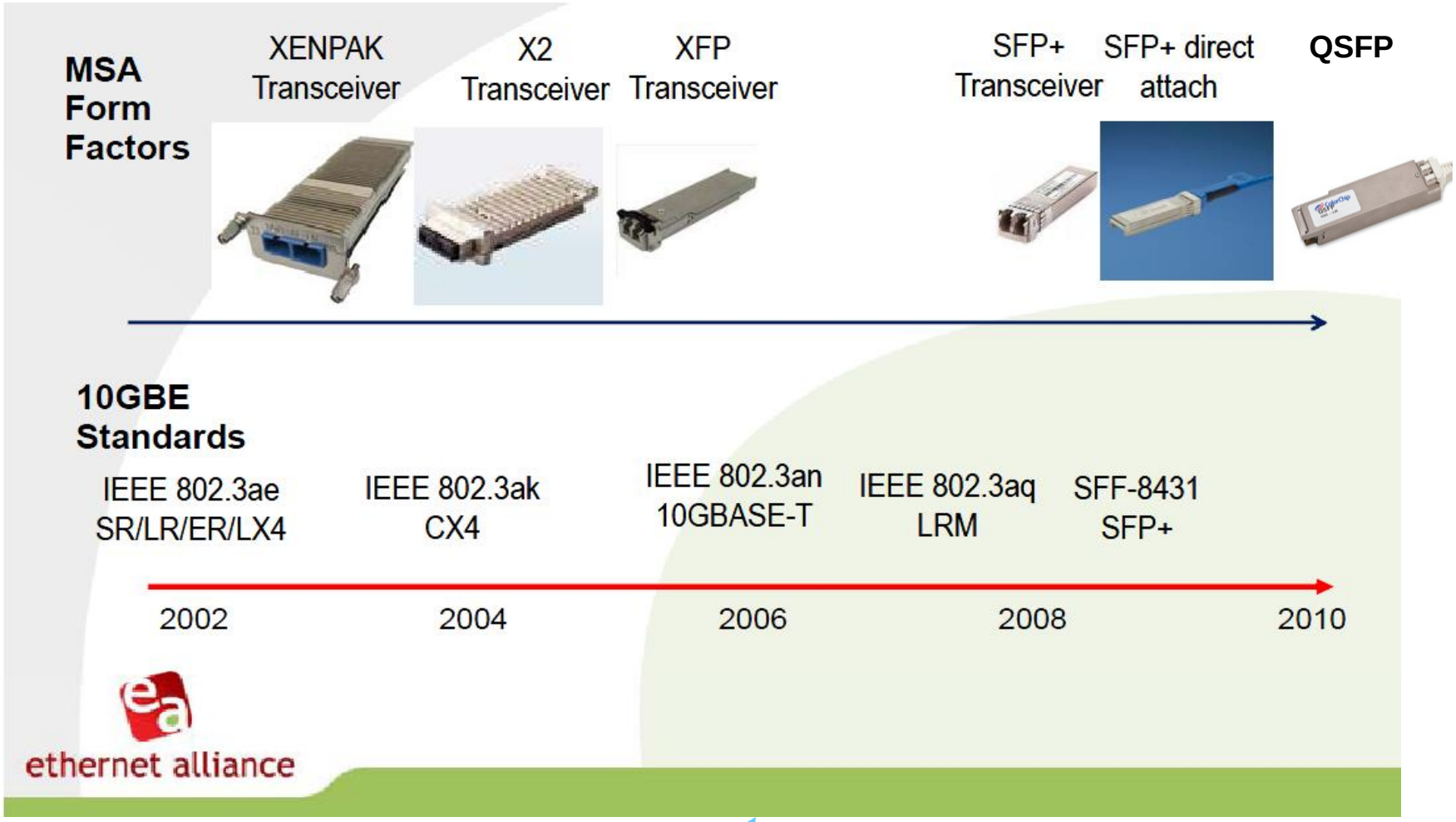


# Testing connection for 10G-KR



# 10Gigabit Ethernet Interface Evolution




Source : Ethernet Alliance

**Next Big Thing**
**SFF-8431**
**SFP+**



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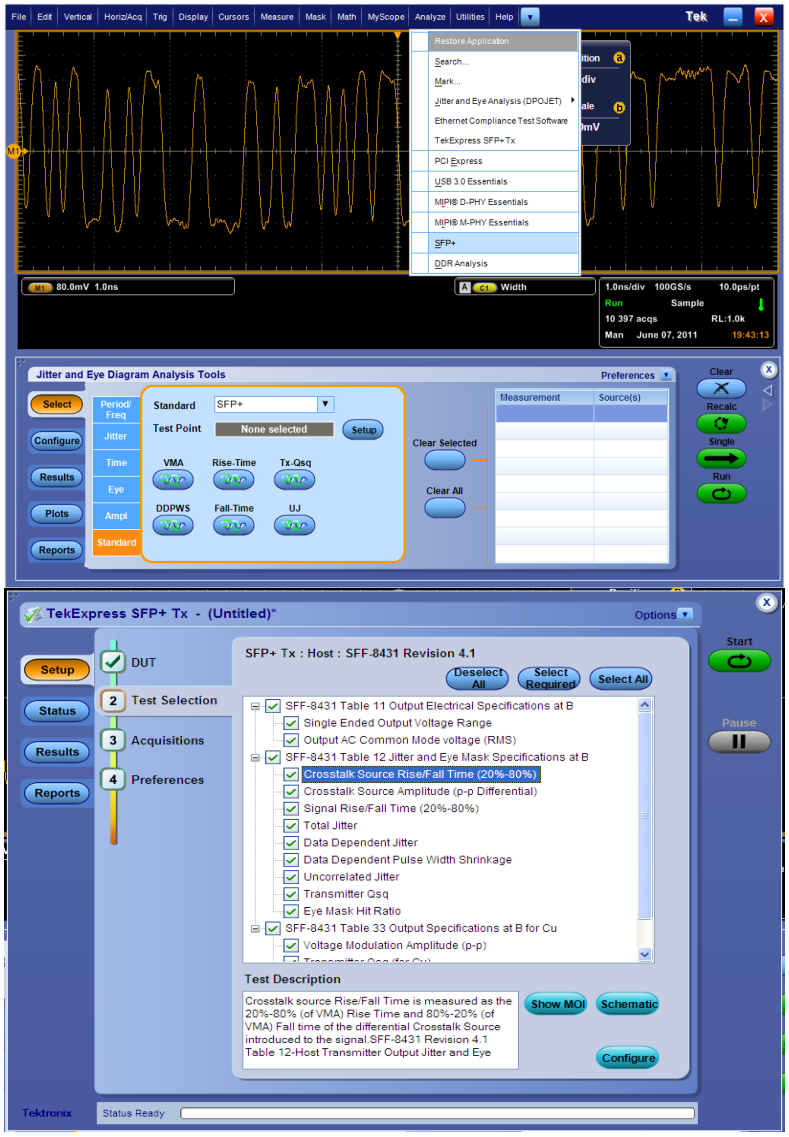
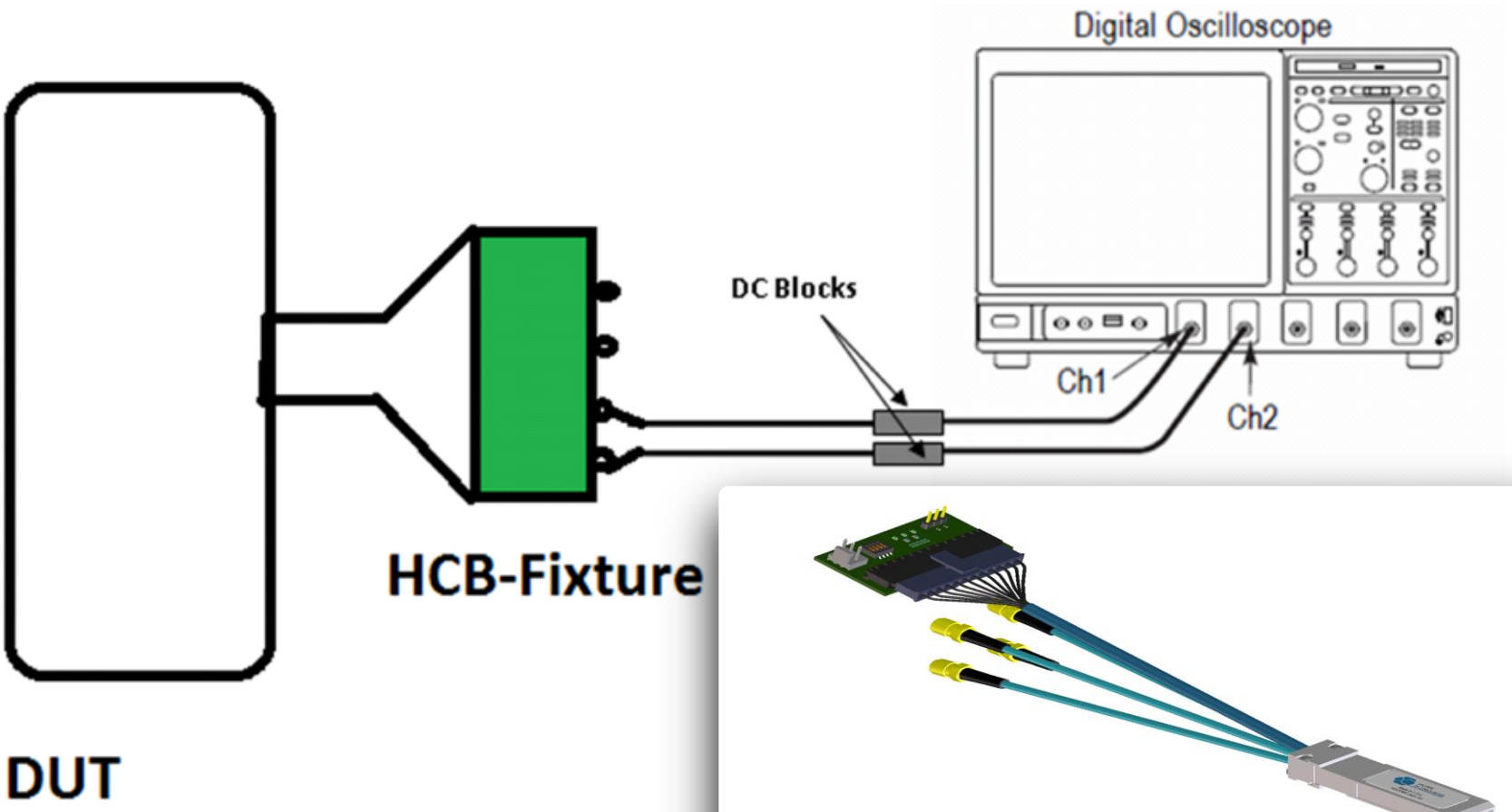
# Tektronix SFP-TX – Automation & DPOJET Option

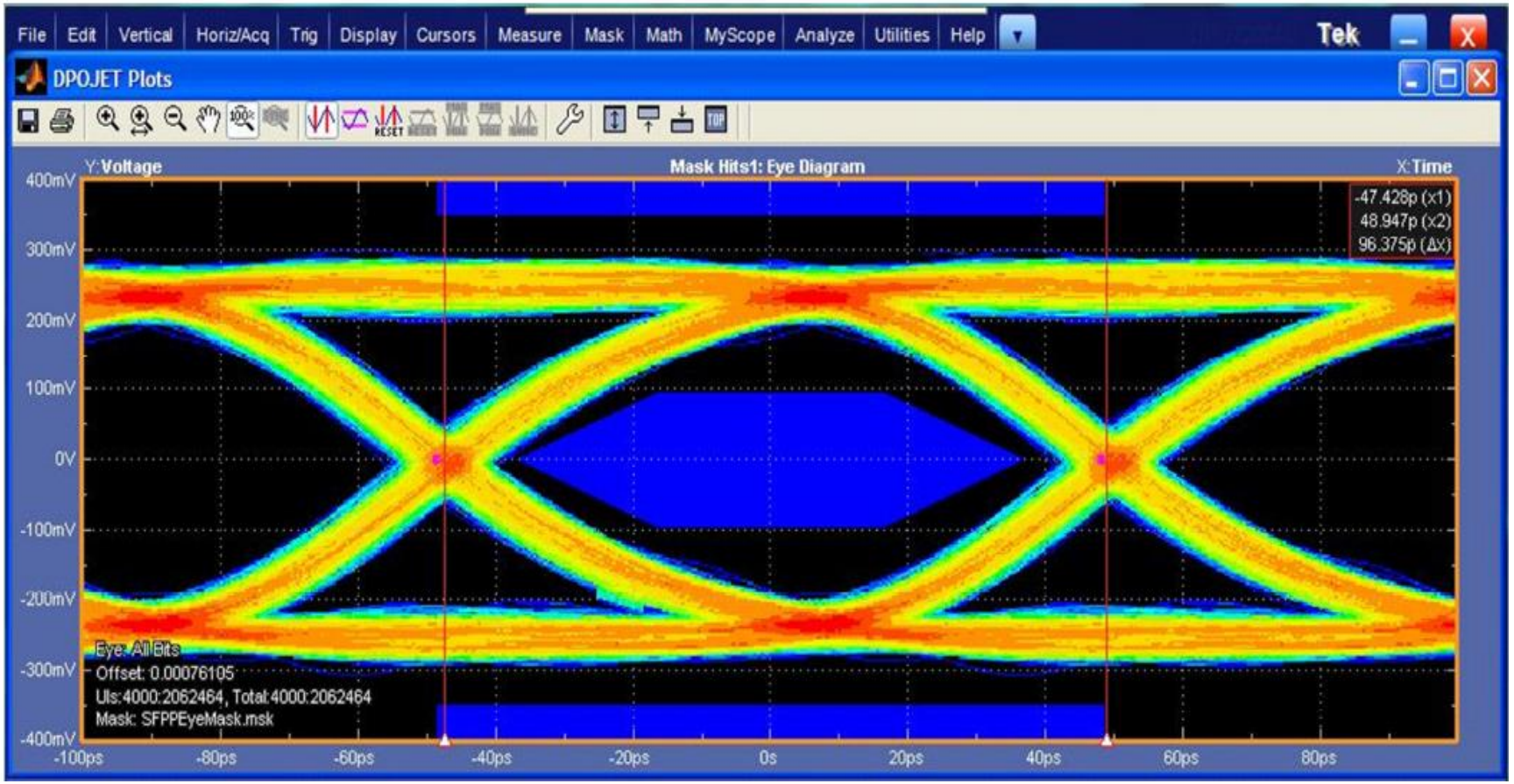
| SL No. | Measuremnts | Signal Type Recommended | Limit Min | Target | Max | Units |
|---|---|---|---|---|---|---|
| Host Transmitter output electrical Specifications: | | | | | | |
| 1 | Single Ended Output Voltage Range | PRBS31 | -0.3 | | 4 | V |
| 2 | Output AC Common Mode voltage (RMS) | PRBS31 | | | 15 | mV(RMS) |
| Host Transmitter Jitter and Eye Mask specifications | | | | | | |
| 3 | Crosstalk source rise/fall time (20%-80%) (Tr, Tf) | 8180 | | 34 | | ps |
| 4 | Crosstalk source amplitude (p-p differential) | 8180 | | 1000 | | mV |
| 5 | Signal rise/fall time (20%-80%) (Tr, Tf) | 8180 | 34 | | | ps |
| 6 | Total Jitter (p-p) (Tj) | PRBS31 | | | 0.28 | UI(p-p) |
| 7 | Data Dependent Jitter (p-p) (DDJ) | PRBS9 | | | 0.1 | UI(p-p) |
| 8 | Data Dependent Pulse Width Shrinkage (p-p) (DDPWS) | PRBS9 | | | 0.055 | UI(p-p) |
| 9 | Uncorrelated Jitter (RMS) (UJ) | PRBS9 | | | 0.023 | UI(p-p) |
| 10 | Transmitter Qsq | 8180 | 50 | | | |
| 11 | Eye mask hit ratio(Mask hit ratio of 5×10-5) | PRBS31 | X1=0.12UI, X2=0.33UI, Y1=95mV, Y2=350mV | | | |
| Host Transmitter output specifications for Cu (SFP+ host supporting direct | | | | | | |
| 12 | Voltage Modulation Amplitude (p-p) | 8180 | 300 | | | mV |
| 13 | Transmitter Qsq Output AC Common Mode voltage | 8180 | 63.1 | | | |
| 14 | Output AC Common Mode Voltage | PRBS31 | | | 12 | mV(RMS) |
| 15 | Host Output TWDPc | PRBS9 | | | 10.7 | dBe |



# SFP test connection



# SFP Eye Mask hit ratio :less than 5E10-5



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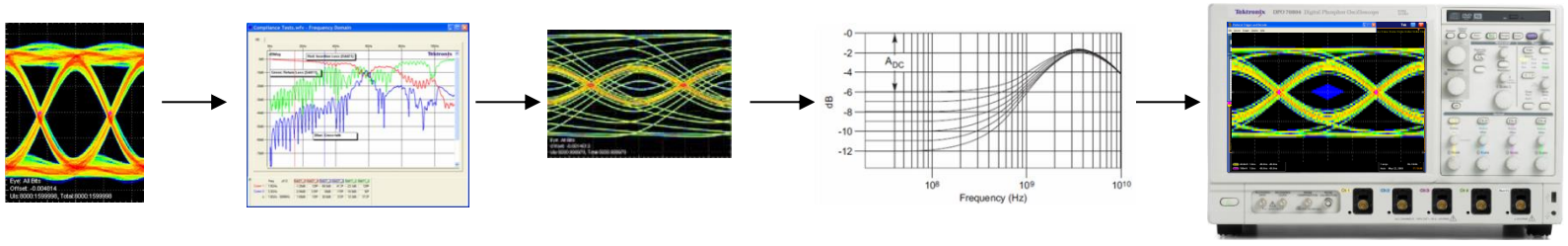
# Add-In Card (CEM Spec) Tx Testing

- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements




Signal Acquired from Compliance Board

Embed Compliance Channel and Package

Closed Eye due to the Channel

Apply CTLE + DFE

Open Eye for Measurements



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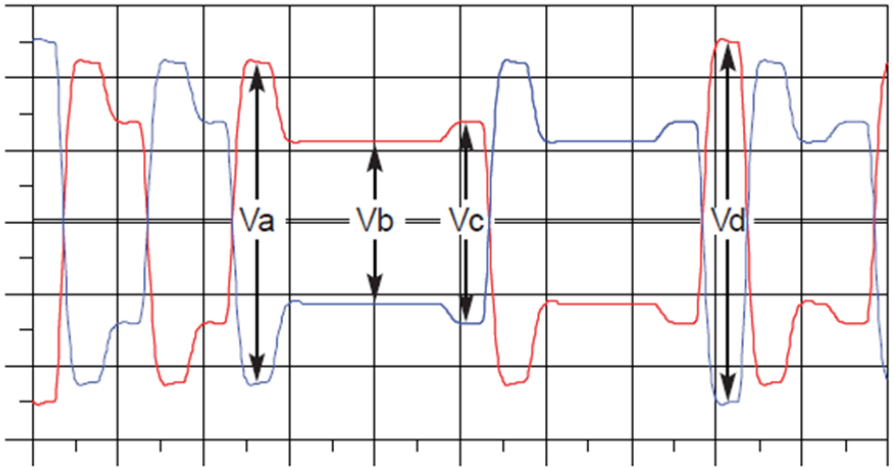
# Compliance Patterns

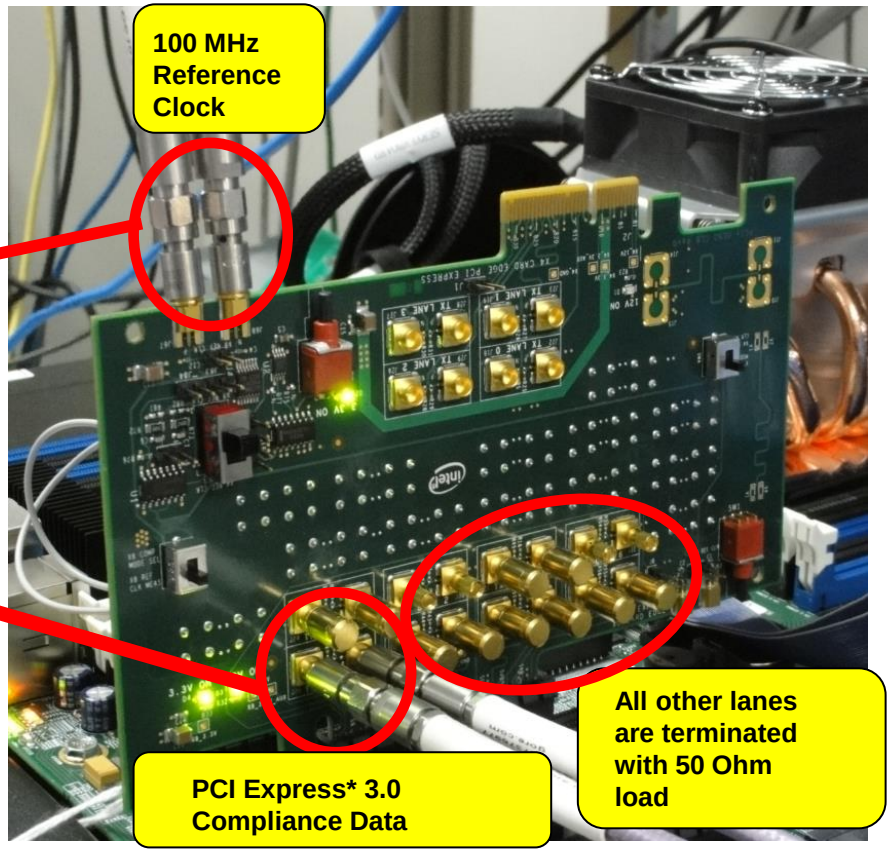
- Once in compliance mode, bursts of 100MHz clock can used to cycle through various settings of compliance patterns to perform, Jitter, voltage, timing measurements.

| Data Rate | Preshoot | De-emphasis |
|---|---|---|
| 2.5 GT/s, | | -3.5 dB |
| 5.0 GT/s, | | -3.5 dB |
| 5.0 GT/s, | | -6.0 dB |
| 8.0 GT/s, | P0 = 0.0 | -6.0±1.5dB |
| 8.0 GT/s, | P1 = 0.0 | -3.5±1.5dB |
| 8.0 GT/s, | P2 = 0.0 | -4.4±1.5dB |
| 8.0 GT/s, | P3 = 0.0 | -2.5±1dB |
| 8.0 GT/s, | P4 = 0.0 | 0.0dB |
| 8.0 GT/s, | P5 = 1.9±1dB | 0.0dB |
| 8.0 GT/s, | P6 = 1.9±1dB | 0.0dB |
| 8.0 GT/s, | P7 = 1.9±1dB | -6.0±1.5dB |
| 8.0 GT/s, | P8 = 1.9±1dB | -3.5±1dB |
| 8.0 GT/s, | P9 = 1.9±1dB | 0.0dB |
| 8.0 GT/s, | P10 = 1.9±1dB | Test Max Boost Limit |




De-emphasis = $20\log_{10}$ Vb/Va
Preshoot = $20\log_{10}$ Vc/Vb
Boost = $20\log_{10}$ Vd/Vb

# PCIE Dual-Port TX Measurement Example for System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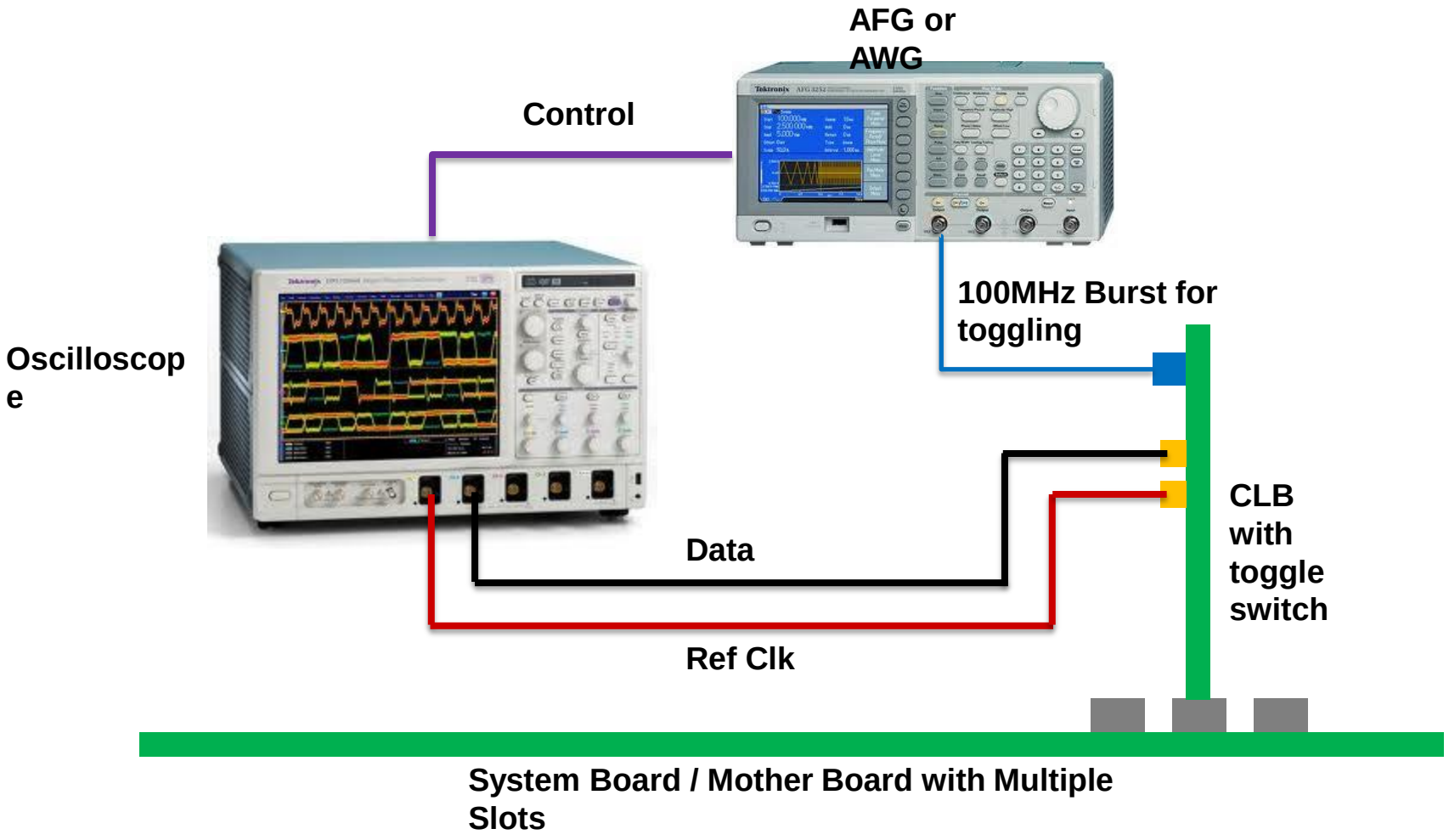
# Automated DUT Control



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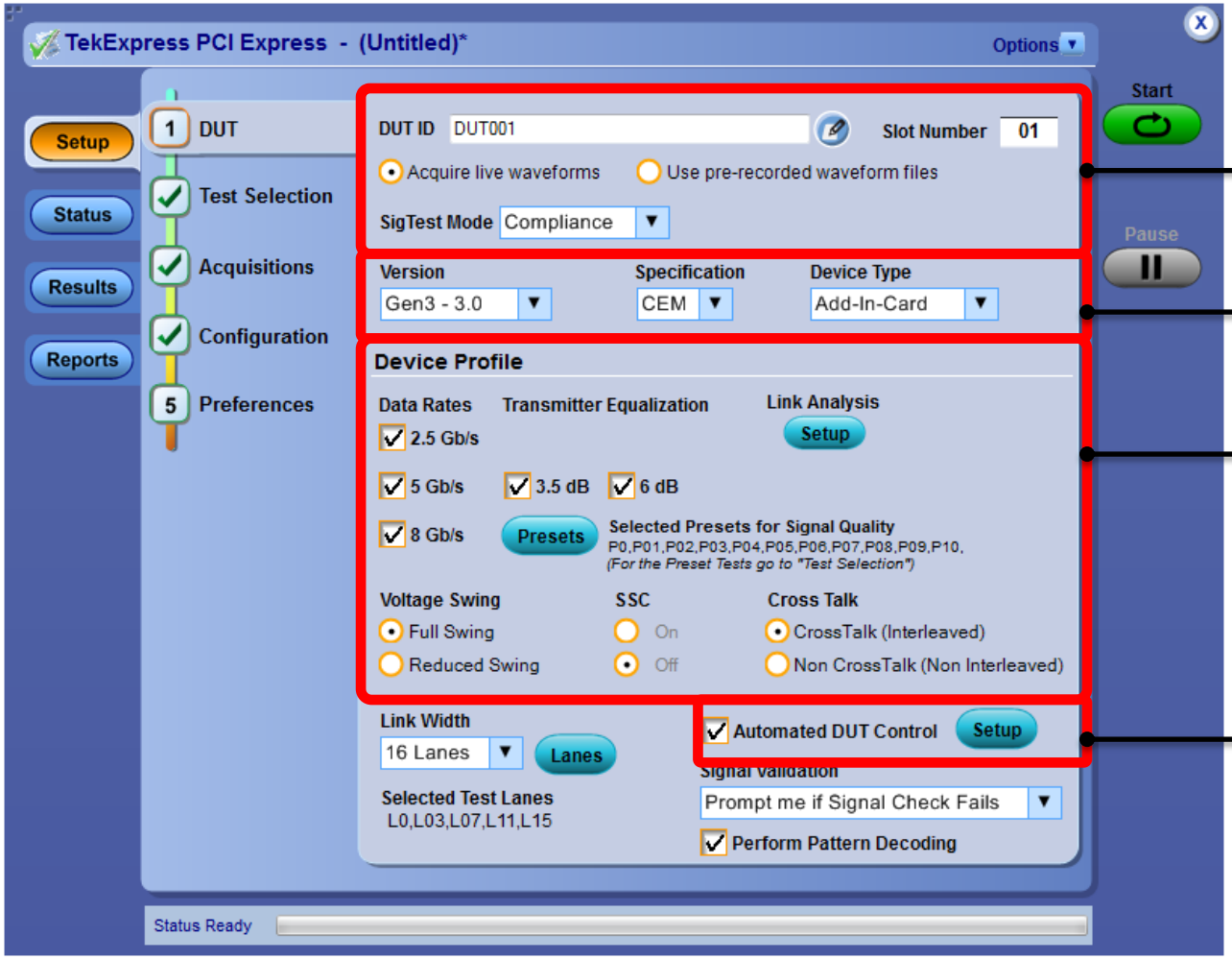
# TekExpress Automation for Tx Compliance - Setup




Run Analysis on Live or Pre-Recorded Data

Type of test / device selection

Test selection

Automate DUT control



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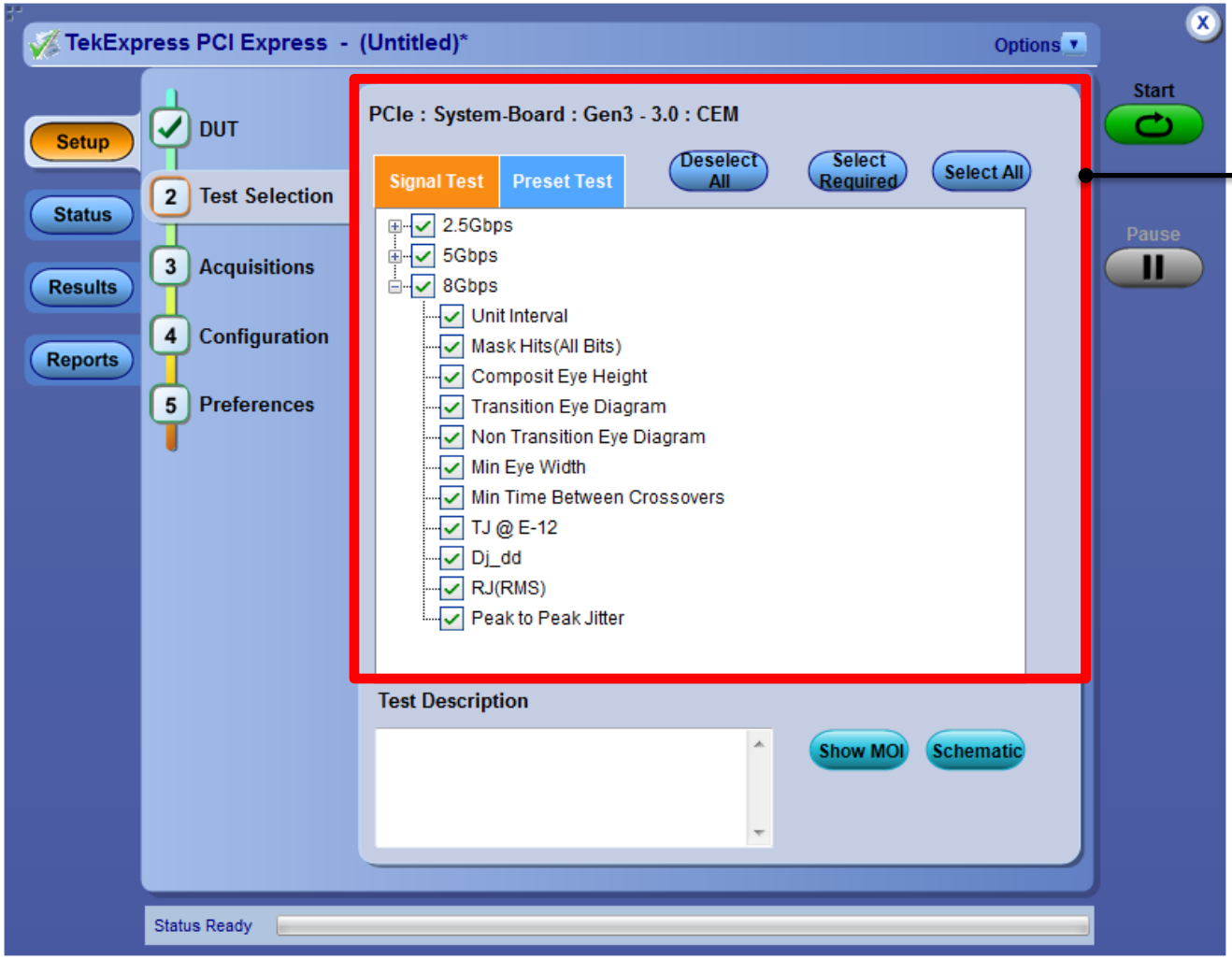
# TekExpress Automation for Tx Compliance – Test




**Test Selection**



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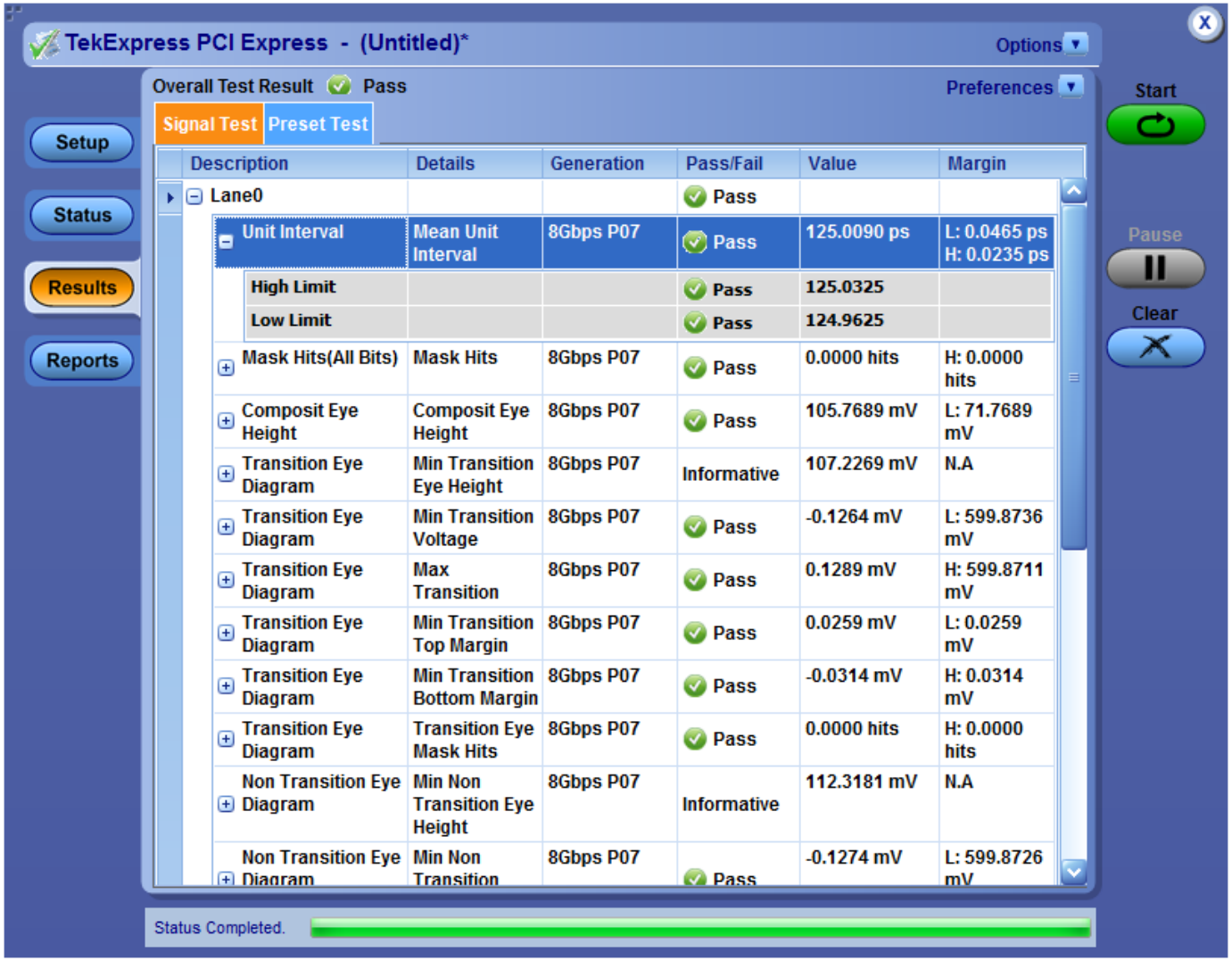
# TekExpress Automation for Tx Compliance – Reports



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# TekExpress Automation for Tx Compliance – Reports

Tektronix Enabling Innovation

## TekExpress PCI Express

### Add-In-Card Test Report

| Setup Information | |
|---|---|
| | DPOJET Version : 6.0.1 Build 8 |
| | Scope Model : DPO73304D |
| | Scope Serial Number : B241123 |
| DUT ID : DUT001 | SPC, FactoryCalibration : PASS;PASS |
| Date/Time : 2013-06-10 17:28:45 | Scope F/W Version : 6.7.4 Build 3 |
| Device Type : PCIe | Probe1 Model : TCA292D |
| TekExpress Version : PCI Express:2.0.0.66 (Beta_Build) Framework:3.0.0.16_RevD | Probe1 Serial Number : N/A |
| Spec Version : Gen3 - 3.0 | Probe2 Model : TCA292D |
| SigTest Version : 3_2_0 | Probe2 Serial Number : N/A |
| Slot Number : 01 | Probe3 Model : TCA292D |
| Overall Execution Time : 0:03:21 | Probe3 Serial Number : N/A |
| Overall Test Result : Pass | Probe4 Model : TCA292D |
| | Probe4 Serial Number : N/A |
| | Signal Source Model : AFG3252 |
| | Signal Source Serial Number : C010899 |
| DUT Comment :DUT001 | |

| Test Name:Summary Table | |
|---|---|
| Unit Interval | Pass |
| Mask Hits(All Bits) | Pass |
| Composit Eye Height | Pass |
| Transition Eye Diagram | Pass |
| Non Transition Eye Diagram | Pass |
| Min Eye Width | Informative |
| Min Time Between Crossovers | Informative |
| mhtml:file://X:\PCI Express\Reports\DUT081.mht#TJ @ E-12 | Pass |
| Dj_dd | Informative |
| RJ(RMS) | Pass |
| Peak to Peak Jitter | Informative |

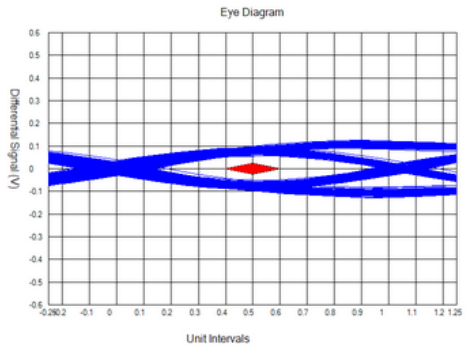
Unit Interval

| Measurement Details | Lane Name | DataRate | Equalization | Measured Value | Test Result | Margin | Low Limit | High Limit | Comments |
|---|---|---|---|---|---|---|---|---|---|
| Mean Unit Interval | Lane0 | 8Gbps | P07 | 125.0090 ps | Pass | L: 0.0465 ps H: 0.0235 ps | 124.9625 | 125.0325 | |

Back To Summary Table

**Transition Eye Diagram**

Transition Eye - Lane0 8Gbps P07

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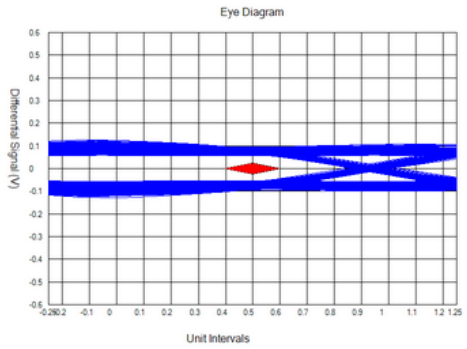
**Non Transition Eye Diagram**

Non Transition Eye - Lane0 8Gbps P07




Back To Summary Table



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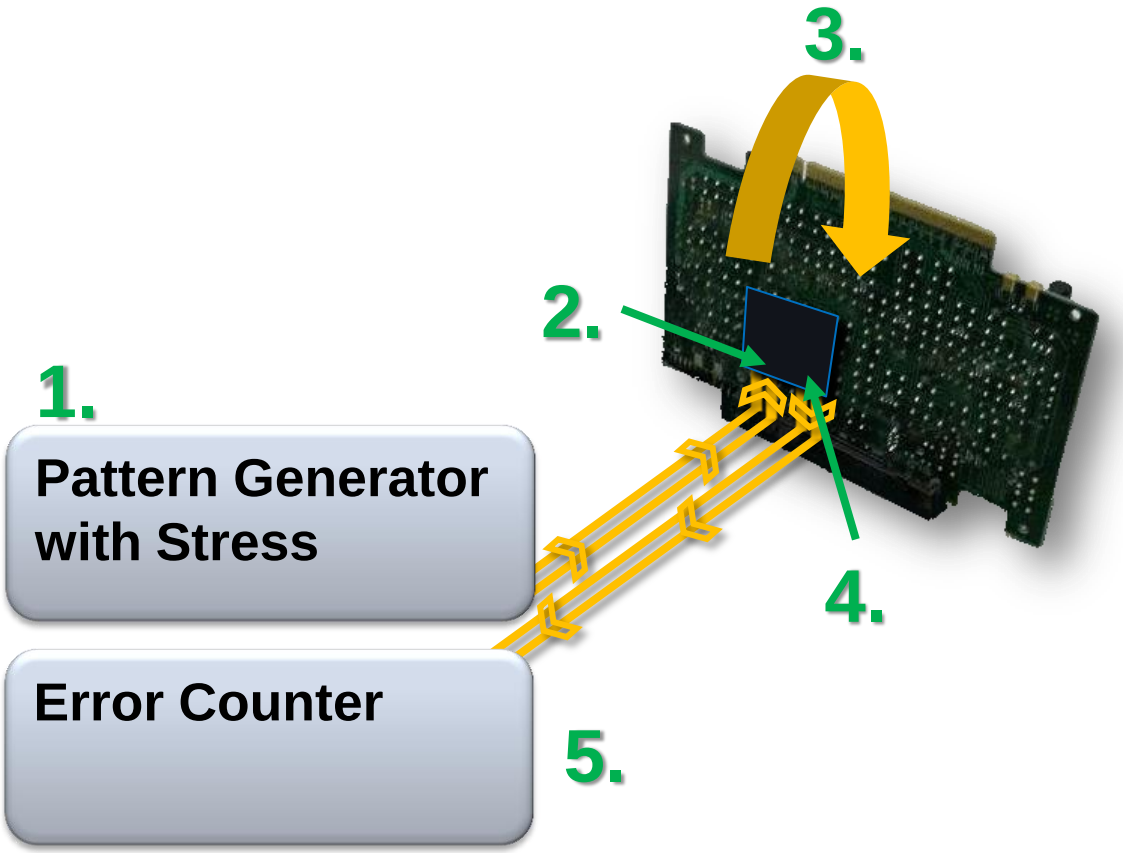
# Basic Receiver Testing




**At the simplest level, receiver testing is composed of:**

1. **Send impaired signal to the receiver under test**
2. **The receiver decides whether the incoming bits are a one or a zero**
3. **The chip loops back the bit stream to the transmitter**
4. **The transmitter sends out exactly the bits it received**
5. **An error counter compares the bits to the expected signal and looks for mistakes (errors)**



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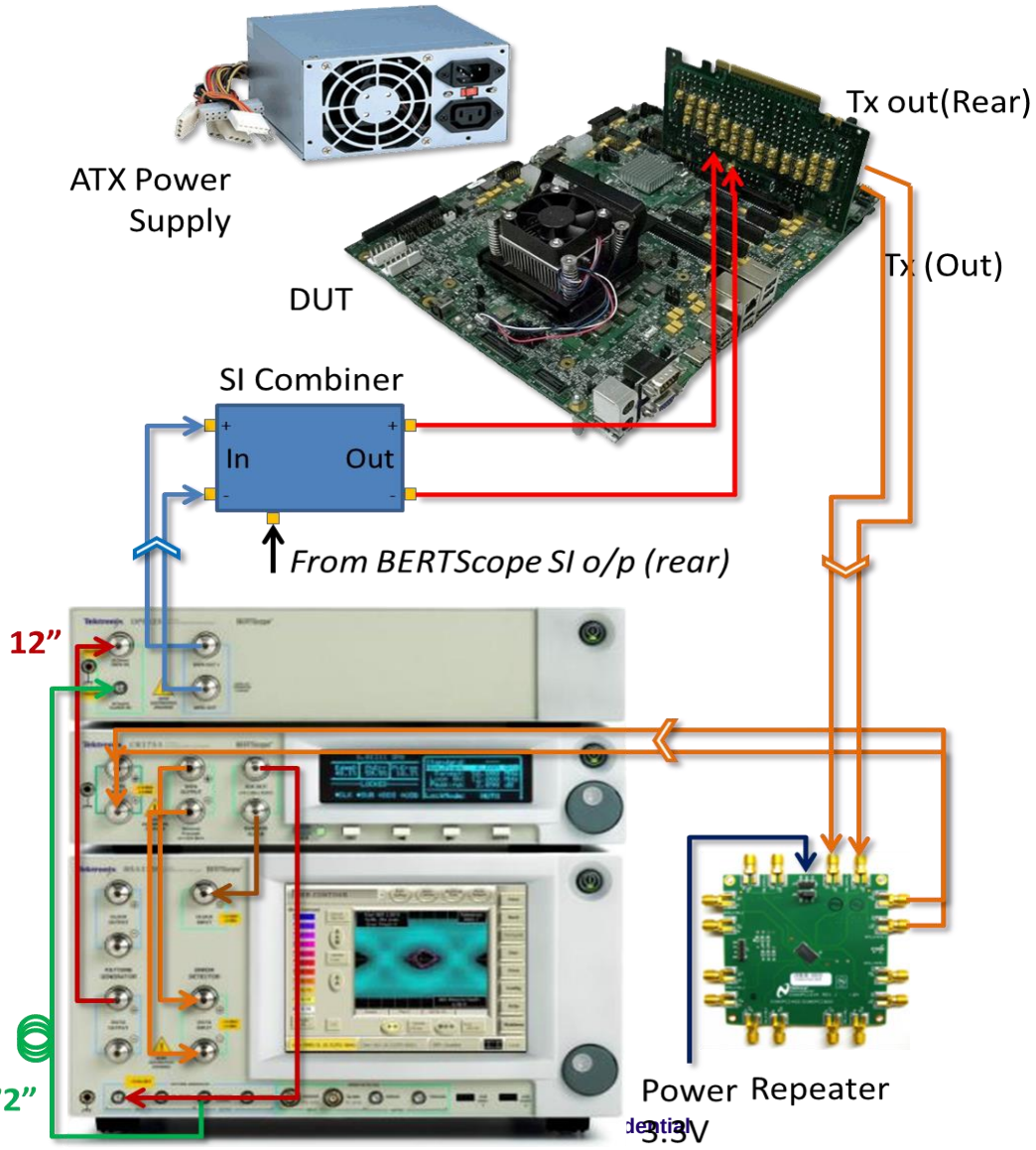
# RX Measurement Example for Host



# USB 3.0 Key Considerations

- Receiver Testing Now Required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues
- Channel Considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs
- New Challenges
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx

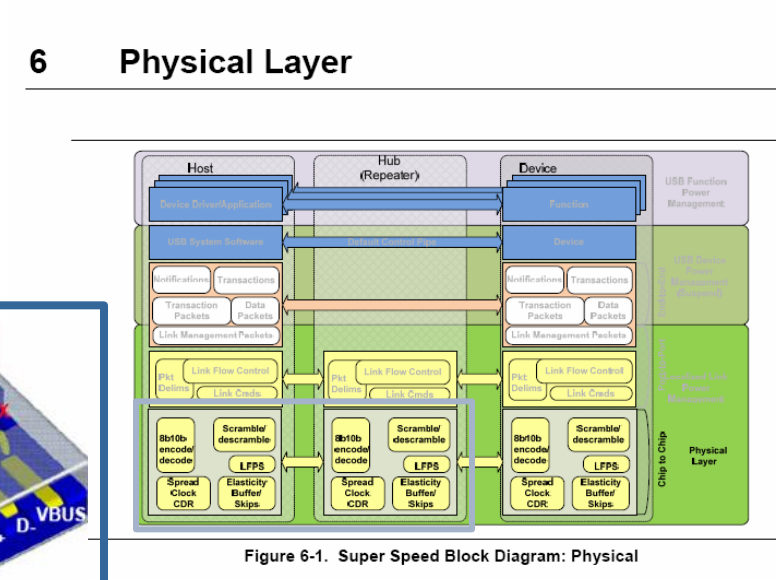



Figure 6-1. Super Speed Block Diagram: Physical

**Source: USB 3.0 Rev 1.0 Specification**

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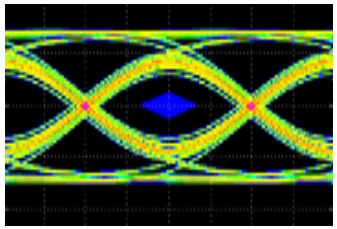
# USB 3.0 Compliance Test Configuration

- USB 3.0 is a closed eye specification
  - Reference channel is embedded and CTLE is applied
- USB 3.0 Reference Channels
  - Host Reference Channel
    - 11” back panel is applied for device testing
  - Device Reference Channel
    - 5” device channel is applied for host testing
  - 3 Meter Reference Cable
    - Used for host and device (except captive devices) testing in addition to reference channels
- USB 3.0 Reference Equalizer
  - Attenuates the low frequer t of the signal to open th



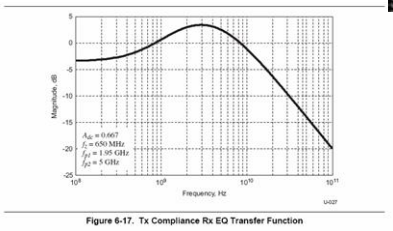
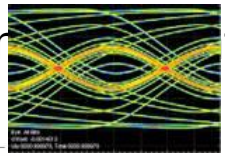


Figure 6-17. Tx Compliance Rx EQ Transfer Function



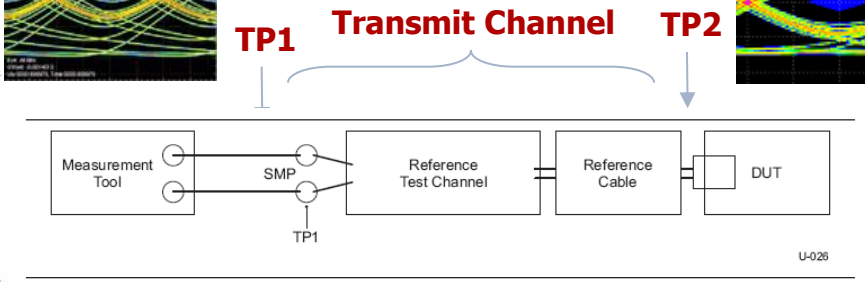
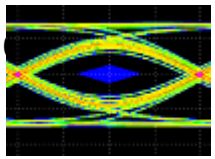
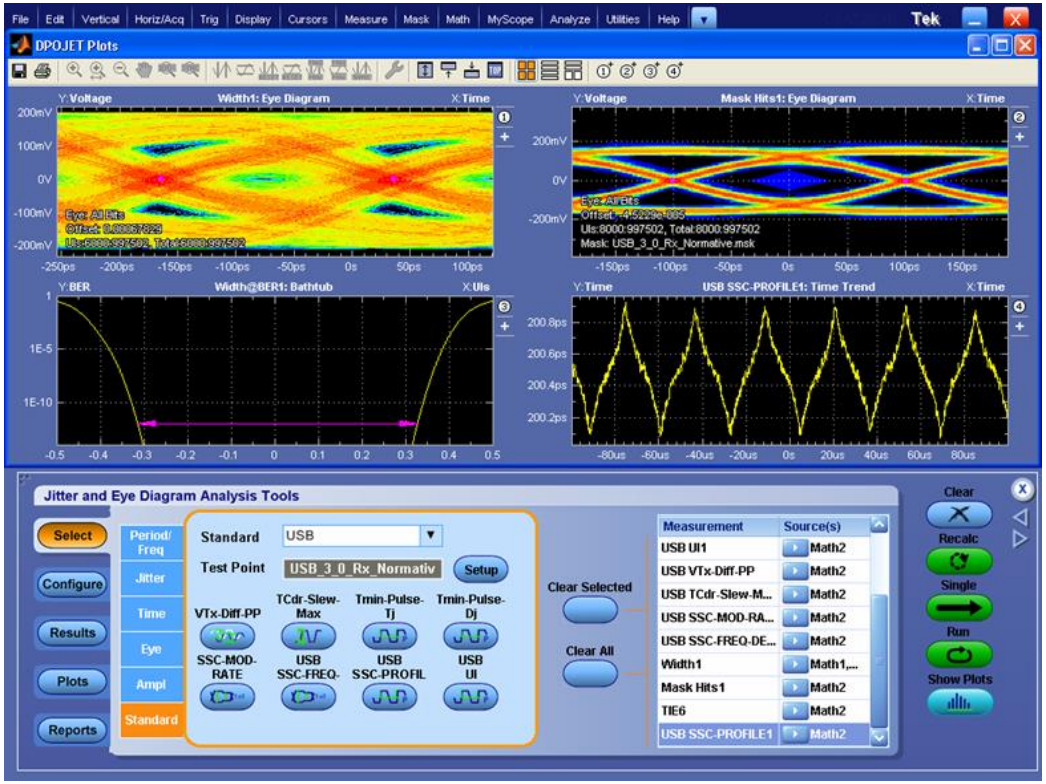


Figure 6-14. Tx Normative Setup with Reference Channel



# USB 3.0 Transmitter Measurement Overview

- Voltage and Timing
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate
- Low Frequency Periodic Signaling (LFPS)
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod
- SSC
  - Modulation Rate
  - Deviation



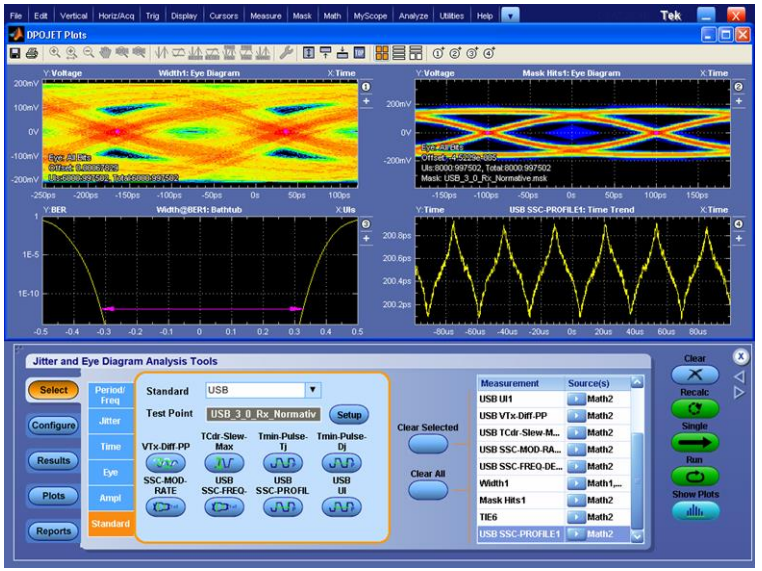

  

# Complete USB 3.0 Transmitter Solution

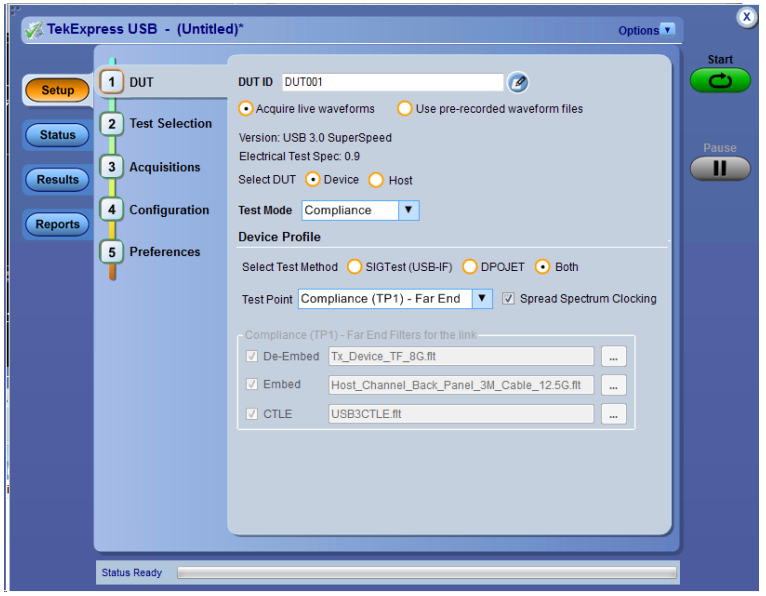
*DPO/DSA70000 Series Oscilloscopes*

- Go Beyond Compliance Testing
  - Debug Suite with DPOJET
  - SDLA for Channel Modeling
  - Tektronix Super Speed USB Fixtures
- Automation software for characterization and compliance
  - TekExpress with option USB-TX (includes option USB3)
- Recommended Scope
  - 12.5 GHz Real-Time Scope
    - 50 GS/s Sample Rate
  - P7313SM[illegible]e
    (Optiona[illegible]

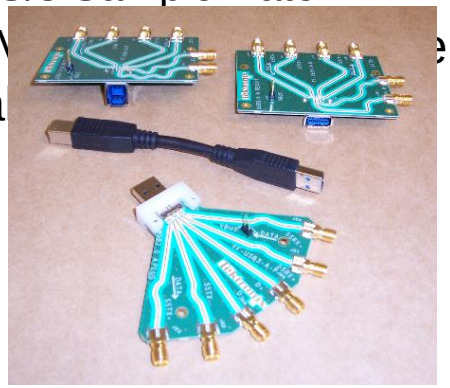
***Opt. USB3***




***Opt. USB-TX***




***TF-USB3-AB-KIT***



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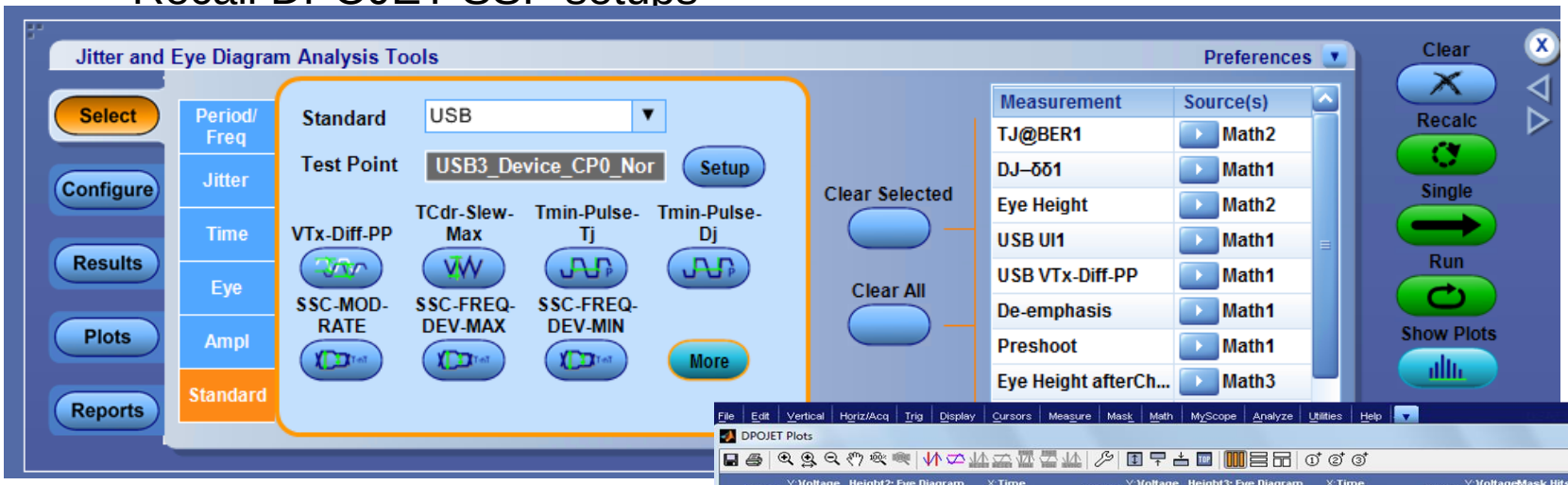
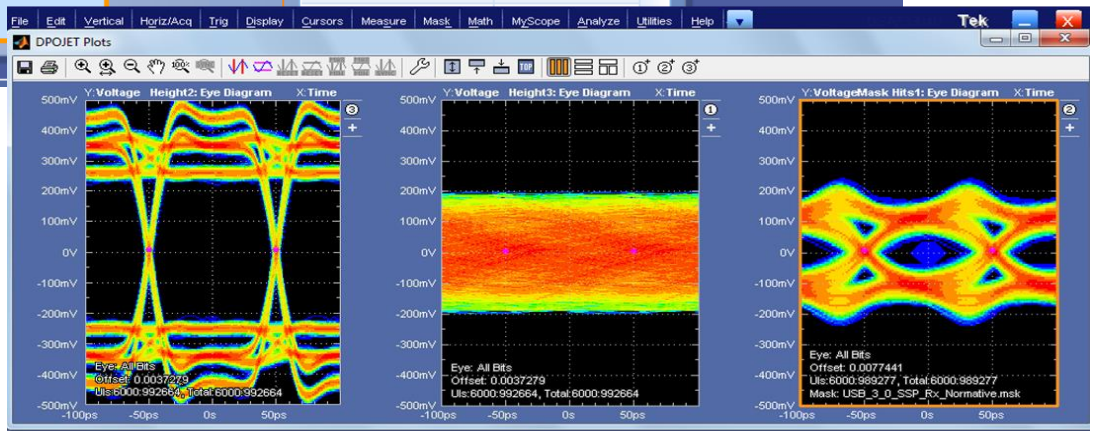
# Increasing Serial Data Bandwidth

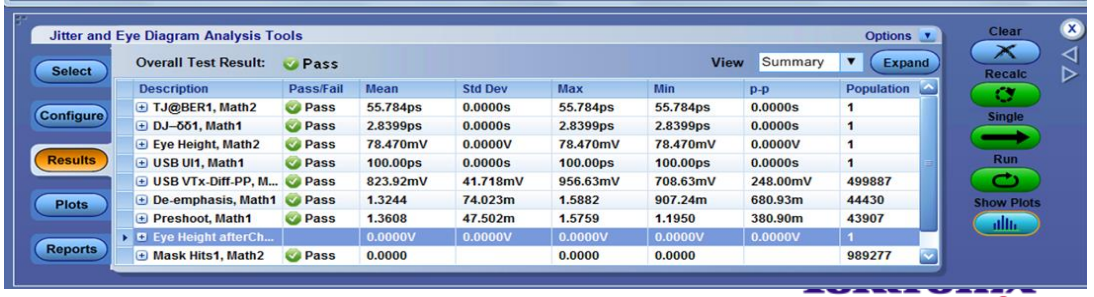
- **USB 2.0, 480 Mb/s** (2000)
  - Shift from slower, wide, parallel buses to narrow, high speed serial bus
  - 40x faster data rate, support for new connectors & charging
- **USB 3.0, 5 Gb/s** (2008)
  - ~10x faster data rate over 3 meter cable
  - Faster edges, ‘closed eye’ architecture
- **USB 3.0, 10 Gb/s** (2013)
  - 2x faster data rate over 1 meter cable
  - ‘Scaled’ SuperSpeed implementation

# Transmitter Validation Example - DPOJET

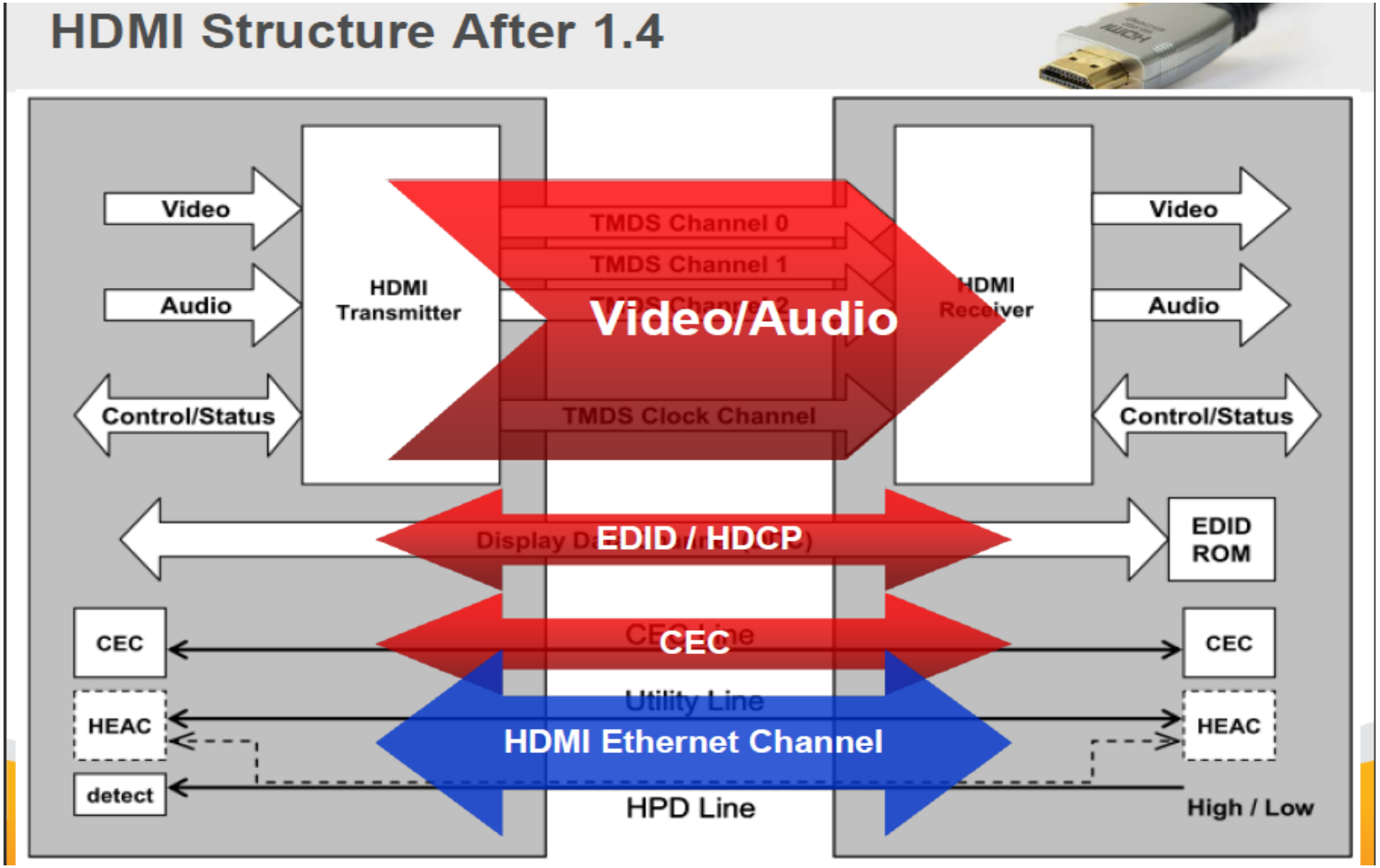
- Recall DPOJET SSP setups



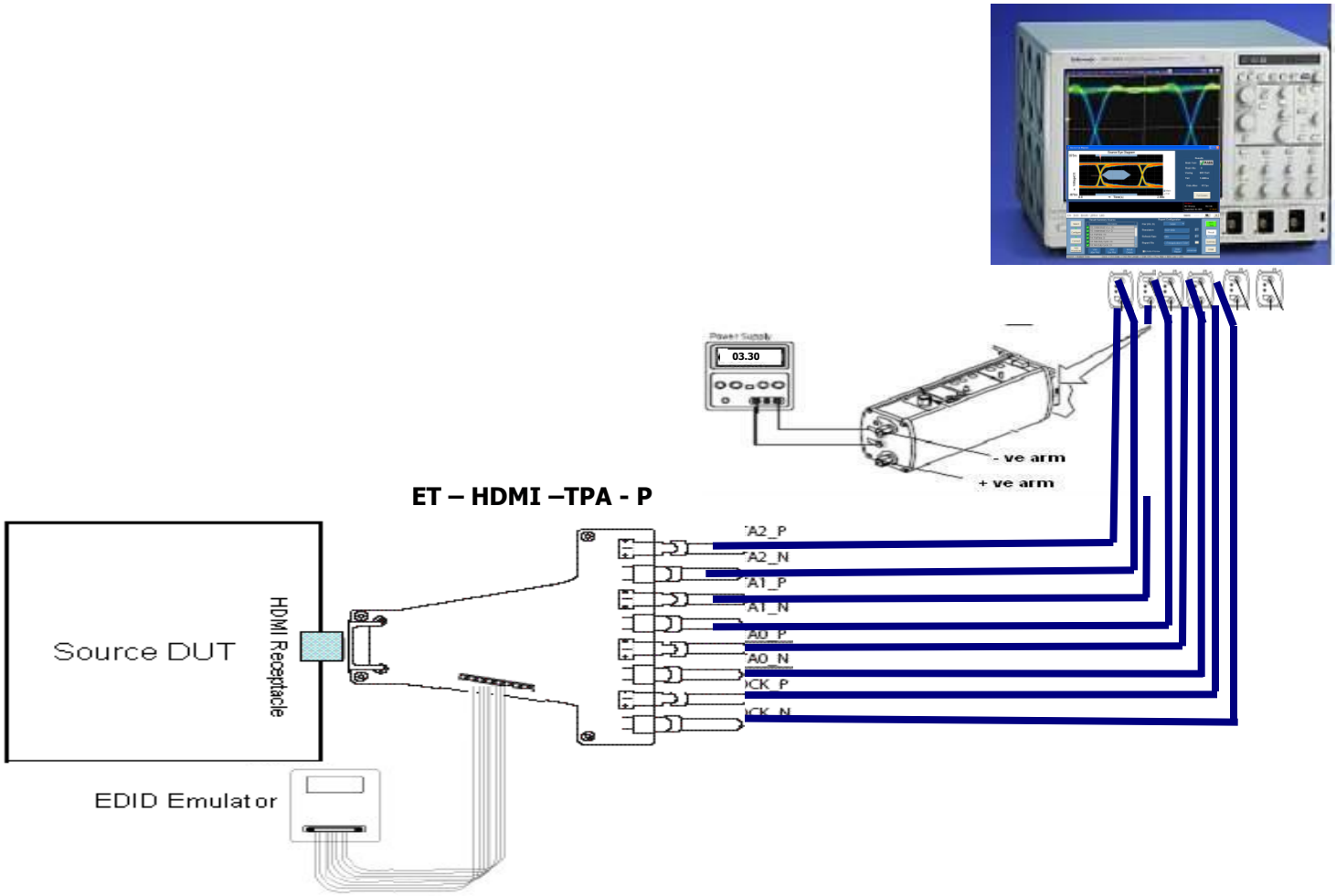



# HDMI Basics



# HDMI 测试方案-源端



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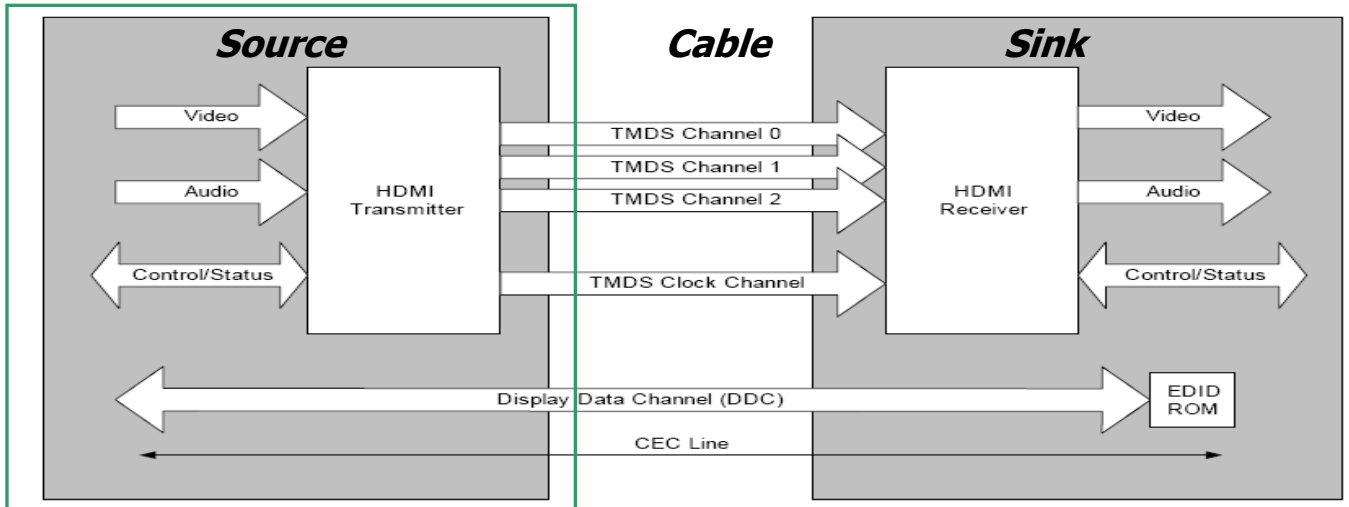
# HDMI Source Testing



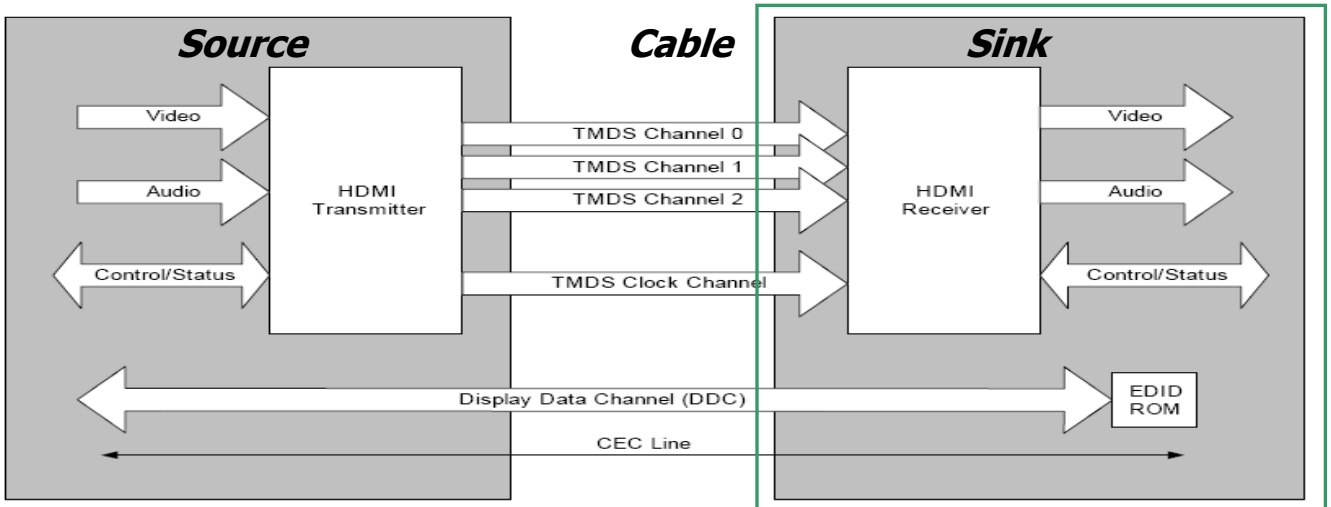

- **Rise/Fall Time**
- **Inter-pair Skew**
- **Clock Duty Cycle**
- **Clock Jitter**
- **Eye Diagram**

**Differential**

- **Voltage VL**
- **Intra-pair Skew**

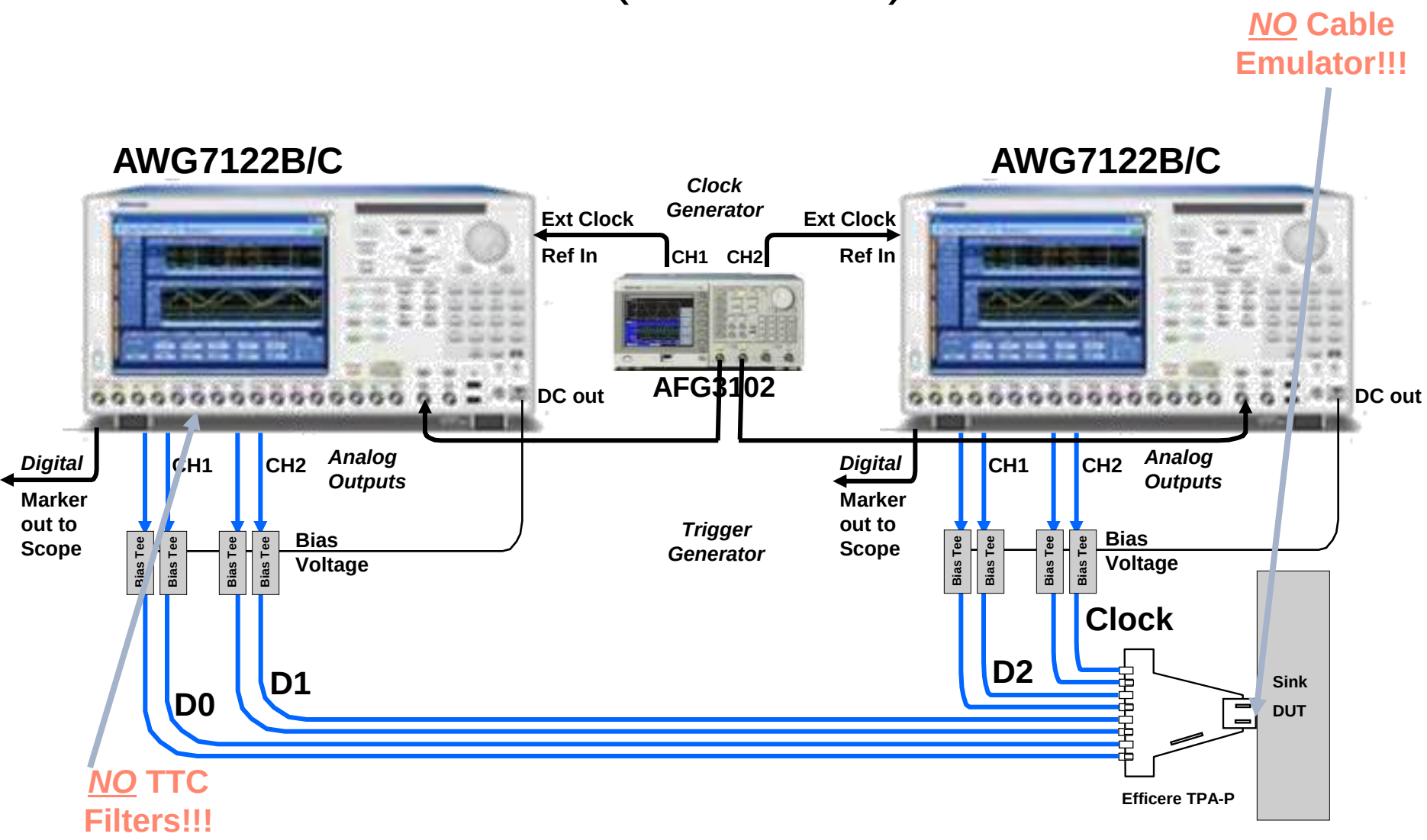
**Single-ended**

# HDMI Sink Testing




- **Jitter Tolerance**
- **Min/Max Differential Swing**
- **Intra-Pair Skew**
- **Differential Impedance**

# HDMI 测试方案-接收端(TV/Monitor)



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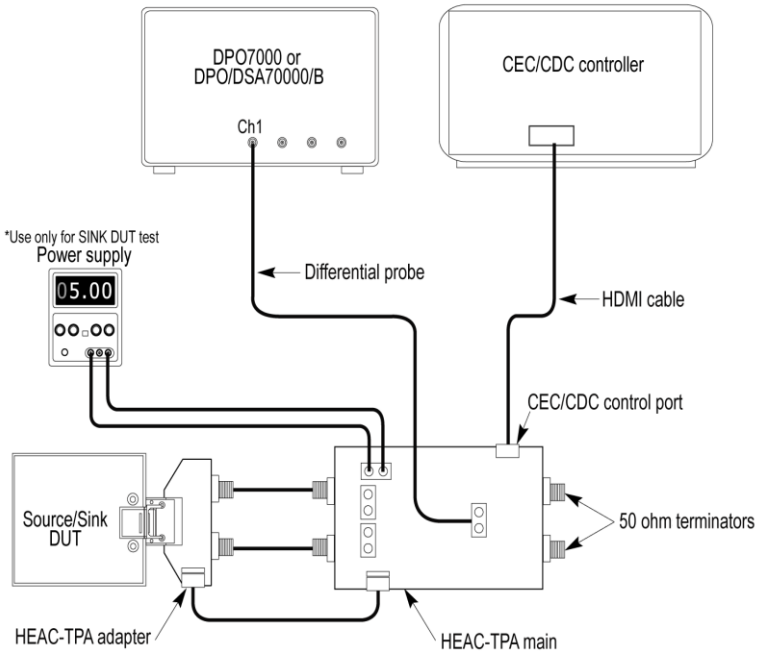
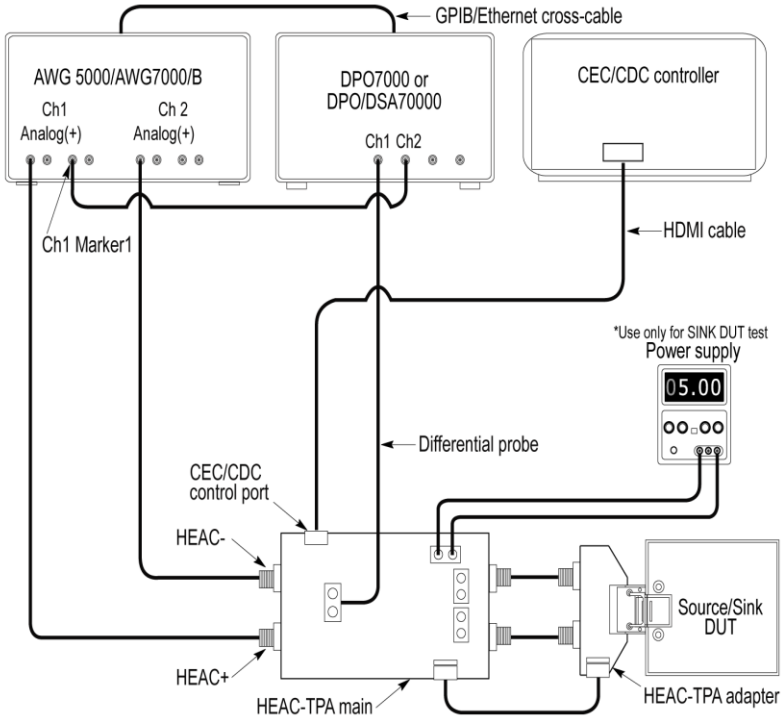
# HDMI 1.4 HEAC Solution Configuration




**Tx Test Setup**




**Rx Test Setup**



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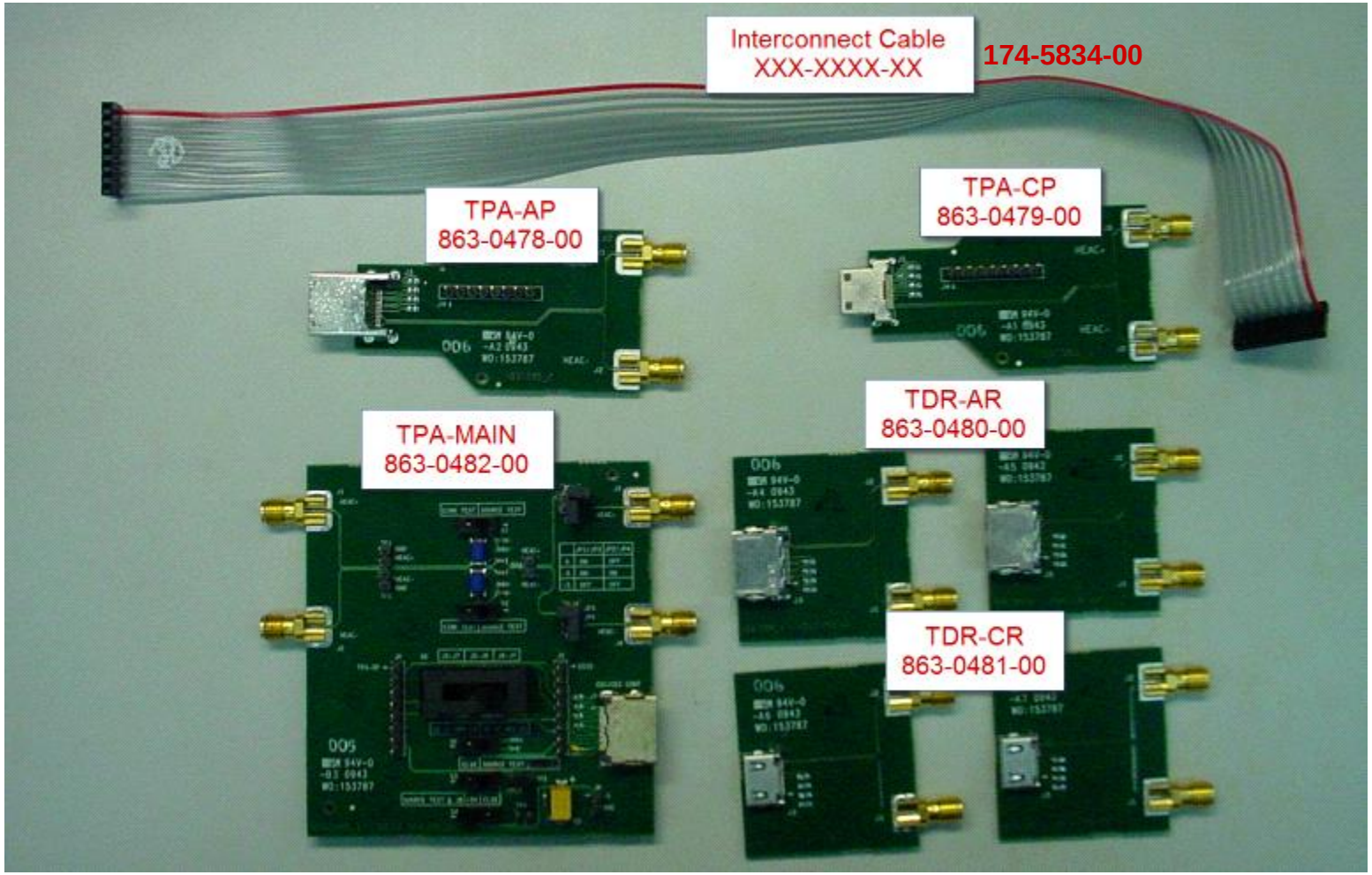
# Tektronix HDMI 1.4a Test Solutions
# HEAC Fixtures

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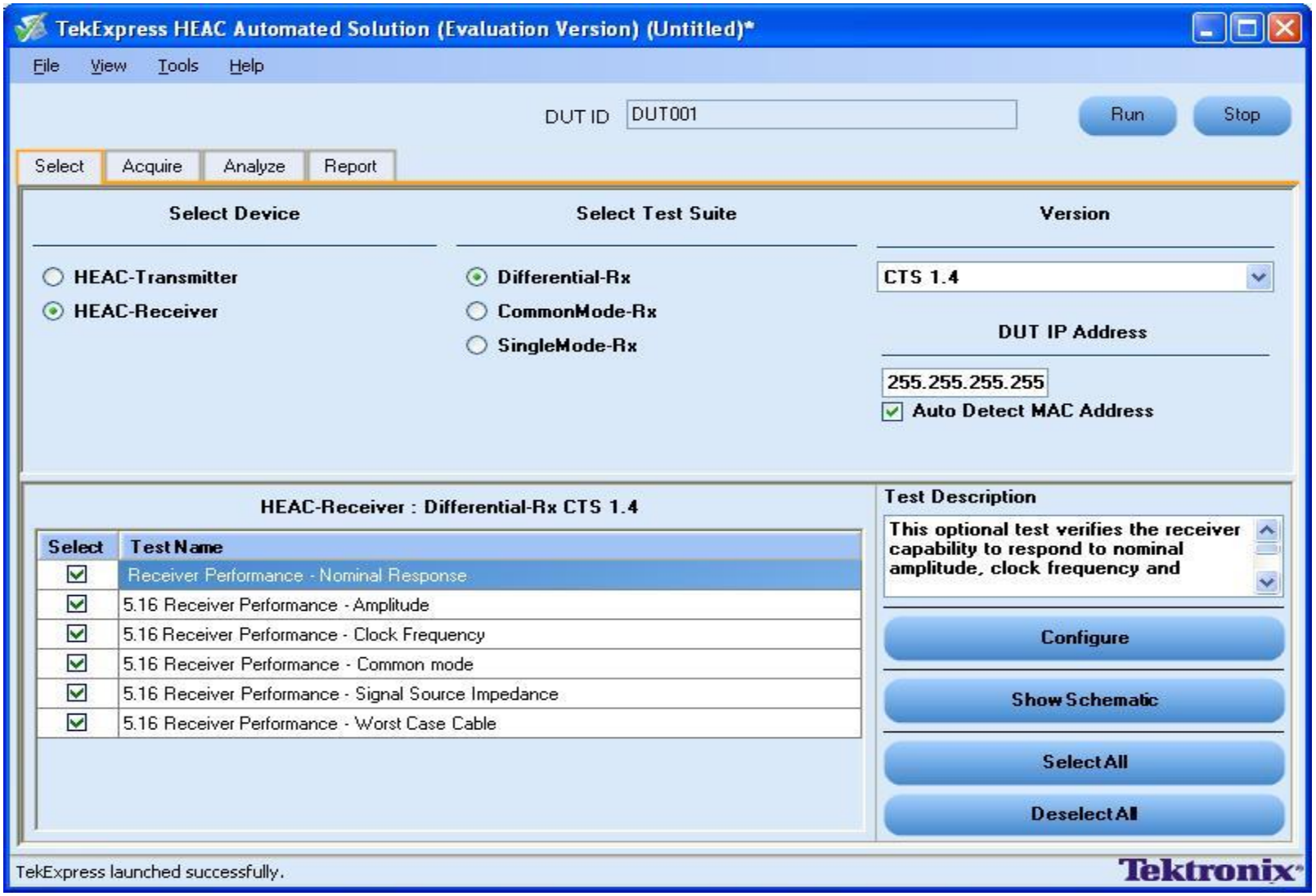
# HEAC Software



# Proposed HDMI 2.0 features-Not finalized

- Uses same Cat 2 Cable and HDMI 1.4b connector
- Support 4K 2K 4:4:4 60 Hz – 594Mhz
- Support 4K 2K 4:2:0 – 297Mhz
- Direct Attach device support
- Low level Bit error rate testing
- Scrambling is likely to be introduced for rates >340Mcps.

# Rise time Needs

*Table 4-24 Source AC Characteristics at TP1*

| Item | Value |
|---|---|
| Rise time / fall time (20%-80%) | if attached Sink supports < 340MHz<br>75psec ≤ Rise time / fall time<br>if attached Sink supports ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz<br>42.5psec ≤ Data Rise time / Data fall time<br>75psec ≤ Clock Rise time / Clock fall time |

*Table 4-30 TP7 Direct Attach AC Characteristics at 6Gbps*

| Item | Value |
|---|---|
| Rise time / fall time (20%-80%) | if attached Sink supports ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz<br>42.5psec ≤ Data Rise time / Data fall time<br>75psec ≤ Clock Rise time / Clock fall time |

- HDMI 1.4b, should be capable of measuring 75 psec, but no word about the System Rise time.
- **HDMI 2.0 should be capable of measuring 42.5 psec, but no word about System Rise time**.

- The Error contribution of RT measurement due to System and DUT generally not accounted when we refer to specification

# What is the system bandwidth needed to measure 42.5 (20-80% )psec or less DUT Rise time

- System bandwidth should be around (42.5/1.5 ) 28psec
- Scope bandwidth of 16 Ghz and 16 Ghz DSP enhanced probe has System Rise time of about 23 psec. It can measure the DUT Rise time of 42.5 psec with error of 1%. And can measure DUT Rise time of 37 psec with error of 7%.
- We can indicate Pass or fail confidently only when the System band. width is close to 16 Ghz scope .
- Is it fact for all scope vender ??
  - Spec says it should not be less than 42.5psec.
  - Max Rise time is limited by Eye diagram slope.
  - Both scope and Probe rise time cannot be less or equal to the DUT rise time because it can measure the signal rise time accurately only if DUT RT is slower than system rise time by 1.5 X times.
- How it is handled in HDMI 1.4b today???
  - We recommend 8Ghz scope and 13 Ghz probe, then system rise time is 38 psec which is close 2X faster than 75 psec

# Conclusion

- 16GHz BW scope will give 1% error and hence is recommended for HDMI 2.0 testing.

- HDMI 2.0 RT/FT (20%-80%) data signals is 42.5ps

# HDMI 2.0 Source Testing-Advanced information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# Source Testing 1.4b Vs 2.0

Eye Diagram test is changed

Rest of the tests is same

1.4b CTS test is a pre-requsite for HDMI 2.0

Min 8GHz scope to 16GHz scope

Fixtures and Probes

# Likely Source Electrical tests

**Test ID HF1-1: Source TMDS Electrical – 340-600Mcsc – $V_L$**

**Test ID HF1-2: Source TMDS Electrical – 340-600Mcsc – $T_{RISE}$, $T_{FALL}$**

**Test ID HF1-3: Source TMDS Electrical – 340-600Mcsc – Inter-Pair Skew**

**Test ID HF1-4: Source TMDS Electrical – 340-600Mcsc – Intra-Pair Skew**

**Test ID HF1-5: Source TMDS Electrical – 340-600Mcsc – Differential Voltage**

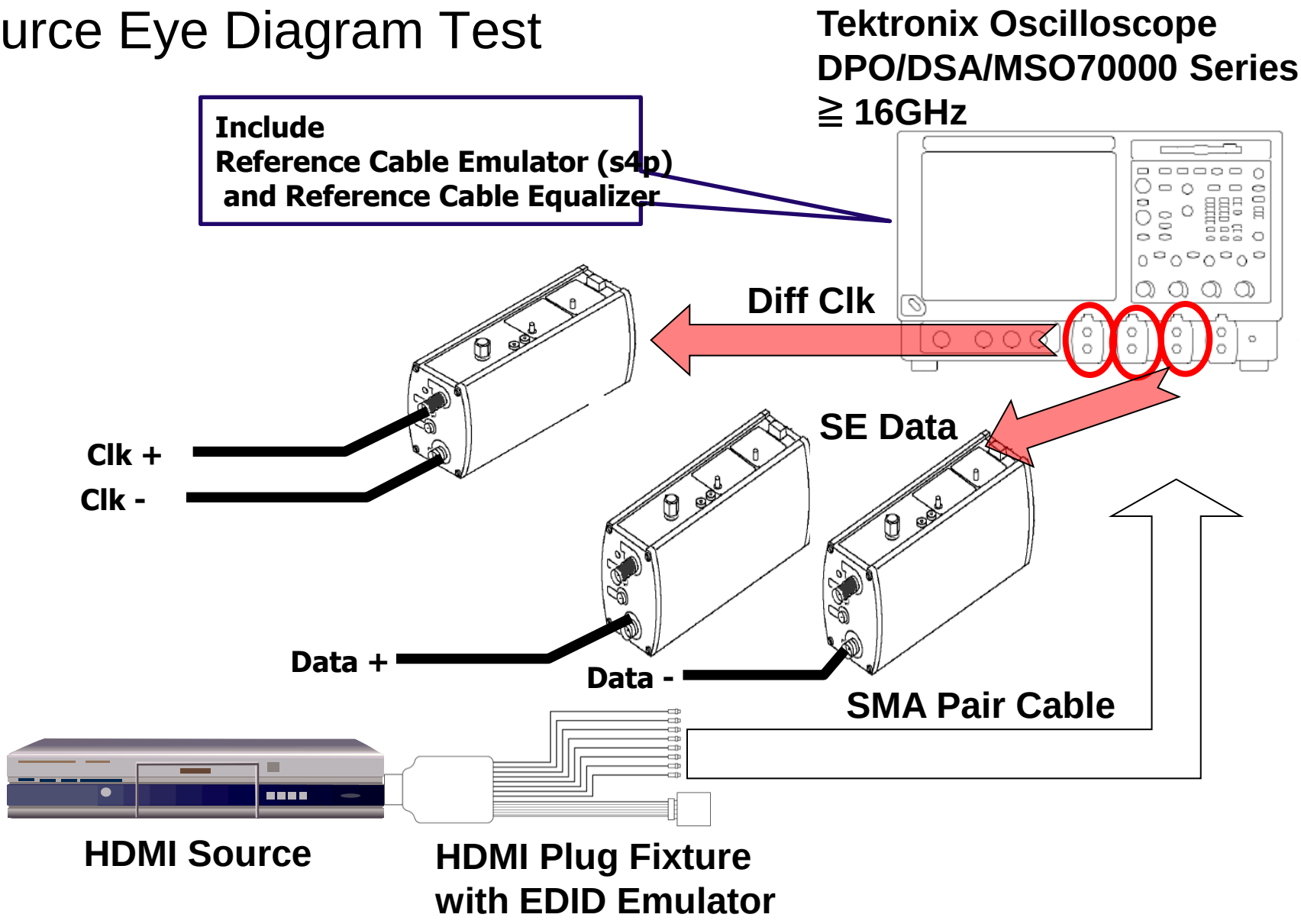
**Test ID HF1-6: Source TMDS Electrical – 340-600Mcsc – Clock Duty Cycle**

**Test ID HF1-7: Source TMDS Electrical – 340-600Mcsc – Clock Jitter**

**Test ID HF1-8: Source TMDS Electrical – 340-600Mcsc – Data Eye Diagram**

**Test ID HF1-9: Source TMDS Electrical – 340-600Mcsc – Differential Impedance**

# Source Eye Diagram Test



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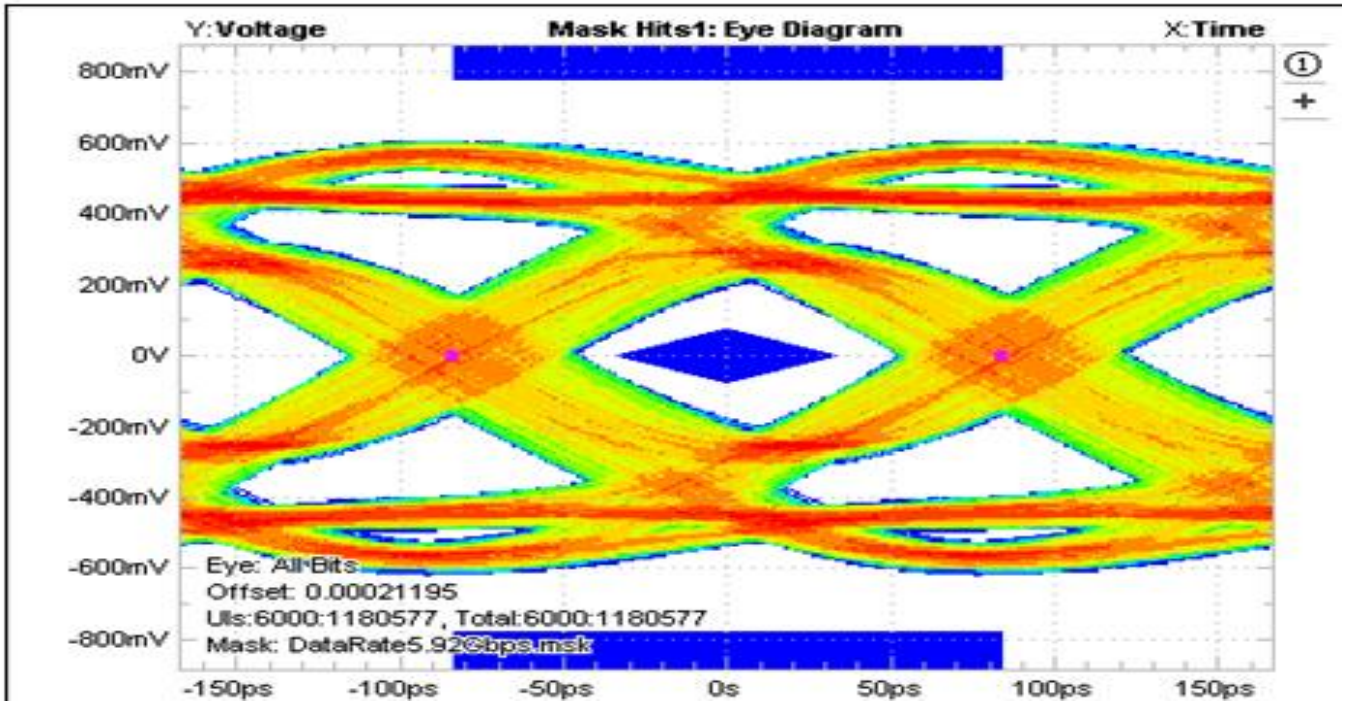
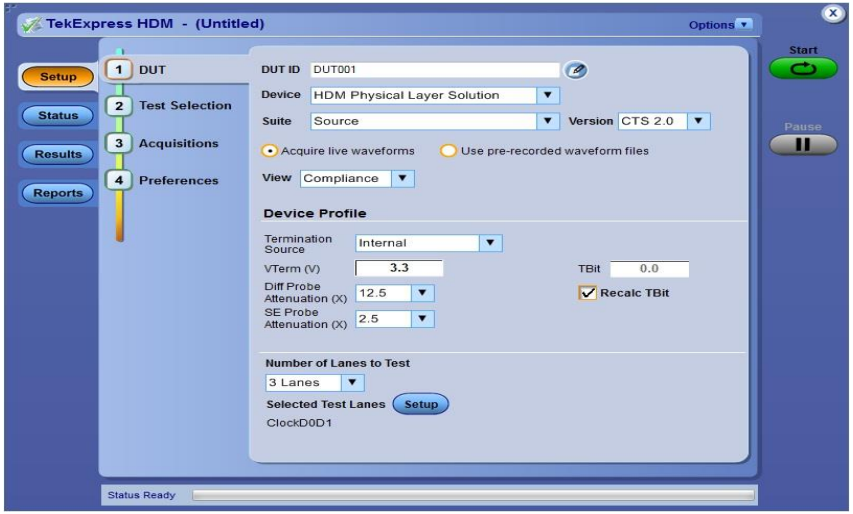
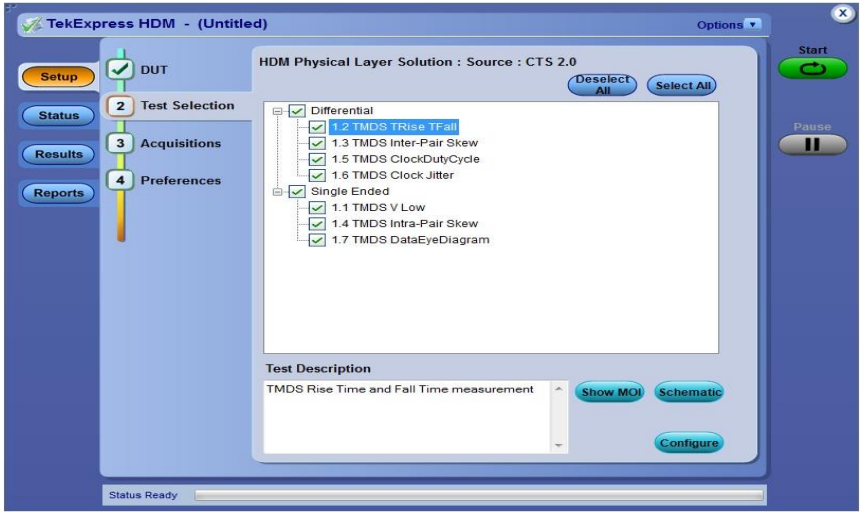
# TP2 Source Eye for HDMI 2.0 6G signal

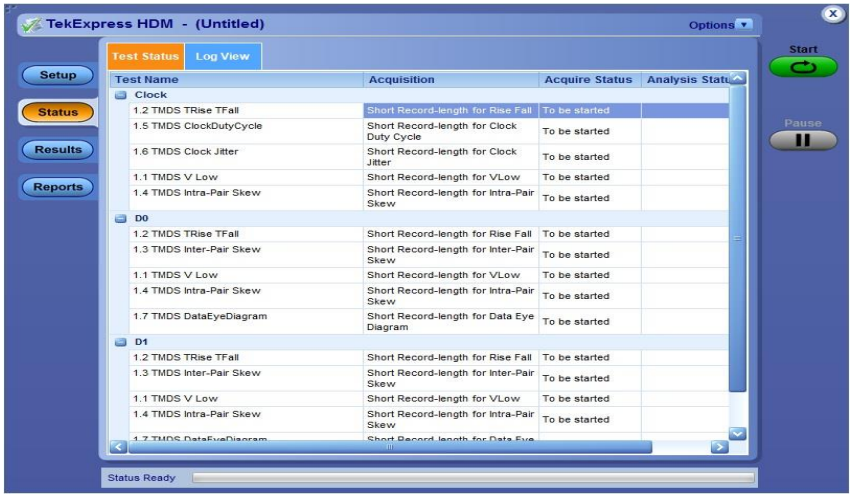


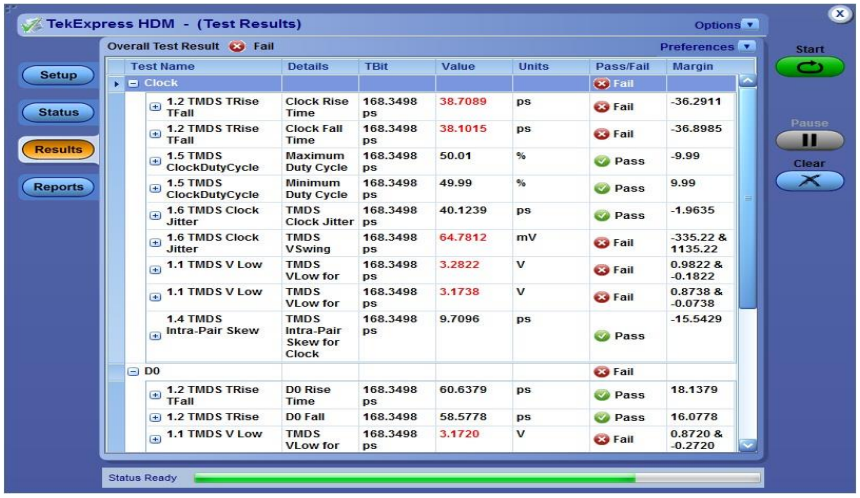

**Single End Input eye rendered at Tek lab**

# HDMI 2.0 Tx Compliance Software

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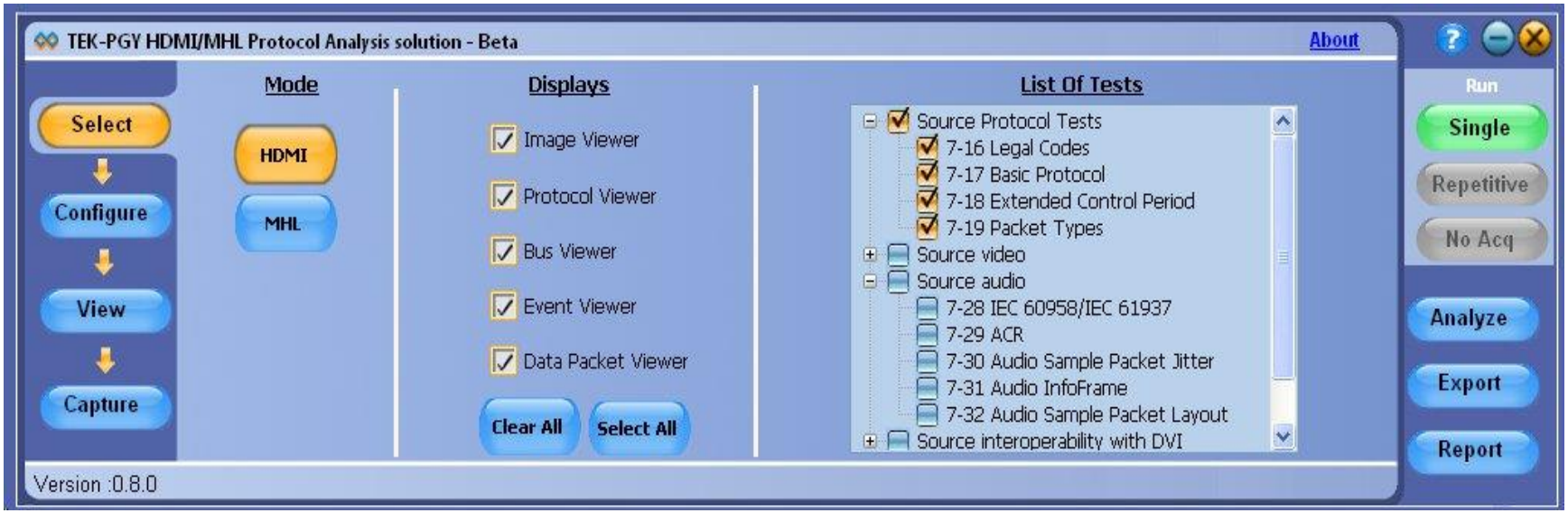
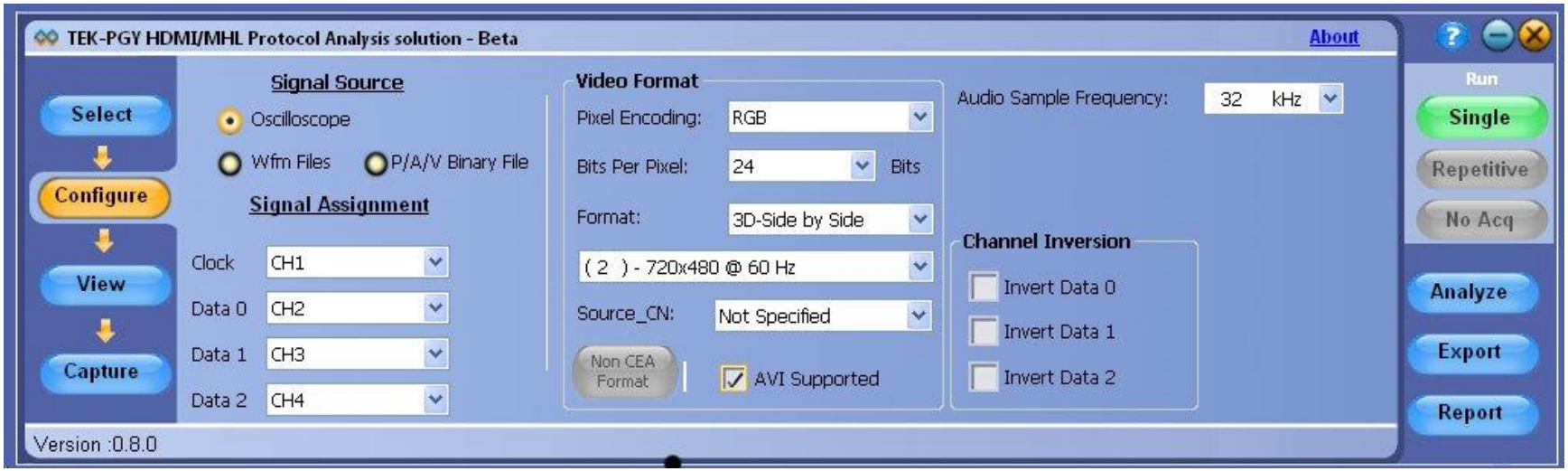
# Tektronix HDMI Protocol Analyzer

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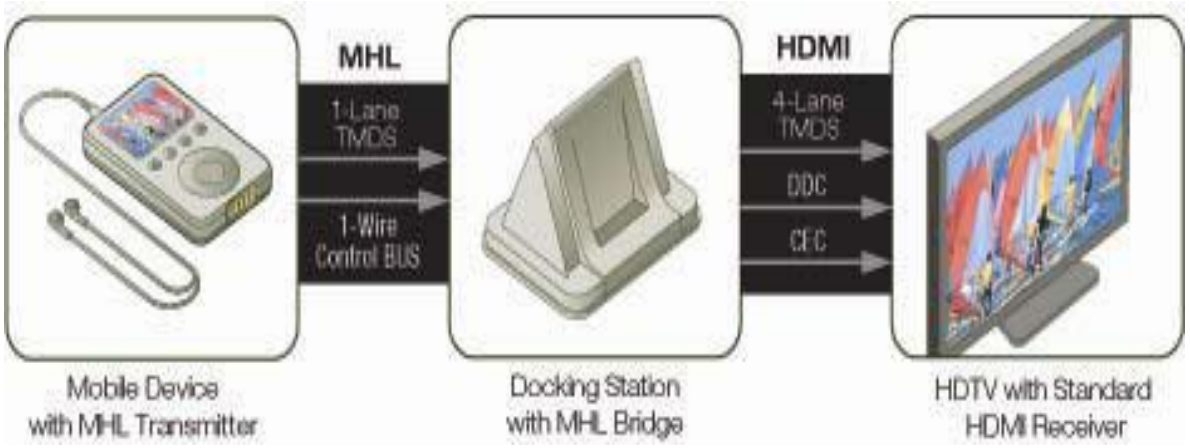
# MHL Introduction




**Source: MHL.org**

- **Mobile HD Link (MHL) technology is a low pin count HD audio and video interface that connects portable electronics devices such as mobile phones, digital cameras, camcorders and portable media players, to HDTVs.**
- **The technology allows mobile devices to output digital 1080 Full HD resolution via the existing mobile connector without the real estate and cost of another dedicated video connector.**
- **Together with an MHL-to-HDMI bridge, the MHL-enabled mobile device becomes a fully compliant HDMI source and can connect to the television's standard HDMI input port.**



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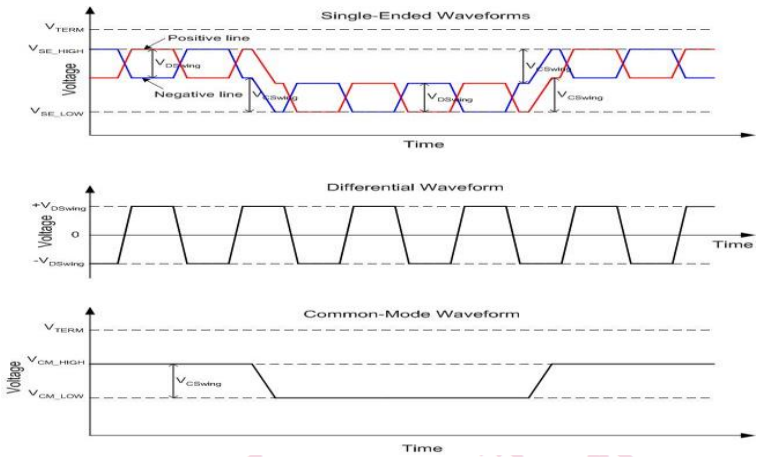
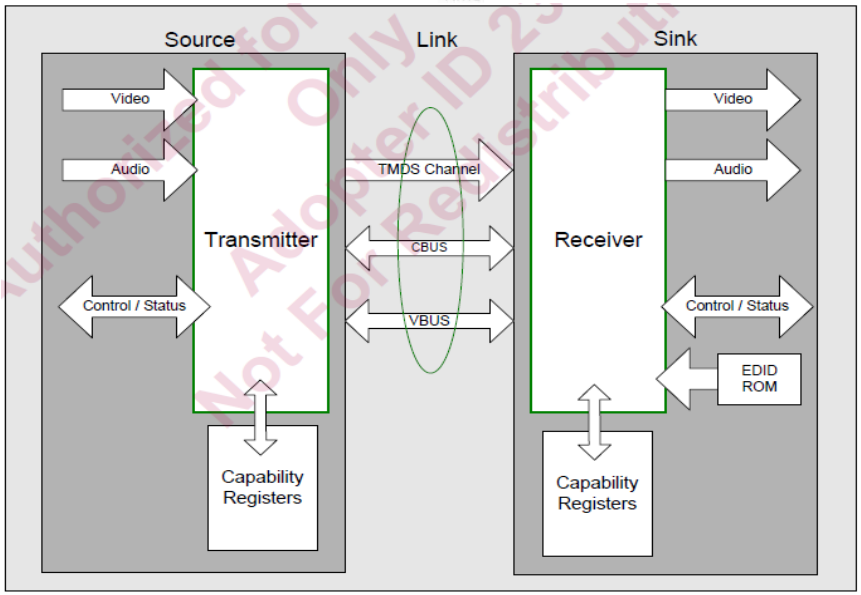
# MHL Introduction

- **MHL Consortium was formed in Sept 2009 with the following founding members:**
  - **NOKIA**
  - **SAMSUNG**
  - **Silicon Image**
  - **Sony**
  - **Toshiba**
- **The Specification 1.1 version was announced in Q12011 , Specification 1.2 in Dec 2011, Specification 2.0 in Feb 2012 and Specification 2.1 NOW.**

  **The Consortium released CTS 1.1 version in June 2011, CTS 1.2 in Jan 2012, CTS 2.0 in Sept 2012 and CTS 2.1 is just announced.**

  **COMPLETE TEKTRONIX SOLUTION APPROVED in CTS1.1 , CTS 1.2 , CTS 2.0 and CTS 2.1 solution**
- **Tektronix is a Contributor adopter and actively involved in defining the CTS 2.1.**




**Source: MHL 1.2 specification document**





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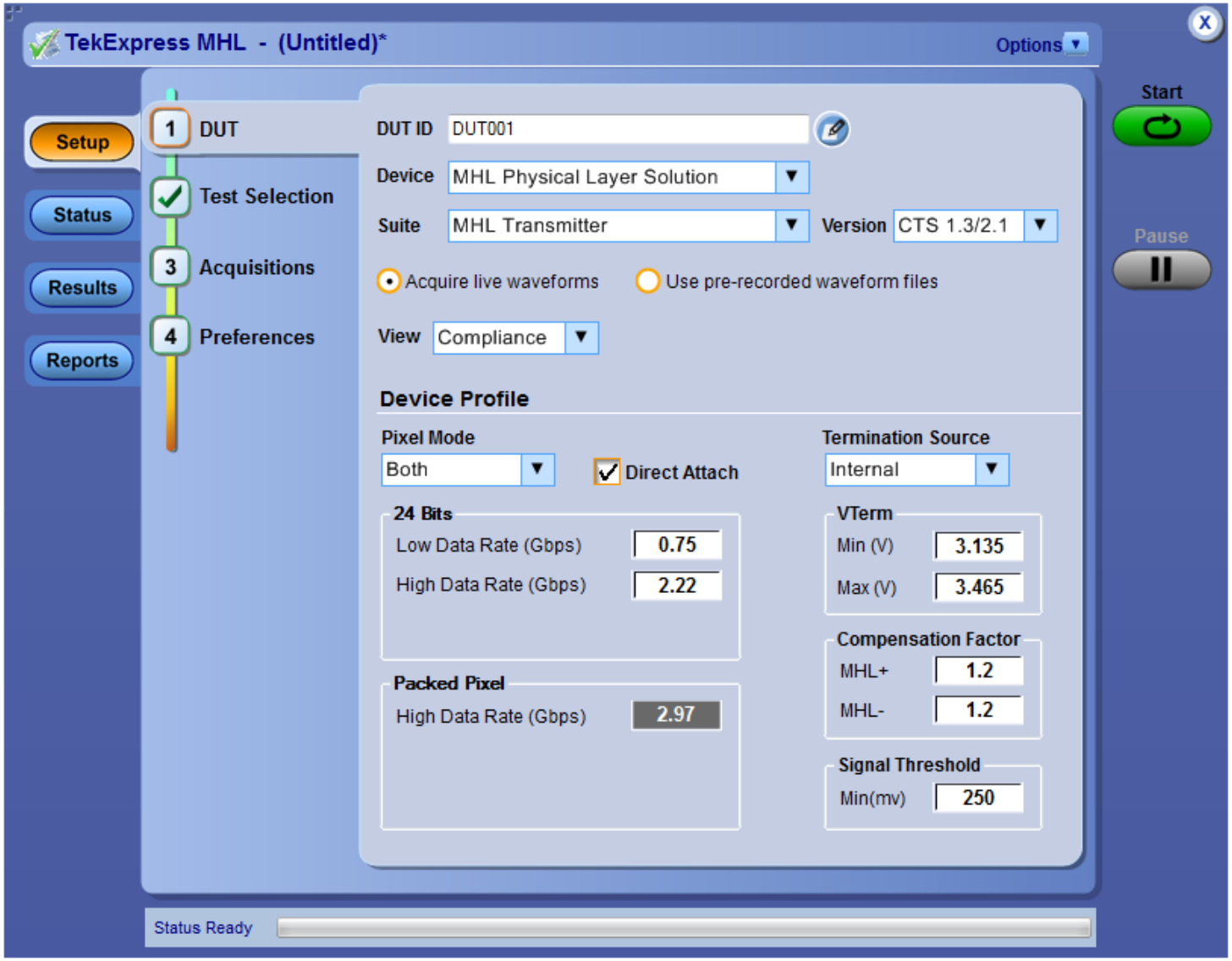
# Tektronix MHL 2.1 Tx Solution with Direct Attach test support



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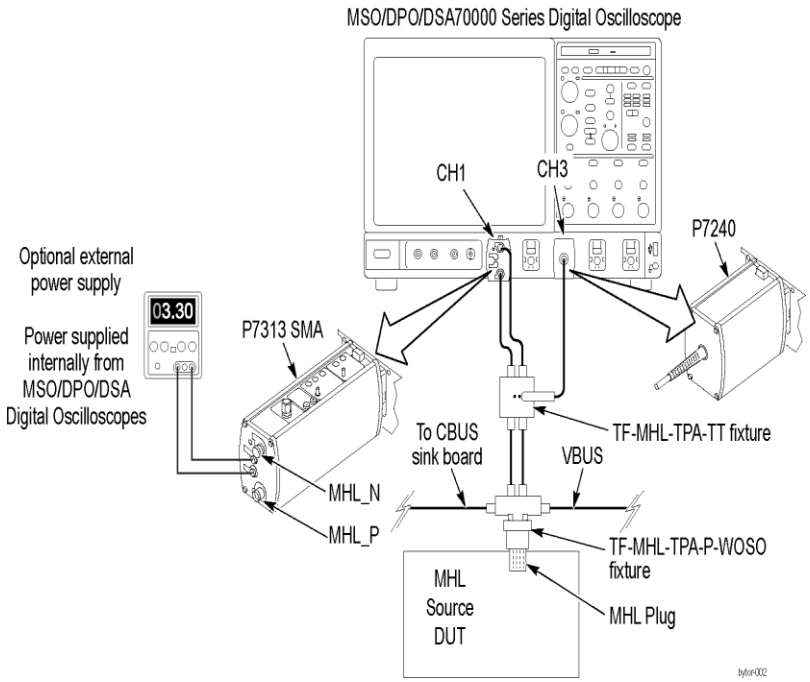
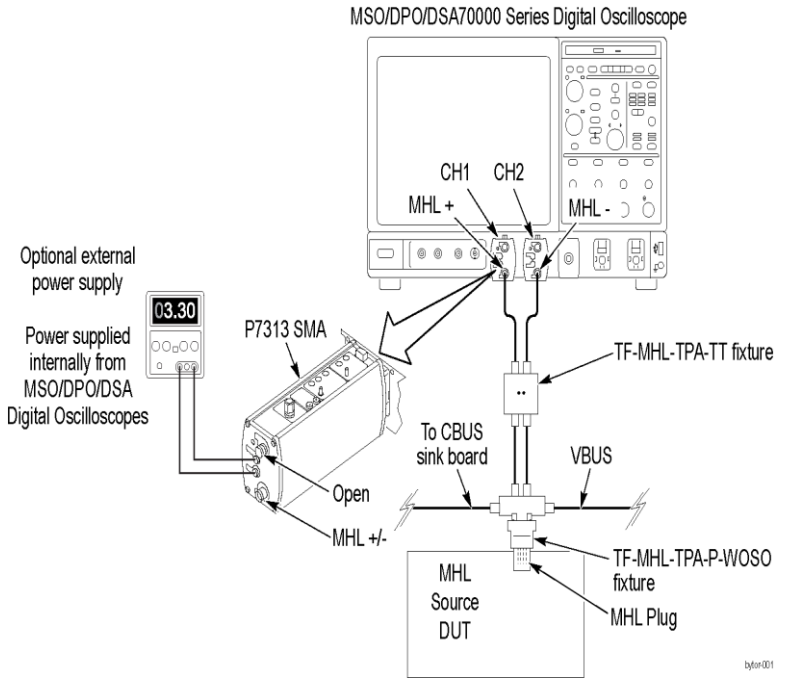
# Tektronix MHL Tx Setup




**MHL Differential and CM Test Setup**
**7 tests**




**Single Ended and Intra Pair Skew Test Setup**
**3Tests**

**Also same setup is used for MHL Protocol Testing**

**** C-Bus Sink and Source Board is needed for hand shaking and is available from Simplay Labs**



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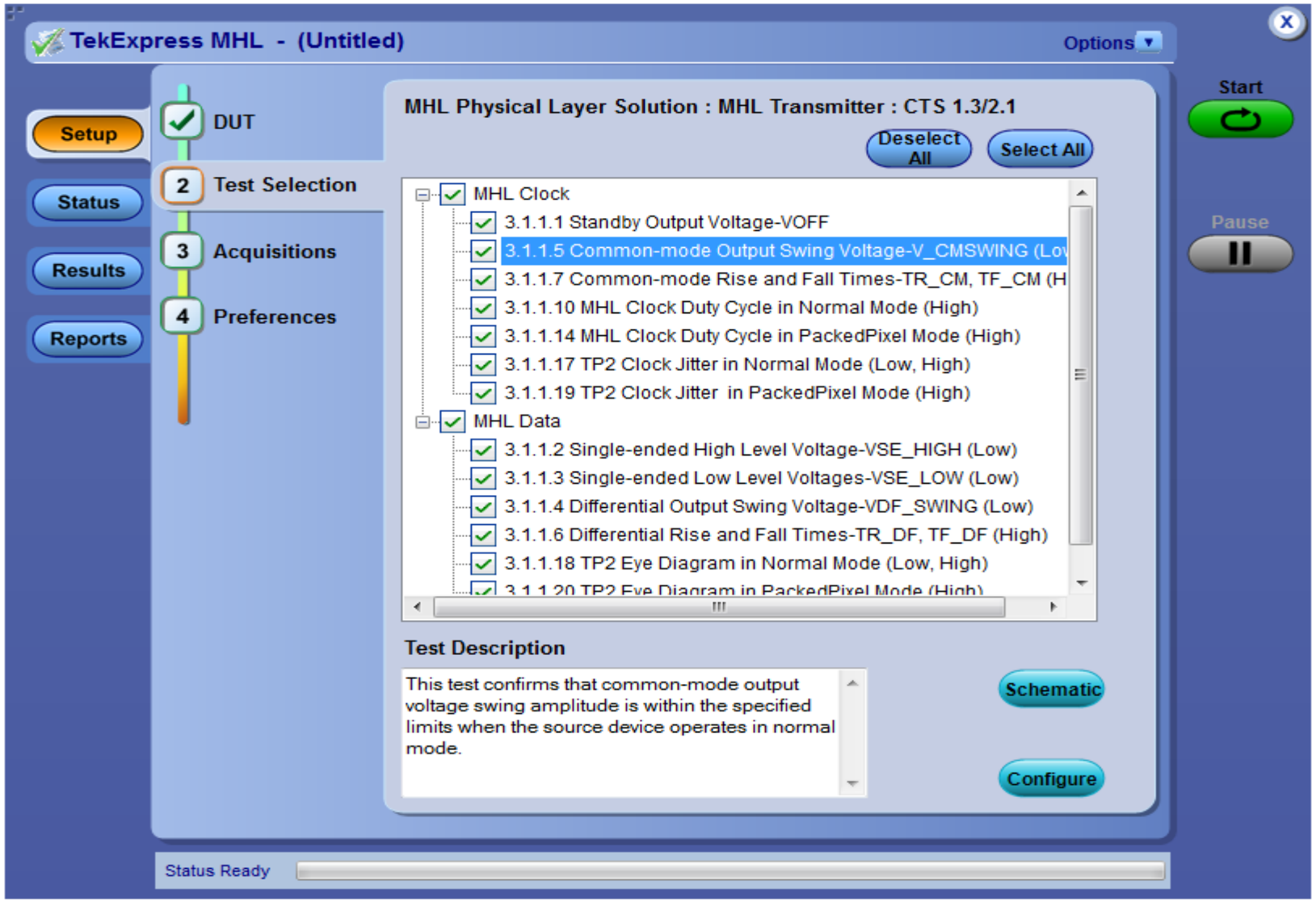
# MHL 2.1 Compliance Software for Automated Tx Tests: Option MHD



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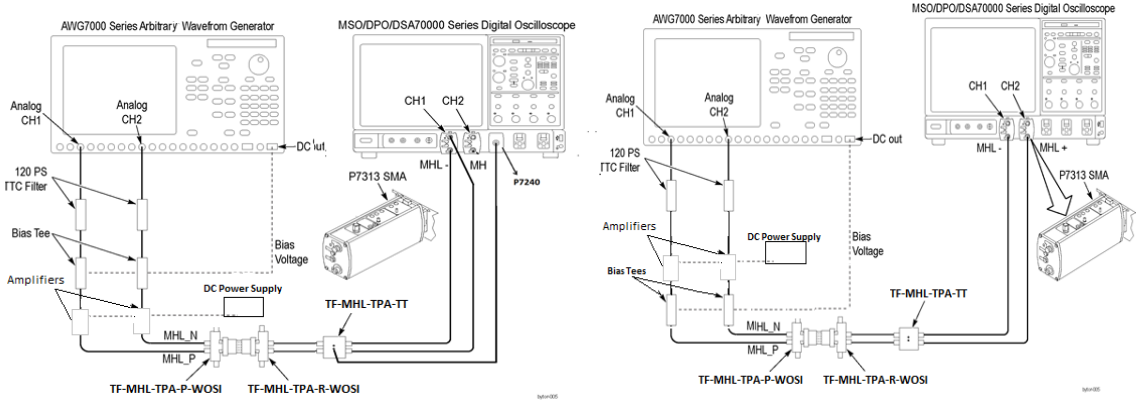
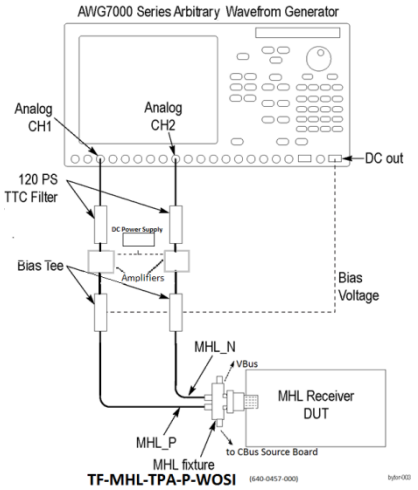
# Tektronix MHL Solution Setup: Simple and Easy Sink and Dongle Min/Max Testing -2

## Setup based on Direct Synthesis Capability of AWG7122C Series

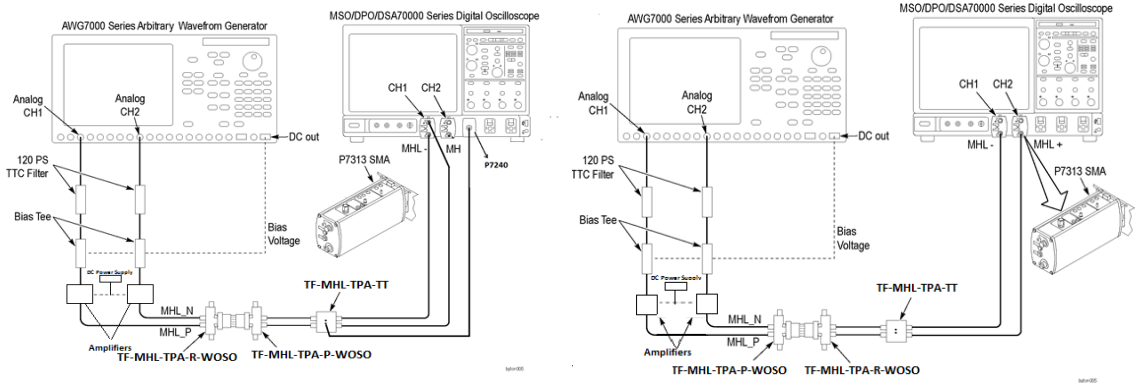
### AWG Sink Min/Max Signal ( CM,SE and Diff) Verification Using Real Time Oscilloscope



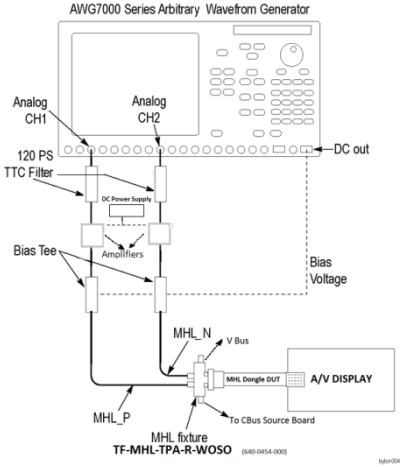

### Test Setup for Sink Min/Max Tests




### AWG Dongle Min/Max Signal ( CM,SE and Diff) Verification Using Real Time Oscilloscope




### Test Setup for Dongle Min/Max Tests



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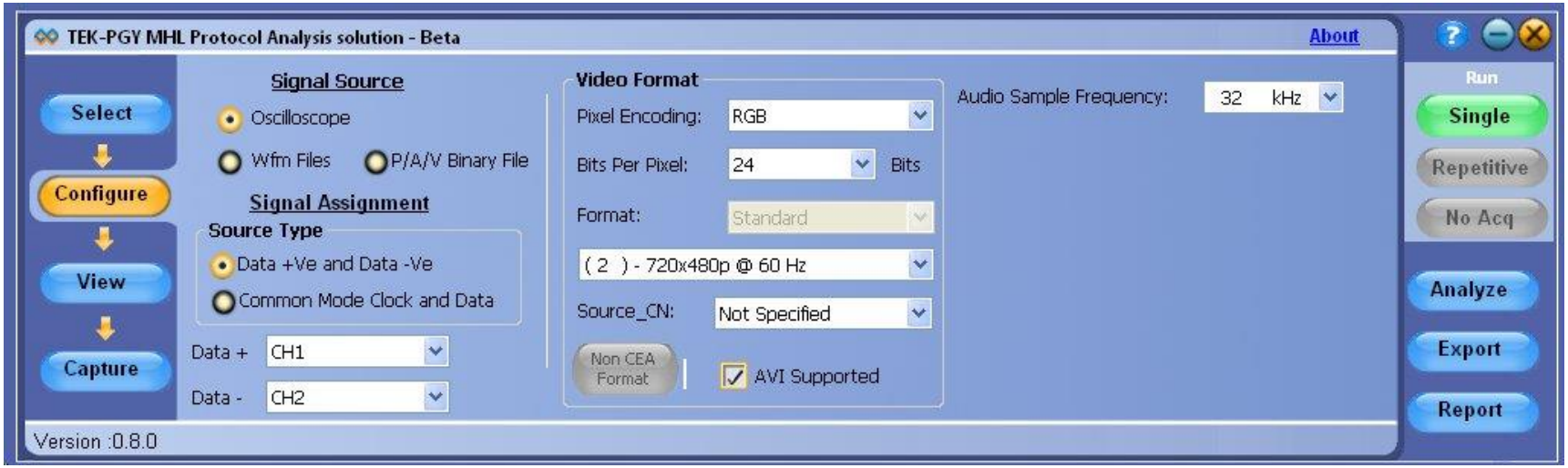
# Tektronix MHL Protocol Analyzer

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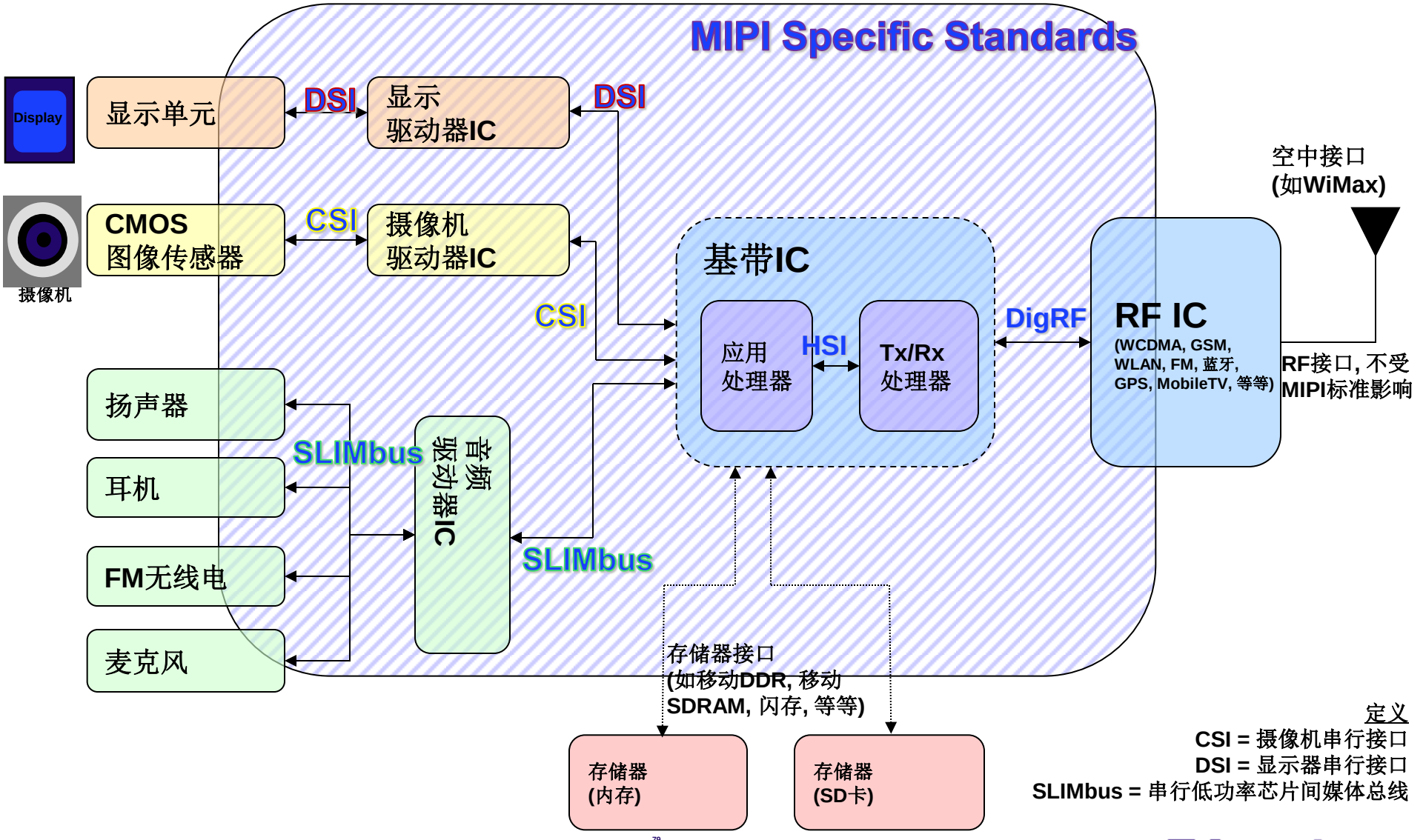
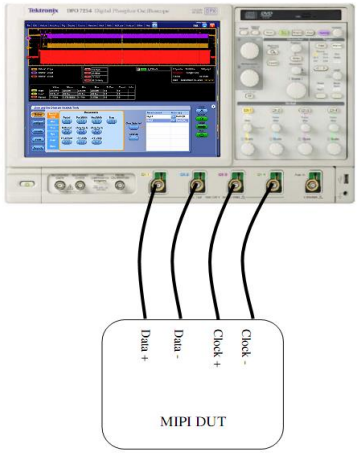
# MIPI标准概述

## 移动终端方框图实例



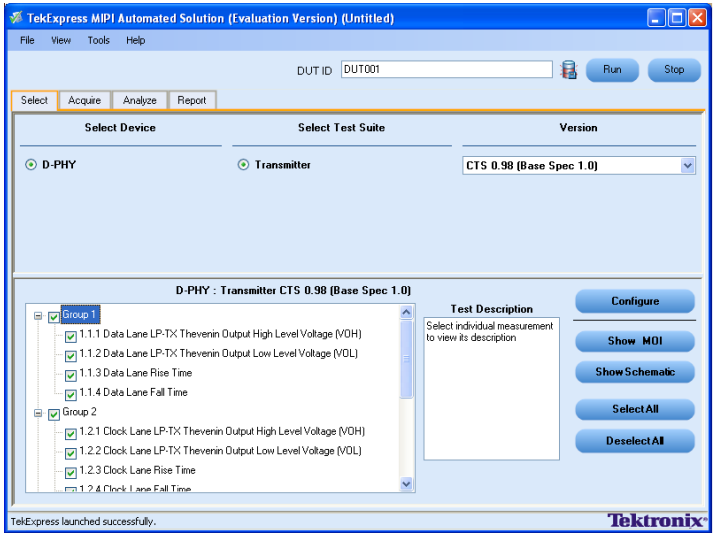
# D-PHY Tx测试解决方案 – 续

- 示波器
  - **推荐: DPO7354或DPO/DSA/MSO70404/B**
    - 用来测量规范+/-5%误差范围内的上升时间(150ps)
  - 如果不考虑上升时间的测试，可以使用DPO7254
- 探头
  - **探头考虑因素**
    - 同时测量单端性能和差分性能
    - 动态范围必须>1.2V
    - 探头衰减要达到最小
      - 1X最好, 2.5X或5X也行
  - **推荐:**
    - **DPO7000采用四只TAP3500；MSO/DPO/DSA70000/B采用四只P7240**
    - (Ch1: D+), (Ch2: D-), (Ch3: Clk+), (Ch4: Clk-)
    - TAP2500也适合低数据速率的DUT
  - **也可以使用:**
    - **焊接式探头**
      - **DPO7000采用TDP3500， 70000系列采用 P73xx**
      - (Ch1: D+, Gnd), (Ch2: D-, Gnd), (Ch3: Clk+ &Clk-)



# **New** Opt.D-PHYTX

- Opt.D-PHYTX : D-PHY Automated Solution
  - TekExpress option for  Fully-Automated testing
  - Automation similar to Opt.USB-TX
  - Provides Conformance and Characterization Testing
  - Based on D-PHY Base Spec v1.0 and UNH's Conformance Test Suite v0.98.
  - Runs on DPO7000, DPO/DSA/MSO70000/B Series oscilloscopes
- Opt.TEKEXP is Pre-Requisite
- Differentiation
  - Un-parallel Automation (Auto-Cursors/ Regions)
  - For Conformance testing to Latest CTS (v0.98)
  - Based on Latest Base spec (v1.0)
- Value proposition
  - Custom-limits/ Limits-Editing on the fly
  - Test Reports
    - Zoom-in waveform captures at the Cursors/ Regions
    - Pass/Fail Summary with Margin details
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
    - i.e. unlike Agilent 4G scope at entry-level



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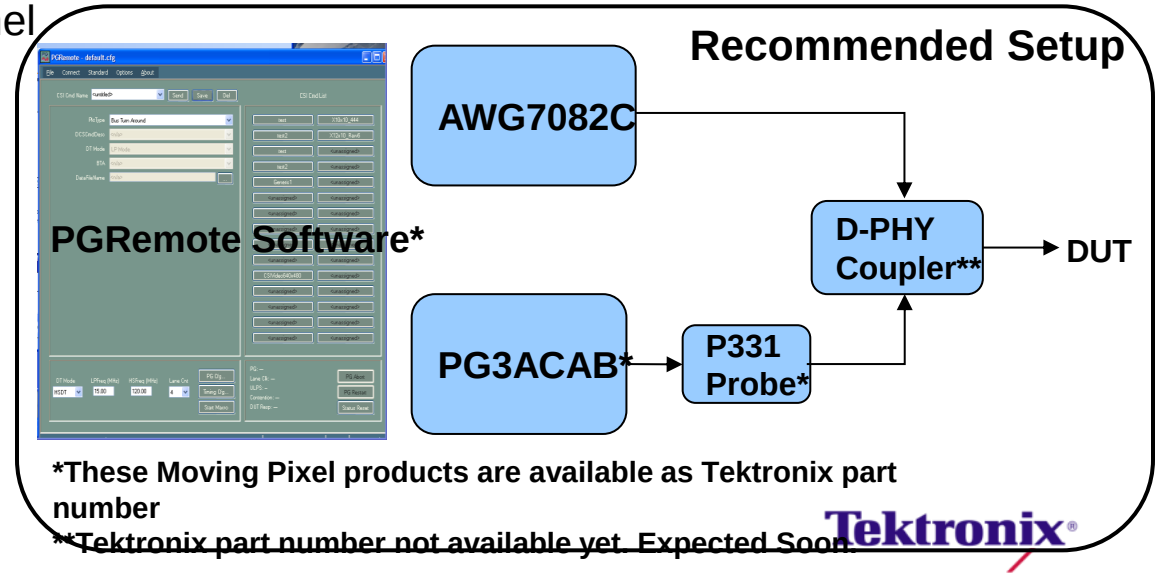
# D-PHY Rx : Test Solution Overview

## Simple, Quick, Easy and Re-usable

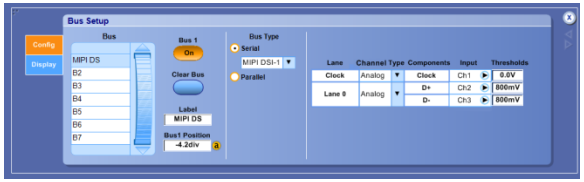
- 100% Coverage to Rx CTS
  - Meets all the requirements in UNH-IOL CTS document (v0.98)
- Quick and Easy setup
  - No complex VXI system, just stand alone instruments, and a probe.
- Cost effective solution
  - 70% Lower list price vs Competition
- Re-usable for Protocol tests
  - PG3A is the Only 4 channel solution for CSI &DSI test
- PG3A Pattern Generator
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver
- AWG7082C Generator
  - Adds jitter and interference to the D-PHY signals



# D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode

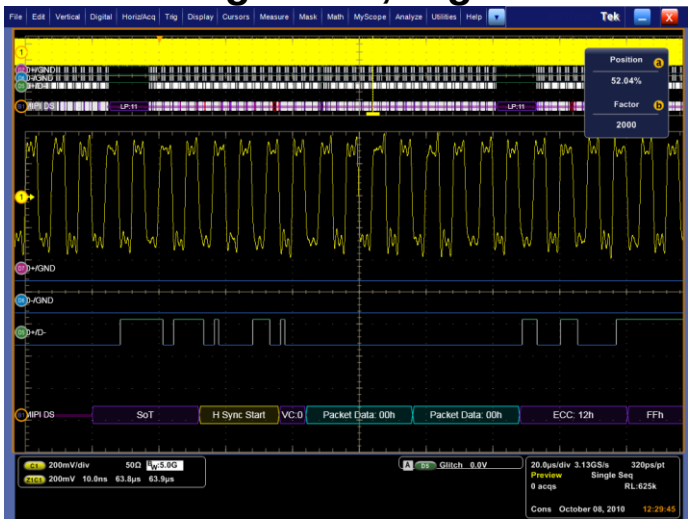
## Simultaneous Acquisition

- Probe using Analog, Digital or Mixed Channels
- Simultaneous probing of DSI &CSI using MSO channels
- Working on multi-lane support, using high performance MSO digital channels
- Supported on all 7KC, 70KC and MSO70K scopes. (**Win7-OS only**)
  - Option key bit #25
- Software installed as part of TekScope firmware v6.1.2.4 or later.
  - Browse to TekScope Menu --> Vertical --> Bus Setup --> Select Bus Type as Serial-- > Select MIPI DSI or CSI from the drop down list.




**Probe using Mixed Channels**

**Analog Clock, Digital Data**





**Digital Clock, Analog Data**

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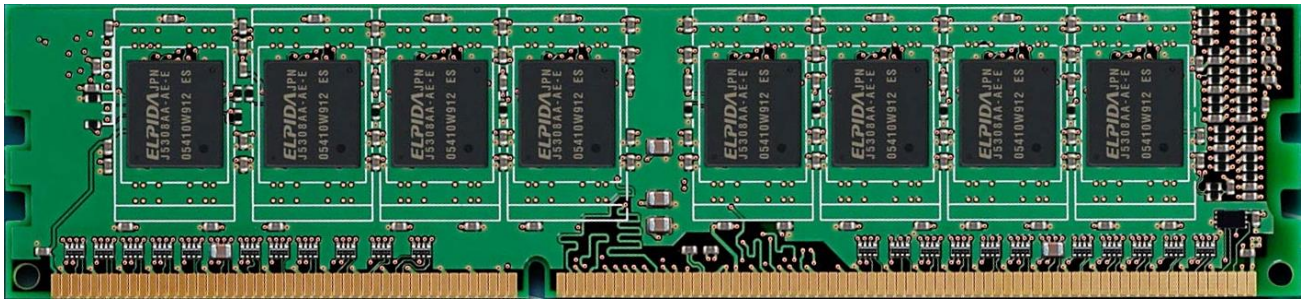
# Memory Technology – Quick Overview

- DRAM - dominant memory technology
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMMs
  - Embedded systems
    - Cell phones, printers, cars
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR3 now available at 1600 (1.6Gb/s) data rates
    - DDR3 2000 emerging soon (overclocked)

- DRAM variants
  - LPDDR – Low Power DDR
    - Power savings for portable computing
  - GDDR – Graphic DDR
    - Optimized for Speed - faster access

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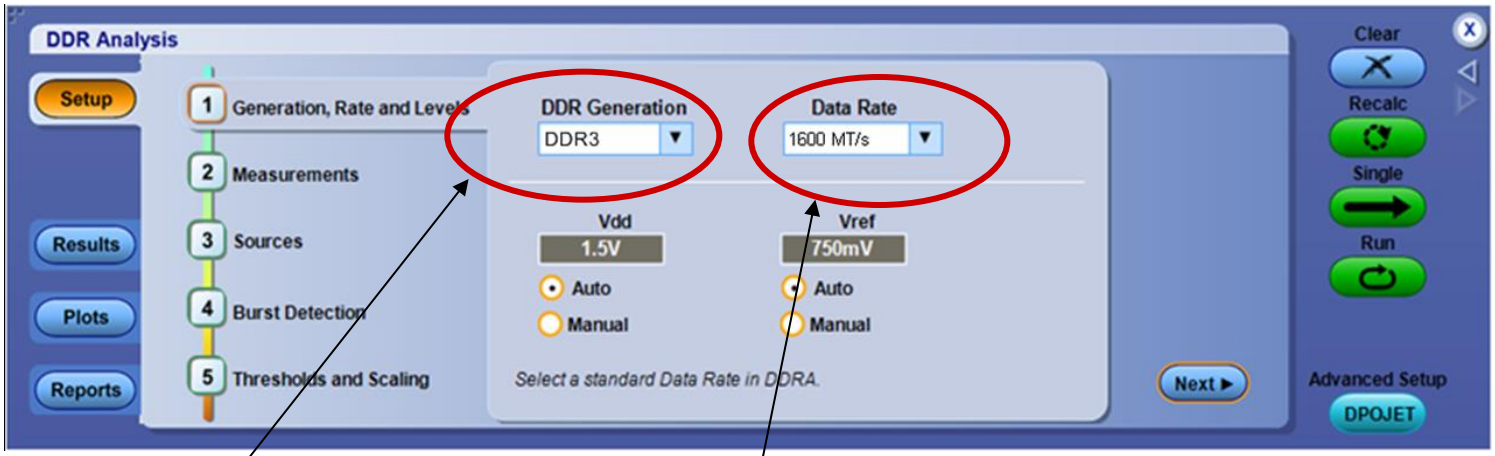
# Automated Test Setup

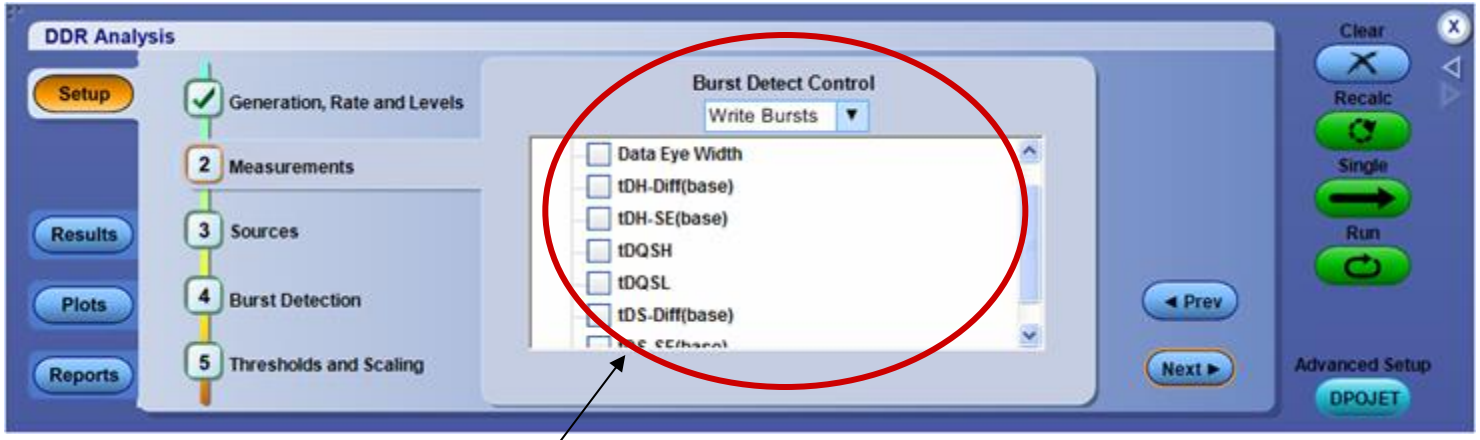
**Step #1**




Select DDR Generation

Select DDR Rate

**Step #2**




Choose measurements (Read / Write / CLK / Addr & Command)

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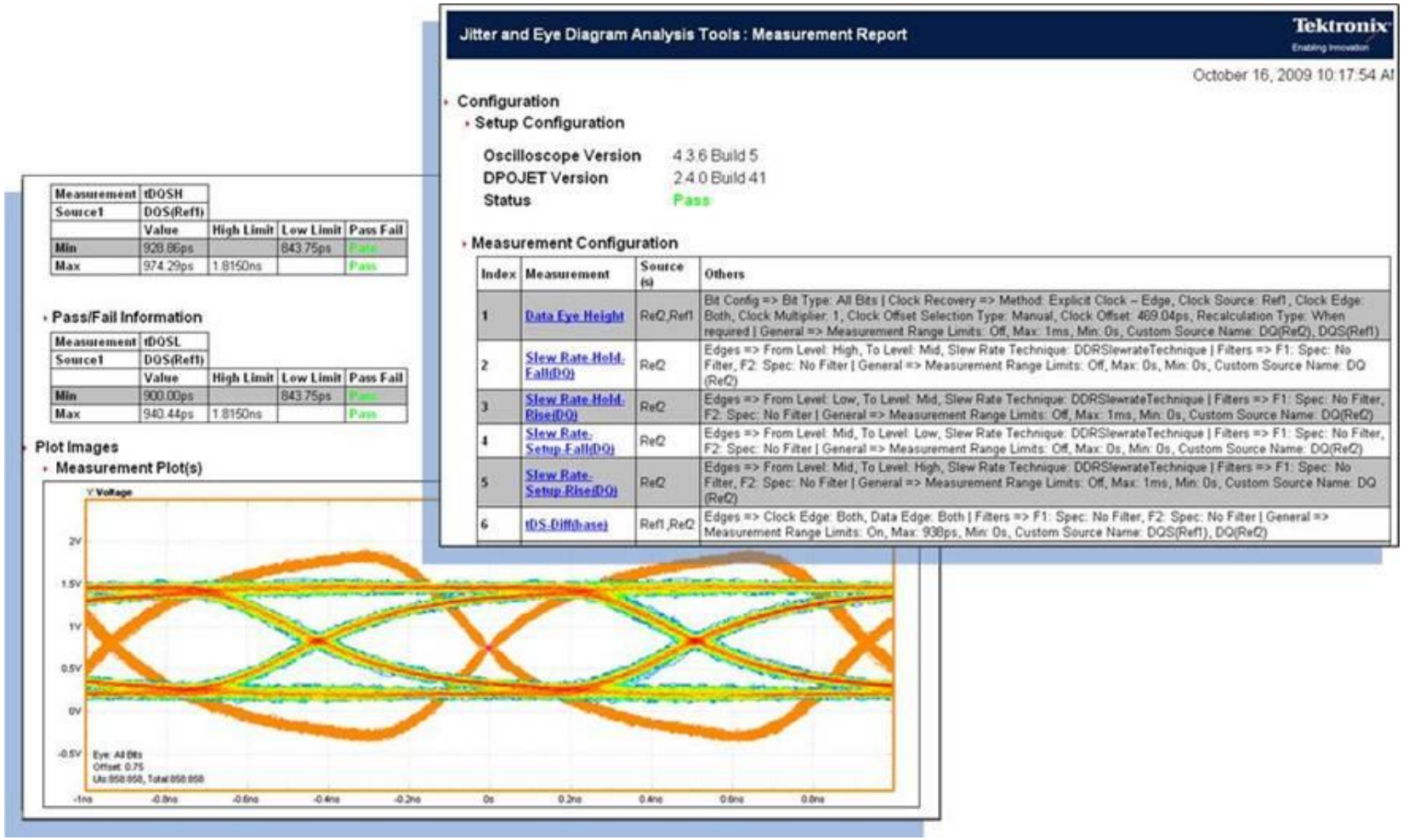
# Effective Reporting / Archiving



Jitter and Eye Diagram Analysis Tools : Measurement Report

Tektronix

October 16, 2009 10:17:54 AM

Configuration

Setup Configuration

| | |
|---|---|
| Oscilloscope Version | 4.3.6 Build 5 |
| DPOJET Version | 2.4.0 Build 41 |
| Status | Pass |

Measurement Configuration

| Index | Measurement | Source (s) | Others |
|---|---|---|---|
| 1 | Data Eye Height | ReQ,Ref1 | Bit Config => Bit Type: All Bits \| Clock Recovery => Method: Explicit Clock – Edge, Clock Source: Ref1, Clock Edge: Both, Clock Multiplier: 1, Clock Offset Selection Type: Manual, Clock Offset: 469.04ps, Recalculation Type: When required \| General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(ReQ), DQS(Ref1) |
| 2 | Slew Rate-Hold-Fall(DQ) | ReQ | Edges => From Level: High, To Level: Mid, Slew Rate Technique: DDRSlewrateTechnique \| Filters => F1: Spec: No Filter, F2: Spec: No Filter \| General => Measurement Range Limits: Off, Max: 0s, Min: 0s, Custom Source Name: DQ (ReQ) |
| 3 | Slew Rate-Hold-Rise(DQ) | ReQ | Edges => From Level: Low, To Level: Mid, Slew Rate Technique: DDRSlewrateTechnique \| Filters => F1: Spec: No Filter, F2: Spec: No Filter \| General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ(ReQ) |
| 4 | Slew Rate-Setup-Fall(DQ) | ReQ | Edges => From Level: Mid, To Level: Low, Slew Rate Technique: DDRSlewrateTechnique \| Filters => F1: Spec: No Filter, F2: Spec: No Filter \| General => Measurement Range Limits: Off, Max: 0s, Min: 0s, Custom Source Name: DQ(ReQ) |
| 5 | Slew Rate-Setup-Rise(DQ) | ReQ | Edges => From Level: Mid, To Level: High, Slew Rate Technique: DDRSlewrateTechnique \| Filters => F1: Spec: No Filter, F2: Spec: No Filter \| General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Source Name: DQ (ReQ) |
| 6 | tDS-Diff(base) | Ref1,ReQ | Edges => Clock Edge: Both, Data Edge: Both \| Filters => F1: Spec: No Filter, F2: Spec: No Filter \| General => Measurement Range Limits: On, Max: 938ps, Min: 0s, Custom Source Name: DQS(Ref1), DQ(ReQ) |

| Measurement | tDQSH | | | |
|---|---|---|---|---|
| Source1 | DQS(Ref1) | | | |
| | Value | High Limit | Low Limit | Pass Fail |
| Min | 928.86ps | | 843.75ps | Pass |
| Max | 974.29ps | 1.8150ns | | Pass |

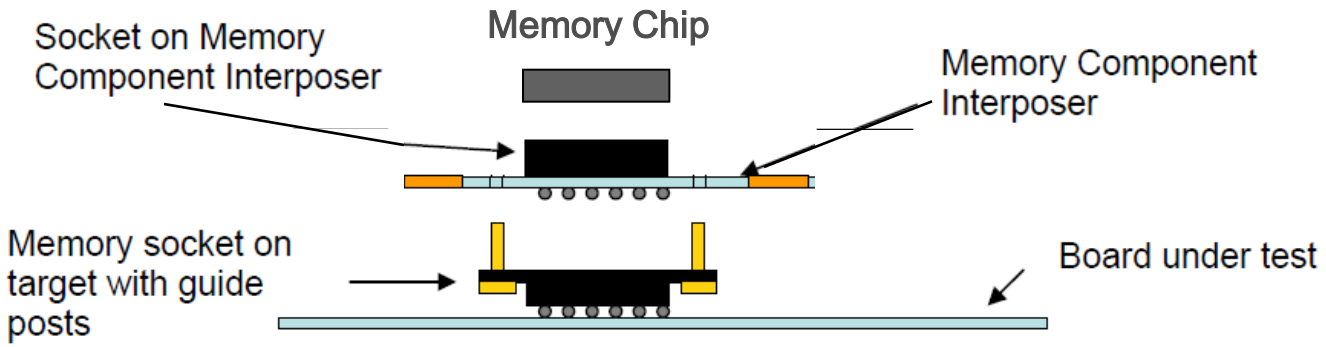
Pass/Fail Information

| Measurement | tDQSL | | | |
|---|---|---|---|---|
| Source1 | DQS(Ref1) | | | |
| | Value | High Limit | Low Limit | Pass Fail |
| Min | 900.00ps | | 843.75ps | Pass |
| Max | 940.44ps | 1.8150ns | | Pass |

Plot Images

Measurement Plot(s)

# Installation Process

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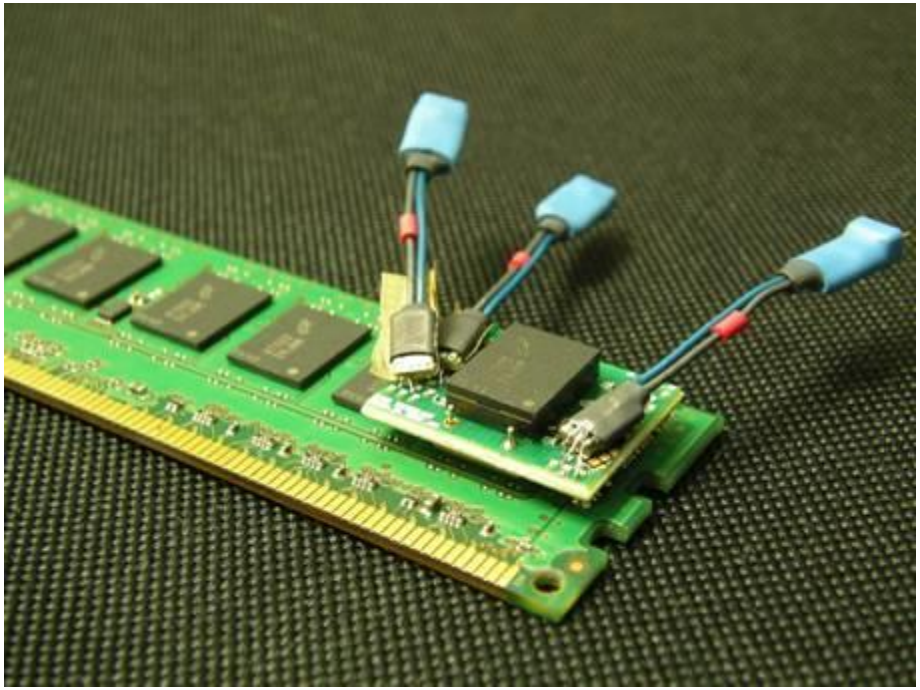
# BGA Chip Interposer for Oscilloscopes



- Available in socket and solder-in versions
  - Socket design allows for multiple chip exchanges
  - Solder-in best for single use
- Recommended probes: P7500 Series
  - P7504, P7506, P7508, P7513A
  - 020-3022-00 TriMode solder tips for Nexus Interposer

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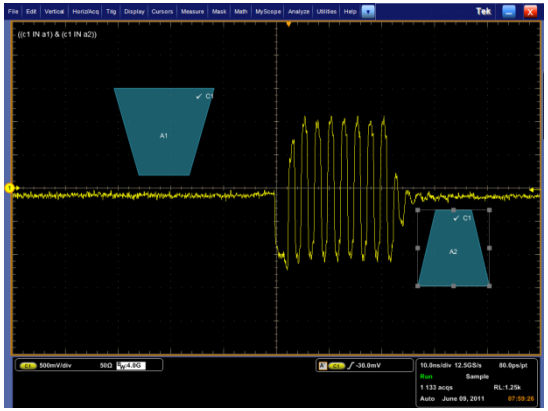
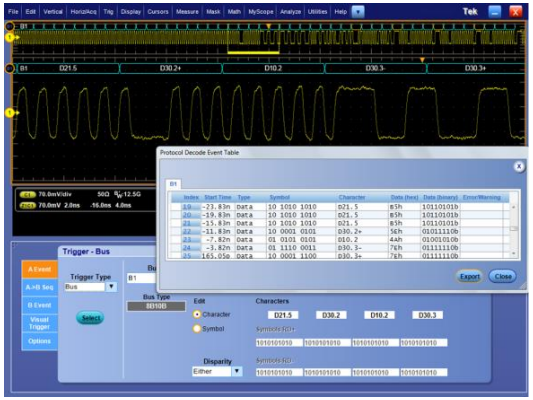
# Visual Trigger and Serial Decode

- Next generation designs have less margin and additional analysis must be done to pinpoint in on pattern dependent issues
  - **NEW!** Visual Trigger qualifies hard to define trigger events
    - 8 customizable shapes for capture of real signal behaviors

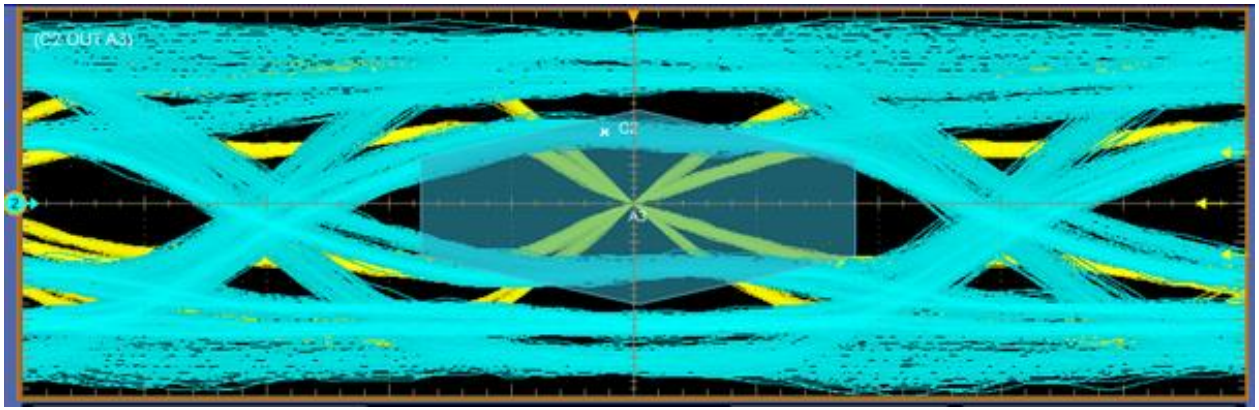


- Electrical and Logic layer are merging and requires simultaneous analog and protocol views
  - **NEW!** 8b/10b Serial Decode
    - Trigger or Search on decoded traffic
    - Compare to analog views to speed up time to answer



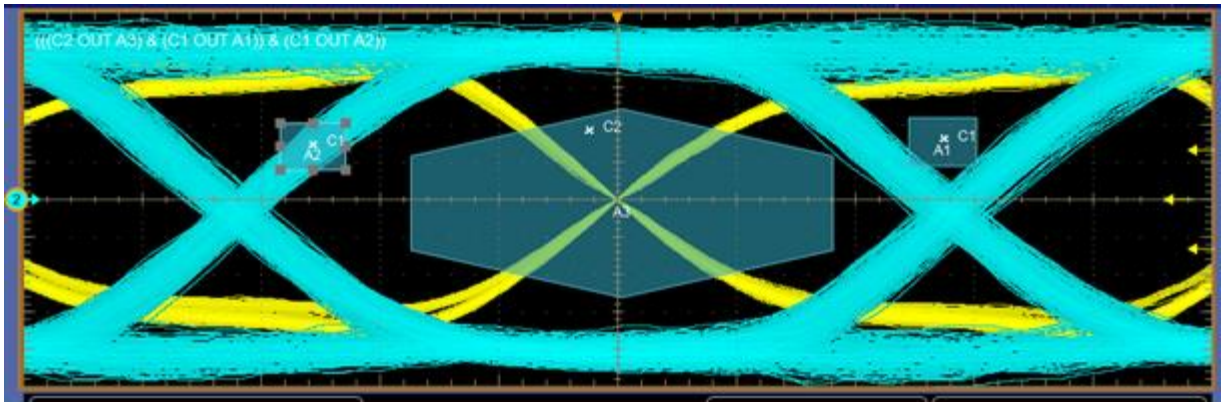
# Triggering Techniques for Debugging DRAM

- **Challenge: Dual-Rank System**
  - **Need to Isolate & Measure a Single Rank**
  - **Difficult to isolate data bursts from one rank only**



# Triggering Techniques for Debugging DRAM

- **'Visual' Trigger Used to Qualify One Rank**
  - **Visual area ("keep-out" region) used to exclude low-amplitude signals**
  - **Eliminates lower-amplitude data bursts from rank 2**

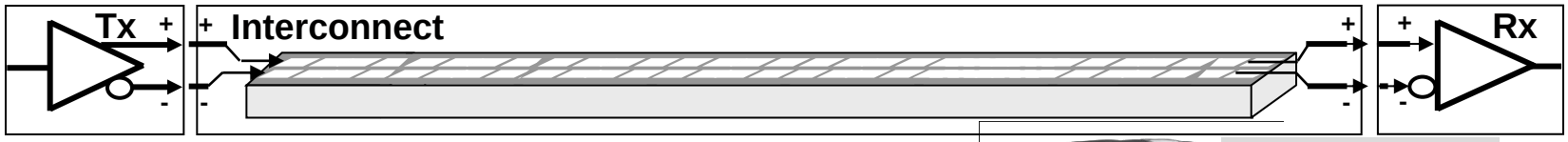



**"After" gating with visual trigger**

# High-Speed Serial Data Test Solutions…

Design → Verification → Compliance Test

PCI EXPRESS, SERIAL ATA, SUPERSPEED USB, ddr3, IEEE, GbE, DisplayPort, HDMI, MHL …



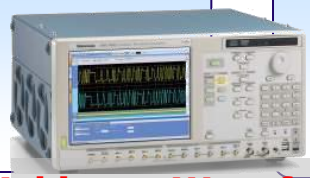

**System Integration**
**Digital Validation & Debug**

Logic Analyzers

Real-time Scopes

**Transmitter Testing**

**Receiver Test**
**Margin Testing**



Arbitrary Waveform Generator

Probing Fixtures

**Interconnect Test**

Sampling Scopes

**Compliance Test**

Compliance Test Software