

40 V High Voltage arbitrary waveform Pulse Generator at Automatic Parametric Tester

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This paper introduces the development work of high voltage pulse capability of Keithley Automatic Parametric Tester (APT). To meet the market demand for high voltage (40V) function/arbitrary waveform pulse generator, Keithley Instruments developed new pulse generator that implements both features of high voltage and function/arbitrary pulse waveform within single instrument. Integrated this new pulse generator into APT, provides flash memory manufacturer a powerful tool to measure flash memory device in both Fab and Lab environment more easily and quickly than ever before.

Flash memories are penetrating a wide variety of markets and products. Application examples are memory cards, MP3 audio players, cell phones, and digital cameras. This development work is driven by the demand of flash memory tests, more specifically, multilevel-flash-memories tests.

Takes same area size of memory cell and same process steps, a multilevel-flash-memory cell can store 2-bit-per-cell data in 4 levels of threshold voltage (V_{th}), or 4-bit-per-cell data in 16 levels of V_{th} . In comparison with 1-bit-per-cell flash memory cell that stores 1-bit data in 2 levels of V_{th} , the data storage density is doubled for 2-bit-per-cell memory, or is two folded for 4-bit-per-cell memory [1] [2]. Therefore, the cost of per bit is reduced significantly in multilevel-flash-memory.

In order to distinguish multilevel of V_{th} practically and easily in memory manufacturing, a higher V_{th} of the largest one is required and necessary, as shown in Fig. 1. This is where the high voltage comes in.

To program (write) each cell to the target V_{th} , program-then-verify approach is widely used. Takes 2-bit-per-cell as example, at beginning, an initial program operation sets each cell of a page of flash memory to one of level in the 3-step waveform pulse signal (Fig. 2). Then, a sequence of pulse is applied, each followed by a read operation for V_{th} verification.

It is essential to control each level of V_{th} in a tight range to avoid adjacent V_{th} overlap one another. Since the manufacturing deviation, the numbers of program pulse needed over a whole page of flash memory is spread widely, for example, the fastest cell needs 5 pulses to program to the target V_{th} , but the slowest cell needs 10 pulses. The slowest cell lags program speed. It is found that ramp-T (increase pulse width) method reduces the numbers of verification steps [3], furthermore, ramp-V (increase pulse amplitude) narrows the pulse width [4]. Put both of them together, the requirement of staircase waveform pulse signal (Fig. 3) comes out.

Figure 4 illustrates the hardware configuration of pulse generator in APT system. The pulse generator (4205-PG2 card) is installed in the chassis of Keithley 4200-SCS, 4200-SCS is mounted in the cabinet of Keithley S600 APT. Pulse signals are routed through test head to probe card, and send to wafer finally.

Software command set are coded to facilitate users to write their own algorithm easily and to migrate old algorithms easily. The commands are `p_init`, `p_config1`, `p_config2`, `p_config3`, `p_configS`, and `p_trig`. The commands start initialization and trig, defines waveform of pulse level 1, 2, 3 and staircase accordingly.

Wafers from different manufacturers were tested using new tool, test results are well correlated to those that is from previous tool. Test speed improvement dramatically.

In summary, high voltage (40V) function/arbitrary waveform pulse generator is integrated in APT tester for multilevel flash memory measurement. The reasons why high voltage arbitrary waveform pulse generator is important are addressed. Hardware and software structure are described. Test result shows satisfied correlation and faster throughput than old tool.

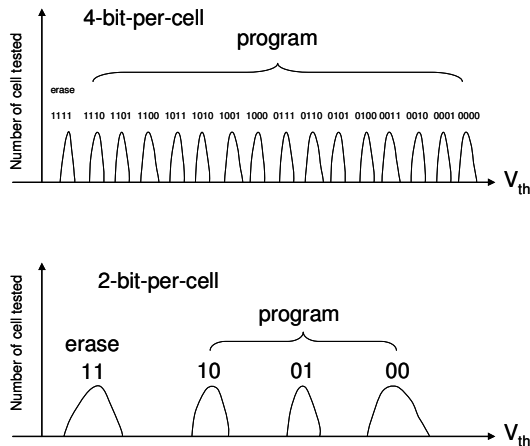


Fig. 1 Profile of multilevel-flash-memory gate threshold voltage V_{th} distribution

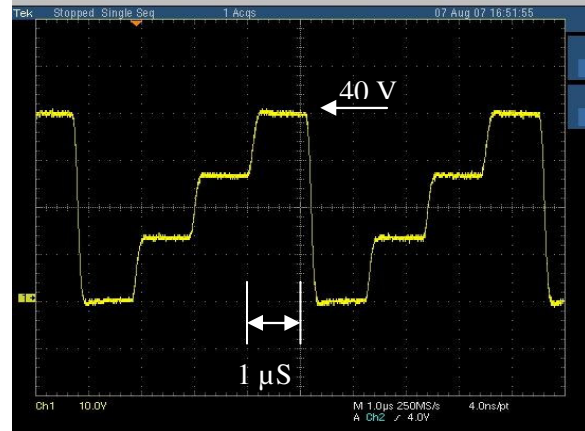


Fig. 2 A 3-step waveform signal in one burst of pulse. It is defined by single command of p_config3.

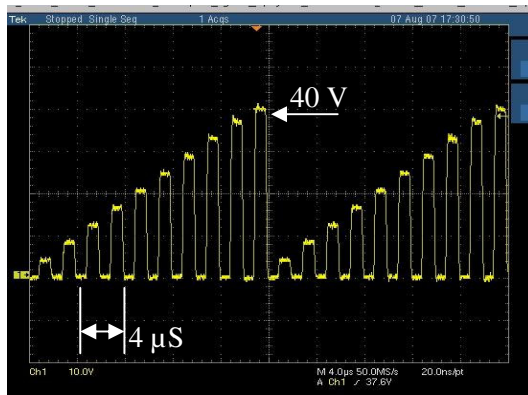


Fig. 3 A 10-levels staircase waveform signal in one burst of pulse. It is defined by single command of p_configS.

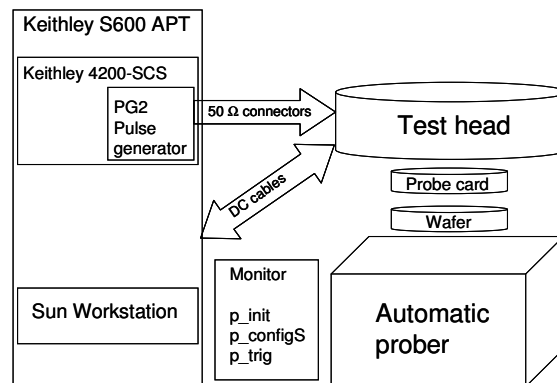


Fig. 4 Hardware configuration of high voltage arbitrary waveform pulse generator in Keithley S600 Automatic Parametric Test (APT) system

References

- [1] Marco Grossi, M. Lanzoni, and B. Ricco, "A Novel Algorithm for High-Throughput Programming of Multilevel Flash Memories," *IEEE Trans. Electron Devices*, Vol. 50, No. 5, pp. 1290-1296, May 2003. (Journal Article)
- [2] Shuka Zernovizky and Rochelle Singer, "4-Bit/Cell NAND Usage Impossible? Possible!," *White Paper, msystems, SanDisk*, 01-WP-0406-00, Rev 1.0, May 2006.
- [3] Toshihiro Tanaka, M. Kato, T. Adachi, K. Ogura, K Kimura and H. Kume, "High-Speed Programming and Program-Verify Methods Suitable for Low-Voltage Flash Memories," *1994 Symposium on VLSI Circuits Digest Technical Papers*, pp. 61-62, June 1994.
- [4] Kang-Deog Suh, B. Suh, Y. Lim, J. Kim, Y. Choi, Y. Koh, S. Lee, S. Kwon, B. Choi, J. Yum, J. Choi, J. Kim, and H. Lim, "A 3.3V 32Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme," *1995 IEEE Internal Solid State Circuits Conference, Digest of Technical papers, 42nd ISSCC*, section 7, pp. 128-129, Feb. 1995.