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An Introduction to GaN-on-Si Power Device Technology

廣鎵光電 研發中心

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Outline

- **Why GaN on Si for Power Device Application**
- **Epitaxial and Device Design Concepts**
- **Current Market & Technology Development Status**

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Why GaN on Si for Power Device Application

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Prerequisites for a Good (Semiconductor) Power Device

- Large forward and/or reverse blocking, small leakage current
- High on-state current, small on-state voltage
- Fast switching – short turn-on and turn-off time
- Small control power – large input impedence
- Withstanding of high voltage and high current during switching – Good SOA (Safe Operating Area)
- Positive temperature coefficient of on-state resistance
- Large dv/dt and di/dt ratings
- Normally off

Power Devices

= High current, High voltage, Low loss (P_{con}, P_{sw}), Reliable, Easy to control

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Materials Property Comparison

Comparison of semiconductor material properties at room temperature

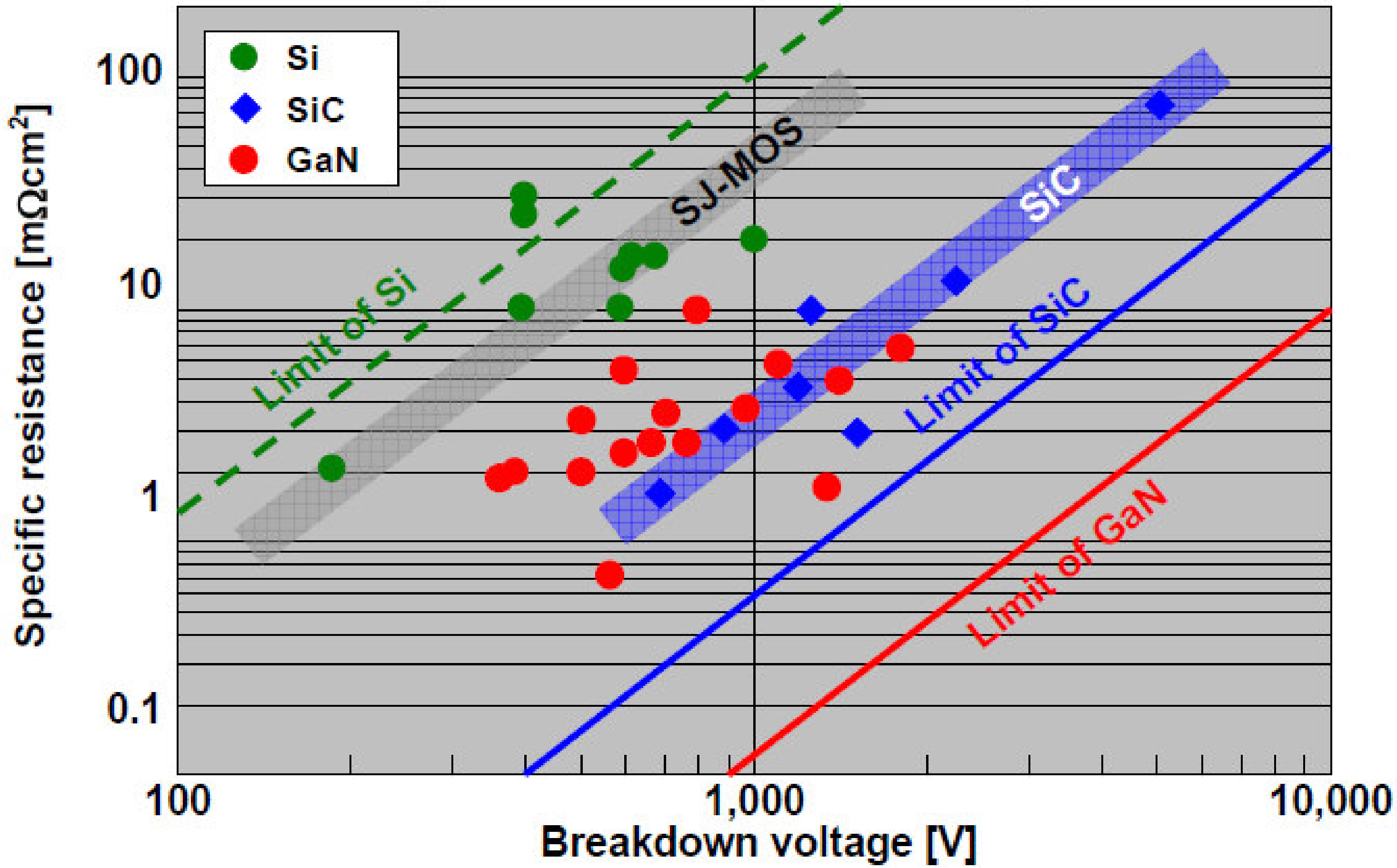
Property	Si	GaAs	4H-SiC	GaN
Bandgap，E_g (eV)	1.12	1.42	3.25	3.4
Dielectric constant，ε	11.8	12.8	9.7	9
Breakdown field Ec (MV/cm)	0.3	0.4	3	4
Electron mobility μ (cm^2/V-s)	1500	8500	1000	1250
Maximum velocity Vs (10^7 cm/s)	1	1	2	3
Thermal conductivity λ (W/cm-K)	1.5	0.5	4.9	2.3
CFOM = $\lambda\ \varepsilon\ \mu V_S E_C^2 / (\lambda\ \varepsilon\ \mu V_S E_C^2)_{si}$	**1**	**3.6**	**358**	**520**

High-speed
High-power
High-temperature

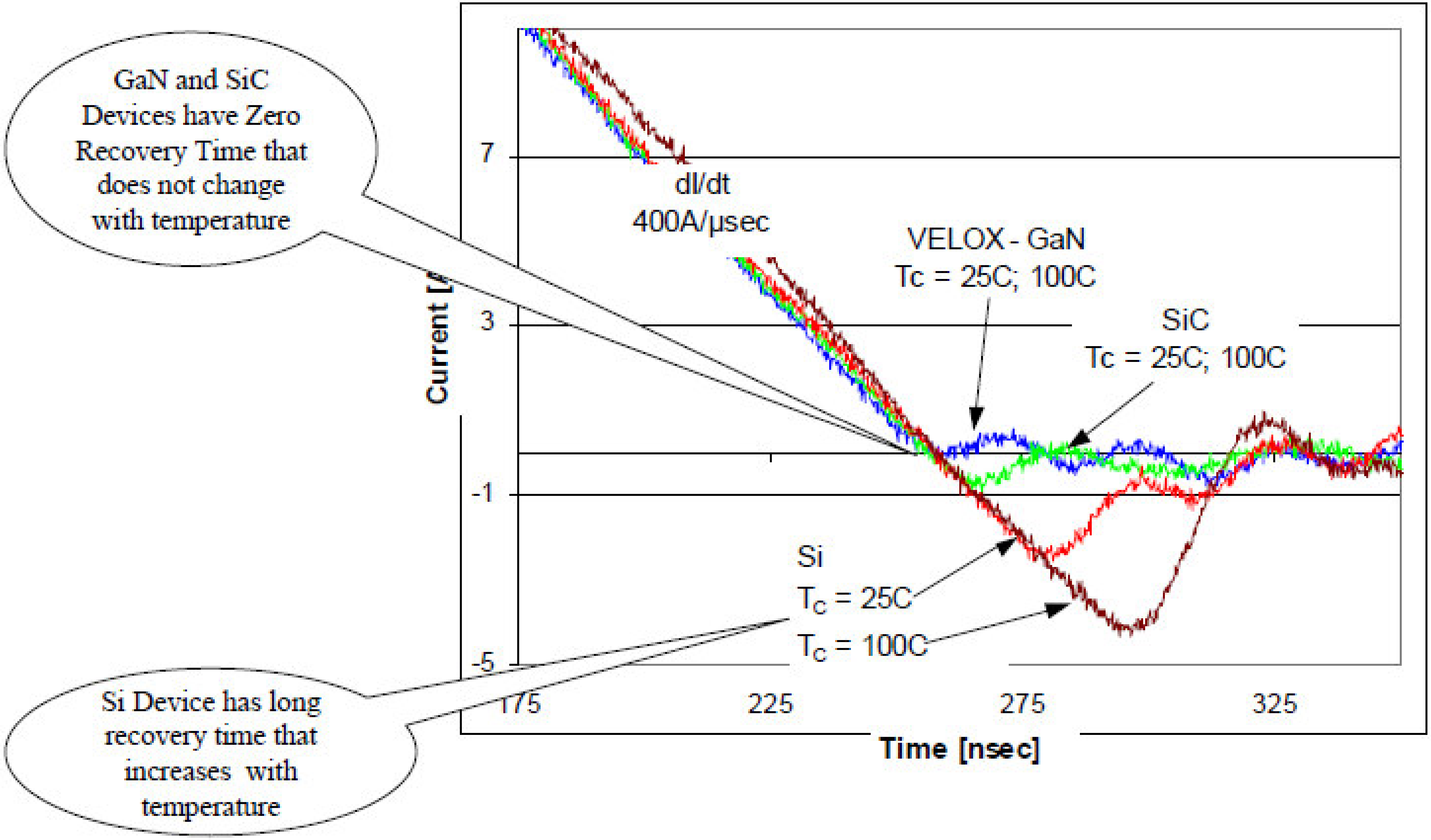
- **Si : lowest cost, large volume, bad Trr characteristic at HT.**
- **SiC : so far high crystal quality, but high cost.**
- **GaN : low cost, highest CFOM value.**

Advantage of High Breakdown and Low On-resistance

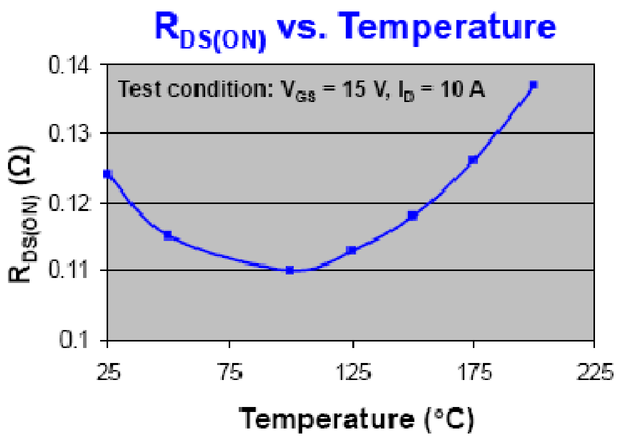
While the performance of Si power devices are approaching the theoretical limit of material, GaN and SiC have much room for both of reduction of specific resistance and improvement of breakdown voltage.

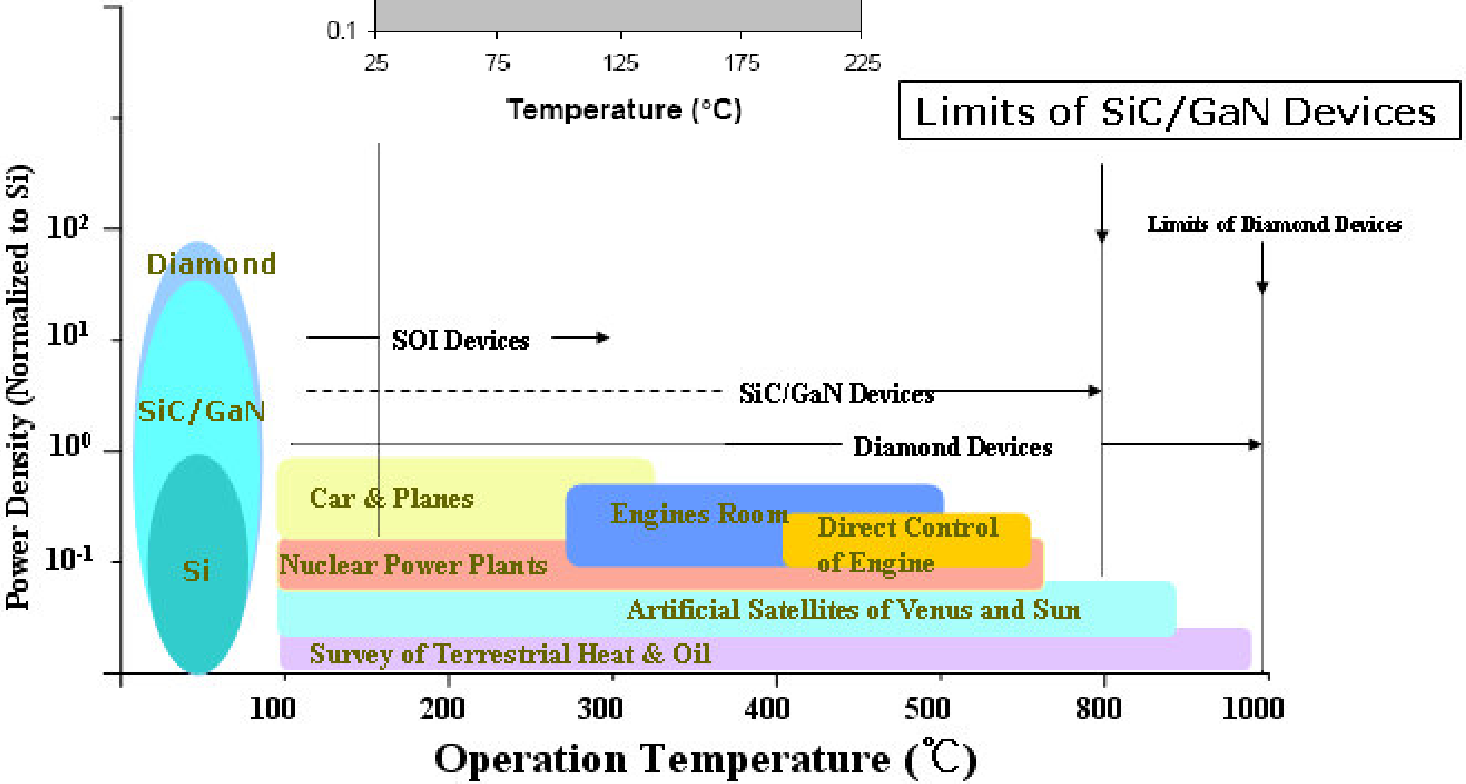


Advantage of Fast Switching Speed

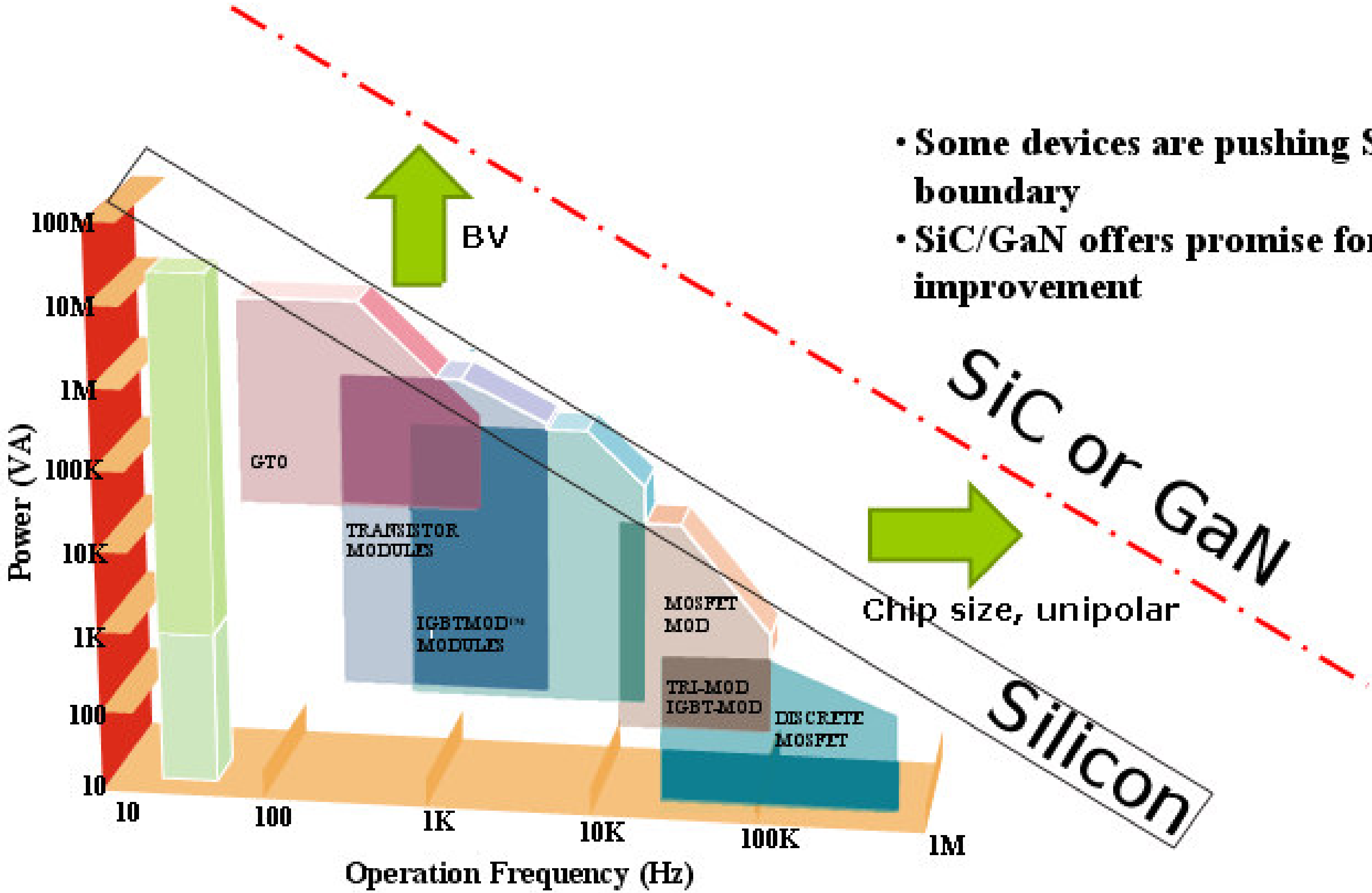


Advantage of High-Temperature Application





Advantage of Microwave High-Power Application



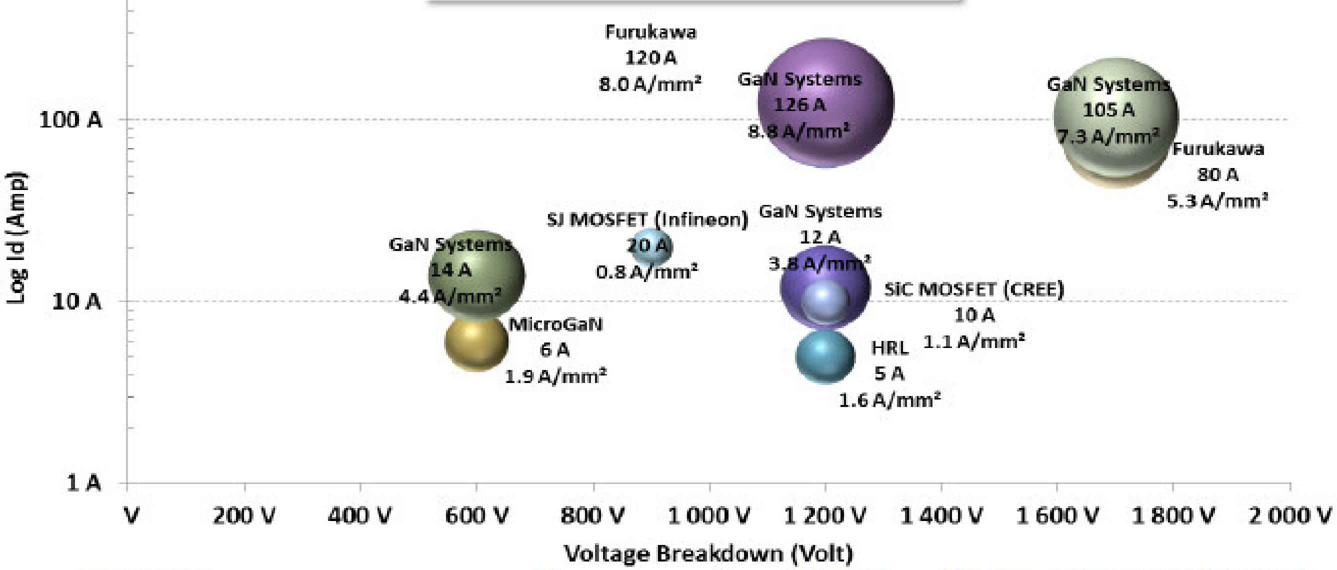
- Some devices are pushing Si boundary
- SiC/GaN offers promise for improvement

Modified from an Application Note of Powerex, Inc. Youngwood, PA.

Comparison of Best Power Device R&D Results

Comparison of Best GaN HEMT R&D Results
Vb, I and A/mm² with Existing SJ MOSFET and SiC MOSFET

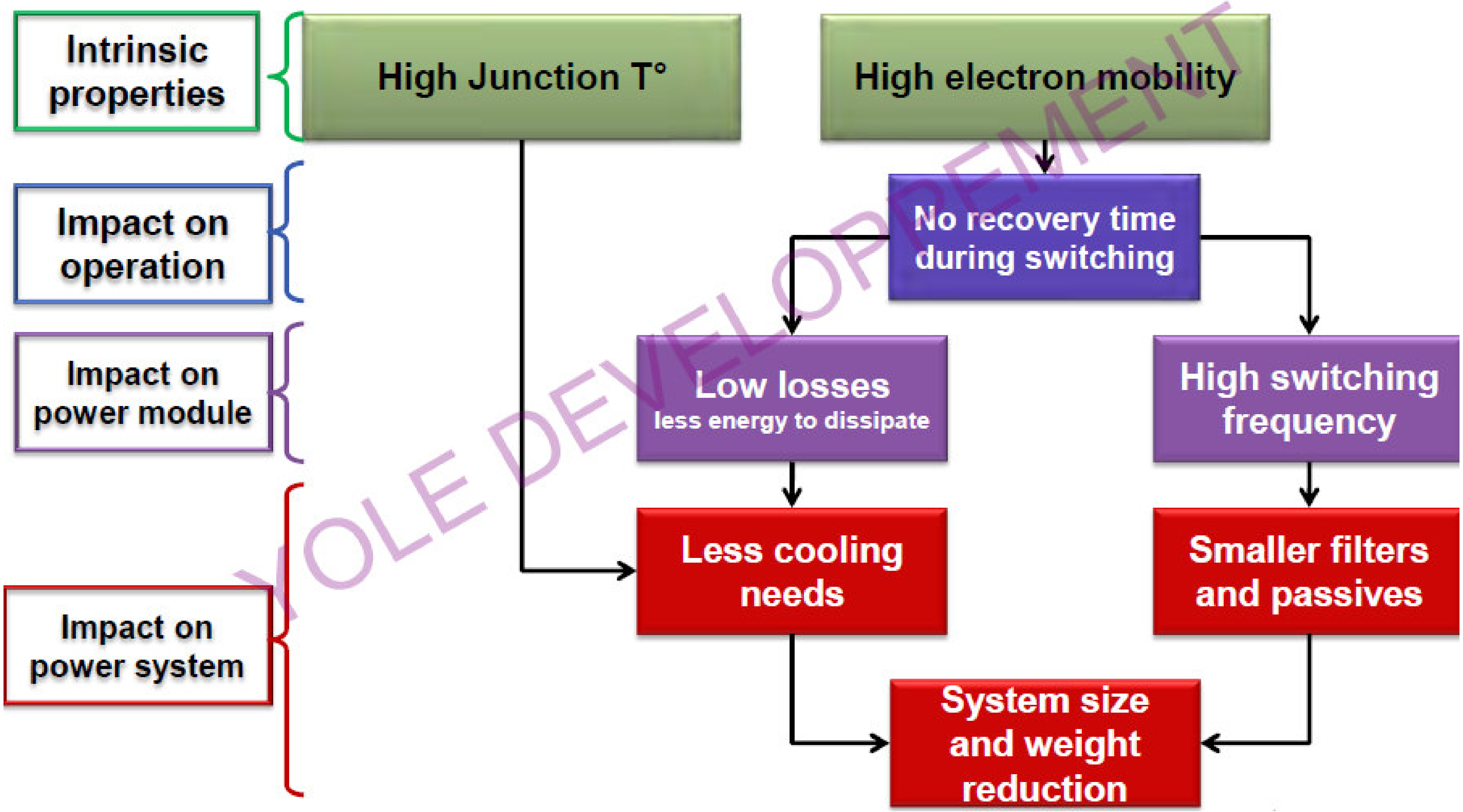
A/mm² as a function of V and I



R&D results	V	I	Chip-size	W/mm²	Amp / mm²	Technology
MicroGaN	600 V	6 A	3.21 mm²	1 121	1.9 A/mm²	GaN-on-Si
GaN Systems	600 V	14 A	3.20 mm²	2 625	4.4 A/mm²	GaN-on-SiC
HRL	1 200 V	5 A	3.13 mm²	1 917	1.6 A/mm²	GaN-on-Si
GaN Systems	1 200 V	12 A	3.20 mm²	4 500	3.8 A/mm²	GaN-on-SiC
Furukawa	1 200 V	120 A	15.00 mm²	9 600	8.0 A/mm²	GaN-on-Si
GaN Systems	1 200 V	126 A	14.40 mm²	10 500	8.8 A/mm²	GaN-on-SiC
Furukawa	1 700 V	80 A	15.00 mm²	9 067	5.3 A/mm²	GaN-on-Si
GaN Systems	1 700 V	105 A	14.40 mm²	12 396	7.3 A/mm²	GaN-on-SiC
SJ MOSFET (Infineon)	900 V	20 A	25.00 mm²	720	0.8 A/mm²	Silicon
SiC MOSFET (CREE)	1 200 V	10 A	9.00 mm²	1 333	1.1 A/mm²	SiC-on-SiC

GaN power devices

GaN & SiC Added Values



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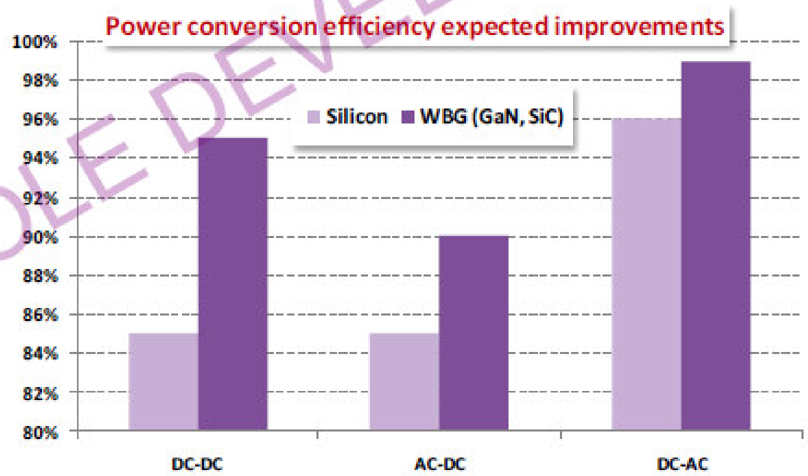
Advantage of Enhanced System Efficiency

GaN & SiC Use

Expected added-value in power conversion

	Expected improvement (%) compared with Silicon	Efficiency value improvements
DC-DC (POL, boost…)	+10% points	85% → 95%
AC-DC (PFC, UPS…)	+5% points	85% → 90%
DC-AC (Motor, PV…)	+2 to +3% points	96% → 99%



GaN power electronics

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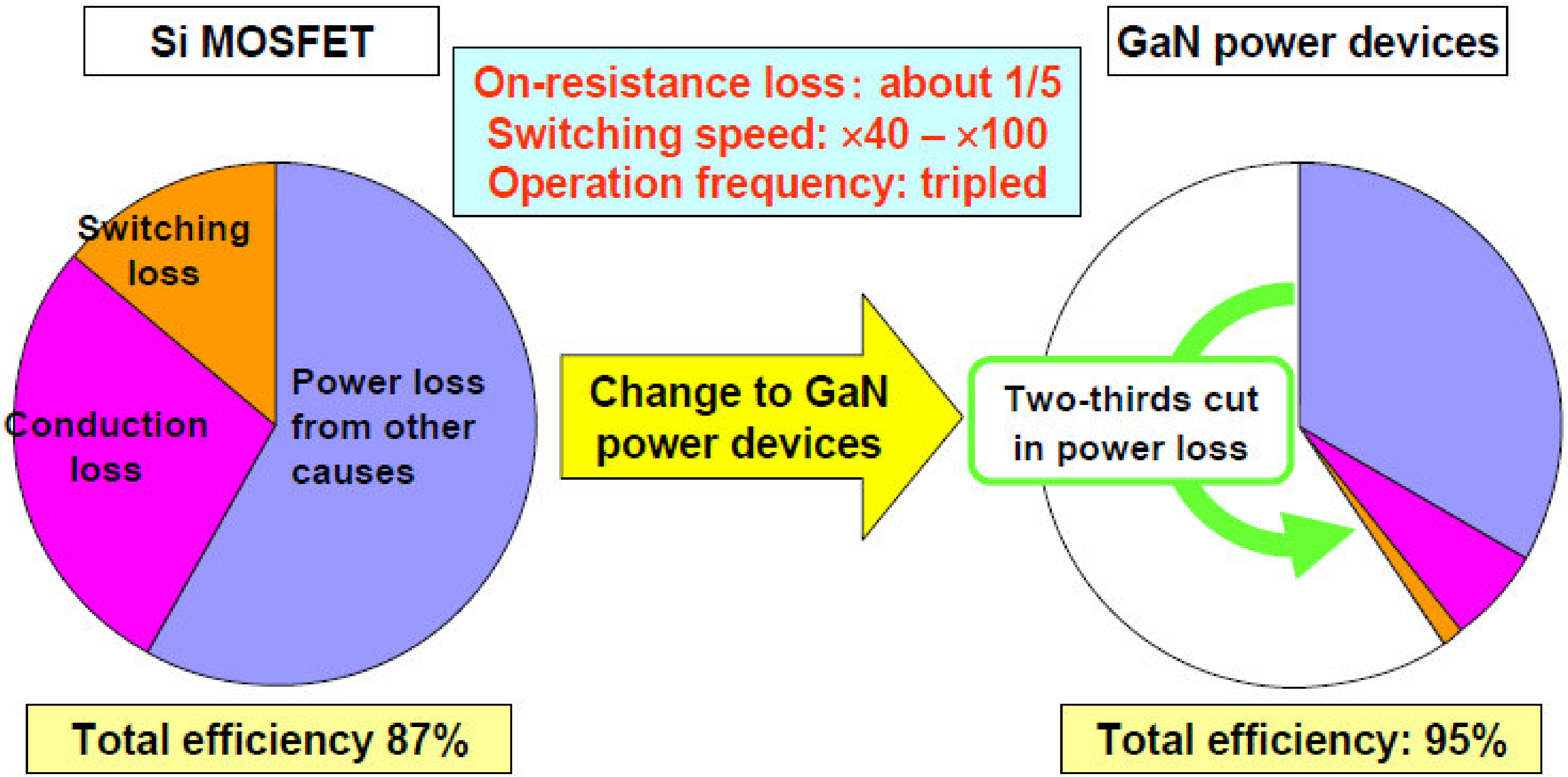
Advantage of Enhanced System Efficiency

GaN power devices are expected to become the key to power saving and downsizing of the system by optimizing the surrounding circuit and components to take maximum advantage of GaN HEMTs that the gate charge can be reduced without increasing the on-resistance.



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Advantage of Cost and Circuit Integration

Materials/ technology	Wafer size	Die area	Circuit integration	Cost
SiC	X	△	X	X
GaN-on-Si	△→√ (?)	√	√ (?)	△
Si	√	X	√	√

√ : Best

△ : Middle

X : Poor

6-inch (and above) AlGaN/GaN wafer on Si (111) substrate is now technologically feasible, low cost and possible integration with Si-based circuits.

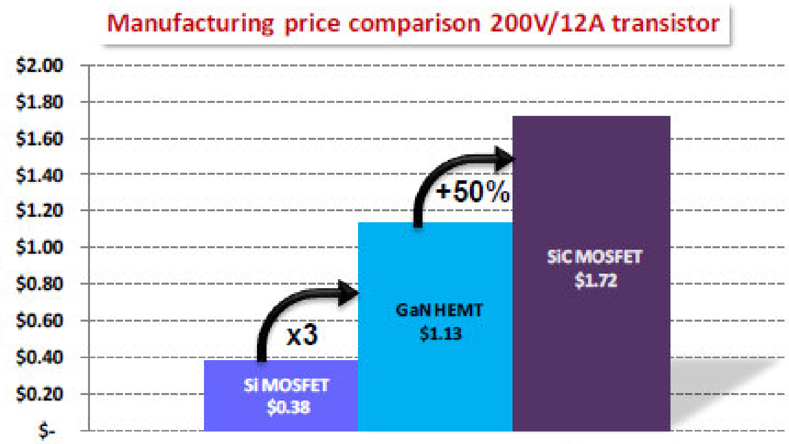
Advantage of Product Cost

Manufacturing Price of a 200V/12A Transistor

Comparison Si, GaN & SiC

- We have used our proprietary reverse costing tool: CoSim+ to simulate the manufacturing price of the same device made with Si, GaN and SiC technologies.
- Manufacturing price is the result of the following operation:
  - Manufacturing cost + G&A (General & Administrative) + R&D expenses + Cost of Sales + Operational margin
  - That is the sale price right at the facility door. The distribution costs (DigiKey…etc…) are not included here.
  - Manufacturing price + Distribution costs = B-to-B floor price

	Si MOSFET	GaN HEMT	SiC MOSFET
Vb	200 V	200 V	200 V
Imax	12 Amp	12 Amp	12 Amp
Die size	6.25 mm²	5.76 mm²	3.06 mm²
Wafer ø	6"	6"	4"
Prod. Yield	95%	88%	75%
Manuf. Cost	$ 0.22	$ 0.57	$ 1.11
Manuf. Price	$ 0.38	$ 1.13	$ 1.72



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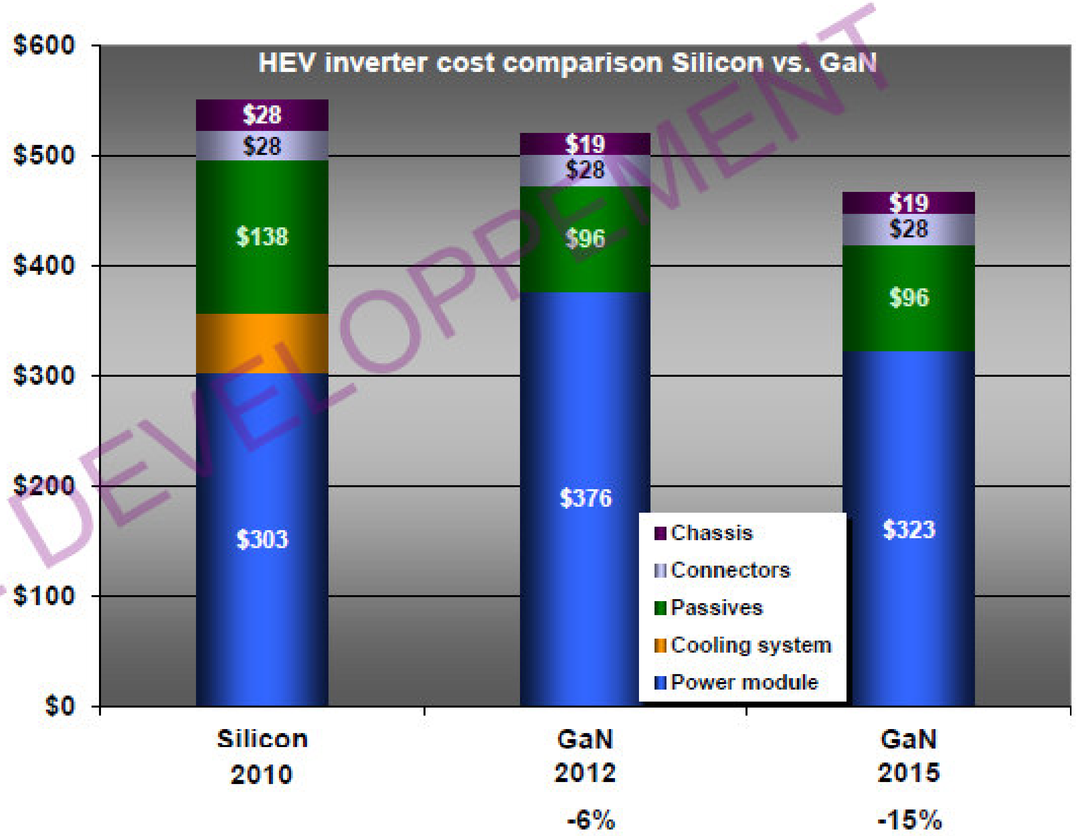
Toyota: Inverter Cost Comparison

Case Study
Silicon vs. GaN HEV inverter cost breakdown

Hypothesis:

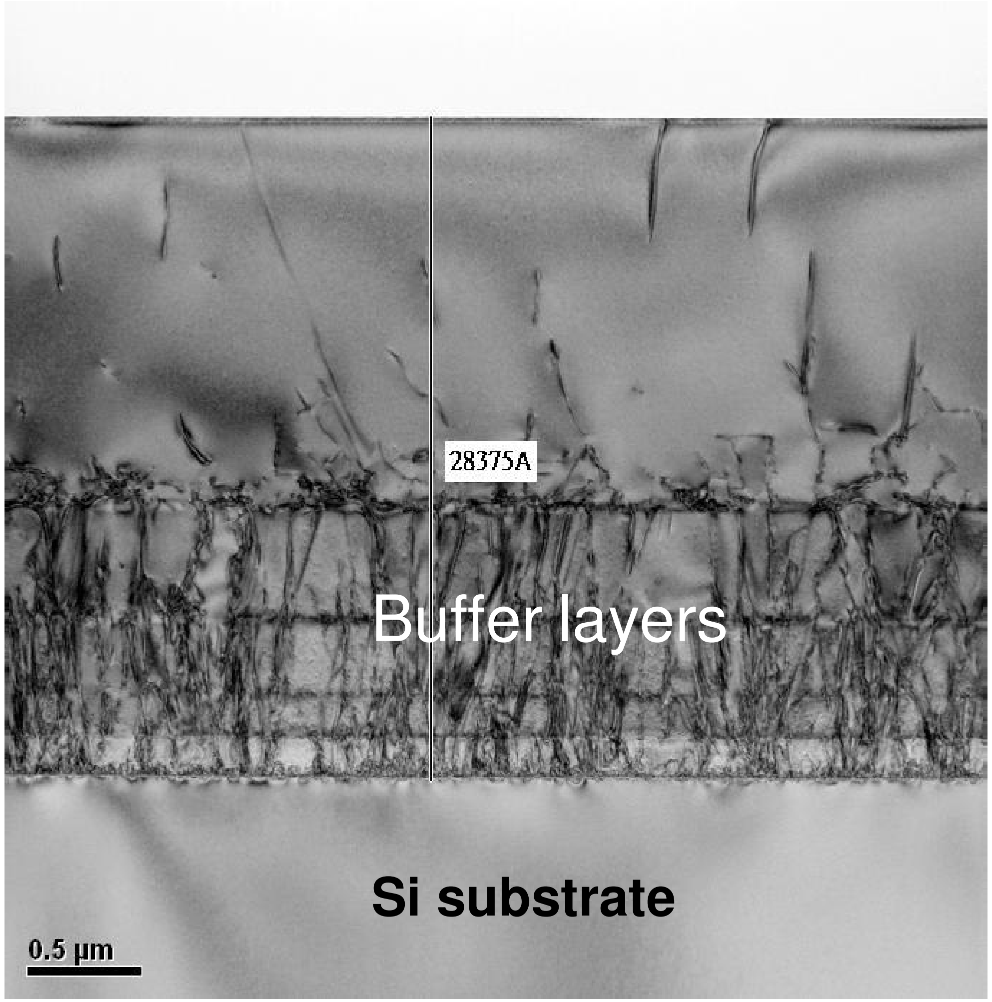
- No more water-cooling system with GaN
- Passive costs will decrease 30% with the use of GaN
- Chassis cost will decrease 30% due to size shrinking and simplification of thermal management
- Connector cost will remain the same
- GaN technology is available and reliable!



Source: CS Europe/Phillip Roussel – Yole Development

Epitaxial and Device Design Concepts

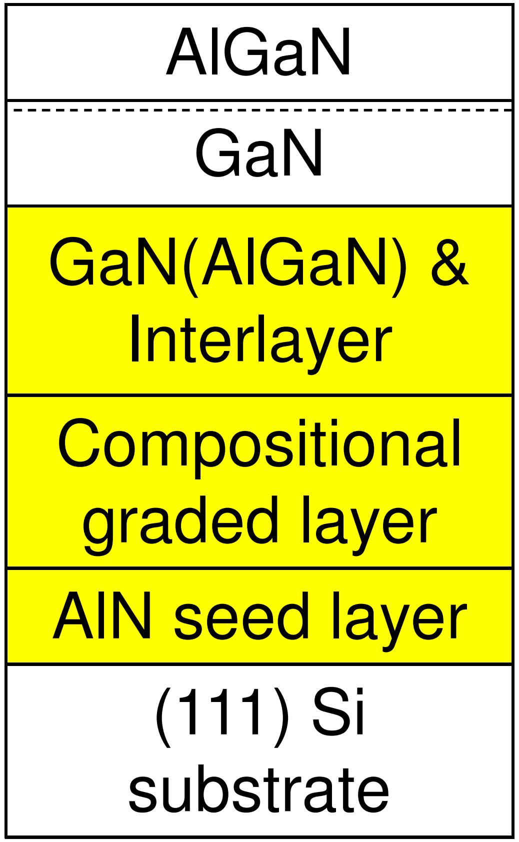
Growth of GaN on Si Substrate



Difficulties of GaN-on-Si epitaxy:

1. Large-area epitaxial technology
2. Ga reaction with Si substrate
3. Large lattice mismatch (~17%)
4. Large thermal expansion coefficient difference (~54%)

Buffer Structure



LT-AlN interlayer

LT-GaN inetrlayer

SiN interlayer

C, Fe…etc doping

1.AlGaN step or linear graded layer

2. AlGaN/AlN SL

1. HT/LT AlN buffer (MOCVD)

2. PVD AlN buffer (or Al2O3, Ga2O3…etc)

1.Thick substrate

2. Selective area growth

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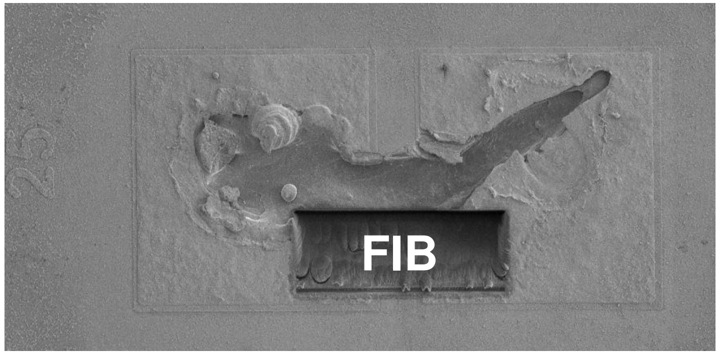
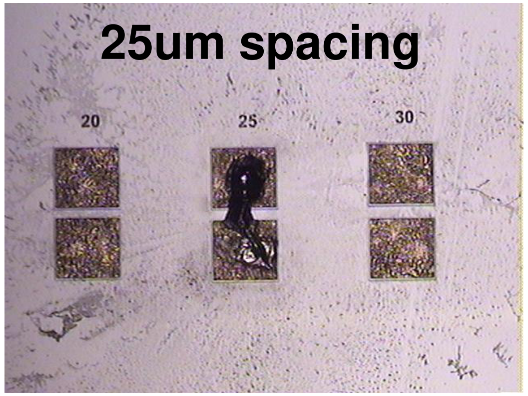
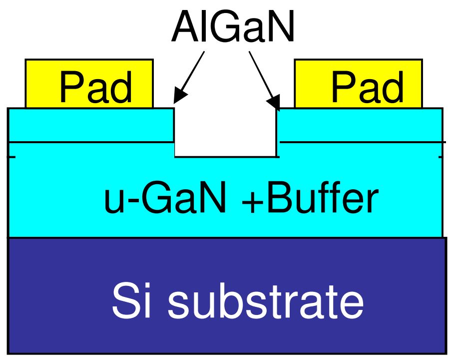
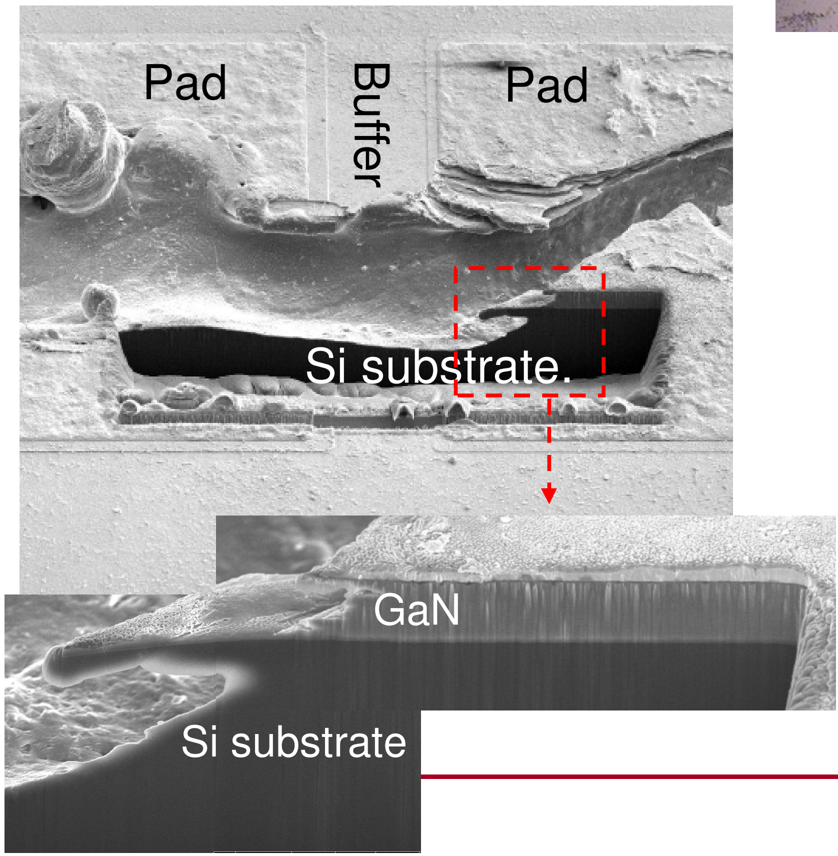
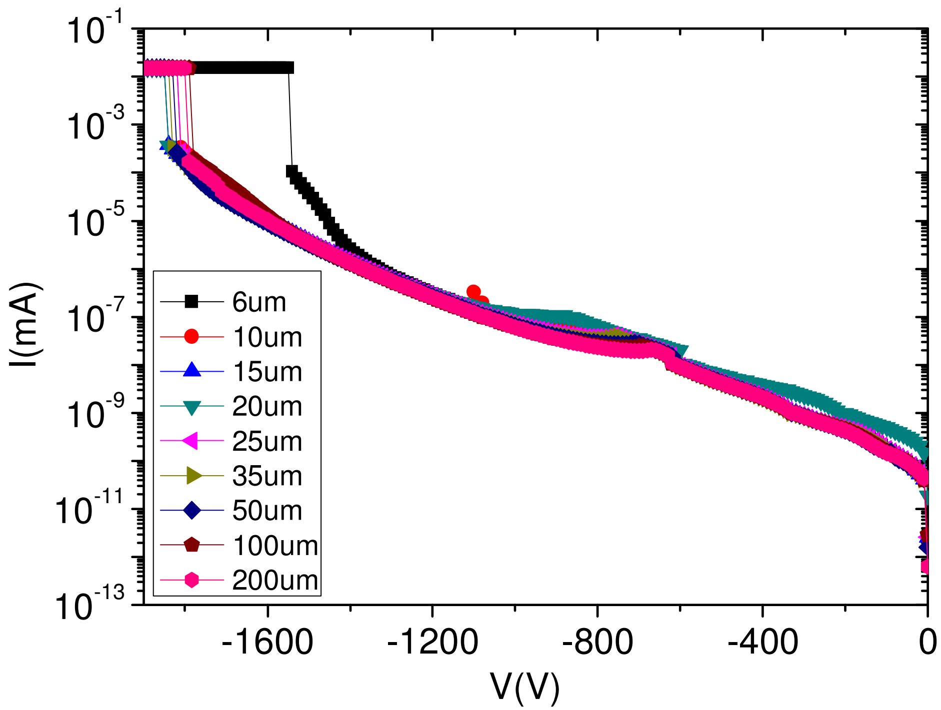
Buffer Breakdown Behavior











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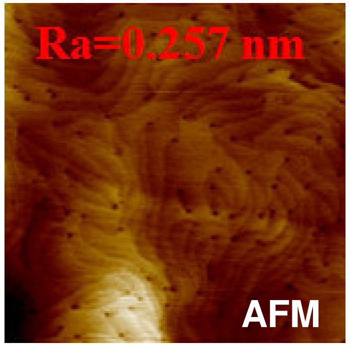
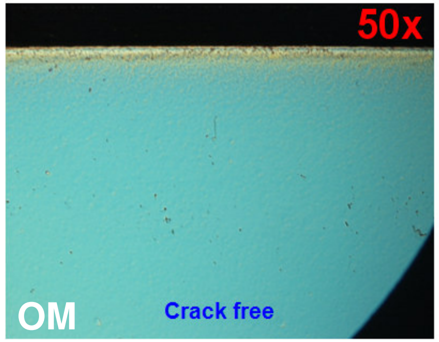
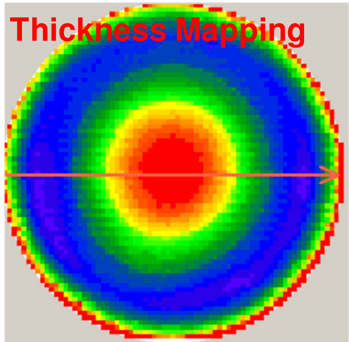
Typical GaN-on-Si 2-DEG Epi Wafer Specification

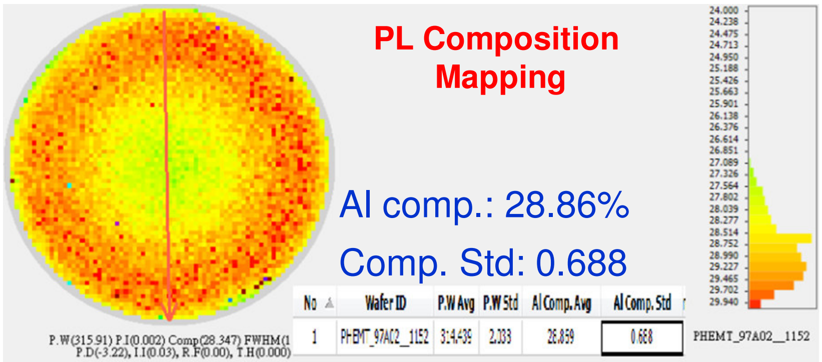
Items	Huga
Mobility	~1300 cm²/V·s
Sheet concentration	~1 × 10^{13} cm^{-2}
FWHM of GaN(002)	~590 arcsec
FWHM of GaN(102)	~850 arcsec
Roughness	~0.5nm
Bowing	< 20 um
Crack area	2mm from edge
Thickness of GaN&buffer	4~7 um
AlGaN Composition U%	Edge to center <2%
Buffer Vbr (Pad width=160um)	>1000V
Buffer leakage current (@600V, Pad width=160um)	~3E-9A





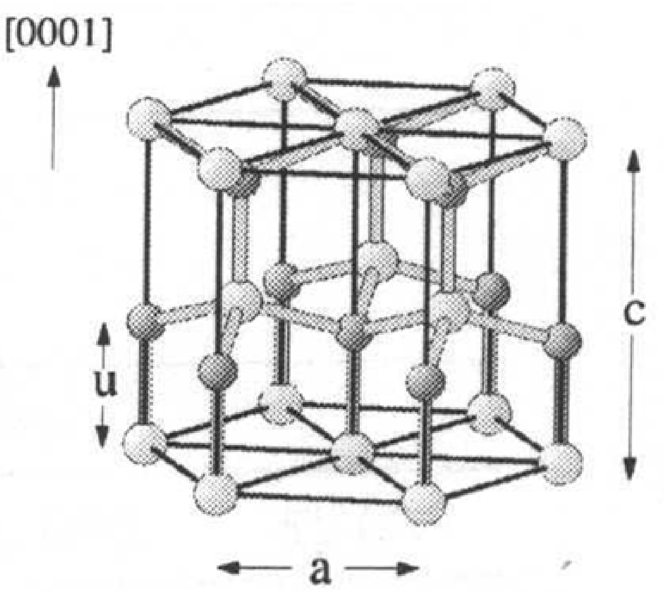


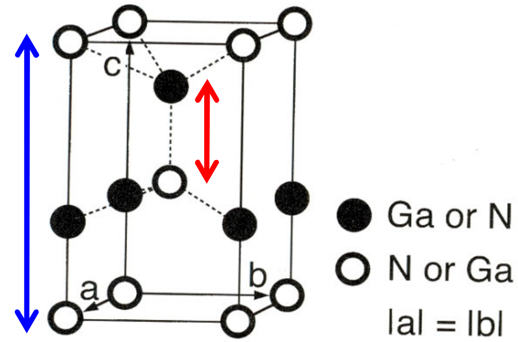
Thickness Avg:4.66μm
Thickness Std:0.064μm
Wafer bow≒10μm



Spontaneous Polarization

Wurtzite (hcp)





u_0 = red/blue

$u_{0,ideal}=0.375$

TABLE I. Structural parameters for AlN, GaN, and InN.

	a_0 (bohr)	c_0/a_0	u_0
AlN	5.814	1.6190	0.380
GaN	6.040	1.6336	0.376
InN	6.660	1.6270	0.377

Cation and anion centers do not overlap.

→ Spontaneous polarization

P_{SP} =

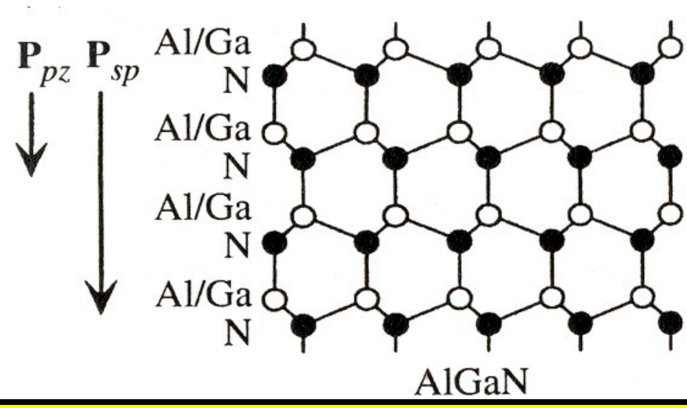
AlN	$-0.081\ C/m^2$
GaN	$-0.029\ C/m^2$
InN	$-0.032\ C/m^2$

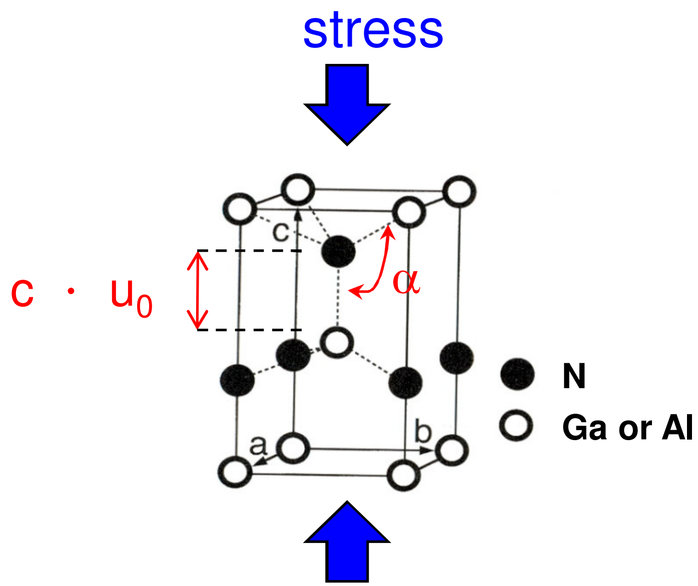
Piezoelectric Polarization

Note: Polarization is oriented from negative to positive charge.

e.g.,
AlGaN coherently strained to GaN (AlGaN is under tensile stress)

Cation-terminated surface





When the AlGaN lattice is compressed in c direction:

- Bonding length c · u_0 is the same; angle α becomes even smaller.
- Negative charge move upward and positive charge moves downward.
- Direction of piezoelectric polarization is toward $[000\bar{1}]$, which is the same as $\mathbf{P}_{sp}$.

AlGaN/GaN Heterojunction

Polarization direction:

e.g.,
AlGaN coherently strained to GaN (AlGaN is under tensile stress)

$$\mathbf{P}_{SP} = P_{SP}\mathbf{z}$$

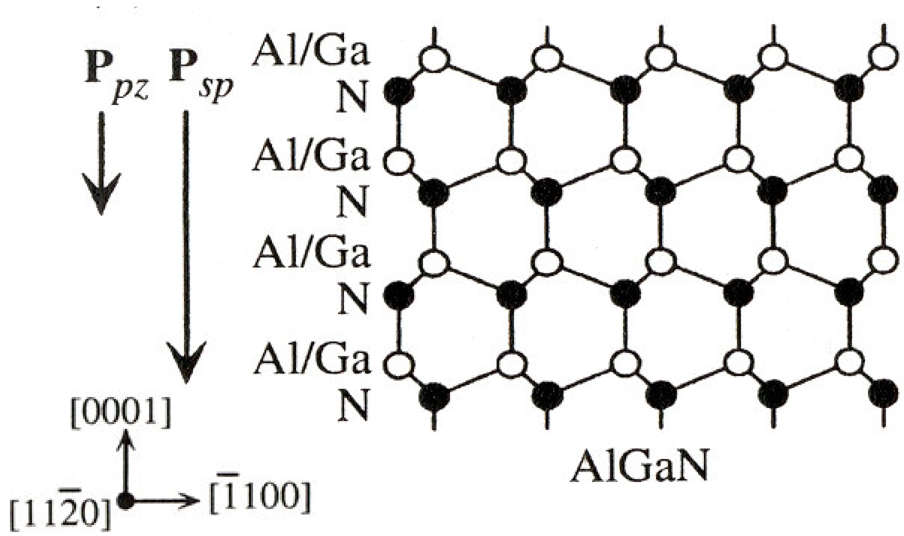
$$\mathbf{P}_{PE} = P_{PE}\mathbf{z}$$

$$P_{PE} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)$$

For AlGaN:

$$[e_{31} - e_{33}(C_{13}/C_{33})] < 0 \qquad \frac{a-a_0}{a_0} > 0$$

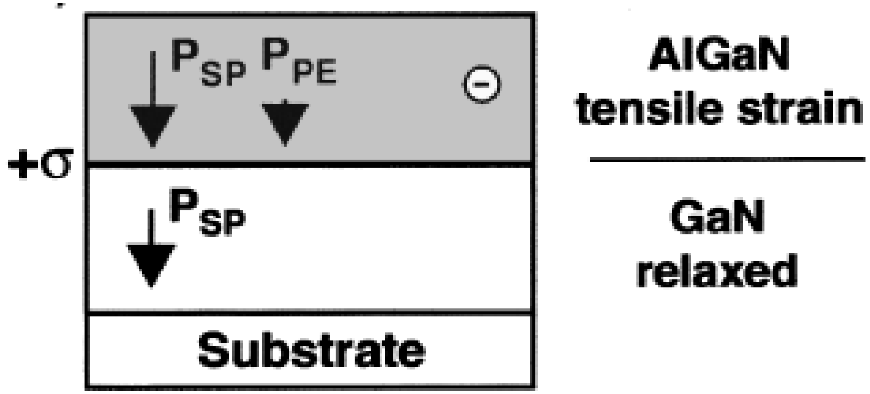
Cation-terminated surface



Both $\mathbf{P}_{SP}$ and $\mathbf{P}_{PE}$ are toward $[000\bar{1}]$ direction.

Polarization-Induced Electrostatic Charge and 2DEG

e.g., For AlGaN/GaN heterostructure with cation-terminated surface



Induced positive electrostatic charge σ at the AlGaN layer of the AlGaN/GaN interface is

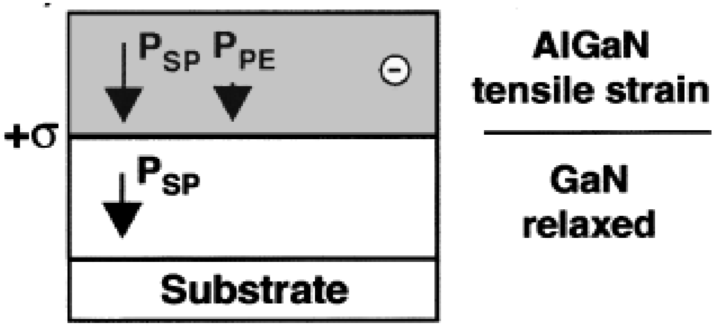
$$\sigma = P(\text{top}) - P(\text{bottom})$$

$$= \{P_{SP}(\text{top}) + P_{PE}(\text{top})\} - \{P_{SP}(\text{bottom}) + P_{PE}(\text{bottom})\}.$$

where the determination of P_{SP} and P_{PE} are mentioned earlier.

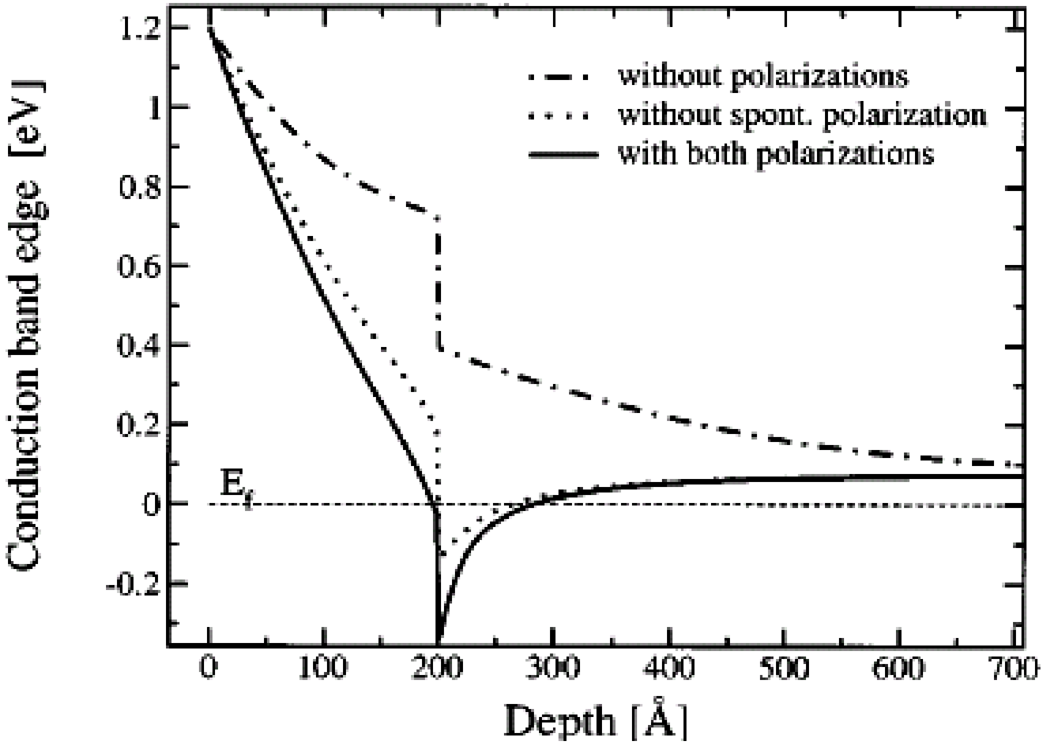
Polarization-Induced Electrostatic Charge and 2DEG

e.g., For AlGaN/GaN heterostructure with cation-terminated surface



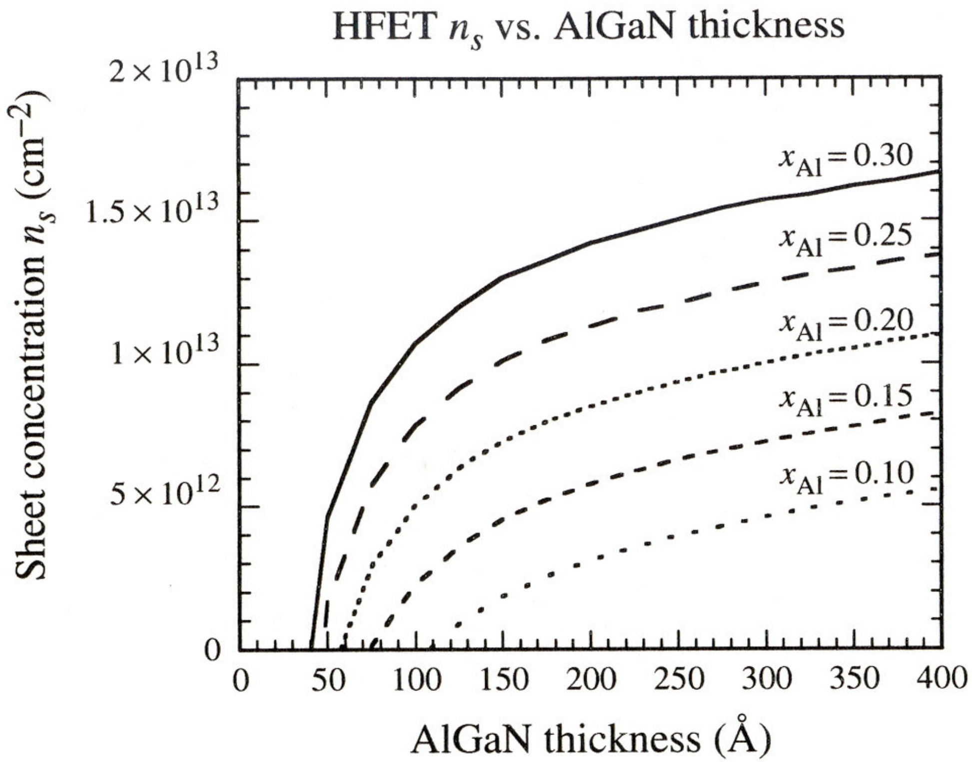
GaN effective conduction band density of states 1.2 x 10^{18} cm^{-3} compared to GaAs 4.7×10^{17} cm^{-3} at 300 K

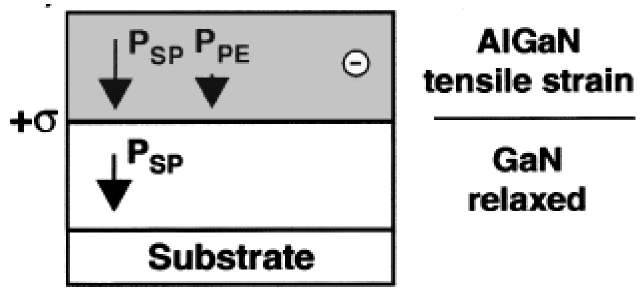
w/o polarization and heterojunction, no interface 2deg is generated.



Polarization-Induced Electrostatic Charge and 2DEG

AlGaN thickness and composition effect on Ns:





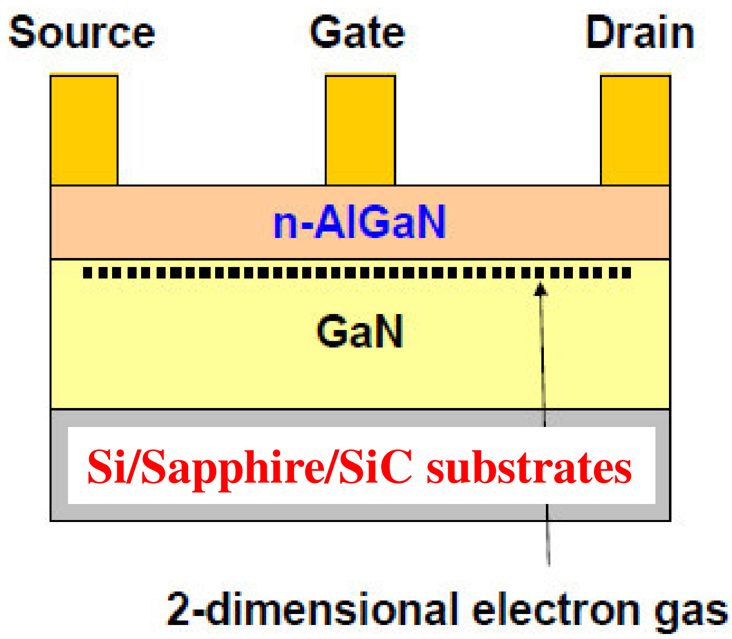
$$n_S(x) = \frac{+\sigma(x)}{e} - \left(\frac{\epsilon_0 \epsilon(x)}{de^2}\right)[e\phi_b(x) + E_F(x) - \Delta E_C(x)],$$

AlGaN/GaN Heterojunction

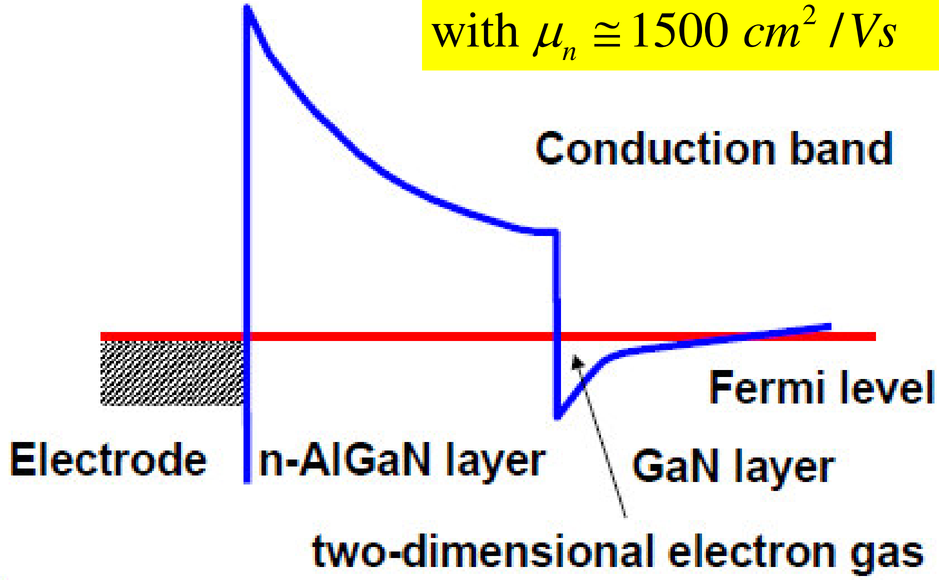
GaN HEMT is a device utilizing two-dimensional electron gas generated at the interface of GaN and n-AlGaN by the difference of the lattice parameter. This working mechanism allows GaN HEMT to suppress gate capacitance and to achieve high-speed switching with low power loss.

$$qn_S = \sigma_{polarization} > 1\times10^{13}/cm^2$$

with $\mu_n \cong 1500\ cm^2/Vs$



Cross section of GaN HEMT (Normally-on)



Band structure of GaN HEMT

Current Market & Technology Development Status

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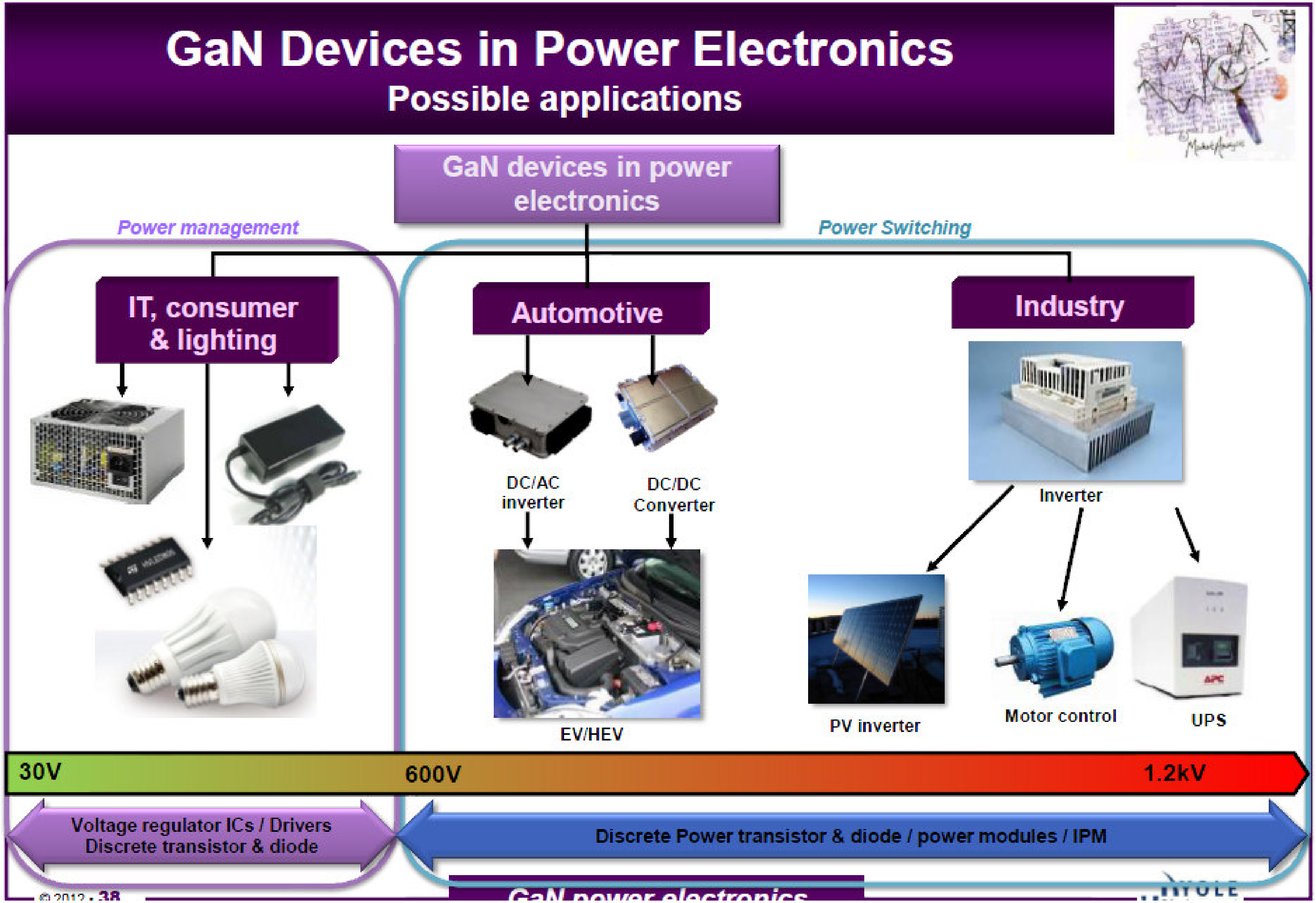
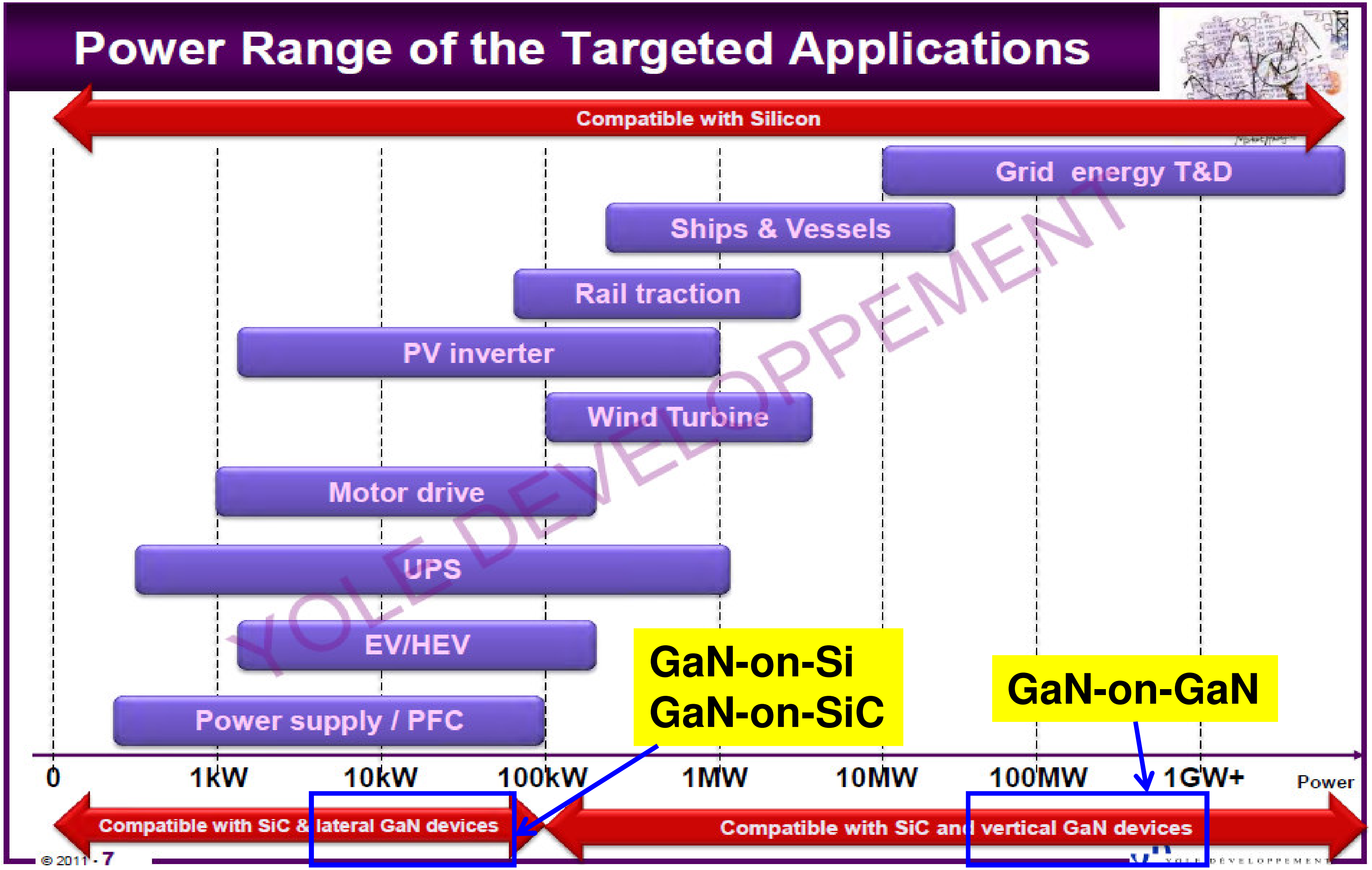
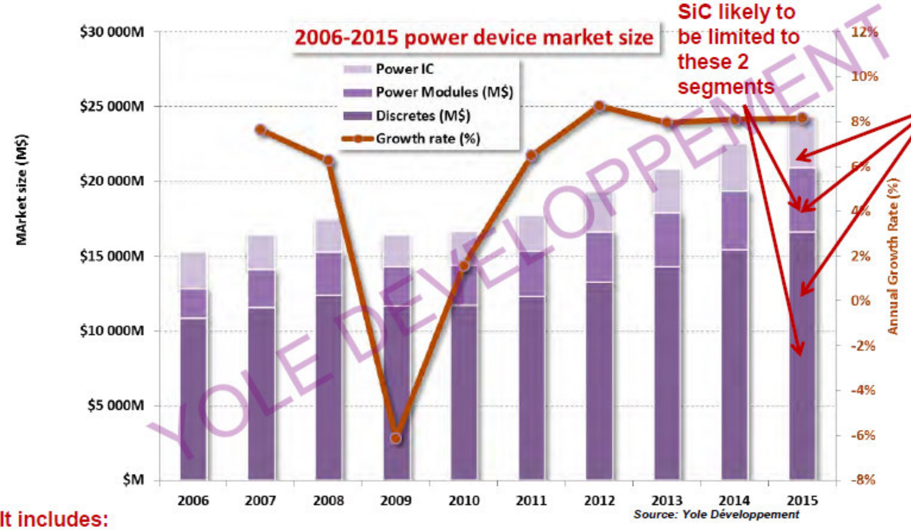
GaN-related Power Device Application



GaN-related Power Device Application

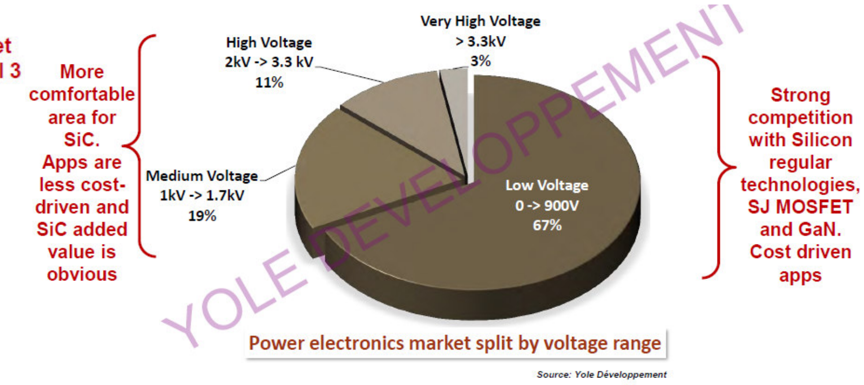


Product Type and Market

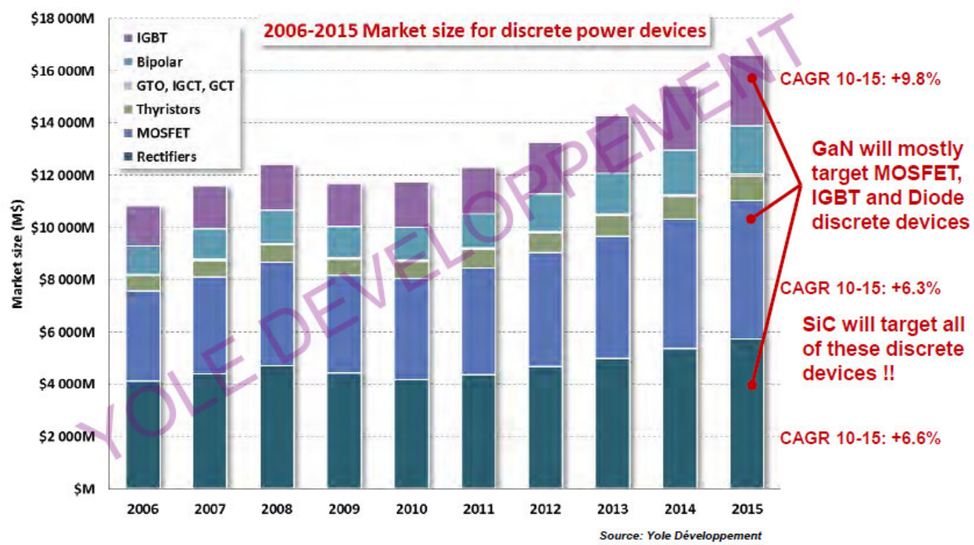


It includes:

- Power IC: power management IC: mainly voltage regulators (POL) and drivers
- Power modules: IGBT, diode or MOSFET modules, IPM
- Power discretes: MOSFET, rectifier, IGBT, Bipolar….

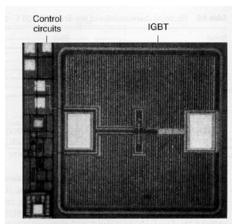


Breakdown for a total market size of ~$16.4B in 2009



Power discrete

Power module



Power IC

Source: CS Europe/Phillip Roussel/ Yole Development

GaN vs SiC Market Growth Prediction Comparison

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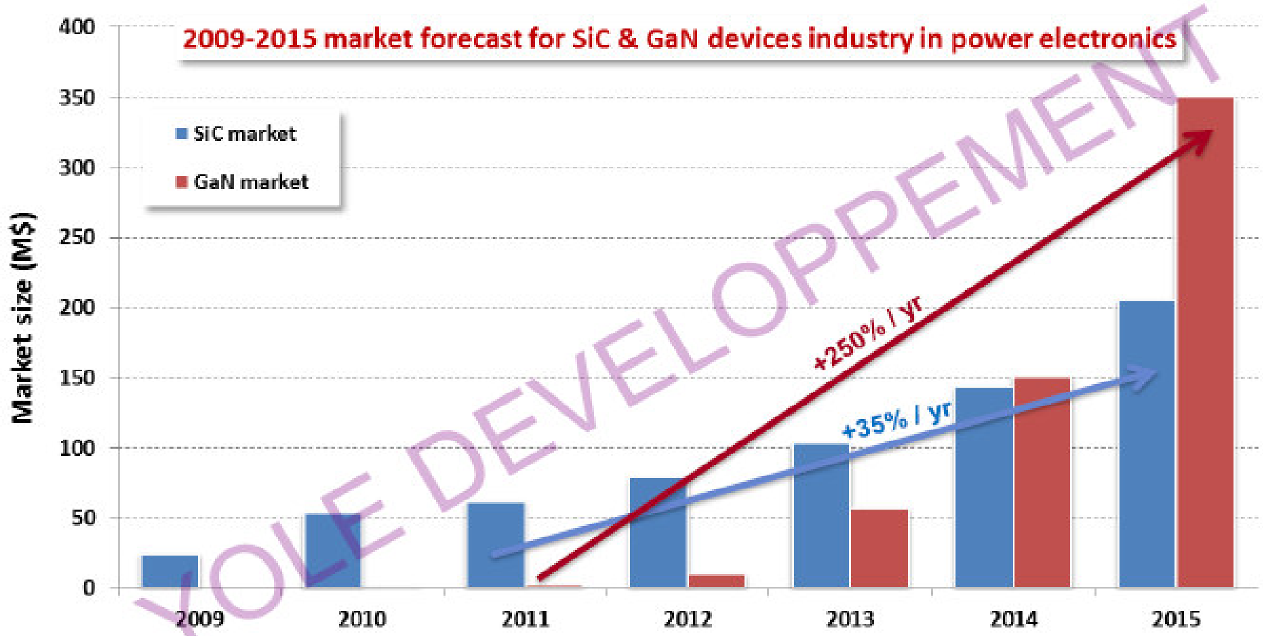
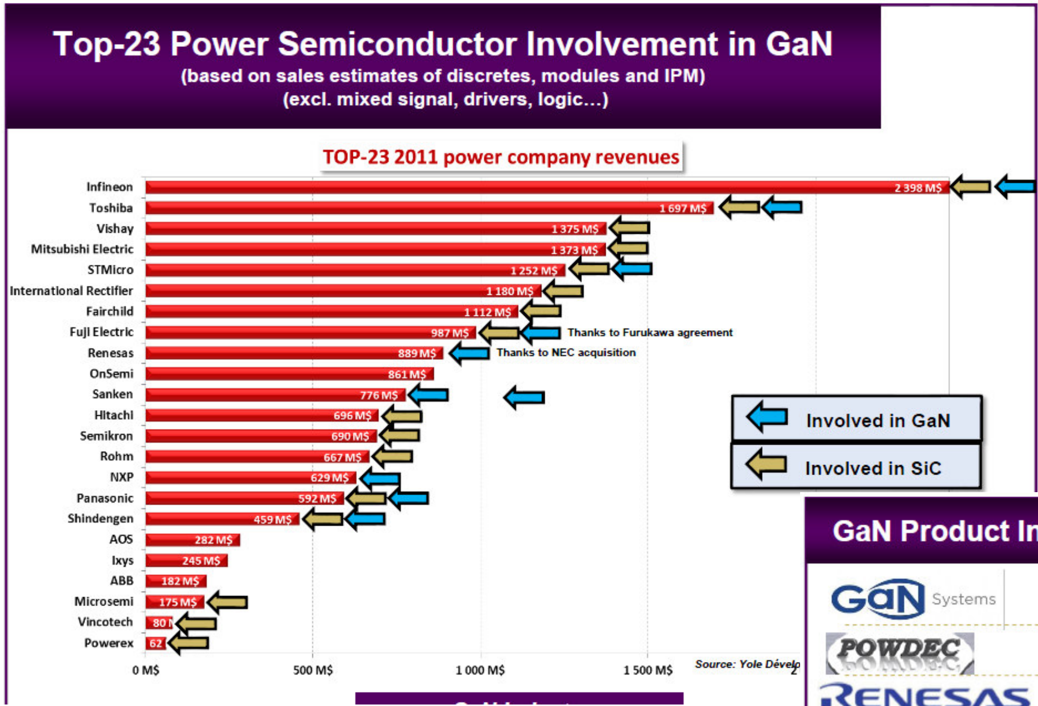
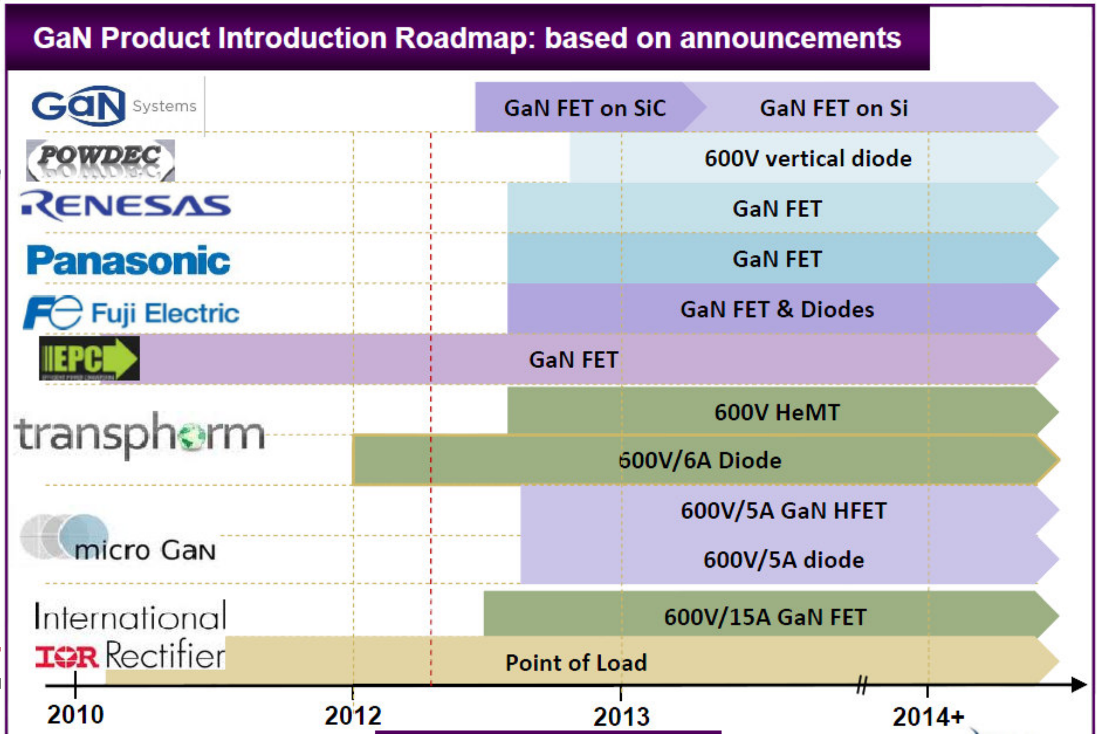
GaN & SiC device market projection comparison to 2015



But careful !! There is a limitation in the analysis as for some of the applications (EV/HEV, PV inverter, motor control or UPS), both technologies are competing. Thus, we cannot exclude part of the business to displace from one to another…

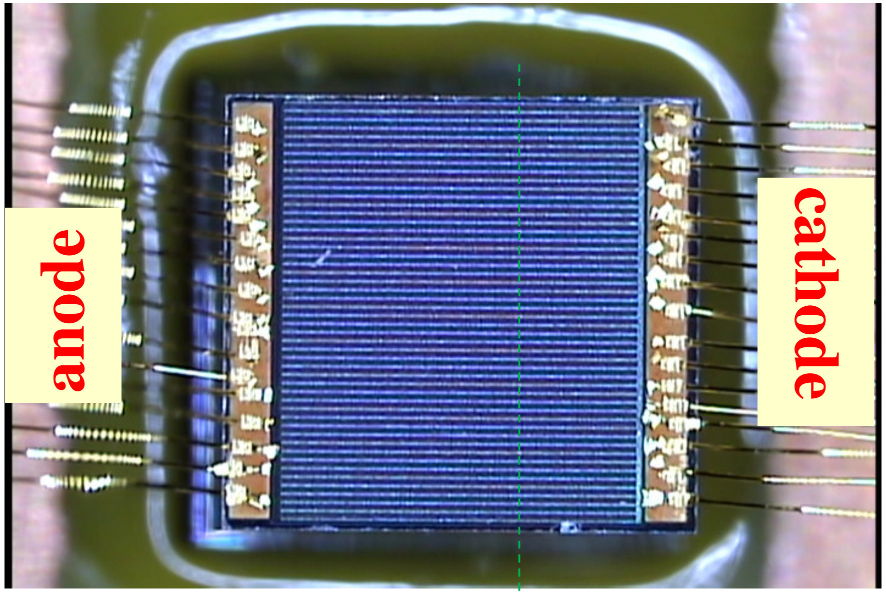
Competitors and Development Roadmap

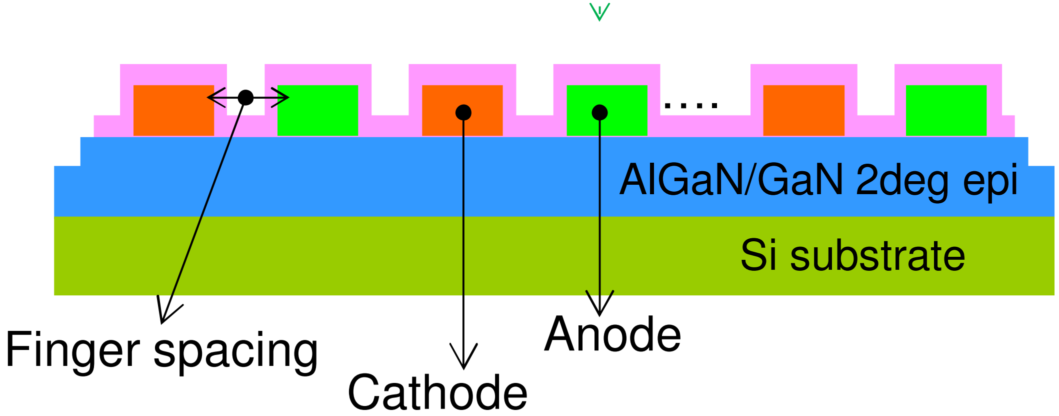




Source: CS Euro

Schottky Barrier Diode (SBD)





TLM
Rsh = 400~500 ohm/sq
ρc ~ 1E5 ohm-cm2
Rc ~ 1 ohm-mm

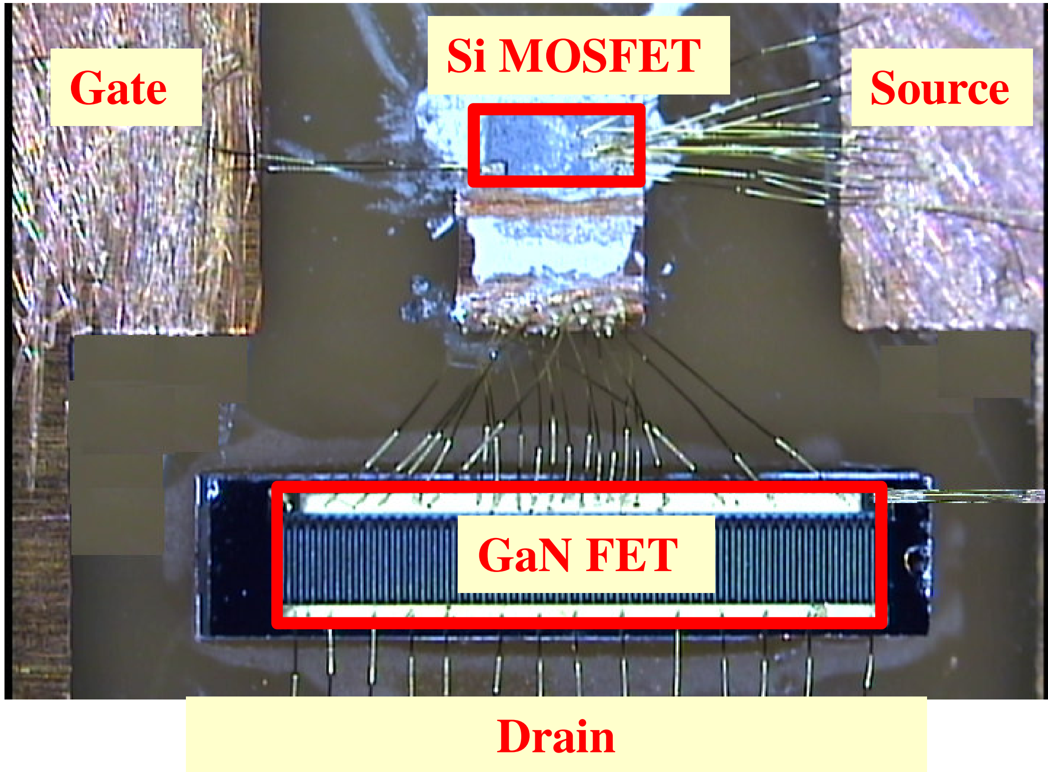
For IF=8A at VF ＜2V and VR=600V, we typically have

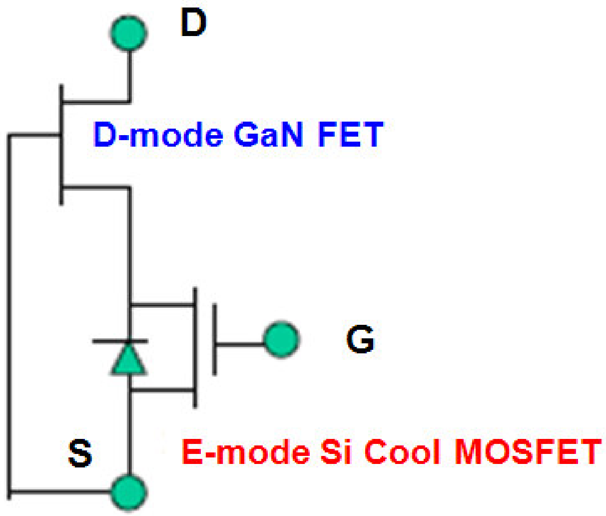
Total finger length= 50~150mm
Finger spacing= 15~30 um
Finger width ＞10um
Finger metal thickness ＞ 2um
…

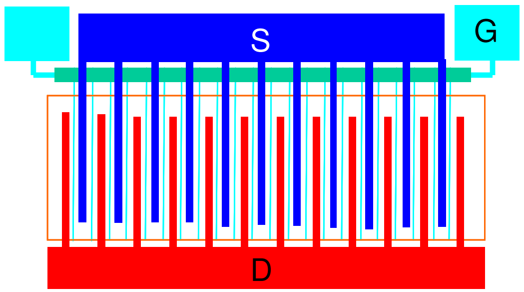
Schottky Barrier Diode (SBD)

Symbol	Parameter (25C unless otherwise noted)	GaN Schottky (T-company)	Si P-N	SiC Schottky	Unit
VF	Forward Voltage	1.3	2.1	1.45 / 1.88	V
IF	Forward Current	6	8	6	A
IR	Reverse Leakage Current (@600V)	30	＜100	＜50	uA
VBR	Breakdown voltage (@100uA)	800	650	950 / 770	V
VRRM	Repetitive Peak Reverse Voltage	600	600	600	V
IFSM	Non-repetitive Peak Surge Current	30	80	70	A
trr	Reverse Recovery Time	12	18	17 / 3.7	ns
Qrr	Reverse Recovery Charge	5	25	1.3 / 0.5	n C

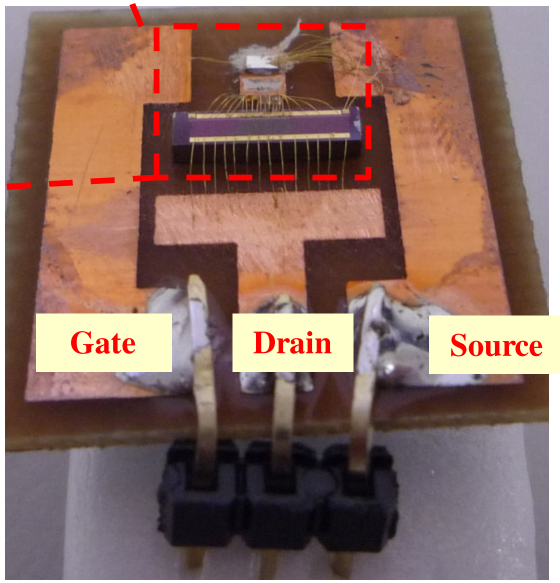
Hybrid E-mode FET (Cascode)







D-mode GaN FET



HUGA 廣鎵光電 HUGA OPTOTECH INC.

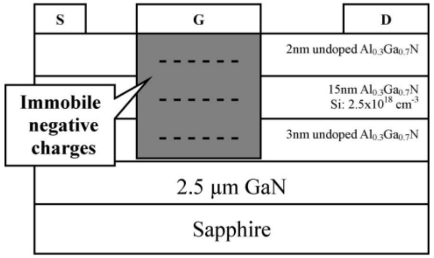
Hybrid E-mode FET (Cascode)

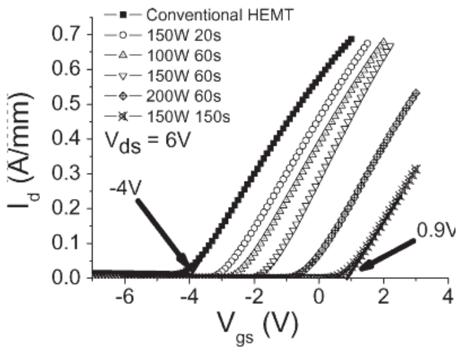
Symbol	Parameter (25C unless otherwise noted)	GaN Hybrid E-mode FET	Si MOSFET	Unit
VDSS	Drain-Source Voltage	600	600	V
ID	Continuous Drain Current	12	12	A
IDSS	Saturation Drain Current	100	35	nA
RDSON	Static Drain-Source On-Resistance	0.15	0.6	Ω
VBR	Breakdown voltage (@250uA)	＞900	660	V
VTH	Threshold Voltage	＞2V	4	V
Ciss	Cgs+Cgd	780	1660	
Qg	Total Gate Charge	7	40	n C
trr	Reverse Recovery Time	30	150	ns
Qrr	Reverse Recovery Charge	12.5	640	n C

HUGA 廣鎵光電 HUGA OPTOTECH INC.

E-mode FETs

Fluorine-plasma treatment





Lg= 1 *μm*, *Lsg* = 1 *μm*, *Lgd* = 2 *μm*.

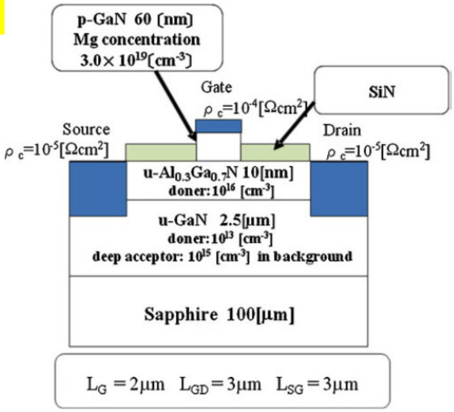
Y. Cai, Y. Zhou, K. M. Lau, and K. Chen, “Control of

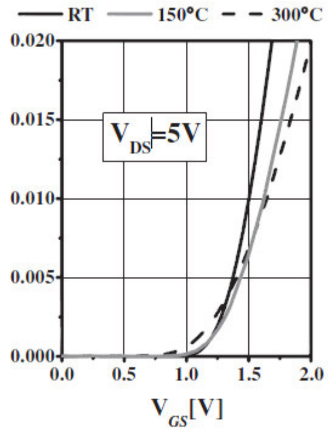
Threshold Voltage of AlGaN/GaN HEMTs by Fluoride-

Based Plasma Treatment From Depletion Mode to

Enhancement Mode,” TED, vol. 53, p. 2207, 2006

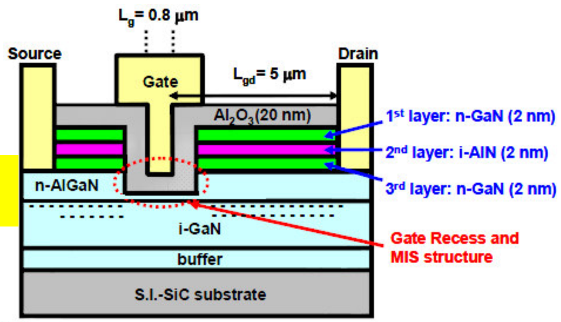
P-GaN capped JFET

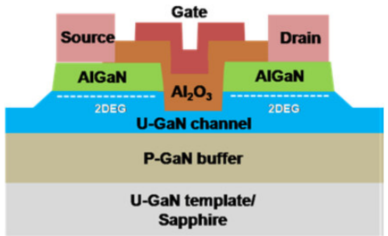


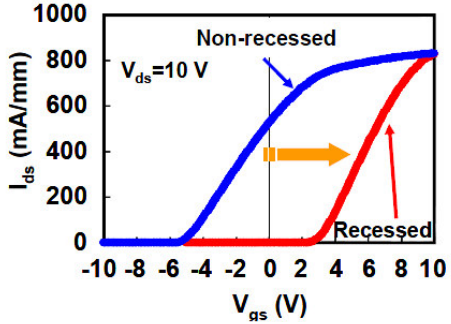


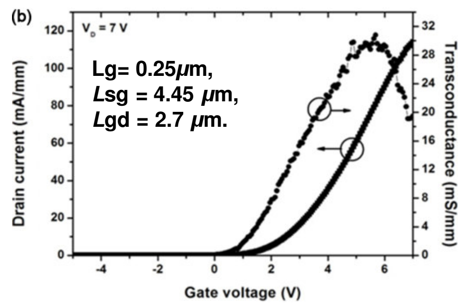
T. Sugiyama1, H..Amano1, D. Iida, M..Iwaya, S..Kamiyama, and I. Akasaki, “High-Temperature Operation of Normally Off-Mode AlGaN/GaN Heterostructure Field-Effect Transistors with p-GaN Gate,” JJAP, vol. 50, 01AD032011, 2011.

Recessed gate



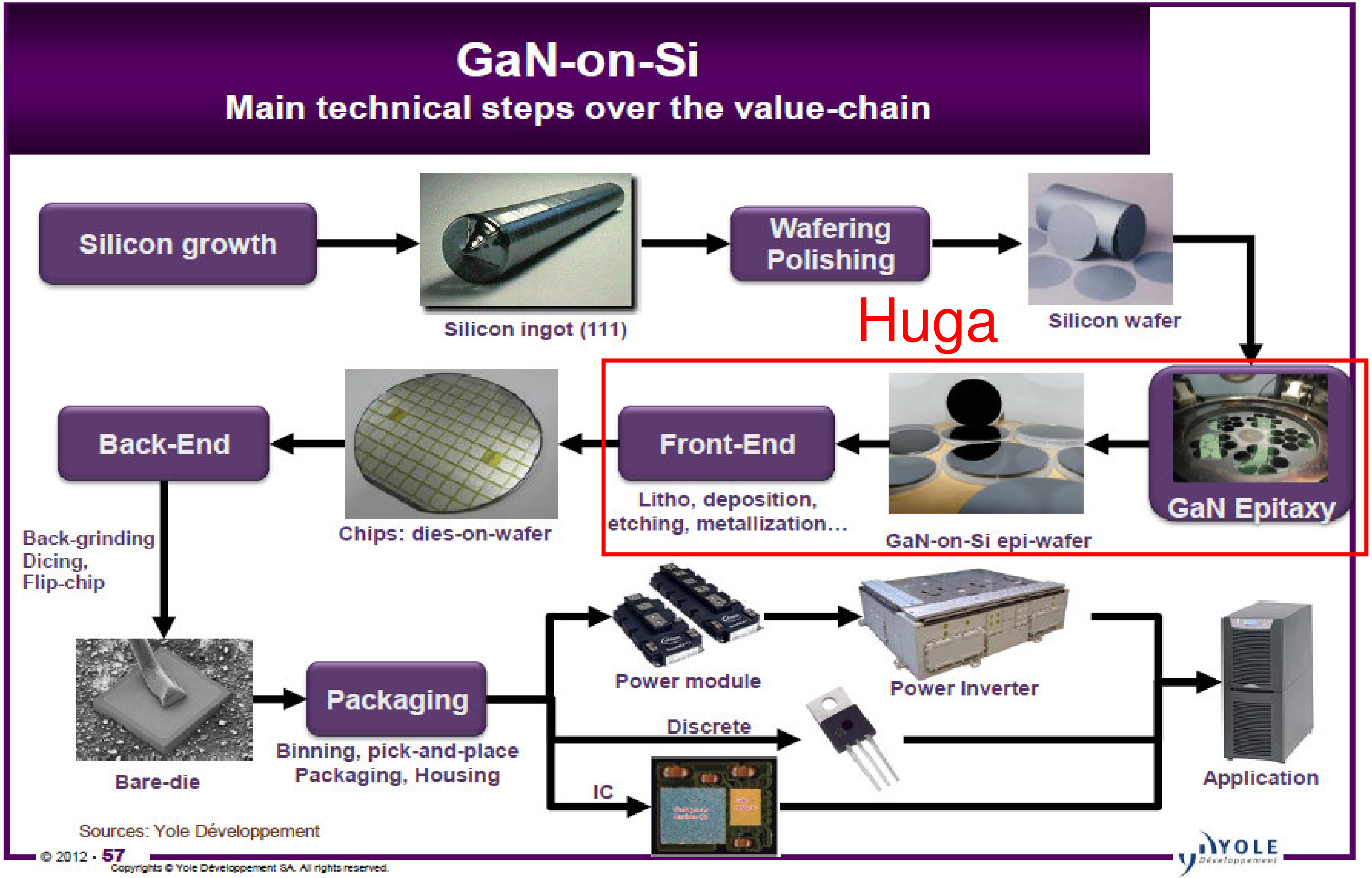






M.Kanamura, T. Ohki, T. Kikkawa, K. Imanishi, and N. Hara, “A Normally-Off GaN HEMT with Large Drain Current,” (Fujitsu)
D.-S. Kim, S.-N. Kim, K.-W. Kim, K.-S. Im, H.-S. Kang, E.-H. Kwak, J.-H. Lee, S-G. Lee, and J.-B. Ha,“High Performance in a Normally-off Al2O3/GaN MOSFET Based on an AlGaN/GaN Heterostructure with a p-GaN Buffer Layer,” (Samsung)

What Huga Do?


GaN-on-Si
Main technical steps over the value-chain
Silicon growth
Silicon ingot (111)
Wafering
Polishing
Silicon wafer
Huga
GaN Epitaxy
GaN-on-Si epi-wafer
Front-End
Litho, deposition,
etching, metallization…
Chips: dies-on-wafer
Back-End
Back-grinding
Dicing,
Flip-chip
Bare-die
Packaging
Binning, pick-and-place
Packaging, Housing
Power module
Power Inverter
Discrete
IC
Application
Sources: Yole Développement
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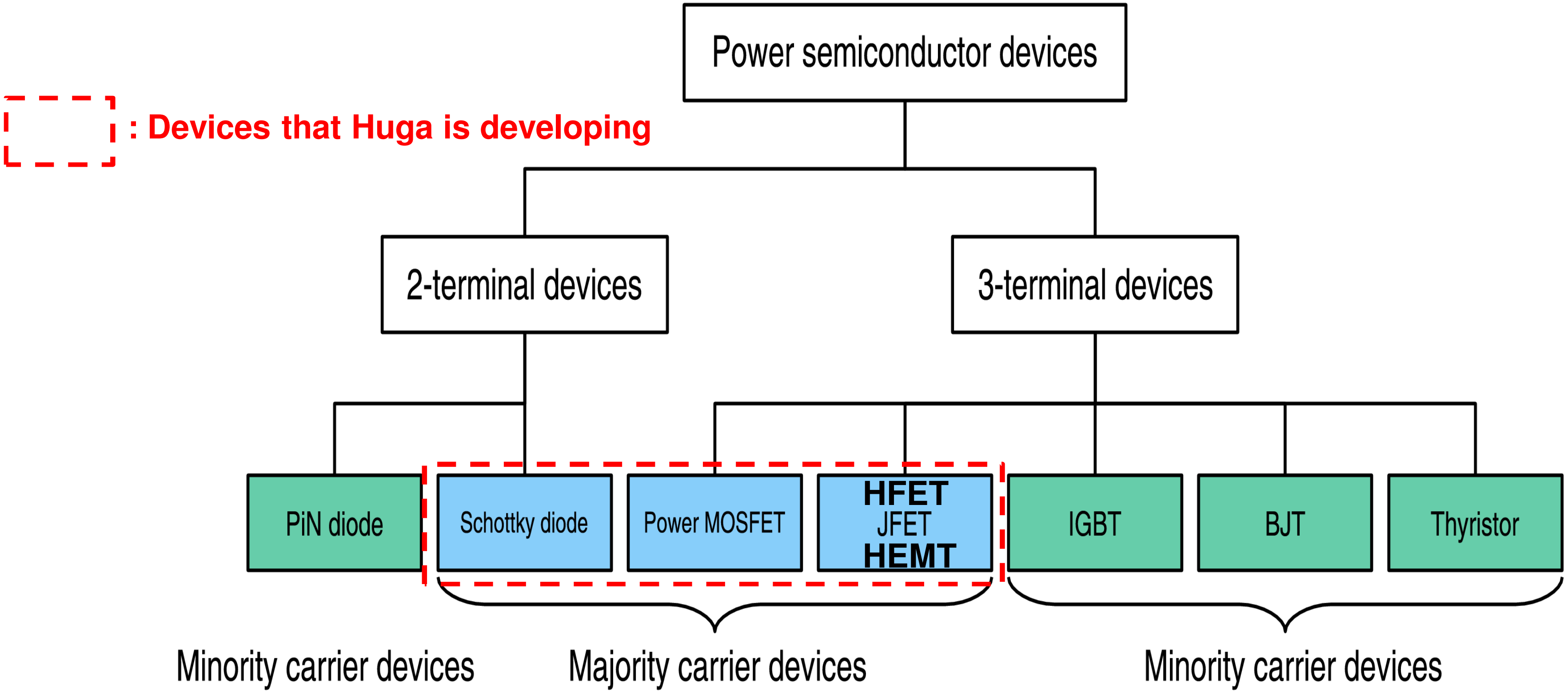
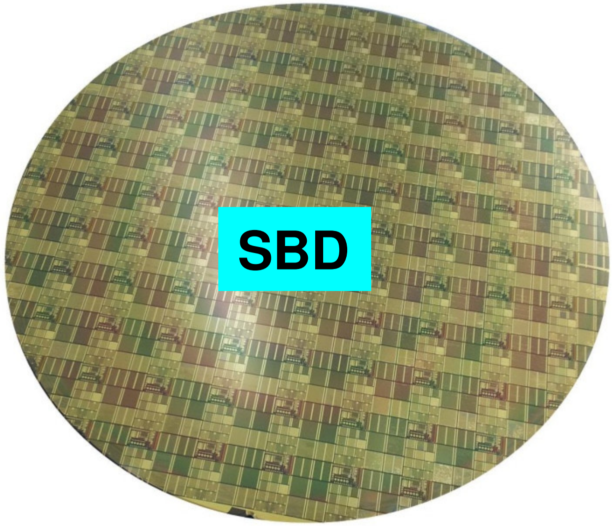
YOLE Développement

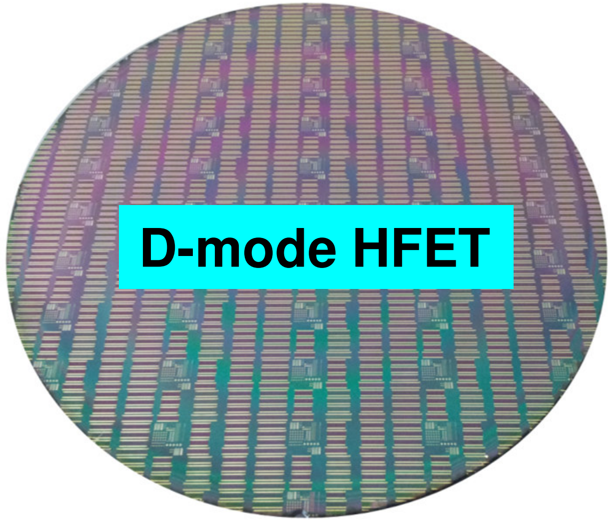
What Huga Do?

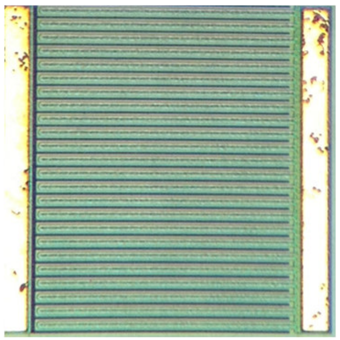


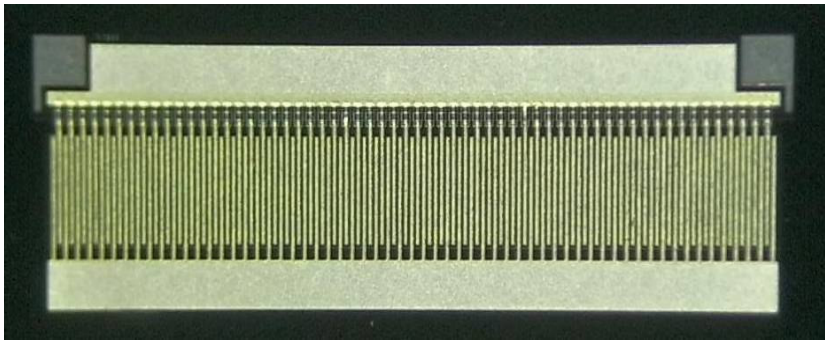
- Rectifying Devices (2-terminal devices)
  - Schottky Barrier Diodes
  - PIN Diodes
- Switching Devices (3-terminal devices)
  - Latching: Thyristors, GTOs, MGTs
  - Continuously controlled: BJTs, MOSFETs, IGBTs

Huga's 6" GaN-on-Si Device Wafer









I_F=8A (@ $V_F < 2V$)
V_R=600V

I_D=10~12A
V_D (off-state)=600V

Summary

- GaN is promising material for power device application. GaN-on-Si solution is an excellent option for balancing the requirement of performance and cost.
- Performance of GaN-on-Si power devices is similar to that of SiC power devices and much better than that of Si power devices. Plus, cost of GaN-on-Si power devices is in between.
- Though 600V GaN-on-Si power device products started appearing in the market recently, I believe it will take some time to have end users willing to widely apply them into various modules/systems.

Thank you !

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