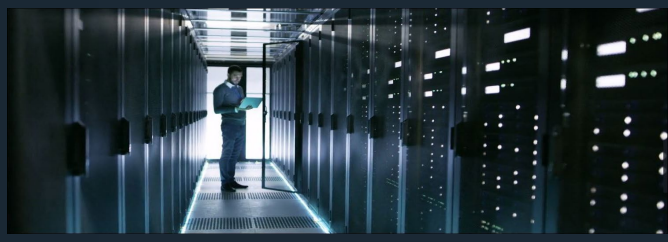
Tektronix®

Efficient Verification & Debugging for LPDDR5 Memory Interfaces



5G Is Coming – Can Your Testing Software Keep Up?

There's a lot we don't know regarding 5G. But we do know that it will be extremely fast and will take existing smartphones to the next level with higher resolutions, augmented/virtual reality and enhanced gaming experiences. LPDDR5 DRAM addresses the specifications of 5G by significantly increasing the data transfer and power efficiency compared to LPDDR4. Higher data transfer rates and faster signal speeds mean complex designs that push the boundaries of signal integrity and require higher performance measurements for compliance, debugging and validation.

The Tektronix LPDDR5 Transmitter Solution is an automated system-level test application that lets you quickly, efficiently and reliably validate and debug LPDDR5 designs to meet more than 50 electrical and timing measurements as defined in JEDEC.

View TekExpress DDR5 Tx Automation Solution for LPDDR5

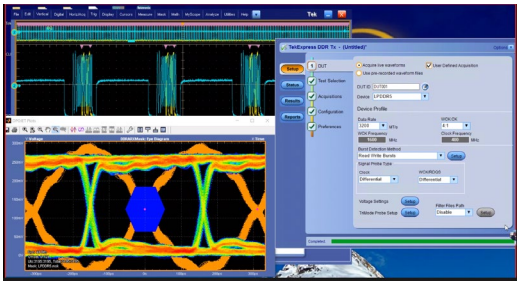
Accelerate Your Time to Market

While DRAM validation is an essential step in product development to ensure the quality of a design, it is also very time-consuming and cumbersome. One way to limit this challenge is to reduce manual testing as much as possible. Our LPDDR5 Transmitter Solution allows you automate LPDDR5 signal integrity testing and cut your total test time in half. This reduces the overall feedback and testing cycle and allows companies to bring their products to market faster.

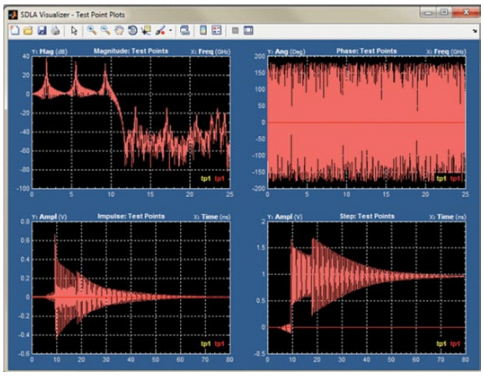
Debugging and Validation

Tektronix's LPDDR5 Transmitter Solution puts control back where it should be—with the user. User-defined acquisition mode allows you to run LPDDR5 JEDEC compliance measurements by customizing scope settings like sample rate, record length, bandwidth and more.

Read/Write burst separation has always been a major issue for the memory validation engineer. Often, at a system level, there is no way to control the data traffic on the DDR bus. With new and improved burst separation algorithms, the LPDDR5 Transmitter solution not only allows simultaneous read/write burst detection but also improves test time and accuracy.



SDLA

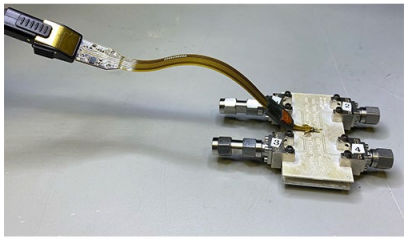


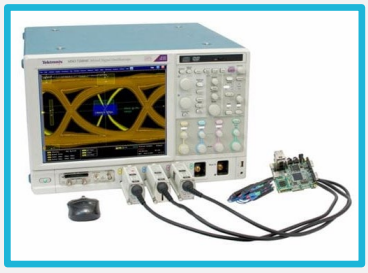
Validating s-parameters is often the primary concern when de-embedding LPDDR5 designs. With improved passivity checking, port assignments and plotting capabilities, not only does Serial Data Link Analysis (SDLA) enhance s-parameter file validation, it improves flexibility, saves time and increases confidence in the de-embedding process. Other debug software tools require you to complete the entire process to find results. Textronix's LPDDR5 Transmitter Solution lets you detect problems at an earlier stage, allowing you to debug and optimize your designs more efficiently. SDLA features can also be helpful for DFE analysis.

For more information check out our SDLA app note here.

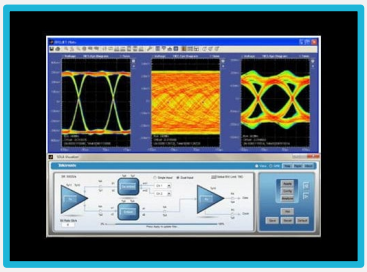
P7700 TriMode Probes

One of the power saving features of LPDDR5 DRAM is an option to change the three differential signals CK, WCK, and RDQS into single-ended signals when running at data rates at or below 1600 Mbps. Depending on the use case, this single ended mode will also need to be thoroughly tested along with the default differential mode. Measure differential and single ended signals using P7700 series TriMode probes. **New P77STFLRB** and **P77HTFLRB** solder-in tips improve signal access and reduce mechanical strain relief. This simplifies the probing setup to test the LPDDR5 DRAM Single Ended Mode.





LPDDR5 Electrical Verification and Debug

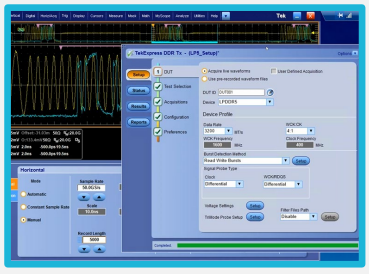


Serial Data Link Analysis Visualizer

P7700 Series TriMode Probes

DPO70000SX ATI Oscilloscope

MSO/DPO70000 Oscilloscope



TekExpress DDR Tx Automation Software