

## Method of Implementation for MIPI<sup>®</sup> C-PHY<sup>SM</sup> Receiver Conformance Tests

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## C-PHY Receiver Setup and Configuration

Required instruments and accessories

Part Number/Model	Description	Quantity
AWG70002A	25Gs/sec 2-Channel AWG	2
AWGSYNC01	AWG Sync Hub	1
MDC4500-4B	Combiner Box	1
P7380A/P7313	Z-Active <sup>™</sup> Differential Probe	3
MIPI CPHY/DPHY Termination Board	MIPI CPHY/DPHY Termination Board	1
174-5771-00	Phase Matched SMA Cable pairs [One Meter Green Cables]	2
	Real-time scope for Calibration. Bandwidth 6GHz or higher based	
DPO70000 series	on the operating symbol rate.	1

## Required software

Name	Description
	AWG based software for Signal
CPHYXpress	Generation
	Oscilloscope application for C-PHY
	clock recover and eye diagram
TekExpress C-PHY Tx Essentials	measurements
	Jitter, Noise and Eye Diagram
DPOJET Opt DJA	Analysis tool

## Test setups

## 1. Receiver Test Setup

Figure1 below shows the functional block diagram of the Rx test setup. This is the test setup is used for the all the measurements except noted otherwise.



Figure 1: Rx Test Setup - Functional Diagram

## 2. HS Signal Calibration Setup

Figure2 below shows the functional block diagram of the setup for HS signal calibration



Figure 2: HS Signal Calibration Setup - Functional Diagram

## 3. LP Signal Calibration Setup

Figure3 below shows the functional block diagram of the setup for LP signal calibration.



Figure 3: LP Signal Calibration Setup - Functional Diagram

## Configuring the Test Setup

The high level block diagram of the receiver test setup is shown below in Figure 4.



Figure 4: High-level Block Diagram - C-PHY Receiver test setup

Steps to configure the test setup

- 1. AWGs, Sync Hub and MDC Setup (Back panel connections)
- 2. Calibrate (de-skew) the AWG channels First time only
- 3. <u>Signal connection to the DUT</u>
- 4. Enable Master & Slave AWG

1. AWGs, Sync Hub and MDC Setup (Back panel connections)

The back panel connections of the setup are listed and shown in the schematic Figure 5.

- a) Connect USB B type AWG-A Port of MDC box to Host USB port of Master AWG using USB cable.
- b) Connect USB B type AWG-B Port of MDC box to Host USB port of Slave AWG using USB cable.
- c) Connect Clock-out from the Master AWG to the 'Clock-in from Master AWG' port of Sync hub using blue cable.
- d) Connect Clock-in from the Slave AWG to the 'Clock-out to AWG clock-in' port of Sync hub using blue cable.
- e) Connect Sync to AWG port slot 1 to Sync to Hub port of Master AWG using orange cables.
- f) Connect Sync to AWG port slot 2 to Sync to Hub port of Slave AWG using orange cables.



Figure 5: Back panel connection of AWGs, Sync Hub and MDC

## 2. Calibrate (de-skew) the AWG channels

# Note: This is required when you first set up the instruments or whenever you make any configuration change in the hardware setup only

This procedure aligns the channel 1 outputs of all connected and enabled instruments to within  $\pm 10$  ps of each other. You should run the de-skew process when you first set up the instruments, and whenever you make any configuration change, such as replacing an AWG, swapping an AWG within the same configuration, changing the de-skew cables, or changing the Master AWG.

## Prerequisites:

- All instruments are connected to the AWGSYNC01 (see section <u>Back panel connections</u>).
- All Slave AWG instruments have been enabled (from each Slave instrument and from the Master instrument).
- The de-skew calibration cables are connected as shown in the following diagram.



Figure 6: Connect the calibration de-skew cables (front panel)

 Use the supplied matched silver calibration cables to connect the Calibration ports on the front of the AWGSYNC01 to the same CH1+ or CH1– output on all AWG Master and Slave instruments. The order of the connections is important. Connect Calibration Port 1 to the CH1 output on the Master AWG instrument, connect Calibration Port 2 to the CH1 output on the Port 2 AWG Slave instrument, and so on. You can use CH1– for de-skew if you connect to the CH1– output on all instruments. The following diagram shows the calibration cables connected to the CH1+ outputs on all AWG instruments.

- 2. Allow all instruments to warm up for 20 minutes.
- 3. Enable the Slave AWG instruments (see Enable the Slave AWG instruments).
- 4. Configure the Master AWG (see Configure the Master AWG).
- Click Setup > De-skew Calibration on the Master AWG. An in-progress dialog is shown on all instruments while running the calibration. De-skew calibration takes approximately 20 to 30 minutes if using the Master AWG as the clock source, or about a minute if using an external clock source (see De-skew and clock source below).

Home	Setup	Wavefor	n Seq	uence l	Jtilities				•
Channe	1 💻	Clock		Trigger		Sync			
Enable Progress	Synchro	nization	Enable	Disable		AWG Typ	e: Mas	ter	
Calib	rating		-						
						Cancel	Conf	figuration	
Calibra	ation							?	
D	eskew C Adj	alibration ust	]	Dat Ter	te and T np:	ime: 6/14/ 34°C	2014 :	10:56:53 Aŀ∕	1

Figure 7: Deskew calibration settings of AWG

6. The Master AWG saves the deskew calibration settings at the completion of the calibration process, and displays the date, time, and instrument temperature of the most-recent successful calibration process.

## 3. Signal connections to the DUT

## a) AWG to MDC connections:

Using the blue cables and attenuators supplied along with MDC4500-4B, make the following connections from the AWG channel outputs to the Input ports of the MDC box.

From AWG		To MDC Box			
	Ch1+	Inputs from AWG_A Ch1	Ch+		
Master AWG	Ch1-	Inputs from AWG_A Ch1	Ch-		
	Ch2+	Inputs from AWG_A <b>Ch2</b>	Ch+		
	Ch2-	Inputs from AWG_A Ch2	Ch-		
Slave AWG	Ch1+	Inputs from <b>AWG_B</b> Ch1	Ch+		
	Ch1-	Inputs from AWG_B Ch1	Ch-		

## b) MDC to DUT connections:

Using SMA cables connect the outputs from the MDC box to the Rx DUT as listed in table below

From M	To Rx DUT	
A Ch1 Outputs	D+	Line A of Rx
A Ch2 Outputs	D+	Line B of Rx
B Ch1 Outputs	D+	Line C of Rx

Note: If there is a need to increase rise time of signal, then there is a provision to include Rise time filter additionally in signal path between MDC and C-PHY Receiver. Typically, it starts with 100 ps. [Part Number PSPL 5915 Opt 100ps – 100ps Filter (SMA Male to SMA Male)]

## 4. Enable Master & Slave AWG

#### a) Enable the Slave AWG instrument

Prerequisite: All instruments are connected to the AWGSYNC01. (See <u>AWGs, Sync Hub and MDC</u> <u>Setup (Back panel connections)</u> section)

- 1. Open the UI of a Slave AWG instrument.
- 2. Click the Setup tab.
- 3. Click the Sync tab.
- 4. Select **Enable** to make the AWG accessible for synchronization with the Master AWG.

#### b) Configure the Master AWG

Prerequisite: Connected Slave AWG instruments have been enabled for synchronization. (See section *Enable the Slave AWG instruments*.)

- 1. Open the UI of the Master AWG.
- 2. Click the **Setup** tab.
- 3. Click the Sync tab.
- 4. Click Enable.



Figure 8: Sync configuration settings of AWG

5. Click Change Configuration. Select the slave ports to enable.

쩆 System Configuration 🧧	x
Select AWGs for the Sync Hub.	
Port 1 (Master AWG)	
Port 2	
Port 3	
Port 4	
Enable slave AWGs before configuration.	
Any time a configuration change is made a deskew calibration is recommended	d.
OK	

Figure 9: Sync configuration settings of AWG to configure Master and Slave AWG

6. Click **OK**. The Master AWG instrument connects to the selected Slave AWG instruments and displays the connections on the Sync tab screen. If the Master AWG cannot connect to a Slave AWG, the Master shows an error message after a minute or so.

## Signal Calibration Procedure

## Voltage (VIH/VIL) Calibration Procedure

This procedure enables the outputs of all channel of instruments to be within  $\pm 5$  % of expected value.



**Figure: C-PHY Signaling Levels** 

Plug-in: C	PHYXpress 🔻			📩 Compile			
Signal Mod	e: High Speed 👻						
High Spee	d High Speed Jitter	High Speed Burst Lo	w Power Low Powe	r Noise High Speed	Batch Mode	Preferences	Comp
Base Pat	ttern						
Pattern	PRBS9	_СРНҮ 🔻			) 📻 🛯	Repeat to a 1	L6 bit b
Previous	Wire State +x	•					
PRBS_CF	PHY Seed						
	0111	10001	0 0 1 1 0	10			
Q18Q17	'Q16	— 0x789A ——		— q1			
Note: Se	ed is applicable only	for PRBS_CPHY Pattern	types.				
Symbol R	ate 1.5 GS/s	Rise/Fall time(0	-100%) OUI	= 0 s			
← Line Lev	els						
	High	Low	Mid			-	
Line A	400 mV	0 V	200 mV	🔄 🛛 🖉 Use Line A leve	ls for Line B a	nd Line C  ?	
Line B	400 mV	0 V	200 mV				
Line C	400 mV	0 V					

Figure 10: CPHYXpress High Speed configuration tab

Steps to calibrate high and low voltage level

- 1. Create a C-PHY signal using a test pattern, using nominal High and Low voltage levels.
- 2. Measure the VIH/VIL using scope Max and Min measurements as shown in the screen shot below.
- 3. Modify VIH/VIL, till the desired level of voltages are measured on the scope



Figure 11: VIH/VIL measurement

## Batch Mode or on the fly differential and common mode voltage level control

Alternatively user can adjust or sweep differential and common mode swing by using the following controls on each of the channel of the AWG as shown in the screen shot below

- 1) Common mode level by setting the Offset control
- 2) Differntail level by setting Amplitude control

With this approach the voltages can will be varied on the fly with no need of generating additional waveforms.

Home Setup Waveform Plug-in Sequence Capture/Playback Utilities							
Channel 1 💻 Char	nnel 2 💻 Clock Trigger	Sync	]				
Channel 1	DC Amplified 🔻						
Amplitude	500 mVpp		Marker 1 🗖	Marker 2			
Offset	0 V						
Resolution (bits)	10 🗸		0 V	0 V			
	Couple settings (CH1, CH2)						
	Output Options Adjust Sk	œw					

Figure 12: AWG screen shot to show how to change offset/amplitude

## Jitter/Timing Calibration

The procedure for calibration jitter is cover in Test 2.3.3

## Correct for Amplitude non-linearity using Correction (\*.corr) file *Note: Recommended for higher operating data rate*

While testing a Device under test, you need to make sure the test equipment generating the signals is of better quality than the Device under Test. The signal generators, Arbitrary Waveform Generators (AWGs) require the generation of waveforms with flat amplitude and linear phase response in the band of interest. This means that the influence of the AWGs and the cables on the signals which could distort the signals should be de-embedded from the signals before sending it to the DUT. For example, of signal trace is running from AWG to DUT thorough MDC, the MDC channel effect also will be in consideration while de-embedding channel effect of signal trace from AWG to DUT.

For a detailed procedure to create a correction file, refer to Help Document of the *Generic Precompensation* plug-in application. Correction file can be applied to any waveform in the AWG waveform list. By default, correction file feature is disabled.

To apply correction, enable "Apply correction file" in the Compile Settings tab. The slave correction file controls will be enabled only if the slave is enabled on the 'Compile Settings' tab. User can select correction file for each channel using the browse button. The correction file will be applied only for those channel waveforms, which are enabled in the application.

Plug-in: CPHYXpre	255	•				ř.	Compile			
Signal Mode: Hig	gh Speed	•								
High Speed High	Speed Jitter	High Speed Burst	Low Power	Low Power Noise	High Speed Ba	atch Mode	Preferences	Compile Settings	Log View	
Sample Rate										
🧿 Auto										
O Manual										
Samples per UI		Samp	le Rate 24 0							
AWG Amplitude	and Offset co	ntrol								
🧿 Auto (Recom	imended) 🔿	Manual O	ffset 0							
		A	mplitude 4							
🛛 🗹 Apply Correc	ction File									
🛃 Master Ch1 🏾	C:\Users\Publ	lic\Tektronix\CPHY	Xpress\DataFi	iles\Example_CPHY_	CH1_25G.corr		💋 Use Master	Ch1 correction file	to all channels	
🗹 Master Ch2	C:\Users\Pub	lic\Tektronix\CPHY	Xpress\DataFi	iles\Example_CPHY_	CH1_25G.corr		Apply Gauss	sian Filter		
🗹 Slave Ch1	C:\Users\Publ	lic\Tektronix\CPHY	Xpress\DataFi	iles\Example_CPHY_	CH1_25G.corr		Bandwidt	th 12 GHz		
🗹 Slave Ch2	C:\Users\Publ	lic\Tektronix\CPHY	Xpress\DataFi	iles\Example_CPHY_	CH1_25G.corr		Remove cor	rrections for Sin(x)/>	distortions from correction file	

Figure: Correction file configuration using preference tab

## References

- [1] Specification for C-PHY<sup>SM</sup>, Version 1.1, 07 October 2014
- [2] DRAFT Conformance Test Suite for C-PHY<sup>SM</sup> v1.0 and v1.1, Version 1.0 Revision 01, 29 February 2016
- [3] Specification for C-PHY<sup>SM</sup>, Version 1.0, 05 August 2014
- [4] Conformance Test Suite for C-PHY<sup>SM</sup> v1.0, Version 1.0, 12 February 2016

## GROUP 1: LP-RX VOLTAGE AND TIMING REQUIREMENTS

## Test/Calibration Setup

If any of the parameters of the LP signal synthesized needs calibration, then the setup with termination board is to be employed. See section LP Signal Calibration Setup.

## Test 2.1.1 – LP-RX Logic 1 Input Voltage (V<sub>IH</sub>)

### Discussion

C-PHY Specification defines the minimum Logic 1 input voltage ( $V_{IH}$ ) as 740 mV. This test verifies if the DUT can detect logic level at least at this voltage specified.

Table 28 LP Receiver DC specifications {copy of D-PHY Table 22}							
Parameter Description Min Nom Max Units Notes						Notes	
L VIH	Logic 1 input voltage	740	I L		l m∨		

#### Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: Low Power
- Low Power: Base Pattern: ULPS or based on the DUT
- Low Power: Symbol rate = 20MHz
- ➢ Low Power: Line Level − High=1.2 V, Low = 0V.

Signal Mode: Low Power 🔻				
High Speed High Speed Jitter Hig	gh Speed Burst Low Powe	r Low Power Noise	High Speed Batch Mode	Preferences Compile Settings
∠ Base pattern				
Pattern ULPS 🔻				
Include LP content in Low Powe	er - High Speed (LP-HS) Sig	nal Mode		
Symbol		Rise/Fall		
Symbol Rate 20 MHz	TLPX 50 ns	Rise/Fall time (15%	6-85%) 0.1 UI	= 5 ns
<ul> <li>Line Levels (High Impedance)</li> </ul>				
High	Low			
Line A 1.2 V C	) V 🛛 🗹 Use	Line A levels for Line	B and Line C ?	
Line B 1.2 V 0	v			
Line C 1.2 V 0	) V			
LP-HS Entry/Exit timing (Applicab	le in LP-HS Signal mode)			
Start LP-111 duration 2	LP Sym	bols = 100 ns		
LP-000 duration(t3_PREPARE)	LP Sym	bols = 50 ns		
Enable THS_Exit				
End LP-111 duration 2	LP Sym	bols = 100 ns		

Figure: 2.2.1(a) Low Power Tab configurations

## Measurement details

•

The following measurements on DPOJET can be used to verify VIH and VIL respectively on all line A,B and C - 1) Ampl->High and 2) Ampl->Low.

C1 200m	7 Offset:438mV 50Ω №	12.50			C1 7 528mV	Stopped 1 acqs Man Dec	Single Seq RL:10.0k
Jitter, No	ise and Eye Diagram Ana	lysis Tools	CH1	Bit Rate : 10 Pattern Len;	0.000Mb/s gth:43UI View De	Options tails <b>T</b> Exp	and Clear X
Configure	Description High1, Ch1 Low1, Ch1 High-Low1, Ch1	Mean         Std Dev           1.0144V         80.597m           -40.361mV         81.507m           1.0642V         6.1807m	Max V 1.1467V V 79.750mV V 1.0736V	Min 865.00mV -195.00mV 1.0524V	p-p         Populatio           201.75mV         108           274.75mV         48           21.258mV         33	n Max-cc Min-cc 191.53mV -17.29 26.839mV -274.79 17.548mV -20.64	5 5

Fig: 2.1.1(b) LP-High and low voltage of Logic 1

## Test Procedure

- 1. Generate a LP waveform with signal parameters listed in the above section.
- 2. Transmit the test sequence to the DUT and Verify via any valid observable that the DUT received the data without errors.
- 3. Decrease the LP Line level: high for all the lines by say 50 mV.
- 4. Repeat steps 1, 2 & 3 till the observable shows an error.
- At this point note record the highest value of Line level: High at which the DUT consistently received the test sequence without errors. This represent the DUT's LP-RX Logic-1 Detection Threshold, V<sub>IH</sub>.

## Observable Results

Verify the notes VIH is = < 740 mV for all lines A, B and C.

## Test 2.1.2 – LP-RX Logic O Input Voltage, Non-ULP State (VIL)

# [This test is similar to Test 2.1.1 – LP-RX Logic 1 Input Voltage (VIH). In this test Logic 0 input threshold conformance is checked for]

### Discussion

C-PHY Specification defines the maximum Logic 0 input voltage ( $V_{IL}$ ) as 550 mV. This test verifies if the DUT can detect logic level at least at this voltage specified.

Parameter	Description	Min	Nom	Max	Units	Notes
VIH	Logic 1 input voltage	740			m٧	!   L!
L VIL	Logic 0 input voltage, not in ULP State			550 ¦	m٧	 L
VIL-ULPS	Logic 0 input voltage, ULP State		I I I I	300 ¦	m٧	

### Signal parameters

Refer to Test 2.1.1.

### Measurement details

Refer to Test 2.1.1.

### Test Procedure

[The test procedure is similar to Test 2.1.1]

- 1. Generate a LP\_HS waveform with signal parameters listed in the above section.
- 2. Transmit the test sequence to the DUT and Verify via any valid observable that the DUT received the data without errors
- 3. Increase the LP Line level: Low for all the lines by say 50 mV
- 4. Repeat steps 1,2 & 3 till the observable shows an error.
- 5. At this point note record the highest value of Line level: High at which the DUT consistently received the test sequence without errors. This represent the DUT's LP-RX Logic-1 Detection Threshold, V<sub>IL</sub>

## Observable Results

Verify that noted  $V_{IL}$  is => 550 mV.

## Test 2.1.3 – LP-RX Input Hysteresis (V<sub>HYST</sub>)

## Discussion

C-PHY includes a specification for  $V_{HYST}$ , or Input Hysteresis to check for the noise sensitivity of the LP receiver. The CTS describes in detail two methods to test for this specification – (1) Static Method and (2) Dynamic Method using additive noise.

Static method is pictorially represented by the graphic below



## Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: Low Power
- Low Power: Base Pattern: ULPS or based on the DUT
- Low Power: Symbol rate = 20MHz
- ➢ Low Power: Line Level − High=1.2 V, Low = 0V.
- Low Power Noise: Sine Noise Enabled, Amplitude =0V, Frequency = 450MHz. [Dynamic Method]

Signal Mode: Low Powe	r 🕶								
High Speed High Speed	litter High Speed Burst L	ow Power Low Power Noise	e High Speed Batch Mode	Preferences Compile Settings					
Base pattern       Pattern       ULPS       Include LP content in Low Power - High Speed (LP-HS) Signal Mode									
Symbol									
Symbol Rate 20 MHz	TLPX 50 ns	s Rise/Fall time (15	i%-85%) 0.1 UI	= 5 ns					
Line Levels (High Imped	ancel								
High	Low								
Line A 1.2 V	0 V	🛛 🗹 Use Line A levels for Lin	e B and Line C ?						
Line B 1.2 V	0 V	]							
Line C 1.2 V	0 V								
LP-HS Entry/Exit timing	(Applicable in LP-HS Signal	mode)							
Start LP-111 duration	2	LP Symbols = 100 ns							
LP-000 duration(t3_PREF	ARE) 1	LP Symbols = 50 ns							
Enable THS_Exit									
End LP-111 duration		LP Symbols = 100 ns							

High Speed	High Speed Jitter	High Speed Burst	Low Power	Low Power Noise	High Speed Batch I	Mode Prefer	ences Com	npile Settings
Impairmer	nts							
🗹 Sine N	oise Amplitude(Pe	ak) 100 mV	Freque	ency 450 MHz	Apply to	o 🗹 Line A	🗹 Line B	🛃 Line C
🗌 eSpike	Area	200 Vps	Durati	on 4 ns	Apply to	🗹 Line A	🗹 Line B	🗹 Line C
<b>TMin</b>	20 ns							

Figure: 2.1.3(a) Low power noise configurations

## Test Procedure

## (Option 1: Static Method):

- 1. Generate a LP waveform with signal parameters listed in the above section.
- 2. Slowly increase the Low level on CPHYXpress application to the point where the DUT's reported internal LP logic states change from LP-0 to LP-1 for VA, VB, and VC, and record the voltages as V1(VA), V1(VB), and V1(VC).
- 3. Continue to increase low level to approximately 100 mV beyond V1. Then begin slowly decreasing the High level, while still monitoring the reported internal LP logic state (which should still be reported as LP-1 for VA, VB, and VC).
- 4. Continue decreasing High level until the reported internal LP logic states for VA, VB, and VC change from LP-1 to LP-0. Record these voltages as V2(VA), V2(VB) and V2(VC).
- 5. Compute the  $V_{IH}$  hysteresis for the VA line as  $V_{HYST-VIH}(VA) = V1(VA) V2(VA)$ .
- 6. Compute the  $V_{IH}$  hysteresis for the VB line as  $V_{HYST-VIH}(VB) = V1(VB) V2(VB)$ .
- 7. Compute the  $V_{IH}$  hysteresis for the VC line as  $V_{HYST-VIH}(VC) = V1(VC) V2(VC)$ .
- Repeat the above procedure a second time (but starting from a nominal LP-1 level of 1200mV, and working downward) to measure the VIL hysteresis for VA, VB, and VC, i.e., V<sub>HYST-VIL</sub>(VA), V<sub>HYST-VIL</sub>(VB), and V<sub>HYST-VIL</sub>(VC). (Note however in this case VHYST will be computed as |V1 V2|.)

## (Option 2: Dynamic Method)

- 1. Generate a LP waveform with signal parameters listed in the above section. Set the High and Low levels that were measured in Tests 2.1.1 and 2.1.2, respectively
- 2. Verify via any valid observable that the DUT received the data without errors.
- 3. With the additive noise source disabled, transmit the test sequence the DUT, and verify via any valid observable that the DUT received the data without errors.
- Repeat the previous step, but with the additive noise source enabled for the V<sub>A</sub> line, using a noise voltage of approximately 5mVpk. Again, verify via any valid observable that the DUT received the data without errors.
- 5. Repeat the previous step multiple times, slowly increasing the additive noise voltage in 3-5 mV steps, until the point is reached where the DUT begins to report errors in the received test sequence.
- 6. Record  $V_{HYST-VIH}(V_A)$  and  $V_{HYST-VIL}(V_A)$  as the maximum additive noise voltage where the test sequence was consistently received without error.
- 7. Repeat the above procedure for the  $V_B$  line to determine  $V_{HYST-VIH}(V_B)$  and  $V_{HYST-VIL}(V_B)$ .
- 8. Repeat the above procedure for the  $V_c$  line to determine  $V_{HYST-VIH}(V_c)$  and  $V_{HYST-VIL}(V_c)$ .

## Observable Results

Verify that all the following determined values is greater than or equal to 25mV.

- 1) V<sub>HYST-VIH</sub>(V<sub>A</sub>)
- 2) V<sub>HYST-VIH</sub>(V<sub>B</sub>)
- 3) V<sub>HYST-VIH</sub>(V<sub>C</sub>)
- 4) V<sub>HYST-VIL</sub>(V<sub>A</sub>)
- 5) V<sub>HYST-VIL</sub>(V<sub>B</sub>)
- 6) V<sub>HYST-VIL</sub>(V<sub>C</sub>)

## Test 2.1.4 – LP-RX Minimum Pulse Width Response (T<sub>MIN-RX</sub>)

#### Discussion

The make the LP receiver robust, one of the parameter defined is the Minimum pulse width response  $T_{MIN-RX}(20 \text{ nsec})$ , which defines the minimum-duration LP pulse width that should still be detected as a valid LP state by an LP receiver.

#### Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: Low Power
- > Low Power: Base Pattern: ULPS or based on the DUT
- Low Power: Symbol rate = 20MHz
- ▶ Low Power: Line Level High=1.0 V, Low = 0V.
- Low Power Noise: TMIN = 30 nsec

Signal Mode: Low Power 🔻								
High Speed High Speed Jitter	High Speed Burst	Low Power	Low Power Noise	High Speed Batch Mode	Preferences	Compile Settings		
Base pattern								
Pattern ULPS 🔻								
Include LP content in Low Power - High Speed (LP-HS) Signal Mode								
Symbol		( I	Rise/Fall					
Symbol Rate 20 MHz	TLPX 50 n	is F	Rise/Fall time (15%	-85%) 0.1 UI	= 5 ns			
Line Levels (High Impedance)								
High	Low	-		_				
Line A 1V	0 V	🛛 🗹 Use Lin	e A levels for Line	B and Line C ?				
Line B 1V	0 V							
Line C 1 V	0 V							
ID US Entry/Evit timing (Appli	rable in LD US Signal	mode)						
LP-HS Entry/Exit unling (Applie		mode)						
Start LP-111 duration	2	LP Symbol	s = 100 ns					
LP-000 duration(t3_PREPARE)	1	LP Symbol	s = 50 ns					
Enable THS_Exit								
End LP-111 duration		LP Symbol	s = 100 ns					

Figure: 2.1.4(a)	Low power	Tab settings
------------------	-----------	--------------

Signal Mode: Low Power 💌				
High Speed High Speed Jitter Hig	h Speed Burst Low	Power Low Power No	ise High Speed Batch Mode	Preferences Compile Settings
/ Impairments				
Sine Noise Amplitude(Peak)	100 mV	Frequency 450 M	Hz Apply to 🔽	Line A 🕑 Line B 🕑 Line C
eSpike Area	200 Vps	Duration 2 ns	Apply to 💟	Line A 🛛 Line B 🗹 Line C
🗹 TMin 🛛 30 ns				



### Measurement details

If you need to verify the Minimum pulse width of the waveforms, employ the following measurement and settings to measure TMIN on a LP waveform.

- DPOJET Measurement: Period;
- Configuration: Edges->Clock, Clock-Edge-> Both
- Minimum of the Period Measurement represent TMIN\_Rx

Select					0	0	View De	tails	Expand	Recalc
	Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc	(CT)
Configure	🛛 🗉 Period1, Ch1	50.000ns	30.066ns	80.423ns	19.313ns	61.110ns	3198	61.110ns	-60.866ns	Finals
oningure					Ŏ	-0				Single
_										
Results										Run
Results										Run
Results										Run CO Show Plots
Results Plots										Run CO Show Plots
Results Plots										Run C Show Plot Illin

Figure: 2.1.4(b) measurement result for TMIN\_Rx of 20 nsec

#### *Test Procedure*

- 1. Generate a LP waveform with signal parameters listed in the above section.
- 2. Transmit the test sequence to the DUT and verify via any valid observable that the DUT received the data without errors.
- 3. Decrease the Low Power Noise: TMIN by say 1ns.
- 4. Repeat steps 1, 2 & 3 till the observable shows an error.
- 5. At this point note record the smallest value of TMIN at which the DUT consistently received the test sequence without errors. This represent the DUT's TMIN\_Rx minimum pulse width response.

#### *Observable Results*

Verify the recoded TMIN\_Rx is  $\leq 20$  nsec.

## Test 2.1.5 – LP-RX Input Pulse Rejection (eSPIKE)

### Discussion

To make the LP Rx robust in the presence short-term glitches  $e_{SPIKE}$  is included in the specification. In this test we shall verify if the LP receiver rejects short-term signal glitches which are smaller than the specified conformance limit of 300Vps.

Parameter	Description	Min	Nom	Мах	Units
espike	Input pulse rejection			300	V∙ps
T <sub>MIN-RX</sub>	Minimum pulse width response	20			ns
VINT	Peak interference amplitude			200	m∨
fint	Interference frequency	450			MHz



#### Signal parameters

The relevant parameters of the CPHYXpress application are listed below, and also shown in the screenshot below

- Signal Mode: Low Power
- Low Power: Symbol rate = 20MHz
- ▶ Low Power: Line Level High=1.0 V, Low = 0V.
- Low Power: Pattern: Based on the DUT.
- Low Power Noise: eSpike Area=300Vps, Duration = 2ns

Signal Mode: Low Power 🔻						
High Speed High Speed Jitter Hig	h Speed Burst Low	Power Low P	ower Noise	High Speed Batch Mod	e Preferences	Compile Settings L
Impairments						
Sine Noise Amplitude(Peak)	100 mV	Frequency	450 MHz	Apply to	🛛 Line A 🛛 🗹 Li	ne B 🗹 Line C
🗹 eSpike Area	300 Vps	Duration	2 ns	Apply to	🛛 Line A 🛛 🗹 Li	ne B 🗹 Line C
D TMin 20 ns						

Figure: 2.1.5(a) LP-eSpike configuration.

### Measurement details

The area of the spike can be measured using cursors, as shown below



Figure: 2.1.5(a) LP-eSpike Measurement.

## Test Procedure

- 1. Generate a LP waveform with signal parameters listed in the above section, with eSpike **disabled**.
- 2. Transmit the test sequence to the DUT.
- 3. Verify via any valid observable that the DUT received the test sequence without errors.
- 4. Reconfigure the Test System to **<u>enable</u>** eSpike, transmit the test sequence to the DUT.

## Observable Results

Verify via any valid observable that the DUT received the test sequence without errors.

## **GROUP 2: LP-RX BEHAVIORAL REQUIREMENTS**

#### Test/Calibration Setup

If any of the signal parameters of interest needs calibration, for this purpose the calibration setup should include with termination board. See section <u>LP Signal Calibration Setup</u>.

### LP-HS Burst waveform

This section provide details on how to create a LP\_HS pattern using C-PHYXPress. This pattern with a valid sequence, to test the Rx for error free reception is used in many test in this section.

The relevant parameters of the CPHYXpress application for this are listed below

- Signal Mode: Low Power High Speed
- Low Power: Symbol rate = 20MHz
- ➢ Low Power: Line Level − High=1.0 V, Low = 0V.
- Low Power: Pattern: Based on the DUT
- High Speed: Pattern: Based on the DUT, say PRBS9\_CPHY
- ▶ High Speed: Symbol Rate: Based on the DUT, say 1.5Gsps



Figure: LP\_HS burst waveform

## Pattern files

A number of pattern files which are needed for the tests in this group, are pre-created and located in \Datafiles folder, which would be available once C-PHYXpress application is installed on the system.

**\DataFiles folder location**: *C*:\*Users*\*Public*\*Tektronix*\*CPHYXpress*\*DataFiles* 

## List of pattern files

File Name	Description
Test_221.LP	TINIT period
Test_222_MARK1.LP	Mark state
Test_222_STOP.LP	Stop state
Test_223_Invalid_Escape_Entry_1.LP	Invalid escape mode entry commands
Test_223_Invalid_Escape_Entry_2.LP	
Test_224_TS1.LP	Various invalid escape mode commands
Test_224_TS2.LP	
Test_224_TS3.LP	
Test_224_TS4.LP	
Test_224_TS5.LP	
Test_224_TS6.LP	
Test_224_TS7.LP	
Test_224_TS8.LP	
Test_225_RT1.LP	Reset trigger and Unknown patterns as defined in escape mode
Test_225_Ukn3.LP	table
Test_225_Ukn4.LP	
Test_225_Ukn5.LP	
Test_226_Udf1.LP	Unsupported/Unassigned Commands
Test_226_Udf2.LP	
Test_226_Ukn3.LP	
Test_226_Ukn4.LP	
Test_226_Ukn5.LP	

## Test 2.2.1 – LP-RX Initialization period (TINIT)

### Discussion

C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for TINIT, which defines the initialization behavior of both Master and Slave devices.

TINIT is a protocol specific parameter. RX Initialization period (TINIT) of the slave DUT is required to be greater than this minimum conformant value.

768Note that  $t_{\text{INIT}}$  is considered a protocol-dependent parameter, and thus the exact requirements for  $t_{\text{INIT,MASTER}}$ 769and  $t_{\text{INIT,SLAVE}}$  (transmitter and receiver initialization Stop state lengths, respectively,) are defined by the770protocol layer specification and are outside the scope of this document. However, the C-PHY specification771does place a minimum bound on the lengths of  $t_{\text{INIT,MASTER}}$  and  $t_{\text{INIT,SLAVE}}$ , which each shall be no less than772100 µs. A protocol layer specification using the C-PHY specification may specify any values greater than this773limit, for example,  $t_{\text{INIT,MASTER}} \ge 1$  ms and  $t_{\text{INIT,SLAVE}} = 500$  to 800 µs.

#### Signal parameter

The relevant parameters of the CPHYXpress application for this test are listed below

- Signal Mode: Low Power
- Low Power: Symbol rate = 20MHz
- ➢ Low Power: Line Level − High=1.0 V, Low = 0V.
- Create a LP waveform representing the initialization period by using the following pattern. Low Power: Pattern:
  - low power state file: C:\Users\Public\Tektronix\CPHYXpress\DataFiles\Test\_221.LP
- This waveform is added in waveform sequence with repeat =1 as below. The setting of this repeat count generates a initialization period of ~1 usec
- The second waveform in the sequence is a valid LP\_HS waveform, whose content is based on the DUT.

н	iome Setup Waveform Plug-in Sequence Capture/Playback										
C	CPhySequence Steps used: 2 Remaining: 16381										
F	File   Edit  Edit  Sequence Settings										
	Track 1 Track 2 Repeat Event						Event	<b>C</b> - 1 -			
-	wait	Irack 1	Flags	I rack 2	Flags	Count	Input	Jump to	Go to		
1	Off	Init_VA		Init_VB		1	Off		Next		
2	Off	LP HS Burst_24GHz_VA		LP HS Burst_24GHz_VB		1	Off		First		
3											
4											
5											
6											

Figure: 2.2.1(a) Waveform Sequence to control the TINIT period

### Measurement details

To measure the TINIT, generated by a waveform sequence, use cursors as shown in the screen shot below.

File	Edit	Vertical	Horiz/Acq	Trig	Display	Cursors	Measure	Mask	Math	MyScope	Analyze	Utilities	Help	•			Ē	DSA73304D		Tek		X
	1									'' !			1									' <u>-</u>
-																						-
																						-
E																						
E			at Laws							tt												-
										‡												
										ļ				-					*****			-
Ē																						+
																	1					-
			+ <mark>-</mark>														_					+
																						-
E																						· ·
										‡												-
																						-
2																						- - -
																						-
Ē																						· · -
																						-
								, i		<u>, , †</u>	1 1 1				1 1	_		i		<u> </u>		
	C1 C2	100.0mV/div			• <sub>₩</sub> :20.0G • <sub>₩</sub> :20.0G		0.0s 121.6µs				A C1 / 392.0mV				Stop	Stopped Single Seq						
							<u>∆t</u> 121.6	µs									1 ac Man	qs Nd	ovembe	r 07. 20	RL:5.0M	35:49
							0.224	LU17														

Figure: 2.2.1(b) TINIT measurement using cursors for lines A and B

## Test Procedure

- 1. Connect the Slave DUT to the Test Setup, leaving the DUT power off.
- 2. Power on the DUT.
- 3. Without sending a valid Initialization period, send a valid test sequence that would otherwise cause an observable result. That is only transmit the second waveform in the sequence. Verify that the DUT ignores the test sequence.
- 4. Repeat the above procedure by slowly increasing the initialization period by increasing the reap count on the AWG sequence window, until the DUT is observed to accept the test sequence.
- 5. At this point record the TINIT = repeat count \* 1 usec.

## Observable Results

Verify that the value of TINIT is greater than the minimum protocol-specific conformance limit.

## Test 2.2.2 – ULPS Exit: LP-RX TWAKEUP Timer Value

## Discussion

The C-PHY Specification defines a mechanism for a lane to exit ULPS state. Mark-1 state (LP-100) for a minimum time TWAKEUP (1 msec), followed by a Stop state (LP-111), should make the slave exit the ULPS state.

## Signal parameter

Multiple waveforms are needed for this test.

- 1) **ULPS entry waveform**: A waveform to put the DUT in ULPS state. A sample *ULPS.LP* pattern file is at \Datafiles folder.
- 2) Valid Test LP\_HS waveform: A LP\_HS waveform with which could be used to check for error in reception.
- 3) **ULPS exit waveform**: A waveform to put the device out of ULPS state. More details on this is provided below

The relevant parameters of the CPHYXpress application to create a **ULPS exit waveform** are listed below

- Signal Mode: Low Power
- Low Power: Symbol rate = 20MHz
- ➢ Low Power: Line Level − High=1.0 V, Low = 0V.
- ULPS exit waveform is created using two pattern files located at \Datafiles, the configurations are show in Figure: 2.2.2(a)
  - Test\_222\_MARK1.LP
  - Test\_222\_STOP.LP
- The waveforms are added in waveform sequence with repeat counts as shown in the Figure 2.2.2(b). A repeat count of 500, results in about 1 ms of TWAKEUP time. The third waveform in the sequence is a valid LP\_HS waveform, whose content is based on the DUT.
| Signal Mode | : Low Power          | •                 |               |                       |                         |               |                  |
|-------------|----------------------|-------------------|---------------|-----------------------|-------------------------|---------------|------------------|
| High Speed  | High Speed Jitter    | High Speed Burst  | Low Power     | Low Power Noise       | High Speed Batch Mod    | e Preferences | Compile Settings |
| Base patt   | ern                  |                   |               |                       |                         |               |                  |
| Pattern     | Low power state file | e ▼ C:\Users\Pu   | blic\Tektroni | ix\CPHYXpress\Datai   | Files\Test_222_MARK1.LP |               |                  |
|             | LP content in Low P  | ower - High Speed | (LP-HS) Signa | al Mode               |                         |               |                  |
| Symbol      |                      |                   |               | Rise/Fall             |                         |               |                  |
| Symbol R    | ate 20 MHz           | TLPX 50           |               | Rise/Fall time (15%   | -85%) 0.1 UI            | = 5 n         |                  |
| C Line Leve | ls (High Impedance)  |                   |               |                       |                         |               |                  |
|             | High                 | Low               | _             |                       | -                       |               |                  |
| Line A      | 1 V                  | 50 mV             | 🗾 🗹 Use L     | ine A levels for Line | B and Line C ?          |               |                  |
| Line B      |                      | 50 mV             |               |                       |                         |               |                  |
| Line C      |                      | 50 mV             |               |                       |                         |               |                  |

Figure: 2.2.2(c) LP tab configuration to create Mark1 waveform

Н	ome Setup	Waveform Plug-in	Sequence	Capture/Playback						
C	PhySequence							Steps u Remain	sed: 3 ing: 1638	T 30 2
F	ile '	▼ Edit	- 61	Sequence	ce Settings					
	Wait	Ті	rack 1	Track 1 Flags	Track 2	Track 2 Flags	Repeat Count	Event Input	Event Jump to	Go to
1	Off	Mark1_VA			Mark1_VB		500	Off		Next
2	Off	StopState_V	/A		StopState_VB		1	Off		Next
3	Off	LP HS Burst	_24GHz_VA		LP HS Burst_24GHz_VB		1	Off		Next
4										
5										
6										
7										

Figure: 2.2.2(d) Waveform Sequence

## Measurement details

Cursor based measurement could be used to measure the TWAKEUP time generated by a waveform sequence.

#### Test Procedure

- 1. Send a **ULPS entry waveform** to put the DUT lane into ULPS state.
- 2. Next the waveform sequence consisting of Mark1 (for 1msec), stop state and a valid HS data sequence, created previously to the DUT in ULPS state.
- 3. Verify via any valid observable that the DUT received the data without errors. Error free reception confirms that the DUT has successfully exited form ULPS state

## Test 2.2.3 – LP-RX Invalid/Aborted Escape Mode Entry

## Discussion

The C-PHY Specification provides a definition of the Escape Mode Entry process in state-machine form. 681 A lane shall enter escape mode via an escape mode entry procedure (LP-111, LP-100, LP-000, LP-001, LP-

A faile shall enter escape indue via an escape indue entry procedure (LP-111, LP-100, LP-000, LP-001, LP-000). As soon as the final Bridge state (LP-000) is observed on the lines the lane shall enter escape mode in space state (LP-000). If an LP-111 is detected at any time before the final Bridge state (LP-000), the Escape

mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the
 Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop
 state.



In this test, the ability of the DUT's LP-RX to properly ignore invalid Escape Mode Entry sequences will be verified. Following two test cases of invalid escape mode entry sequence will be used for this test.

LP-111, LP-100, LP-000, LP-001, LP-000 (valid Escape Mode Entry sequence)

Test Case 1) LP-111, LP-100, LP-000, LP-001, LP-111 Test Case 2) LP-111, LP-100, LP-111, LP-111, LP-111

#### Signal parameters

Multiple waveforms are needed for this test.

- 1) Valid Test LP\_HS waveform: A LP\_HS waveform with which could be used to check for error free reception.
  - a. Procedure to create a LP\_HS waveform is given in section "LP-HS Burst pattern creation"
- 2) Invalid Escape Entry waveform: Waveform with invalid escape entry commands for two test
  - cases
    - a. Create "LP\_Invalid Escape Entry" pattern by selecting "Test 223\_Invalid\_Escape Entry\_1.LP" file in the Custom option as shown below and add the pattern to the AWG sequence.
    - b. Also create "LP\_Invalid Escape Entry" pattern by selecting "Test 223\_Invalid\_Escape Entry\_2.LP" file in the Custom option and add the pattern to the AWG sequence.

Plug-in: CPHYXpress 🔻					Co	mpile	
Signal Mode: Low Power 🔻							
High Speed High Speed Jitter	High Speed Burst	w Power Low Po	wer Noise	High Speed Batch Mode	Preferences	Compile Settings	Log View
Base pattern							
Pattern Low power state file	▼ C:\Users\Publi	c\tektronix\CPHYX	press\DataFil	es\Test_223_Invalid_Esca	pe_Entry_1.LP	F	
Include LP content in Low Po	ower - High Speed (LP	-HS) Signal Mode					
Symbol		Rise/Fa					
Symbol Rate 20 MHz	TLPX 50 ns	Rise/Fa	ll time (15%-	85%) 0.1 UI	= 5 ns		
Line Levels (High Impedance)							
High	Low	<b>—</b> ———————————————————————————————————					
Line A IV	50 mV	🗹 Use Line A lev	els for Line B	and Line C			
Line B 1 V	50 mV						
Line C 1 V	50 mV						
LP-HS Entry/Exit timing (Applic	able in LP-HS Signal r	node)					
Start LP-111 duration	2	LP Symbols =	100 ns				
LP-000 duration(t3_PREPARE)	1	LP Symbols =	50 ns				
Enable THS_Exit							
End LP-111 duration		LP Symbols =	100 ns				

Figure: 2.2.3(a) LP Custom option selection.

(	Channel 1 CPhySeque	nce - Track 1 🛛 👻				,	Amplitude	476 mVpp
	Wait	Track	Flag	Repeat	Event	Jump to		Go to
1	Off	LP HS Burst_24GHz_VA		œ	Off		Next	
2	Off	LP_Valid Escape Entry_24GHz_VA		1	Off		First	
_								
Fo	rce jump to Coupled Seq	uence Current step:						SR: 24.00 GS/s
(	Channel 2 CPhySeque	nce - Track 2 🔹 👻					Amplitude	476 mVpp
	Wait	Track	Flag	Repeat	Event	Jump to		Go to
1	Off	LP HS Burst_24GHz_VB		00	Off		Next	
2	Off	LP_Valid Escape Entry_24GHz_VB	:	1	Off		First	
_								
Fo	rce jump to Coupled Seq	uence Current step:						SR: 24.00 GS/s

## Figure: 2.2.3(b) LP Valid Escape Entry sequence

#### *Test Procedure*

- 1. Connect the DUT to the AWG.
- 2. Configure the Test Setup to transmit sequence with LP HS Burst pattern to the DUT, and verify that the data is properly received by the DUT with no errors.
- 3. Next insert Testcase#1 waveform into the sequence which has invalid Escape Mode Entry sequence.
- 4. Verify that the DUT is still able to successfully receive the data without errors.
- 5. Repeat steps 3 and 4 with Testcase#2 waveform.

#### *Observable Results*

For both test cases, verify that the DUT received the data without errors.

# Test 2.2.4 – LP-RX Invalid/Aborted Escape Mode Command

#### Purpose

To verify that the DUT's LP-RX properly ignores invalid/aborted Escape commands.

### Discussion

The previous test (2.2.3) verified a DUTs ability to detect invalidly formed Escape Mode Entry sequences, which were corrupted with LP-111 Stop states at different locations in the Escape Mode Entry sequence. The result of these tests was that the DUT should have effectively ignored the invalid sequence and not have allowed the invalid sequences to negatively impact reception of subsequent valid data.

A lane shall enter escape mode via an escape mode entry procedure (LP-111, LP-100, LP-000, LP-001, LP-000). As soon as the final Bridge state (LP-000) is observed on the lines the lane shall enter escape mode in space state (LP-000). If an LP-111 is detected at any time before the final Bridge state (LP-000), the Escape

2. If LP-111 occurs during escape mode the lane returns to Stop state (Control Mode LP-111).

#### Signal parameters

Below LP test cases are used to test the invalidly formed Escape Mode Entry.

1)	[Valid EM Entry]	+	LP-001/	000/00	1/000	/001/0	000/10	0/000/	100/0	00/100	/000/	100/0	00/003	/111	+	[Stop]
2)	[Valid EM Entry]	+	LP-001/	000/00	)1/000	)/001/(	000/10	0/000/	100/0	00/100	/000/	100/1	11/11	1/111	+	[Stop]
3)	[Valid EM Entry]	+	LP-001/	000/00	1/000	)/001/(	000/10	0/000/	100/0	00/100	/111/	111/1	11/11	/111	+	[Stop]
4)	[Valid EM Entry]	+	LP-001/	000/00	)1/000	)/001/(	000/10	0/000/	100/ <mark>1</mark>	11/111	/111/	111/1	11/11	1/111	+	[Stop]
5)	[Valid EM Entry]	+	LP-001/	000/00	)1/000	)/001/(	000/10	0/111/	111/1	11/111	/111/	111/1	11/11	1/111	+	[Stop]
6)	[Valid EM Entry]	+	LP-001/	000/00	)1/000	)/001/	111/11	1/111/	111/1	11/111	/111/	111/1	11/11	/111	+	[Stop]
7)	[Valid EM Entry]	+	LP-001/	000/00	)1/111	/111/	111/11	1/111/	111/1	11/111	/111/	111/1	11/11	1/111	+	[Stop]
8)	[Valid EM Entry]	+	LP-001/	111/1	1/111	/111/	111/11	1/111/	111/1	11/111	/111/	111/1	11/11	1/111	+	[Stop]

- 1. Add "LP HS Burst" pattern (Created in the session "LP-HS Burst pattern creation") to the AWG sequence.
- 2. Create "LP\_Escape command Entry\_TS1" pattern by selecting "Test 224\_TS1.LP" file in the Custom option as shown below and add the pattern to the AWG sequence.
- 3. Create "LP\_Escape command Entry\_TS2" pattern by selecting "Test 224\_TS2.LP" file in the Custom option.
- 4. Create "LP\_Escape command Entry\_TS3", "LP\_Escape command Entry\_TS4" "LP\_Escape command Entry\_TS5" "LP\_Escape command Entry\_TS6" "LP\_Escape command Entry\_TS7" and "LP\_Escape command Entry\_TS8" by selecting "Test 224\_TS3.LP" "Test 224\_TS4.LP" "Test 224\_TS5.LP" "Test 224\_TS6.LP" "Test 224\_TS7.LP" and "Test 224\_TS8.LP" file in the Custom option respectively.

s	ignal Mode:	Low Power	-						
ł	High Speed	High Speed Jitter	High Speed Burst	ow Power Low Pov	wer Noise High	Speed Batch Mode	Preferences	•	
	Base patte	rn Custom ▼ C:\U LP content in Low Pc	sers\Public\Tektronix\ wer - High Speed (LP	,CPHYXpress\DataF -HS) Signal Mode	iles\Test 224_TS1.	₽ 📄			
	Symbol Symbol rat	e: 20 MHz	TLPX: 50 ns	Rise/Fa	II time (15%-85%)	0.1 UI	= 5 ns		
	High: 10 Note: High	(High impedance) 00 n line level >= Low lin	nV Low: 50 ne level + 200mV	mV					
	LP-HS Entr	y/Exit timing (Applic	able in LP-HS Signal r	node)					
	Start LP-11	1 duration:	2	LP symbols =					
	LP-000 dur	ation(t3_PREPARE):	1	LP symbols =					
	Enable	THS_Exit							
	End LP-111	duration:	2	LP symbols =	100 ns				l

Figure: 2.2.4(a) LP\_Escape command Entry creation

(1	Channel 1 CPhySeque	nce - Track 1 🔹 🔻				,	Amplitude	476 mVpp
	Wait	Track	Flag	Repeat	Event	Jump to		Go to
1	Off	LP HS Burst_24GHz_VA		00	Off		Next	
2	Off	LP_Escape command Entry_TS1_24		8	Off		Next	
Fo	rce jump to Coupled Seq	uence Current step:						SR: 24.00 GS/s
(	Channel 2 CPhySeque	nce - Track 2 🗸 🗸					Amplitude	476 mVpp
	Wait	Track	Flag	Repeat	Event	Jump to		Go to
1	Off	LP HS Burst_24GHz_VB		8	Off		Next	
2	Off	LP_Escape command Entry_TS1		00	Off		Next	
Fo	rce jump to Coupled Seq	uence Current step:						SR: 24.00 GS/s

Figure 2.2.4(b): LP\_Escape command Entry sequence

- 1. Connect the DUT to the AWG.
- 2. Configure the Test Setup to transmit sequence with LP HS Burst pattern to the DUT, and verify that the data is properly received by the DUT with no errors.
- 3. Once proper operation has been verified as step 1, the Test case 1 pattern with aborted ULPS command sequences is send to DUT.
- 4. Verify that the DUT is still able to successfully receive the data without impairment.
- 5. Once proper operation has been verified as step 1, the Test case 2 pattern with aborted ULPS command sequences is send to DUT.
- 6. Verify that the DUT is still able to successfully receive the data without impairment.
- 7. Repeat for all the steps from 5 to 6 for Test case 3 to 8.

### Observable Results

In all cases, verify that the integrity of the received data, as well as the overall operation of the DUT are not negatively affected by the presence of the invalid/aborted ULPS command sequences.

# Test 2.2.5 – LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits

#### Purpose

To verify that the DUT's LP-RX ignores any extra bits received following a Trigger Command.

#### Discussion

The C-PHY specification defines the Escape Mode behavior for C-PHY transmitters and receivers. This includes a requirement for how receivers treat extra bits that are received after an Escape Mode Trigger command. The choice of the extra post-command bits must be defined for this test. This test will concatenate one extra byte of data after the Trigger command, and will use the ULPS Entry command as this extra byte.

	Table 16 Escape Entry Codes									
Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)								
Low-Power Data Transmission	mode	11100001								
Ultra-Low Power State	mode	00011110								
Undefined-1	mode	10011111								
Undefined-2	mode	11011110								
Reset-Trigger [Remote Application]	Trigger	01100010								
Unknown-3	Trigger	01011101								
Unknown-4	Trigger	00100001								
Unknown-5	Trigger	10100000								

## Signal parameters:

- Signal Mode: Low Power-High Speed
- ▶ HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz resulting TLPX of 50ns
- Low Power Pattern: Low power state file
- Add "LP HS Burst" pattern (Created in the session "LP-HS Burst pattern creation") to the AWG sequence.
- Many pattern files needed for this test are at "C:\Users\Public\Tektronix\CPHYXpress\DataFiles"
- Create "Reset Trigger" pattern by selecting "Test 225\_RT1.LP" file in the Custom option as shown below and add the pattern to the AWG sequence.
- Create "Unknown-3" pattern by selecting "Test\_225\_Ukn3.LP" file in the Custom option as shown below.
- Create "Unknown-4" pattern by selecting "Test\_225\_Ukn4.LP" file in the Custom option as shown below.
- Create "Unknown-5" pattern by selecting "Test\_225\_Ukn5.LP" file in the Custom option as shown below.

|--|

Plug-in: CPHYXpress 👻	Compile	Reset Plug-in Help 👻
Signal Mode: Low Power 🗸		
High Speed High Speed Jitter High Speed Burs	Low Power Low Power Noise High Speed Batch Mode Preferences Compile Settings Log View	•
Base pattern		
Pattern Low power state file ▼ C:\Users\	Public\Tektronix\CPHYXpress\DataFiles\Test_225_RT1.LP	
Include LP content in Low Power - High Spee	d (LP-HS) Signal Mode	
Symbol	Rise/Fall	
Symbol Rate 20 MHz TLPX	0 ns Rise/Fall time (15%-85%) 0.1 UI = 5 ns	
Line Levels (High Impedance)		
High Low		
Line A 1 V 50 mV	☑ Use Line A levels for Line B and Line C ?	
Line B 1 V 50 mV		
Line C 1 V 50 mV		
LP-HS Entry/Exit timing (Applicable in LP-HS Sig	inal mode)	
Start LP-111 duration 2	LP Symbols = 100 ns	
LP-000 duration(t3 PREPARE)	LP Symbols = 50 ns	
Fnahle THS Evit		
End LP-111 duration 2	LP Symbols = 100 ns	

Figure: 2.2.5(a) Low power state file for "Reset Trigger"

Above created base pattern using Low power state file is sequenced with the "LP HS Burst" pattern (Created in the session "LP-HS Burst pattern creation") to the AWG sequence is shown below

н	ome Setup Wa	veform Plug-in Sequence Capture	/Playback									-
C	PhySequence							St Re	teps used: 2 emaining: 16	Tota 381 S/	l time: /s	
F	ile 🔻	Edit 🗸 🖥 🖬 🖬	Sequence Setti	ings								
	Wait	Track 1	Track 1 Flags	Track 2	Track 2 Flags	Repeat Count	Event Input	Event Jump to	Go to	Length	Time	
1	Off	LP HS Burst_24GHz_VA		LP HS Burst_24GHz_VB		10	Off		Next	73.008 k		
2	Off	LP_2GHz_VA		LP_2GHz_VB		10	Off		First	4.2 k		
3												
4												
5												
6												

Figure 2.4.5(b) Sequenced Waveform of LP-HS Burst and LP state file pattern

- 1. Connect the DUT to the AWG.
- 2. Configure the Test Setup to transmit sequence with LP HS Burst pattern to the DUT, and verify that the data is properly received by the DUT with no errors.
- 3. Once proper operation has been verified as step 1, Reset Trigger pattern with ULPS command added in sequence shown in Figure 2.4.5(b) is send to DUT.
- 4. Verify that the DUT is still able to successfully receive the data without impairment.
- 5. Repeat for all the steps from 3 to 4 for Unknown-3, Unknown-4, and Unknown-5 Trigger commands in place of the Reset-Trigger pattern.

#### Observable Results

Verify that in all test cases (Trigger command, Unknown-3, Unknown-4, and Unknown-5) the DUT ignores all bits occurring after the last bit of the Trigger Command, by observing that the DUT properly received the data stream without error.

## Test 2.2.6 – LP-RX Escape Mode Unsupported/Unassigned Commands

#### Purpose

To verify that the DUT's LP-RX properly ignores unsupported and unassigned Escape Mode commands.

#### Discussion

The Escape Mode sequence will contain an unassigned Escape command byte. The DUT's behavior will be observed to verify that the presence of the unassigned command code does not impact reception of the valid data stream. In this test, the AWG will be sent all 5 unassigned Command codes, contained in properly formed, valid Escape sequences. It will also be sent the Undefined-1, Undefined-2, Unknown-3, Unknown-4, and Unknown-5 Command codes shown below. In all cases, the DUT should ignore the command code.

Table 16 Escape Entry Codes								
Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)						
Low-Power Data Transmission	mode	11100001						
Ultra-Low Power State	mode	00011110						
Undefined-1	mode	10011111						
Undefined-2	mode	11011110						
Reset-Trigger [Remote Application]	Trigger	01100010						
Unknown-3	Trigger	01011101						
Unknown-4	Trigger	00100001						
Unknown-5	Trigger	10100000						

#### Signal parameters

- Signal Mode: Low Power-High Speed
- HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz resulting TLPX of 50ns
- Low Power Pattern: Low power state file
- Add "LP HS Burst" pattern (Created in the session "LP-HS Burst pattern creation") to the AWG sequence.
- Many pattern files needed for this test are at <u>DataFiles</u> folder.
- Create "Undefined-1" pattern by selecting "Test\_226\_Udf1.LP" file in the Custom option as shown below and add the pattern to the AWG sequence.
- Create "Undefined-2" pattern by selecting "Test\_226\_Udf2.LP" file in the Custom option as shown below.

Create "Unknown-3", "Unknown-4", and "Unknown-5", pattern by selecting "Test\_226\_Ukn3.LP", "Test\_226\_Ukn4.LP" and "Test\_226\_Ukn5.LP" file respectively.

Plug-in: CPHYXpress 🔻	Compile	Reset Plug-in Help 👻					
Signal Mode: Low Power 👻							
High Speed High Speed Jitter High Speed Burst	Low Power Low Power Noise High Speed Batch Mode Preferences Compile Settings Log View	•					
Base pattern							
Pattern Low power state file  C:\Users\Put	olic\Tektronix\CPHYXpress\DataFiles\Test_226_Udf1.LP						
Include LP content in Low Power - High Speed (	P-HS) Signal Mode						
Symbol	Rise/Fall						
Symbol Rate 20 MHz TLPX 50	ns Rise/Fall time (15%-85%) 0.1 UI = 5 ns						
Cline Levels (High Impedance)							
High Low							
Line A 1V 50 mV	Use Line A levels for Line B and Line C						
Line B 1 V 50 mV							
Line C 1 V 50 mV							
LP-HS Entry/Exit timing (Applicable in LP-HS Signa	l mode)						
Start LP-111 duration 2	LP Symbols = 100 ns						
LP-000 duration(t3_PREPARE) 1	LP Symbols = 50 ns						
Enable THS_Exit							
End LP-111 duration 2	LP Symbols = 100 ns						

Low Power State file to be used to create Escape Mode Action which is given in above table.

Figure 2.4.6(a) Low Power Base pattern

Above created base pattern using Low power state file is sequenced with the "LP HS Burst" pattern (Created in the session "LP-HS Burst pattern creation") to the AWG sequence is shown below

н	iome Setup Wave	form Plug-in Sequence Capture/	Playback									
С	CPhySequence Steps used: 2 Total time: Parminican 16291 Steps											
F	File  Edit  Sequence Settings											
	Wait	Track 1	Track 1 Flags	Track 2	Track 2 Flags	Repeat Count	Event Input	Event Jump to	Go to	Length	Time	
1	Off	LP HS Burst_24GHz_VA		LP HS Burst_24GHz_VB		10	Off		Next	73.008 k		
2	Off	LP_2GHz_VA		LP_2GHz_VB		10	Off		First	4.2 k		
3	<b>.</b>											
4												
5												
6												

Figure 2.4.6(b) Sequenced Waveform of LP-HS Burst and LP state file pattern

- 1. Connect the DUT to the AWG.
- 2. Configure the Test Setup to transmit sequence with LP HS Burst pattern to the DUT, and verify that the data is properly received by the DUT with no errors.
- 3. Once proper operation has been verified as step 1, Undefined-1 pattern added in sequence Figure 2.4.6(b) is send to DUT.
- 4. Verify that the DUT is still able to successfully receive the data without impairment.
- 5. Repeat for all the steps from 3 to 4 for Undefined-2, Unknown-3, Unknown-4, and Unknown-5 Trigger commands in place of the Undefined-1 command.

## Observable Results

For all test cases, verify that the DUT ignores the unsupported/unassigned command, and successfully receives the data in DUT.

# GROUP 3: HS-RX VOLTAGE AND JITTER TOLERANCE REQUIREMENTS

## Test/Calibration Setup

This group of tests requires HS only signals. For calibration of these stimuli, the signal generator outputs is directly connected to an oscilloscope. See section <u>HS Signal Calibration Setup</u>.

# Test 2.3.1 - HS-RX Amplitude Tolerance (VCPRX (DC), VIHHS, VILHS)

## Discussion

In this the DUT is tested for various cases of common mode and differential voltage levels covering the maximum and minimum levels allowed for these two parameters. The Table below list four test cases for this measurement.

Test	Test     Common-Mode Level     Differential Voltage Pk-pk       Case     (mV)     (2*VOD) (mVppd)		Single Ended Voltage
Case			VIHHS/VILHS (mV)
1	95	540	230/-40
		(strong one to strong zero level)	
2	95	80	135/55
		(Weak one to weak zero level)	
3	390	580	535/245
		(strong one to strong zero level)	
4	390	80	430/350
		(Weak one to weak zero level)	

## Table 2.3.1-1: Differential/Common-Mode Amplitude Test Cases

## Signal parameters

- Signal Mode: HS
- ➢ HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Line Levels: High and Low, represent the VIHHS/VILHS voltages

File Connectivity Tools N	Vindows Help			
				Stopped
Home Setup Wavefor	m Plug-in Sequence Capture	e/Playback		
Plug-in: CPHYXpress	•			Compile
Signal Mode: High Sp	æd ▼			
High Speed High Spee	d Jitter High Speed Burst Lo	w Power Low Power	Noise High Speed Batch Mode Pre	ferences
Base Pattern				
Pattern PRBS9_CPH	Y 🔻		🛐 🗹 Repeat to a 16 bit boundary	
PRBS_CPHY Seed				
		0 0 1 1 0	10	
Q18Q17Q16	0x789A		— Q1	
Note: Seed is applicab	le only for PRBS_CPHY Pattern	types.		
Symbol	Rise/F	all		
Symbol rate 1.5	Gsps Rise/Fa	all time(0-100%) 0 L	II = 0 s	
Line Levels	VIIHIS LOW VILHS	Mid		
Line A: 230 mV	-40 mV		🗹 Use Line A levels for Line B and Li	ne C <mark>?</mark>
Line B: 230 mV	-40 mV	95 mV		
Line C: 230 mV	40 mV	95 mV		

Figure 2.3.1(a): Configurations for line levels

- Generate a HS waveform with signal parameter listed above and VIHHS/VILHS mentioned for test case 1 in Table 2.3.1.1. VIHHS/VILHS are set by configuring high and low voltage values in the Line Levels configuration sections Figure 2.3.1(a) ("Use Line A levels for Line B and Line C should be checked")
- 2. Measure VIHHS/VILHS for all the three wire A, B and C. Measurement can be performed using a cursor based measurement as shown in Figure 2.3.1(b). To calibrate for the VIH/VIL levels follow the procedure in section <u>Voltage (VIH/VIL) Calibration Procedure</u>
- 3. Transmit the test sequence to the Rx DUT. Verify via any valid observable that the DUT received the test sequence without errors
- 4. Repeat all the above steps for Test case 2, 3 and 4 given in the Table 2.3.1-1.

## Observable Results

Verify that for all four test cases that the test sequence was received by the DUT without error.

Exa	mp	le Res	sult																		
File	Edit	Vertical	Horiz/Acq	Trig	Display	Cursors	Measure	Mask	Math	MyScope	Analyze	Utilities	Help	•			0207	0804C	Tek		×
0																					
1 militari									• • •	· · · · · · · · · · · · ·											
	c1 ) c2 ) C3 )	90.0mV/d 90.0mV/d 90.0mV/d	liv liv liv	50Ω 50Ω 50Ω	¶¥√8.0G ¶¥√8.0G ¶¥√8.0G		230.74 2 43.54 2 -274.2	42mV 12mV 184mV				A' 💽	<b>1</b> ) / 9	7.2mV		20. Pro 0 a Ma	.0µs/di eview icqs in Fe	ebruary	GS/s Single S 7 05, 201	40.0ps eq RL:5.0M 6 02:2	/pt 25:05
1		Vertic	al Setup																		8
	han 1 han 2 han 3	Lat	blay bel	Terr	mination 50 Ω	(	Coupling DC GND	•	8 Digital I (Digital F	Bandwidt 0.0 GHz Filters (DSI	th P) Enabled ed when the	1	Por -40.0 -50	sition Omdiv cale .0mV	a	Chu Dei	skew tten		Multi Zoo Vert	View m ical	$\nabla \Delta$
	han 4 Aux	Un No	its ne					•	(Digit	ce Constar al fiters ensu Only	nt Sample ured)	Rate	•			Pr	obe		9		
		Prop	erties						Ap	ply To All C	Channels			ffset .0V		Cor	trois				J

Figure 2.3.1(b): VIHHS/VILHS result on Line A



Figure 2.3.1(c): Differential Eye diagram (AB)

# Test 2.3.2 HS-RX Differential Input High/Low Thresholds (VIDTH, VIDTL)

#### Discussion

The definition and the conformance limits for the Differential Input High and Low Thresholds are given below. These are the minimum differential signal levels seen as an HS Strong 1 and HS Strong 0 by the receiver.

1189 The differential input high and low threshold voltages of the high-speed receiver are denoted by  $V_{IDTH}$  and 1190  $V_{IDTL}$ , respectively.  $V_{ILHS}$  and  $V_{IHHS}$  are the single-ended, input low and input high voltages, respectively. 1191  $V_{CPRX(DC)}$  is the differential input common-point voltage. The high-speed receiver shall be able to detect 1192 differential signals at its A, B and C input signal pins when all three signal voltages,  $V_A$ ,  $V_B$  and  $V_C$ , are 1193 within the common-point voltage range and if the voltage differences between  $V_A$ ,  $V_B$  and  $V_C$  exceed either 1194  $V_{IDTH}$  or  $V_{IDTL}$ . The high-speed receiver shall receive high-speed data correctly while rejecting common-

Parameter	Min	Max	
Differential input high threshold		40	mV
Differential input low threshold	-40		mV

Table 2.3.2-2: VIDTH, VIDTL Conformance Limits

## Signal parameters

- Signal Mode: HS
- ▶ HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Line Levels: High = 325mV and Low = 175 mV, represent the VIHHS/VILHS voltages to achieve a nominal differential voltage of 300mV strong one to strong zero level and common-mode level of 250mV.

File	Connectivity Tools Window	s Help		(	Stopped	
0	Home Setup Waveform Plug	in Sequence Capt	ure/Playback			
onnectiv	Plug-in: CPHYXpress 🔹				Compile	
ity W	Signal Mode: High Speed 🕶	)				
avefor	High Speed High Speed Jitter	High Speed Burst	Low Power Low Power	Noise High Speed Batch Mode Prefer	rences	
Suu	Base Pattern					
equer	Pattern PRBS9_CPHY -			🛐 💆 Repeat to a 16 bit boundary		
ices	PRBS_CPHY Seed	1000 1	001 10	10		
	Q18Q17Q16	— 0x789A —		— q1		
	Note: Seed is applicable only	for PRBS_CPHY Patter	m types.			
	Symbol	Rise	:/Fall			
	Symbol rate 1.5	Gsps Rise	/Fall time(0-100%) 0	<b>A</b> = 0s		
	Line Levels High	Low	Mid			
	Line A: 325 mV	175 mV	250 mV	🗹 Use Line A levels for Line B and Line	e C 🖸	
	Line B: 325 mV					
	Line C: 325 mV					

Figure 2.3.2-3: Line level configuration

## Measurement details

The following two measurement from the TekExpress C-PHY\_Tx Essentials application to be used for this test.

- a) Eye Diagram
- b) DC Common Mode Measurement

TekExpres	ss C-PHY Tx Esse	ntials - (Untitled)*	Options	$- \times$
Setup	DUT	Transmitter : Essentials	Select All	Start
Status       Results       Reports	<ul> <li>Test Selection</li> <li>Acquisitions</li> <li>Configuration</li> <li>Preferences</li> </ul>	Essentials     Rise Time     Fall Time     DC Common Mode measurement     AC Common Mode Mismatch Measurement     AC common mode Level variation between (50MHz ar     AC common mode Level variation (Above 450MHz)     IntraPair Skew	1d 450MHz)	Pause
		Test Description This test confirms that the static point common mode voltage of DUT Trio signal are within the limits of the specification	Schematic	
Re	ady.			

Eye Diagram		<u></u>					
Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
Eye Height of AB	195.0544	mV	Pass	115.0544	80	N.A	-
Eye Height of BC	201.5637	mV	Pass	121.5637	80	N.A	-
Eye Height of CA	207.8915	mV	Pass	127.8915	80	N.A	-
Eye Width of AB	313.2222	ps	Pass	153.2222	160.0000	N.A	-
Eye Width of BC	355.3846	ps	Pass	195.3846	160.0000	N.A	-
Eye Width of CA	332.0000	ps	Pass	172.0000	160.0000	N.A	-
MaskHits of AB	0.0000	Hits	Pass	0.0000	N.A	0	-
MaskHits of BC	0.0000	Hits	Pass	0.0000	N.A	0	-
MaskHits of CA	0.0000	Hits	Pass	0.0000	N.A	0	-
COMMENTS							
DC Common Mod	e measurement						Back to Summary Ta
Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
DC Common Mode Voltage	191.5115	mV	Pass	16.5115, 118.4885	175	310	-
COMMENTS							

Figure 2.3.2-4: CPHY\_Tx Essentials application and report example

- Beginning with HS line levels of high = 325 mV, low = 175 mV to achieve nominal differential and common mode level. Adjust HS High level and HS Low level on CPHYXpress, to measure the following for using TekXpress CPHY\_Tx Essentials.
  - a. Eye height of differential AB, BC & CA to be 150 mV (300 mV pk-pk differential voltage).
  - b. DC Common Mode Voltage ~ 250mV
- 2. Transmit the test sequence to the DUT. Verify via any valid observable that the DUT received the test sequence without errors.
- 3. On CPHYXpress do the following, to reduce the pk-pk differential and maintain the nominal common mode level of 250 mV:
  - a. Decrease HS Line level: high by (say 20mV) and
  - b. Increase HS Line level: low by the same amount (20 mV)
- 4. Repeat the steps (2) and (3) until the DUT begins to indicate errors
- 5. Note the smallest value of the measurement of Eye\_Height of AB, BC and CA, for which the DUT was able to receive the test sequence without errors.
- 6. Compute the half of the minimum of eye height of the three differential waveforms. This value represent the peak differential voltage  $V_{IDTH}/V_{IDTL}$

#### Observable Results

Verify that  $V_{IDTH}/V_{IDTL} \le 40 \text{mV}$ .

## Test 2.3.3 – HS-RX Jitter Tolerance

## Discussion

C-PHY Specification defines the High Speed Timing requirements in the form of Rx eye diagram, which HS receiver must support. The Rx eye diagram is shown in figure below:



Parameter	Description	Min	Nom	Max	Units	Notes
teye_ramp_rx	Eye ramp time at the receiver	0.25			UI	
t <sub>EYE_WIDTH_RX</sub>	Eye width at the receiver	0.5			UI	
tui_average	UI average		UIINST			

## Figure 2.3.3(a): HS Rx Eye Diagram and Timing parameters

In this test, the timing of a test signal will be modified, and the test signal will be sent to the DUT, to see if it can properly receive the signal. The signal will be calibrated using the HS-RX eye diagram as a reference.

The methodology to create the eye diagram for C-PHY signaling is slightly different than for traditional 2-level signaling. C-PHY uses a 'triggered eye' as shown in figure below. Additionally, the eye mask is allowed to be moved horizontally (optimally) to the left (i.e., away from the zero crossing) to a position where there are zero mask hits.



This following reference channel specified in v1.0 is shown in Figure 2.3.3(b). This channel is named as the CPHY Legacy channel in specification v1.1. In addition, three more reference channels which are specified in v1.1, Figure 2.3.3(c).



Figure 2.3.3(b): Legacy Channel



Figure 2.3.3(c): Reference channels – Short, Standard and Long

For the purposes of this test,

- 1. To test specification v1.0 devices, the CPHY legacy channel is to be used as a reference for testing. Maximum operating as specified in the device datasheet used for this test.
- 2. To test specification v1.1 devices, Maximum operating as specified in the device datasheet used for this test. Based on this maximum speed and the equalization options, the test channel is chosen as per the table below.

Channel	TXEQ Option Disabled	TXEQ Option Enabled
Short Reference Channel	1.7Gsps < Rate ≤ 2.5Gsps	2.8Gsps < Rate ≤ 3.0Gsps
Standard Reference Channel	1.3Gsps < Rate ≤ 1.7Gsps	2.0Gsps < Rate ≤ 2.8Gsps
Long Reference Channel	80Msps ≤ Rate ≤ 1.3Gsps	80Msps ≤ Rate ≤ 2.0Gsps

Table 2.3.3-1 Channel Selection Based on Symbol Rate

# Signal parameters

- Signal Mode: HS
- Maximum symbol rate supported by the DUT is used for this test.
- > HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Line Levels: High = 250 mV and Low = 0 mV

- High Speed Jitter Tab ->Duty cycle distortion
- ➢ High Speed Jitter Tab ->Channel embedding vis FLT files

88		Stopped
Home Setup Waveform Plug-in Sequence Capt	ire/Playback	
Plug-in: CPHYXpress •		Compile
Signal Mode: High Speed •		
High Speed High Speed Jitter High Speed Burst	ow Power Low Power Noise High Speed Batch Mode Preferences	
Rase Pattern		
Pattern PR859_CPHY +	📄 🧭 Repeat to a 16 bit boundary	
PR85_CPHY Seed		
Q18Q17Q16 0x789A		
Note: Seed is applicable only for PR85_CPHY Patter	n types.	
Symbol	rfall	1
Symbol Rise Symbol rate 2.5 Gips Rise	Fall Fall time(0-100%) 0 UI = 0 s	
Symbol Symbol rate 2.5 Gsps Rise	Fall Fall time(0-100%) 0 Ut = 0 s	
Symbol Symbol rate 2.5 Gsps Rise Line Levels High Low	Fall         =         0 s           Mid	
Symbol Rise Symbol rate 2.5 Gips Rise Line Levels Line A: 250 mV 0 V	Fall     0 s       Fall time(D-100%)     0 Lt       Mid       125 mV   Use Line A levels for Line B and Line C	
Symbol rate 2.5 Gaps Rise Symbol rate 2.5 Gaps Rise Line Levels High Low Line A: 250 mV 0 V Line B: 250 mV 0 V	Fall     =     0 s       Fall time(0-100%)     0 LI     =     0 s       Mid     125 mV     Image: Second Seco	
Symbol rate 2.5 Gaps Rise Symbol rate 2.5 Gaps Rise Line Levels Line A: 250 mV 0 V Line B: 250 mV 0 V Line C: 250 mV 0 V	Fall time(D-100%) OLT = 0 5 Mid 125 mV V Use Line A levels for Line B and Line C 1 125 mV 125 mV	
Symbol set 25 Gips Rise Symbol rate 25 Gips Rise Line Levels High Low Line A: 250 mV 0 V Line B: 250 mV 0 V Line C: 250 mV 0 V	Fall     0 s       Fall time(D-100%)     0 UI       Mid       125 mV       125 mV       125 mV	
Symbol rate 2.5 Gips Rise Symbol rate 2.5 Gips Rise Line Levels Use All 250 mV OV Line A: 250 mV OV Line C: 250 mV OV	Fall     0 s       Fall time(0-100%)     0 Lt       Mid       125 mV       225 mV       125 mV       125 mV       125 mV	

Figure 2.3.3(a): Data rate and Line level configurations

File Connectivity Tools Windows Help  Stopped
Home Setup Waveform Plug-in Sequence Capture/Playback
Signal Mode: High Speed -
High Speed High Speed Jitter High Speed Burst Low Power Low Power Noise High Speed Batch Mode Preferences Jitter Periodic Jitter(pk-pk) 0 UI Frequency: 10 MHz Random Jitter(RMS) 0 UI
Duty Cycle Distortion     5 %     Apply to:     Ine A     Ine B     Ine C       Sine Noise Amplitude(pk)     0 V     Frequency:     10 MHz
Embed Channel     FLT Files     Line A: E\OldPC_652\Tektronix\SPL\Projects\MIP\C&DX\Filt\CPHY_legacy_fs25G.flt     E\OldPC_652\Tektronix\SPL\Projects\MIP\C&DX\Filt\CP
S-Parameter File

Figure 2.3.3(b): Duty Cycle Distortion and Channel embedding

## Measurement details

The following two measurement from the TekXpress CPHY\_Tx Essentials application to be used for this test.

- a) Eye Diagram
- b) DC Common Mode Measurement

🗸 TekExp	ress C-PHY Tx Esse	ntials - (Untitled)*	Options	-×
Setup	DUT	Transmitter : Essentials	Select All	Start
Status Results Reports	<ul> <li>2 Test Selection</li> <li>3 Acquisitions</li> <li>4 Configuration</li> <li>5 Preferences</li> </ul>	Essentials     Rise Time     Fall Time     Fye Diagram     OC Common Mode measurement     AC Common Mode Mismatch Measurement     AC common mode Level variation between (50MHz an     AC common mode Level variation (Above 450MHz)     IntraPair Skew	ıd 450MHz)	Pause
		Test Description		
		mode voltage of DUT Trio signal are within the limits of the specification	schematic	
	Ready.			

Eye Diagram							
Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
Eve Height of AB	195.0544	mV	Pass	115.0544	80	N.A	-
Eye Height of BC	201.5637	mV	Pass	121.5637	80	N.A	-
Eve Height of CA	207.8915	mV	Pass	127.8915	80	N.A	-
Eye Width of AB	313.2222	ps	Pass	153.2222	160.0000	N.A	-
Eye Width of BC	355.3846	ps	Pass	195.3846	160.0000	N.A	-
Eye Width of CA	332.0000	ps	Pass	172.0000	160.0000	N.A	-
MaskHits of AB	0.0000	Hits	Pass	0.0000	N.A	0	-
MaskHits of BC	0.0000	Hits	Pass	0.0000	N.A	0	-
MaskHits of CA	0.0000	Hits	Pass	0.0000	N.A	0	-
COMMENTS							
Back to Summary Table							
Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
DC Common Mode Voltage	191.5115	mV	Pass	16.5115, 118.4885	175	310	-
COMMENTS							
COMMENTS						В	ack to Sumr

Figure 2.3.2-4: CPHY\_Tx Essentials application and report example

Г

## Calibration Procedure

Step	Procedure	Expected Result
1.	Create a PRBS9 pattern with nominal voltages	Eye width<=0.865 UI
	Refer Figure 2.3.3(a)	
		If Eye width is > 0.865UI adjust the RT/FT to generate signal with Eye width≤0.865UI.
	Run TekExpress CPHY-Tx Essentials to perform Eye	
	Diagram measurement.	
2.	Add the C-PHY Reference channel.	
	Refer Figure 2.3.3(b)	
3.	Add the DCD in increments until the Eye width is approximately $\sim 0.5$ LIL and adjust the amplitude	Eye WIDTH reduced to ~0.5UI and Eye
	(Line Levels) to achieve Eye height: +40mVpk. Move	
	the mask horizontally so that it is aligned on the	
	taken care by TekExpress CPHY-Tx Essentials).	Ensure than there are minimal or no Mask hits.
4.	Calibrate for DC Common Mode by adjusting the bias Tee voltage.	$V_{\mbox{\tiny CPTX}}$ based on the test case
	This test is required to be formed for multiple cases of DC common mode voltage.	
	Testcase#1: VCPTX = 250mV	
	Testcase#2: VCPTX = 175mV	
	Testcase#3: VCPTX = 310mV	
	Run TekExpress CPHY-Tx essentials to perform DC common mode measurement.	

- 1. The calibrated stimulus is fed to the DUT.
- 2. Transmit the test sequence to the DUT. Verify via any valid observable that the DUT received the test sequence without errors.
- 3. Repeat the test for all the three cases of DC common mode listed in step 4 of the calibration table above.

**Note**: Low BER will not be verified. Each test case will be performed using a target BER of 1E-10 and a confidence level of 95% (i.e., 3E10 bits). This corresponds to approximately 20 seconds per test case (assuming a bit rate of 3.35Gbps (1.5Gsps), and a line utilization of 50%, i.e., one burst-width of LP between bursts).

#### Observable Results

Verify that for all three test cases that the test sequence was received by the DUT without error.

#### Example Result

Following are the result after each step of the calibration routine described above for a PRBS9 test sequence at symbol rate of 2.5Gbps

1) Differential Eye diagram with Nominal Voltage. Eye width is about 344psec (0.86UI).



2) Slow down the RT/FT and add the reference channel (Legacy channel in this example). Eye width is reduced to 269psec (0.67UI)



3) Add the DCD and adjust amplitude to achieve target eye width and eye height. Eye width is reduced to 215psec (0.53UI).



## **GROUP 4: HS-RX TIMER REQUIREMENTS**

## Test/Calibration Setup

If any of the signal parameters of interest needs calibration, for this purpose the calibration setup should include with termination board. See section <u>LP Signal Calibration Setup</u>.

# Test 2.4.1 – HS-RX T3-TERM-EN Duration

#### Discussion

C-PHY Specification mentions the maximum time within which the slave has to enable HS line termination.

t3-TERM-EN	Time for the slave to enable the HS line termination, starting from the time point when the	Note 5	38	ns	3
	A, B and C whe closs VIL_MAX				

3. Receiver-specific parameter.

- The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.
- As specified in Section 9.2.1, the receiver termination impedances shall not be enabled until the single-ended voltages on all of A, B and C fall below V<sub>TERM-EN</sub>.



Figure: 2.4.1(a) Termination enable duration definition

## Signal parameters

- Signal Mode: LowPower\_HighSpeed
- ➢ HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz
- Low Power: Set LP-000 duration(t3\_PREPARE) = 2 LP symbols(implying Prepare time of 100 nsec)

Signal Mode: Low Power - Hig	µh Speed ▼	
High Speed High Speed Jitter	High Speed Burst	ow Power Low Power Noise High Speed Batch Mode Preferences Compile Settings Log View +
Base pattern		
Pattern ULPS 🔻		
Include LP content in Low P	ower - High Speed (LF	2-HS) Signal Mode
Symbol		Rise/Fall
Symbol Rate 20 MHz	TLPX 50 ns	Rise/Fall time (15%-85%) 0.1 UI = 5 ns
Line Levels (High Impedance)		
High	Low	_
Line A 1V	50 mV	☑ Use Line A levels for Line B and Line C 🕐
Line B 1 V		
Line C 1 V		
LD-HS Entry/Evit timing (Appli	rable in LD-HS Signal	model
Start I P-111 duration	2	IP Symbols - 100 ns
	2	
Enable THS_Exit		
End LP-111 duration		LP Symbols = 100 ns

Figure: 2.4.2(a) LP Tab Configuration

#### Measurement details

The  $T_{3-TERM-EN}$  interval begins at the point where the LP-00 falling edge (on line C) crosses  $V_{IL,MAX}$  (550mV), and ends at the point when the HS line termination is enabled. As described in the CTS, the exact point when HS line termination is considered enabled is subjective. The text in the CTS is reproduced below – "Note that the exact point when the HS line termination is considered "enabled" can be somewhat subjective in some cases, as the voltage spike that typically occurs on the line when the termination is enabled does not necessarily have a well-defined shape (and in some cases may not be visible at all). For the purposes of this test, the measurement point for the termination-enable voltage spike is defined as the maximum voltage point of the spike (as opposed to the 'start' of the spike, which can be even more difficult to clearly identify.) For devices with sufficient margin in their  $T_{3-TERM-EN}$  timer values, the impact of any potential measurement uncertainty should be minimal" [2]

T<sub>3-TERM-EN</sub> interval is measured on the Line C waveform using the cursors as shown below



- 1) Test setup: Similar to other Rx tests the DUT is connected waveform generator. However, the DUT behavior is assessed by measuring the signal captured on an oscilloscope by probing at the Rx pins.
- 2) Generate a LP\_HS waveform with signal parameters listed in the above section.
- 3) Transmit the test sequence to the DUT and capture the signal at the Rx pins on the oscilloscope.
- 4) T<sub>3-TERM-EN</sub> interval is measured on the captured on the line C waveform as described above.

### Observable Results

Verify that  $T_{3-TERM-EN}$  is less than 38ns.

## Test 2.4.2 – HS-RX T3-PREPARE Tolerance

## Discussion

This test is to verify that the DUT's HS-RX can tolerate reception of conformant values for  $T_{3-PREPARE}$ . Shown below is the requirements for  $T_{3-PREPARE}$  interval, which is required to understand switching a lane into HS mode.



Given below are the T<sub>3-PREPARE</sub> interval definition, and conformance limits and test cases will be performed using the TX values maximum of 95 ns and minimum 38 ns.

Table 18 Global Operation Timing Parameters							
Parameter	Description	Min	Max	Unit	Notes		
t3-PREPARE	Time that the transmitter drives the 3-wire LP-000 line state immediately before the HS_+x line state starting the HS transmission.	38	95	ns	2		

## Signal parameters

- Signal Mode: LowPowerHighSpeed
- ▶ HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz
- Low Power: Set LP-000 duration (t3\_PREPARE) to be configured based on the test case. The minimum and maximum t3\_PREPARE is achieved by the configuration shown in Table 2.4.2(b). This setting in the application is shown in Figure 2.4.2(c)
- Nominal burst parameters for the HS burst for this test is listed below and also shown in Figure 2.4.2(b)
  - High Speed Burst: PreBegin Pattern = 3333333.
  - High Speed Burst: PREBEGIN Repeat = 63.
  - High Speed Burst: ProgSeq = Disabled.

- High Speed Burst: PreEnd Pattern = 3333333.
- High Speed Burst: PreEnd Repeat = 0.
- High Speed Burst: SYNC = 3444443.
- High Speed Burst: Sync word Repeat = 7 symbols.
- High Speed Burst: POST pattern = 4444444.
- High Speed Burst: POST Repeat = 224 Symbols.

Signal Mode: Low Po	wer - High Speed 🔻	]							
High Speed High Spee	ed Jitter High Speed	Burst	w Power Lo	ow Power N	loise	High Speed Batch Mode	Preferences	Compile Settings	Log View
🕜 🗹 Create Burst —									
Include High Spec	ad Race Dattern	Dravious	Wire State		7				
		FIEVIOUS	while State	<u>-y</u> .					
Preamble Pattern									
	🗹 PreBegin		Pro	ogSeq		🗹 PreEnd			
Pattern	333333					3333333			
Repeat	63	x 7			x 14	1	x 7		
Preamble Length	448	Symbols							
Note: Preamble len	gth = [(PreBegin Repe	eat * 7) + (I	ProgSeq Rep	eat * 14) + (	(PreEnd	d Repeat * 7)]			
Sync Word	344443	]							
Sync Word Repeat	1	x 7 =		Symbols					
🗹 Post Pattern	444444	]							
Post Pattern Repeat	32	x 7 =	224	Symbols					
Note:									
Preamble, sync and p	ost patterns are each	specified b	y 7 symbols.						
A symbol is defined b	y a value in the range	:: {0,1,2,3,4}							

# Figure: 2.4.2(a) HS Burst settings

Test Case #	T <sub>3-prepare</sub>	LP-000 duration [Setting on CPHYXpress]	Notes
1	38ns	0.8 LP symbols	Minimum T <sub>3-PREPARE</sub>
2	95ns	1.9 LP symbols	Maximum T <sub>3-PREPARE</sub>

Table: 2.4.2(b) T3\_PREPARE configuration values on CPHYXPress

Signal Mode: Low Power - High Speed 🔻	
High Speed High Speed Jitter High Speed Burst L	ow Power Low Power Noise High Speed Batch Mode Preferences Compile Settings Log View
Base pattern	
Pattern ULPS 🔻	
Include LP content in Low Power - High Speed (LP	P-HS) Signal Mode
Symbol	Rise/Fall
Symbol Rate 20 MHz TLPX 50 ns	s Rise/Fall time (15%-85%) 0.1 UI = 5 ns
Produced (Fight Incodered)	
Line Levels (High Impedance) High Low	
Line A 1 V 50 mV	Source Contract State Contract State Contract State St
Line B 1 V 50 mV	
Line C 1 V 50 mV	
LD US Entry/Exit timing (Analisable in LD US Singel)	
Start LP-111 duration 2	LP symbols = 100 ns
LP-000 duration(t3_PREPARE) 1.9	LP Symbols = 95 ns
Enable THS_Exit	
End LP-111 duration 2	LP Symbols = 100 ns

Table: 2.4.2(c) LP tab setting of T3\_PREPARE to achieve a maximum of 95 nsec

- 1. Generate a LP\_HS waveform with signal parameter listed above (for testcase1).
- 2. Verify via any valid observable that the DUT received the test sequence without errors.
- 3. Repeat the above steps for Testcase2.

## Observable Results

Verify via any valid observable that the DUT received the test sequence without errors.

# Example Result

The test waveform with maximum T3\_PREPARE of 95 nsec is shown below.



Figure: 2.4.2(d) Measured 95 ns as maximum t3 Prepare conformance limit
# Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance

#### Discussion

 $T_{3-PREBEGIN}$  has a range of 1 to 64 words that is 7 to 448 UI. The Rx needs to recognize the presence of PREBEGIN for a length within the range specified.



T <sub>LPX</sub>	T <sub>3-PREPARE</sub>	T <sub>3-PROGSEQ</sub>	T <sub>3-PREEND</sub>	T <sub>3-SYNC</sub>	T <sub>3-POST</sub>
50ns	70ns	Disabled (0UI)	701	701	112UI

#### Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: LowPower\_HighSpeed
- HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz, resulting TLPX of 50ns
- Low Power: Set LP-000 duration (t3\_PREPARE) is set to 1.4 symbols to achieve 70ns, which is used as the nominal setting for this test.
- Nominal burst parameters for the HS burst for this test is listed below
  - High Speed Burst: PreBegin Pattern = 3333333.
  - High Speed Burst: PREBEGIN Repeat = 1 (i.e. 7 Symbols)
  - High Speed Burst: ProgSeq = Disabled.
  - High Speed Burst: PreEnd Pattern = 3333333.
  - High Speed Burst: PreEnd Repeat = 1 (i.e. 7 Symbols)
  - High Speed Burst: SYNC = 3444443.
  - High Speed Burst: Sync word Repeat = 1

- High Speed Burst: POST pattern = 4444444.
- High Speed Burst: POST Repeat = 16 (i.e. 224 Symbols)
- High Speed Batch Mode: Parameter-> PreBegin Repeat. Start, end and Increment values are set as shown in the Figure 2.4.3(a).
  - With this setting multiple waveforms are created with increasing lengths of PreBegin.
  - A waveform sequence is created in the AWG, to step through the waveforms for testing with varying PreBegin lengths. Waveform sequence is shown in Figure 2.4.3(b)

Signal Mode:	Low Power - High Spec	eed 🔻		
High Speed	High Speed Jitter High	Speed Burst Low Power	· Low Power Noise	High Speed Batch Mode
🛛 🗹 Enable B	atch Waveform Creation	·		
Parameter	PreBegin_Repeat 💌			
Start	1 w	Vords		
End	64 W	Vords		
Increment	1 w	Vords		
This range o	reates 64 waveform sets.			



Н	Home Setup Waveform Plug-in Sequence Capture/Playback										
CPhySequence Steps used: 64 Total time									:		
Γ.			Comune Cottings			H	emainir	ng: 16319	, -	· 3/s	
Ľ	·ile •		Sequence Settings								
	Wait	Track 1	Track: Flags	1 Track 2	Track 2 Flags	Repeat Count	Event Input	Event Jump te	Go to	Length	Time
1	Off	Test_PreBeginLen_1_Words_15GHz_VA		Test_PreBeginLen_1_Words_15GHz_VB	T T	8	Off		Next	6.12	
2	Off	Test_PreBeginLen_2_Words_15GHz_VA		Test_PreBeginLen_2_Words_15GHz_VB		8	Off		Next	6.19	
3	Off	Test_PreBeginLen_3_Words_15GHz_VA		Test_PreBeginLen_3_Words_15GHz_VB		8	Off		Next	6.26	
4	Off	Test_PreBeginLen_4_Words_15GHz_VA		Test_PreBeginLen_4_Words_15GHz_VB		00	Off		Next	6.33	
5	Off	Test_PreBeginLen_5_Words_15GHz_VA		Test_PreBeginLen_5_Words_15GHz_VB		8	Off		Next	6.40	
6	Off	Test_PreBeginLen_6_Words_15GHz_VA		Test_PreBeginLen_6_Words_15GHz_VB		œ	Off		Next	6.47	
7	Off	Test_PreBeginLen_7_Words_15GHz_VA		Test_PreBeginLen_7_Words_15GHz_VB		œ	Off		Next	6.54	
8	Off	Test_PreBeginLen_8_Words_15GHz_VA		Test_PreBeginLen_8_Words_15GHz_VB		00	Off		Next	6.61	
9	Off	Test_PreBeginLen_9_Words_15GHz_VA		Test_PreBeginLen_9_Words_15GHz_VB		œ	Off		Next	6.68	
10	Off	Test_PreBeginLen_10_Words_15GHz_VA		Test_PreBeginLen_10_Words_15GHz_VB		80	Off		Next	6.75	
11	l Off	Test_PreBeginLen_11_Words_15GHz_VA		Test_PreBeginLen_11_Words_15GHz_VB		œ	Off		Next	6.82	
12	2 Off	Test_PreBeginLen_12_Words_15GHz_VA		Test_PreBeginLen_12_Words_15GHz_VB		œ	Off		Next	6.89	
13	3 Off	Test_PreBeginLen_13_Words_15GHz_VA	L	Test_PreBeginLen_13_Words_15GHz_VB		8	Off		Next	6.96	
14	1 Off	Test_PreBeginLen_14_Words_15GHz_VA		Test_PreBeginLen_14_Words_15GHz_VB		8	Off		Next	7.03	
15	5 Off	Test_PreBeginLen_15_Words_15GHz_VA	\	Test_PreBeginLen_15_Words_15GHz_VB		8	Off		Next	7.10	
16	5 Off	Test_PreBeginLen_16_Words_15GHz_VA	\	Test_PreBeginLen_16_Words_15GHz_VB		œ	Off		Next	7.17	
17	7 Off	Test_PreBeginLen_17_Words_15GHz_VA	L	Test_PreBeginLen_17_Words_15GHz_VB		8	Off		Next	7.24	
18	3 Off	Test_PreBeginLen_18_Words_15GHz_VA	\	Test_PreBeginLen_18_Words_15GHz_VB		œ	Off		Next	7.31	
19	Off	Test_PreBeginLen_19_Words_15GHz_VA		Test_PreBeginLen_19_Words_15GHz_VB		œ	Off		Next	7.38	
20	Off	Test_PreBeginLen_20_Words_15GHz_VA		Test_PreBeginLen_20_Words_15GHz_VB		œ	Off		Next	7.45	
21	l Off	Test_PreBeginLen_21_Words_15GHz_VA	<b>L</b>	Test_PreBeginLen_21_Words_15GHz_VB		00	Off		Next	7.52	
22	2 Off	Test_PreBeginLen_22_Words_15GHz_VA		Test_PreBeginLen_22_Words_15GHz_VB		8	Off		Next	7.59	
23	3 Off	Test_PreBeginLen_23_Words_15GHz_VA		Test_PreBeginLen_23_Words_15GHz_VB		00	Off		Next	7.66	
24	1 Off	Test_PreBeginLen_24_Words_15GHz_VA		Test_PreBeginLen_24_Words_15GHz_VB		8	Off		Next	7.73	
25	5 Off	Test_PreBeginLen_25_Words_15GHz_VA		Test_PreBeginLen_25_Words_15GHz_VB		00	Off		Next	7.80	

Figure: 2.4.3(b) AWG Sequence showing Line A and Line B waveforms in Track1 & Track2 respectively

#### Test Procedure

- 1. Generate a Low Power-High Speed waveform with signal parameter listed above (PREBEGIN Repeat =1) using CPHYXpress.
- 2. Transmit the test sequence to the DUT and Verify via any valid observable that the DUT received the data without errors.
- 3. Increase the PREBEGIN Repeat by 1 (7 symbols), this is done by playing out the next wfm in the AWG sequence. Repeat this process, until the DUT successfully and consistently receives the HS image data without error.
- 4. Record the (PREBEGIN Repeat value x 7) as the DUT's T<sub>3-PREBEGIN</sub> detection threshold in symbols or UI.

#### Observable Results

Verify that the DUT's  $T_{3-PREBEGIN}$  detection threshold is between 1 and 64 words (i.e. that is 7 and 448UI.)

## Test 2.4.4 – HS-RX T3-PROGSEQ Tolerance

#### Discussion

A programmable sequence of 14 symbols ( $T_{3-PROGSEQ}$ ) is allowed as a part of the burst. This test is check for the performance of the Rx in presence of this sequence (shown in the figure below)



#### Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: LowPower\_HighSpeed
- ▶ HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz, , resulting TLPX of 50ns
- Low Power: Set LP-000 duration (t3\_PREPARE) is set to 1.4 symbols to achieve 70ns, which is used as the nominal setting for this test.
- Nominal burst parameters for the HS burst for this test is listed below and also shown in Figure 2.4.4(a)
  - High Speed Burst: PreBegin Pattern = 3333333.
  - High Speed Burst: PREBEGIN Repeat = 16 (i.e. 112 Symbols)
  - High Speed Burst: ProgSeq = Enabled.
  - High Speed Burst: ProgSeq = Enabled, and set to 43434343434343
  - High Speed Burst: PreEnd Pattern = 3333333.
  - High Speed Burst: PreEnd Repeat = 1 (i.e. 7 Symbols)
  - High Speed Burst: SYNC = 3444443.
  - High Speed Burst: Sync word Repeat = 1 (i.e. 7 Symbols)
  - High Speed Burst: POST pattern = 4444444.
  - High Speed Burst: POST Repeat = 16 (i.e. 112 Symbols)

Si	gnal Mode: Low Po	wer - High Speed 🔻	)								
н	ligh Speed High Spee	ed Jitter High Speed	Burst	Low	Power	Low Power	Noise	High	Speed Batch N	lode	Preferences
	🗹 Create Burst 🛛 —										
	_ Include High Spee	d Base Pattern	Previo	us W	/ire State	: <u>-</u> у	•				
	Preamble Pattern										
		🗹 PreBegin			<b>S</b> 1	ProgSeq			🗹 PreEnd		
	Pattern	3333333			434343	43434343	]	3	333333		
	Repeat	16	x 7		1		x 14	1		×	:7
	Preamble Length	133	Symbo	ols							
	Note: Preamble leng	gth = [(PreBegin Repe	eat * 7) -	+ (Pr	ogSeq R	epeat * 14) ·	+ (PreEn	nd Rep	eat * 7)]		
	Sync Word	344443	]								
	Sync Word Repeat	1	) x 7 =			Symbo	ols				
	🗹 Post Pattern	444444	]								
	Post Pattern Repeat	16	) x 7 =	1	.12	Symbo	ols				
	Note:										
Preamble, sync and post patterns are each specified by 7 symbols.											
	A symbol is defined b	y a value in the range	:: {0,1,2,3	3,4}							

Figure 2.4.4(a) High Speed Burst settings

#### *Test procedure*

- 1. Generate a Low Power-High Speed waveform with signal parameter listed above using CPHYXpress.
- 2. Transmit the test sequence to the DUT and Verify via any valid observable that the DUT received the data without errors

### Test 2.4.5 – HS-RX T3-POST Tolerance

# [This test is similar to Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance. In this test tolerance of the Rx with regard to the length of the Post ( $T_{3_POST}$ ) is checked for]

#### Discussion

The range for the length of the POST sequence is defined as 7 to 224 UI.

#### Signal parameters

The setting are similar to that in Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance, with now focus on the Post length

- Signal Mode: LowPower-HighSpeed
- ▶ HS Base Pattern: PRBS9\_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz, resulting TLPX of 50ns
- Low Power: Set LP-000 duration (t3\_PREPARE) is set to 1.4 symbols to achieve 70ns, which is used as the nominal setting for this test.
- Nominal burst parameters for the HS burst for this test is listed below and also shown in Figure 2.4.2(b)
  - High Speed Burst: PreBegin Pattern = 3333333.
  - High Speed Burst: PREBEGIN Repeat = 16 (i.e. 112 Symbols)
  - High Speed Burst: ProgSeq = Disabled.
  - High Speed Burst: PreEnd Pattern = 3333333.
  - High Speed Burst: PreEnd Repeat = 1 (i.e. 7 Symbols)
  - High Speed Burst: SYNC = 3444443.
  - High Speed Burst: Sync word Repeat = 1
  - High Speed Burst: POST pattern = 4444444.
  - High Speed Burst: POST Repeat = 1 (i.e. 7 Symbols)
- High Speed Batch Mode: Parameter-> Post Repeat. Start, end and Increment values are set as shown in the Figure 2.4.3(a).
  - With this setting multiple waveforms are created with increasing lengths of Post.
  - A waveform sequence is created in the AWG, to step through the waveforms for testing with varying Post lengths. Waveform sequence is shown in Figure 2.4.3(b)

Signal Mode:	Low Power - Hi	gh Speed 🔻			
High Speed	High Speed Jitter	High Speed Burst	Low Power	Low Power Noise	High Speed Batch Mode
🛛 🖂 Enable B	Batch Waveform Cr	eation			
Parameter	Post_Repeat				
Start	i	Words			
End	32	Words			
Increment	1	Words			
This range of	creates 32 wavefor	m sets.			

Test Procedure

Refer to Test Procedure in Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance

# Appendix A – Supported list of tests

Test Number	Test Name	Supported
Test 2.1.1	LP-RX Logic 1 Input Voltage (VIH)	Yes
Test 2.1.2	LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	Yes
Test 2.1.3	LP-RX Input Hysteresis (VHYST)	Yes
Test 2.1.4	LP-RX Minimum Pulse Width Response (TMIN-RX)	Yes
Test 2.1.5	LP-RX Input Pulse Rejection (eSPIKE)	Yes
Test 2.2.1	LP-RX Initialization period (TINIT)	Yes
Test 2.2.2	ULPS Exit: LP-RX TWAKEUP Timer Value	Yes
Test 2.2.3	LP-RX Invalid/Aborted Escape Mode Entry	Yes
Test 2.2.4	LP-RX Invalid/Aborted Escape Mode Command	Yes
Test 2.2.5	LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits	Yes
Test 2.2.6	LP-RX Escape Mode Unsupported/Unassigned Commands	Yes
Test 2.3.1	HS-RX Amplitude Tolerance (VCPRX(DC), VIHHS, VILHS)	Yes
Test 2.3.2	HS-RX Differential Input High/Low Thresholds (VIDTH, VIDTL)	Yes
Test 2.3.3	HS-RX Jitter Tolerance	Yes
Test 2.4.1	HS-RX T3-TERM-EN Duration	Yes
Test 2.4.2	HS-RX T3-PREPARE Tolerance	Yes
Test 2.4.3	HS-RX T3-PREBEGIN Tolerance	Yes
Test 2.4.4	HS-RX T3-PROGSEQ Tolerance	Yes
Test 2.4.5	Test 2.4.5 HS-RX T3-POST Tolerance	Yes

# Appendix B – Measurement Guidance

For measuring various parameters of the signal being calibrated/captured from the device, the oscilloscope needs to be set for an appropriate trigger setting. The following parameters would decide the selection of the trigger type

- 1) Signal Type: HS only signal or LP only signal or Burst waveform(LP\_HS)
- 2) Waveform region of interest

For capturing a burst waveform, one of the trigger type that is suitable is 'transition trigger'. For HS\_only and LP\_only waveforms, the default Edge trigger would serve the purpose.