Method of Implementation
for
MIPI® C-PHY℠ Receiver Conformance Tests

MOI Document Version 1.2

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- Worldwide, visit www.tek.com to find contacts in your area

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C-PHY Receiver Setup and Configuration

Required instruments and accessories

Part Number/Model	Description	Quantity
AWG70002A	25Gs/sec 2-Channel AWG	2
AWGSYNC01	AWG Sync Hub	1
MDC4500-4B	Combiner Box	1
P7380A/P7313	Z-Active™ Differential Probe	3
MIPI CPHY/DPHY Termination Board	MIPI CPHY/DPHY Termination Board	1
174-5771-00	Phase Matched SMA Cable pairs [One Meter Green Cables]	2
DPO70000 series	Real-time scope for Calibration. Bandwidth 6GHz or higher based on the operating symbol rate.	1

Required software

Name	Description
CPHYXpress	AWG based software for Signal Generation
TekExpress C-PHY Tx Essentials	Oscilloscope application for C-PHY clock recover and eye diagram measurements
DPOJET Opt DJA	Jitter, Noise and Eye Diagram Analysis tool

Test setups

1. *Receiver Test Setup*

Figure1 below shows the functional block diagram of the Rx test setup. This is the test setup is used for the all the measurements except noted otherwise.

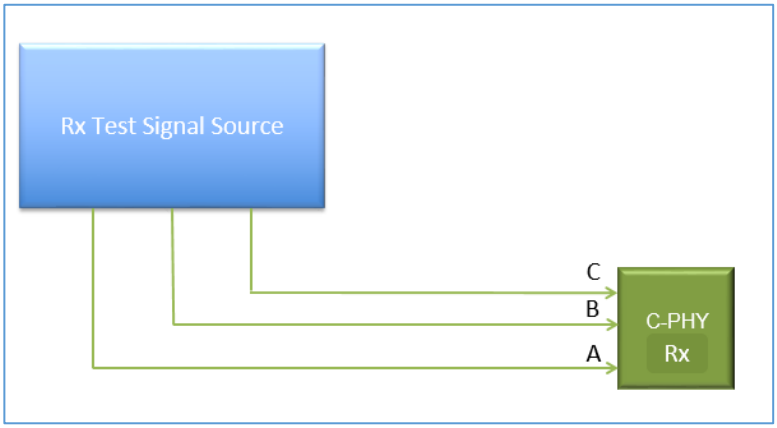


Figure 1: Rx Test Setup - Functional Diagram

2. *HS Signal Calibration Setup*

Figure2 below shows the functional block diagram of the setup for HS signal calibration

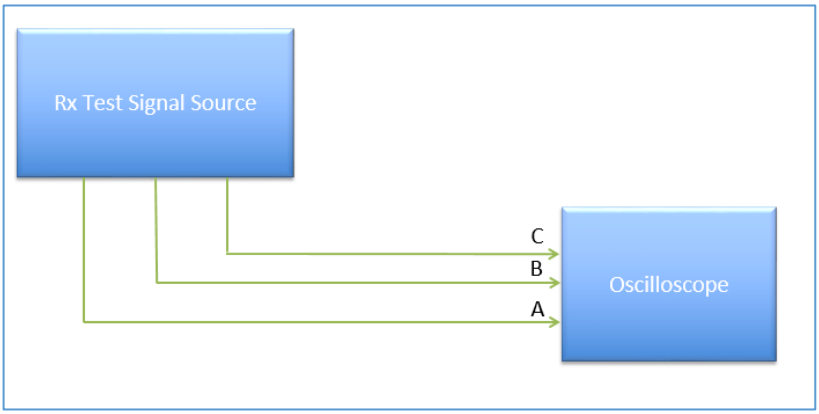


Figure 2: HS Signal Calibration Setup - Functional Diagram

3. *LP Signal Calibration Setup*

Figure3 below shows the functional block diagram of the setup for LP signal calibration.

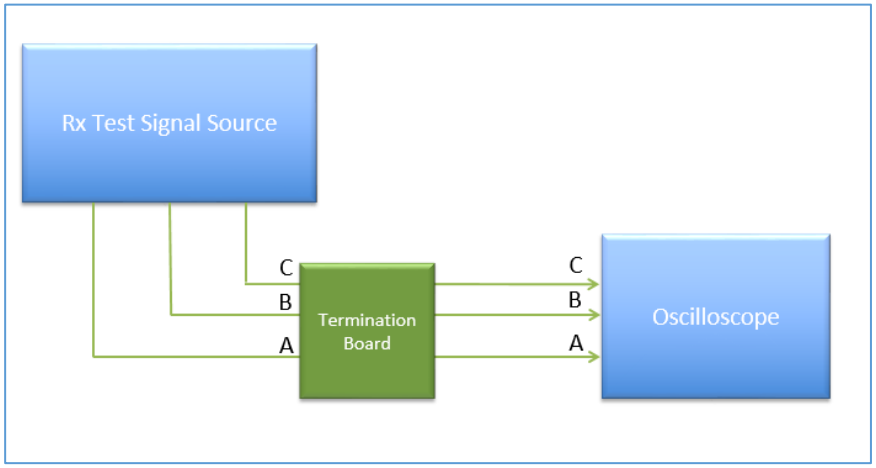


Figure 3: LP Signal Calibration Setup - Functional Diagram

Configuring the Test Setup

The high level block diagram of the receiver test setup is shown below in Figure4.

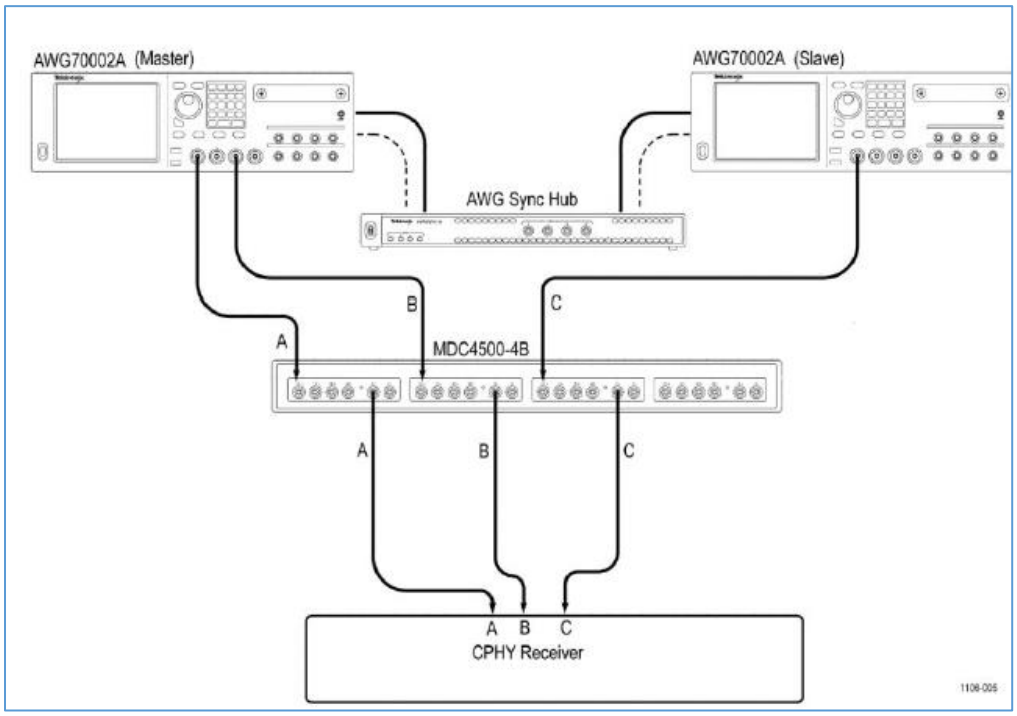


Figure 4: High-level Block Diagram - C-PHY Receiver test setup

Steps to configure the test setup

1. AWGs, Sync Hub and MDC Setup (Back panel connections)
2. Calibrate (de-skew) the AWG channels – **First time only**
3. Signal connection to the DUT
4. Enable Master & Slave AWG

1. *AWGs, Sync Hub and MDC Setup (Back panel connections)*

The back panel connections of the setup are listed and shown in the schematic Figure 5.

a) Connect USB B type AWG-A Port of MDC box to Host USB port of Master AWG using USB cable.

b) Connect USB B type AWG-B Port of MDC box to Host USB port of Slave AWG using USB cable.

c) Connect Clock-out from the Master AWG to the 'Clock-in from Master AWG' port of Sync hub using blue cable.

d) Connect Clock-in from the Slave AWG to the 'Clock-out to AWG clock-in' port of Sync hub using blue cable.

e) Connect Sync to AWG port slot 1 to Sync to Hub port of Master AWG using orange cables.

f) Connect Sync to AWG port slot 2 to Sync to Hub port of Slave AWG using orange cables.

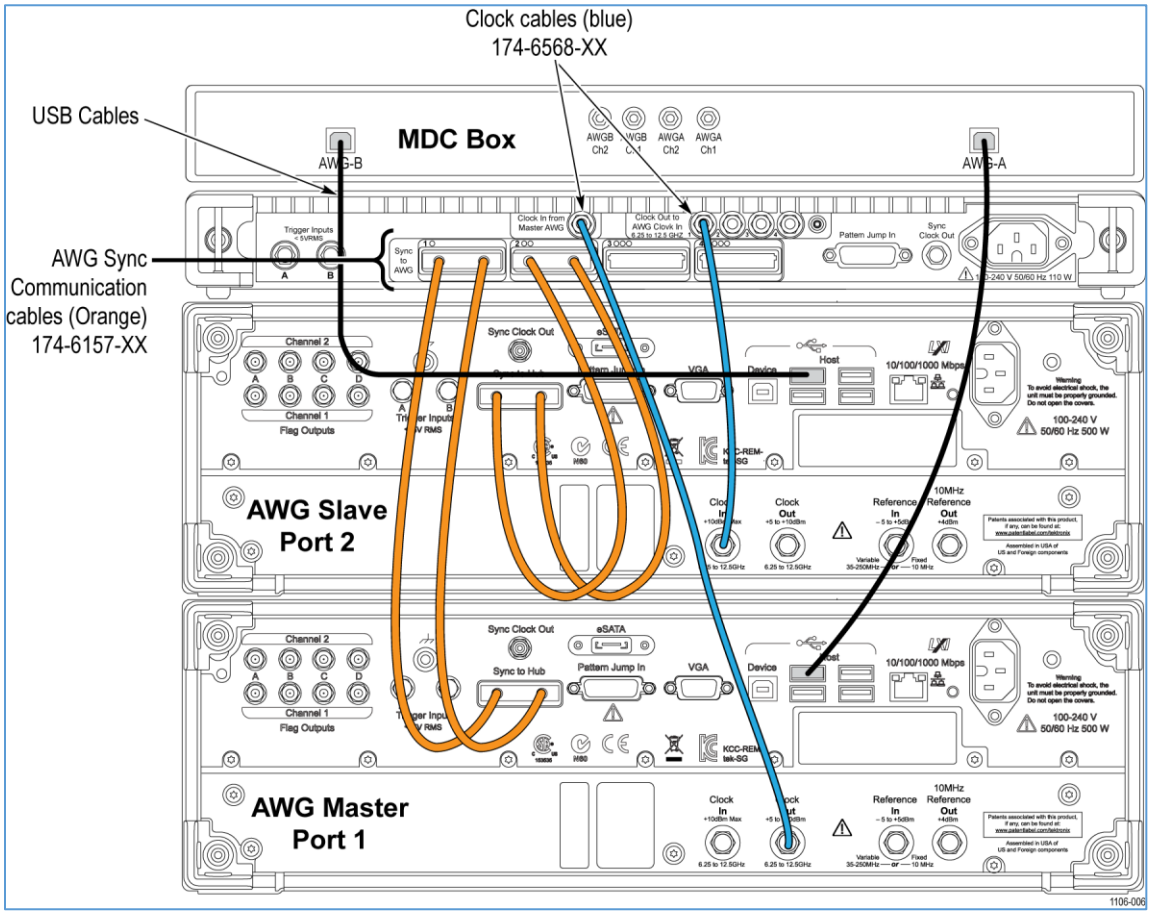


Figure 5: Back panel connection of AWGs, Sync Hub and MDC

2. *Calibrate (de-skew) the AWG channels*

Note: This is required when you first set up the instruments or whenever you make any configuration change in the hardware setup only

This procedure aligns the channel 1 outputs of all connected and enabled instruments to within ±10 ps of each other. You should run the de-skew process when you first set up the instruments, and whenever you make any configuration change, such as replacing an AWG, swapping an AWG within the same configuration, changing the de-skew cables, or changing the Master AWG.

Prerequisites:

- All instruments are connected to the AWGSYNC01 (see section *Back panel connections*).
- All Slave AWG instruments have been enabled (from each Slave instrument and from the Master instrument).
- The de-skew calibration cables are connected as shown in the following diagram.

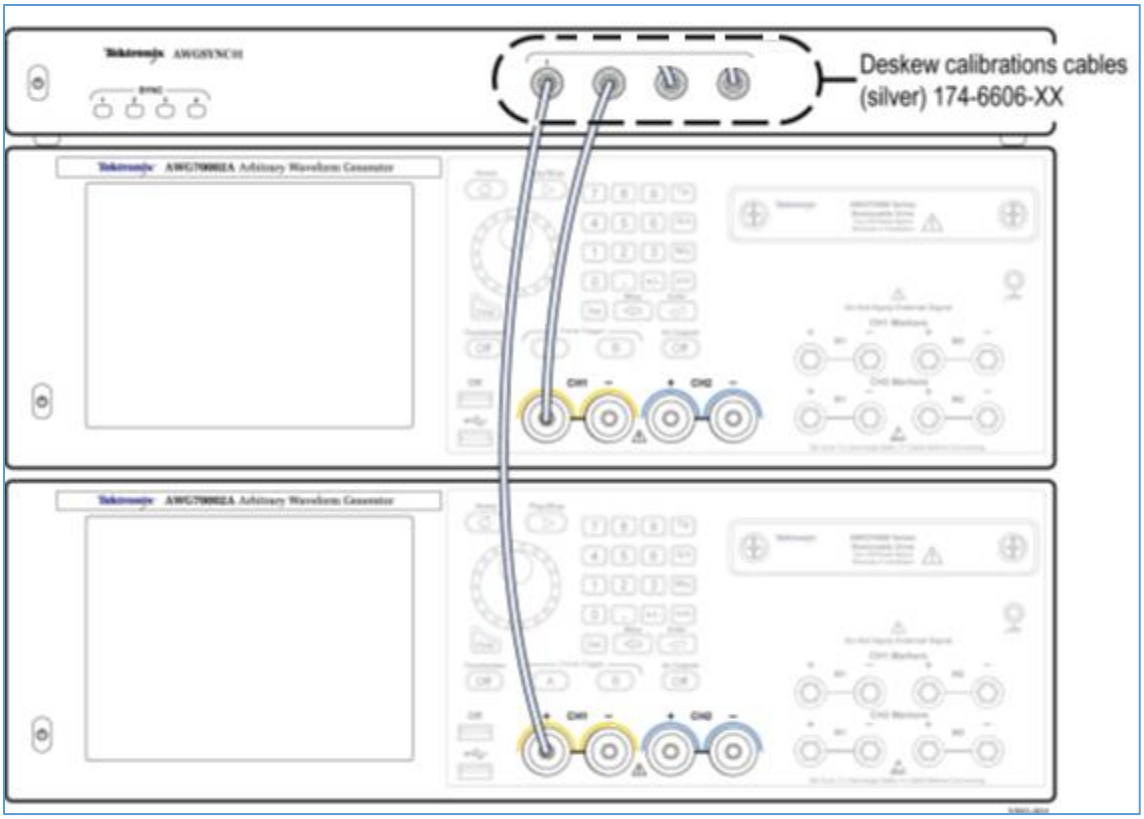


Figure 6: Connect the calibration de-skew cables (front panel)

1. Use the supplied matched silver calibration cables to connect the Calibration ports on the front of the AWGSYNC01 to the same CH1+ or CH1– output on all AWG Master and Slave instruments. The order of the connections is important. Connect Calibration Port 1 to the CH1 output on the

Master AWG instrument, connect Calibration Port 2 to the CH1 output on the Port 2 AWG Slave instrument, and so on. You can use CH1– for de-skew if you connect to the CH1– output on all instruments. The following diagram shows the calibration cables connected to the CH1+ outputs on all AWG instruments.

2. Allow all instruments to warm up for 20 minutes.
3. Enable the Slave AWG instruments (see Enable the Slave AWG instruments).
4. Configure the Master AWG (see Configure the Master AWG).
5. Click Setup > De-skew Calibration on the Master AWG. An in-progress dialog is shown on all instruments while running the calibration. De-skew calibration takes approximately 20 to 30 minutes if using the Master AWG as the clock source, or about a minute if using an external clock source (see De-skew and clock source below).

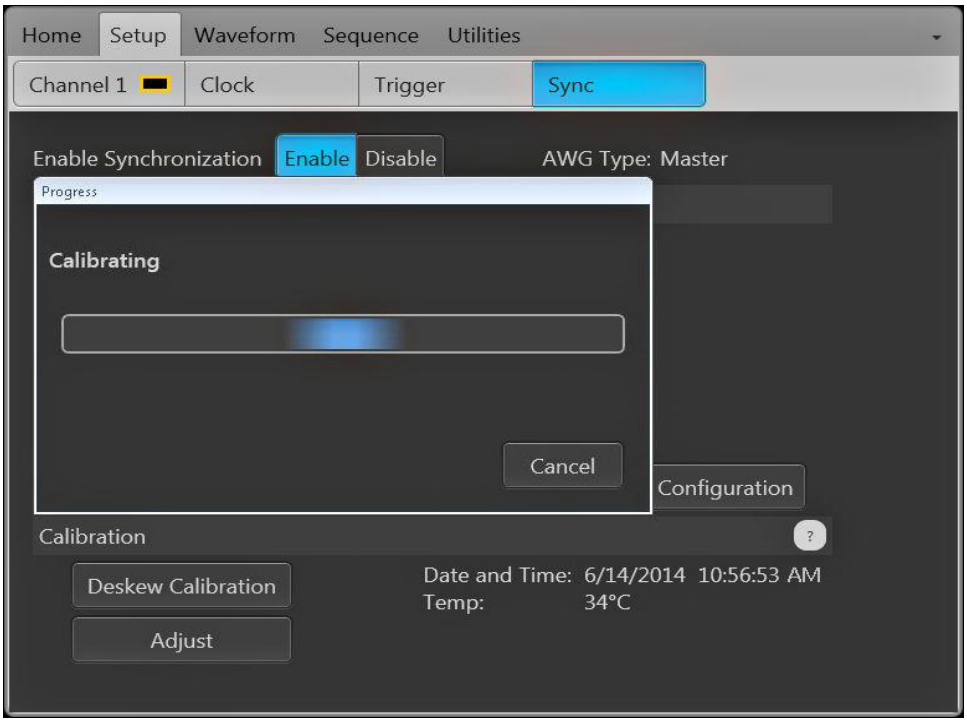


Figure 7: Deskew calibration settings of AWG

6. The Master AWG saves the deskew calibration settings at the completion of the calibration process, and displays the date, time, and instrument temperature of the most-recent successful calibration process.

3. *Signal connections to the DUT*

a) AWG to MDC connections:

Using the blue cables and attenuators supplied along with MDC4500-4B, make the following connections from the AWG channel outputs to the Input ports of the MDC box.

From AWG		To MDC Box	
Master AWG	Ch1+	Inputs from AWG_A Ch1	Ch+
	Ch1-	Inputs from AWG_A Ch1	Ch-
	Ch2+	Inputs from AWG_A **Ch2**	Ch+
	Ch2-	Inputs from AWG_A **Ch2**	Ch-
Slave AWG	Ch1+	Inputs from **AWG_B** Ch1	Ch+
	Ch1-	Inputs from **AWG_B** Ch1	Ch-

b) MDC to DUT connections:

Using SMA cables connect the outputs from the MDC box to the Rx DUT as listed in table below

From MDC		To Rx DUT
A Ch1 Outputs	D+	Line A of Rx
A Ch2 Outputs	D+	Line B of Rx
B Ch1 Outputs	D+	Line C of Rx

Note: If there is a need to increase rise time of signal, then there is a provision to include Rise time filter additionally in signal path between MDC and C-PHY Receiver. Typically, it starts with 100 ps. [Part Number PSPL 5915 Opt 100ps – 100ps Filter (SMA Male to SMA Male)]

4. *Enable Master & Slave AWG*

a) Enable the Slave AWG instrument

Prerequisite: All instruments are connected to the AWGSYNC01. (See AWGs, Sync Hub and MDC Setup (Back panel connections) section)

1. Open the UI of a Slave AWG instrument.
2. Click the **Setup** tab.
3. Click the Sync tab.
4. Select **Enable** to make the AWG accessible for synchronization with the Master AWG.

b) Configure the Master AWG

Prerequisite: Connected Slave AWG instruments have been enabled for synchronization. (See section *Enable the Slave AWG instruments*.)

1. Open the UI of the Master AWG.
2. Click the **Setup** tab.
3. Click the Sync tab.
4. Click Enable.

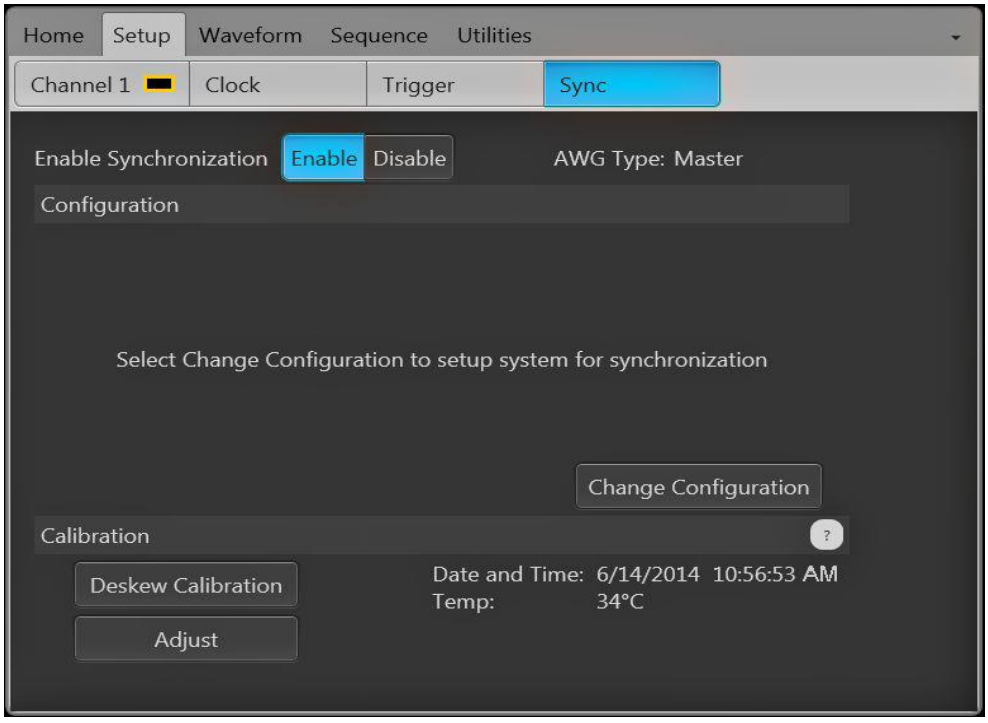


Figure 8: Sync configuration settings of AWG

5. Click **Change Configuration**. Select the slave ports to enable.

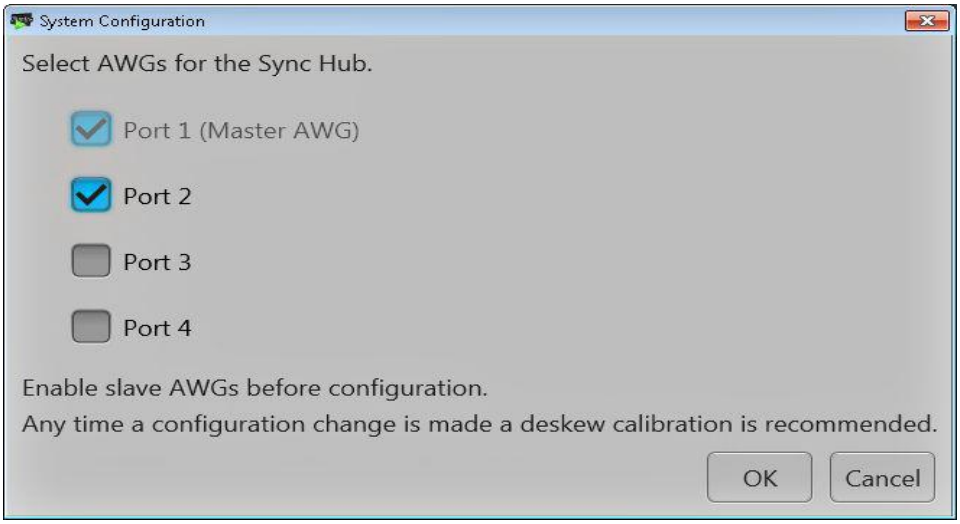


Figure 9: Sync configuration settings of AWG to configure Master and Slave AWG

6. Click **OK**. The Master AWG instrument connects to the selected Slave AWG instruments and displays the connections on the Sync tab screen. If the Master AWG cannot connect to a Slave AWG, the Master shows an error message after a minute or so.

Signal Calibration Procedure

Voltage (VIH/VIL) Calibration Procedure

This procedure enables the outputs of all channel of instruments to be within ±5 % of expected value.

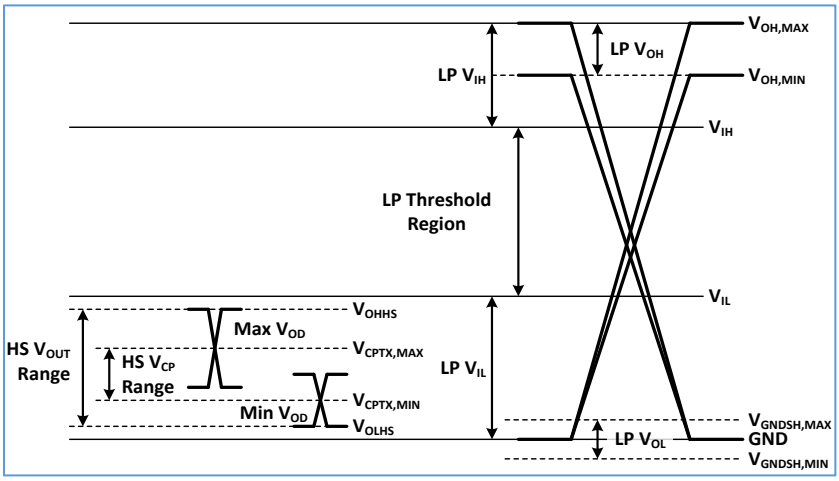


Figure: C-PHY Signaling Levels

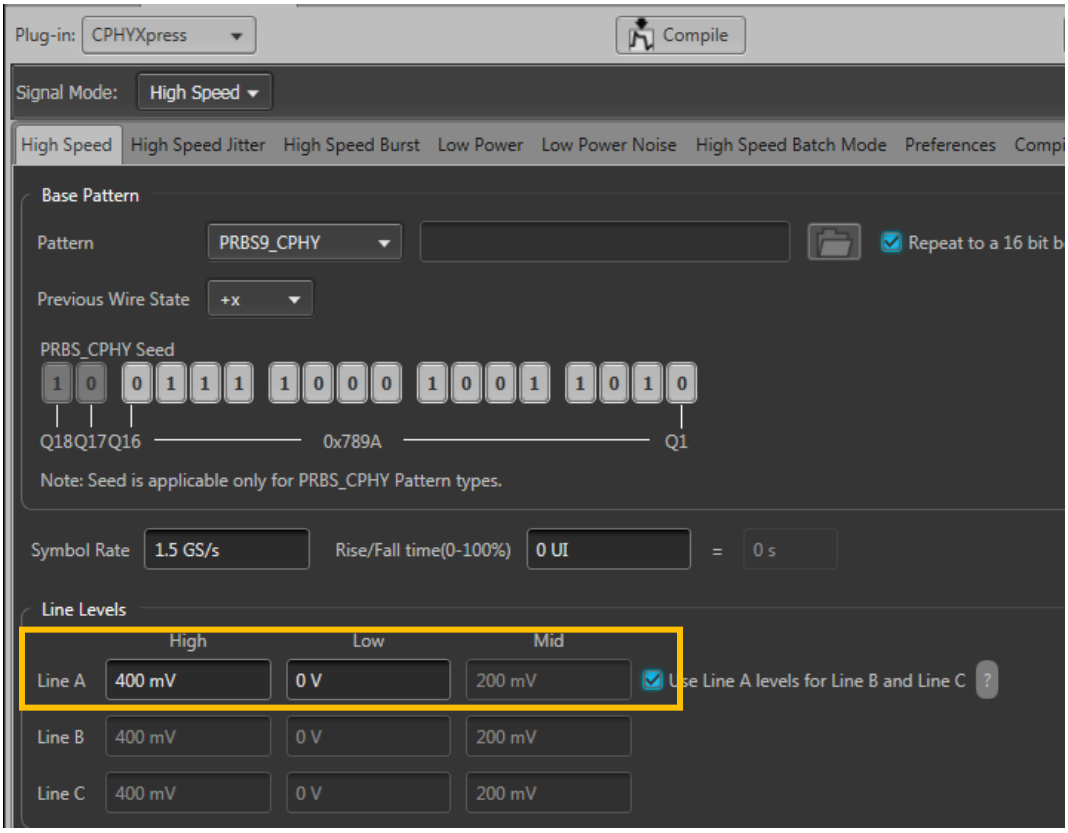


Figure 10: CPHYXpress High Speed configuration tab

Steps to calibrate high and low voltage level

1. Create a C-PHY signal using a test pattern, using nominal High and Low voltage levels.
2. Measure the VIH/VIL using scope Max and Min measurements as shown in the screen shot below.
3. Modify VIH/VIL, till the desired level of voltages are measured on the scope

Figure 11: VIH/VIL measurement

Batch Mode or on the fly differential and common mode voltage level control

Alternatively user can adjust or sweep differential and common mode swing by using the following controls on each of the channel of the AWG as shown in the screen shot below

1) Common mode level by setting the **Offset control**
2) Differntail level by setting **Amplitude control**

With this approach the voltages can will be varied on the fly with no need of generating additional waveforms.

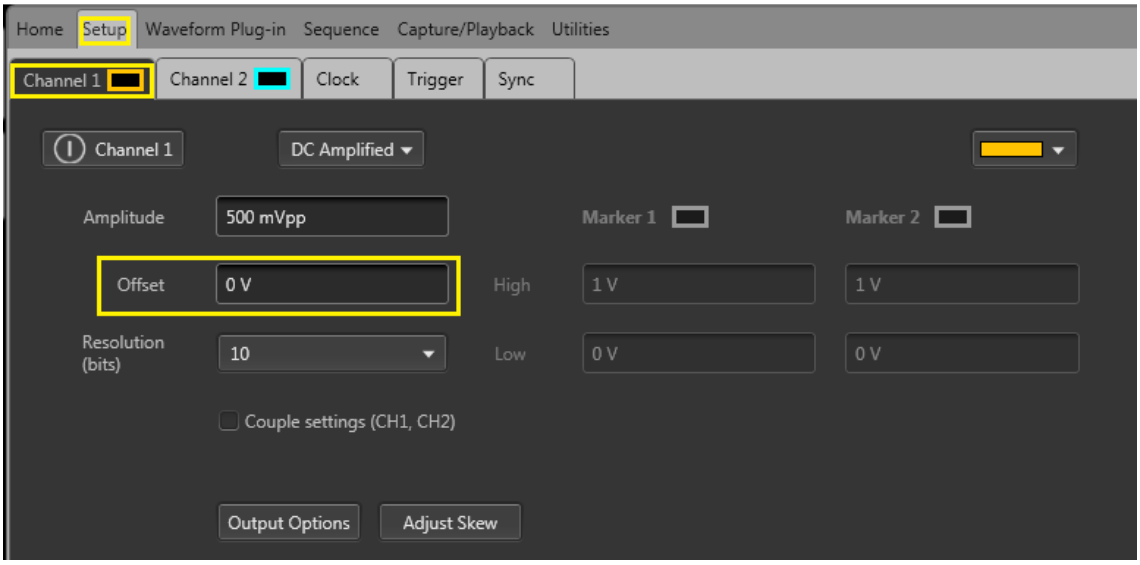


Figure 12: AWG screen shot to show how to change offset/amplitude

Jitter/Timing Calibration

The procedure for calibration jitter is cover in Test 2.3.3

Correct for Amplitude non-linearity using Correction (*.corr) file

Note: Recommended for higher operating data rate

While testing a Device under test, you need to make sure the test equipment generating the signals is of better quality than the Device under Test. The signal generators, Arbitrary Waveform Generators (AWGs) require the generation of waveforms with flat amplitude and linear phase response in the band of interest. This means that the influence of the AWGs and the cables on the signals which could distort the signals should be de-embedded from the signals before sending it to the DUT. For example, of signal trace is running from AWG to DUT thorough MDC, the MDC channel effect also will be in consideration while de-embedding channel effect of signal trace from AWG to DUT.

For a detailed procedure to create a correction file, refer to Help Document of the *Generic Precompensation* plug-in application. Correction file can be applied to any waveform in the AWG waveform list. By default, correction file feature is disabled.

To apply correction, enable "Apply correction file" in the Compile Settings tab. The slave correction file controls will be enabled only if the slave is enabled on the 'Compile Settings' tab.
User can select correction file for each channel using the browse button. The correction file will be applied only for those channel waveforms, which are enabled in the application.

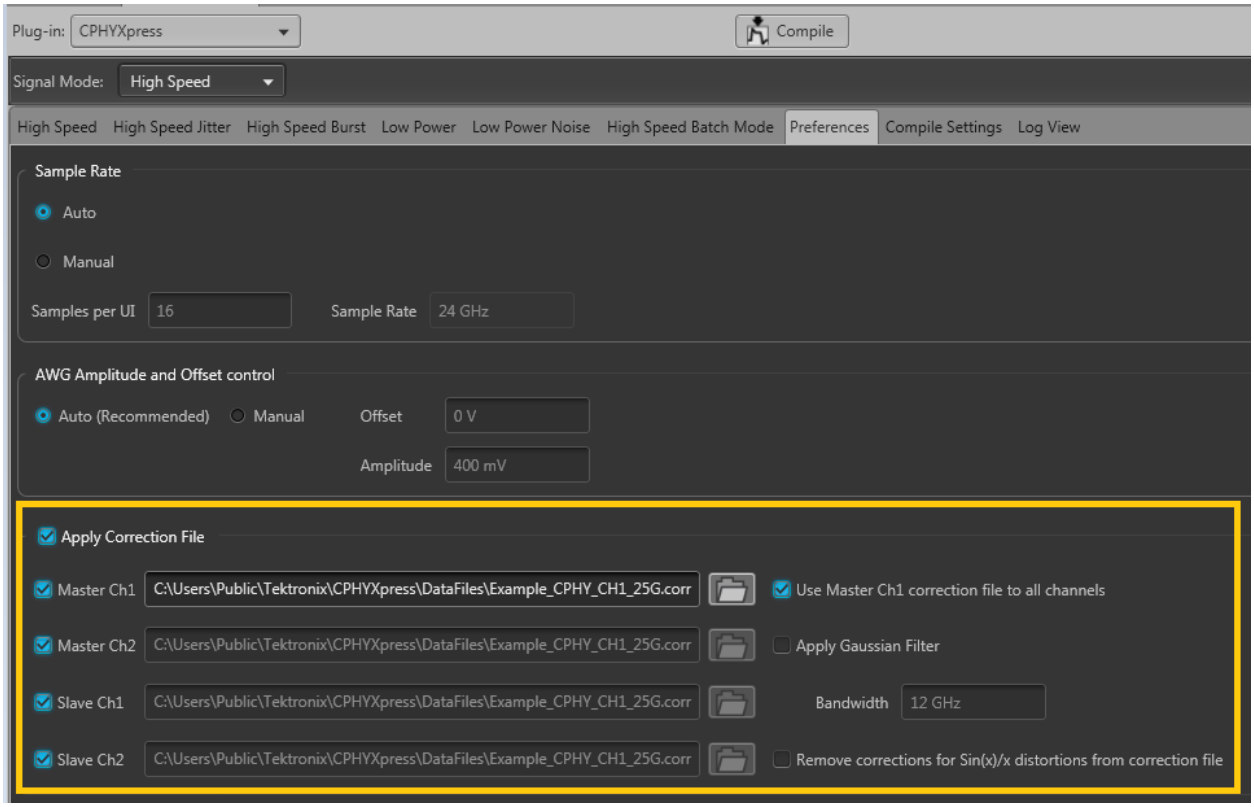


Figure: Correction file configuration using preference tab

References

[1] Specification for C-PHY℠, Version 1.1, 07 October 2014

[2] DRAFT Conformance Test Suite for C-PHY℠ v1.0 and v1.1, Version 1.0 Revision 01, 29 February 2016

[3] Specification for C-PHY℠, Version 1.0, 05 August 2014

[4] Conformance Test Suite for C-PHY℠ v1.0, Version 1.0, 12 February 2016

GROUP 1: LP-RX VOLTAGE AND TIMING REQUIREMENTS

Test/Calibration Setup

If any of the parameters of the LP signal synthesized needs calibration, then the setup with termination board is to be employed. See section LP Signal Calibration Setup .

Test 2.1.1 – LP-RX Logic 1 Input Voltage (V_{IH})

Discussion

C-PHY Specification defines the minimum Logic 1 input voltage (V_{IH}) as 740 mV. This test verifies if the DUT can detect logic level at least at this voltage specified.

Table 28 LP Receiver DC specifications {copy of D-PHY Table 22}

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IH}	Logic 1 input voltage	740			mV	

Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: Low Power
- Low Power: Base Pattern: ULPS or based on the DUT
- Low Power: Symbol rate = 20MHz
- Low Power: Line Level – High=1.2 V, Low = 0V.

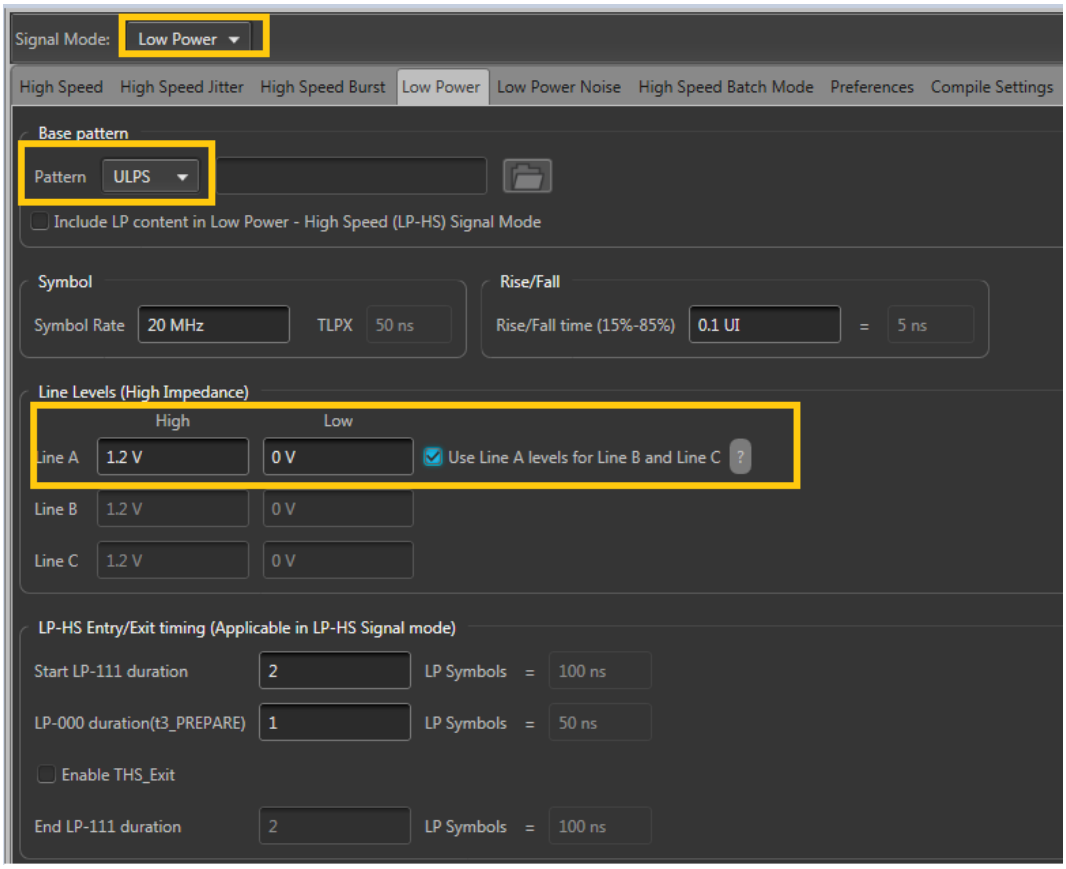


Figure: 2.2.1(a) Low Power Tab configurations

Measurement details

The following measurements on DPOJET can be used to verify VIH and VIL respectively on all line A,B and C – 1) Ampl->High and 2) Ampl->Low.

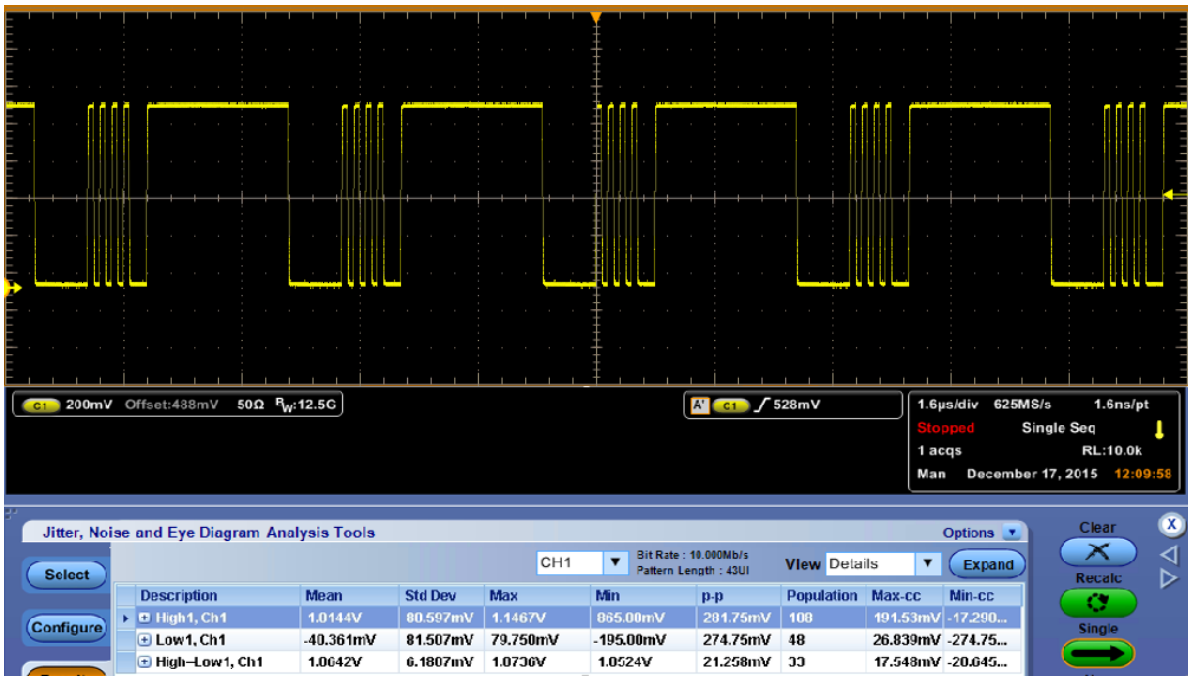


Fig: 2.1.1(b) LP-High and low voltage of Logic 1

Test Procedure

1. Generate a LP waveform with signal parameters listed in the above section.
2. Transmit the test sequence to the DUT and Verify via any valid observable that the DUT received the data without errors.
3. Decrease the LP Line level: high for all the lines by say 50 mV.
4. Repeat steps 1, 2 & 3 till the observable shows an error.
5. At this point note record the highest value of Line level: High at which the DUT consistently received the test sequence without errors. This represent the DUT's LP-RX Logic-1 Detection Threshold, V_{IH}.

Observable Results

Verify the notes VIH is =< 740 mV for all lines A, B and C.

Test 2.1.2 – LP-RX Logic 0 Input Voltage, Non-ULP State (V_{IL})

[This test is similar to Test 2.1.1 –LP-RX Logic 1 Input Voltage (VIH). In this test Logic 0 input threshold conformance is checked for]

Discussion

C-PHY Specification defines the maximum Logic 0 input voltage (V_{IL}) as 550 mV. This test verifies if the DUT can detect logic level at least at this voltage specified.

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IH}	Logic 1 input voltage	740			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	

Signal parameters

Refer to Test 2.1.1.

Measurement details

Refer to Test 2.1.1.

Test Procedure

[The test procedure is similar to Test 2.1.1]

1. Generate a LP_HS waveform with signal parameters listed in the above section.
2. Transmit the test sequence to the DUT and Verify via any valid observable that the DUT received the data without errors
3. Increase the LP Line level: Low for all the lines by say 50 mV
4. Repeat steps 1 ,2 & 3 till the observable shows an error.
5. At this point note record the highest value of Line level: High at which the DUT consistently received the test sequence without errors. This represent the DUT's LP-RX Logic-1 Detection Threshold, V_{IL}

Observable Results

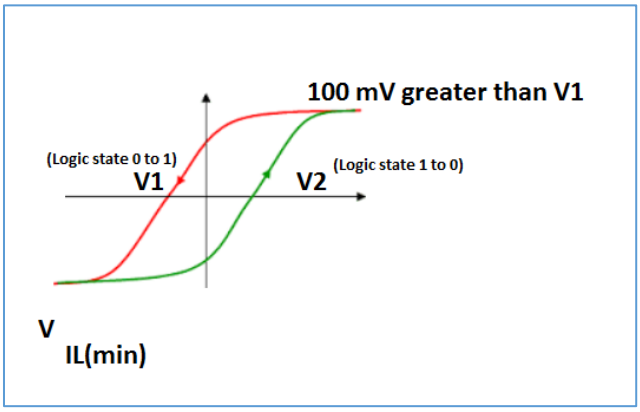
Verify that noted V_{IL} is => 550 mV.

Test 2.1.3 – LP-RX Input Hysteresis (V_{HYST})

Discussion

C-PHY includes a specification for V_{HYST}, or Input Hysteresis to check for the noise sensitivity of the LP receiver. The CTS describes in detail two methods to test for this specification – (1) Static Method and (2) Dynamic Method using additive noise.

Static method is pictorially represented by the graphic below



Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: Low Power
- Low Power: Base Pattern: ULPS or based on the DUT
- Low Power: Symbol rate = 20MHz
- Low Power: Line Level – High=1.2 V, Low = 0V.
- Low Power Noise: Sine Noise Enabled, Amplitude =0V, Frequency = 450MHz. [Dynamic Method]

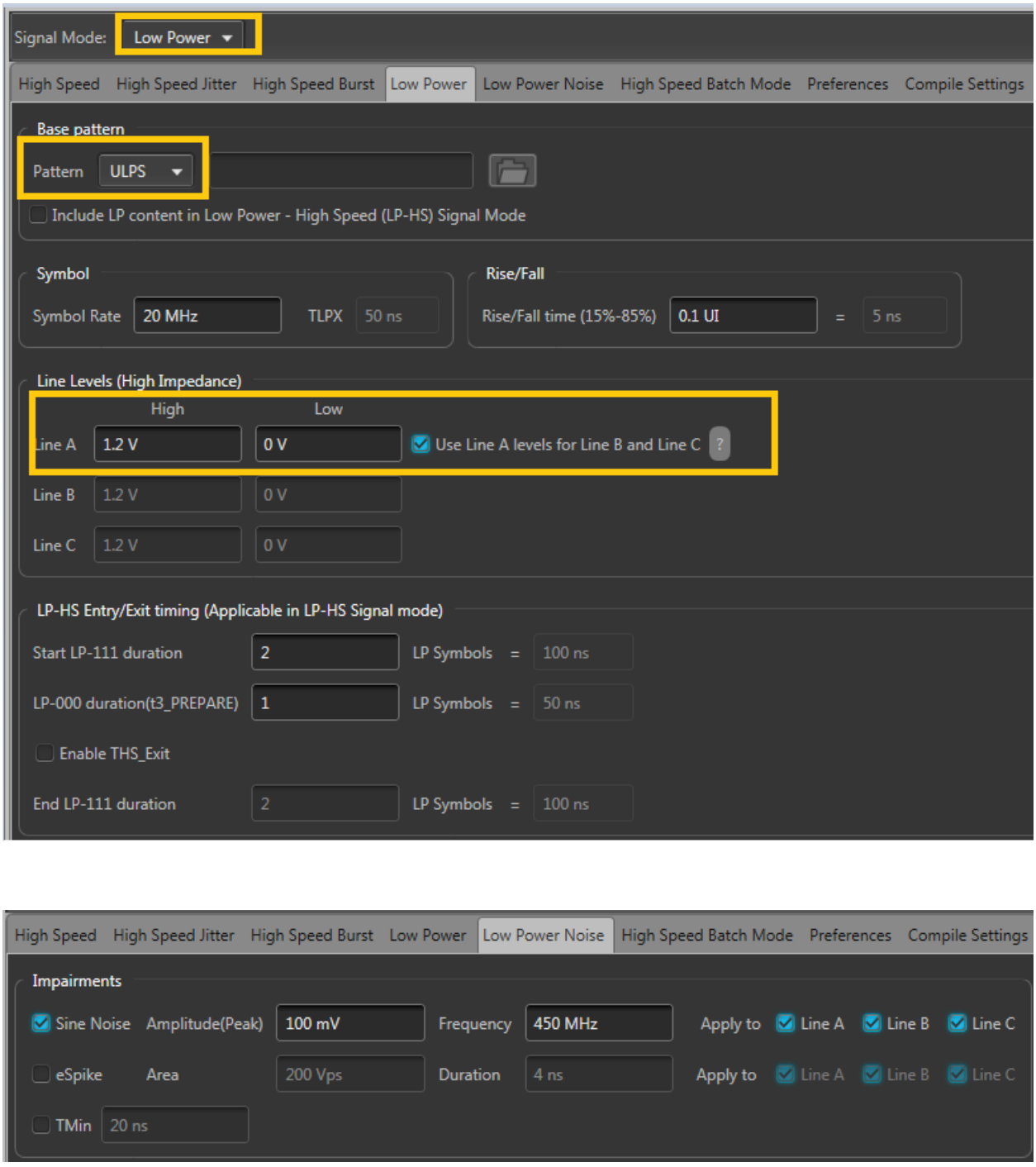


Figure: 2.1.3(a) Low power noise configurations

Test Procedure

(Option 1: Static Method):

1. Generate a LP waveform with signal parameters listed in the above section.
2. Slowly increase the Low level on CPHYXpress application to the point where the DUT's reported internal LP logic states change from LP-0 to LP-1 for VA, VB, and VC, and record the voltages as V1(VA), V1(VB), and V1(VC).
3. Continue to increase low level to approximately 100 mV beyond V1. Then begin slowly decreasing the High level, while still monitoring the reported internal LP logic state (which should still be reported as LP-1 for VA, VB, and VC).
4. Continue decreasing High level until the reported internal LP logic states for VA, VB, and VC change from LP-1 to LP-0. Record these voltages as V2(VA), V2(VB) and V2(VC).
5. Compute the V_{IH} hysteresis for the VA line as $V_{HYST\text{-}VIH}(VA) = V1(VA) – V2(VA)$.
6. Compute the V_{IH} hysteresis for the VB line as $V_{HYST\text{-}VIH}(VB) = V1(VB) – V2(VB)$.
7. Compute the V_{IH} hysteresis for the VC line as $V_{HYST\text{-}VIH}(VC) = V1(VC) – V2(VC)$.
8. Repeat the above procedure a second time (but starting from a nominal LP-1 level of 1200mV, and working downward) to measure the VIL hysteresis for VA, VB, and VC, i.e., $V_{HYST\text{-}VIL}(VA)$, $V_{HYST\text{-}VIL}(VB)$, and $V_{HYST\text{-}VIL}(VC)$. (Note however in this case VHYST will be computed as $|V1 – V2|$.)

(Option 2: Dynamic Method)

1. Generate a LP waveform with signal parameters listed in the above section. Set the High and Low levels that were measured in Tests 2.1.1 and 2.1.2, respectively
2. Verify via any valid observable that the DUT received the data without errors.
3. With the additive noise source disabled, transmit the test sequence the DUT, and verify via any valid observable that the DUT received the data without errors.
4. Repeat the previous step, but with the additive noise source enabled for the V_A line, using a noise voltage of approximately 5mVpk. Again, verify via any valid observable that the DUT received the data without errors.
5. Repeat the previous step multiple times, slowly increasing the additive noise voltage in 3-5 mV steps, until the point is reached where the DUT begins to report errors in the received test sequence.
6. Record $V_{HYST\text{-}VIH}(V_A)$ and $V_{HYST\text{-}VIL}(V_A)$ as the maximum additive noise voltage where the test sequence was consistently received without error.
7. Repeat the above procedure for the V_B line to determine $V_{HYST\text{-}VIH}(V_B)$ and $V_{HYST\text{-}VIL}(V_B)$.
8. Repeat the above procedure for the V_C line to determine $V_{HYST\text{-}VIH}(V_C)$ and $V_{HYST\text{-}VIL}(V_C)$.

Observable Results

Verify that all the following determined values is greater than or equal to 25mV.

1) $V_{HYST\text{-}VIH}(V_A)$
2) $V_{HYST\text{-}VIH}(V_B)$
3) $V_{HYST\text{-}VIH}(V_C)$
4) $V_{HYST\text{-}VIL}(V_A)$
5) $V_{HYST\text{-}VIL}(V_B)$
6) $V_{HYST\text{-}VIL}(V_C)$

Test 2.1.4 – LP-RX Minimum Pulse Width Response (T_{MIN-RX})

Discussion

The make the LP receiver robust, one of the parameter defined is the Minimum pulse width response T_{MIN-RX}(20 nsec), which defines the minimum-duration LP pulse width that should still be detected as a valid LP state by an LP receiver.

Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: Low Power
- Low Power: Base Pattern: ULPS or based on the DUT
- Low Power: Symbol rate = 20MHz
- Low Power: Line Level – High=1.0 V, Low = 0V.
- Low Power Noise: TMIN = 30 nsec

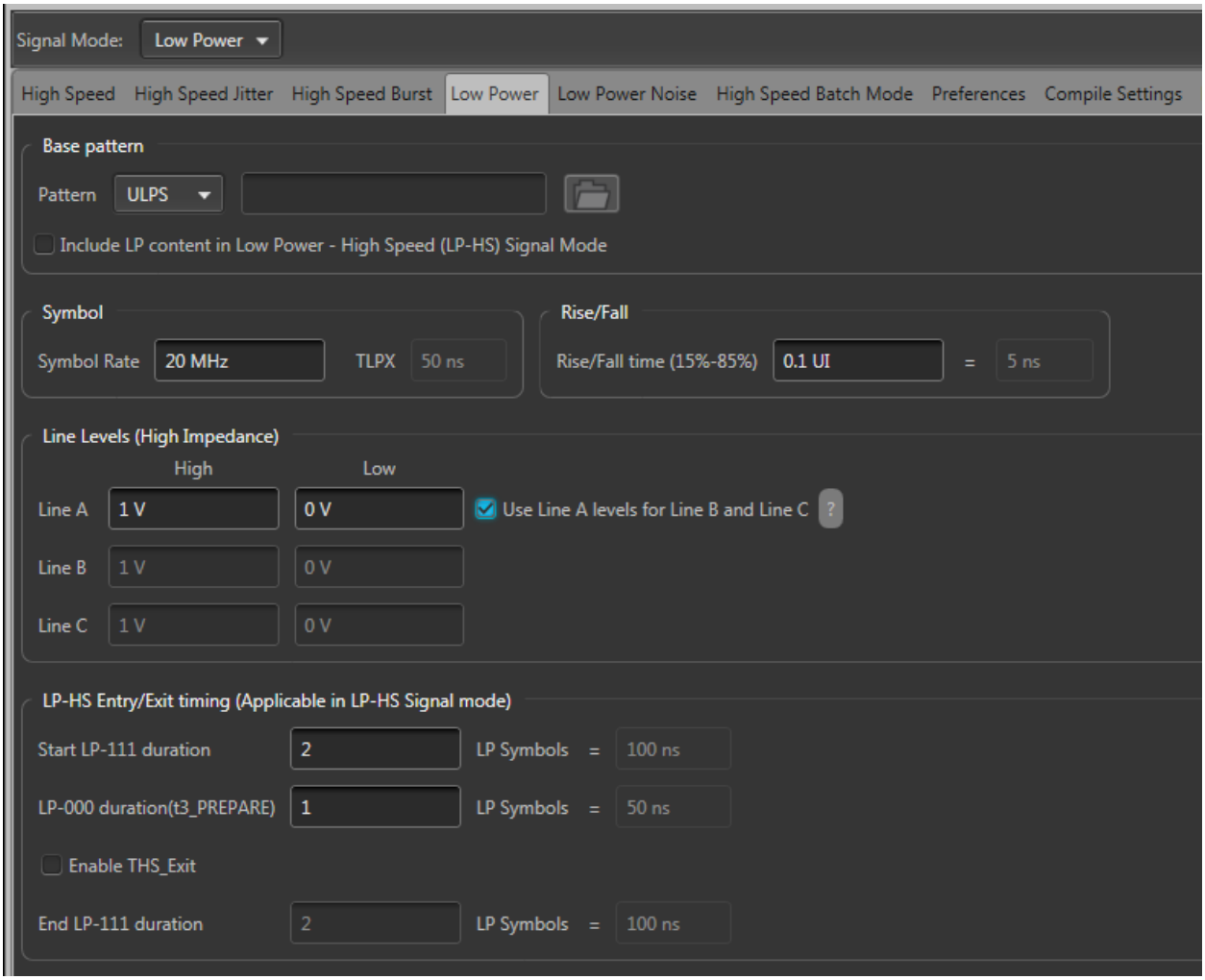


Figure: 2.1.4(a) Low power Tab settings

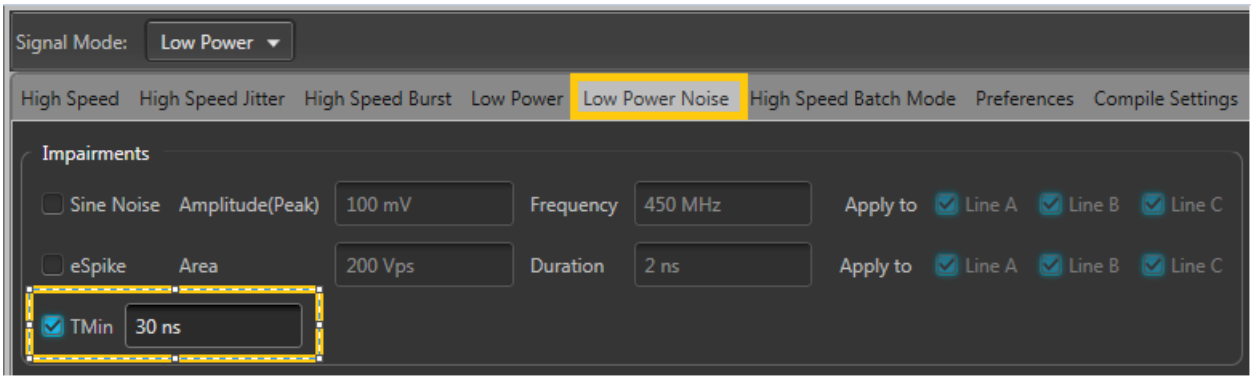


Figure: 2.1.4(b) Low power Noise settings - TMIN

Measurement details

If you need to verify the Minimum pulse width of the waveforms, employ the following measurement and settings to measure TMIN on a LP waveform.

- DPOJET Measurement: Period;
- Configuration: Edges->Clock, Clock-Edge-> Both
- Minimum of the Period Measurement represent TMIN_Rx

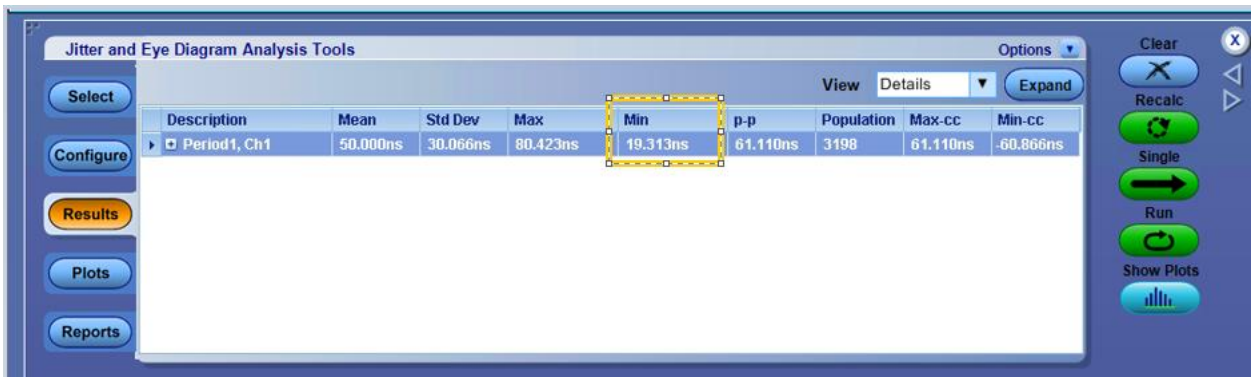


Figure: 2.1.4(b) measurement result for TMIN_Rx of 20 nsec

Test Procedure

1. Generate a LP waveform with signal parameters listed in the above section.
2. Transmit the test sequence to the DUT and verify via any valid observable that the DUT received the data without errors.
3. Decrease the Low Power Noise: TMIN by say 1ns.
4. Repeat steps 1, 2 & 3 till the observable shows an error.
5. At this point note record the smallest value of TMIN at which the DUT consistently received the test sequence without errors. This represent the DUT's TMIN_Rx minimum pulse width response.

Observable Results

Verify the recoded TMIN_Rx is <= 20 nsec.

Test 2.1.5 – LP-RX Input Pulse Rejection (eSPIKE)

Discussion

To make the LP Rx robust in the presence short-term glitches e_{SPIKE} is included in the specification. In this test we shall verify if the LP receiver rejects short-term signal glitches which are smaller than the specified conformance limit of 300Vps.

Parameter	Description	Min	Nom	Max	Units
e_{SPIKE}	Input pulse rejection			300	V·ps
T_{MIN-RX}	Minimum pulse width response	20			ns
V_{INT}	Peak interference amplitude			200	mV
f_{INT}	Interference frequency	450			MHz

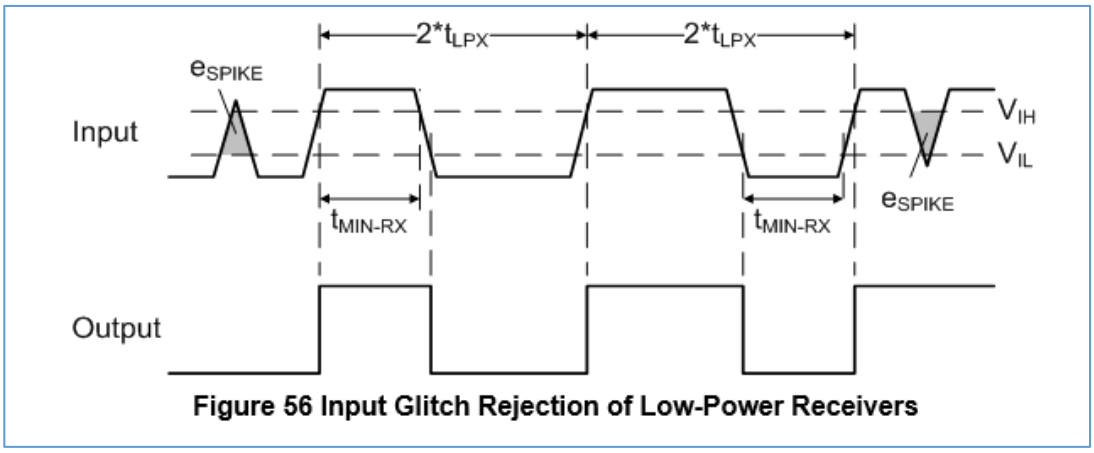


Figure 56 Input Glitch Rejection of Low-Power Receivers

Signal parameters

The relevant parameters of the CPHYXpress application are listed below, and also shown in the screenshot below

- Signal Mode: Low Power
- Low Power: Symbol rate = 20MHz
- Low Power: Line Level – High=1.0 V, Low = 0V.
- Low Power: Pattern: Based on the DUT.
- Low Power Noise: eSpike Area=300Vps, Duration = 2ns

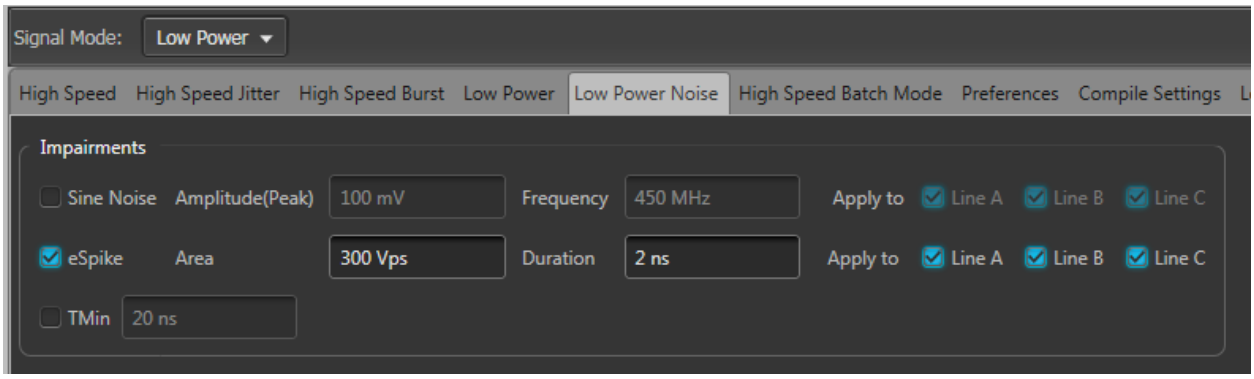


Figure: 2.1.5(a) LP-eSpike configuration.

Measurement details

The area of the spike can be measured using cursors, as shown below

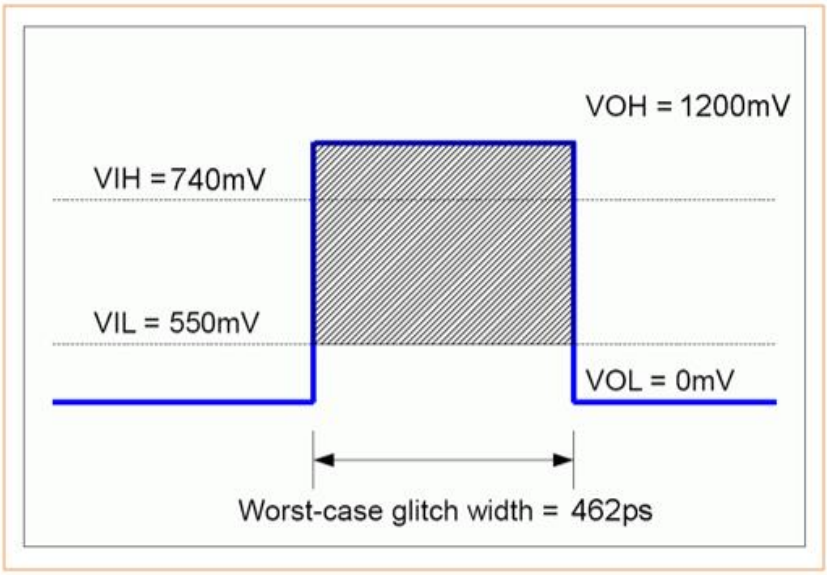


Figure: 2.1.5(a) LP-eSpike Measurement.

Test Procedure

1. Generate a LP waveform with signal parameters listed in the above section, with eSpike **disabled.**
2. Transmit the test sequence to the DUT.
3. Verify via any valid observable that the DUT received the test sequence without errors.
4. Reconfigure the Test System to **enable** eSpike, transmit the test sequence to the DUT.

Observable Results

Verify via any valid observable that the DUT received the test sequence without errors.

GROUP 2: LP-RX BEHAVIORAL REQUIREMENTS

Test/Calibration Setup

If any of the signal parameters of interest needs calibration, for this purpose the calibration setup should include with termination board. See section LP Signal Calibration Setup .

LP-HS Burst waveform

This section provide details on how to create a LP_HS pattern using C-PHYXPress. This pattern with a valid sequence, to test the Rx for error free reception is used in many test in this section.

The relevant parameters of the CPHYXpress application for this are listed below

- Signal Mode: Low Power High Speed
- Low Power: Symbol rate = 20MHz
- Low Power: Line Level – High=1.0 V, Low = 0V.
- Low Power: Pattern: *Based on the DUT*
- High Speed: Pattern: *Based on the DUT*, say PRBS9_CPHY
- High Speed: Symbol Rate: *Based on the DUT*, say 1.5Gsps

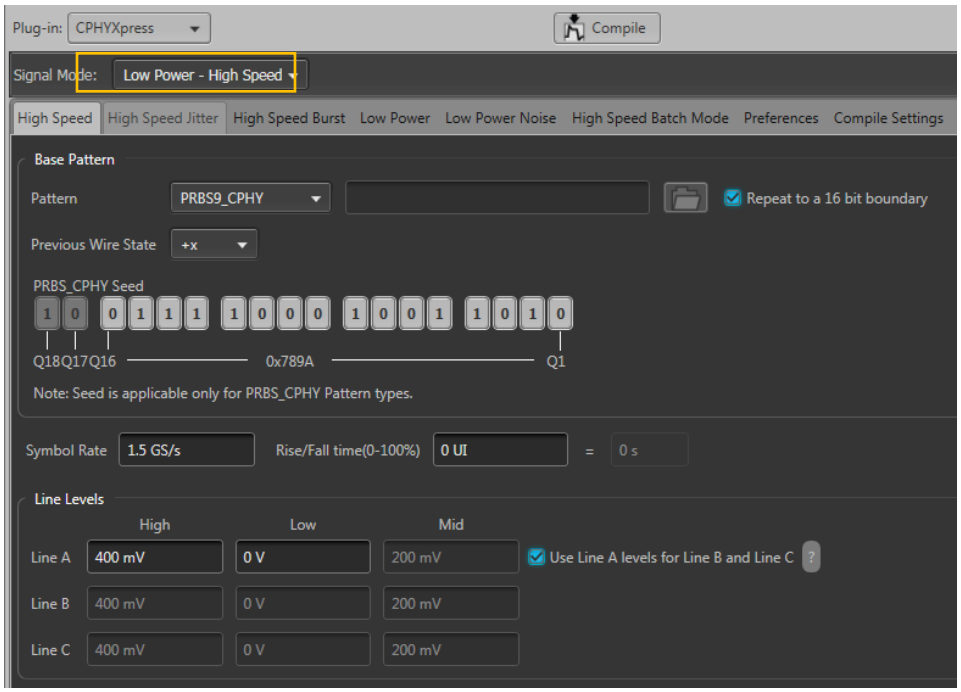


Figure: LP_HS burst waveform

Pattern files

A number of pattern files which are needed for the tests in this group, are pre-created and located in \Datafiles folder, which would be available once C-PHYXpress application is installed on the system.

\DataFiles folder location: *C:\Users\Public\Tektronix\CPHYXpress\DataFiles*

List of pattern files

File Name	Description
Test_221.LP	TINIT period
Test_222_MARK1.LP	Mark state
Test_222_STOP.LP	Stop state
Test_223_Invalid_Escape_Entry_1.LP Test_223_Invalid_Escape_Entry_2.LP	Invalid escape mode entry commands
Test_224_TS1.LP Test_224_TS2.LP Test_224_TS3.LP Test_224_TS4.LP Test_224_TS5.LP Test_224_TS6.LP Test_224_TS7.LP Test_224_TS8.LP	Various invalid escape mode commands
Test_225_RT1.LP Test_225_Ukn3.LP Test_225_Ukn4.LP Test_225_Ukn5.LP	Reset trigger and Unknown patterns as defined in escape mode table
Test_226_Udf1.LP Test_226_Udf2.LP Test_226_Ukn3.LP Test_226_Ukn4.LP Test_226_Ukn5.LP	Unsupported/Unassigned Commands

Test 2.2.1 – LP-RX Initialization period (TINIT)

Discussion

C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for TINIT, which defines the initialization behavior of both Master and Slave devices.

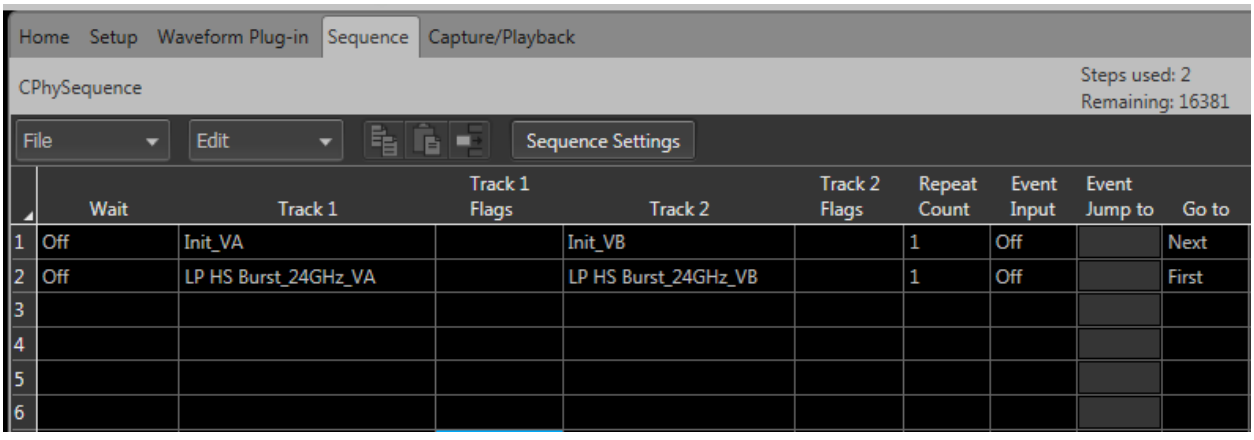
TINIT is a protocol specific parameter. RX Initialization period (TINIT) of the slave DUT is required to be greater than this minimum conformant value.

> Note that t_{INIT} is considered a protocol-dependent parameter, and thus the exact requirements for $t_{INIT,MASTER}$ and $t_{INIT,SLAVE}$ (transmitter and receiver initialization Stop state lengths, respectively,) are defined by the protocol layer specification and are outside the scope of this document. However, the C-PHY specification does place a minimum bound on the lengths of $t_{INIT,MASTER}$ and $t_{INIT,SLAVE}$, which each shall be no less than 100 µs. A protocol layer specification using the C-PHY specification may specify any values greater than this limit, for example, $t_{INIT,MASTER} \geq 1$ ms and $t_{INIT,SLAVE} = 500$ to 800 µs.

Signal parameter

The relevant parameters of the CPHYXpress application for this test are listed below

- Signal Mode: Low Power
- Low Power: Symbol rate = 20MHz
- Low Power: Line Level – High=1.0 V, Low = 0V.
- Create a LP waveform representing the initialization period by using the following pattern. Low Power: Pattern:
  - low power state file: C:\Users\Public\Tektronix\CPHYXpress\DataFiles\Test_221.LP
- This waveform is added in waveform sequence with repeat =1 as below. The setting of this repeat count generates a initialization period of ~1 usec
- The second waveform in the sequence is a valid LP_HS waveform, whose content is based on the DUT.



	Wait	Track 1	Track 1 Flags	Track 2	Track 2 Flags	Repeat Count	Event Input	Event Jump to	Go to
1	Off	Init_VA		Init_VB		1	Off		Next
2	Off	LP HS Burst_24GHz_VA		LP HS Burst_24GHz_VB		1	Off		First
3									
4									
5									
6									

Figure: 2.2.1(a) Waveform Sequence to control the TINIT period

Measurement details

To measure the TINIT, generated by a waveform sequence, use cursors as shown in the screen shot below.

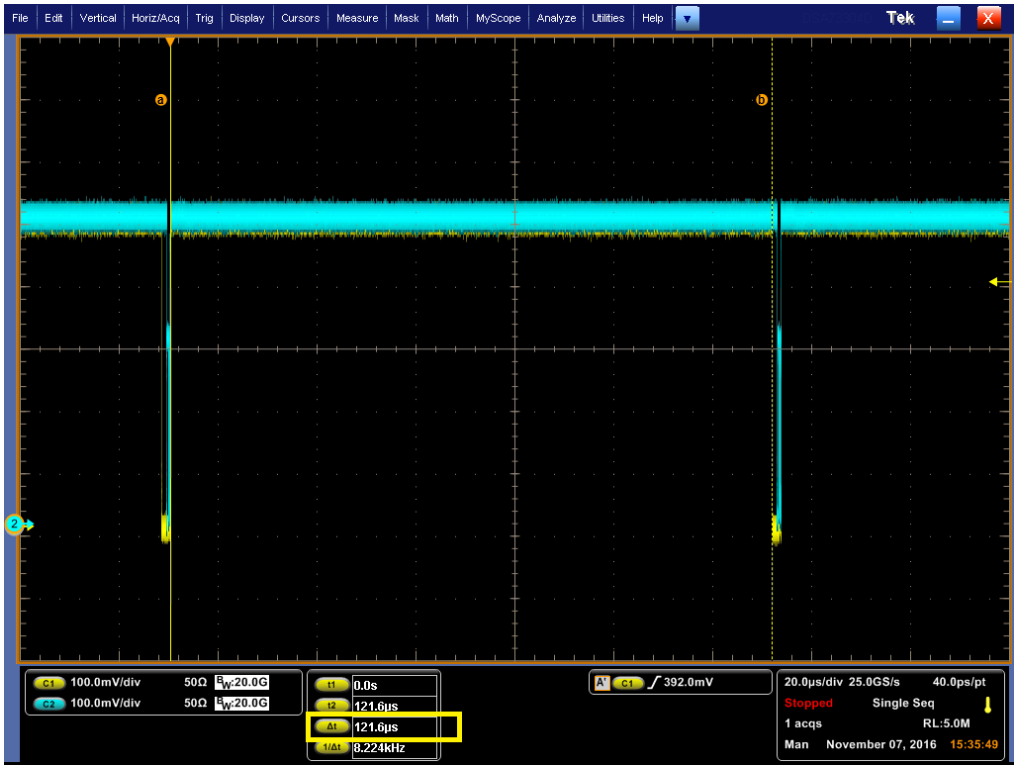


Figure: 2.2.1(b) TINIT measurement using cursors for lines A and B

Test Procedure

1. Connect the Slave DUT to the Test Setup, leaving the DUT power off.
2. Power on the DUT.
3. Without sending a valid Initialization period, send a valid test sequence that would otherwise cause an observable result. That is only transmit the second waveform in the sequence. Verify that the DUT ignores the test sequence.
4. Repeat the above procedure by slowly increasing the initialization period by increasing the reap count on the AWG sequence window, until the DUT is observed to accept the test sequence.
5. At this point record the TINIT = repeat count * 1 usec.

Observable Results

Verify that the value of TINIT is greater than the minimum protocol-specific conformance limit.

Test 2.2.2 – ULPS Exit: LP-RX T_{WAKEUP} Timer Value

Discussion

The C-PHY Specification defines a mechanism for a lane to exit ULPS state. Mark-1 state (LP-100) for a minimum time TWAKEUP (1 msec), followed by a Stop state (LP-111), should make the slave exit the ULPS state.

Signal parameter

Multiple waveforms are needed for this test.

1) **ULPS entry waveform**: A waveform to put the DUT in ULPS state. A sample *ULPS.LP* pattern file is at \Datafiles folder.
2) **Valid Test LP_HS waveform**: A LP_HS waveform with which could be used to check for error in reception.
3) **ULPS exit waveform**: A waveform to put the device out of ULPS state. More details on this is provided below

The relevant parameters of the CPHYXpress application to create a **ULPS exit waveform** are listed below

- Signal Mode: Low Power
- Low Power: Symbol rate = 20MHz
- Low Power: Line Level – High=1.0 V, Low = 0V.
- ULPS exit waveform is created using two pattern files located at \Datafiles, the configurations are show in Figure: 2.2.2(a)
    - Test_222_MARK1.LP
    - Test_222_STOP.LP
- The waveforms are added in waveform sequence with repeat counts as shown in the Figure 2.2.2(b). A repeat count of 500, results in about 1 ms of TWAKEUP time. The third waveform in the sequence is a valid LP_HS waveform, whose content is based on the DUT.

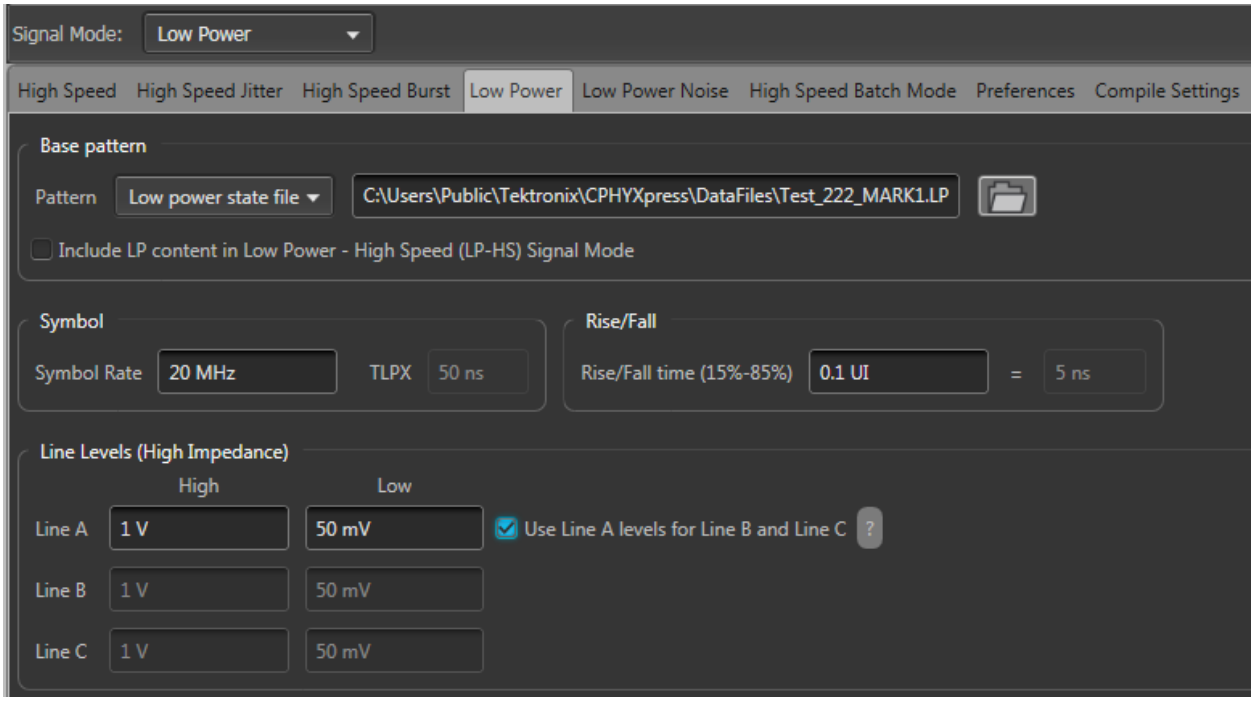
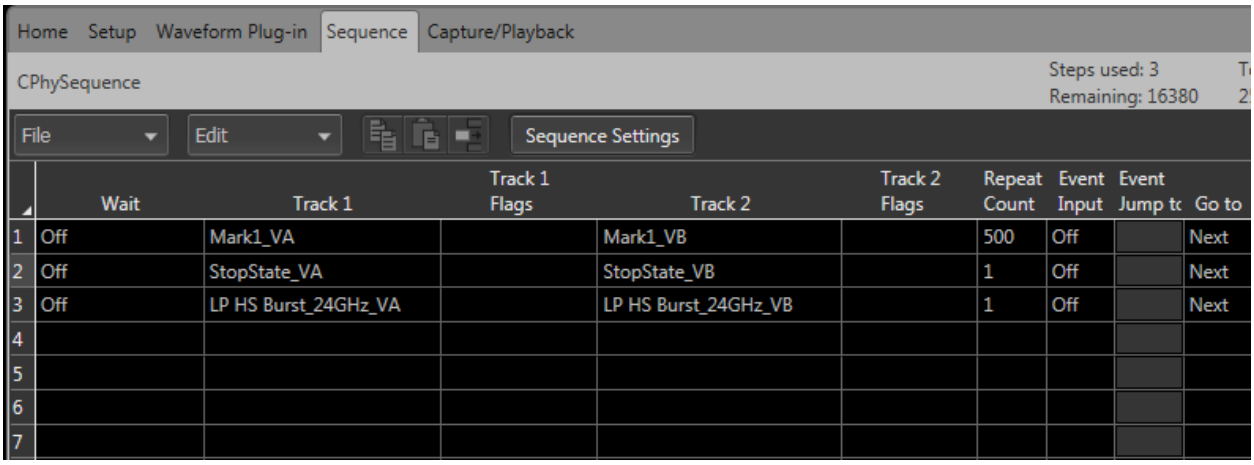


Figure: 2.2.2(c) LP tab configuration to create Mark1 waveform



	Wait	Track 1	Track 1 Flags	Track 2	Track 2 Flags	Repeat Count	Event Input	Event Jump to	Go to
1	Off	Mark1_VA		Mark1_VB		500	Off		Next
2	Off	StopState_VA		StopState_VB		1	Off		Next
3	Off	LP HS Burst_24GHz_VA		LP HS Burst_24GHz_VB		1	Off		Next
4									
5									
6									
7									

Figure: 2.2.2(d) Waveform Sequence

Measurement details

Cursor based measurement could be used to measure the TWAKEUP time generated by a waveform sequence.

Test Procedure

1. Send a **ULPS entry waveform** to put the DUT lane into ULPS state.
2. Next the waveform sequence consisting of Mark1 (for 1msec), stop state and a valid HS data sequence, created previously to the DUT in ULPS state.

3. Verify via any valid observable that the DUT received the data without errors. Error free reception confirms that the DUT has successfully exited form ULPS state

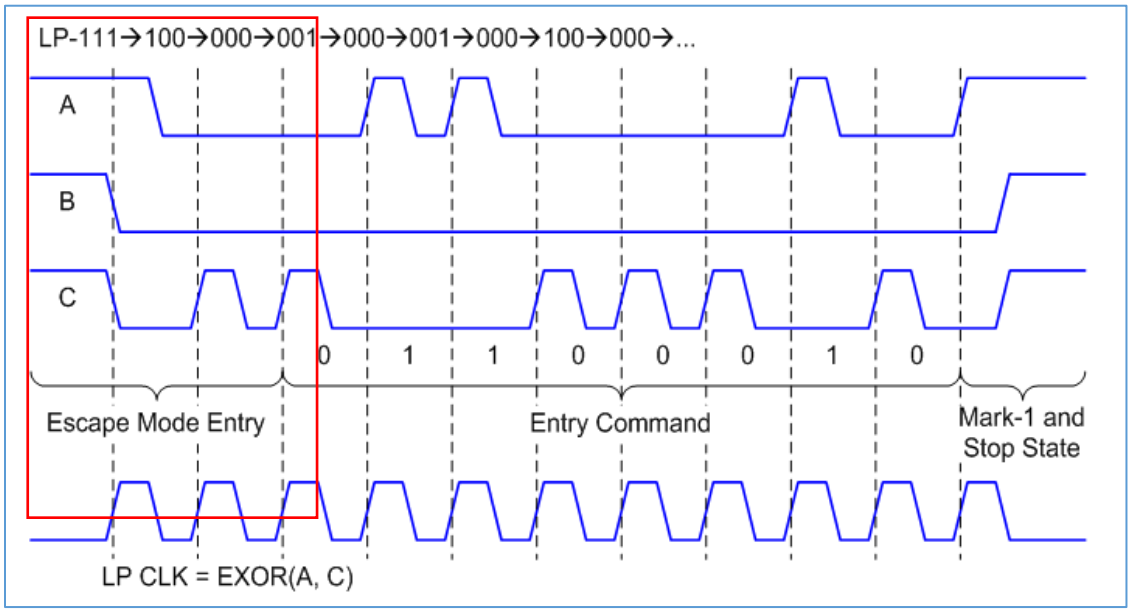
Test 2.2.3 – LP-RX Invalid/Aborted Escape Mode Entry

Discussion

The C-PHY Specification provides a definition of the Escape Mode Entry process in state-machine form.

681 A lane shall enter escape mode via an escape mode entry procedure (LP-111, LP-100, LP-000, LP-001, LP-
682 000). As soon as the final Bridge state (LP-000) is observed on the lines the lane shall enter escape mode in
683 space state (LP-000). If an LP-111 is detected at any time before the final Bridge state (LP-000), the Escape

469 mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the
470 Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop
471 state.



In this test, the ability of the DUT's LP-RX to properly ignore invalid Escape Mode Entry sequences will be verified. Following two test cases of invalid escape mode entry sequence will be used for this test.

LP-111, LP-100, LP-000, LP-001, LP-000 (valid Escape Mode Entry sequence)

Test Case 1) LP-111, LP-100, LP-000, LP-001, LP-111

Test Case 2) LP-111, LP-100, LP-111, LP-111, LP-111

Signal parameters

Multiple waveforms are needed for this test.

1) **Valid Test LP_HS waveform**: A LP_HS waveform with which could be used to check for error free reception.
    a. Procedure to create a LP_HS waveform is given in section "LP-HS Burst pattern creation"
2) **Invalid Escape Entry waveform:** Waveform with invalid escape entry commands for two test cases
    a. Create "LP_Invalid Escape Entry" pattern by selecting "Test 223_Invalid_Escape Entry_1.LP" file in the Custom option as shown below and add the pattern to the AWG sequence.
    b. Also create "LP_Invalid Escape Entry" pattern by selecting "Test 223_Invalid_Escape Entry_2.LP" file in the Custom option and add the pattern to the AWG sequence.

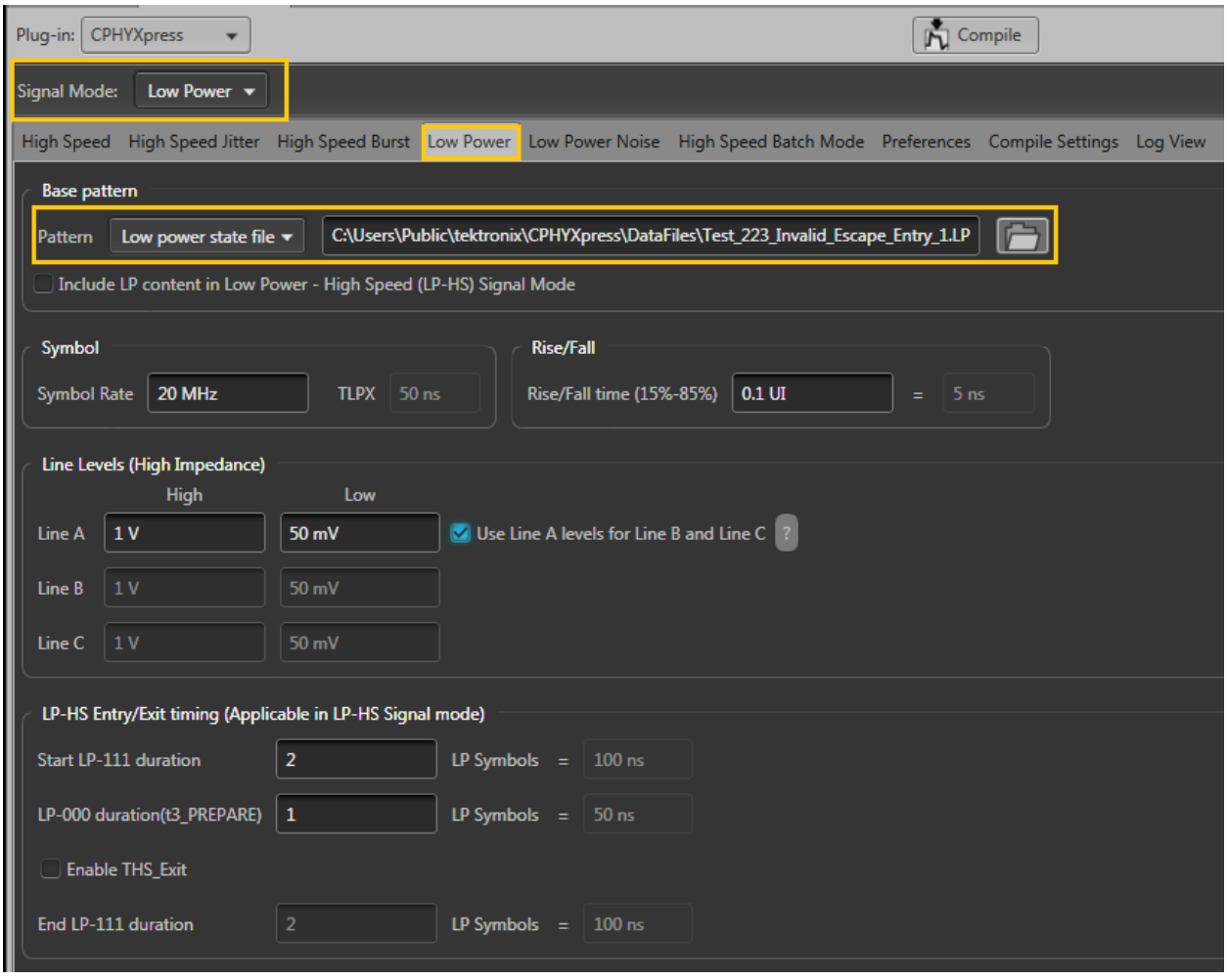


Figure: 2.2.3(a) LP Custom option selection.

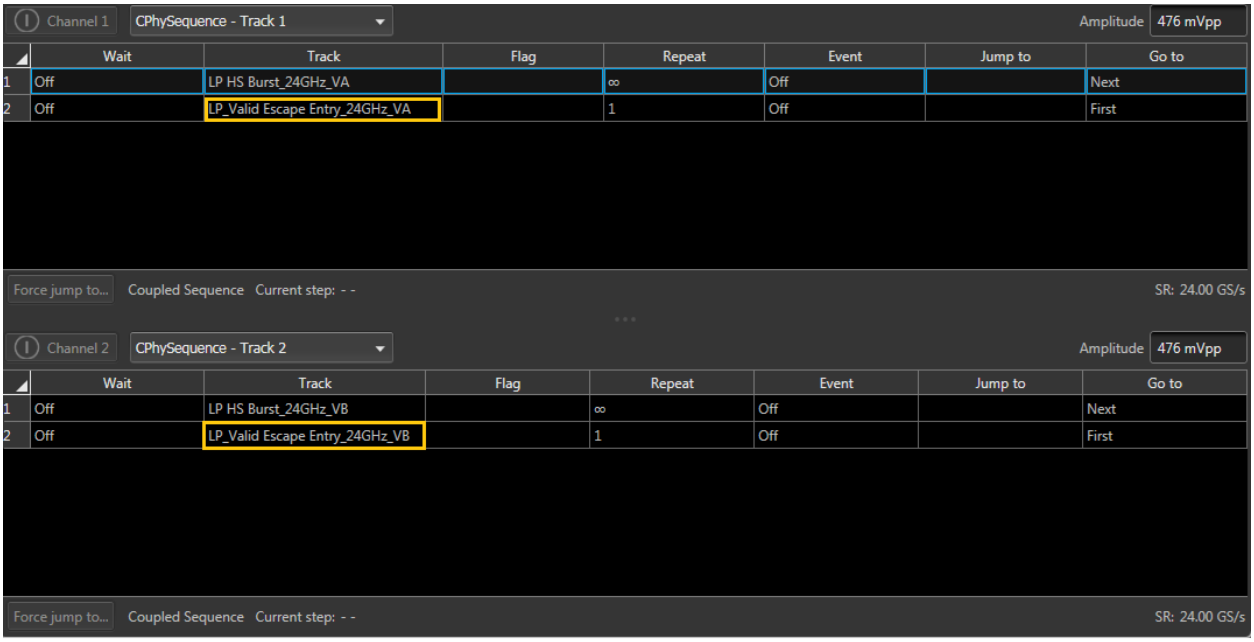


Figure: 2.2.3(b) LP Valid Escape Entry sequence

Test Procedure

1. Connect the DUT to the AWG.
2. Configure the Test Setup to transmit sequence with LP HS Burst pattern to the DUT, and verify that the data is properly received by the DUT with no errors.
3. Next insert Testcase#1 waveform into the sequence which has invalid Escape Mode Entry sequence.
4. Verify that the DUT is still able to successfully receive the data without errors.
5. Repeat steps 3 and 4 with Testcase#2 waveform.

Observable Results

For both test cases, verify that the DUT received the data without errors.

Test 2.2.4 – LP-RX Invalid/Aborted Escape Mode Command

Purpose

To verify that the DUT's LP-RX properly ignores invalid/aborted Escape commands.

Discussion

The previous test (2.2.3) verified a DUTs ability to detect invalidly formed Escape Mode Entry sequences, which were corrupted with LP-111 Stop states at different locations in the Escape Mode Entry sequence. The result of these tests was that the DUT should have effectively ignored the invalid sequence and not have allowed the invalid sequences to negatively impact reception of subsequent valid data.

681 A lane shall enter escape mode via an escape mode entry procedure (LP-111, LP-100, LP-000, LP-001, LP-
682 000). As soon as the final Bridge state (LP-000) is observed on the lines the lane shall enter escape mode in
683 space state (LP-000). If an LP-111 is detected at any time before the final Bridge state (LP-000), the Escape

2. If LP-111 occurs during escape mode the lane returns to Stop state (Control Mode LP-111).

Signal parameters

Below LP test cases are used to test the invalidly formed Escape Mode Entry.

1) [Valid EM Entry] + LP-001/000/001/000/001/000/100/000/100/000/100/000/100/000/001/111 + [Stop]
2) [Valid EM Entry] + LP-001/000/001/000/001/000/100/000/100/000/100/000/100/111/111/111 + [Stop]
3) [Valid EM Entry] + LP-001/000/001/000/001/000/100/000/100/000/100/111/111/111/111/111 + [Stop]
4) [Valid EM Entry] + LP-001/000/001/000/001/000/100/000/100/111/111/111/111/111/111/111 + [Stop]
5) [Valid EM Entry] + LP-001/000/001/000/001/000/100/111/111/111/111/111/111/111/111/111 + [Stop]
6) [Valid EM Entry] + LP-001/000/001/000/001/111/111/111/111/111/111/111/111/111/111/111 + [Stop]
7) [Valid EM Entry] + LP-001/000/001/111/111/111/111/111/111/111/111/111/111/111/111/111 + [Stop]
8) [Valid EM Entry] + LP-001/111/111/111/111/111/111/111/111/111/111/111/111/111/111/111 + [Stop]

1. Add "LP HS Burst" pattern (Created in the session "LP-HS Burst pattern creation") to the AWG sequence.
2. Create "LP_Escape command Entry_TS1" pattern by selecting "Test 224_TS1.LP" file in the Custom option as shown below and add the pattern to the AWG sequence.
3. Create "LP_Escape command Entry_TS2" pattern by selecting "Test 224_TS2.LP" file in the Custom option.
4. Create "LP_Escape command Entry_TS3", "LP_Escape command Entry_TS4" "LP_Escape command Entry_TS5" "LP_Escape command Entry_TS6" "LP_Escape command Entry_TS7" and "LP_Escape command Entry_TS8" by selecting "Test 224_TS3.LP" "Test 224_TS4.LP" "Test 224_TS5.LP" "Test 224_TS6.LP" "Test 224_TS7.LP" and "Test 224_TS8.LP" file in the Custom option respectively.

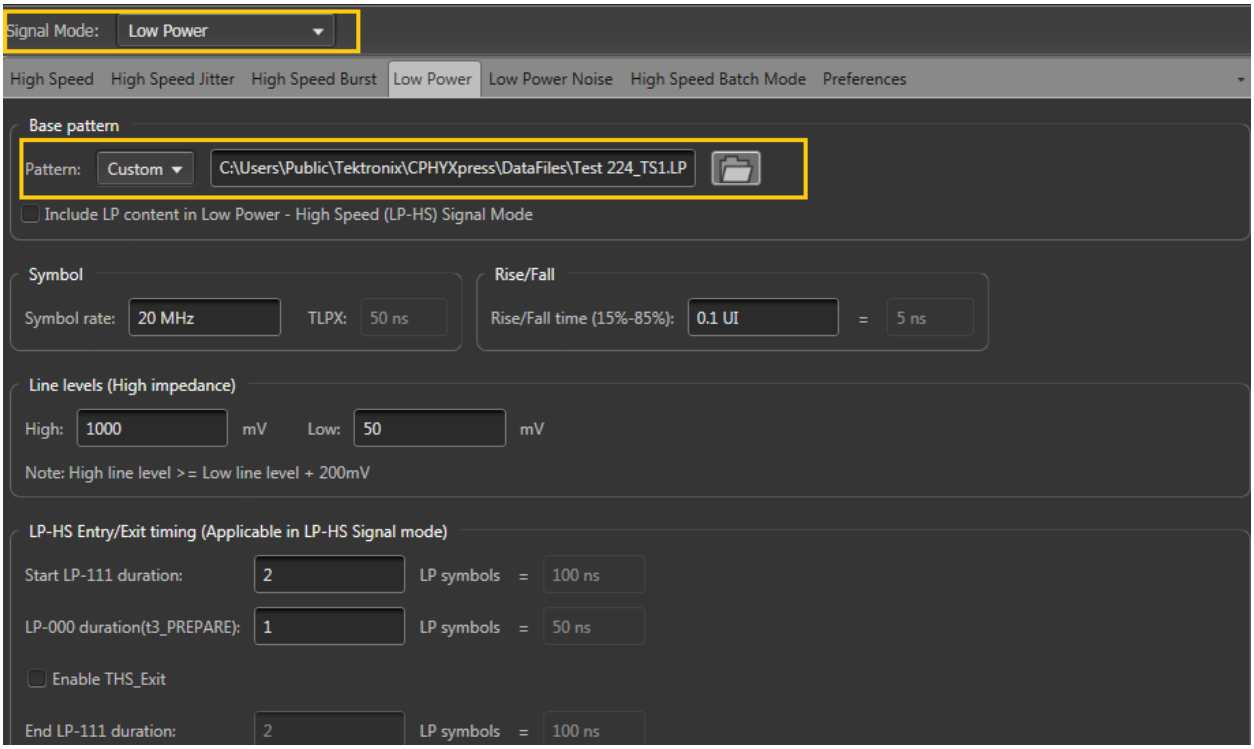


Figure: 2.2.4(a) LP_Escape command Entry creation

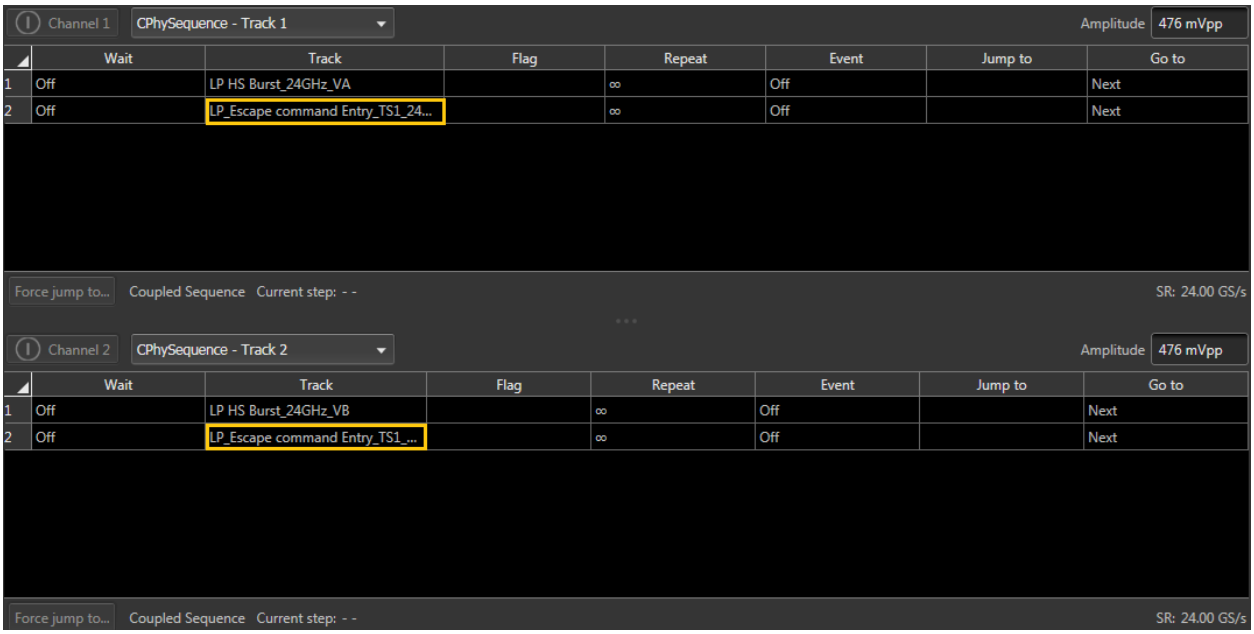


Figure 2.2.4(b): LP_Escape command Entry sequence

Test Procedure

1. Connect the DUT to the AWG.
2. Configure the Test Setup to transmit sequence with LP HS Burst pattern to the DUT, and verify that the data is properly received by the DUT with no errors.
3. Once proper operation has been verified as step 1, the Test case 1 pattern with aborted ULPS command sequences is send to DUT.
4. Verify that the DUT is still able to successfully receive the data without impairment.
5. Once proper operation has been verified as step 1, the Test case 2 pattern with aborted ULPS command sequences is send to DUT.
6. Verify that the DUT is still able to successfully receive the data without impairment.
7. Repeat for all the steps from 5 to 6 for Test case 3 to 8.

Observable Results

In all cases, verify that the integrity of the received data, as well as the overall operation of the DUT are not negatively affected by the presence of the invalid/aborted ULPS command sequences.

Test 2.2.5 – LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits

Purpose

To verify that the DUT's LP-RX ignores any extra bits received following a Trigger Command.

Discussion

The C-PHY specification defines the Escape Mode behavior for C-PHY transmitters and receivers. This includes a requirement for how receivers treat extra bits that are received after an Escape Mode Trigger command. The choice of the extra post-command bits must be defined for this test. This test will concatenate one extra byte of data after the Trigger command, and will use the ULPS Entry command as this extra byte.

Table 16 Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

Signal parameters:

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: Low Power-High Speed
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz resulting TLPX of 50ns
- Low Power Pattern: Low power state file
- Add "LP HS Burst" pattern (Created in the session "LP-HS Burst pattern creation") to the AWG sequence.
- Many pattern files needed for this test are at "C:\Users\Public\Tektronix\CPHYXpress\DataFiles"
- Create "Reset Trigger" pattern by selecting "Test 225_RT1.LP" file in the Custom option as shown below and add the pattern to the AWG sequence.
- Create "Unknown-3" pattern by selecting "Test _225_Ukn3.LP" file in the Custom option as shown below.
- Create "Unknown-4" pattern by selecting "Test_225_Ukn4.LP" file in the Custom option as shown below.
- Create "Unknown-5" pattern by selecting "Test_225_Ukn5.LP" file in the Custom option as shown below.

Low Power State file to be used to create Escape Mode Action which is given in above table.

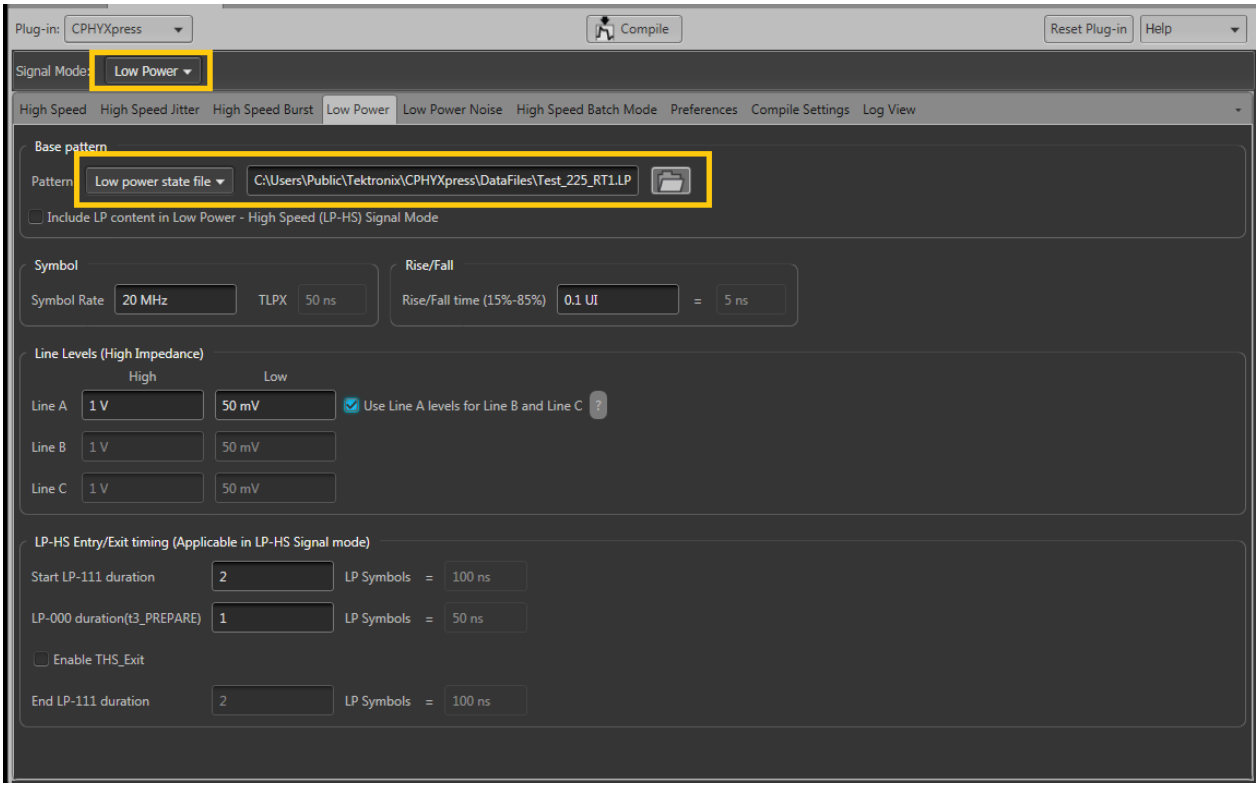


Figure: 2.2.5(a) Low power state file for "Reset Trigger"

- Above created base pattern using Low power state file is sequenced with the "LP HS Burst" pattern (Created in the session "LP-HS Burst pattern creation") to the AWG sequence is shown below

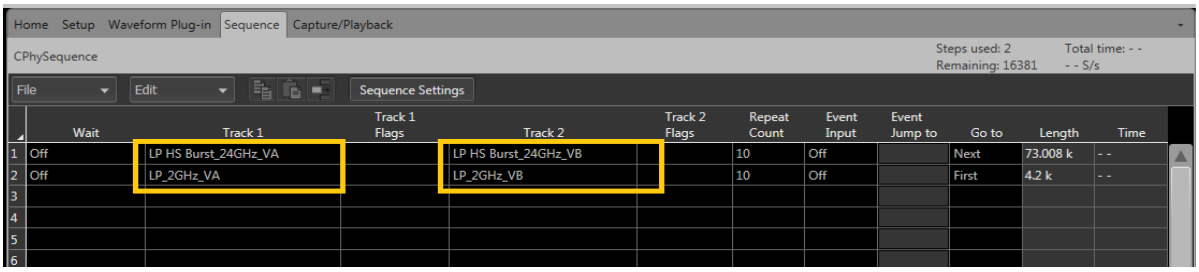


Figure 2.4.5(b) Sequenced Waveform of LP-HS Burst and LP state file pattern

Test Procedure

1. Connect the DUT to the AWG.
2. Configure the Test Setup to transmit sequence with LP HS Burst pattern to the DUT, and verify that the data is properly received by the DUT with no errors.
3. Once proper operation has been verified as step 1, Reset Trigger pattern with ULPS command added in sequence shown in Figure 2.4.5(b) is send to DUT.
4. Verify that the DUT is still able to successfully receive the data without impairment.
5. Repeat for all the steps from 3 to 4 for Unknown-3, Unknown-4, and Unknown-5 Trigger commands in place of the Reset-Trigger pattern.

Observable Results

Verify that in all test cases (Trigger command, Unknown-3, Unknown-4, and Unknown-5) the DUT ignores all bits occurring after the last bit of the Trigger Command, by observing that the DUT properly received the data stream without error.

Test 2.2.6 – LP-RX Escape Mode Unsupported/Unassigned Commands

Purpose

To verify that the DUT's LP-RX properly ignores unsupported and unassigned Escape Mode commands.

Discussion

The Escape Mode sequence will contain an unassigned Escape command byte. The DUT's behavior will be observed to verify that the presence of the unassigned command code does not impact reception of the valid data stream. In this test, the AWG will be sent all 5 unassigned Command codes, contained in properly formed, valid Escape sequences. It will also be sent the Undefined-1, Undefined-2, Unknown-3, Unknown-4, and Unknown-5 Command codes shown below. In all cases, the DUT should ignore the command code.

Table 16 Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: Low Power-High Speed
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz resulting TLPX of 50ns
- Low Power Pattern: Low power state file
- Add "LP HS Burst" pattern (Created in the session "LP-HS Burst pattern creation") to the AWG sequence.
- Many pattern files needed for this test are at \DataFiles folder.
- Create "Undefined-1" pattern by selecting "Test_226_Udf1.LP" file in the Custom option as shown below and add the pattern to the AWG sequence.
- Create "Undefined-2" pattern by selecting "Test_226_Udf2.LP" file in the Custom option as shown below.

- Create “Unknown-3”, “Unknown-4”, and “Unknown-5”, pattern by selecting “Test_226_Ukn3.LP”, “Test_226_Ukn4.LP” and “Test_226_Ukn5.LP” file respectively.

Low Power State file to be used to create Escape Mode Action which is given in above table.

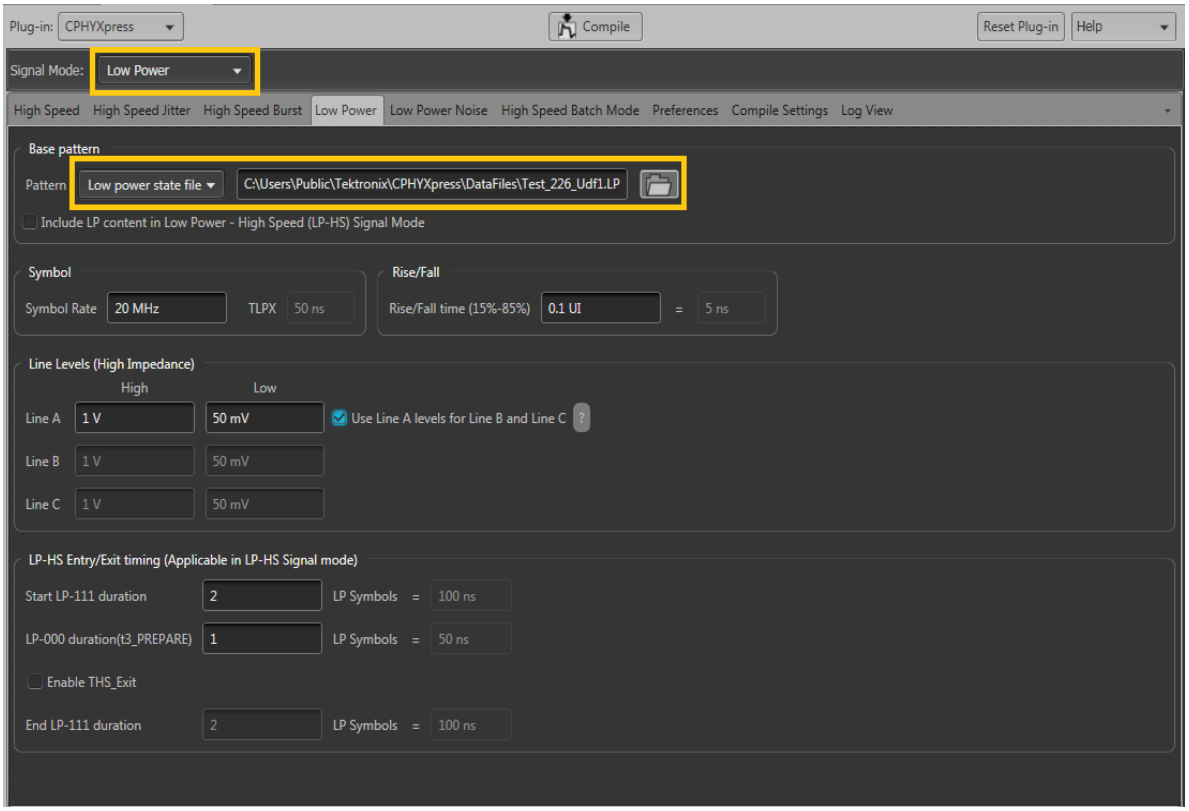


Figure 2.4.6(a) Low Power Base pattern

- Above created base pattern using Low power state file is sequenced with the “LP HS Burst” pattern (Created in the session “LP-HS Burst pattern creation”) to the AWG sequence is shown below

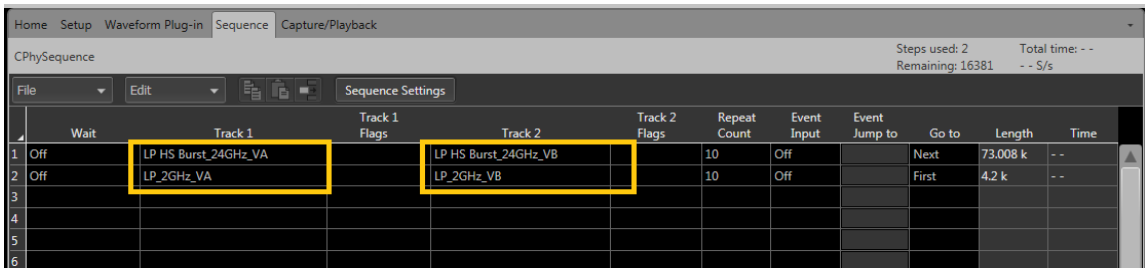


Figure 2.4.6(b) Sequenced Waveform of LP-HS Burst and LP state file pattern

Test procedure

1. Connect the DUT to the AWG.
2. Configure the Test Setup to transmit sequence with LP HS Burst pattern to the DUT, and verify that the data is properly received by the DUT with no errors.
3. Once proper operation has been verified as step 1, Undefined-1 pattern added in sequence Figure 2.4.6(b) is send to DUT.
4. Verify that the DUT is still able to successfully receive the data without impairment.
5. Repeat for all the steps from 3 to 4 for Undefined-2, Unknown-3, Unknown-4, and Unknown-5 Trigger commands in place of the Undefined-1 command.

Observable Results

For all test cases, verify that the DUT ignores the unsupported/unassigned command, and successfully receives the data in DUT.

GROUP 3: HS-RX VOLTAGE AND JITTER TOLERANCE REQUIREMENTS

Test/Calibration Setup

This group of tests requires HS only signals. For calibration of these stimuli, the signal generator outputs is directly connected to an oscilloscope. See section HS Signal Calibration Setup .

Test 2.3.1 - HS-RX Amplitude Tolerance ($V_{CPRX(DC)}$, V_{IHHS}, V_{ILHS})

Discussion

In this the DUT is tested for various cases of common mode and differential voltage levels covering the maximum and minimum levels allowed for these two parameters. The Table below list four test cases for this measurement.

Test Case	Common-Mode Level (mV)	Differential Voltage Pk-pk (2*VOD) (mVppd)	Single Ended Voltage VIHHS/VILHS (mV)
1	95	540 (strong one to strong zero level)	230/-40
2	95	80 (Weak one to weak zero level)	135/55
3	390	580 (strong one to strong zero level)	535/245
4	390	80 (Weak one to weak zero level)	430/350

Table 2.3.1-1: Differential/Common-Mode Amplitude Test Cases

Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: HS
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Line Levels: High and Low, represent the VIHHS/VILHS voltages

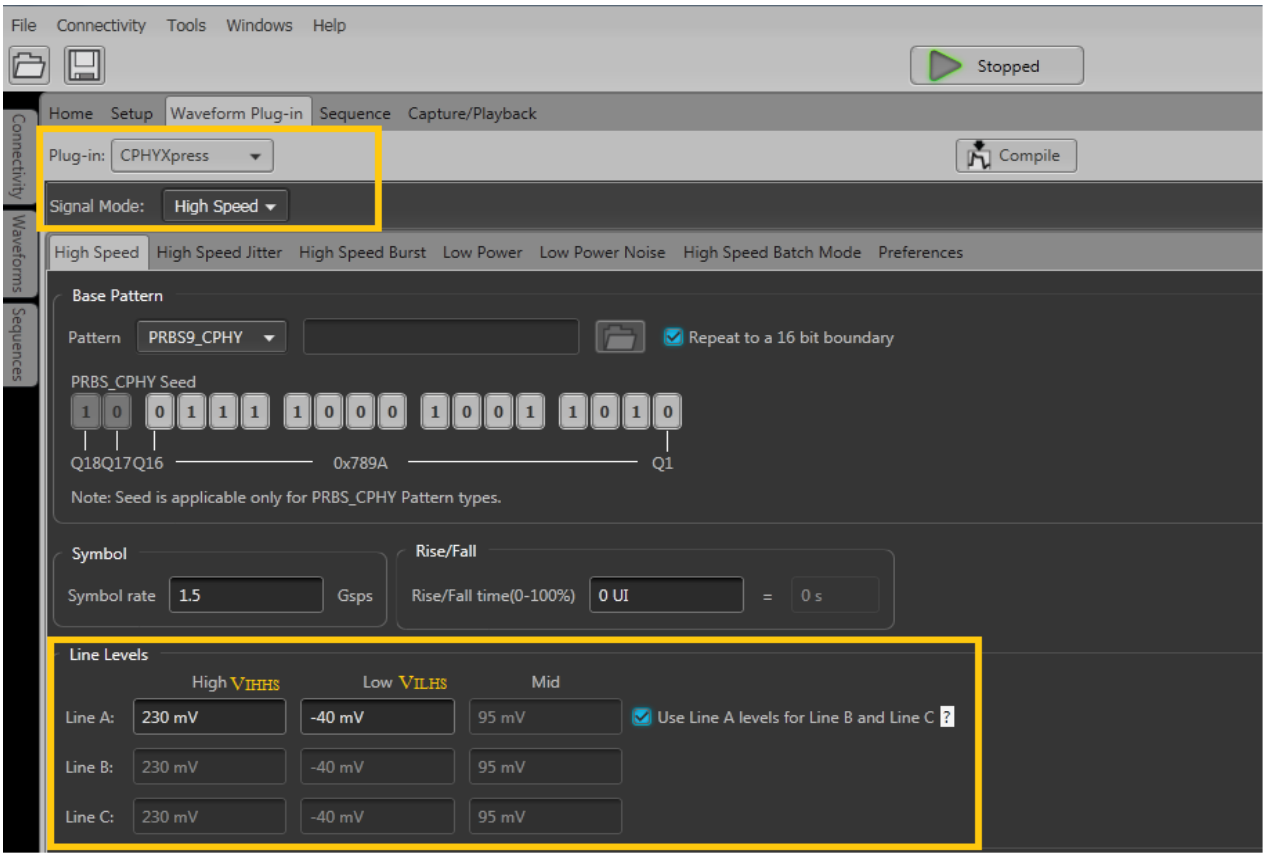


Figure 2.3.1(a): Configurations for line levels

Test Procedure

1. Generate a HS waveform with signal parameter listed above and VIHHS/VILHS mentioned for test case 1 in Table 2.3.1.1. VIHHS/VILHS are set by configuring high and low voltage values in the Line Levels configuration sections Figure 2.3.1(a) ("Use Line A levels for Line B and Line C should be checked")
2. Measure VIHHS/VILHS for all the three wire A, B and C. Measurement can be performed using a cursor based measurement as shown in Figure 2.3.1(b). To calibrate for the VIH/VIL levels follow the procedure in section *Voltage (VIH/VIL) Calibration Procedure*
3. Transmit the test sequence to the Rx DUT. Verify via any valid observable that the DUT received the test sequence without errors
4. Repeat all the above steps for Test case 2, 3 and 4 given in the Table 2.3.1-1.

Observable Results

Verify that for all four test cases that the test sequence was received by the DUT without error.

Example Result

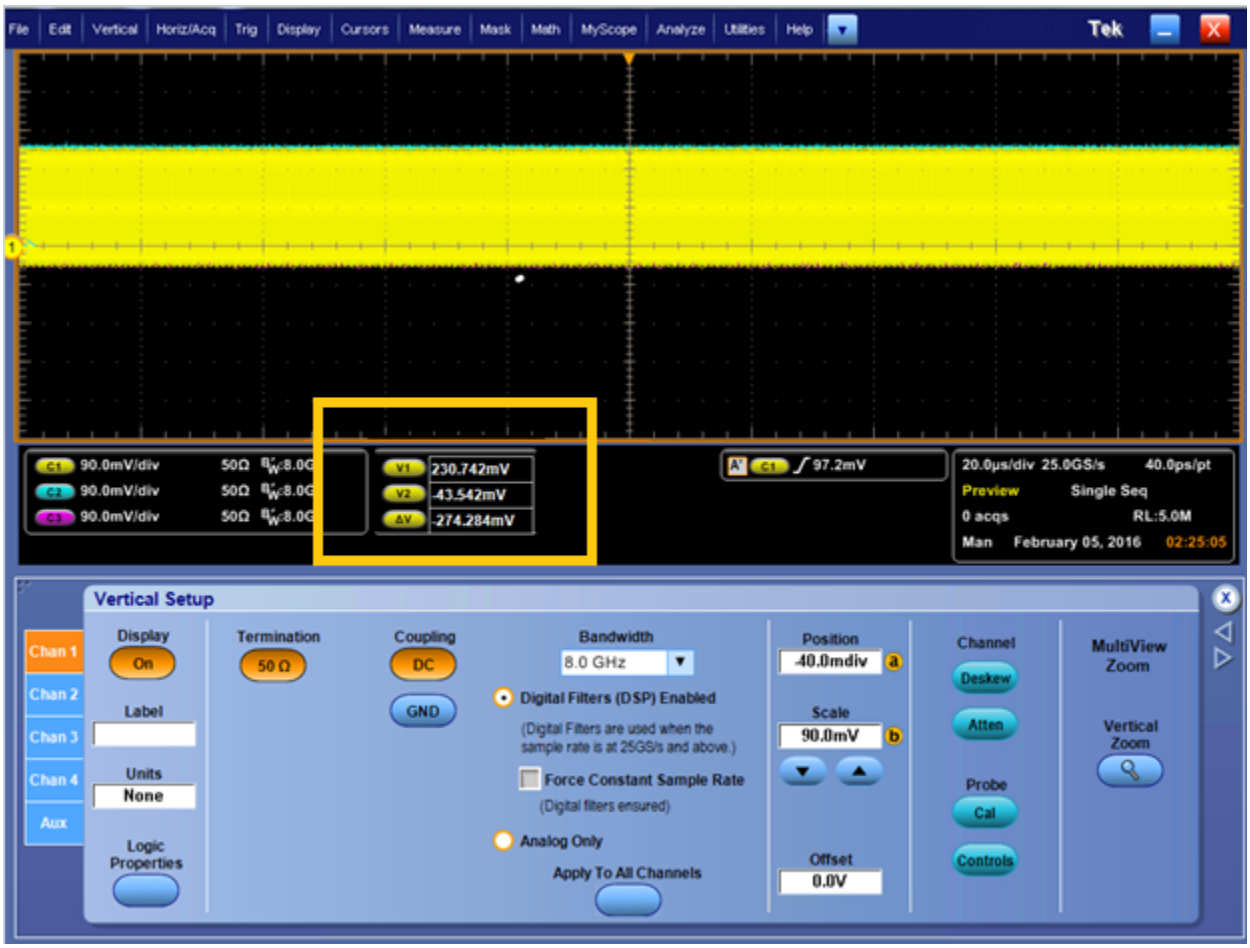


Figure 2.3.1(b): VIHHS/VILHS result on Line A

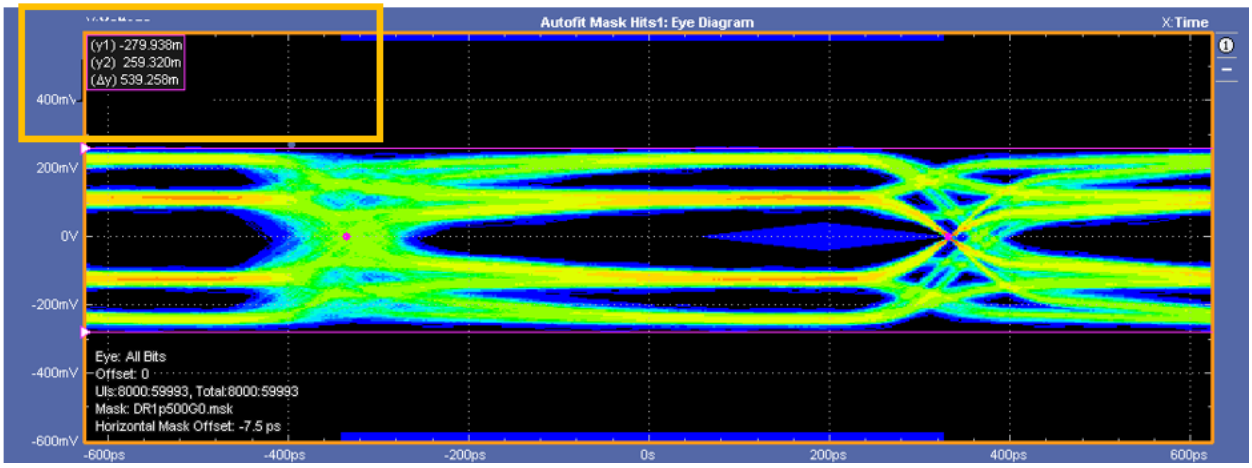


Figure 2.3.1(c): Differential Eye diagram (AB)

Test 2.3.2 HS-RX Differential Input High/Low Thresholds (V_{IDTH}, V_{IDTL})

Discussion

The definition and the conformance limits for the Differential Input High and Low Thresholds are given below. These are the minimum differential signal levels seen as an HS Strong 1 and HS Strong 0 by the receiver.

> The differential input high and low threshold voltages of the high-speed receiver are denoted by V_{IDTH} and V_{IDTL}, respectively. V_{ILHS} and V_{IHHS} are the single-ended, input low and input high voltages, respectively. $V_{CPRX(DC)}$ is the differential input common-point voltage. The high-speed receiver shall be able to detect differential signals at its A, B and C input signal pins when all three signal voltages, V_A, V_B and V_C, are within the common-point voltage range and if the voltage differences between V_A, V_B and V_C exceed either V_{IDTH} or V_{IDTL}. The high-speed receiver shall receive high-speed data correctly while rejecting common-

Figure 2.3.2-1: VIDTH Specification Definition

Parameter	Min	Max	
Differential input high threshold		40	mV
Differential input low threshold	-40		mV

Table 2.3.2-2: V_{IDTH}, V_{IDTL} Conformance Limits

Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: HS
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Line Levels: High = 325mV and Low = 175 mV, represent the VIHHS/VILHS voltages to achieve a nominal differential voltage of 300mV strong one to strong zero level and common-mode level of 250mV.

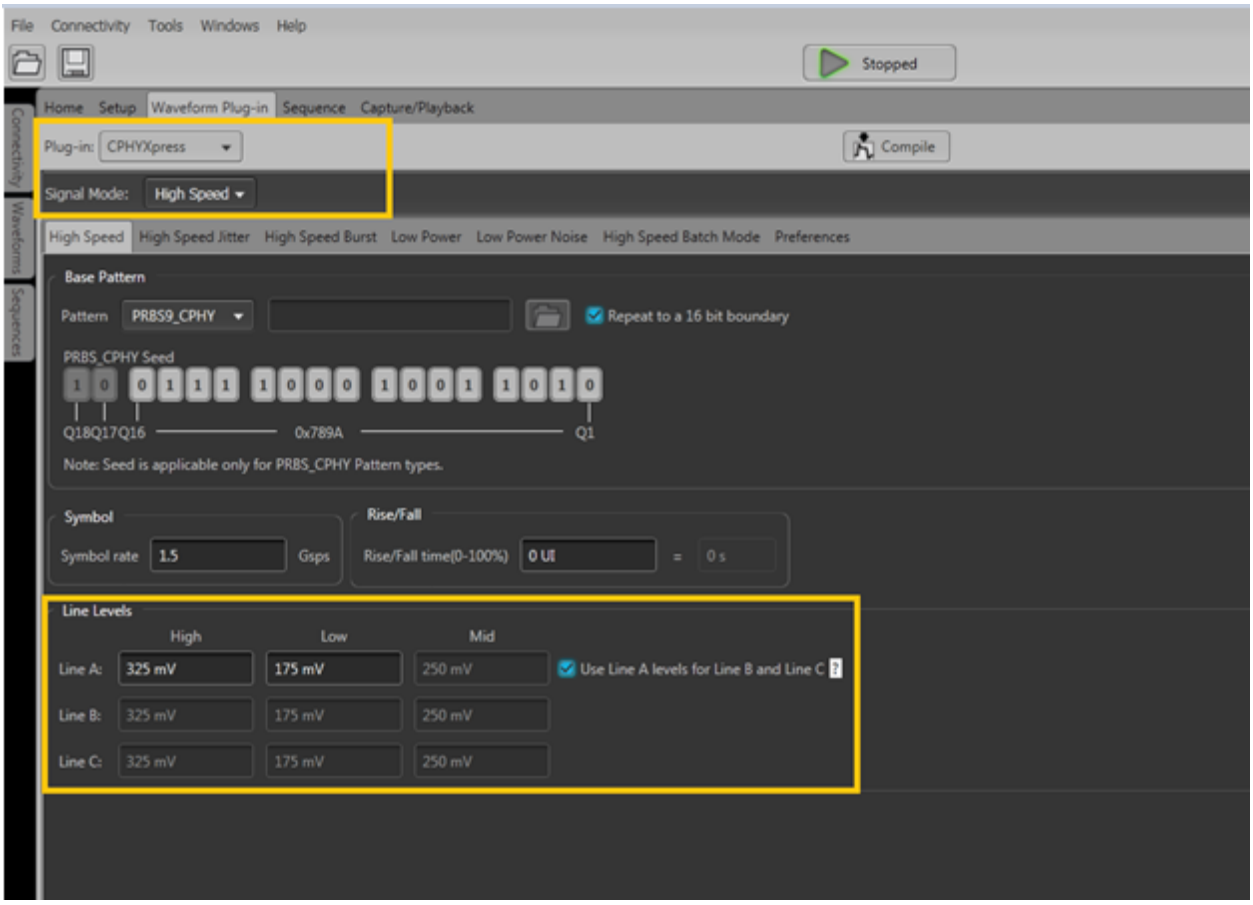
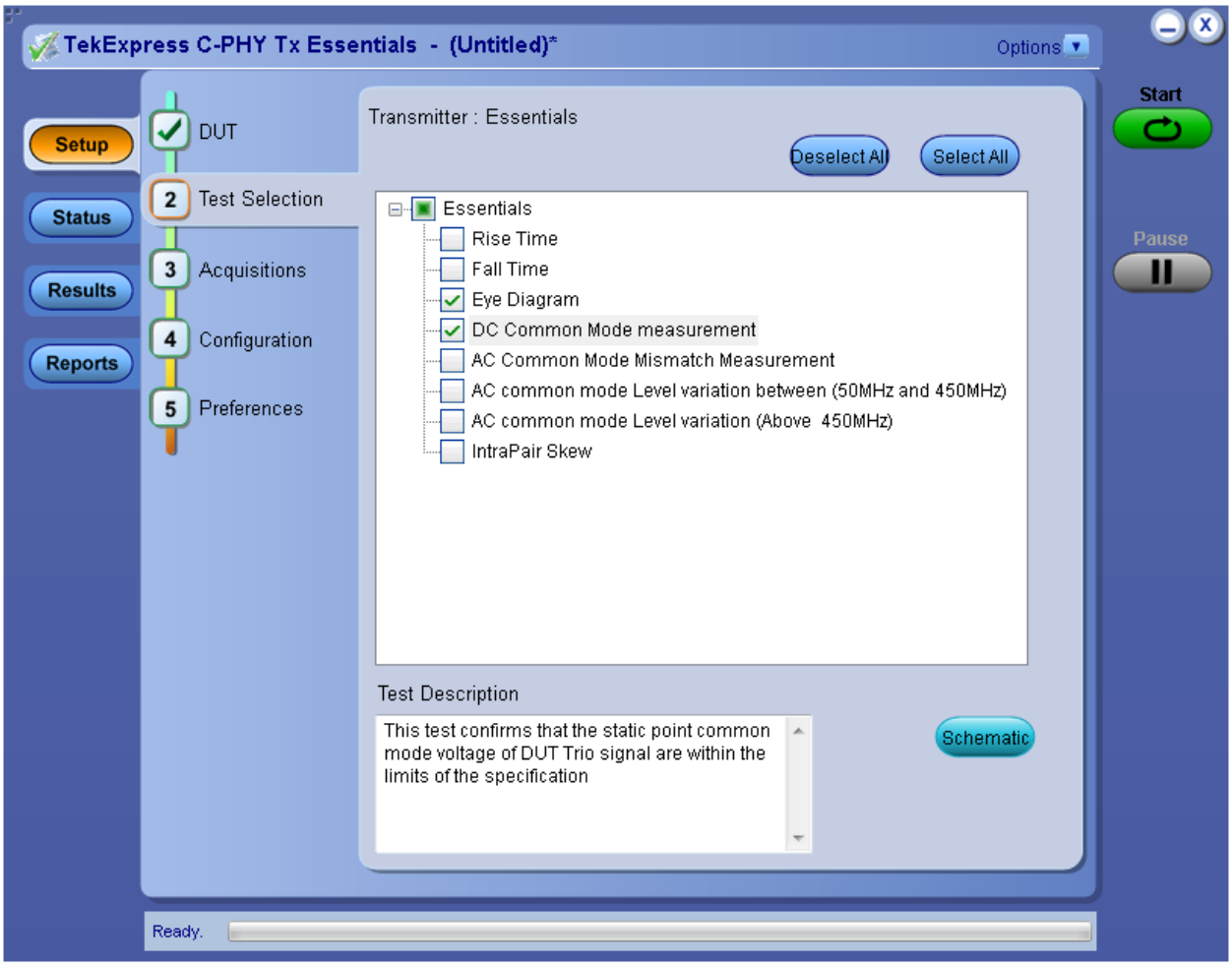


Figure 2.3.2-3: Line level configuration

Measurement details

The following two measurement from the TekExpress C-PHY_Tx Essentials application to be used for this test.

a) Eye Diagram
b) DC Common Mode Measurement



Eye Diagram							
Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
Eye Height of AB	195.0544	mV	Pass	115.0544	80	N.A	-
Eye Height of BC	201.5637	mV	Pass	121.5637	80	N.A	-
Eye Height of CA	207.8915	mV	Pass	127.8915	80	N.A	-
Eye Width of AB	313.2222	ps	Pass	153.2222	160.0000	N.A	-
Eye Width of BC	355.3846	ps	Pass	195.3846	160.0000	N.A	-
Eye Width of CA	332.0000	ps	Pass	172.0000	160.0000	N.A	-
MaskHits of AB	0.0000	Hits	Pass	0.0000	N.A	0	-
MaskHits of BC	0.0000	Hits	Pass	0.0000	N.A	0	-
MaskHits of CA	0.0000	Hits	Pass	0.0000	N.A	0	-
COMMENTS							

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DC Common Mode measurement							
Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
DC Common Mode Voltage	191.5115	mV	Pass	16.5115, 118.4885	175	310	-
COMMENTS							

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Figure 2.3.2-4: CPHY_Tx Essentials application and report example

Test Procedure

1. Beginning with HS line levels of high = 325 mV, low = 175 mV to achieve nominal differential and common mode level. Adjust HS High level and HS Low level on CPHYXpress, to measure the following for using TekXpress CPHY_Tx Essentials.
    a. Eye height of differential AB, BC & CA to be 150 mV (300 mV pk-pk differential voltage).
    b. DC Common Mode Voltage ~ 250mV
2. Transmit the test sequence to the DUT. Verify via any valid observable that the DUT received the test sequence without errors.
3. On CPHYXpress do the following, to reduce the pk-pk differential and maintain the nominal common mode level of 250 mV:
    a. Decrease HS Line level: high by (say 20mV) and
    b. Increase HS Line level: low by the same amount (20 mV)
4. Repeat the steps (2) and (3) until the DUT begins to indicate errors
5. Note the smallest value of the measurement of Eye_Height of AB, BC and CA, for which the DUT was able to receive the test sequence without errors.
6. Compute the half of the minimum of eye height of the three differential waveforms. This value represent the peak differential voltage V_{IDTH}/V_{IDTL}.

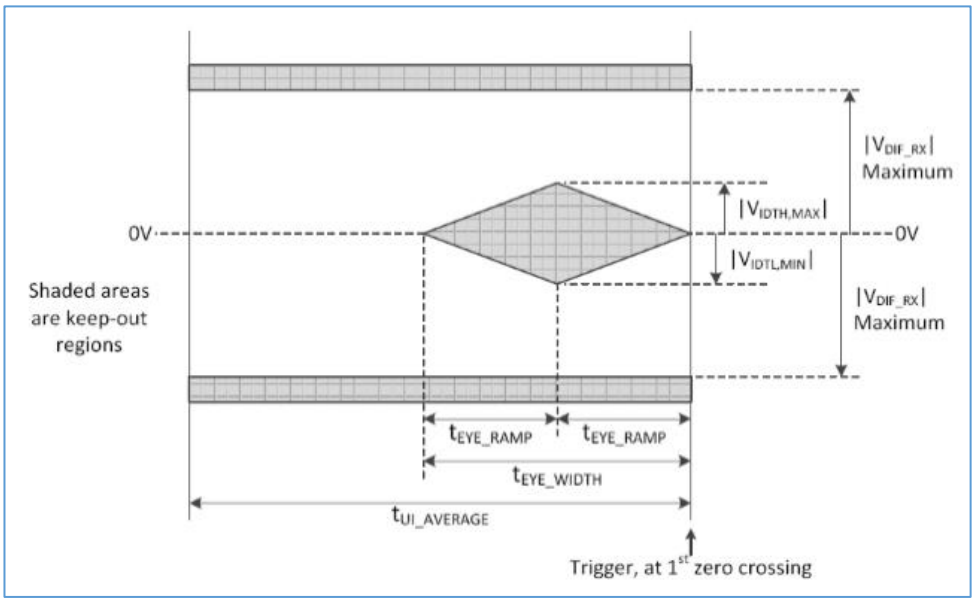
Observable Results

Verify that V_{IDTH}/V_{IDTL} <= 40mV.

Test 2.3.3 – HS-RX Jitter Tolerance

Discussion

C-PHY Specification defines the High Speed Timing requirements in the form of Rx eye diagram, which HS receiver must support. The Rx eye diagram is shown in figure below:

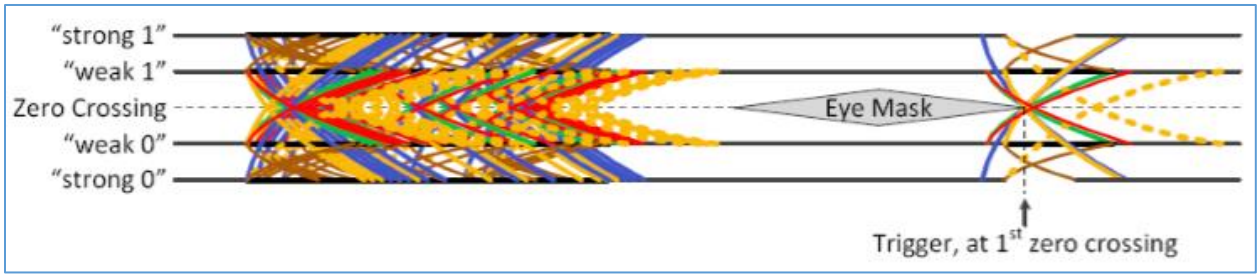


Parameter	Description	Min	Nom	Max	Units	Notes
$t_{EYE\_RAMP\_RX}$	Eye ramp time at the receiver	0.25			UI	
$t_{EYE\_WIDTH\_RX}$	Eye width at the receiver	0.5			UI	
$t_{UI\_AVERAGE}$	UI average		UI_{INST}			

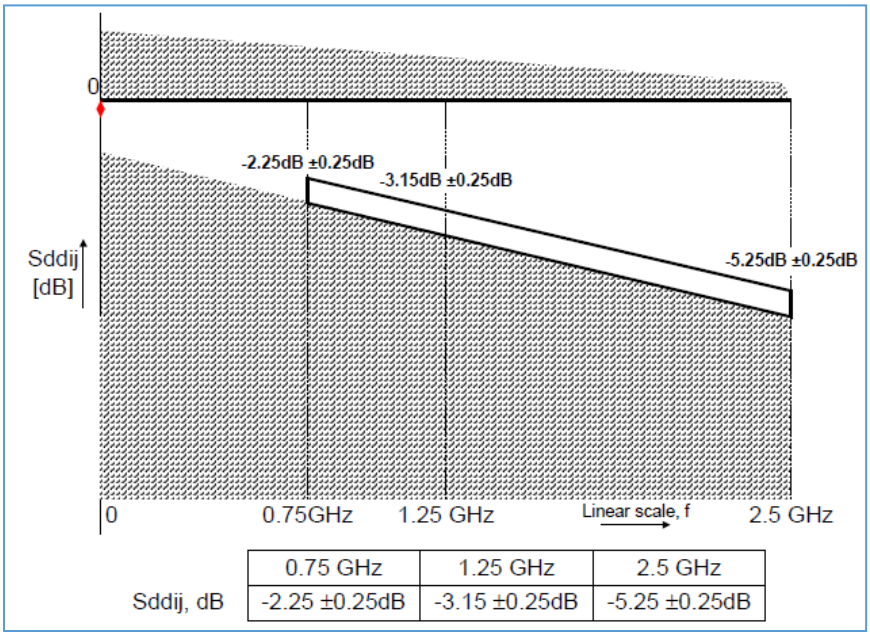
Figure 2.3.3(a): HS Rx Eye Diagram and Timing parameters

In this test, the timing of a test signal will be modified, and the test signal will be sent to the DUT, to see if it can properly receive the signal. The signal will be calibrated using the HS-RX eye diagram as a reference.

The methodology to create the eye diagram for C-PHY signaling is slightly different than for traditional 2-level signaling. C-PHY uses a 'triggered eye' as shown in figure below. Additionally, the eye mask is allowed to be moved horizontally (optimally) to the left (i.e., away from the zero crossing) to a position where there are zero mask hits.

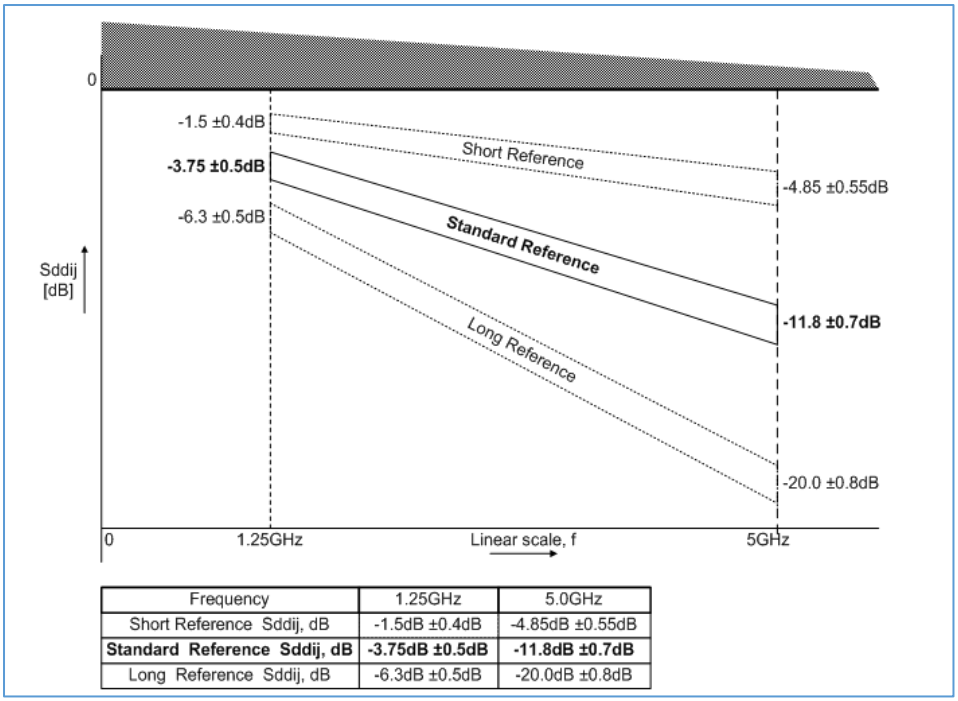


This following reference channel specified in v1.0 is shown in Figure 2.3.3(b).This channel is named as the CPHY Legacy channel in specification v1.1. In addition, three more reference channels which are specified in v1.1, Figure 2.3.3(c).



	0.75 GHz	1.25 GHz	2.5 GHz
Sddij, dB	-2.25 ±0.25dB	-3.15 ±0.25dB	-5.25 ±0.25dB

Figure 2.3.3(b): Legacy Channel



Frequency	1.25GHz	5.0GHz
Short Reference Sddij, dB	-1.5dB ±0.4dB	-4.85dB ±0.55dB
Standard Reference Sddij, dB	**-3.75dB ±0.5dB**	**-11.8dB ±0.7dB**
Long Reference Sddij, dB	-6.3dB ±0.5dB	-20.0dB ±0.8dB

Figure 2.3.3(c): Reference channels – Short, Standard and Long

For the purposes of this test,

1. To test specification v1.0 devices, the CPHY legacy channel is to be used as a reference for testing. Maximum operating as specified in the device datasheet used for this test.
2. To test specification v1.1 devices, Maximum operating as specified in the device datasheet used for this test. Based on this maximum speed and the equalization options, the test channel is chosen as per the table below.

Table 2.3.3-1 Channel Selection Based on Symbol Rate

Channel	TxEQ Option Disabled	TxEQ Option Enabled
Short Reference Channel	1.7Gsps < Rate ≤ 2.5Gsps	2.8Gsps < Rate ≤ 3.0Gsps
Standard Reference Channel	1.3Gsps < Rate ≤ 1.7Gsps	2.0Gsps < Rate ≤ 2.8Gsps
Long Reference Channel	80Msps ≤ Rate ≤ 1.3Gsps	80Msps ≤ Rate ≤ 2.0Gsps

Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: HS
- Maximum symbol rate supported by the DUT is used for this test.
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Line Levels: High = 250 mV and Low = 0 mV

- High Speed Jitter Tab ->Duty cycle distortion
- High Speed Jitter Tab ->Channel embedding vis FLT files

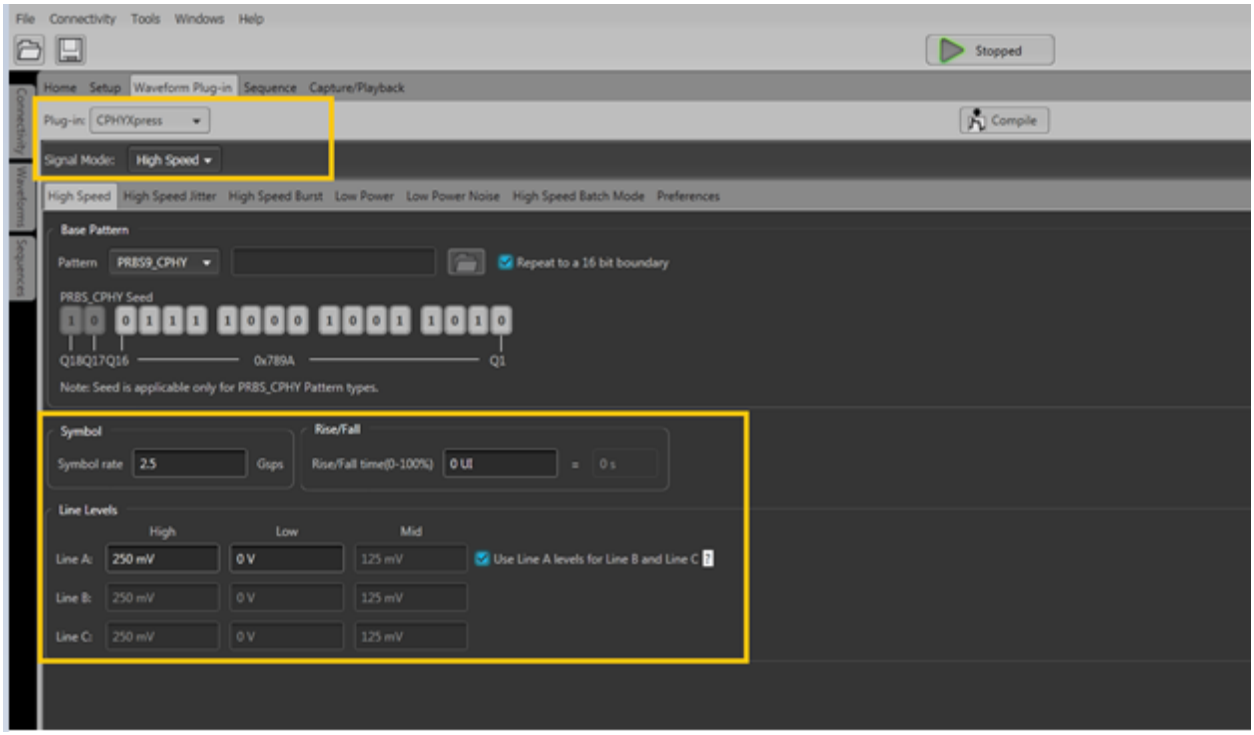


Figure 2.3.3(a): Data rate and Line level configurations

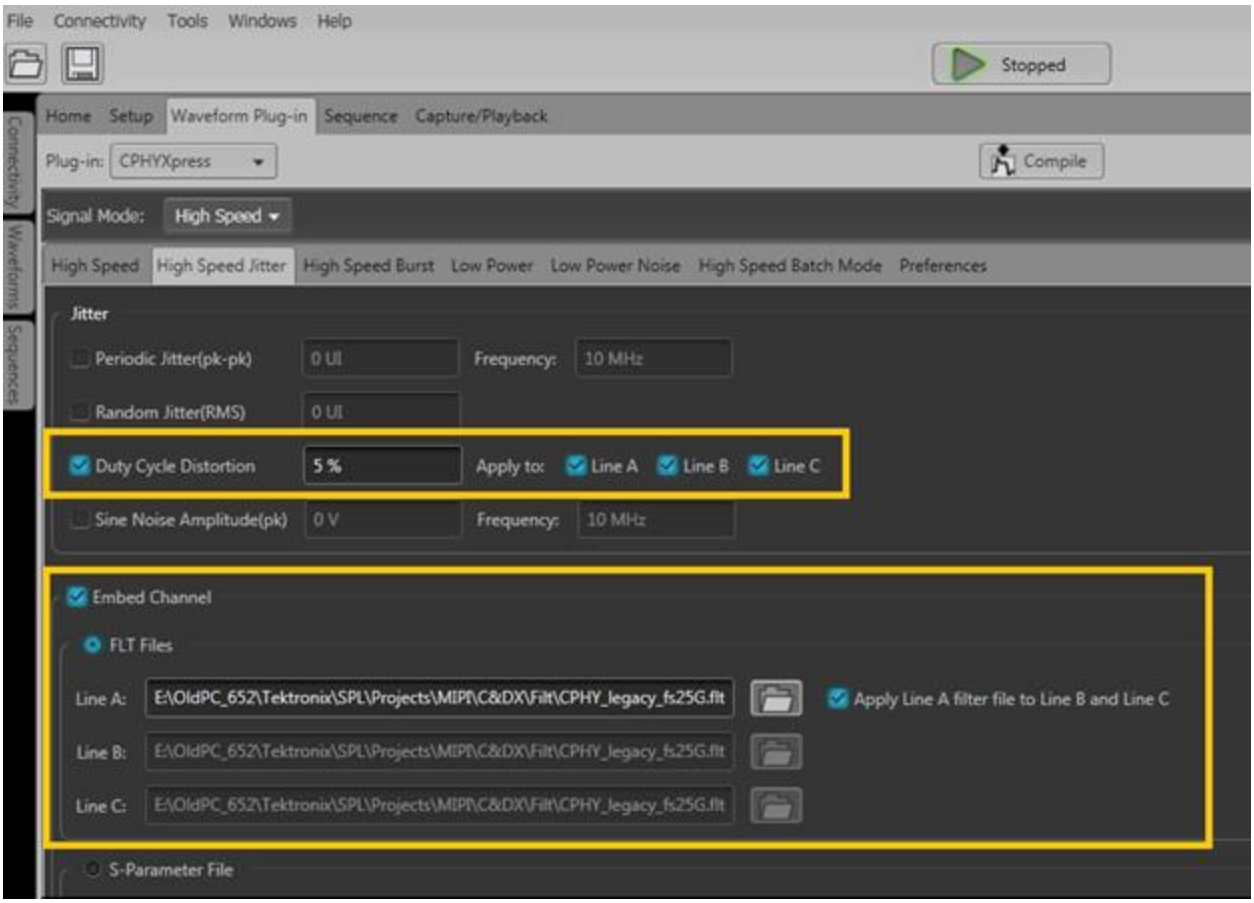
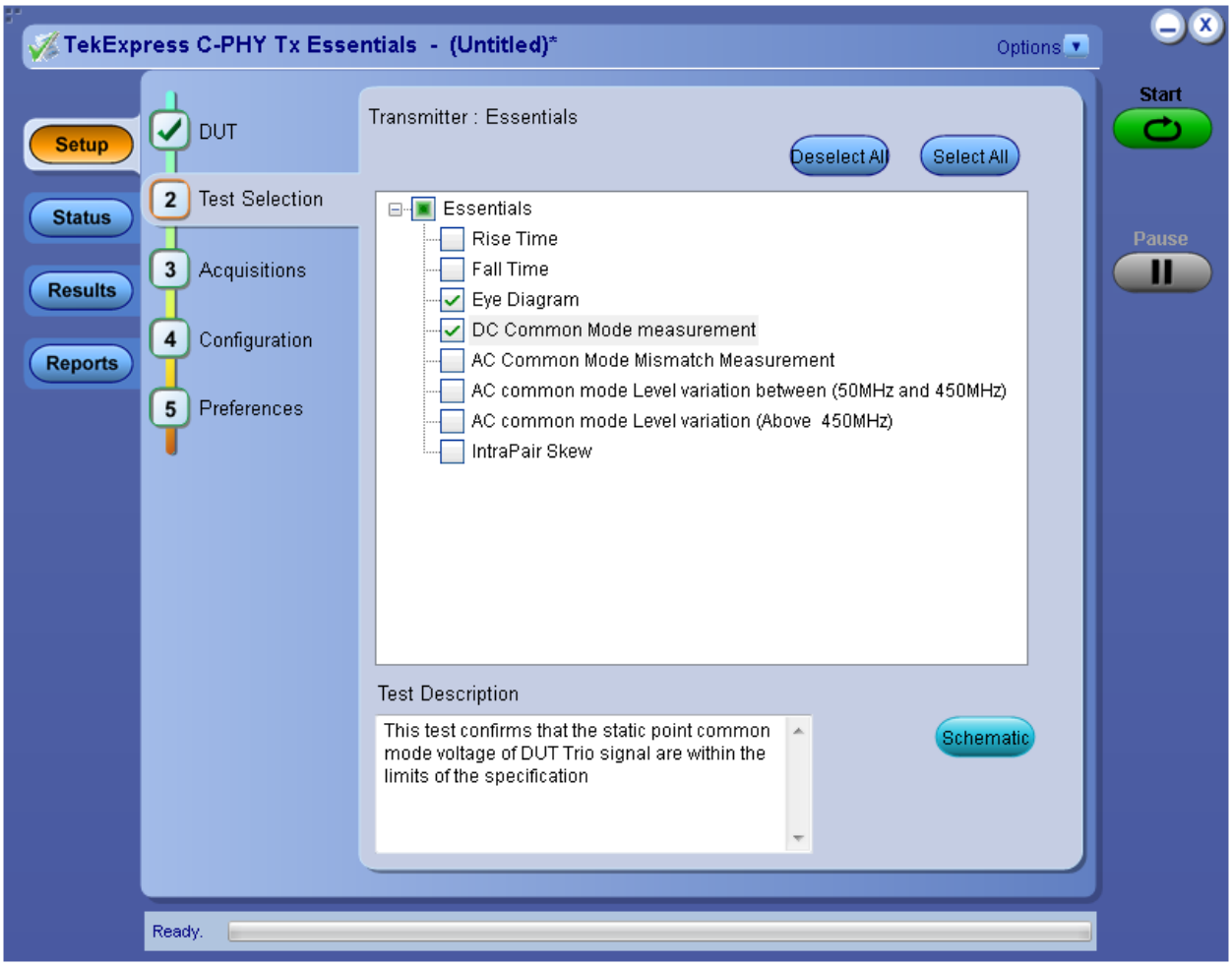


Figure 2.3.3(b): Duty Cycle Distortion and Channel embedding

Measurement details

The following two measurement from the TekXpress CPHY_Tx Essentials application to be used for this test.

a) Eye Diagram
b) DC Common Mode Measurement



Eye Diagram							
Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
Eye Height of AB	195.0544	mV	Pass	115.0544	80	N.A	-
Eye Height of BC	201.5637	mV	Pass	121.5637	80	N.A	-
Eye Height of CA	207.8915	mV	Pass	127.8915	80	N.A	-
Eye Width of AB	313.2222	ps	Pass	153.2222	160.0000	N.A	-
Eye Width of BC	355.3846	ps	Pass	195.3846	160.0000	N.A	-
Eye Width of CA	332.0000	ps	Pass	172.0000	160.0000	N.A	-
MaskHits of AB	0.0000	Hits	Pass	0.0000	N.A	0	-
MaskHits of BC	0.0000	Hits	Pass	0.0000	N.A	0	-
MaskHits of CA	0.0000	Hits	Pass	0.0000	N.A	0	-
COMMENTS							

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DC Common Mode measurement							
Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Comments
DC Common Mode Voltage	191.5115	mV	Pass	16.5115, 118.4885	175	310	-
COMMENTS							

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Figure 2.3.2-4: CPHY_Tx Essentials application and report example

Calibration Procedure

Step	Procedure	Expected Result
1.	Create a PRBS9 pattern with nominal voltages Refer Figure 2.3.3(a) Run TekExpress CPHY-Tx Essentials to perform Eye Diagram measurement.	Eye width<=0.865 UI If Eye width is > 0.865UI adjust the RT/FT to generate signal with Eye width≤0.865UI.
2.	Add the C-PHY Reference channel. Refer Figure 2.3.3(b)	
3.	Add the DCD in increments until the Eye width is approximately ~ 0.5 UI and adjust the amplitude (Line Levels) to achieve Eye height: +40mVpk. Move the mask horizontally so that it is aligned on the Right side without any hits on the signal (This is taken care by TekExpress CPHY-Tx Essentials).	Eye WIDTH reduced to ~0.5UI and Eye Height to ~+40mVpk Ensure than there are minimal or no Mask hits.
4.	Calibrate for DC Common Mode by adjusting the bias Tee voltage. This test is required to be formed for multiple cases of DC common mode voltage. Testcase#1: V_{CPTX} = 250mV Testcase#2: V_{CPTX} = 175mV Testcase#3: V_{CPTX} = 310mV Run TekExpress CPHY-Tx essentials to perform DC common mode measurement.	V_{CPTX} based on the test case

Test Procedure

1. The calibrated stimulus is fed to the DUT.
2. Transmit the test sequence to the DUT. Verify via any valid observable that the DUT received the test sequence without errors.
3. Repeat the test for all the three cases of DC common mode listed in step 4 of the calibration table above.

Note: Low BER will not be verified. Each test case will be performed using a target BER of 1E-10 and a confidence level of 95% (i.e., 3E10 bits). This corresponds to approximately 20 seconds per test case (assuming a bit rate of 3.35Gbps (1.5Gsps), and a line utilization of 50%, i.e., one burst-width of LP between bursts).

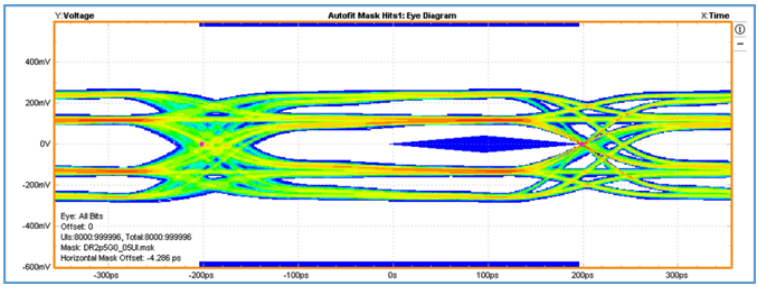
Observable Results

Verify that for all three test cases that the test sequence was received by the DUT without error.

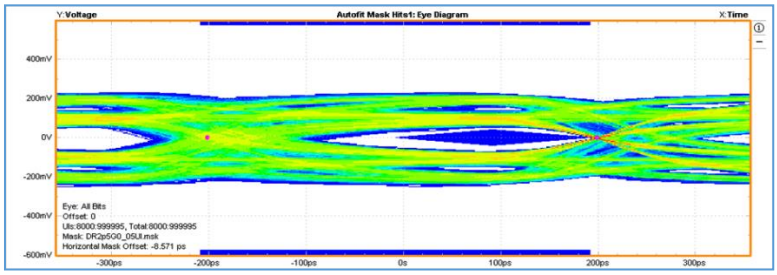
Example Result

Following are the result after each step of the calibration routine described above for a PRBS9 test sequence at symbol rate of 2.5Gbps

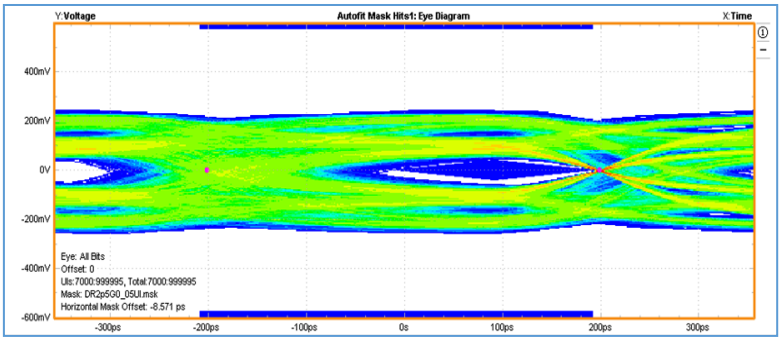
1) Differential Eye diagram with Nominal Voltage. Eye width is about 344psec (0.86UI).



2) Slow down the RT/FT and add the reference channel (Legacy channel in this example). Eye width is reduced to 269psec (0.67UI)



3) Add the DCD and adjust amplitude to achieve target eye width and eye height. Eye width is reduced to 215psec (0.53UI).


Y: Voltage
Autofit Mask Hits1: Eye Diagram
X: Time
400mV
200mV
0V
-200mV
-400mV
-600mV
Eye: All Bits
Offset: 0
UIs:7000:999995, Total:7000:999995
Mask: DR2p5G0_05UI.msk
Horizontal Mask Offset: -8.571 ps
-300ps
-200ps
-100ps
0s
100ps
200ps
300ps

GROUP 4: HS-RX TIMER REQUIREMENTS

Test/Calibration Setup

If any of the signal parameters of interest needs calibration, for this purpose the calibration setup should include with termination board. See section LP Signal Calibration Setup .

Test 2.4.1 – HS-RX T3-TERM-EN Duration

Discussion

C-PHY Specification mentions the maximum time within which the slave has to enable HS line termination.

$t_{3\text{-TERM-EN}}$	Time for the slave to enable the HS line termination, starting from the time point when the A, B and C wire cross V_{IL_MAX}	Note 5	38	ns	3

3. *Receiver-specific parameter.*
4. *The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.*
5. *As specified in Section 9.2.1, the receiver termination impedances shall not be enabled until the single-ended voltages on all of A, B and C fall below $V_{TERM-EN}$.*

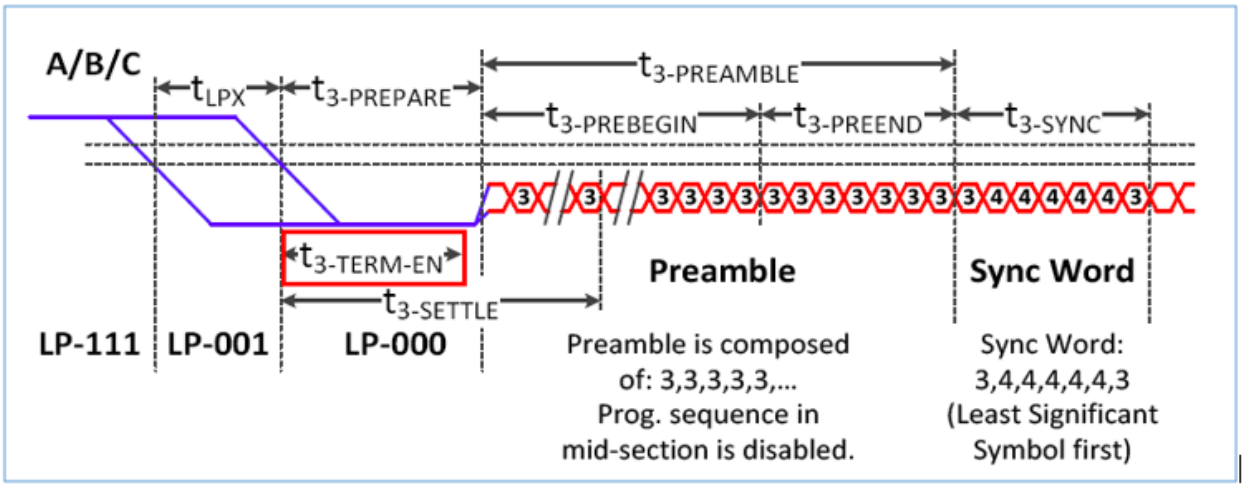


Figure: 2.4.1(a) Termination enable duration definition

Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: LowPower_HighSpeed
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz
- Low Power: Set LP-000 duration(t3_PREPARE) = 2 LP symbols(implying Prepare time of 100 nsec)

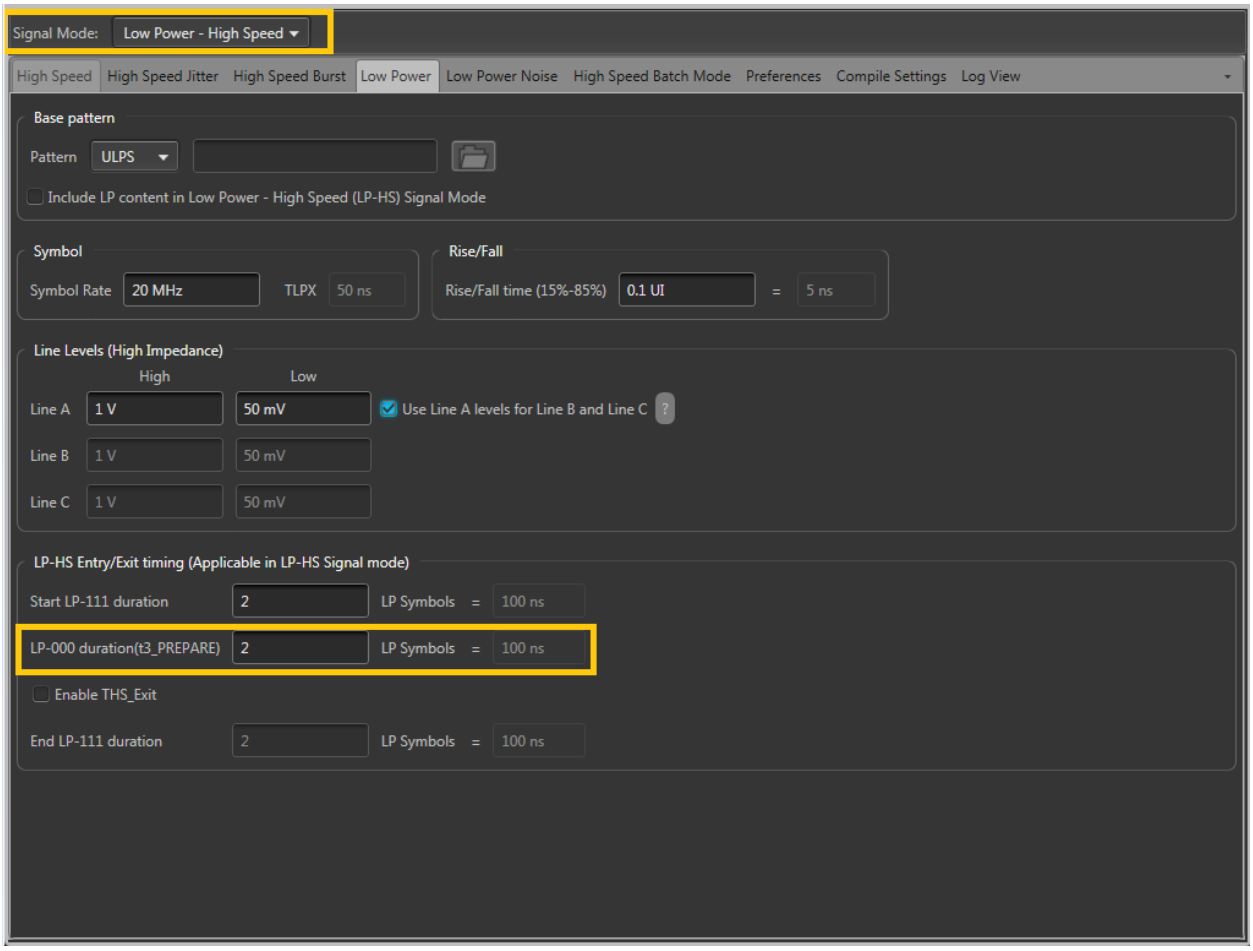


Figure: 2.4.2(a) LP Tab Configuration

Measurement details

The $T_{3\text{-TERM-EN}}$ interval begins at the point where the LP-00 falling edge (on line C) crosses $V_{IL,MAX}$ (550mV), and ends at the point when the HS line termination is enabled. As described in the CTS, the exact point when HS line termination is considered enabled is subjective. The text in the CTS is reproduced below – *"Note that the exact point when the HS line termination is considered "enabled" can be somewhat subjective in some cases, as the voltage spike that typically occurs on the line when the termination is enabled does not necessarily have a well-defined shape (and in some cases may not be visible at all). For the purposes of this test, the measurement point for the termination-enable voltage spike is defined as the maximum voltage point of the spike (as opposed to the 'start' of the spike, which can be even more difficult to clearly identify.) For devices with sufficient margin in their $T_{3\text{-TERM-EN}}$ timer values, the impact of any potential measurement uncertainty should be minimal" [2]*

$T_{3\text{-TERM-EN}}$ interval is measured on the Line C waveform using the cursors as shown below

Test Procedure

1) Test setup: Similar to other Rx tests the DUT is connected waveform generator. However, the DUT behavior is assessed by measuring the signal captured on an oscilloscope by probing at the Rx pins.
2) Generate a LP_HS waveform with signal parameters listed in the above section.
3) Transmit the test sequence to the DUT and capture the signal at the Rx pins on the oscilloscope.
4) $T_{3\text{-TERM-EN}}$ interval is measured on the captured on the line C waveform as described above.

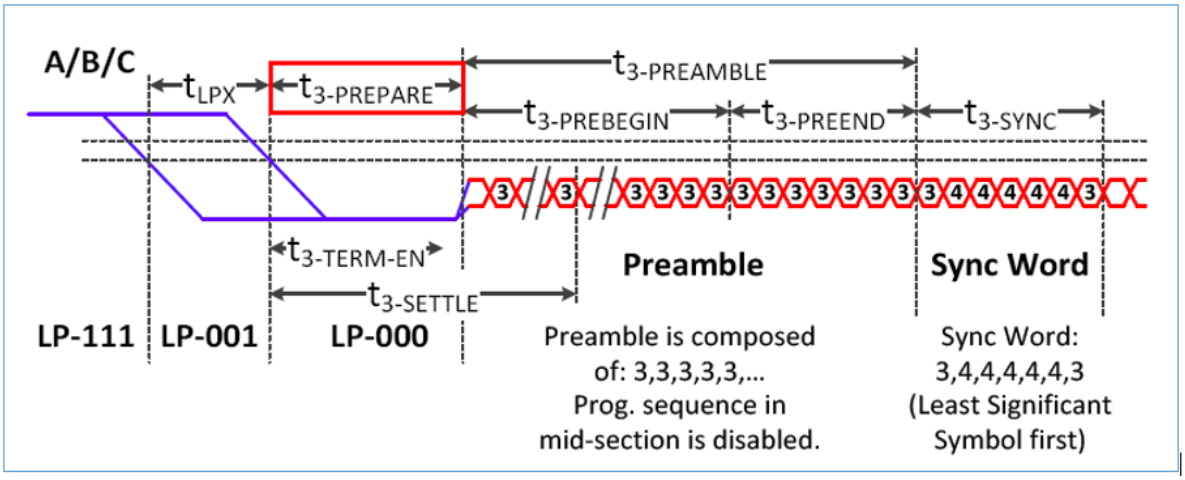
Observable Results

Verify that $T_{3\text{-TERM-EN}}$ is less than 38ns.

Test 2.4.2 – HS-RX T3-PREPARE Tolerance

Discussion

This test is to verify that the DUT's HS-RX can tolerate reception of conformant values for $T_{3\text{-PREPARE}}$. Shown below is the requirements for $T_{3\text{-PREPARE}}$ interval, which is required to understand switching a lane into HS mode.



Given below are the $T_{3\text{-PREPARE}}$ interval definition, and conformance limits and test cases will be performed using the TX values maximum of 95 ns and minimum 38 ns.

Table 18 Global Operation Timing Parameters

Parameter	Description	Min	Max	Unit	Notes
$t_{3\text{-PREPARE}}$	Time that the transmitter drives the 3-wire LP-000 line state immediately before the HS_+x line state starting the HS transmission.	38	95	ns	2

Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: LowPowerHighSpeed
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz
- Low Power: Set LP-000 duration (t3_PREPARE) to be configured based on the test case. The minimum and maximum t3_PREPARE is achieved by the configuration shown in Table 2.4.2(b). This setting in the application is shown in Figure 2.4.2(c)
- Nominal burst parameters for the HS burst for this test is listed below and also shown in Figure 2.4.2(b)
    - High Speed Burst: PreBegin Pattern = 3333333.
    - High Speed Burst: PREBEGIN Repeat = 63.
    - High Speed Burst: ProgSeq = Disabled.

- High Speed Burst: PreEnd Pattern = 3333333.
- High Speed Burst: PreEnd Repeat = 0.
- High Speed Burst: SYNC = 3444443.
- High Speed Burst: Sync word Repeat = 7 symbols.
- High Speed Burst: POST pattern = 4444444.
- High Speed Burst: POST Repeat = 224 Symbols.

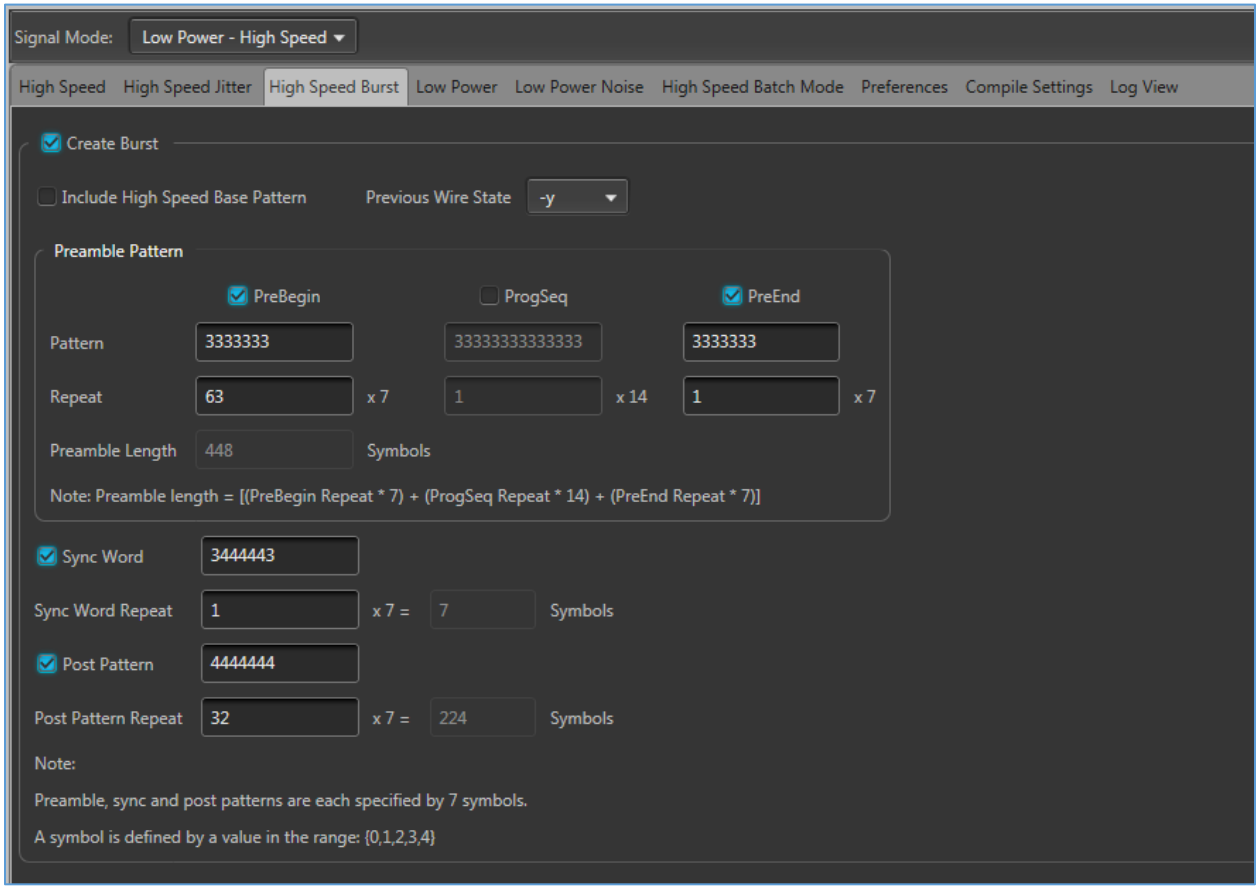


Figure: 2.4.2(a) HS Burst settings

Test Case #	$T_{3\text{-PREPARE}}$	LP-000 duration [Setting on CPHYXpress]	Notes
1	38ns	0.8 LP symbols	Minimum $T_{3\text{-PREPARE}}$
2	95ns	1.9 LP symbols	Maximum $T_{3\text{-PREPARE}}$

Table: 2.4.2(b) T3_PREPARE configuration values on CPHYXPress

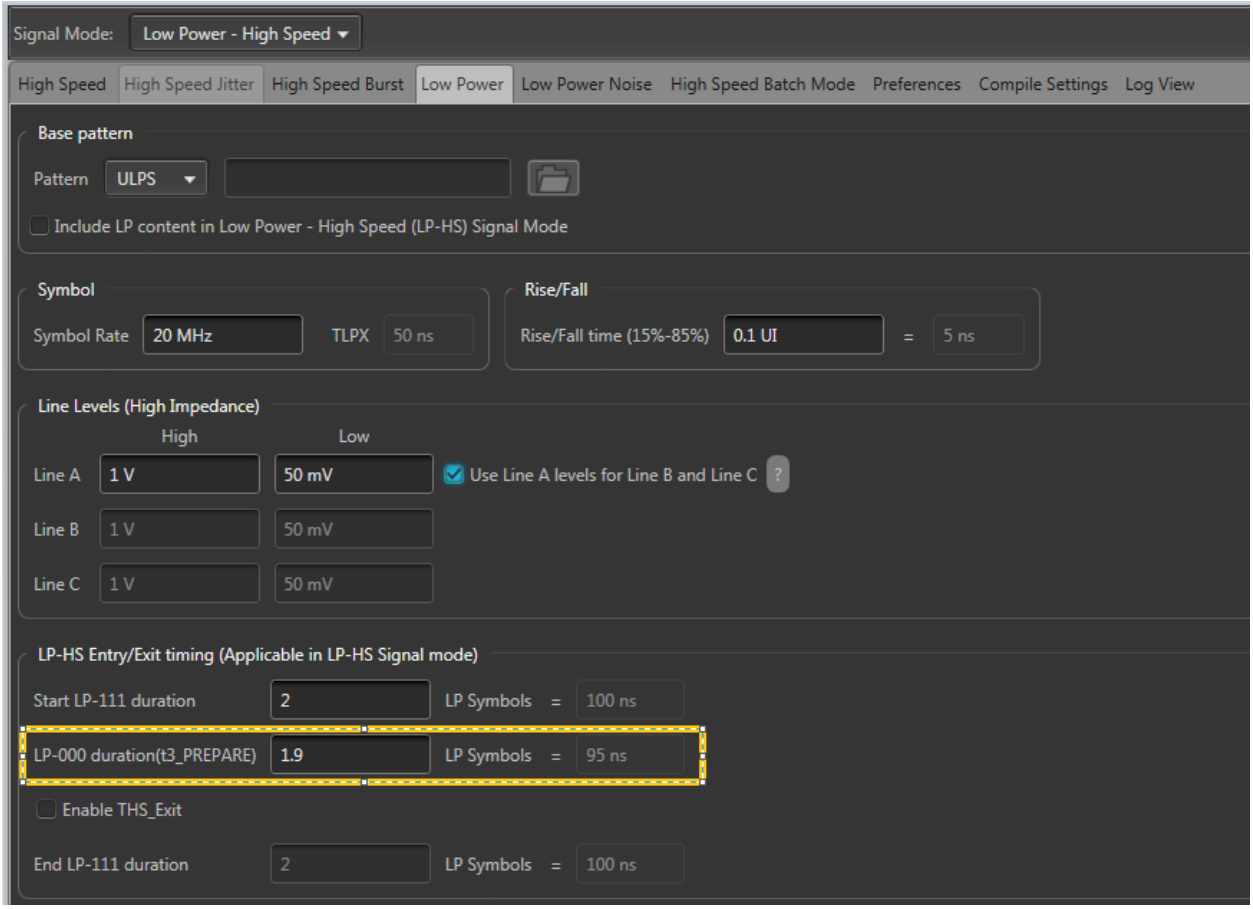


Table: 2.4.2(c) LP tab setting of T3_PREPARE to achieve a maximum of 95 nsec

Test Procedure

1. Generate a LP_HS waveform with signal parameter listed above (for testcase1).
2. Verify via any valid observable that the DUT received the test sequence without errors.
3. Repeat the above steps for Testcase2.

Observable Results

Verify via any valid observable that the DUT received the test sequence without errors.

Example Result

The test waveform with maximum T3_PREPARE of 95 nsec is shown below.

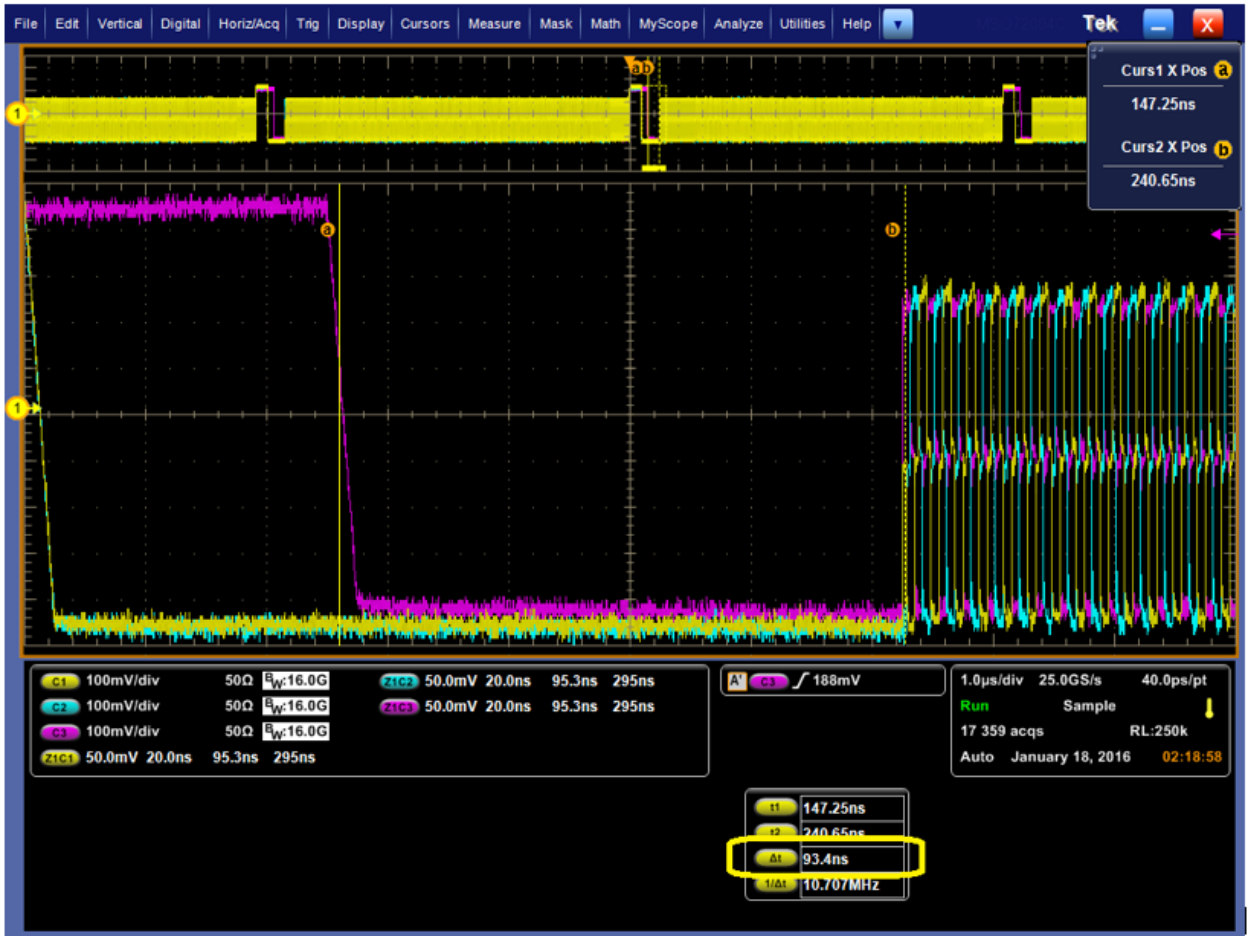
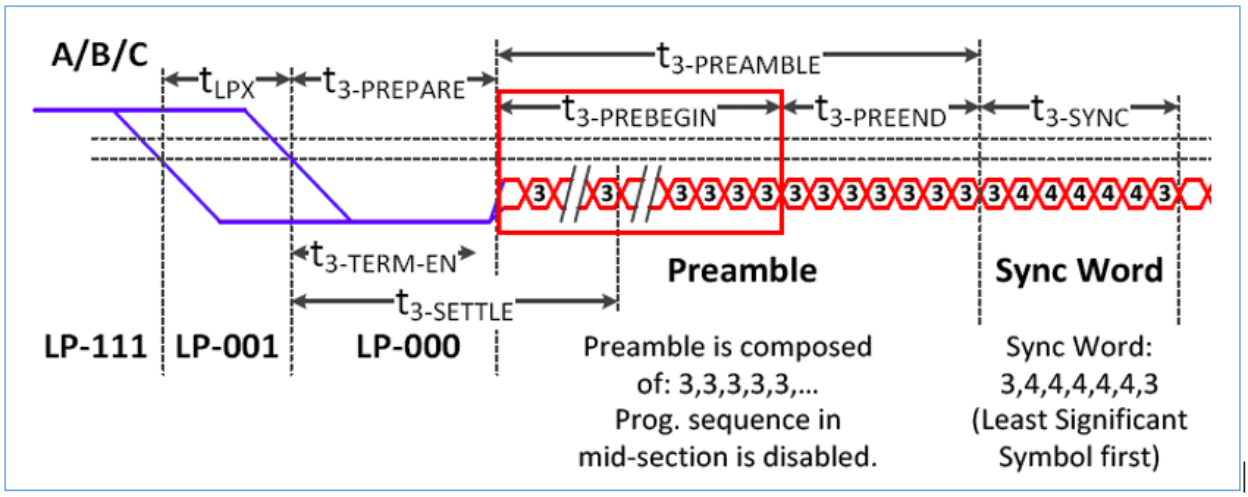


Figure: 2.4.2(d) Measured 95 ns as maximum t3 Prepare conformance limit

Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance

Discussion

$T_{3\text{-PREBEGIN}}$ has a range of 1 to 64 words that is 7 to 448 UI. The Rx needs to recognize the presence of PREBEGIN for a length within the range specified.



T_{LPX}	$T_{3\text{-PREPARE}}$	$T_{3\text{-PROGSEQ}}$	$T_{3\text{-PREEND}}$	$T_{3\text{-SYNC}}$	$T_{3\text{-POST}}$
50ns	70ns	Disabled (0UI)	7UI	7UI	112UI

Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: LowPower_HighSpeed
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz, resulting TLPX of 50ns
- Low Power: Set LP-000 duration (t3_PREPARE) is set to 1.4 symbols to achieve 70ns, which is used as the nominal setting for this test.
- Nominal burst parameters for the HS burst for this test is listed below
    - High Speed Burst: PreBegin Pattern = 3333333.
    - High Speed Burst: PREBEGIN Repeat = 1 (i.e. 7 Symbols)
    - High Speed Burst: ProgSeq = Disabled.
    - High Speed Burst: PreEnd Pattern = 3333333.
    - High Speed Burst: PreEnd Repeat = 1 (i.e. 7 Symbols)
    - High Speed Burst: SYNC = 3444443.
    - High Speed Burst: Sync word Repeat = 1

- High Speed Burst: POST pattern = 4444444.
- High Speed Burst: POST Repeat = 16 (i.e. 224 Symbols)

➢ High Speed Batch Mode: Parameter-> PreBegin Repeat. Start, end and Increment values are set as shown in the Figure 2.4.3(a).

- With this setting multiple waveforms are created with increasing lengths of PreBegin.
- A waveform sequence is created in the AWG, to step through the waveforms for testing with varying PreBegin lengths. Waveform sequence is shown in Figure 2.4.3(b)

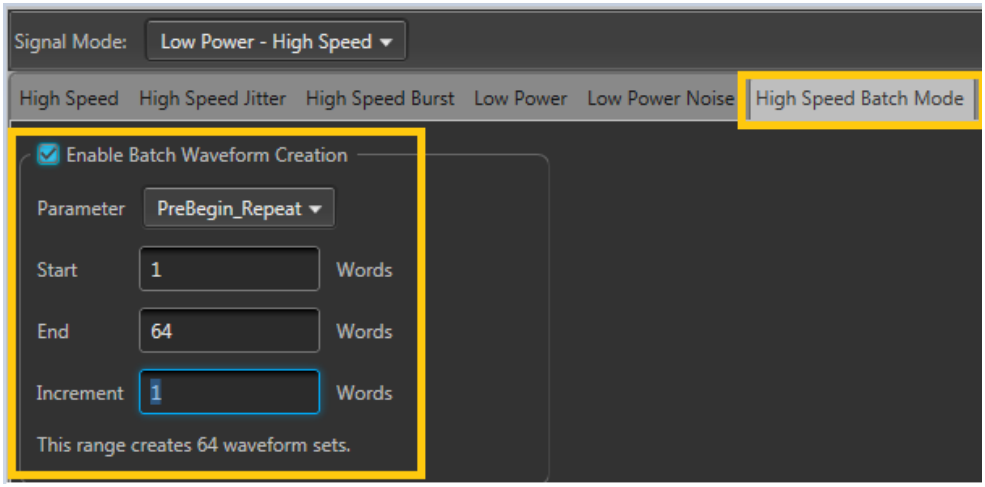
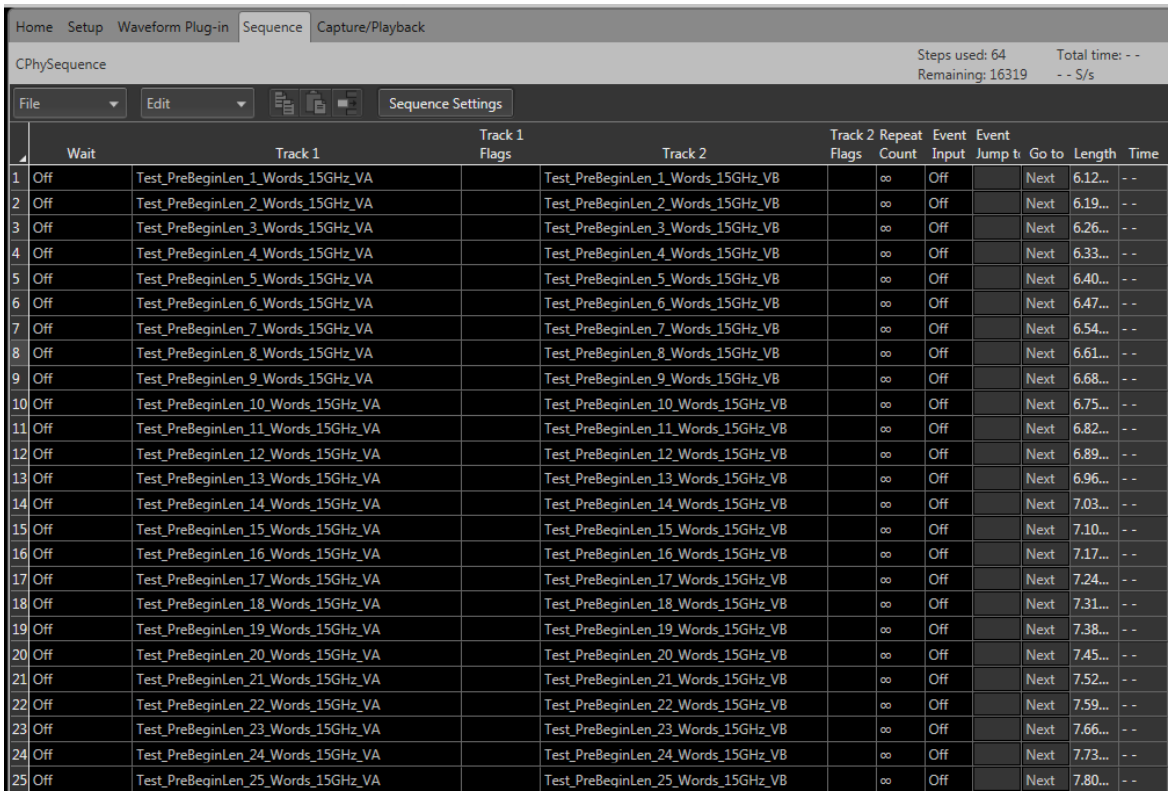


Figure: 2.4.3(a) HS Batch Mode Configuration



	Wait	Track 1	Track 1 Flags	Track 2	Track 2 Flags	Repeat Count	Event Input	Event Jump t	Go to	Length	Time
1	Off	Test_PreBeginLen_1_Words_15GHz_VA		Test_PreBeginLen_1_Words_15GHz_VB		∞	Off		Next	6.12...	- -
2	Off	Test_PreBeginLen_2_Words_15GHz_VA		Test_PreBeginLen_2_Words_15GHz_VB		∞	Off		Next	6.19...	- -
3	Off	Test_PreBeginLen_3_Words_15GHz_VA		Test_PreBeginLen_3_Words_15GHz_VB		∞	Off		Next	6.26...	- -
4	Off	Test_PreBeginLen_4_Words_15GHz_VA		Test_PreBeginLen_4_Words_15GHz_VB		∞	Off		Next	6.33...	- -
5	Off	Test_PreBeginLen_5_Words_15GHz_VA		Test_PreBeginLen_5_Words_15GHz_VB		∞	Off		Next	6.40...	- -
6	Off	Test_PreBeginLen_6_Words_15GHz_VA		Test_PreBeginLen_6_Words_15GHz_VB		∞	Off		Next	6.47...	- -
7	Off	Test_PreBeginLen_7_Words_15GHz_VA		Test_PreBeginLen_7_Words_15GHz_VB		∞	Off		Next	6.54...	- -
8	Off	Test_PreBeginLen_8_Words_15GHz_VA		Test_PreBeginLen_8_Words_15GHz_VB		∞	Off		Next	6.61...	- -
9	Off	Test_PreBeginLen_9_Words_15GHz_VA		Test_PreBeginLen_9_Words_15GHz_VB		∞	Off		Next	6.68...	- -
10	Off	Test_PreBeginLen_10_Words_15GHz_VA		Test_PreBeginLen_10_Words_15GHz_VB		∞	Off		Next	6.75...	- -
11	Off	Test_PreBeginLen_11_Words_15GHz_VA		Test_PreBeginLen_11_Words_15GHz_VB		∞	Off		Next	6.82...	- -
12	Off	Test_PreBeginLen_12_Words_15GHz_VA		Test_PreBeginLen_12_Words_15GHz_VB		∞	Off		Next	6.89...	- -
13	Off	Test_PreBeginLen_13_Words_15GHz_VA		Test_PreBeginLen_13_Words_15GHz_VB		∞	Off		Next	6.96...	- -
14	Off	Test_PreBeginLen_14_Words_15GHz_VA		Test_PreBeginLen_14_Words_15GHz_VB		∞	Off		Next	7.03...	- -
15	Off	Test_PreBeginLen_15_Words_15GHz_VA		Test_PreBeginLen_15_Words_15GHz_VB		∞	Off		Next	7.10...	- -
16	Off	Test_PreBeginLen_16_Words_15GHz_VA		Test_PreBeginLen_16_Words_15GHz_VB		∞	Off		Next	7.17...	- -
17	Off	Test_PreBeginLen_17_Words_15GHz_VA		Test_PreBeginLen_17_Words_15GHz_VB		∞	Off		Next	7.24...	- -
18	Off	Test_PreBeginLen_18_Words_15GHz_VA		Test_PreBeginLen_18_Words_15GHz_VB		∞	Off		Next	7.31...	- -
19	Off	Test_PreBeginLen_19_Words_15GHz_VA		Test_PreBeginLen_19_Words_15GHz_VB		∞	Off		Next	7.38...	- -
20	Off	Test_PreBeginLen_20_Words_15GHz_VA		Test_PreBeginLen_20_Words_15GHz_VB		∞	Off		Next	7.45...	- -
21	Off	Test_PreBeginLen_21_Words_15GHz_VA		Test_PreBeginLen_21_Words_15GHz_VB		∞	Off		Next	7.52...	- -
22	Off	Test_PreBeginLen_22_Words_15GHz_VA		Test_PreBeginLen_22_Words_15GHz_VB		∞	Off		Next	7.59...	- -
23	Off	Test_PreBeginLen_23_Words_15GHz_VA		Test_PreBeginLen_23_Words_15GHz_VB		∞	Off		Next	7.66...	- -
24	Off	Test_PreBeginLen_24_Words_15GHz_VA		Test_PreBeginLen_24_Words_15GHz_VB		∞	Off		Next	7.73...	- -
25	Off	Test_PreBeginLen_25_Words_15GHz_VA		Test_PreBeginLen_25_Words_15GHz_VB		∞	Off		Next	7.80...	- -

Figure: 2.4.3(b) AWG Sequence showing Line A and Line B waveforms in Track1 & Track2 respectively

Test Procedure

1. Generate a Low Power-High Speed waveform with signal parameter listed above (PREBEGIN Repeat =1) using CPHYXpress.
2. Transmit the test sequence to the DUT and Verify via any valid observable that the DUT received the data without errors.
3. Increase the PREBEGIN Repeat by 1 (7 symbols), this is done by playing out the next wfm in the AWG sequence. Repeat this process, until the DUT successfully and consistently receives the HS image data without error.
4. Record the (PREBEGIN Repeat value x 7) as the DUT's $T_{3\text{-PREBEGIN}}$ detection threshold in symbols or UI.

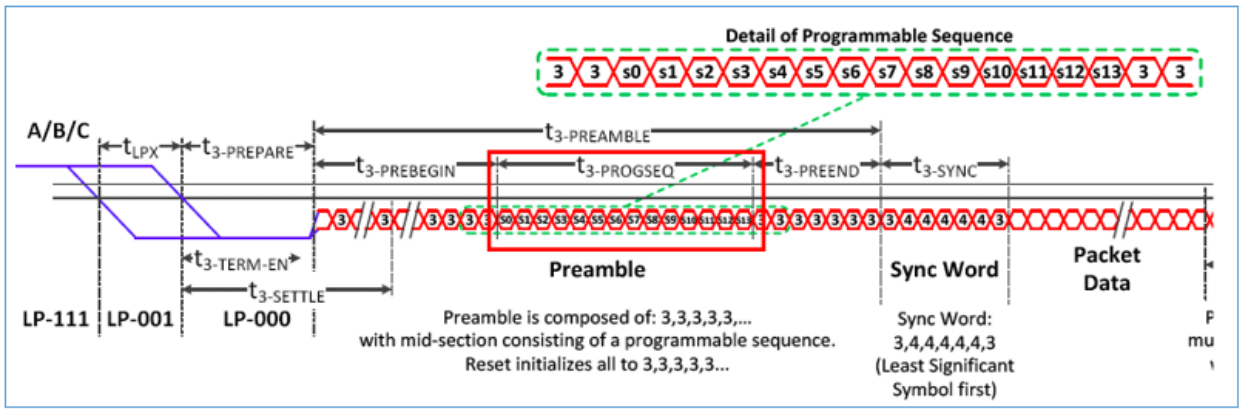
Observable Results

Verify that the DUT's $T_{3\text{-PREBEGIN}}$ detection threshold is between 1 and 64 words (i.e. that is 7 and 448UI.)

Test 2.4.4 – HS-RX T3-PROGSEQ Tolerance

Discussion

A programmable sequence of 14 symbols ($T_{3\text{-}PROGSEQ}$) is allowed as a part of the burst. This test is check for the performance of the Rx in presence of this sequence (shown in the figure below)



Signal parameters

The relevant parameters of the CPHYXpress application for this test are listed below and also highlighted in the screenshot

- Signal Mode: LowPower_HighSpeed
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz, , resulting TLPX of 50ns
- Low Power: Set LP-000 duration (t3_PREPARE) is set to 1.4 symbols to achieve 70ns, which is used as the nominal setting for this test.
- Nominal burst parameters for the HS burst for this test is listed below and also shown in Figure 2.4.4(a)
    - High Speed Burst: PreBegin Pattern = 3333333.
    - High Speed Burst: PREBEGIN Repeat = 16 (i.e. 112 Symbols)
    - High Speed Burst: ProgSeq = Enabled.
    - High Speed Burst: ProgSeq = Enabled, and set to 43434343434343
    - High Speed Burst: PreEnd Pattern = 3333333.
    - High Speed Burst: PreEnd Repeat = 1 (i.e. 7 Symbols)
    - High Speed Burst: SYNC = 3444443.
    - High Speed Burst: Sync word Repeat = 1 (i.e. 7 Symbols)
    - High Speed Burst: POST pattern = 4444444.
    - High Speed Burst: POST Repeat = 16 (i.e. 112 Symbols)

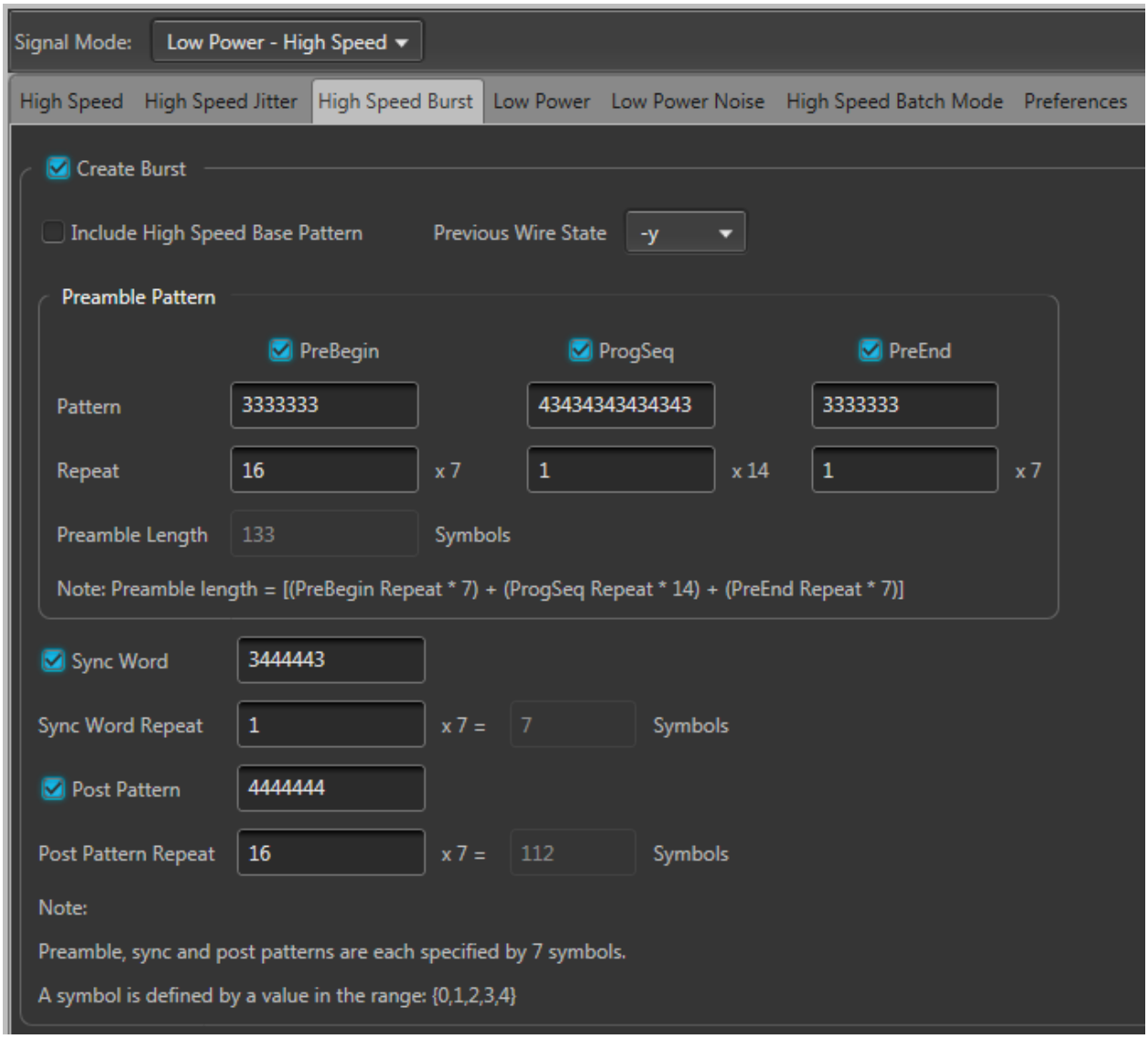


Figure 2.4.4(a) High Speed Burst settings

Test procedure

1. Generate a Low Power-High Speed waveform with signal parameter listed above using CPHYXpress.
2. Transmit the test sequence to the DUT and Verify via any valid observable that the DUT received the data without errors

Test 2.4.5 – HS-RX T3-POST Tolerance

[This test is similar to Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance. In this test tolerance of the Rx with regard to the length of the Post (T_{3_POST}) is checked for]

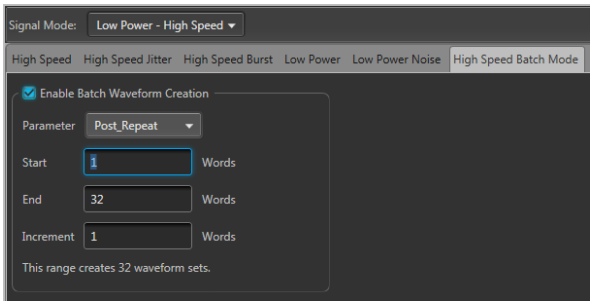
Discussion

The range for the length of the POST sequence is defined as 7 to 224 UI.

Signal parameters

The setting are similar to that in Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance, with now focus on the Post length

- Signal Mode: LowPower-HighSpeed
- HS Base Pattern: PRBS9_CPHY or based on the DUT
- Low Power: Symbol rate = 20MHz, resulting TLPX of 50ns
- Low Power: Set LP-000 duration (t3_PREPARE) is set to 1.4 symbols to achieve 70ns, which is used as the nominal setting for this test.
- Nominal burst parameters for the HS burst for this test is listed below and also shown in Figure 2.4.2(b)
  - High Speed Burst: PreBegin Pattern = 3333333.
  - High Speed Burst: PREBEGIN Repeat = 16 (i.e. 112 Symbols)
  - High Speed Burst: ProgSeq = Disabled.
  - High Speed Burst: PreEnd Pattern = 3333333.
  - High Speed Burst: PreEnd Repeat = 1 (i.e. 7 Symbols)
  - High Speed Burst: SYNC = 3444443.
  - High Speed Burst: Sync word Repeat = 1
  - High Speed Burst: POST pattern = 4444444.
  - High Speed Burst: POST Repeat = 1 (i.e. 7 Symbols)
- High Speed Batch Mode: Parameter-> Post Repeat. Start, end and Increment values are set as shown in the Figure 2.4.3(a).
  - With this setting multiple waveforms are created with increasing lengths of Post.
  - A waveform sequence is created in the AWG, to step through the waveforms for testing with varying Post lengths. Waveform sequence is shown in Figure 2.4.3(b)



Test Procedure

Refer to Test Procedure in Test 2.4.3 – HS-RX T3-PREBEGIN Tolerance

Appendix A – Supported list of tests

Test Number	Test Name	Supported
Test 2.1.1	LP-RX Logic 1 Input Voltage (VIH)	Yes
Test 2.1.2	LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	Yes
Test 2.1.3	LP-RX Input Hysteresis (VHYST)	Yes
Test 2.1.4	LP-RX Minimum Pulse Width Response (TMIN-RX)	Yes
Test 2.1.5	LP-RX Input Pulse Rejection (eSPIKE)	Yes
Test 2.2.1	LP-RX Initialization period (TINIT)	Yes
Test 2.2.2	ULPS Exit: LP-RX TWAKEUP Timer Value	Yes
Test 2.2.3	LP-RX Invalid/Aborted Escape Mode Entry	Yes
Test 2.2.4	LP-RX Invalid/Aborted Escape Mode Command	Yes
Test 2.2.5	LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits	Yes
Test 2.2.6	LP-RX Escape Mode Unsupported/Unassigned Commands	Yes
Test 2.3.1	HS-RX Amplitude Tolerance (VCPRX(DC), VIHHS, VILHS)	Yes
Test 2.3.2	HS-RX Differential Input High/Low Thresholds (VIDTH, VIDTL)	Yes
Test 2.3.3	HS-RX Jitter Tolerance	Yes
Test 2.4.1	HS-RX T3-TERM-EN Duration	Yes
Test 2.4.2	HS-RX T3-PREPARE Tolerance	Yes
Test 2.4.3	HS-RX T3-PREBEGIN Tolerance	Yes
Test 2.4.4	HS-RX T3-PROGSEQ Tolerance	Yes
Test 2.4.5	Test 2.4.5 HS-RX T3-POST Tolerance	Yes

Appendix B – Measurement Guidance

For measuring various parameters of the signal being calibrated/captured from the device, the oscilloscope needs to be set for an appropriate trigger setting. The following parameters would decide the selection of the trigger type

1) Signal Type: HS only signal or LP only signal or Burst waveform(LP_HS)
2) Waveform region of interest

For capturing a burst waveform, one of the trigger type that is suitable is ‘transition trigger’. For HS_only and LP_only waveforms, the default Edge trigger would serve the purpose.