Technical Reference

Tektronix

MIPI® D-PHY* Measurements & Setup Library
Methods of Implementation (MOI) for Verification, Debug, Characterization, Compliance and Interoperability Test

DPOJET Opt. D-PHY

077-0428-00

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TABLE OF CONTENTS

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MODIFICATION RECORD

Feb 08, 2008 (Version .01) Initial Document
Oct 12, 2008 (Version .02) HS, LP, and Clock measurements added.
Dec 12, 2008 (Version .03) Minor corrections to the text.
Mar 11, 2009 (Version .03) Minor corrections to the text.
Oct 16, 2009 (Version .04) Updated tests in HS and LP TX. Added tests in HS TX, LP TX and Data-Clock Timing.

ACKNOWLEDGMENTS

Tektronix, Inc. – Creation of this document
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INTRODUCTION

The tests contained in this document are organized in such an order as to simplify the identification of information related to a test, and to facilitate in the actual testing process. There is no implied order to execute these tests in this document.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test.

*: Other names and brands may be claimed as the property of others.

ELECTRICAL CHARACTERISTICS

Overview:

This selection of tests verifies various Electrical Characteristic requirements of D-PHY* products defined Section 8 of the D-PHY* Specification, version 0.9.

Group 1 (8.1.x) verifies the High-Speed Transmitter AC and DC Specifications, which are summarized in Tables 16 and 17 of Section 8.

Group 2 (8.2.x) verifies the Low Power Transmitter AC and DC Specifications, which are summarized in Tables 18 and 19 of Section 8.

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GROUP 1: HS TX ELECTRICAL TESTS

Overview:

This group of tests verifies the High Speed TX electrical requirements of the data lane as defined in the D-PHY* Standard.

*: Other names and brands may be claimed as the property of others.

Test 8.1.1 – Data Lane HS TX Static Common-Mode Voltage (V_{CMTX})

Purpose: To verify that the Static Common-Mode Voltages (V_{CMTX} High, and V_{CMTX} Low) of the DUT Data Lane HS transmitter are within the conformance limits.

References:

[1] D-PHY* Specification, Section 8.1.1, Line 1325
[2] Ibid, Section 8.1.1, Figure 39
[3] Ibid, Section 8.1.1, Table 16
[4] UNH* D-PHY* Conformance Test Suite, ver0.08, Test1.3.7

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [4]:
The common-mode voltage V_{CMTX} is defined as, *"the arithmetic mean value of the voltages at the Dp and Dn pins: $V_{CMTX} = (V_{DP}+V_{DN})/2$"* [1]. Because of various types of signal distortions that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is being driven. Because of this, V_{CMTX} must be measured separately for both the 0 and 1 states, at the "static" value corresponding to the settled voltage at the center of the UI (as opposed to the "dynamic" AC fluctuations that occur at the bit transitions, which are covered by a separate specification). The specification includes a figure showing various different types of signal distortions that can occur [2]. This figure is reproduced below, with the static common-mode distortion type highlighted in red.

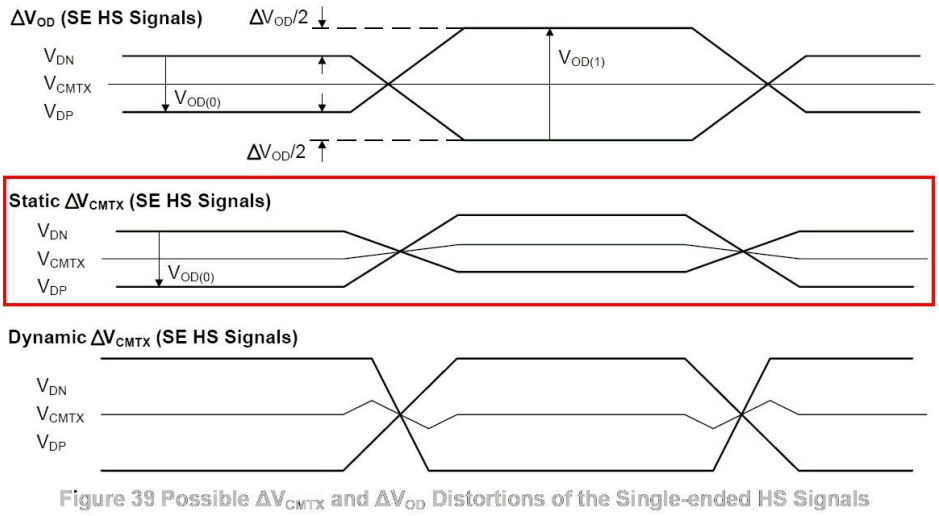


Figure 39 Possible ΔV_{CMTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

Figure: Static V_{CMTX} Distortion

In this test, a portion of the DUT's HS Data Lane signaling will be captured using a real-time DSO. The V_{DP} and V_{DN} single-ended waveforms will be averaged together (as described above) to create the V_{CMTX} common-mode waveform. The V_{CMTX} waveform will be sampled at the center of each UI, corresponding to each Differential-1 and Differential-0 state in the HS burst. The average common-mode voltage across all Differential-1 UIs will be computed as $V_{CMTX(1)}$, and the average common-mode voltage across all Differential-0 UIs will be computed as $V_{CMTX(0)}$. The values for both $V_{CMTX(1)}$ and $V_{CMTX(0)}$ must be between 150 to 250 mV in order to be considered conformant [3].

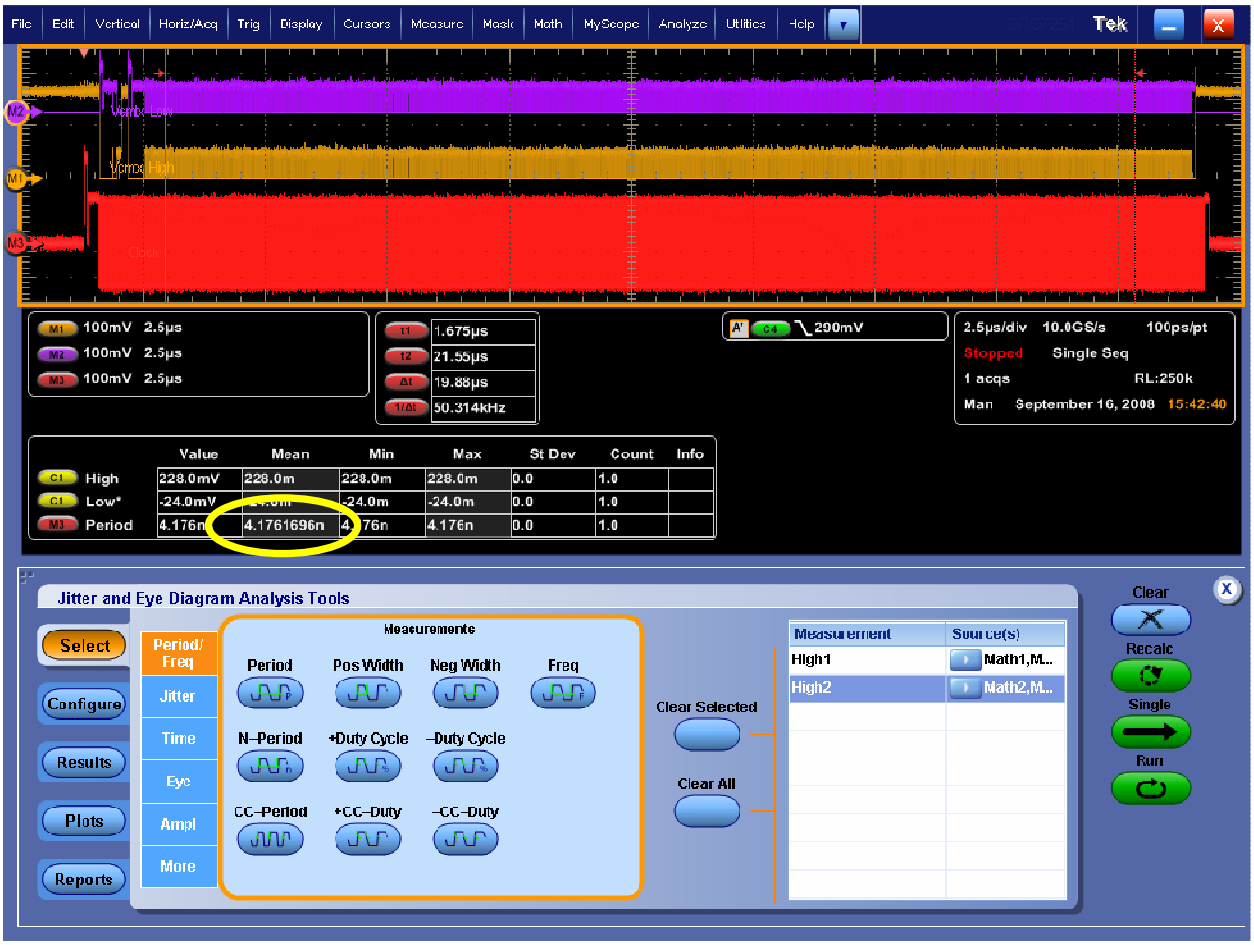
(Must add test cases to cover ZID requirements.)

Test Setup: See Appendix A and B.

*: Other names and brands may be claimed as the property of others.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix B)
2. Using DUT vendor-specific techniques, put the DUT into a state where it is transmitting a HS data burst.
3. Launch DPOJET using the main menu: Analyze/Jitter and Eye Analysis.
4. Recall setting file "D-PHY_Test_8_1_1.set.", using the main menu: File/Recall…/Setup

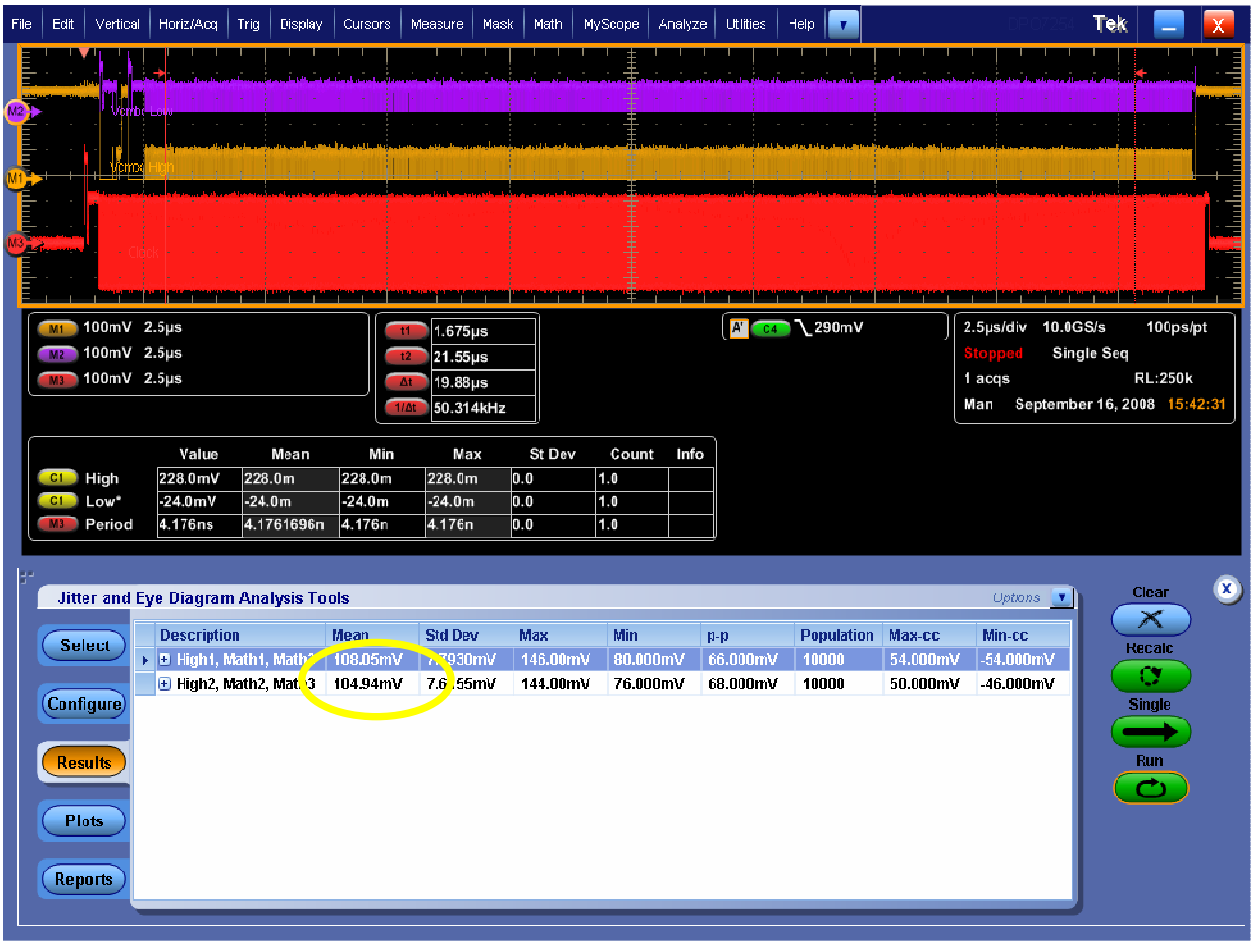


3. Click the "Configure" button in DPOJET. Click on "Clock Recovery". Click "Advanced". Enter a value that is approx. ¼ of value shown in M3 Mean display (enter a negative value).

*: Other names and brands may be claimed as the property of others.

5. Click “Results”, and click “Run”. This will make multiple acquisitions until 10,000 samples have been acquired.
6. Read the measured values for High1 (V_{cmtx} High) and High2 (V_{cmtx} Low) from the results table (mean value).
7. Compare against test limits of 150 mV and 250 mV.

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that V_{CMTX} is between 150 and 250 mV for both the Differential-1 and Differential-0 states.

*: Other names and brands may be claimed as the property of others.

Test 8.1.2 – Data Lane HS TX V_{CMTX} Mismatch ($\Delta V_{CMTX(1,0)}$)

Purpose: To verify that the Static Common-Mode Voltage Mismatch ($\Delta V_{CMTX(1,0)}$) of the DUT Data Lane HS transmitter is less than the maximum conformance limit.

References:

[1] D-PHY* Specification, Section 8.1.1, Line 1340
[2] Ibid, Section 8.1.1, Table 16
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test1.3.8

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion[4]:

The specification states, *"The static common-mode voltage mismatch between the Differential-1 and Differential-0 state is given by:* $\Delta V_{CMTX(1,0)} = (V_{CMTX(1)} - V_{CMTX(0)})/2$*"*[1].

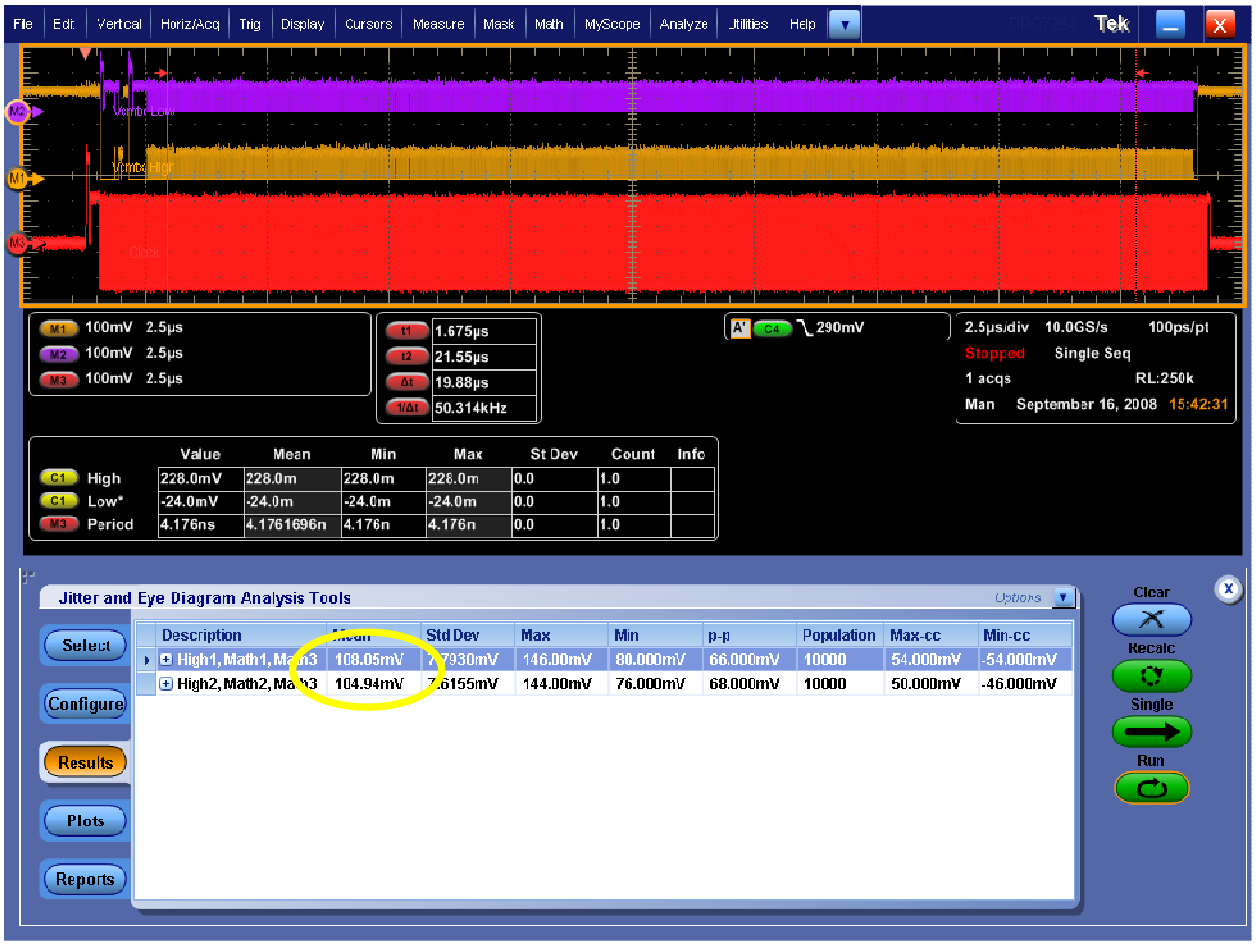
In this test, the numerical results from Test 8.1.1 for $V_{CMTX(1)}$ and $V_{CMTX(0)}$ will be used to compute the Data Lane HS-TX Static Common-Mode Voltage Mismatch, $\Delta V_{CMTX(1,0)}$. The result for $\Delta V_{CMTX(1,0)}$ will be taken as one-half of the difference of $V_{CMTX(1)}$ and $V_{CMTX(0)}$. The value for $\Delta V_{CMTX(1,0)}$ must be less than 5 mV in order to be considered conformant [2].

Test Setup: See Appendix A and B.

Test Procedure:

1. Perform setup for test 8.1.1 as previously described.

*: Other names and brands may be claimed as the property of others.



2. Read mean values for High1 and High2, as highlighted above.
3. Compute the mismatch by: $\Delta V_{CMTX(1,0)}$ = abs(High1-High2)/2.
4. Compare mismatch against observable results.

Observable Results:

- Verify that $\Delta V_{CMTX(1,0)}$ is less than 5 mV.

*: Other names and brands may be claimed as the property of others.

Test 8.1.3 – Data Lane HS TX Differential Voltage (V_{OD})

Purpose: To verify that the Differential Voltages ($V_{OD(0)}$ and $V_{OD(1)}$) of the DUT Data Lane HS transmitter are within the conformance limits.

References:

[1] D-PHY* Specification, Section 8.1.1, Line 1318
[2] Ibid, Section 8.1.1, Figure 38
[3] Ibid, Section 8.1.1, Table 16
[4] UNH* D-PHY* Conformance Test Suite, ver0.08, Test1.3.4

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion[4]:

The D-PHY Specification states, *"The differential output voltage V_{OD} is defined as the difference of the voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively. $V_{OD} = V_{DP} - V_{DN}$."* [1]. Note that this definition is potentially ambiguous in that, while it does define how the differential ***signal*** is computed, it does not specify how the differential ***voltage*** is measured for the purposes of conformance testing. (Note that a diagram is presented in [2], but this shows 'ideal' signaling, which is not an accurate representation for measurement purposes.) Given that there are multiple possible ways to implement a differential voltage measurement (peak-to-peak, mode-to-mode, average over entire UI, average over 40%-60% UI, etc), a common method must be chosen for consistency. A simple averaged method is defined here, using the averaged HS-1 and HS-0 voltage levels at the center of each Unit Interval.

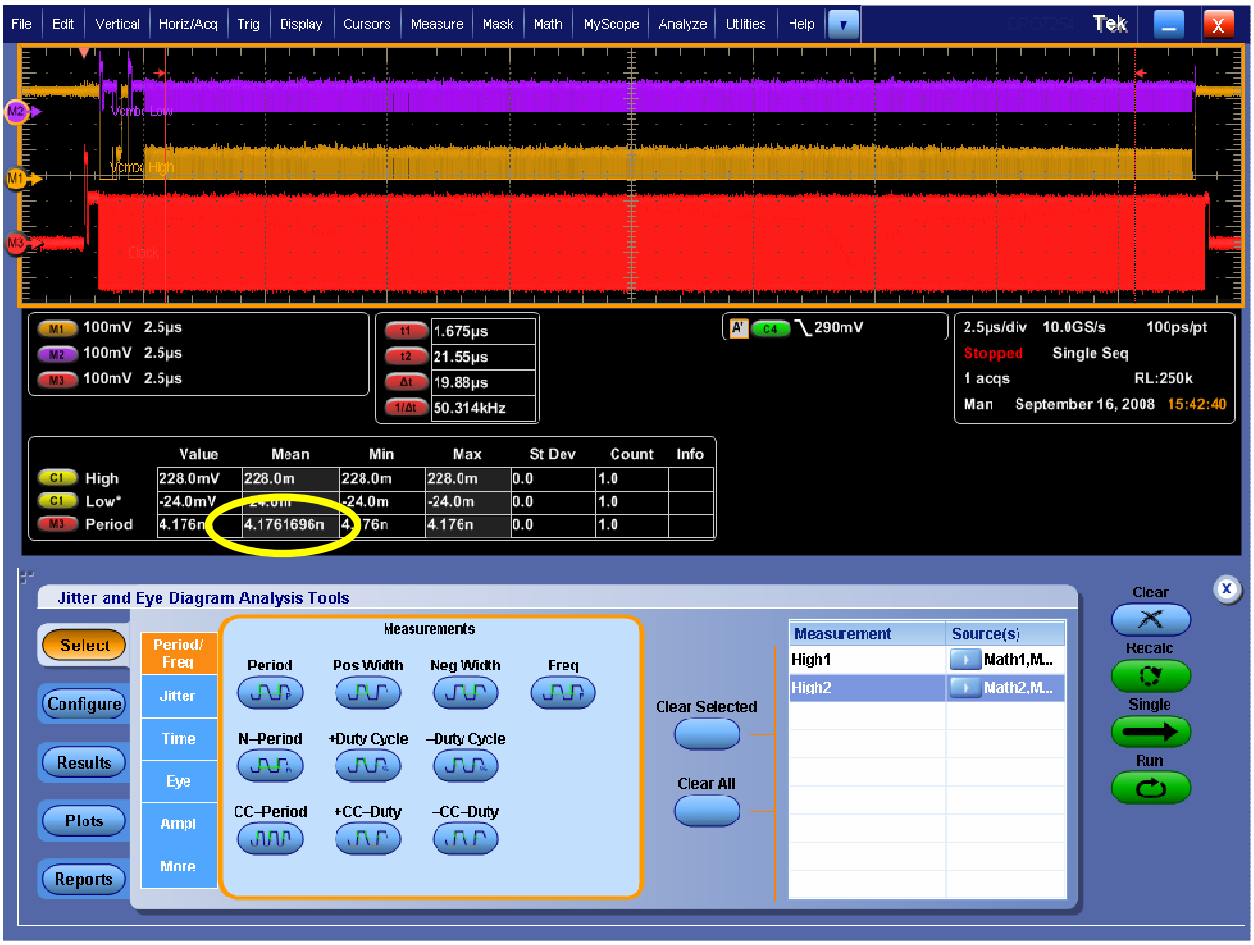
In this test, a sample of the DUT's HS Data Lane signaling will be captured using a real-time DSO. The differential waveform V_{OD} will be computed as difference of the positive and negative single-ended waveforms (V_{DP}-V_{DN}). The differential waveform V_{OD} will then be sampled at the center of each Unit Interval in order to determine the $V_{OD(0)}$ and $V_{OD(1)}$ values, which will each be averaged over all of the bits in an entire HS burst to produce the averaged $V_{OD(0)}$ and $V_{OD(1)}$ values. The averaged $V_{OD(1)}$ value must be within the range of 140 to 270 mV in order to be considered conformant [3]. The averaged $V_{OD(0)}$ value must be within the range of -140 to -270 mV in order to be considered conformant [3]. (Note that this equates to a differential peak-to-peak voltage value of 280 to 540mVppd.)

(Must add test cases to cover ZID requirements.)

Test Setup: See Appendix A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix B)
2. Configure the Test System to emulate the DUT link partner (Master or Slave).
3. Launch DPOJET using the main menu: Analyze/Jitter and Eye Analysis.
4. Recall setting file "D-PHY_Test_8_1_3.set." using the main menu: File/Recall…/Setup.

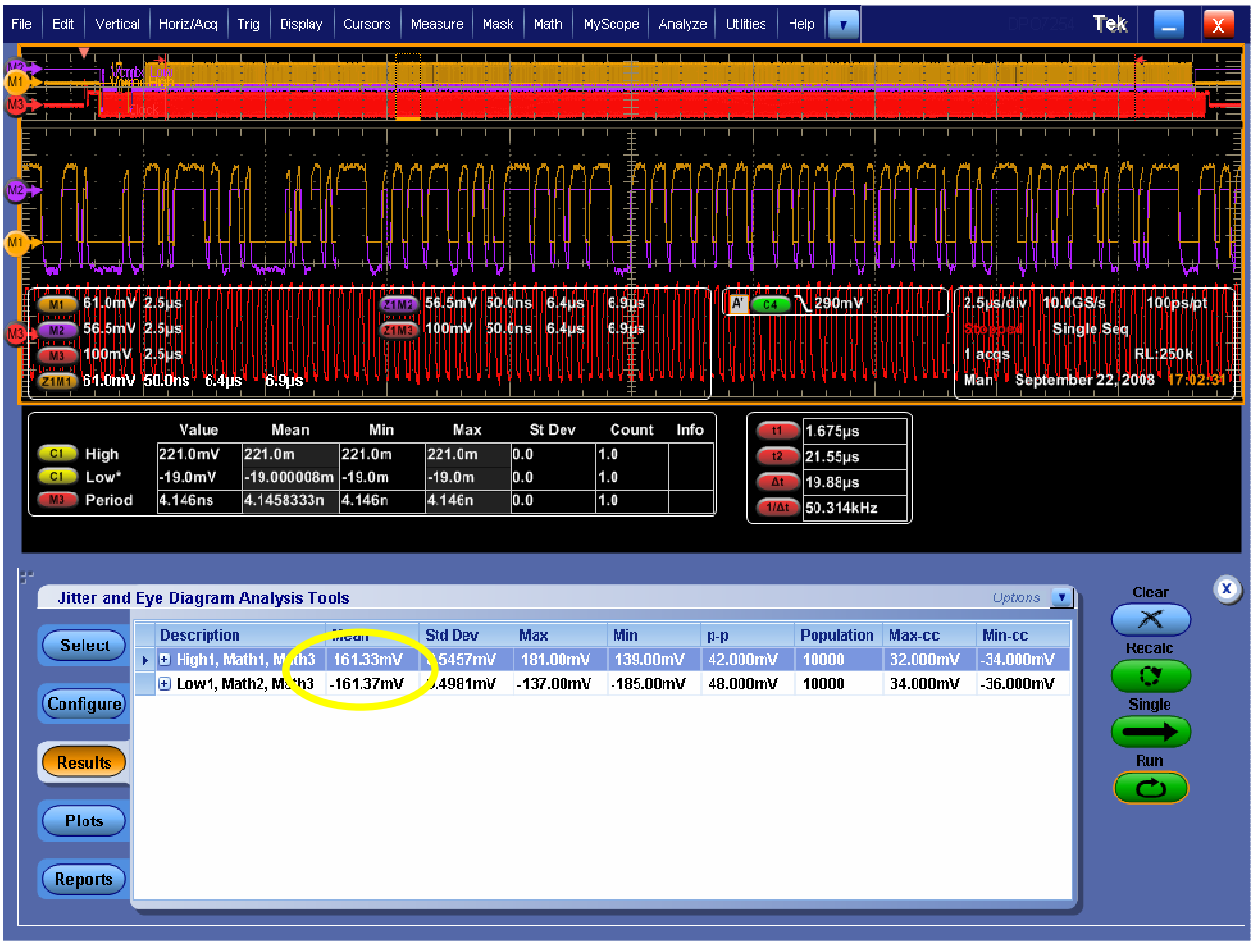


3. Click the “Configure” button in DPOJET. Click “Clock Recovery”. Click “Advanced”. Enter in a value that is approx. ¼ of value shown in M3 Mean display (enter a negative value).

*: Other names and brands may be claimed as the property of others.

5. Click “Results”, and click “Run”. This will make multiple acquisitions until 10,000 acquisitions have been acquired.
6. Read the measured values for High1 (V_{OD} High) and High2 (V_{OD} Low) from the results table (mean value).
7. Compare against test limits of 140 mV and 270 mV.

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that V_{OD} High is between 140 and 270 mV (i.e. 280 to 540mV_{ppd})
- Verify that V_{OD} Low is between -140 and -270 mV (i.e. -280 to -540mV_{ppd})

*: Other names and brands may be claimed as the property of others.

Test 8.1.4 – Data Lane HS TX Differential Voltage Mismatch (ΔV_{OD})

Purpose: To verify that the Differential Voltage Mismatch (ΔV_{OD}) of the DUT Data Lane HS transmitter is within the conformance limits.

References:

[1] D-PHY* Specification, Section 8.1.1, Line 1330
[2] Ibid, Section 8.1.1, Table 16
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test1.3.5

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion[3]:

The D-PHY Specification states, *"The output differential voltage mismatch ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$. This is expressed by $\Delta V_{OD} = | V_{OD(1)}| - | V_{OD(0)}|$"* [1].

In this test, the numerical $V_{OD(0)}$ and $V_{OD(1)}$ results obtained in the previous test (see Test 8.1.3) is used to compute the ΔV_{OD} result. The difference of the absolute values of these two values will be taken to produce ΔV_{OD}. The absolute value of ΔV_{OD} must be less than 10 mV to be considered conformant [2].

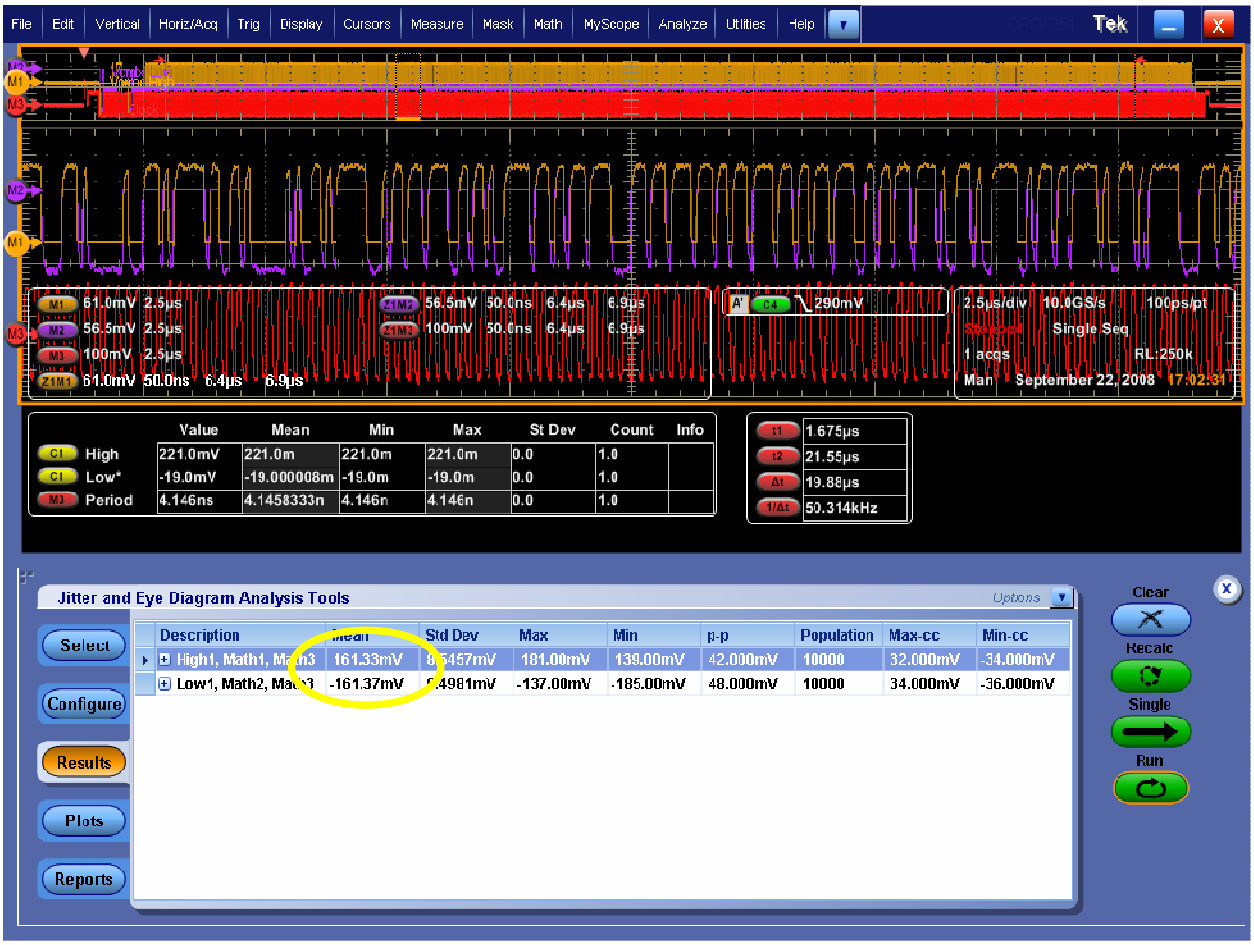
(Must add test cases to cover ZID requirements.)

Test Setup: See Appendix A.

Test Procedure:

1. Perform test 8.1.3 as previously described.
2. Launch DPOJET using the main menu: Analyze/Jitter and Eye Analysis.
3. Recall setting file "D-PHY_Test_8_1_3.set." using the main menu: File/Recall…/Setup

*: Other names and brands may be claimed as the property of others.



4. Read mean values for High1 and High2 as highlighted above.
5. Compute the mismatch by: ΔV_{OD} = abs(High1)-abs(High2).
6. Compare mismatch against observable results.

Observable Results:

- Verify that the absolute value of ΔV_{OD} is less than 10 mV.

*: Other names and brands may be claimed as the property of others.

Test 8.1.5 – Data Lane HS TX Single-Ended Output High Voltage (V_{OHHS})

Purpose: To verify that the Single-Ended Output High Voltages ($V_{OHHS(DP)}$ and $V_{OHHS(DN)}$) of the DUT Data Lane HS transmitter are less than the maximum conformance limit.

References:

[1] D-PHY* Specification, Section 8.1.1, Line 1321
[2] Ibid, Section 8.1.1, Table 16
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test1.3.6

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion[3]:

The D-PHY Specification states, *"The output voltages V_{DP} and V_{DN} at the Dp and Dn pins shall not exceed the High-Speed output high voltage V_{OHHS}. V_{OLHS} is the High-Speed output, low voltage on Dp and Dn and is determined by V_{OD} and V_{CMTX}. The High-Speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value of V_{OHHS}."* [1].

In this test, a sample of the DUT's HS Data Lane signaling will be captured using a real-time DSO. The V_{DP} and V_{DN} single-ended waveforms will be captured using separate channels of the DSO, and processed independently. The maximum instantaneous voltages for both the V_{DP} and V_{DN} signals measured across the entire HS burst (between the end of $T_{HS-ZERO}$ and the start of $T_{HS-TRAIL}$) will be recorded as V_{OHHS}. (Note that these will be denoted as $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ for this test, though they are not explicitly defined this way in the specification.) The V_{OHHS} results for both V_{DP} and V_{DN} shall be less than 360mV in order to be considered conformant [2].

Note:
- TX Vdiff range is 140-270 mV (280 to 540mV$_{ppd}$)
- TX Vcm range is 150-250 mV
- TX max SE voltage (V_{OHHS}) is 360mV

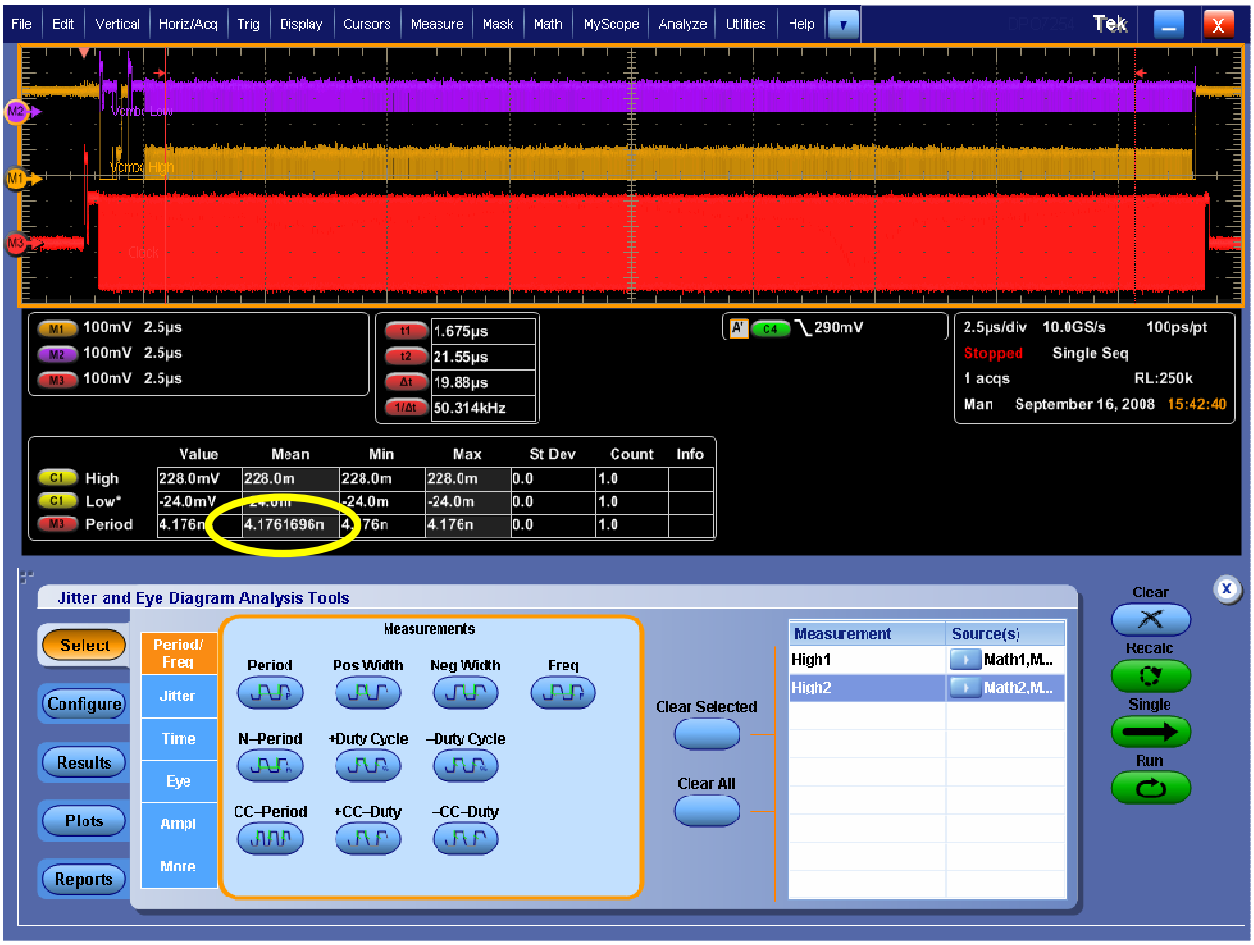
If you run at maximum allowed TX common-mode level and max differential output, your single-ended upper voltage will be 250+135 = 385mV. Therefore, if you want to run at the maximum allowed TX single-ended rail of 360mV, you need to decrease either common-mode or diff output.

(Must add test cases to cover ZID requirements.)

Test Setup: See Appendix A and B.

Test Procedure:

1. Launch DPOJET using the main menu: Analyze/Jitter and Eye Analysis.
2. Recall setting file "D-PHY_Test_8_1_5.set." using the main menu: File/Recall…/Setup

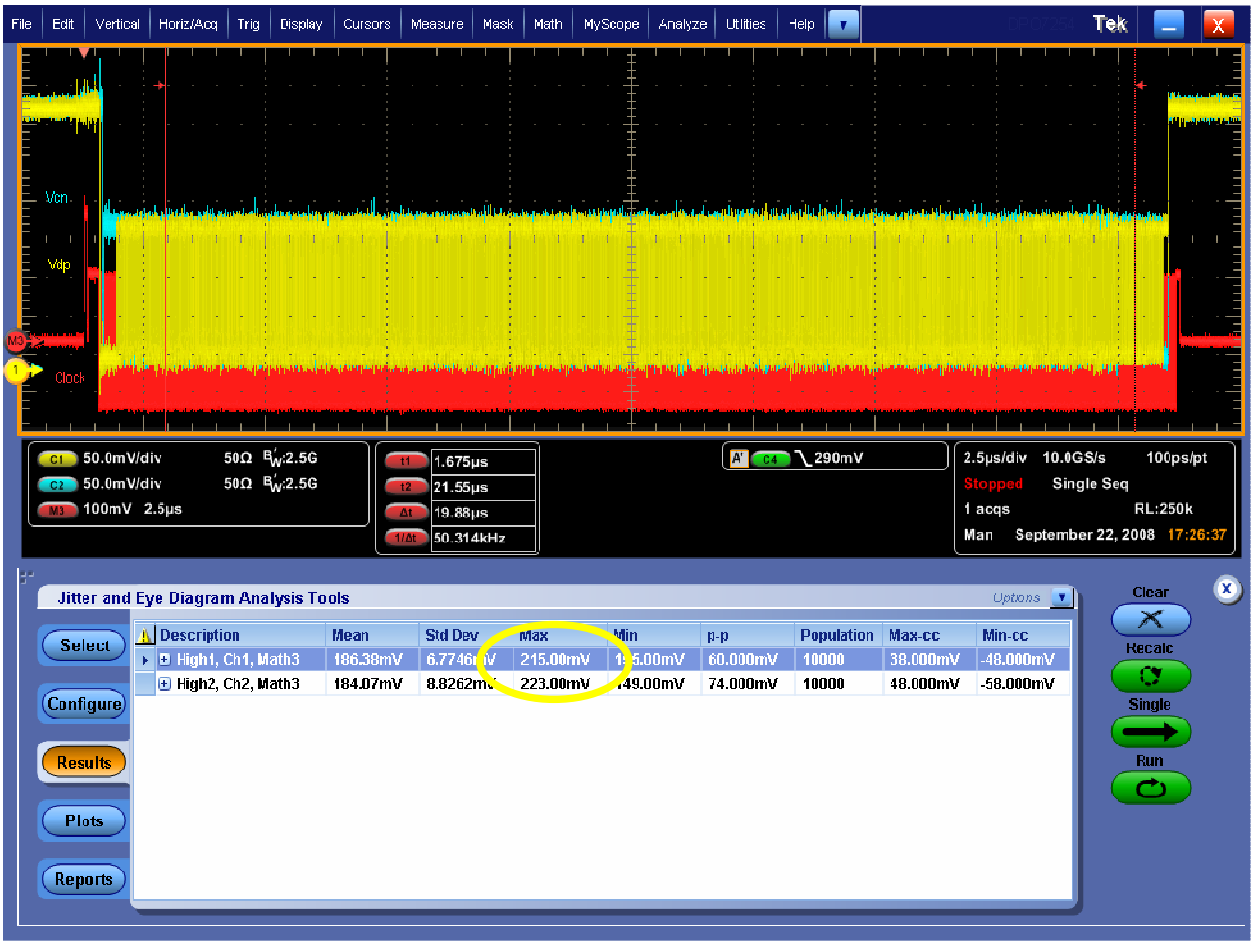


3. Click the “Configure” button in DPOJET. Click “Clock Recovery”. Click “Advanced”. Enter a value that is approx. ¼ of value shown in M3 Mean display (enter a negative value).

*: Other names and brands may be claimed as the property of others.

3. Click “Results”, and click “Run”. This will make multiple acquisitions until 10,000 samples have been acquired.
4. Read the measured values for High1 ($V_{OHHS(DP)}$) and High2 ($V_{OHHS(DN)}$) from the results table (Max value).
5. Compare against test limits of 360 mV.

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that V_{OHHS} is less than 360 mV for both the Dp and Dn signals.

*: Other names and brands may be claimed as the property of others.

Test 8.1.6 – Data Lane HS Entry: Data Lane T_{LPX} Value

Purpose: To verify that the HS AC Common-Mode Signal Level Variations above 450 MHz ($V_{CMTX(HF)}$) of the DUT transmitter are below the maximum allowable limit.

References:

[1] D-PHY* Specification, Section 5.2, Line 746
[2] Ibid, Section 5.9, Table 14
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.3.1

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion[3]:
The D-PHY Low-Power (LP) mode of operation is comprised of state transitions occurring at some implementation-specific rate less than 20M transitions/sec. Note that these state transitions may have different meanings depending on the context (Control, Escape, or LPDT mode), and do not equate to 'bits' on the wire. The D-PHY Specification specifies that, *"All LP state periods shall be at least T_{LPX} in duration."* [1], and defines the minimum value of T_{LPX} to be 50ns [2].

In this test, the focus is specifically the duration of the last LP-01 state that occurs immediately before an HS burst sequence. The state will be measured starting at the time where the V_{DP} falling edge crosses the maximum low-level LP threshold, $V_{IL,MAX}$ (550mV), and ending at the time where the V_{DN} falling edge crosses the same $V_{IL,MAX}$ threshold. A picture of the T_{LPX} interval is shown in the figure below.

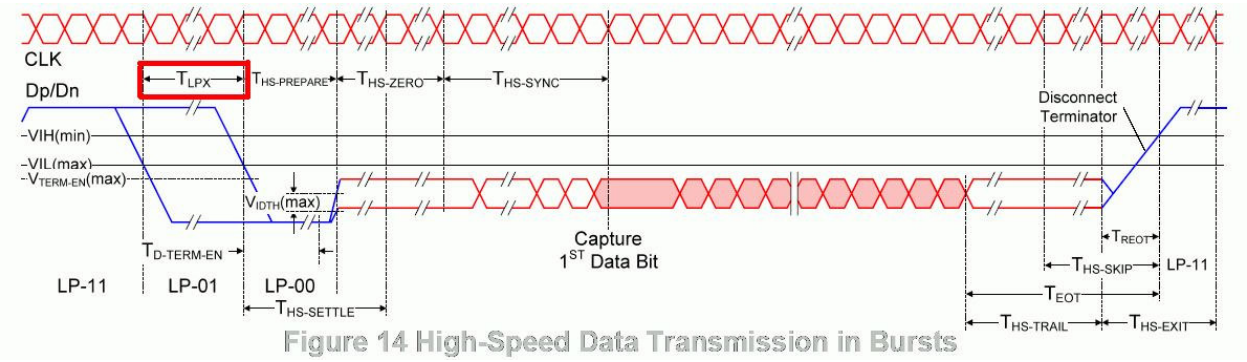


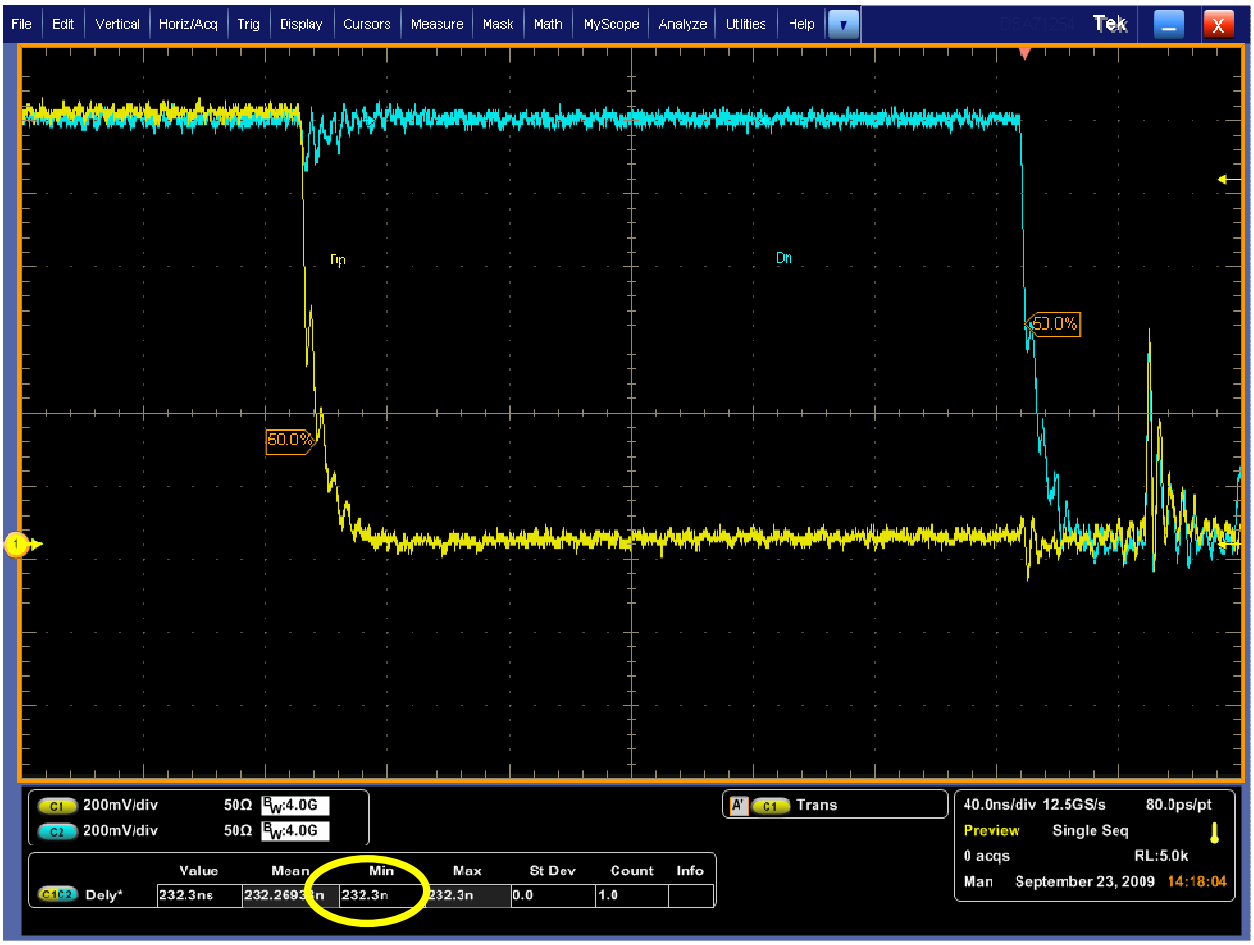
Figure 14 High-Speed Data Transmission in Bursts

Test Setup: See Appendix A and B.

Test Procedure:

1. Recall setting file "D-PHY_Test_8_1_6.set." using the main menu: File/Recall…/Setup
2. Press the Multiview Zoom button and then press Single on the oscilloscope.
3. Verify if the zoom is correctly located as per the diagram shown above.
4. Note the minimum value of Delay between Ch1 and Ch2 at the bottom of the screen.
5. The value should be greater than 50 ns to meet the required specification.

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that T_{LPX} value is greater than 50 ns.

*: Other names and brands may be claimed as the property of others.

Test 8.1.7 – Data Lane HS Entry: $T_{HS\text{-}PREPARE}$ Value

Purpose: To verify that the duration of the final LP-00 state immediately before HS transmission ($T_{HS\text{-}PREPARE}$) is within the conformance limits.

References:

[1] D-PHY* Specification, Section 5.14.2, Line 1027
[2] Ibid, Section 5.9, Table 14
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.3.2

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

As part of the process for switching the Data Lane into HS mode, the D-PHY Specification provides a specification for the minimum time interval that a device must transmit the final LP-00 state before enabling HS mode (which occurs at the start of the $T_{HS\text{-}ZERO}$ interval). This interval is defined as $T_{HS\text{-}PREPARE}$, and is shown in the figure below.

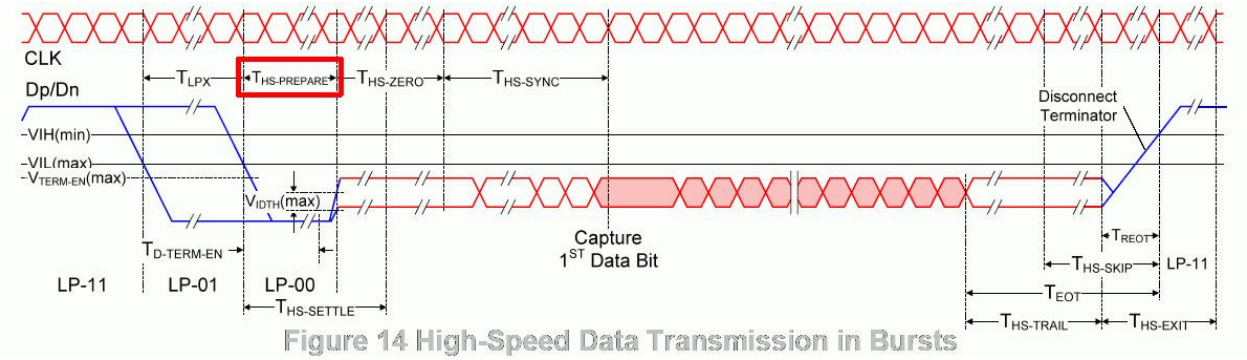


Figure: $T_{HS\text{-}PREPARE}$ Interval

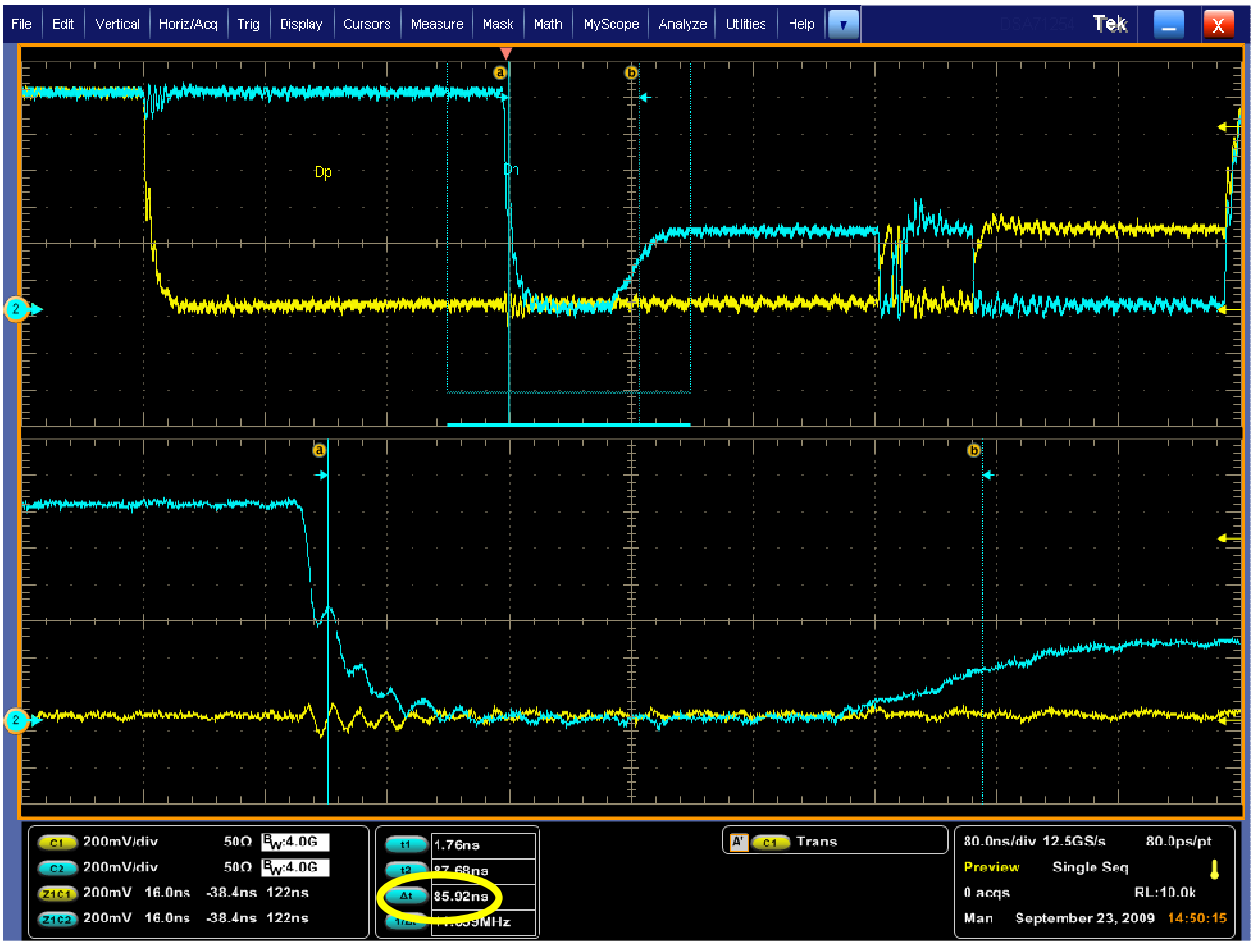
In this test, the DUT will be configured to source an HS burst sequence, starting and ending with LP-11 states. The $T_{HS\text{-}PREPARE}$ interval begins at the time where the Data Lane V_{DN} signal crosses below $V_{IL,MAX}$ (550mV), and ends at the beginning of the extended $T_{HS\text{-}ZERO}$ HS differential state, at the point where the V_{OD} differential voltage crosses above the minimum valid HS-RX differential threshold level (+/-70mV). The measured duration of $T_{HS\text{-}PREPARE}$ should be between (40ns + 4*UI) and (85ns + 6*UI) (where UI is the nominal HS Unit Interval for the DUT) in order to be considered conformant.

Test Setup: See Appendix A and B.

Test Procedure:

1. Recall setting file "D-PHY_Test_8_1_7.set." using the main menu: File/Recall…/Setup
2. Ensure the cursors are marked at the location as per the diagram above.
3. Note the value of Δt as $T_{HS\text{-}PREPARE}$
4. Calculate the limits (40ns + 4*UI) and (85ns + 6*UI). Confirm that $T_{HS\text{-}PREPARE}$ lies between these limits.

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that $T_{HS\text{-}PREPARE}$ is within the limits of (40 ns + 4*UI) and (85 ns + 6*UI).

*: Other names and brands may be claimed as the property of others.

Test 8.1.8 – Data Lane HS TX Common-Level Variations Above 450 MHz ($V_{CMTX(HF)}$)

Purpose: To verify that the AC Common-Mode Signal Level Variations above 450 MHz ($V_{CMTX(HF)}$) of the DUT Data Lane HS transmitter are below the maximum allowable limit.

References:

[1] D-PHY* Specification, Section 8.1.1, Line 1342
[2] Ibid, Section 8.1.1, Table 17
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.3.10

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion[3]:

Note that the procedure for this test is essentially identical to the previous $V_{CMTX(LF)}$ test, except that a highpass test filter is used rather than a bandpass filter, and the result is measured as V_{RMS} rather than V_{PEAK}. The test filter for this test is an 8^{th}-order Butterworth highpass filter, with a cutoff frequency of 450MHz. $V_{CMTX(HF)}$ is measured as the RMS value of the highpass-filtered V_{CMTX} waveform.

The value of $V_{CMTX(HF)}$ must be less than $15mV_{RMS}$ in order to be considered conformant [2].

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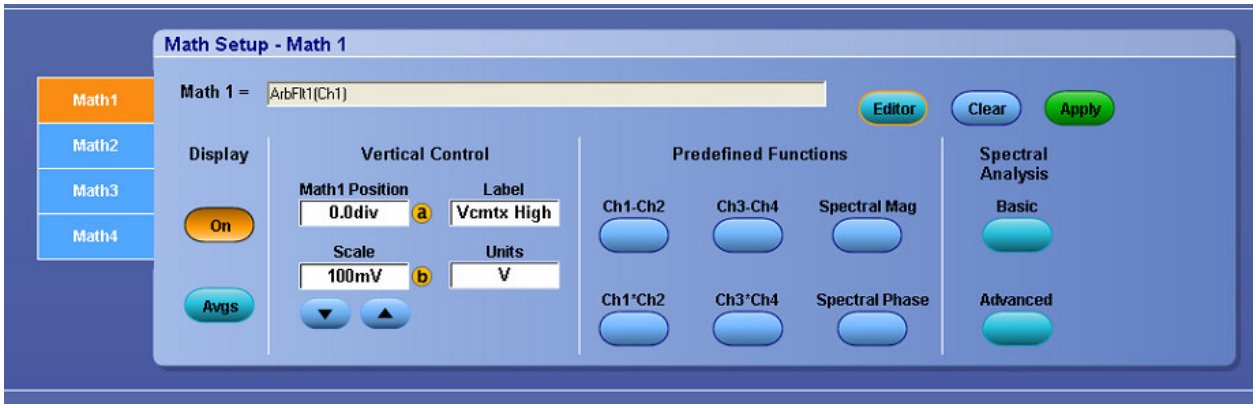
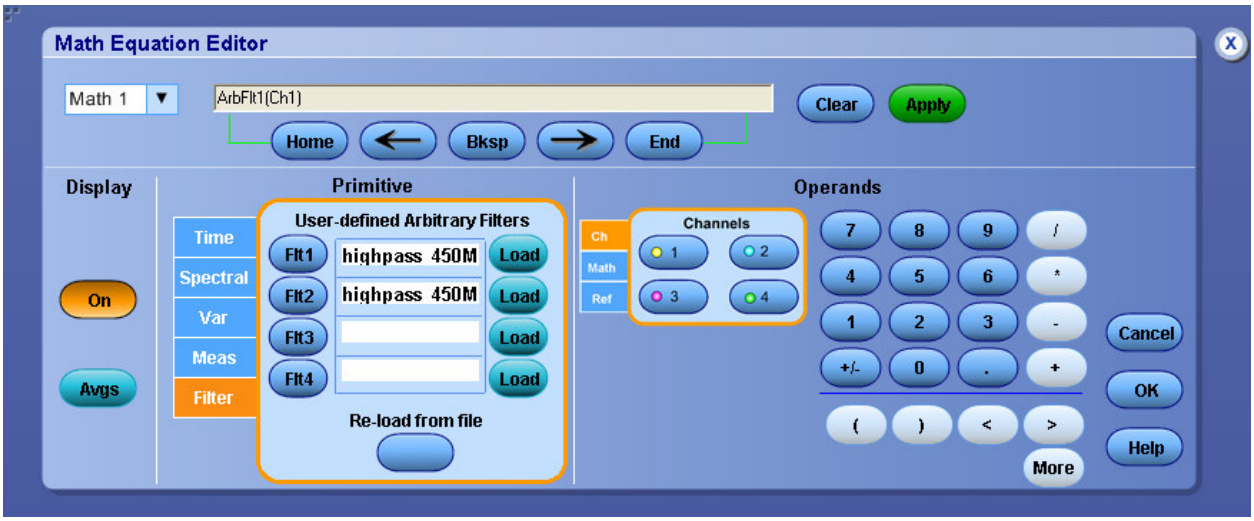
Test Setup: See Appendix A and B.

Test Procedure:

1. Launch DPOJET using the main menu: Analyze/Jitter and Eye Analysis.
2. Recall setting file "D-PHY_Test_8_1_8.set." using the main menu: File/Recall…/Setup
3. Ensure that the correct filter file is chosen based on your acquisition settings. To confirm or change the filter file, go to Math > Math Setup > Math1> Editor > Filter > Load (See figure below). Apply the same to Math 2.



*: Other names and brands may be claimed as the property of others.



4. Read $V_{CMTX(HF)}$ value as the mean value of measurement 3 as shown in the screen capture above.
5. Compare measured value to the observable limits.

Observable Results:

- Verify that $V_{CMTX(HF)}$ is less than 15 mV_{RMS}.

*: Other names and brands may be claimed as the property of others.

Test 8.1.9 – Data Lane HS TX Common-Level Variations Between 50-450 MHz ($V_{CMTX(LF)}$)

Purpose: To verify that the AC Common-Mode Signal Level Variations between 50 and 450 MHz ($V_{CMTX(LF)}$) of the DUT Data Lane HS transmitter are below the maximum allowable limit.

References:

[1] D-PHY* Specification, Section 8.1.1, Line 1342
[2] Ibid, Section 8.1.1, Figure 39
[3] Ibid, Section 8.1.1, Table 17
[4] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.3.9

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [4]:

The specification defines several requirements regarding a device's common-mode signaling. These specifications each measure slightly different distortions of the common-mode signal, which can result from very specific and distinct types of waveform asymmetry. "Dynamic" (or AC) variations are typically caused by an asymmetry in the rise/fall times of the single-ended HS signals. The specification states, *"The transmitter shall send data such that the high frequency and low frequency common-mode voltage variations do not exceed $\Delta V_{CMTX(HF)}$ and $\Delta V_{CMTX(LF)}$, respectively."* [1].

The specification includes a figure showing various different types of signal distortions that can occur [2]. This figure is reproduced below, with the dynamic common-mode distortion type highlighted in red.

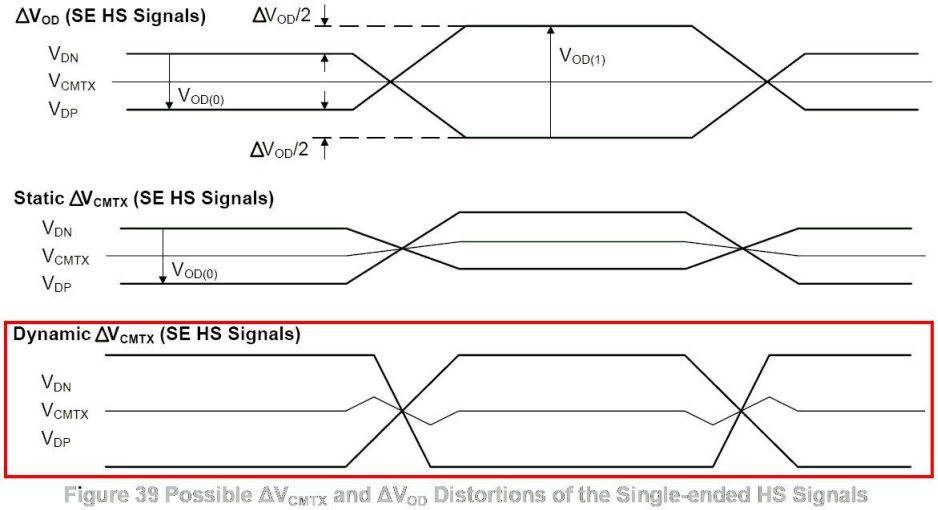


Figure 39 Possible ΔV_{CMTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

Figure: Dynamic V_{CMTX} Distortion

In this test, the V_{CMTX} common-mode signal will be captured using a real-time DSO, in the same manner as was used for the HS-TX Static Common-Mode Voltages measurement. However for this test, rather than measuring the average 1/0 DC levels, the AC voltage will be measured, specifically for the frequency range between 50 and 450MHz.

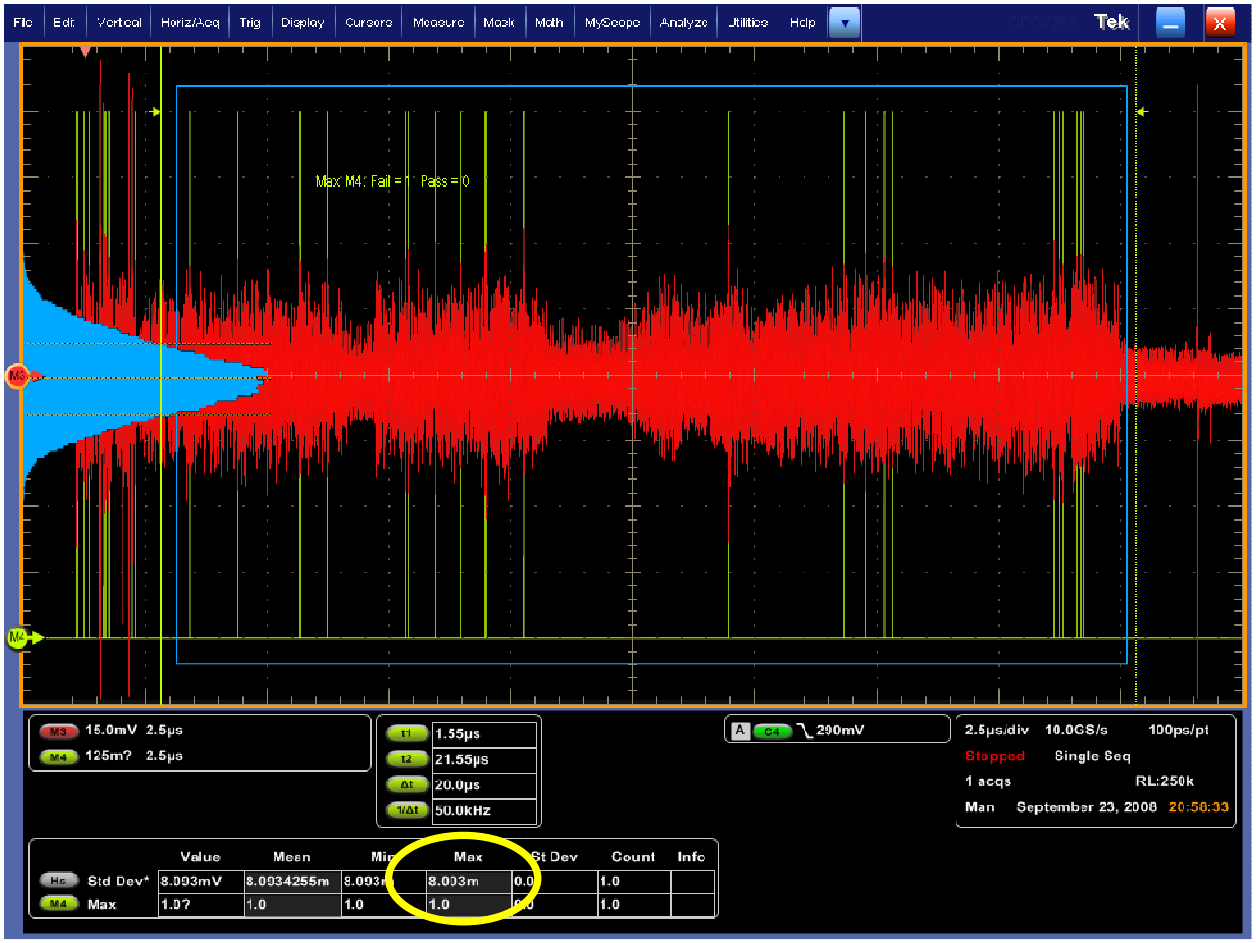
The value of $V_{CMTX(LF)}$ must be less than 25 mV_{PEAK} in order to be considered conformant [3].

Test Setup: See Appendix A and B.

*: Other names and brands may be claimed as the property of others.

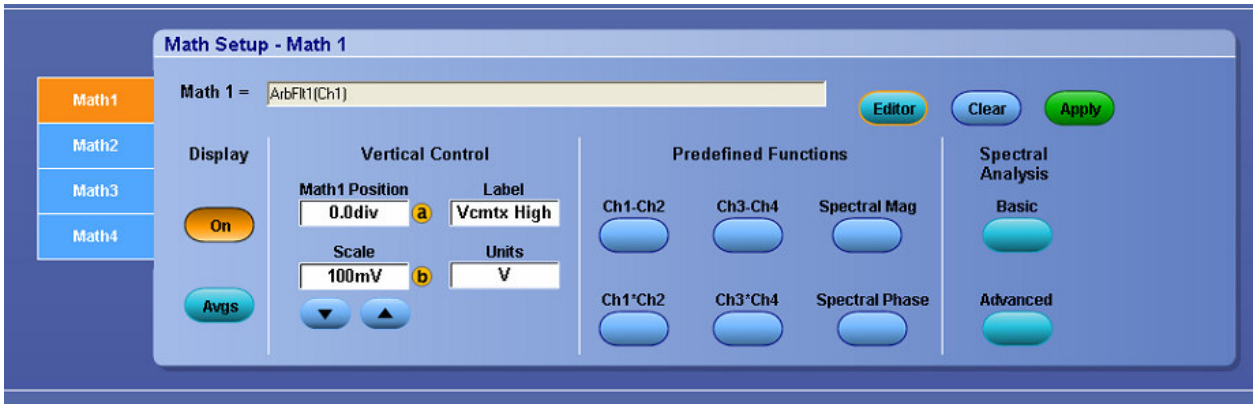
Test Procedure:

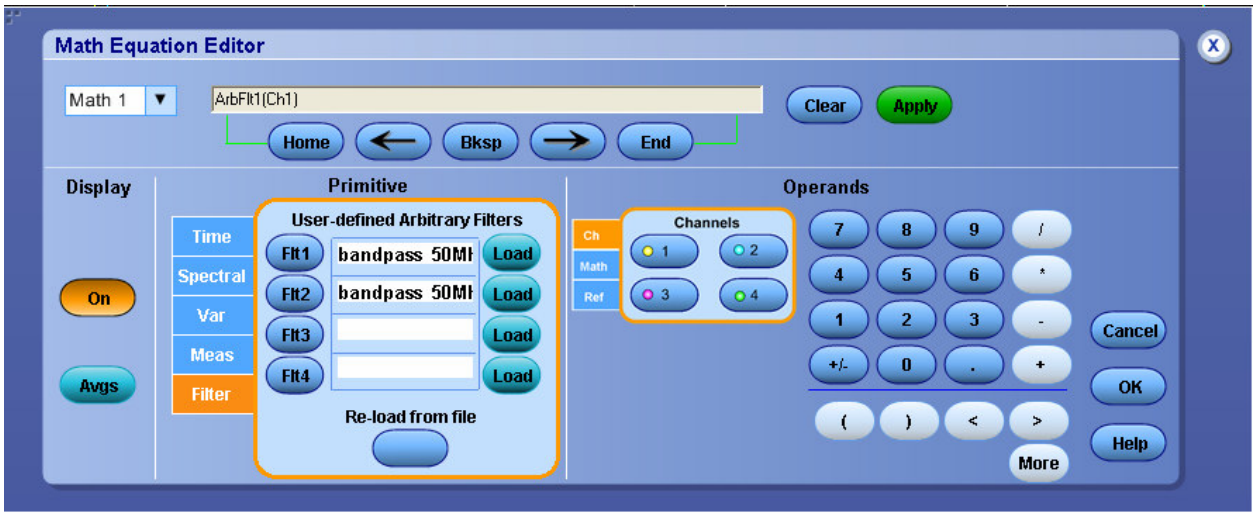
1. Connect the DUT to the Test System (See Appendix A)
2. Create a condition that causes an HS Data Transmission Burst to be sourced from the DUT, and capture the exchange using the DSO.
3. Launch DPOJET using the main menu: Analyze/Jitter and Eye Analysis.
4. Recall setting file "D-PHY_Test_8_1_9.set." using the main menu: File/Recall…/Setup.



5. This test detects whether $V_{CMTX(LF)}$ exceeds the limits specified in the observable results.
6. Ensure that the correct filter file is chosen based on your acquisition settings. To confirm or change the filter file, go to Math > Math Setup > Math1 > Editor > Filter > Load (See pictures below). Apply the same to Math 2.

*: Other names and brands may be claimed as the property of others.





7. The value of this measurement will be 0 if the Math4 waveform is always below 25 mV for the interval between the vertical cursors. This condition represents a pass.
8. The measurement will have a value of 1 if the waveform goes greater than or equal to 25 mV at one or more points. This condition indicates a failure.

Observable Results:

- Verify that $V_{CMTX(LF)}$ is less than 25 mV_{PEAK}.

*: Other names and brands may be claimed as the property of others.

Test 8.1.10 – Data Lane HS TX 20%-80% Rise Time (t_R)

Purpose: To verify that the 20%-80% Rise Time (t_R) of the DUT Data Lane HS transmitter is within the conformance limits.

References:

[1] D-PHY* Specification, Section 8.1.1, Line 1361
[2] Ibid, Section 8.1.1, Table 17
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.3.11

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

The D-PHY Specification states, *"The rise and fall times, t_R and t_F, are defined as the transition time between 20% and 80% of the full HS signal swing. The driver shall meet the t_R and t_F specifications for all allowable Z_{ID}."* [1].

In this test, a sample of the DUTs HS Data Lane signaling will be captured using a real-time DSO. The differential waveform V_{OD} will be computed as difference of the positive and negative single-ended waveforms (V_{DP}-V_{DN}). The average 20%-80% Rise Time (t_R) across all HS transitions will be measured relative to the average $V_{OD(0)}$ and $V_{OD(1)}$ amplitude values determined previously, to produce the final t_R result.

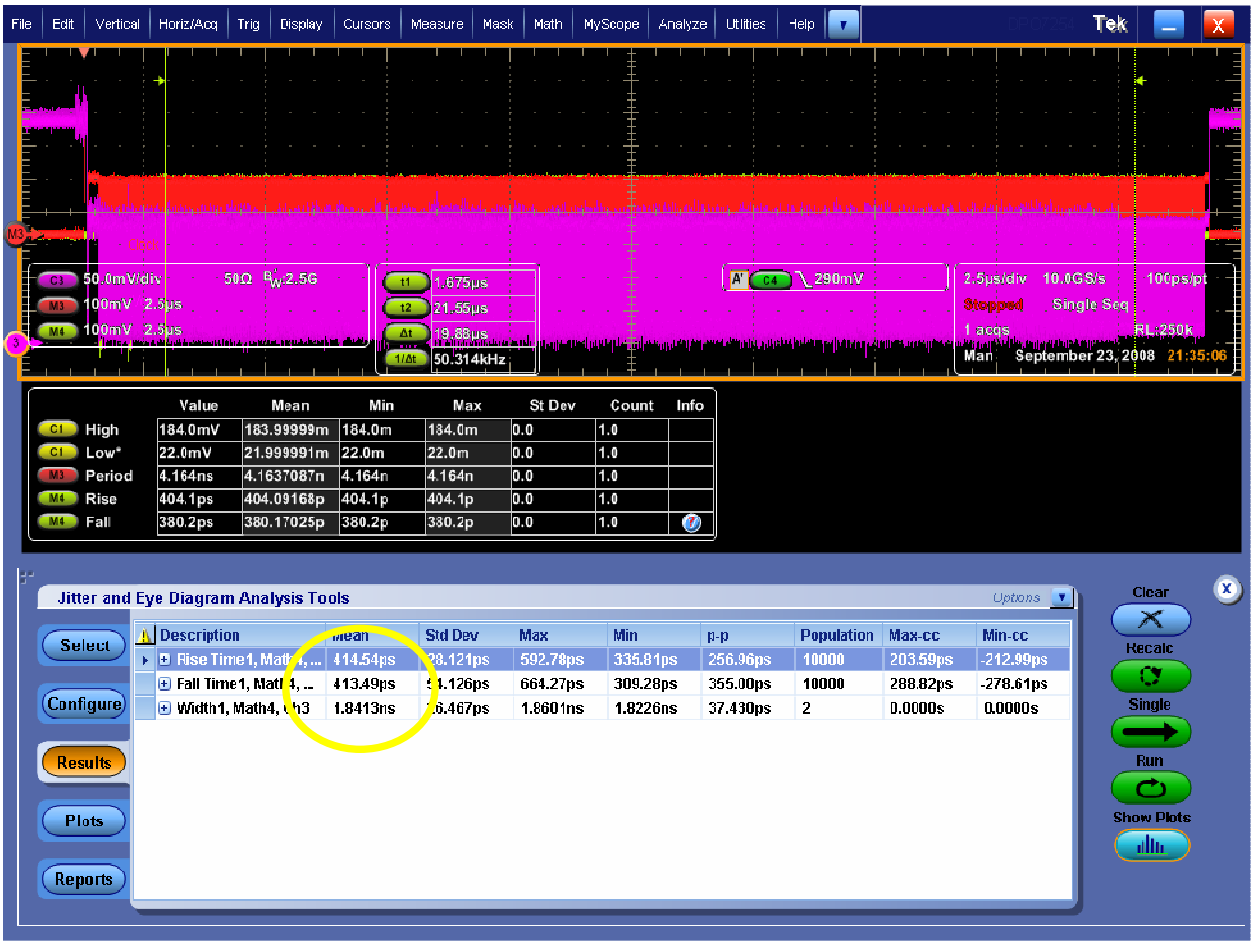
The value of t_R must be greater than 150ps and less than 0.3 UI (where UI is the nominal HS Unit Interval for the DUT) to be considered conformant [2].

Test Setup: See Appendix A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix A)
2. Configure the Test System to emulate the DUT link partner (Master or Slave).
3. Create a condition that causes an HS Data Transmission Burst to be sourced from the DUT, and capture the exchange using the DSO.
4. From the oscilloscope main menu, select Analyze>Jitter and Eye Analysis>Select
5. Recall the setup file "D-PHY_Test_8_1_10.set".
6. Ensure explicit clock edge is set correctly by going to Configure > Clock Recovery > Advanced. (How to set this has been shown in the earlier tests).
7. Click "Run" to compute the rise and fall times on 10K or more edges. Go to Results tab to view the measured results for rise and fall time.
8. Compare measured results against the limits in the observable results.

*: Other names and brands may be claimed as the property of others.



In this example, UI is measured with the width measurement, showing 1.84 ns. The upper limit is calculated at .3*1.84 ns=552 ps, and the lower limit is 150 ps So this device passes the test.

Observable Results:

- Verify that t_R is greater than 150ps and less than 0.3UI.
- The UI width can be read from the mean value of the width displayed in the table. Use this value to calculate .3*UI and verify that the measured rise and fall times are less than the calculated value.

*: Other names and brands may be claimed as the property of others.

Test 8.1.11 – Data Lane HS TX 20%-80% Fall Time (t_F)

Purpose: To verify that the 80%-20% Fall Time (t_F) of the DUT Data Lane HS transmitter is within the conformance limits.

References:

[1] D-PHY* Standard, Section 8.1.1, Line 1361
[2] Ibid, Section 8.1, Table 17
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.3.12

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

The D-PHY Specification states, *"The rise and fall times, t_R and t_F, are defined as the transition time between 20% and 80% of the full HS signal swing. The driver shall meet the t_R and t_F specifications for all allowable Z_{ID}."* [1].

Note the procedure for this test is identical to the previous test (see Test 1.3.11), except that the average 80%-20% Fall Time (t_F) is measured.

The value of t_F must be greater than 150ps and less than 0.3 UI (where UI is the nominal HS Unit Interval for the DUT, see Test 1.4.16) in order to be considered conformant [2].

(Must add test cases to cover ZID requirements.)

Test Setup: See Appendix A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix A)
2. Configure the Test System to emulate the DUT link partner (Master or Slave).
3. Create a condition that causes an HS Data Transmission Burst to be sourced from the DUT, and capture the exchange using the DSO.
4. Measure t_F as described above.

Observable Results:

- Read the value for t_F from the data gathered from 8.1.10, and verify that the value is greater than 150ps and less than 0.3UI.

*: Other names and brands may be claimed as the property of others.

Test 8.1.12 – Data Lane HS Entry: $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ Value

Purpose: To verify that the combined time of $T_{HS\text{-}PREPARE}$ plus the time the DUT Data Lane transmitter drives the HS-0 differential state prior to transmitting the HS Sync sequence ($T_{HS\text{-}ZERO}$) is greater than the minimum required duration.

References:

[1] D-PHY* Standard, Section 5.14.2, Line 1028
[2] Ibid, Section 5.9, Table 14
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.3.3

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

As part of the process for switching the Data Lane into HS mode, the D-PHY Specification provides a specification for the minimum duration that a device must drive the extended Data HS-0 differential state prior to starting HS differential data transmission. This interval is defined as $T_{HS\text{-}ZERO}$, and is shown in the figure below.

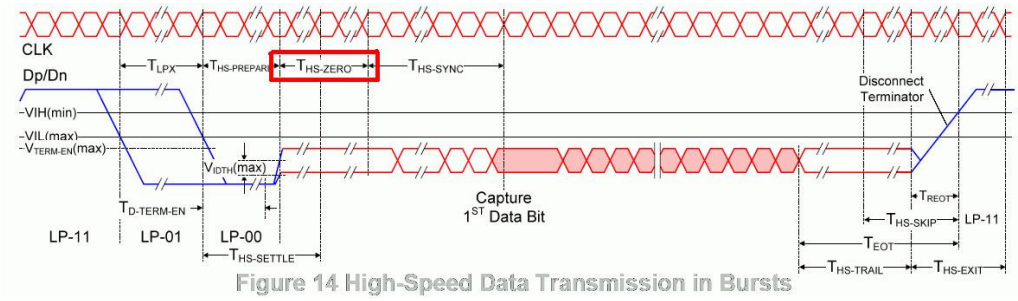


Figure: $T_{HS\text{-}ZERO}$ Interval

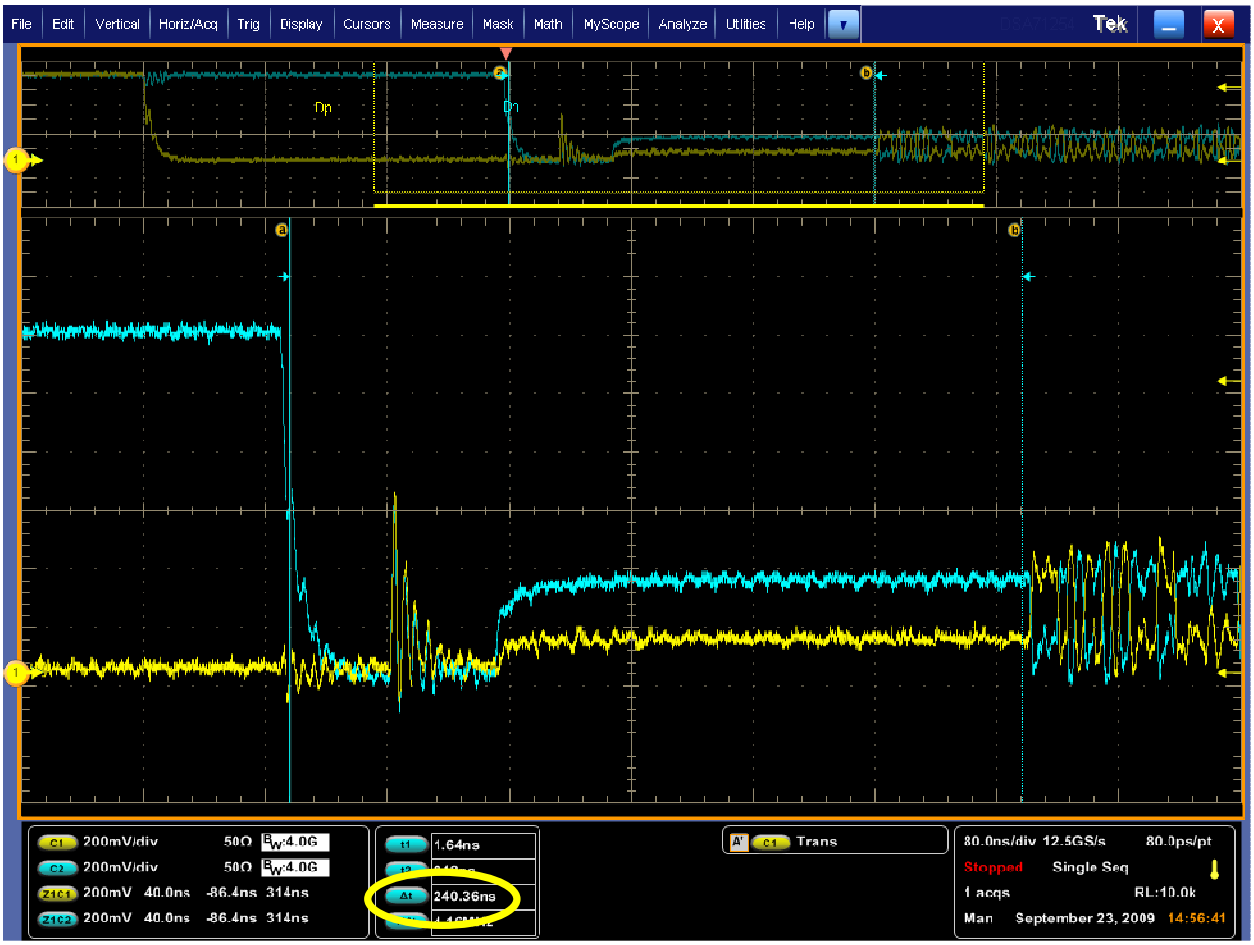
In this test, the DUT will be configured to source an HS burst sequence, starting and ending with LP-11 states. The ($T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$) interval begins at the time where the Data Lane V_{DN} signal crosses below $V_{IL,MAX}$ (550mV), and ends at the end of the extended $T_{HS\text{-}ZERO}$ HS-0 differential state, at the point corresponding to the start of the first bit of the HS Sync sequence. (Note that this point is not at the first HS-1 transition, but rather three HS Unit Intervals prior, as the Sync sequence starts with 0001. Thus there is no visible delineation between the extended HS-0 and the first HS-0 of the Sync sequence.) The measured duration of ($T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$) should be greater than (145ns + 10*UI) ns (where UI is the nominal HS Unit Interval for the DUT) in order to be considered conformant.

Test Setup: See Appendix A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix A)
2. Recall setup file "D-PHY_Test_8_1_12.set". Press the Single button to capture the desired part of the signal. (Note: If you do not see the zoomed portion of the signal, press the Multiview Zoom button.)
3. Ensure that the cursors are placed as per the diagram above. Include both $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ when taking measurement. Note that the Δt value as the total $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$.
4. Repeat for each data lane.

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that ($T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$) is greater than (145ns + 10*UI) ns for each Data Lane.

*: Other names and brands may be claimed as the property of others.

Test 8.1.13 – Data Lane HS Exit: $T_{HS\text{-}TRAIL}$ Value

Purpose: To verify that the duration the DUT Data Lane TX drives the inverted final differential state following the last payload data bit of a HS-TX burst ($T_{HS\text{-}TRAIL}$), is greater than the minimum required value.

References:

[1] D-PHY* Standard, Section 5.14.2, Line 1031
[2] Ibid, Section 5.9, Table 14
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.3.13

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

As part of the process of completing a HS Data Transmission Burst, the D-PHY Specification provides a requirement for the length of time that a device must drive the final extended HS differential state following the last payload data bit of a HS transmission burst. This interval is defined as $T_{HS\text{-}TRAIL}$, and is shown in the figure below.

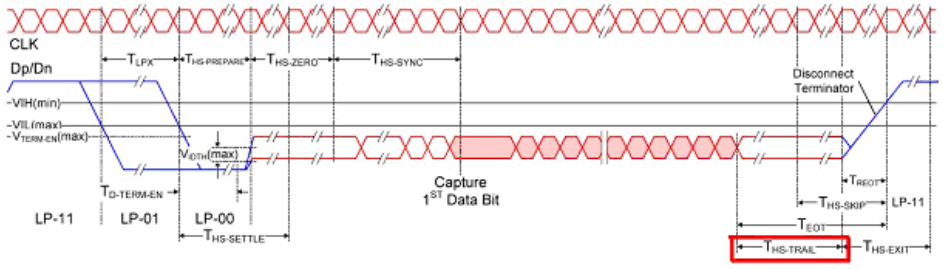


Figure: $T_{HS\text{-}TRAIL}$ Interval

After transmitting the final payload data bit of a HS Data Transmission Burst, the final extended HS differential state shall be held for a minimum duration of (n*8*UI) or (60 ns + n*4*UI), whichever is greater (where n = 1 for Forward-direction HS mode, and n = 4 for Reverse-direction HS mode).

In this test, an HS-TX Data Lane signaling burst from the DUT transmitter is captured using a real-time DSO. The differential waveform V_{OD} is computed as difference of the positive and negative single-ended waveforms (V_{DP}-V_{DN}). The $T_{HS\text{-}TRAIL}$ interval is measured for the final extended HS differential state, at the points where V_{OD} enters and exits the minimum valid HS-RX differential range (that is, when V_{OD} crosses +70 or -70 mV). The measured $T_{HS\text{-}TRAIL}$ result should be greater than max ((n*8*UI), (60 ns + n*4*UI)) to be considered conformant [2].

Test Setup: See Appendices A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix A).
2. Recall setup file "D-PHY_Test_8_1_13.set". Press single to get to the desired part of the signal. Note: Click on Multiview Zoom if you do not see the zoom area.
3. Ensure that the cursors apply to the area of the signal as shown in the diagram above.
4. Note the Δt value as the value of $T_{HS\text{-}TRAIL}$.
5. Repeat for each data lane.

*: Other names and brands may be claimed as the property of others.

Observable Results:

- Verify that $T_{HS\text{-}TRAIL}$ is greater than max ((n*8*UI), (60 ns + n*4*UI)) for each Data Lane.

*: Other names and brands may be claimed as the property of others.

GROUP 2: LP TX ELECTRICALS

Overview:

This group of tests verifies the Low-Power TX electrical requirements defined in Section 8.1.2 of the D-PHY* Standard.

Status:

The preliminary draft descriptions for the tests defined in this group are considered complete, and the tests are pending implementation (during which time additional revisions/modifications are likely to occur).

*: Other names and brands may be claimed as the property of others.

Test 8.2.1 – Data Lane LP-TX Thevenin Output High Level Voltage (V_{OH})

Purpose: To verify that the Thevenin Output High Level Voltage (V_{OH}) of the DUT's Data Lane LP transmitter is within the conformance limits.

References:

[1] D-PHY* Standard, Section 8.1.2, Line 1382
[2] Ibid, Section 8.1.2, Table 18
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.1.1

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

The D-PHY Specification states, *"V_{OH} is the Thevenin output, high-level voltage in the high-level state, when the pad pin is not loaded."* [1].

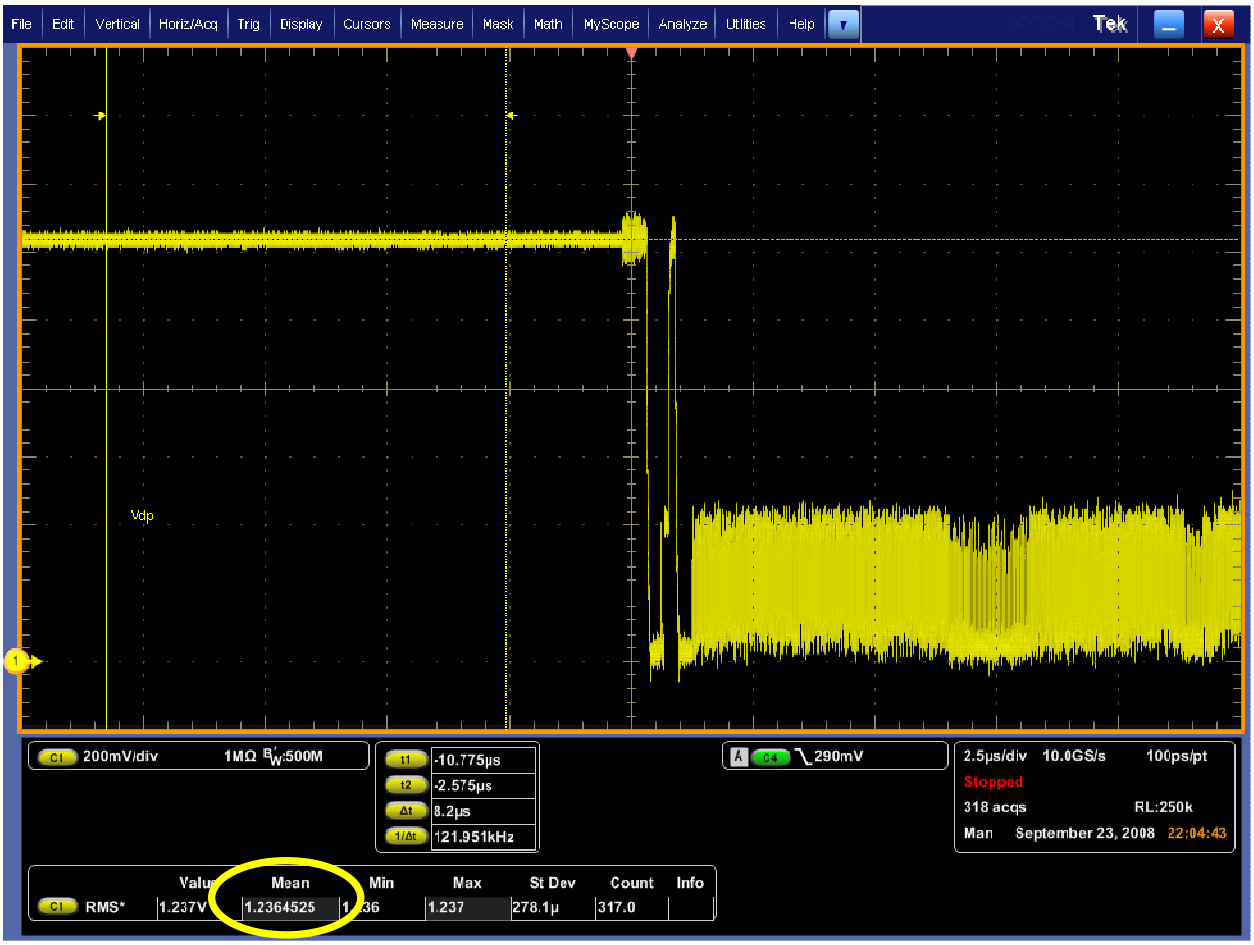
In this test, the DUT's Data Lane V_{OH} values is measured using a high-speed, real-time DSO while the DUT is driving an LP signaling sequence into an open termination. (Note that this test may be performed while the DUT is sourcing a fixed LP-11 state, but is typically intended to be performed with the other tests in this group on a single captured LP Escape Mode sequence waveform, in which case the measurement is performed on the output-high bits only.) For this measurement, V_{OH} is measured as the mode of all waveform samples that are greater than 50% of the absolute peak-to-peak V_{DP} and V_{DN} signal amplitudes. (Note that this measurement is performed separately on both the V_{DP} and V_{DN} waveforms, and for each DUT Data Lane.)

The value of V_{OH} for both the V_{DP} and V_{DN} signals for each Data Lane must be between 1.1 V and 1.3 V in order to be considered conformant [2].

Test Setup: See Appendices A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix A).
2. Create a condition that causes the DUT to source a continuous LP-11 state.
3. Recall setup file "D-PHY_Test_8_2_1.set". Press Single button to reach the desired part of the signal.
4. Note the value of Mean RMS as V_{OH}.
   - Place cursors in the LP-11 part of the signal.
   - Go to Measure > Amplitude > RMS.
   - Ensure that the correct source is chosen and cursor gating is applied.
5. Repeat for Ch 2 (D_N) and note the result.



Observable Results:

- Verify that V_{OH} for the V_{DP} waveform is between 1.1 and 1.3 Volts for each Data Lane.
- Verify that V_{OH} for the V_{DN} waveform is between 1.1 and 1.3 Volts for each Data Lane.

*: Other names and brands may be claimed as the property of others.

Test 8.2.2 – Data Lane LP-TX Thevenin Output Low Level Voltage (V_{OL})

Purpose: To verify that the Thevenin Output Low Level Voltage (V_{OL}) of the DUT's Data Lane LP transmitter is within the conformance limits.

References:

[1] D-PHY* Standard, Section 8.1.2, Line 1381
[2] Ibid, Section 8.1.2, Table 18
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.1.2

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

The D-PHY Specification states, *"V_{OL} is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low-level state."* [1].

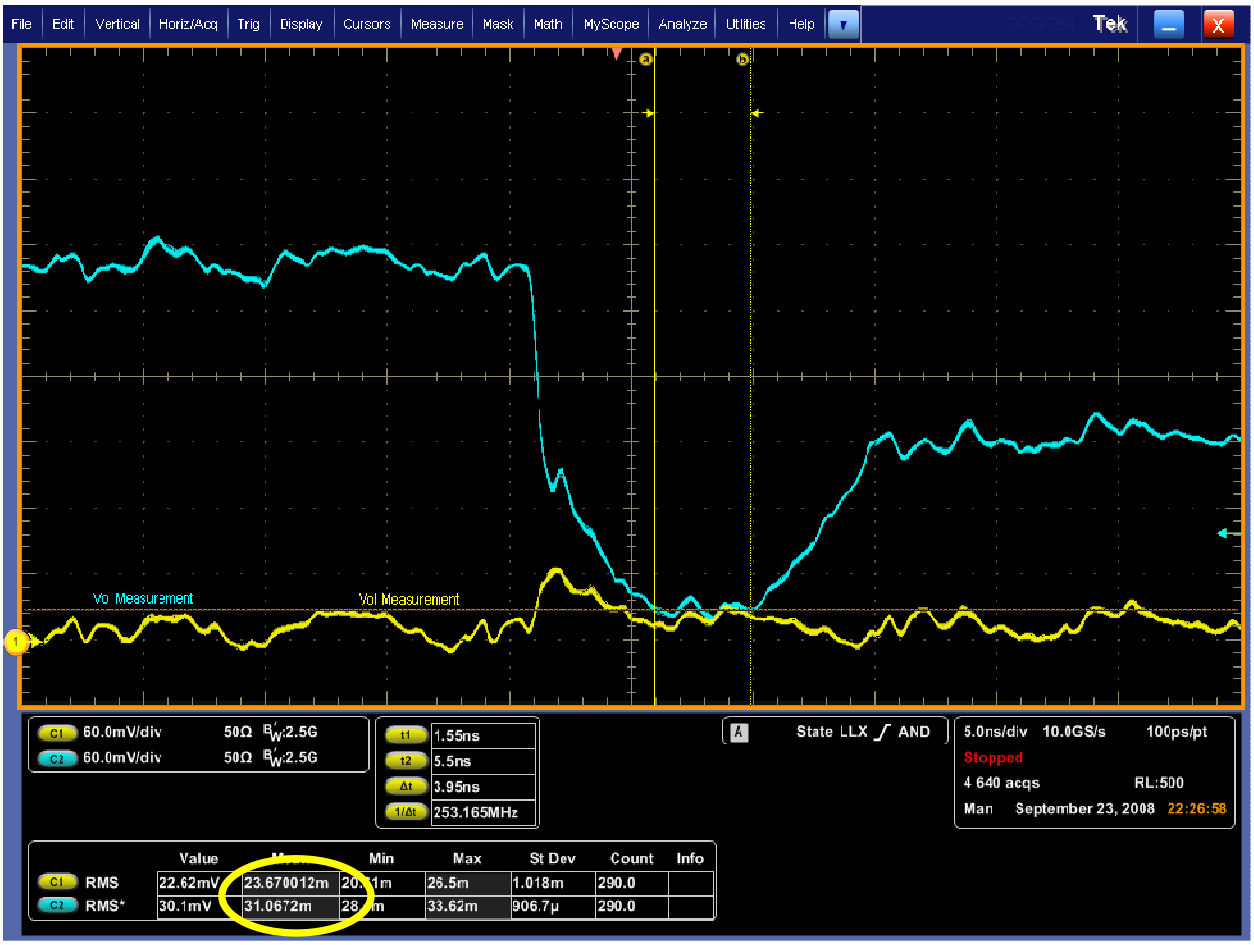
In this test, the DUT's Data Lane V_{OL} values is measured using a high-speed, real-time DSO while the DUT is driving an LP signaling sequence into an open termination. (Note that this test is intended to be performed in conjunction with the other tests in this group on a single captured LP Escape Mode sequence waveform, in which case the measurement is performed on the output-low bits only.) For this measurement, V_{OL} is measured as the mode of all waveform samples that are less than 50% of the absolute peak-to-peak V_{DP} and V_{DN} signal amplitudes. (Note that this measurement is performed separately on both the V_{DP} and V_{DN} waveforms, and for each DUT Data Lane.)

The value of V_{OL} for both the V_{DP} and V_{DN} signals for each Data Lane must be between –50 mV and +50 mV in order to be considered conformant [2].

Test Setup: See Appendices A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix B).
2. Create a condition that causes the DUT to source a continuous LP-00 state.
3. Load the setup file named D-PHY_Test_8_2_2.set.
4. Make sure cursors are set to cover only the portion of the waveform where both Dp and Dn are simultaneously low. Read the Ch1 and Ch2 RMS voltage measurement from the display.



Observable Results:

- Verify that V_{OL} for the V_{DP} waveform is between -50 and +50 mV for each Data Lane.
- Verify that V_{OL} for the V_{DN} waveform is between -50 and +50 mV for each Data Lane.

*: Other names and brands may be claimed as the property of others.

Test 8.2.3 – Data Lane LP-TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$)

Purpose: To verify that the Slew Rate ($\delta V/\delta t_{SR}$) of the DUT's Data Lane LP transmitter is within the conformance limit, for different capacitive loading conditions.

References:

[1] D-PHY* Specification, Section 8.1.2, Line 1397
[2] Ibid, Section 8.1.2, Table 19
[3] Ibid, Section 8.1.2, Figure 45
[4] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.1.5

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [4]:

The D-PHY Specification states, *"The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The slew rate specification shall be met for the 15% to 85% range while driving a capacitive load, C_{LOAD}."* [1]. A Figure provided in the specification that shows a graphical representation of the Slew Rate conformance range, is reproduced below.

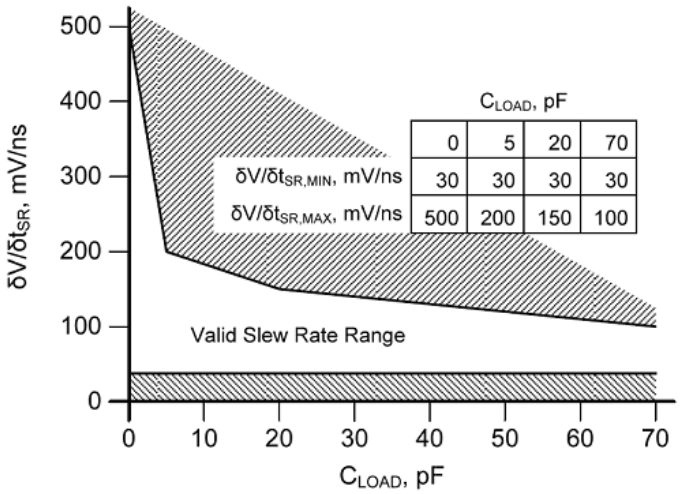


Figure: Slew Rate vs. C_{LOAD} Mask

The specific values are defined in [2] as:

- $\delta V/\delta t_{SR}$ into C_{LOAD} = 0pF shall be between 30 and 500 mV/ns.
- $\delta V/\delta t_{SR}$ into C_{LOAD} = 5pF shall be between 30 and 200 mV/ns.
- $\delta V/\delta t_{SR}$ into C_{LOAD} = 20pF shall be between 30 and 150 mV/ns.
- $\delta V/\delta t_{SR}$ into C_{LOAD} = 70pF shall be between 30 and 100 mV/ns.

The specification also states that the ***maximum*** Slew Rate requirement is to be measured when the output voltage is between 15% to 85% of the "fully settled LP signal levels" and is measured as an average across any 50 mV segment of the output signal transition.

Also note that the ***minimum*** Slew Rate requirement is applicable over the vertical region between 400 and 930 mV across any 50 mV segment of the output signal transition. [2]. (This is different from the applicable range for the maximum Slew Rate specification.)

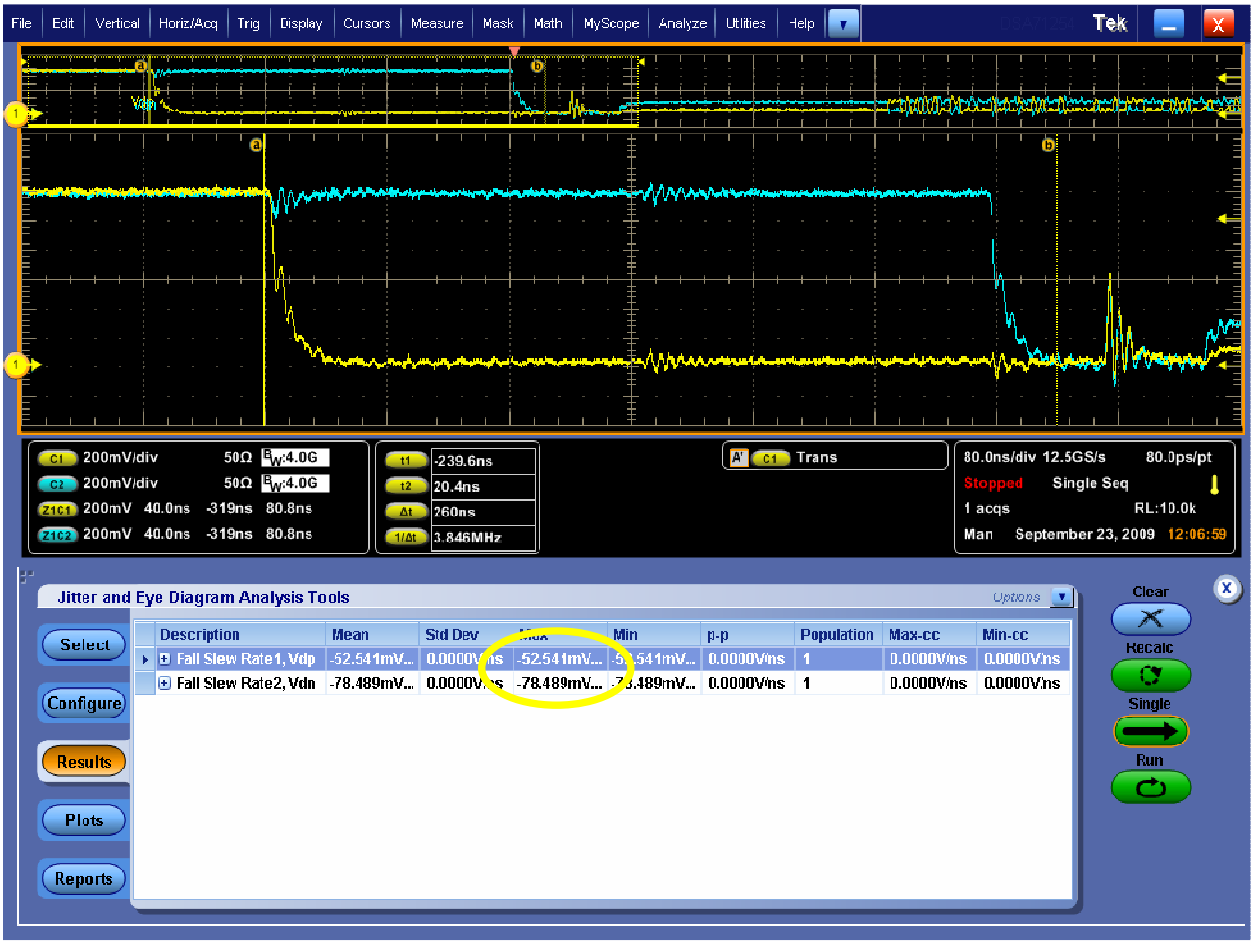
*: Other names and brands may be claimed as the property of others.

In this test, the two single-ended V_{DP} and V_{DN} signals from the DUT's Data Lane LP transmitter is captured using two channels of a real-time DSO. The Slew Rate is measured independently for each edge of the V_{DP} and V_{DN} signals. Maximum and minimum Slew Rate values is computed and reported for each rising and falling edge, across the applicable vertical ranges using a 50 mV vertical window. The measurement is repeated for all C_{LOAD} cases, and for all Data Lanes.

Test Setup: See Appendices A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix B).
2. Configure the load termination for C_{LOAD} = 0pF.
3. Create a condition that causes the DUT to source an LP Escape Mode sequence on Data Lane 0.
4. From the oscilloscope main menu, select Analyze>Jitter and Eye Analysis>Select.
5. Recall setup file D-PHY_Test_8_2_3.set.
6. Press Single button on the oscilloscope panel to reach the desired part of the signal.
7. Apply cursors to the specific part of the signal with rising and falling edges.
8. Press Single on DPOJET to make the measurement.



9. Repeat the previous steps for C_{LOAD} values of 5pF, 20pF, and 70pF.
10. Repeat the previous steps for Data Lanes 1, 2, and 3 (if the DUT implements multiple Data Lanes).

Observable Results:

*: Other names and brands may be claimed as the property of others.

- Verify that the maximum $\delta V/\delta t_{SR}$ into a C_{LOAD} of 0pF is less than 500 mV/ns for each Data Lane.
- Verify that the maximum $\delta V/\delta t_{SR}$ into a C_{LOAD} of 5pF is less than 200 mV/ns for each Data Lane.
- Verify that the maximum $\delta V/\delta t_{SR}$ into a C_{LOAD} of 20pF is less than 150 mV/ns for each Data Lane.
- Verify that the maximum $\delta V/\delta t_{SR}$ into a C_{LOAD} of 70pF is less than 100 mV/ns for each Data Lane.
- For all load cases, verify that the minimum $\delta V/\delta t_{SR}$ is greater than 30 mV/ns for each Data Lane.

Test 8.2.4 – Data Lane LP-TX 15%-85% Rise Time (T_{RLP})

Purpose: To verify that the 15%-85% Rise Time (T_{RLP}) of the DUT's Data Lane LP transmitter is within the conformance limits.

References:

[1] D-PHY* Specification, Section 8.1.2, Line 1395
[2] Ibid, Section 8.1.2, Table 19
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.1.3

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

The D-PHY Specification states, *"The times T_{RLP} and T_{FLP} are the 15%-85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages."* [1].

In this test, the two single-ended V_{DP} and V_{DN} signals from the DUT's Data Lane LP transmitter is captured using two channels of a real-time DSO. Using the measured V_{OH} and V_{OL} LP-TX Thevenin Output Voltage Levels as references, the 15%-85% Rise Time (T_{RLP}) is measured independently for each rising edge of the V_{DP} and V_{DN} waveforms. The mean value across all observed rising edges is computed to produce the final T_{RLP} result, and the maximum and minimum observed values is reported as informative results.

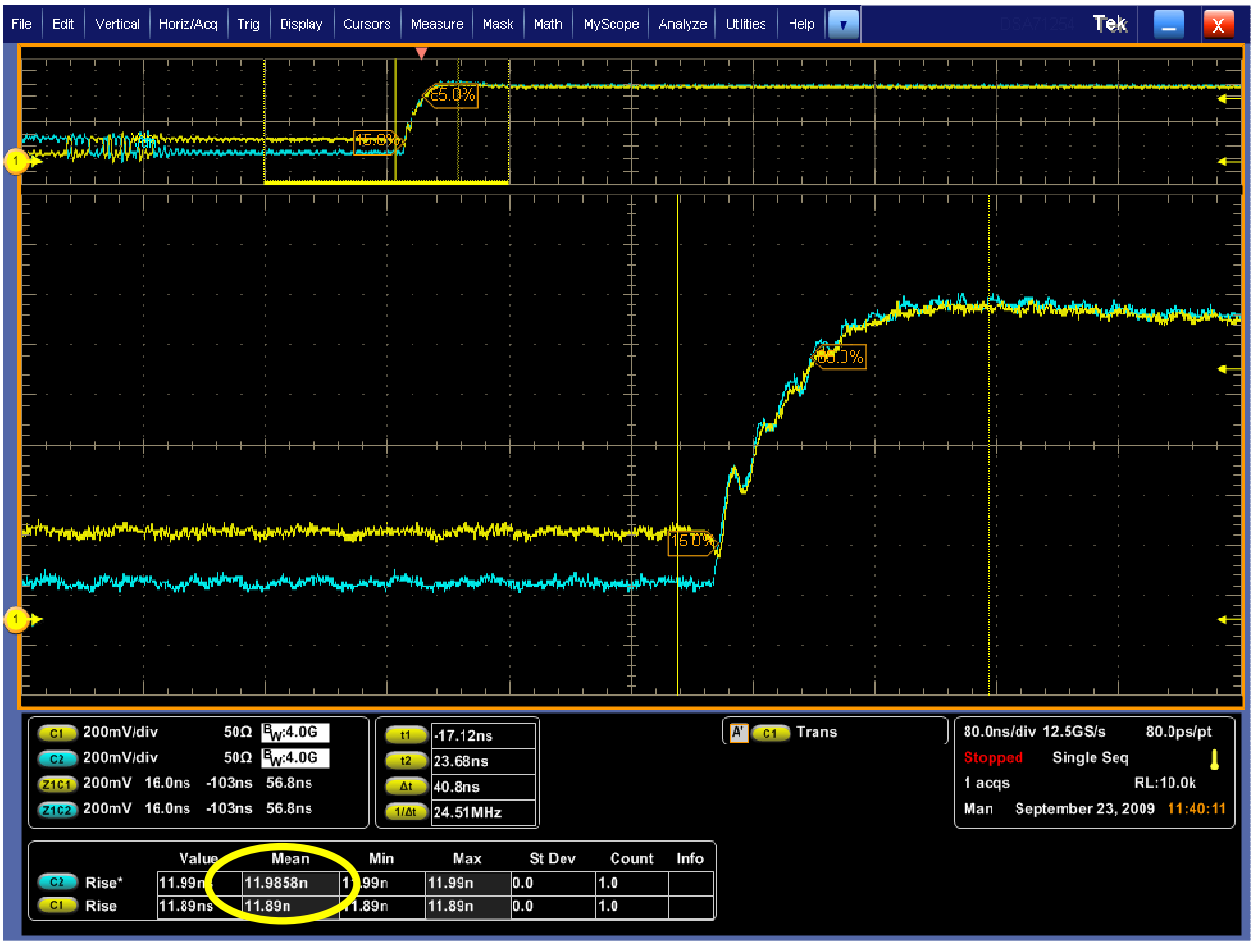
The value of T_{RLP} for V_{DP} and V_{DN} must be less than 25ns to be considered conformant [2].

Test Setup: See Appendices A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix B).
2. Recall setup "D-PHY_Test_8_2_4.set".
3. Press single to go to the desired part of the signal.
4. Measure T_{RLP} from the Rise time values.

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that T_{RLP} is less than 25 ns for the V_{DP} waveform for all C_{LOAD} cases for each Data Lane.
- Verify that T_{RLP} is less than 25 ns for the V_{DN} waveform for all C_{LOAD} cases for each Data Lane.

*: Other names and brands may be claimed as the property of others.

Test 8.2.5 – Data Lane LP-TX 15%-85% Fall Time (T_{FLP})

Purpose: To verify that the 15%-85% Fall Time (T_{FLP}) of the DUT's Data Lane LP transmitter is within the conformance limits.

References:

[1] D-PHY* Specification, Section 8.1.2, Line 1395
[2] Ibid, Section 8.1.2, Table 19
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.1.4

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

The D-PHY Specification states, *"The times T_{RLP} and T_{FLP} are the 15%-85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15% to 85% levels are relative to the fully settled V_{OH} and V_{OL} voltages."* [1].

In this test, the two single-ended V_{DP} and V_{DN} signals from the DUT's Data Lane LP transmitter is captured using two channels of a real-time DSO. Using the measured V_{OH} and V_{OL} LP-TX Thevenin Output Voltage Levels as references, the 15% to 85% Fall Time (T_{FLP}) is measured independently for each falling edge of the V_{DP} and V_{DN} waveforms. The mean value across all observed falling edges is computed to produce the final T_{FLP} result, and the maximum and minimum observed values is reported as informative results.

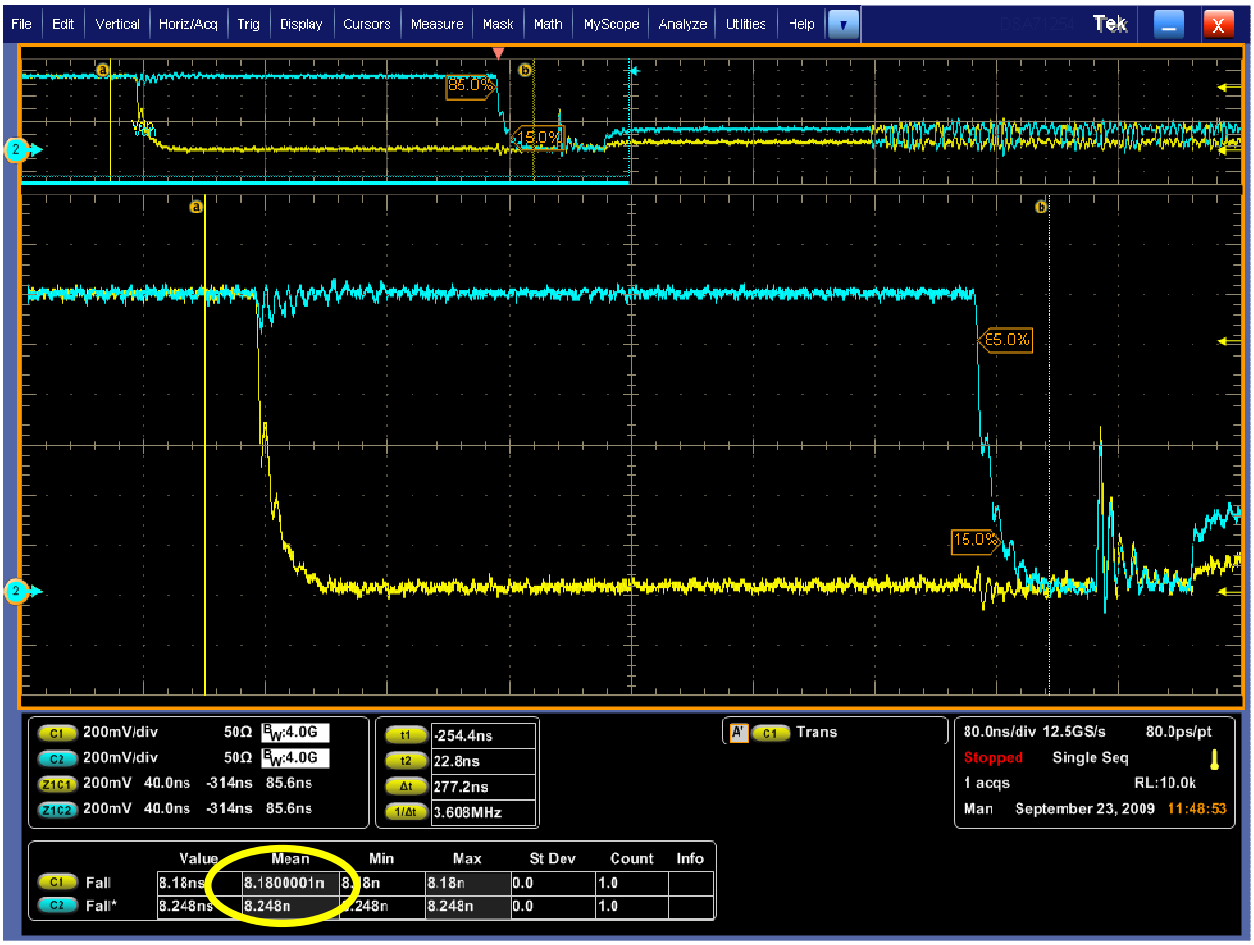
The value of T_{FLP} for V_{DP} and V_{DN} must be less than 25 ns to be considered conformant [2].

Test Setup: See Appendices A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix B).
2. Recall setup "D-PHY_Test_8_2_5.set".
3. Press single to go to the desired part of the signal.
4. Measure T_{FLP} from the Fall time values.

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that T_{FLP} is less than 25 ns for the V_{DP} waveform for all C_{LOAD} cases for each Data Lane.
- Verify that T_{FLP} is less than 25 ns for the V_{DN} waveform for all C_{LOAD} cases for each Data Lane.

*: Other names and brands may be claimed as the property of others.

Test 8.2.6 – Data Lane LP TX: 30%-85% Post-EoT Rise Time (T_{REOT})

Purpose: To verify that the 30%-85% Post-EoT Rise Time (T_{REOT}) of the DUT LP Data Lane transmitter is within the conformance limits.

References:

[1] D-PHY* Standard, Section 8.1.2, Line 1417
[2] Ibid, Section 8.1.2, Table 19
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.3.14

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

The D-PHY Specification states, *"The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70 mV, due to stopping the differential drive."* [1].

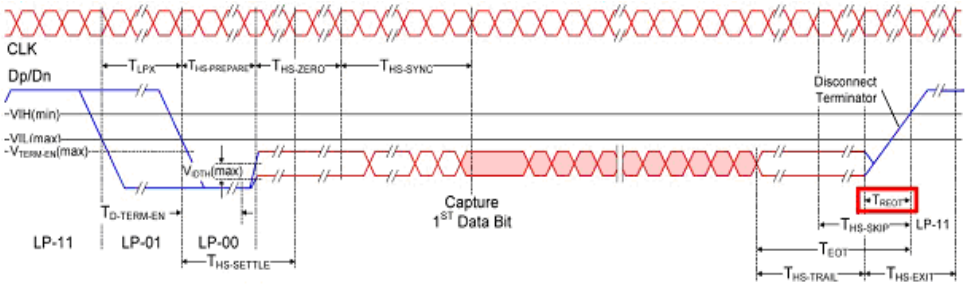


Figure: T_{REOT} Rise Time

In this test, an HS-TX Data Lane signaling burst from the DUT transmitter is captured using a real-time DSO. The differential waveform V_{OD} is computed as difference of the positive and negative single-ended waveforms (V_{DP}-V_{DN}). The T_{REOT} Rise Time is measured starting at the time where V_{OD} last crosses +/- 70 mV, and ends where V_{DP} crosses $V_{IH,MIN}$ = 880 mV. (Note that the spec does not differentiate whether V_{DP} or V_{DN} should be used, as they are identical from the spec's perspective. However, for real devices the rise times may not be the same, and it may make a difference.)

The value of T_{REOT} must be less than 35 ns to be considered conformant [2].

Test Setup: See Appendices A and B.

Test Procedure:

1. Connect the DUT to the Test System (See Appendix B).
2. Configure the Test System to emulate the DUT link partner (Master or Slave).
3. Create a condition that causes a HS Data Transmission Burst to be sourced from the DUT and capture the exchange using the DSO.
4. Load the setup file named D-PHY_Test_8_2_6.set. Press Single to reach the desired part of the signal.
5. Cursors are set so that a min and a max of the waveform are between them and so that the edge to be measured is between them as shown in screen shot below.
6. Read out the Rise time measurements from Ch1 and Ch2.
7. Watch out for: If the HS signal is high at the time of transition to LP high then this may be very close to the 30% level. The noise may periodically result in incorrect rise time measurement that is too long. To check for this go to the Measurement Setup menu as shown in the fixture below and select Annotation to be for "1 Rise Time" or for "2 Rise Time". Either way the annotation marker

*: Other names and brands may be claimed as the property of others.

arrows on screen indicate the position at which the measurement is taken. If the arrows periodically jump then that is observable. This is only likely if the HS starts from a high level rather than from a low level.

Observable Results:

- Verify that T_{REOT} is less than 35 ns, for each Data Lane.

*: Other names and brands may be claimed as the property of others.

DATA-CLOCK TIMING

Overview:

This selection of tests verifies the Data and Clock requirements of D-PHY* products defined in the D-PHY* Standard.

Group 1 (9.1.x) verifies various requirements related to the HS Clock signal and the skew and setup/hold relationships to the HS Data signal.

GROUP 1: HS-TX CLOCK-TO-DATA LANE TIMING REQUIREMENTS

Overview:

This group of tests verifies various requirements regarding Clock Lane to Data Lane timing.

Status:

These tests have been performed manually as per the conformance requirements. All tests listed by the UNH* Conformance Test Suite ver 0.08 are present here.

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*: Other names and brands may be claimed as the property of others.

Test 9.1.1 – HS Entry: $T_{CLK\text{-}PRE}$ Value

Purpose: To verify that the time that the HS clock is driven prior to an associated Data Lane beginning the transition from LP to HS mode ($T_{CLK\text{-}PRE}$), is greater than the minimum required value.

References:

[1] D-PHY* Standard, Section 5.14.1, Line 1013
[2] Ibid, Section 5.9, Table 14
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.5.1

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

As part of the process for initiating an HS data burst transmission, the D-PHY Specification provides a requirement for the minimum duration that the Master must transmit valid HS Clock signaling before driving any Data Lane out of LP mode. (Note that this test is only applicable to Master DUT's that support LP capability on the Clock Lane). This interval is defined as $T_{CLK\text{-}PRE}$, and is shown in the figure below.

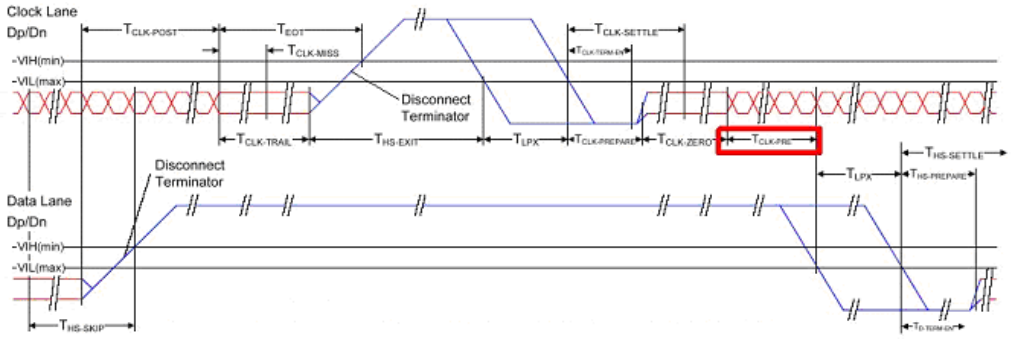


Figure: $T_{CLK\text{-}PRE}$ Interval

In this test, the DUT is configured to send an HS burst sequence, and the $T_{CLK\text{-}PRE}$ value is observed. The $T_{CLK\text{-}PRE}$ interval is measured from the end of the Clock Lane $T_{CLK\text{-}ZERO}$ interval (at the point where V_{OD} crosses below the minimum valid HS-RX differential threshold level of +/-70 mV) to the point where the Data Lane's V_{DP} LP-01 falling edge crosses $V_{IL,MAX}$ (550 mV).

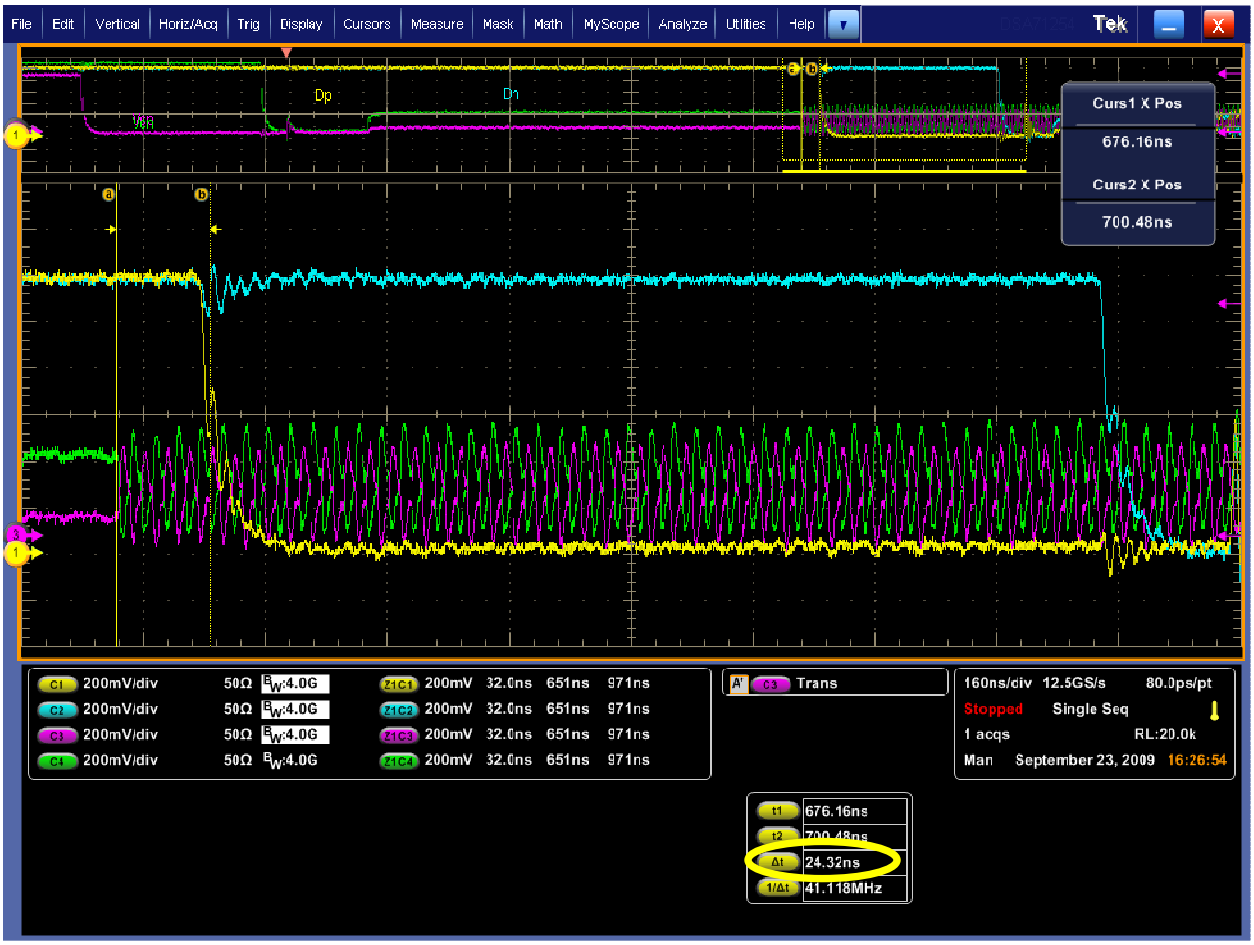
The measured value of $T_{CLK\text{-}PRE}$ must be greater than 8*UI to be considered conformant[2]

Test Setup: See Appendix A.

Test Procedure:

1. Connect the DUT to the Test Setup.
2. Create a condition that causes the DUT to source a Clock Lane/Data Lane 0 HS burst sequence.
3. Recall setup file D-PHY_Test_9_1_1.set.
4. Press Single button to reach the desired portion of the signal. Apply cursors as shown in the diagram above.
5. Measure Δt as the $T_{CLK\text{-}PRE}$.
6. Repeat the previous steps for Data Lanes 1, 2, and 3 (if the DUT implements multiple Data Lanes).

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that $T_{CLK\text{-}PRE}$ is greater than 8*UI for each Data Lane.

*: Other names and brands may be claimed as the property of others.

Test 9.1.2 – HS Exit: $T_{CLK\text{-}POST}$ Value

Purpose: To verify that the DUT Clock Lane HS transmitter continues to transmit clock signaling for the minimum required duration ($T_{CLK\text{-}POST}$) after the last Data Lane switches to LP mode.

References:

[1] D-PHY* Standard, Section 5.7, Line 920
[2] Ibid, Section 5.9, Table 14
[3] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.5.2

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [3]:

As part of the process for completing an HS data burst transmission, the D-PHY Specification provides a requirement for the minimum duration that the Master must continue to transmit HS Clock signaling after the last Data Lane has switched to LP mode [1]. (Note this test is only applicable to Master DUT's that support LP capability on the Clock Lane). This interval is defined as $T_{CLK\text{-}POST}$, and is shown in the figure below.

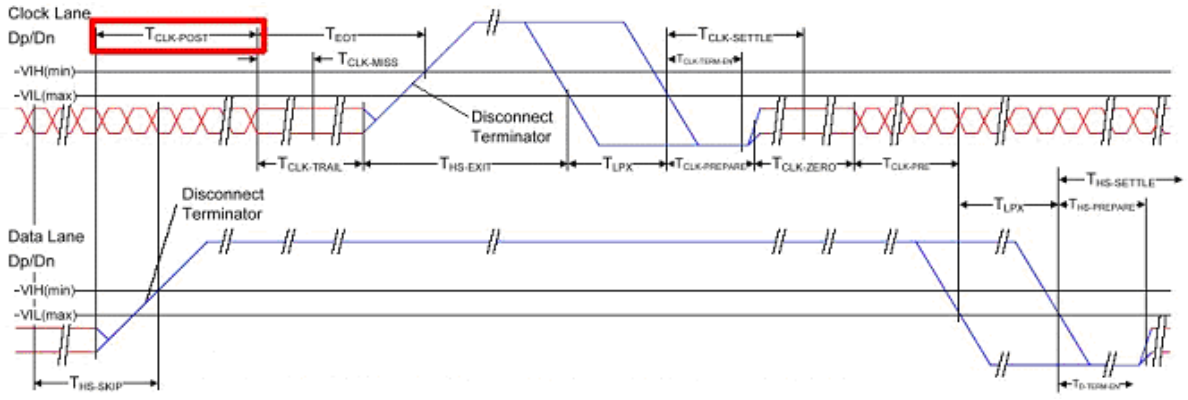


Figure: $T_{CLK\text{-}POST}$ Interval

In this test, the DUT is configured to send an HS burst sequence, and the $T_{CLK\text{-}POST}$ value is observed. The $T_{CLK\text{-}POST}$ interval is measured from the end of the Data Lane $T_{HS\text{-}TRAIL}$ period to the start of the Clock Lane $T_{CLK\text{-}TRAIL}$ period.

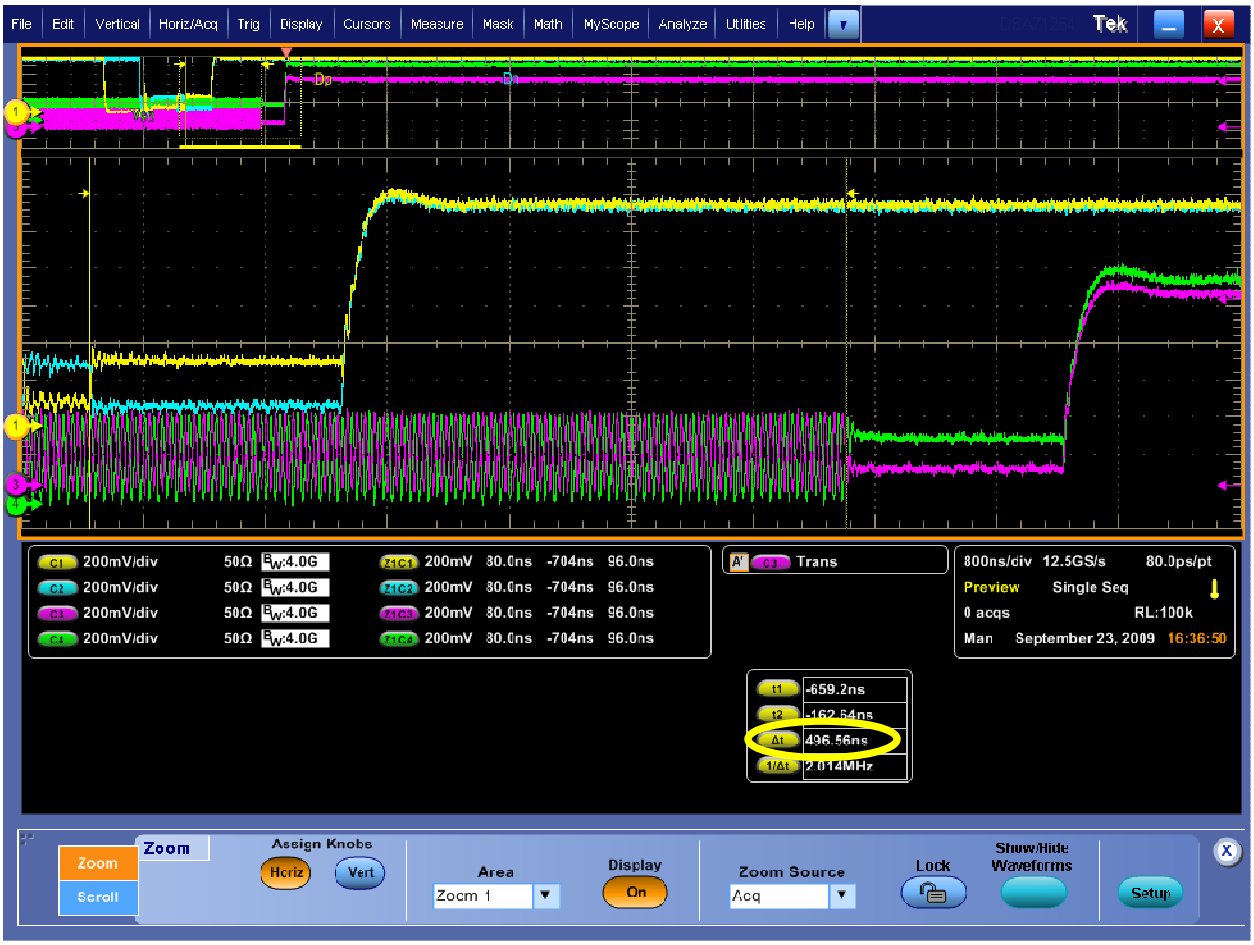
The measured value of $T_{CLK\text{-}POST}$ must be greater than (60 ns + 52*UI) ns in order to be considered conformant[2].

Test Setup: See Appendices A and B.

Test Procedure:

1. Connect the DUT to the Test Setup.
2. Create a condition that causes the DUT to source a Clock Lane/Data Lane 0 HS burst sequence.
3. Recall setup file D-PHY_Test_9_1_2.set.
4. Press the Single button to reach the desired portion of the signal. Apply cursors as shown in the diagram above.
5. Measure Δt as the $T_{CLK\text{-}POST}$.

*: Other names and brands may be claimed as the property of others.



Observable Results:

- Verify that $T_{CLK\text{-}POST}$ is greater than (60 ns + 52*UI) ns for each Data Lane.

*: Other names and brands may be claimed as the property of others.

Test 9.1.3 – HS Clock Rising Edge Alignment to First Payload Bit

Purpose: To verify that the DUT HS Clock is properly aligned to the payload data signaling.

References:

[1] D-PHY* Standard, Section 9.2, Line 1575
[2] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.5.3

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [2]:

The D-PHY Specification states, *"The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges."* [1].

In this test, the DUT is configured to send an HS burst sequence, and the Clock and Data Lane signals is observed using a real-time DSO. The signaling behavior is visually examined to verify that the first payload bit of a transmission burst aligns with a rising edge of the DDR clock.

Test Setup: See Appendices A and B.

Test Procedure:

- Connect the DUT to the Test Setup.
- Create a condition that causes the DUT to source a Clock Lane/Data Lane 0 HS burst sequence.
- Recall setup file D-PHY_Test_9_1_3.set. Press Single for getting to the desired part of the signal.
- Using oscilloscope cursors, find the direction of the DDR clock edge that corresponds to the first Data Lane payload bit of the transmission burst (that is, rising or falling).
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if the DUT implements multiple Data Lanes).

Observable Results:

- The first Data Lane payload bit of the transmission burst must align with a rising edge of the DDR clock for each Data Lane.

*: Other names and brands may be claimed as the property of others.

Test 9.1.4 – Data-to-Clock Skew ($T_{SKEW(TX)}$)

Purpose: To verify that the skew between the clock and data signaling, as measured at the transmitter ($T_{SKEW(TX)}$) is within the conformance limits.

References:

[1] D-PHY* Standard, Section 9.2.1, Line 1589

[2] UNH* D-PHY* Conformance Test Suite, ver0.08, Test 1.5.3

Resource Requirements: Real-time DSO, D-PHY* test signal generator.

Last Modification: October 16, 2009

Discussion [2]:

The specification states, *"The skew specification, $T_{SKEW[TX]}$, is the allowed deviation of the data launch time to the ideal ½UI_{INST} displaced quadrature clock edge."*[1]. This relationship is graphically demonstrated using a figure in the specification, which is reproduced in the figure below.

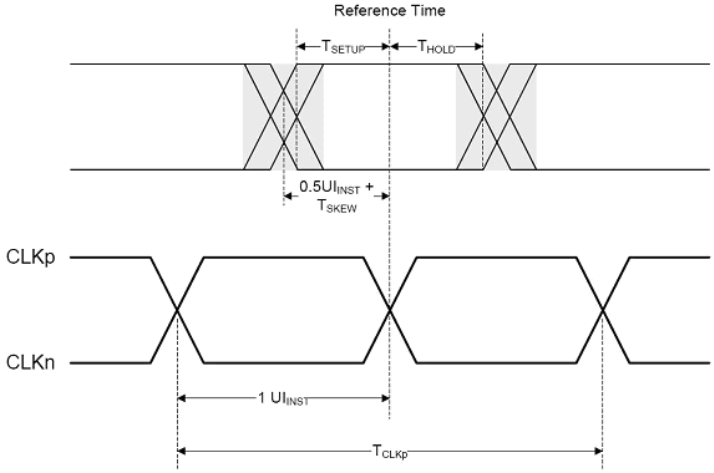


Figure: $T_{SKEW(TX)}$ Definition

In this test, the DUT is configured to send an HS burst sequence, and the Clock and Data Lane signals is observed using a real-time DSO. The timing error between each Data Lane edge and its respective Clock Lane edge is computed, to produce an array of timing error values. The max, min, and mean timing error values measured across all observed edges is recorded.

Test Setup: See Appendices A and B.

Test Procedure:

1. Connect the DUT to the Test Setup.
2. Create a condition that causes the DUT to source a Clock Lane/Data Lane 0 HS burst sequence.
3. Launch DPOJET using the main menu: Analyze>Jitter and Eye Analysis.
4. Recall the setup file D-PHY_Test_9_1_4.set.
5. Apply the explicit clock recovery as detailed in the previous tests.
6. Click Run.
7. Record the max, min, and mean timing error values from the results as given in the table.
8. Compare with the compliance requirement between 0.65UI_{INST} and 0.35UI_{INST}.
9. Repeat the previous steps for Data Lanes 1, 2, and 3 (if the DUT implements multiple Data Lanes).

*: Other names and brands may be claimed as the property of others.

Observable Results:

- Verify that the max, min, and mean Clock-to-Data timing error values are within the range (0.50+/-0.15)*UI_{INST} for each Data Lane.

Appendix A – Resource Requirements

The resource requirements include two separate sets of equipment.

A.1 Equipment for D-PHY* tests

1. Real-time Digital Oscilloscope (any one of the following instruments)
   Minimum DSA/DPO7254: Criteria is that it should support 1Gbps data rates
   Preferred DSA/DPO70604/70804: Since rise time criteria can be met +/- 5% (150ps)
   4 channel support required for clock and data

2. Software
   DPOJET

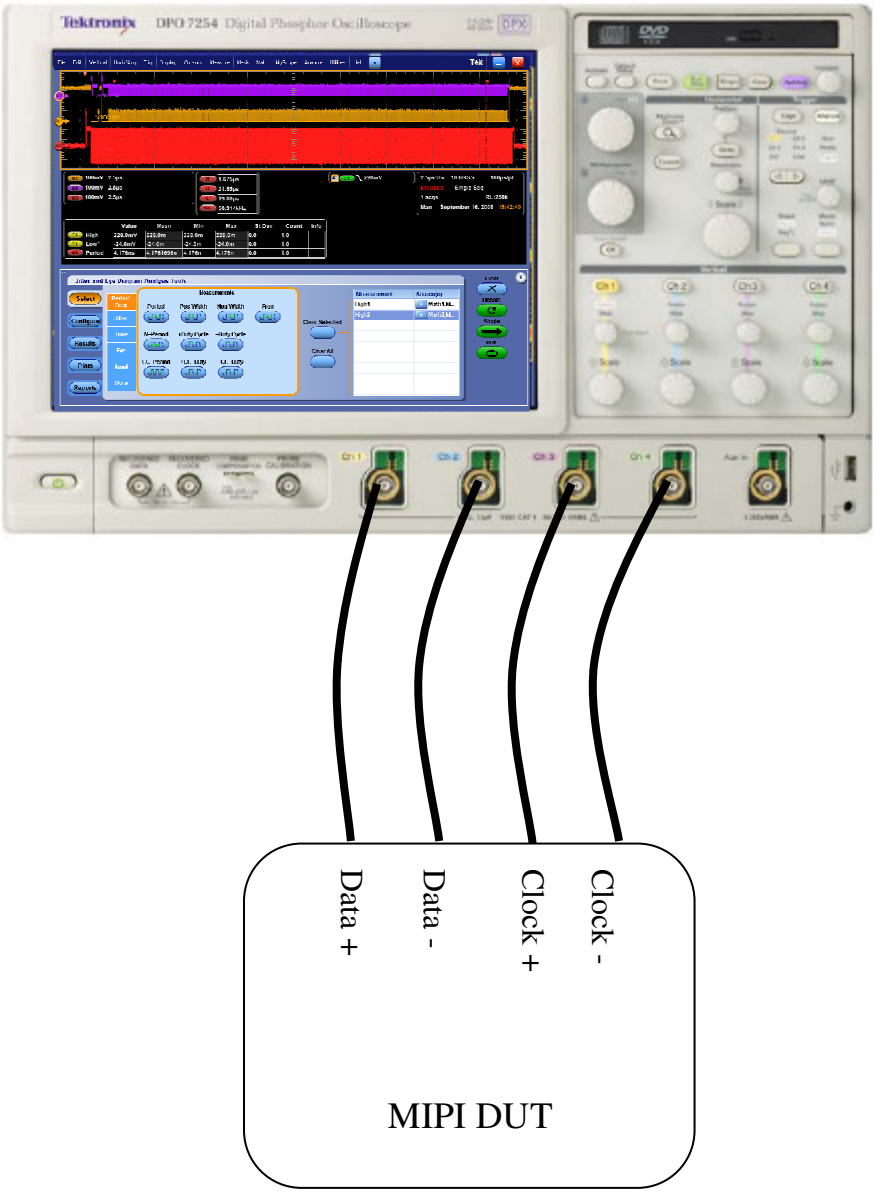
3. Probes P7240 for DSA/DPO70K and TDP3500 for DSA/DPO7K. P6249 is another alternative for DPO7K however; it is not going to be supported by Tektronix in the long term.
   a. Criteria - >1.2V dynamic range, 1x probe attenuation (2.5x or 5x are also ok) and we need to measure both single-ended and differential signals

4. (8) Cables - 1 meter SMA cable

5. (4.) TCA-292MM or TCS-SMA

*: Other names and brands may be claimed as the property of others.

Appendix B – DUT Connection



*: Other names and brands may be claimed as the property of others.

Appendix C – Deskew Procedure

Deskew for SMA Channels

Use the following procedure for de-skewing direct input SMA channels on an oscilloscope. This procedure is useful for any Tektronix real-time oscilloscope, using either SMA or 292mm inputs.

1. Run SPC on the oscilloscope.
2. Connect an SMA Power Splitter (preferred) or SMA 50 ohm coax tee to the Fast Edge output of the oscilloscope.
3. Connect SMA cables from each of the two channels to be de-skewed, to the power splitter (or SMA coax tee). It is best to use matched cables when making high speed serial measurements. It is critical to use the same cables that is used for subsequent measurements.
4. Press Default Setup, then Autoset on oscilloscope front panel.
5. Set oscilloscope for 70%-90% full screen amplitude on both channels. Center both traces to overlap.
6. Make sure that volts/div, position, and offset are identical for the two channels being de-skewed.
7. Set time/div to approx. 100 ps/div or less, with sample rate at 1 ps/pt. These settings are not critical, but should be close.
8. Set horizontal acquisition mode to average, which provides a more stable display.
9. Select Deskew from the Vertical menu.
10. Verify ref channel (typically Ch1 or Ch2) is set to 0 ps deskew.
11. In the deskew control window, click on channel to deskew (typically Ch3 or Ch4). Adjust deskew to overlay rising edge as best possible.

Note: Typical values are in the 10's of ps or less with cables connected directly from Fast Edge to SMA inputs. If you are using an RF relay switch box (for example Keithley), deskew the complete path from where the test fixture connects, through the switch, and into the oscilloscope. Deskew values in these cases may be as much as 30ps or more.

There are sometimes significant differences in skew between two TCA-SMA adapters. If you find that a system requires very large correction, it might be better to find a pair of TCA-SMA adapters that match each other better.

Do not forget to set the oscilloscope back to default settings when done.