

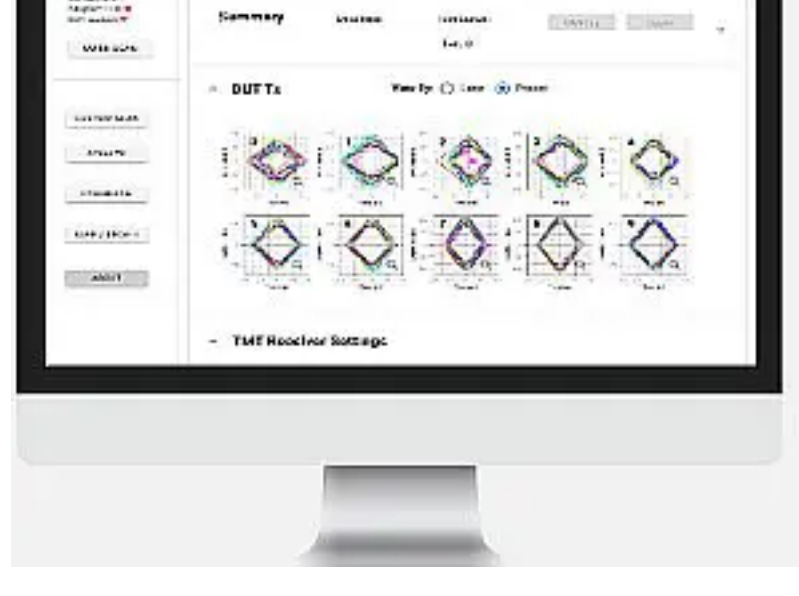
DESIGN
GUIDE ON RELAYS

In this Design Guide, the editors of EEWorld present not just the basics of this not-so-basic device, but key criteria to help you choose the best relay for your application, be it electromechanical or solid-state.

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ONLINEMargin tester checks out PCIe Gen 3,
Gen 4 designsOCTOBER 25, 2022 BY [LEE TESCHLER](#)

The new TMT4 Margin Tester breaks conventions of PCIe testing, delivering fast test times. Plug-and-play set up and easy-to-use interface combine to deliver in minutes results that, until now, required hours or even days of set up and testing, often stretching costs to seven figures.

"TMT4 Margin Tester is the latest example of how Tektronix continues to develop innovative test equipment, advancing technology solutions that accelerate progress and uniquely solve real-world problems" said Chris Witt, Vice President and General Manager of Portfolio Solutions at Tektronix. "The TMT4 Margin Tester empowers engineers to realize technological advances with ever greater ease and speed."



While PCIe testing normally requires complex test systems and engineers with deep expertise and knowledge, the TMT4 Margin Tester enables engineers at all levels of experience to evaluate the health of transmitter (Tx) and receiver (Rx) links faster than ever, greatly reducing time to market and cost of ownership. The platform supports the majority of common PCIe form factors, including CEM, M.2, U.2, and U.3, with testing capabilities of up to 16 lanes across PCIe presets 0-9, using a single standard connector.

The Tektronix TMT4 Margin Tester is intended to complement full validation and compliance testing systems consisting of oscilloscopes and BERTs, by making it possible to uncover issues earlier in the design process prior to an in-depth examination using traditional equipment.

New technologies are more complex than ever, requiring significant time and expertise to validate them. The new TMT4 Margin Tester enables engineers at all levels of expertise to test PCIe devices across up to 160 combinations of lanes and presets in as little as 20 minutes at Gen 4 speeds. Multi-lane testing capabilities enable users to significantly improve overall testing times by reducing the number of connection changes needed to perform testing.

Rina Raman, Vice President and General Manager DCAI, Embedded Acceleration Division at Intel, says: "Our team supported Tektronix to develop this new product category, knowing the importance of getting earlier insights and faster, more reliable results. The Tektronix TMT4 Margin Tester solution, built on the Intel Stratix 10 FPGA with PCIe, is easy for our engineers to use and the results are available substantially faster, in most cases, in minutes rather than hours. We have seen the benefits of this product to identify design issues much earlier in the design process."

Features:

- Quick Scan mode enables evaluation of link health for Gen 3 or Gen 4 devices, up to 16 lanes, in minutes, not hours or days.
- Custom Scan mode provides deeper insights by enabling users to scan Gen 3 or 4 devices, up to 16 lanes, across PCIe presets 0-9 (up to 160 combinations) in as little as 20 minutes.
- Simple setup and configuration minimize the need for senior-level engineers to perform link health evaluations of their designs.
- Full Tx/Rx protocol capability that enables link health evaluation of PCIe Gen 3 and Gen 4 communication technologies on both sides of the link in a single box.
- Multi-lane testing capabilities enable users to significantly improve overall testing times by reducing the number of connection changes needed to perform testing.
- Visibility of link training parameters provides additional insights into which equalization was used to form the link.
- Variety of adapters supporting the most common PCIe form factors for easy connection to motherboard and add-in card DUTs including CEM, M.2, U.2 and U.3.

Tektronix Inc., 14150 Southwest Karl Braun Drive, PO Box 500, Beaverton, OR 97077.

www.tek.com

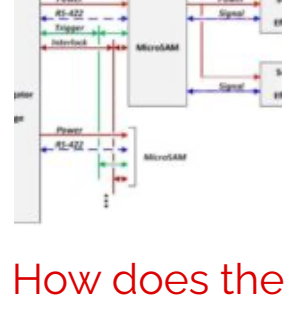
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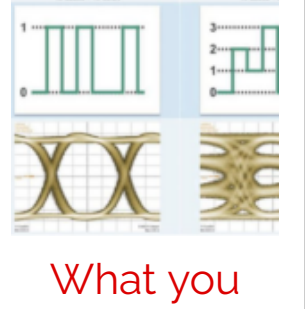
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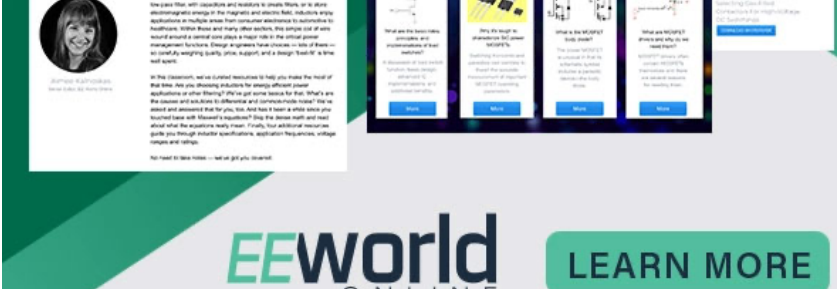
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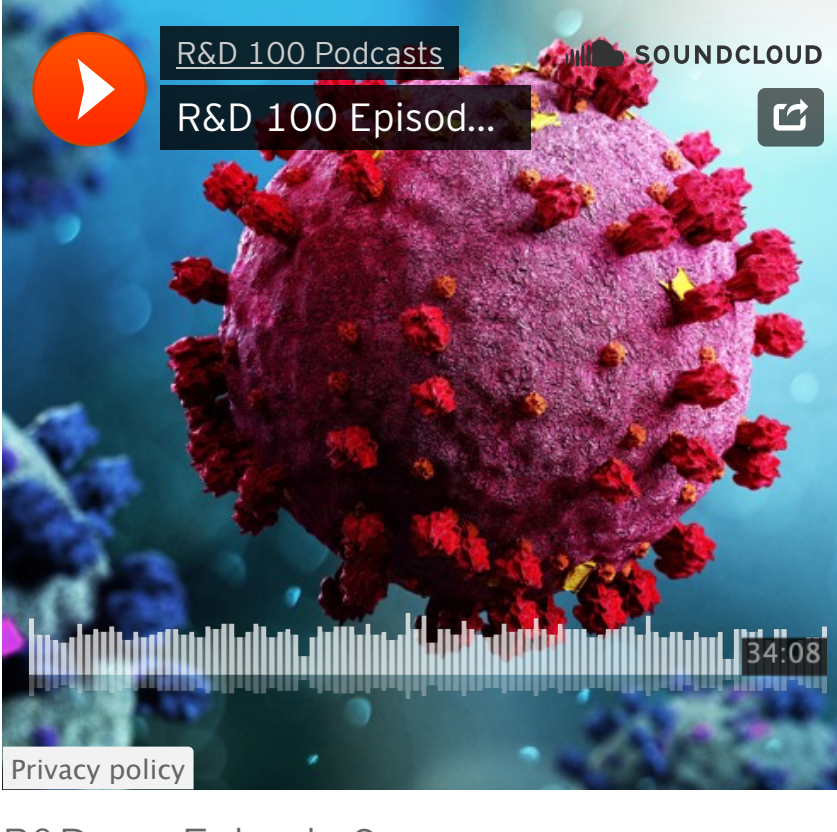
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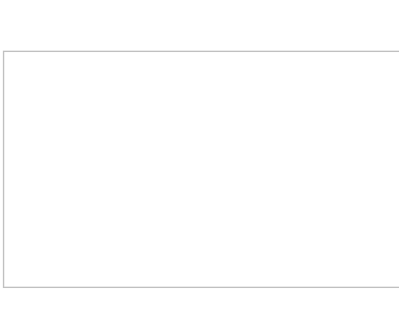
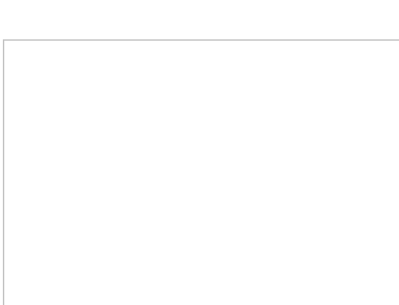
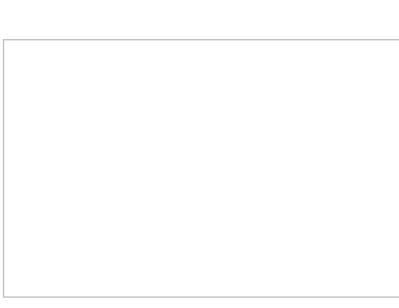
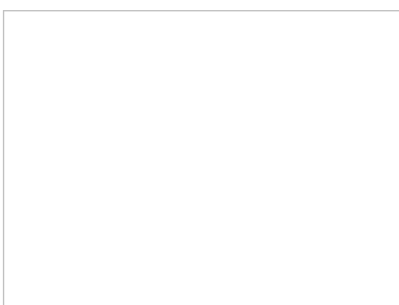
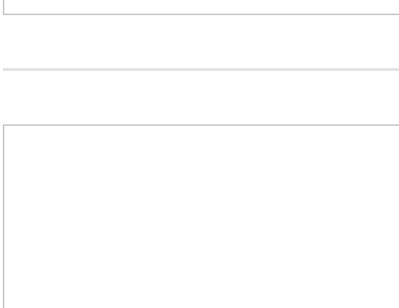
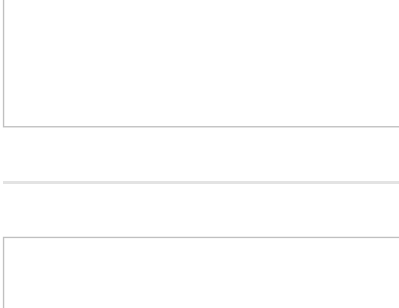
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