A Creative Solution for MIPI D-PHY Rx Validation

How NXP Semiconductors uses Tektronix transmitter test application to calibrate their receiver testing setup

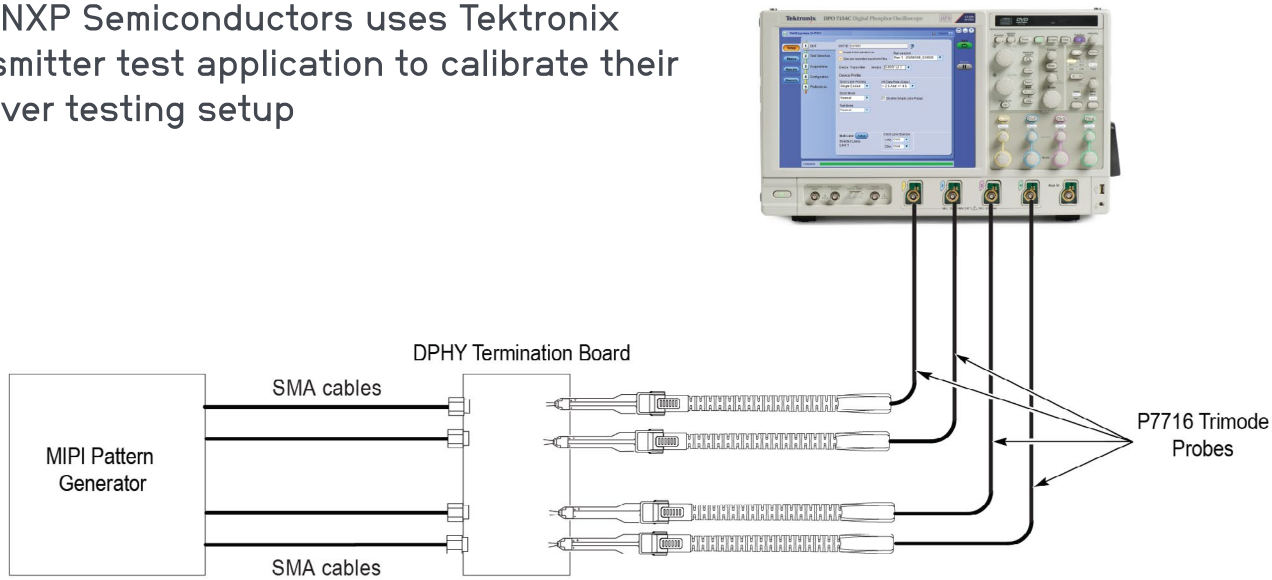

Figure 1. NXP uses a Tektronix automated D-PHY transmitter test system to calibrate a pattern generator and cabling used for receiver testing. The system includes a DPO71604C oscilloscope with the TekExpress D-PHY 1.2 automated compliance testing application and four P7716 TriMode Probes.

THE CHALLENGE

As a leader in secure connections and infrastructure for embedded applications, NXP Semiconductors is driving innovation in a variety of fields including automotive systems, where MIPI D-PHY is used as an interface to connect to RF MMICs that integrate radar transceivers.

With MIPI D-PHY being increasingly utilized in the development of multimedia processors, it can be challenging to validate MIPI D-PHY receivers (Rx) on IC designs. D-PHY often has 4 data lanes plus a clock lane. One typical method of covering all the necessary lanes is to use one multi-channel or several single-channel arbitrary waveform generators (AWGs). While precision AWGs are accurate and flexible, they're also expensive. It's also possible to use a pattern generator which is capable of sending data over 4 lanes simultaneously, and they're typically less expensive than AWGs. However, lower cost pattern generators require manual calibration for both amplitude and timing.

THE SOLUTION

Narender Singh, Staff Engineer at NXP Semiconductors developed an innovative method using a Tektronix oscilloscope's D-PHY transmitter (Tx) application to accurately and efficiently calibrate a pattern generator they are using for D-PHY receiver validation.

This is possible because all the measurements performed with the D-PHY Tx app are directly related to the parameters run in a D-PHY Rx validation framework. In other words, the D-PHY pattern generator signals measured using the D-PHY Tx app are the actual applied signals on the D-PHY Rx DUT.

Using the D-PHY Tx app for a D-PHY Rx calibration allows NXP to create the eye diagrams of each lane individually and store them in reports as needed. They can also measure a number of deterministic voltage characteristics in the pattern generator including:

- Differential amplitude
- Amplitude mismatch
- HS-Zero
- HS-Trail
- HSUI tolerance
- LP voltage (min/max)

In addition, time consuming measurements such as static and dynamic jitter in HS mode can also be calibrated using the D-PHY Tx app.

System Configuration

NXP Semiconductors utilized Tektronix's automated D-PHY Tx testing application, which is a standalone app that runs on a Tek oscilloscope, to calibrate a pattern generator for D-PHY Rx validation. Figure 1 (page 1) illustrates the connections NXP made in this set up. The instruments used in this system are:

- DPO71604C 16 GHz Oscilloscope
- P7716 16 GHz TriMode Probe with P77STFLXA probe tip
- DPHY 1.2 TAutomated Tx Testing Application

It's important to note that any connections between the pattern generator and the DUT should be de-embedded, and also the connections of the calibration setup must be de-embedded. To have a perfectly calibrated system, all setup losses must be accounted for.

The Tektronix automated D-PHY testing app was configured to measure the parameters NXP wants to calibrate with measured values. Once the calibration connections were made, NXP ran a test with the pattern generator using the testing app with the defined test parameters. Once the test was completed, the automated testing app generated a report listing the measured values for the pattern generator and test setup.

> The D-PHY Tx app is quite easy and intuitive to use. Even though the application is designed for D-PHY transmitter testing, I could successfully use it to calibrate my receiver test setup.
>
> **Narender Singh, Staff Engineer, NXP**

The screen capture in Figure 2 shows part of the test report as an example of some parameters that were measured on Tek's automated D-PHY testing application. With the differential output voltage (VOD) configured on the pattern generator at 200 mV, the VODs measured in Test 1.3.4 were 189mV and –197 mV. NXP could then make corrections of 10–12 mV in the Rx validation results.

Test Name Summary Table		
Test Name	**Result**	**Measurment Data**
1.3.1 Data Lane HS Entry: Data Lane TLPX Value	Pass	• Data Lane HS Entry: Data Lane TLPX Value (ns) : **83.486ns**
1.3.2 Data Lane HS Entry: THS-PREPARE Value	Pass	• Data Lane HS Entry: THS-PREPARE Value (ns) : **63.571ns**
1.3.3 Data Lane HS Entry: THS-PREPARE + THS-ZERO Value	Pass	• Data Lane HS Entry: THS-PREPARE + THS-ZERO Value = Value1 + Value2*UI (ns) : **213.198ns**
1.3.4 Data Lane HS-TX Differential Voltages (VOD(0), VOD(1))	Pass	• Data Lane VOD(1)(mV) : **189.855mV** • Data Lane VOD(0)(mV) : **-197.104mV**
1.3.5 Data Lane HS-TX Differential Voltage Mismatch (VOD)	Pass	• VOD(mV) : **7.25mV**
1.3.6 Data Lane HS-TX Single-Ended Output High Voltages (VOHHS(DP), VOHHS(DN))	Pass	• Data Lane HS-TX Single-Ended Output High Voltage (VOHHS(DP))(mV) : **289.91mV** • Data Lane HS-TX Single-Ended Output High Voltage (VOHHS(DN))(mV) : **293.294mV**
1.3.7 Data Lane HS-TX Static Common-Mode Voltages (VCMTX(1), VCMTX(0))	Pass	• Data Lane HS-TX Static Common-Mode Voltage VCMTX(0)(mV) : **191.511mV** • Data Lane HS-TX Static Common-Mode Voltage VCMTX(1)(mV) : **199.655mV**
1.3.8 Data Lane HS-TX Static Common-Mode Voltage Mismatch (VCMTX(1,0))	Pass	• Data Lane HS-TX Static Common-Mode Voltage Mismatch (VCMTX(1,0))(mV) : **-4.072mV**
1.3.9 Data Lane HS-TX Dynamic Common-Level Variations Between 50-450 MHz (VCMTX(LF))	Pass	• Data Lane HS-TX Dynamic Common-Level Variations(VCMTX(LF))(mV) : **8.21mV**
1.3.10 Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz (VCMTX(HF))	Pass	• Data Lane HS-TX Dynamic Common-Level Variations(VCMTX(HF))(mV) : **8.101mV**

Figure 2. An example of a test report showing parameters that were measured with Tektronix automated D-PHY testing application.

Figures 3a and 3b show examples of setup/hold measurements and an eye diagram produced on the D-PHY Tx oscilloscope application at a 2.5G data rate. This eye diagram and the measurements were used to calibrate the Rx setup. In this case, the values shown in the measurements closely matched with the configured values on the pattern generator. When NXP encountered any discrepancies between the measured and configured values on their pattern generator, they would use these measurements to create a look-up table that could be subsequently used in the D-PHY Rx validation.

Note how all the data-to-clock skew parameters in Figure 3a were recorded. This allowed them to be used later for Rx validation. In this example, the calibration was performed at 2.5G, but the same can be accomplished at any data-rate of the Rx DUT. Figure 3b is an eye diagram of a 2.5G example captured with the Tektronix D-PHY Tx scope application used to determine the quality of the eye for the Rx validation setup.

1.5.4 Data to Clock Skew (TSKEW(TX))								
Lane	Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit	Additional Information
Lane1	Max Data to Clock Skew LTEQ 1Gbps = (Value1 +/- Value2)* UIINST (ns)	0.225	ns	Pass	L:0.085ns H:0.035ns	0.14	0.26	Min value = 0.148, Max value = 0.225, Region count = 20158.0
Lane1	Min Data to Clock Skew LTEQ 1Gbps = (Value1 +/- Value2)* UIINST (ns)	0.148	ns	Pass	L:0.008ns H:0.112ns	0.14	0.26	N.A
Lane1	Mean Data to Clock Skew LTEQ 1Gbps = (Value1 +/- Value2)* UIINST (ns)	0.188	ns	Pass	L:0.048ns H:0.072ns	0.14	0.26	N.A
COMMENTS	Computed UI value(ns):0.4							

Figure 3a. Data to Clock Skew Measurements at 2.5G data rate.

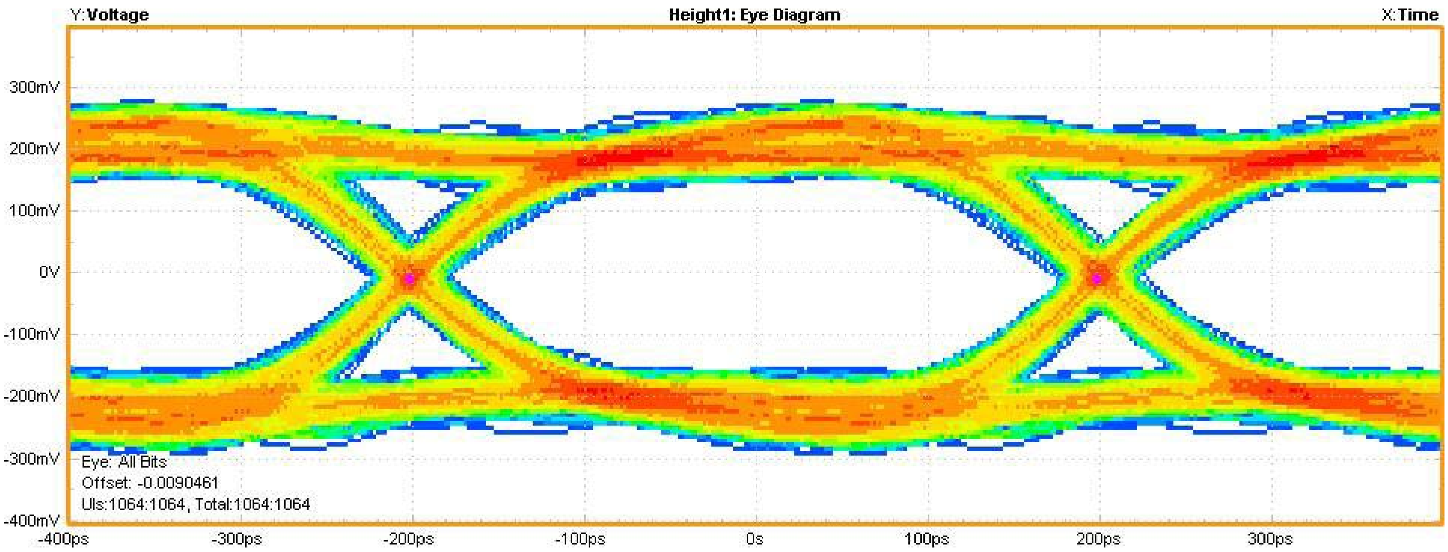

Figure 3b. Eye diagram at 2.5G data rate. This eye diagram and the measurements in Figure 3a are examples of data from the Tektronix D-PHY 1.2 Automated Transmitter Testing Software used to calibrate the Rx setup.

THE CONCLUSION

By using Tektronix's automated D-PHY Tx testing oscilloscope application, NXP Semiconductors was able to accurately and efficiently calibrate their pattern generator for D-PHY Rx validation. This solution has become instrumental in their ongoing innovation developing cutting-edge automotive processors.

For Further Information
Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

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