Tektronix

New application and test introduction

KEITHLEY
A Tektronix Company

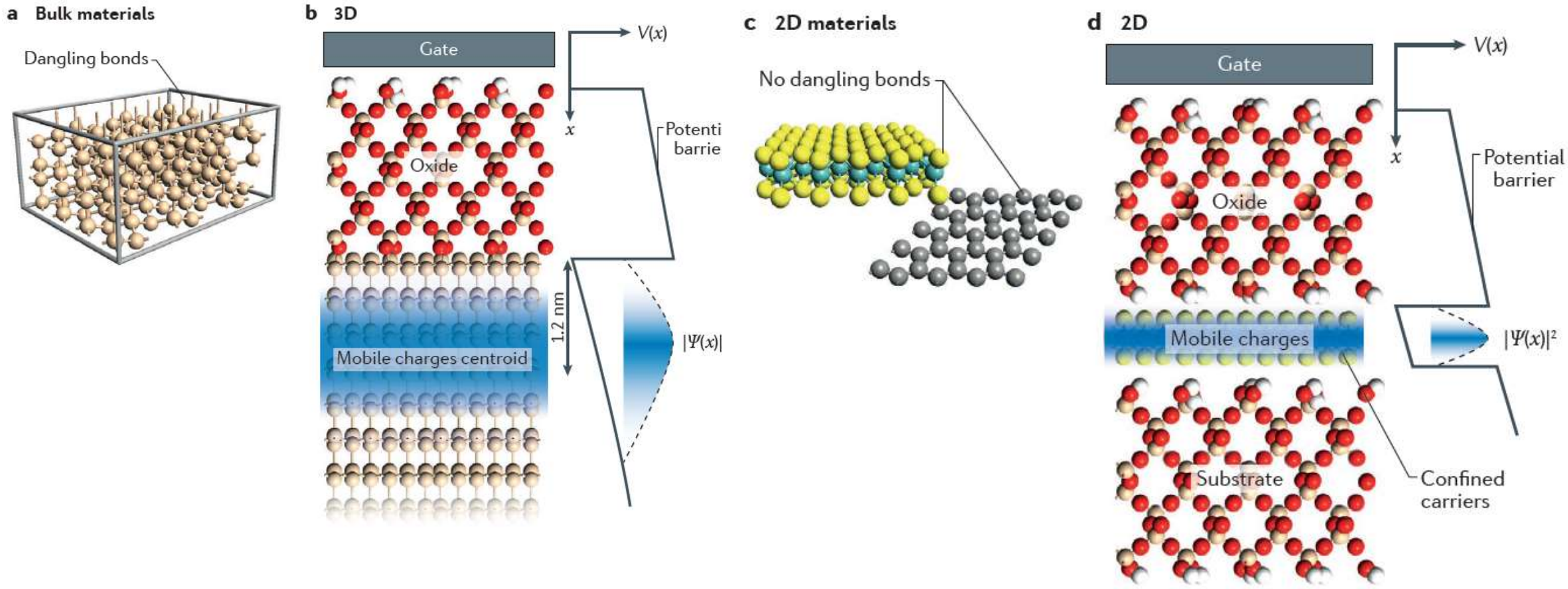
Outline

- 2D materials and devices
- NVMs
- CMOS characterization
- WBG
- 3D sensing

2D materials and devices

2D materials and devices

INTRODUCTION

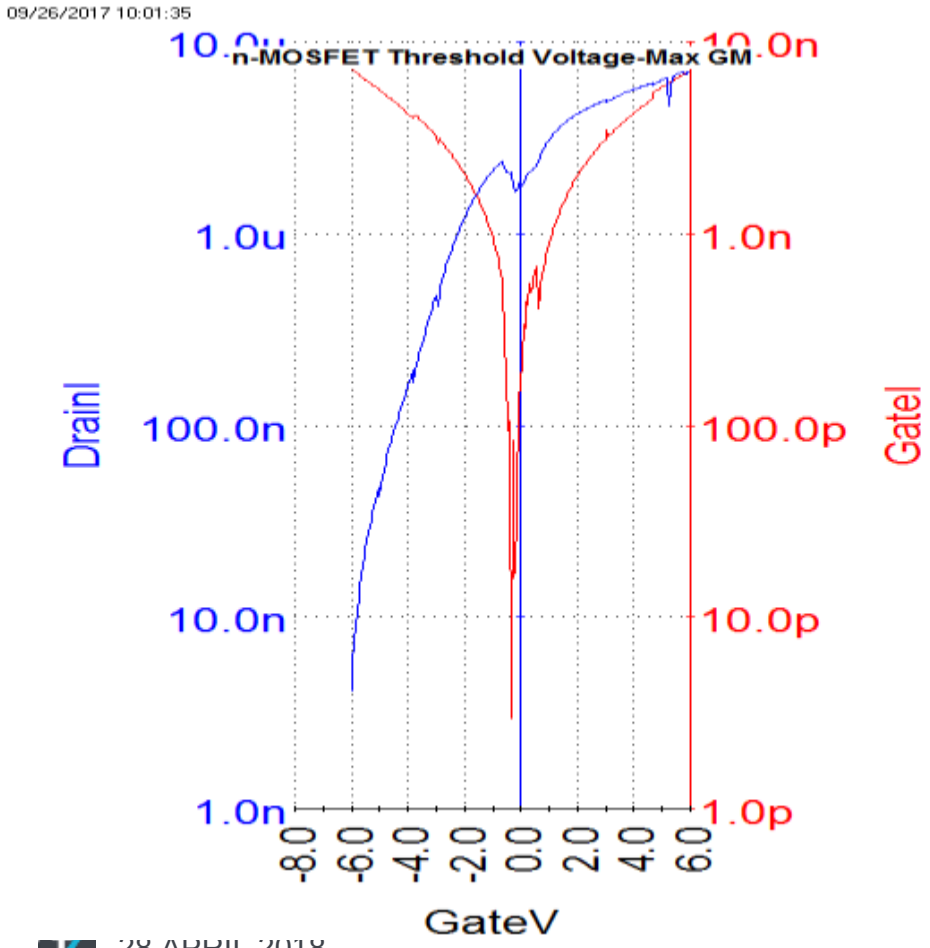


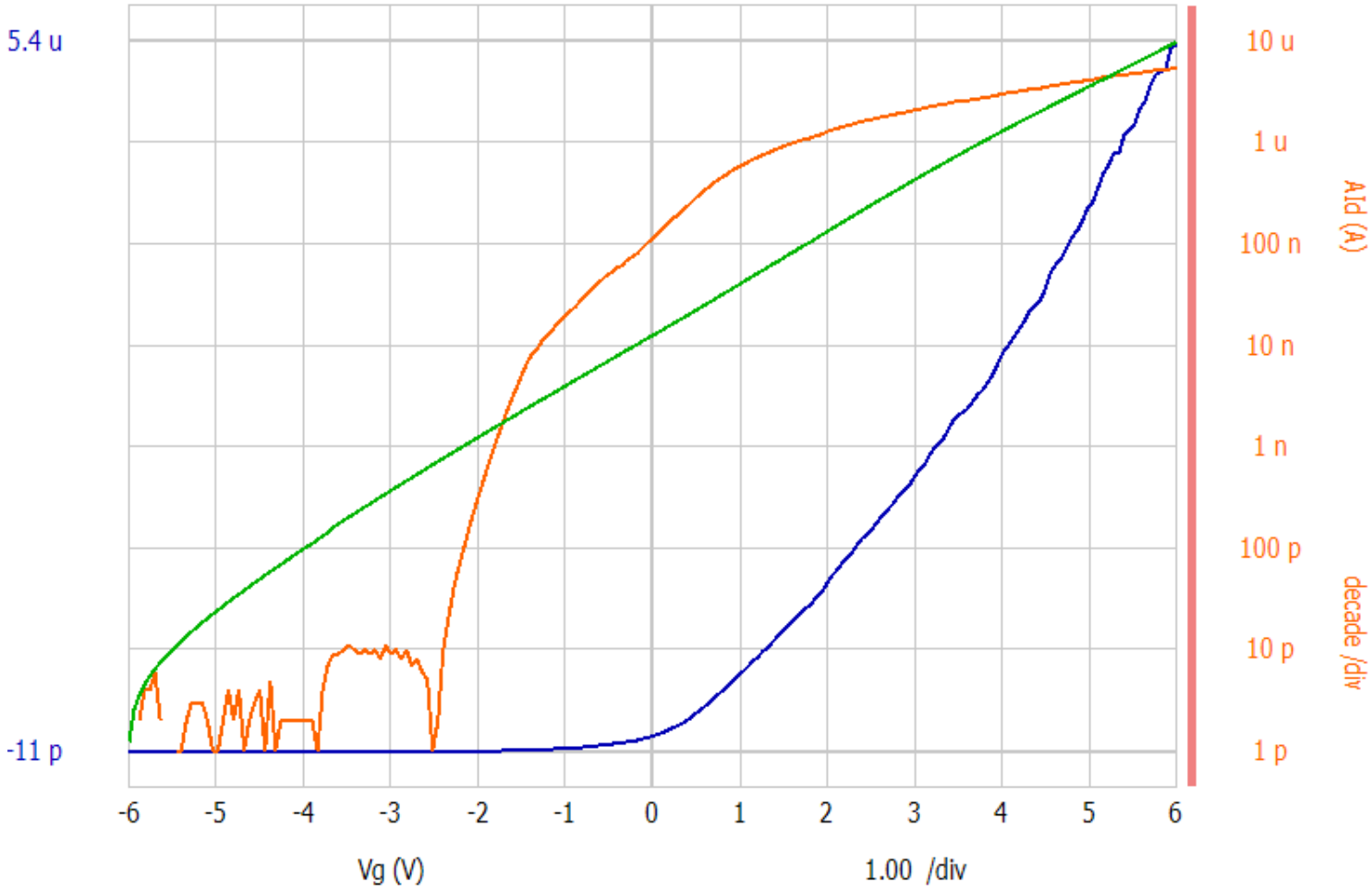
Two-dimensional semiconductors for transistors； Manish Chhowalla1,2, Debdeep Jena3,4 and Hua Zhang5； NATURE REVIEWS | MATERIALS

2D materials and devices

I-V TEST TECHNIQUE

- Which one is better?

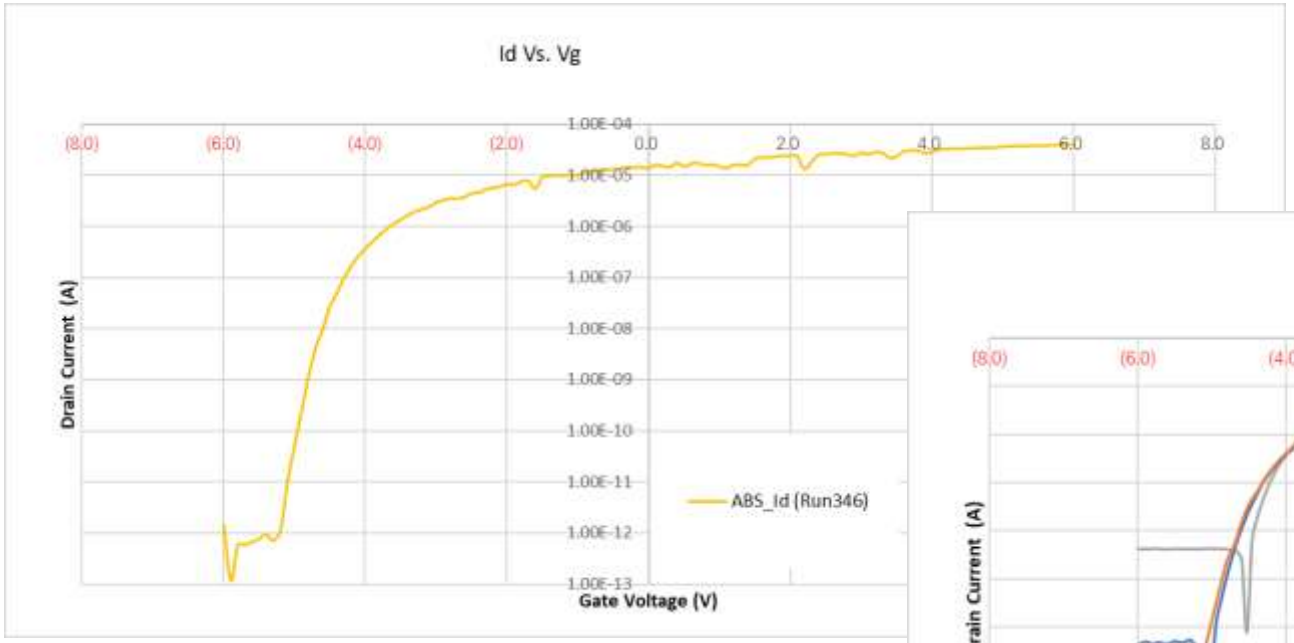


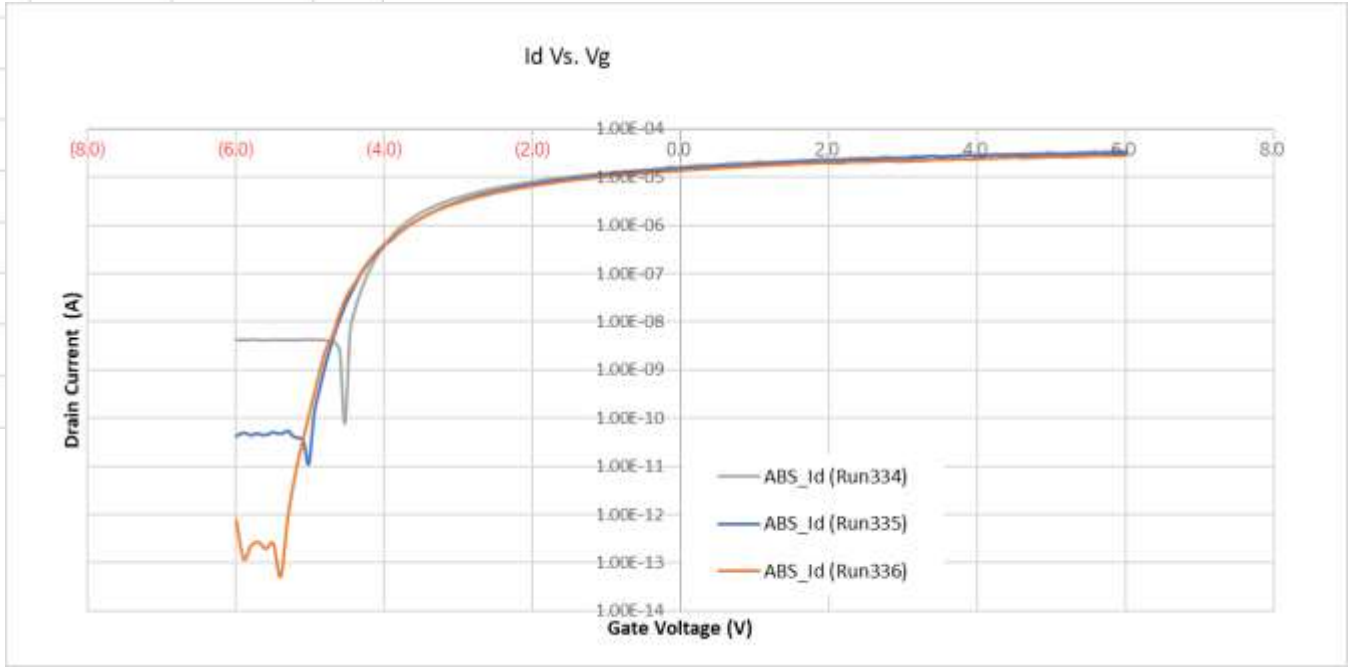


2D materials and devices

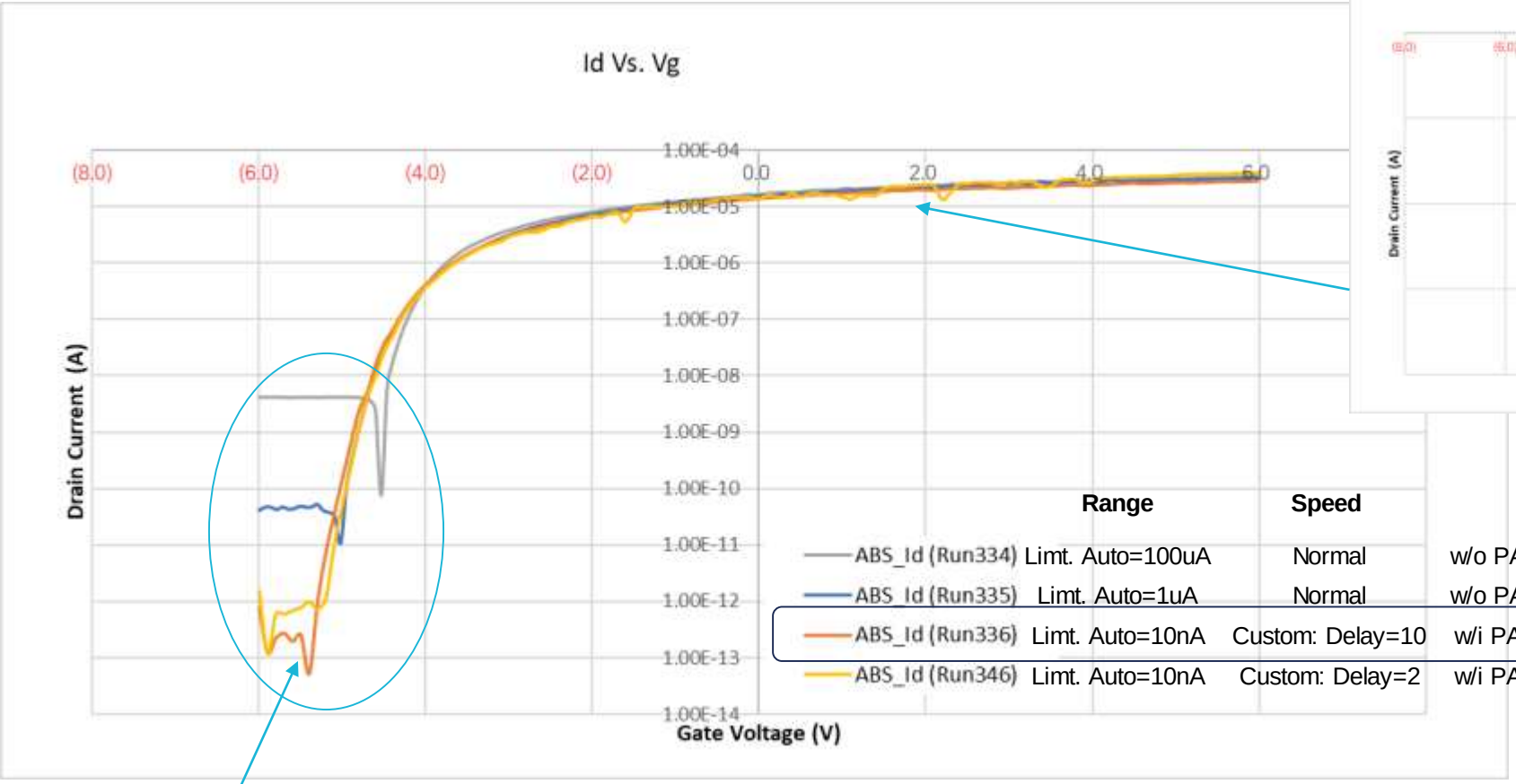
I-V TEST TECHNIQUE

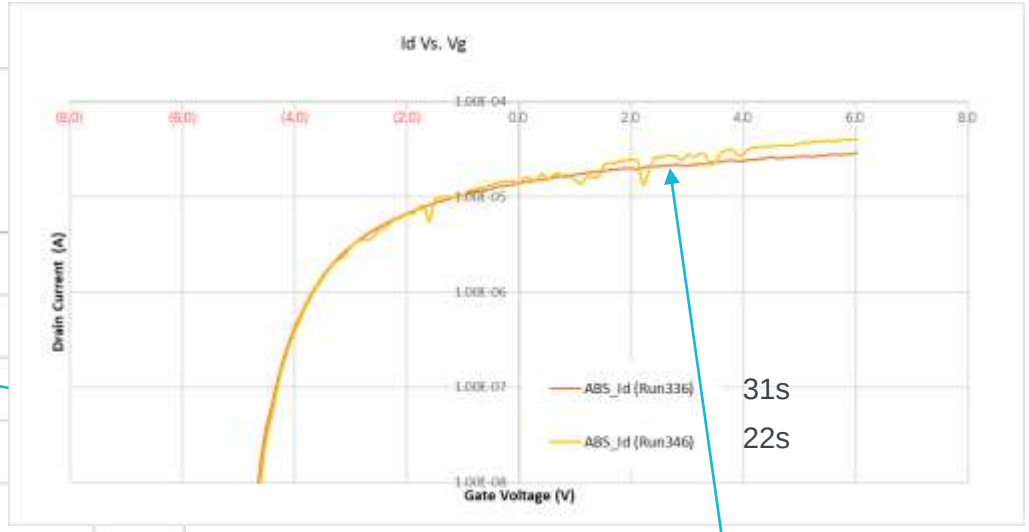
- Which one is better?





Data



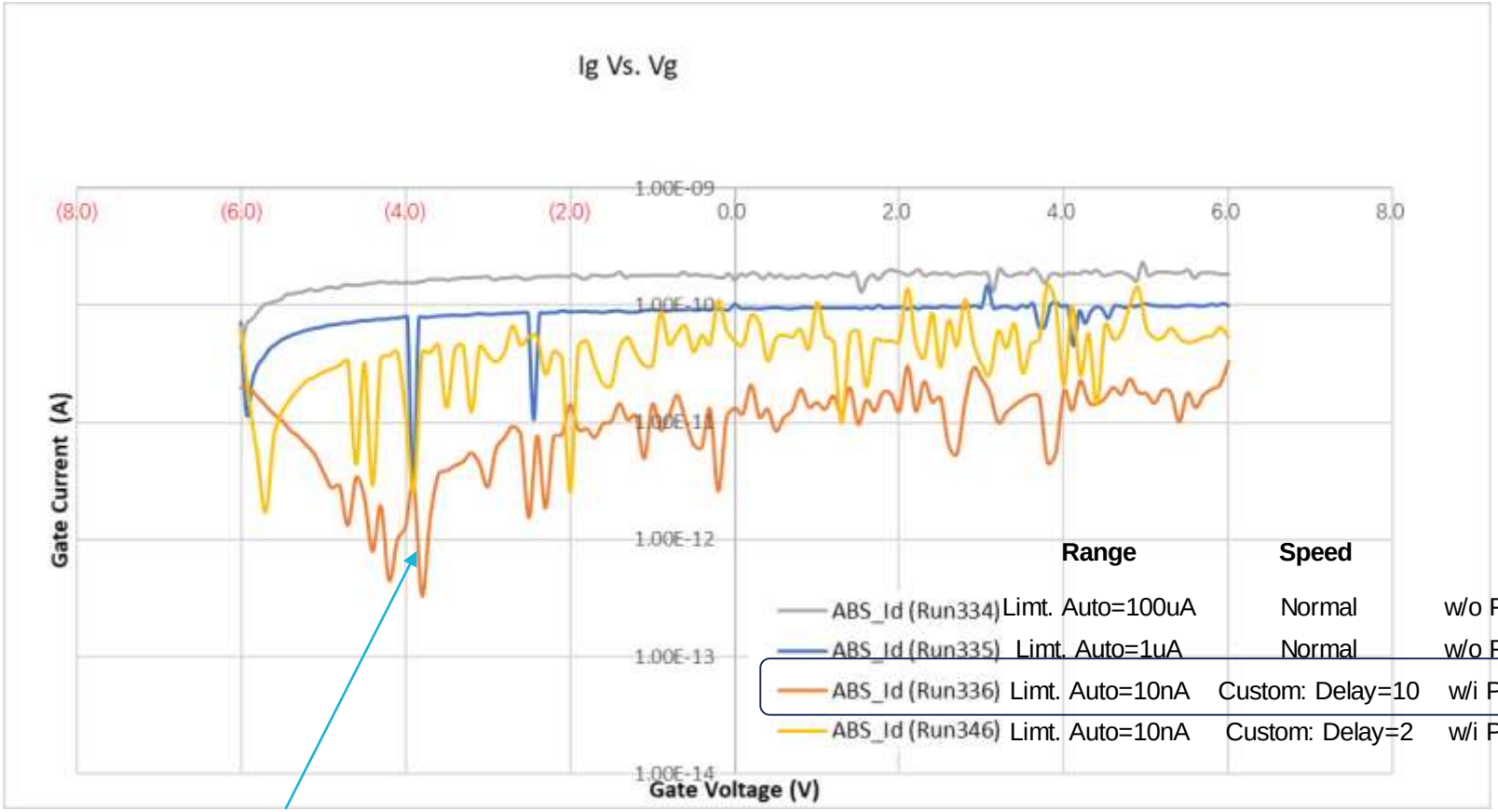


Delay factor should be bigger than 10, so that Drain current can be well settled. While, the test duration is not increased obviously.

Lowest Ioff as DUT it is.

Best test setting

Data



Lowest Ig as DUT it is.

Best test setting

2D materials and devices

I-V TEST TECHNIQUE

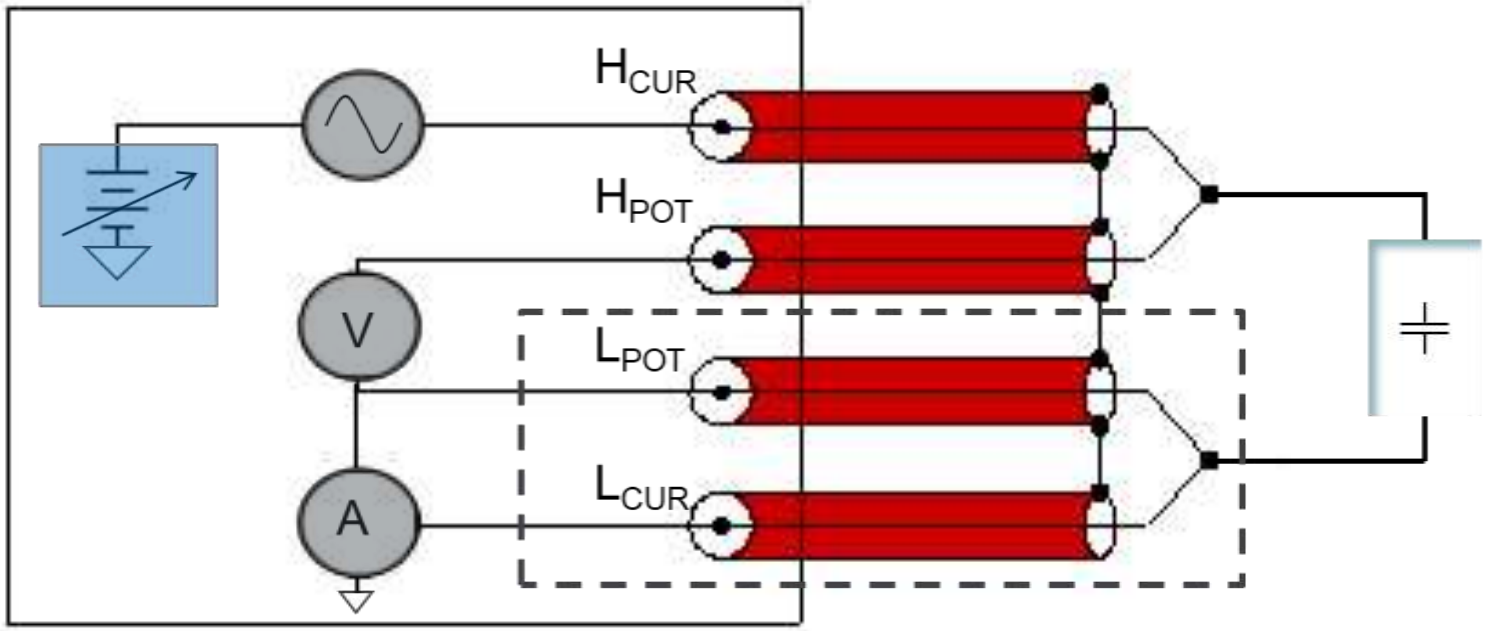
- What matters for IV test?

Range	• Reasonable Range Selection for specific I-V test
Delay	• Adjust the delay factor for “sharp” devices
Speed	• Balance between test speed and accuracy
Hardware	• Make sure there is no hi-leakage curr. and noise

2D materials and devices

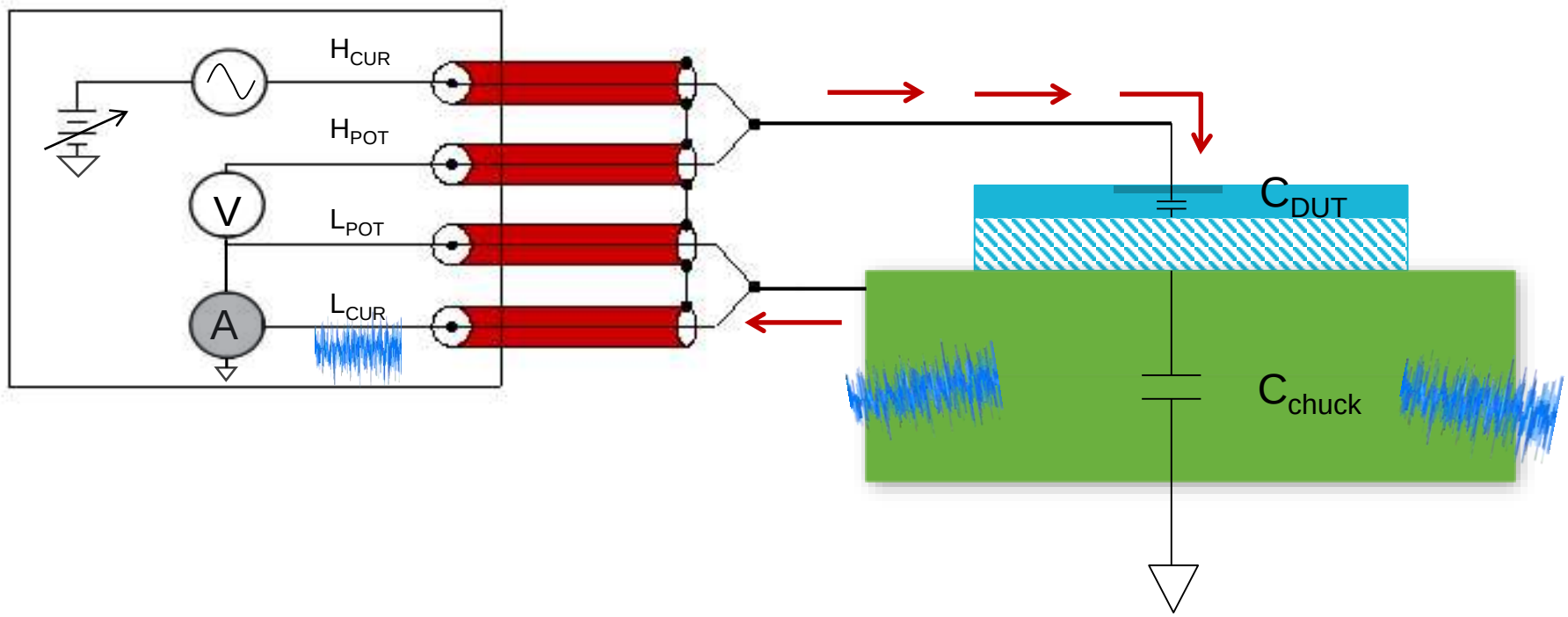
C-V TEST TECHNIQUE

Auto-balance Bridge with 4 Terminal Pair Configuration

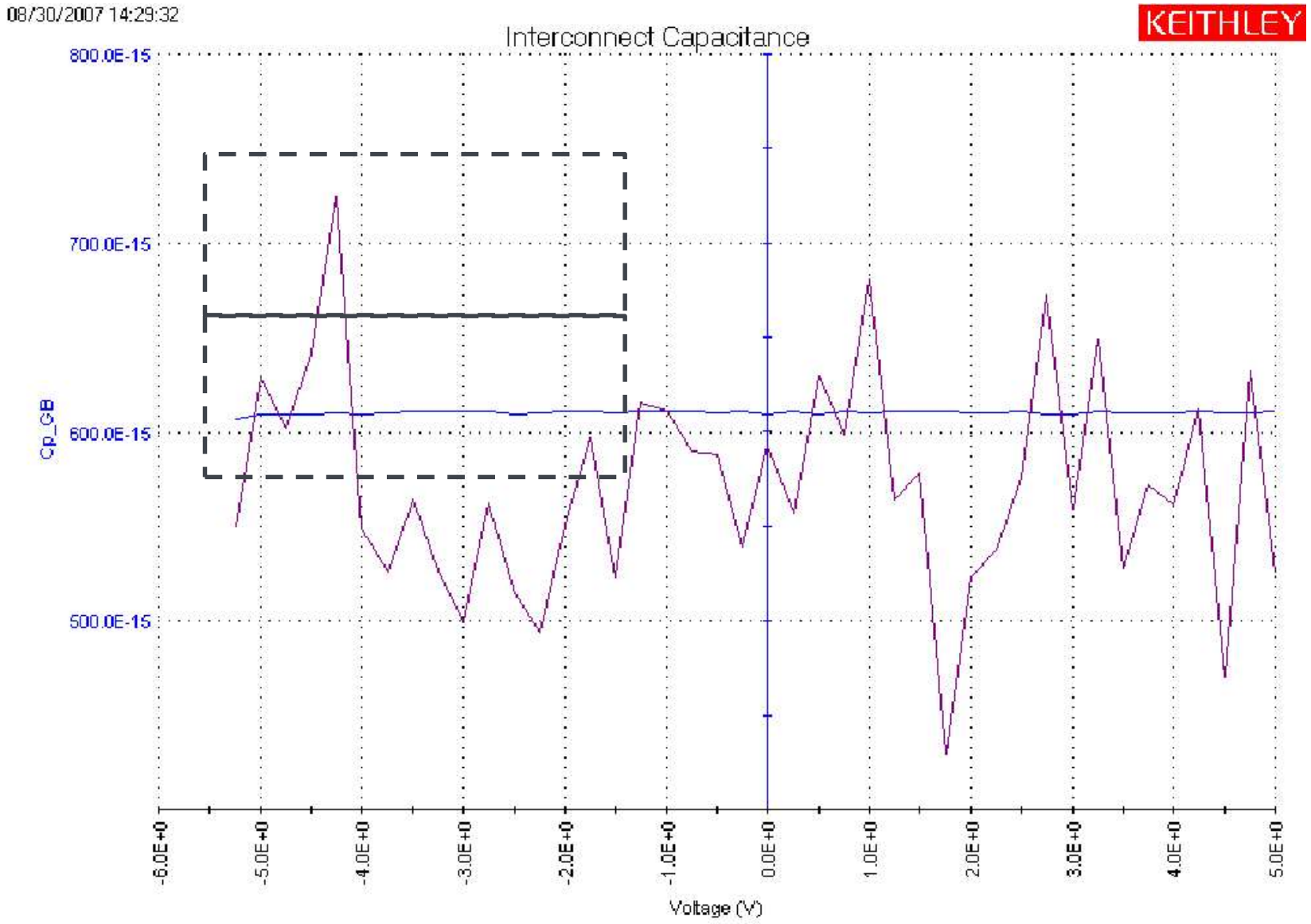


Measuring C on a Wafer and Probe Station

#1: Connect AC Ammeter to Least Noisy DUT Terminal



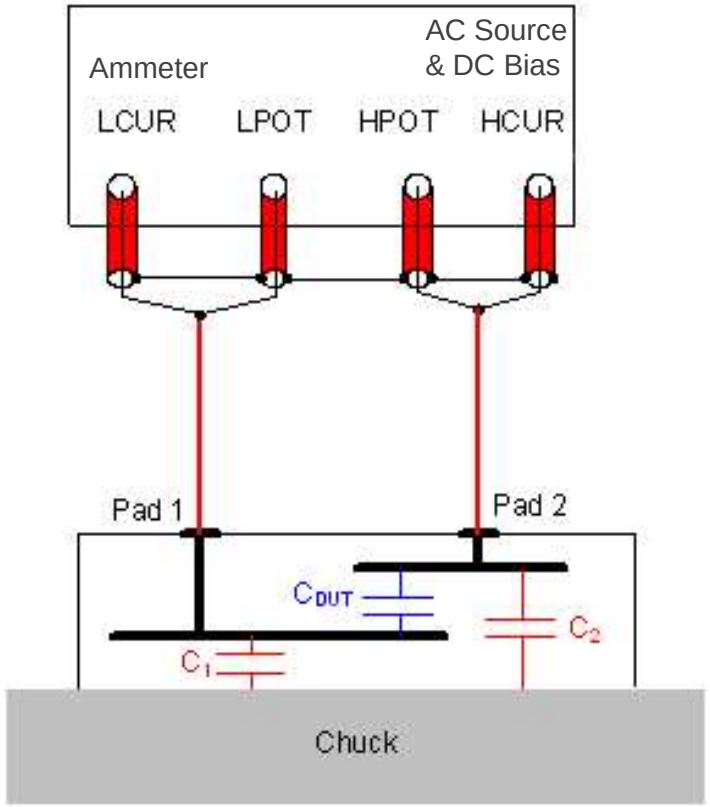
Exam



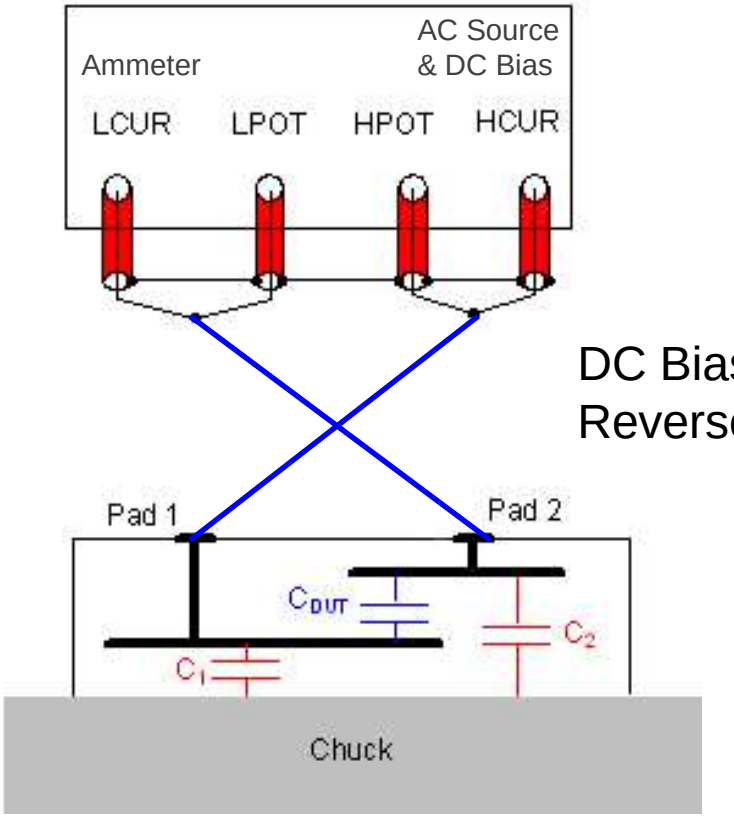
Data:Variables
Data:NOISE = 836.63e-18

Switch High and Lo Leads

Noisy measurement connection scheme

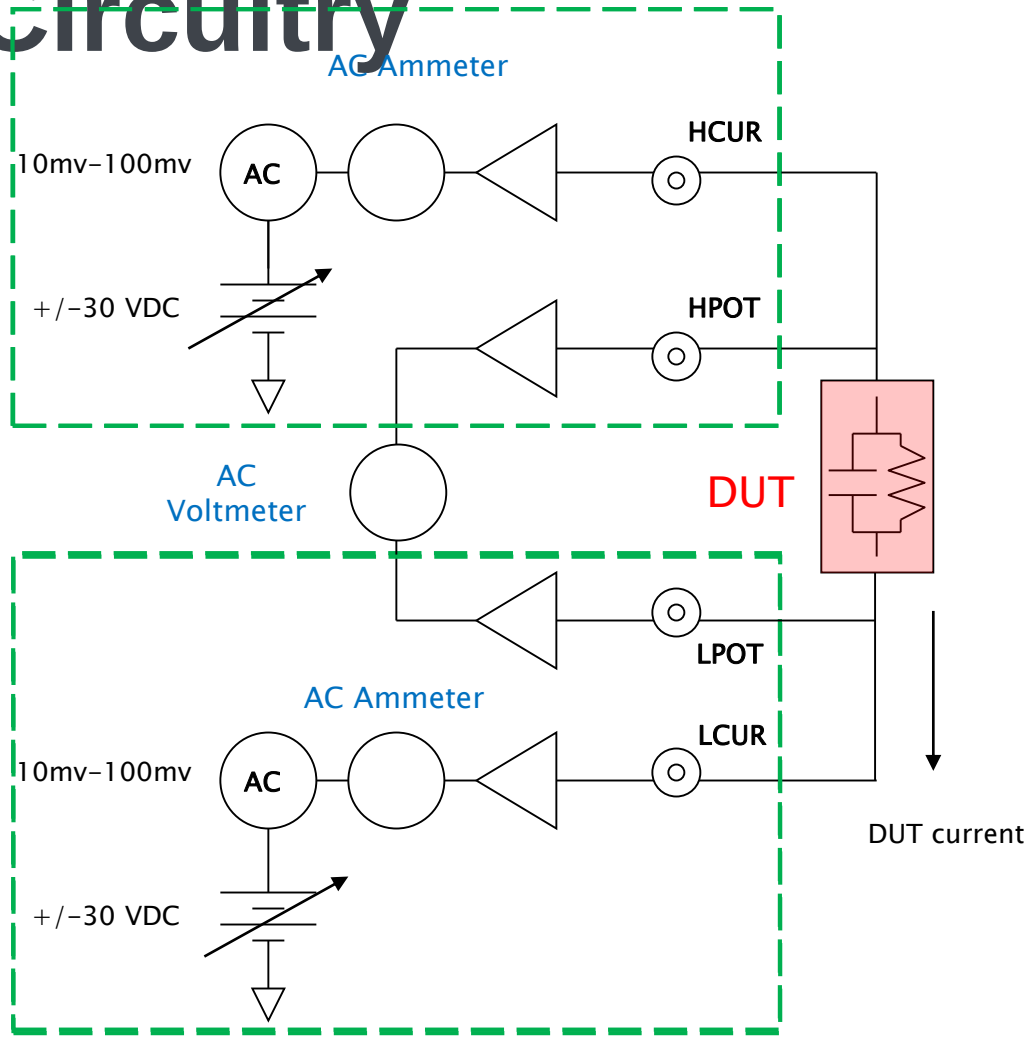


Terminal connections switched



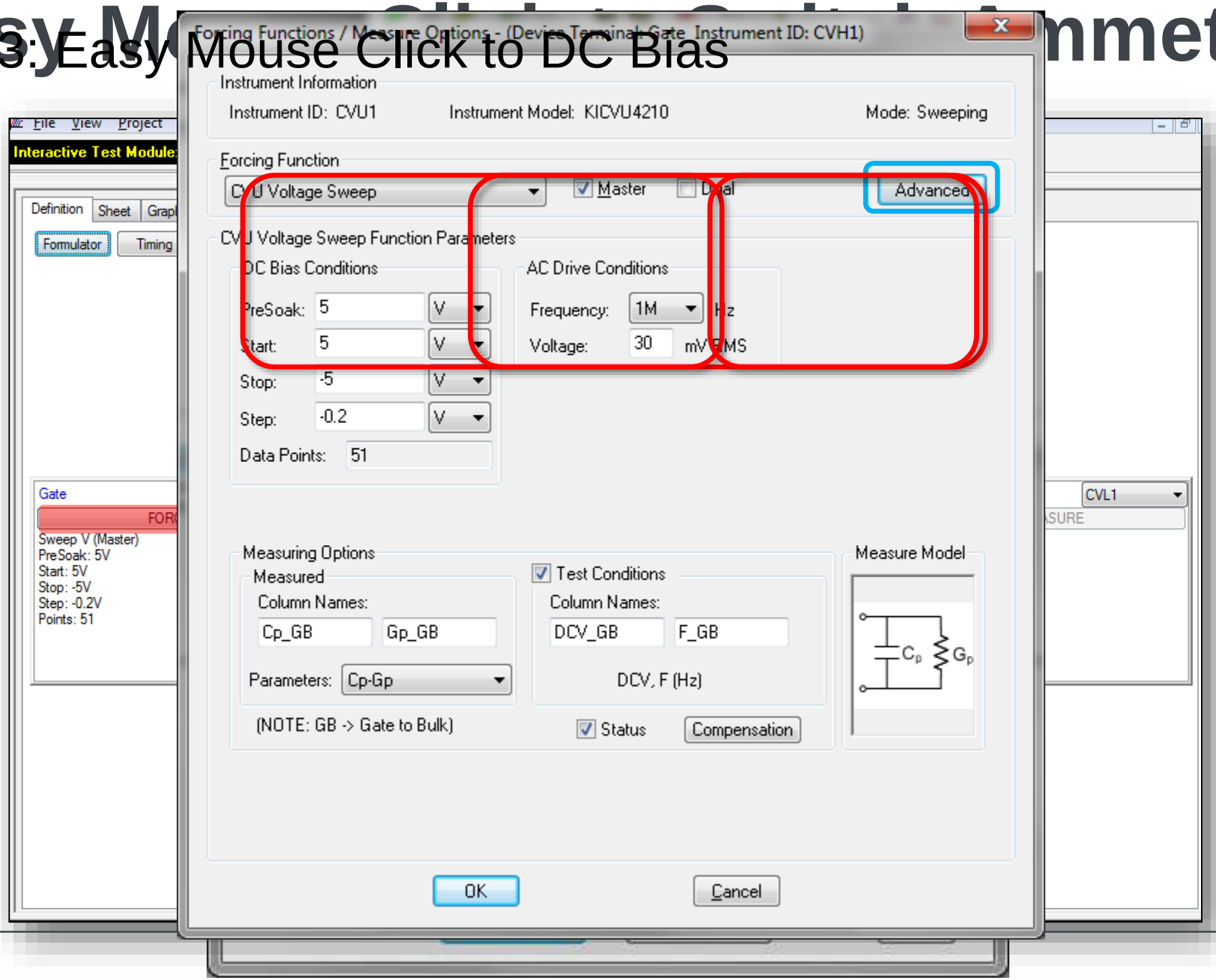
DC Bias Reversed!

Keithley Improved the C-V Meter with Symmetrical Circuitry

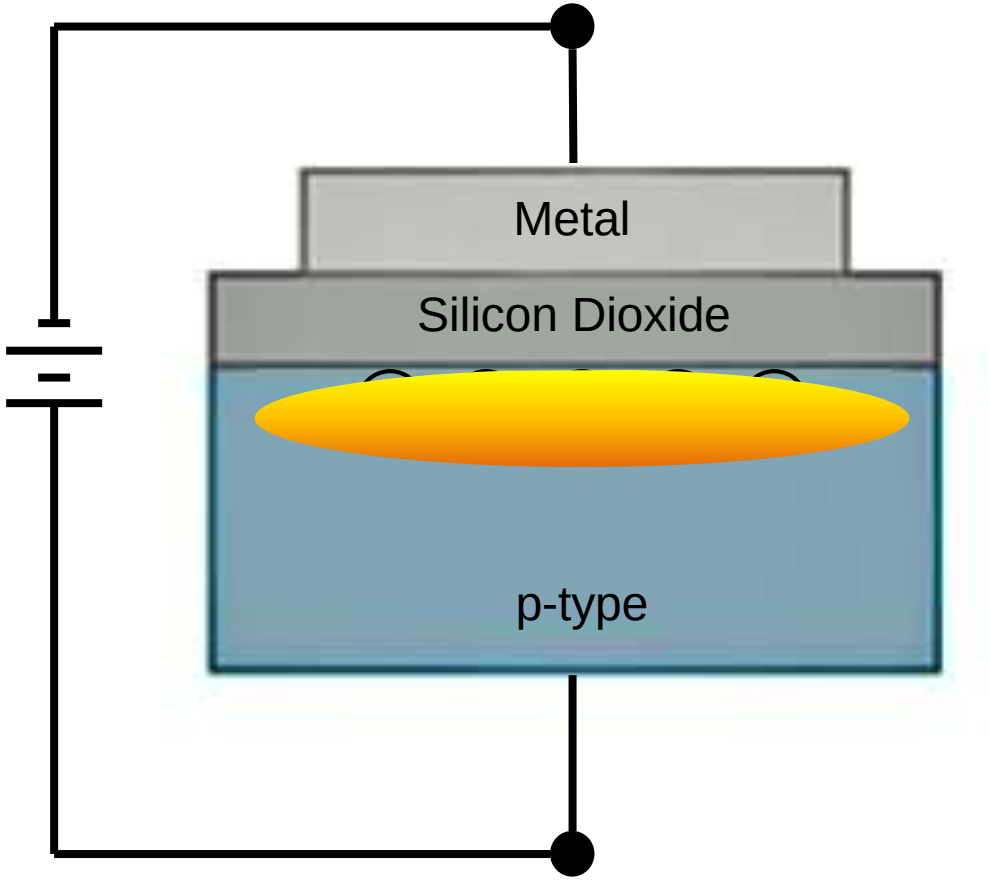


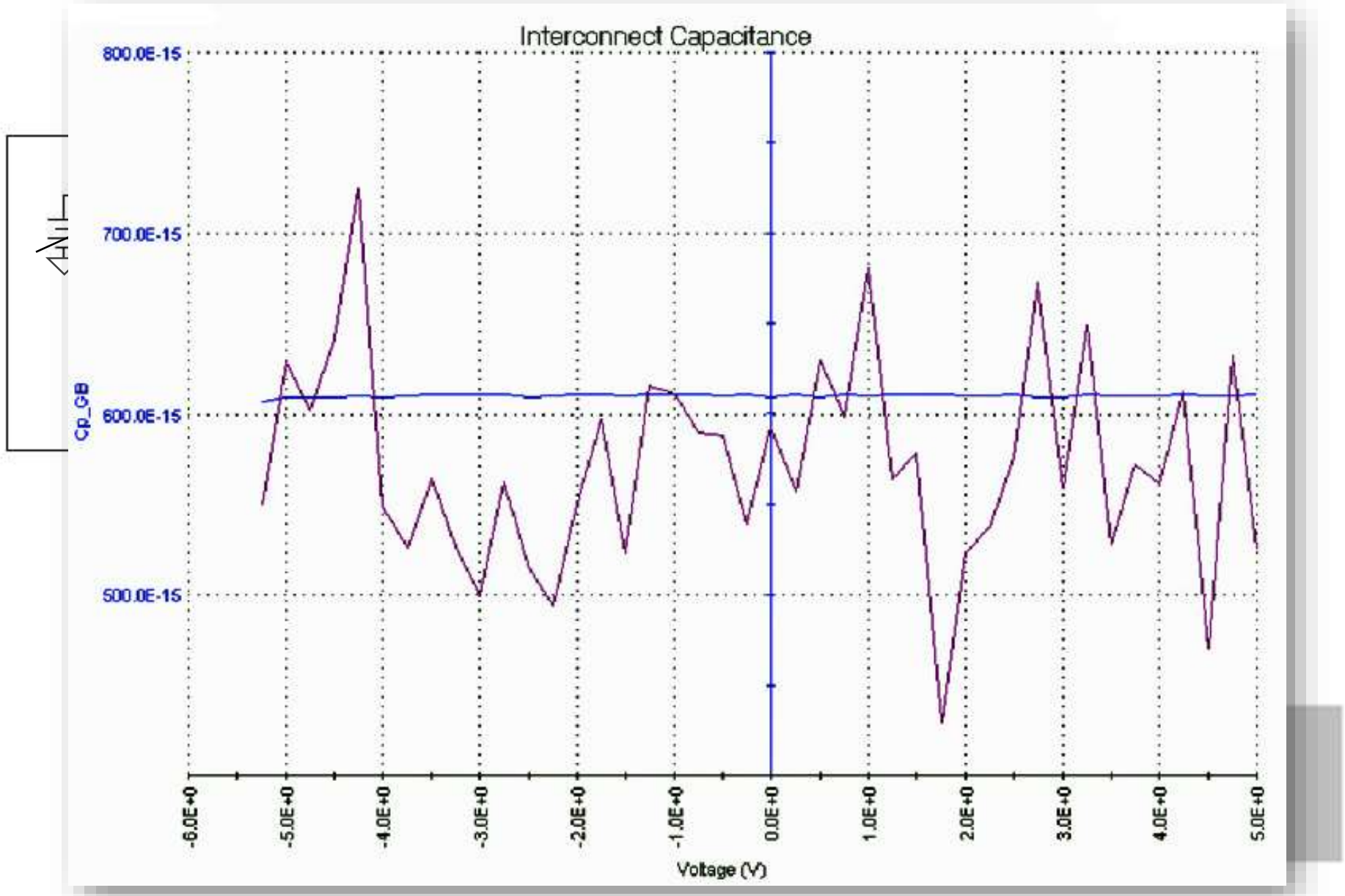
#2: Easy M… …mmeter

#3: Easy Mouse Click to DC Bias

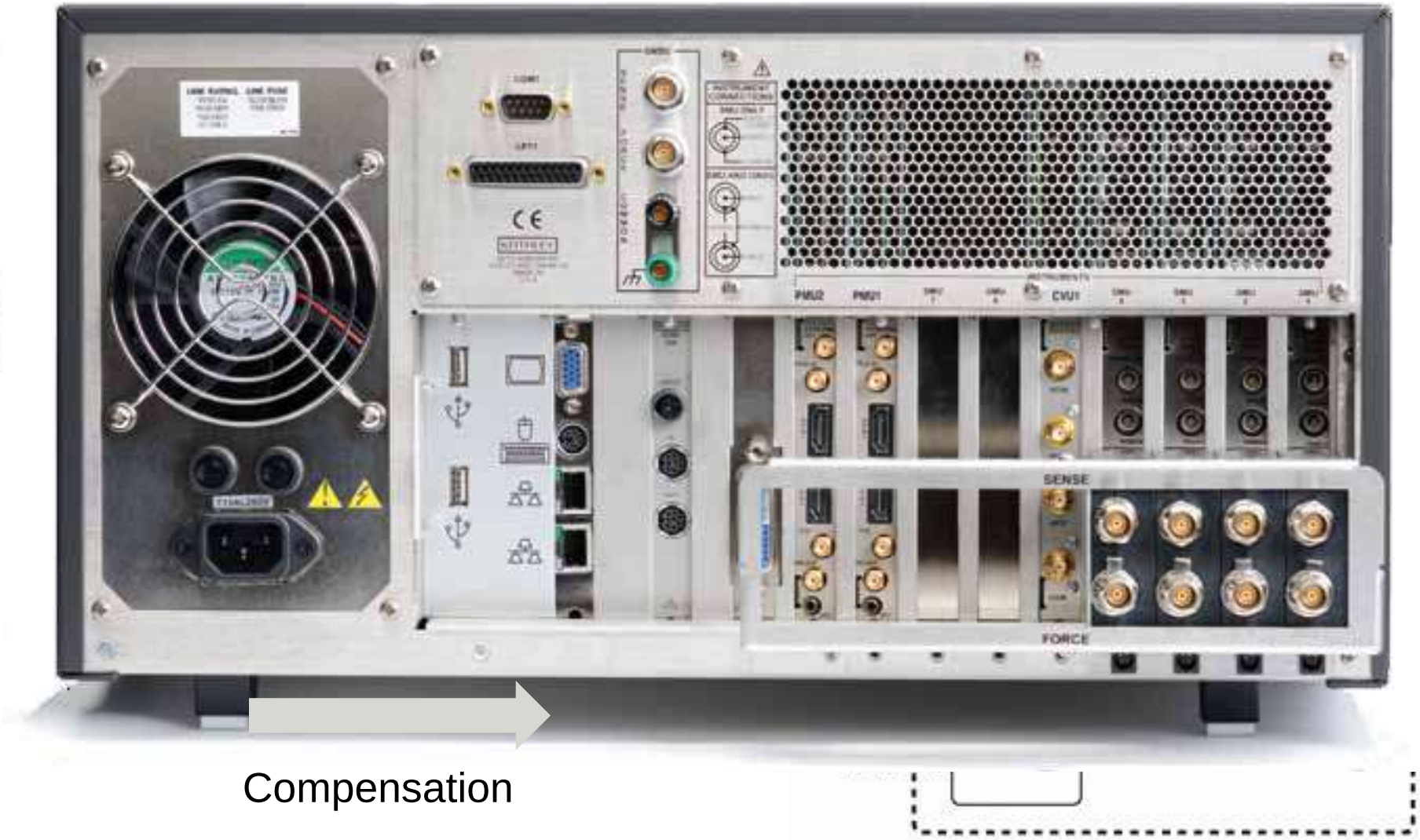


Control of DC Bias Provides Precise Control of Electric Field

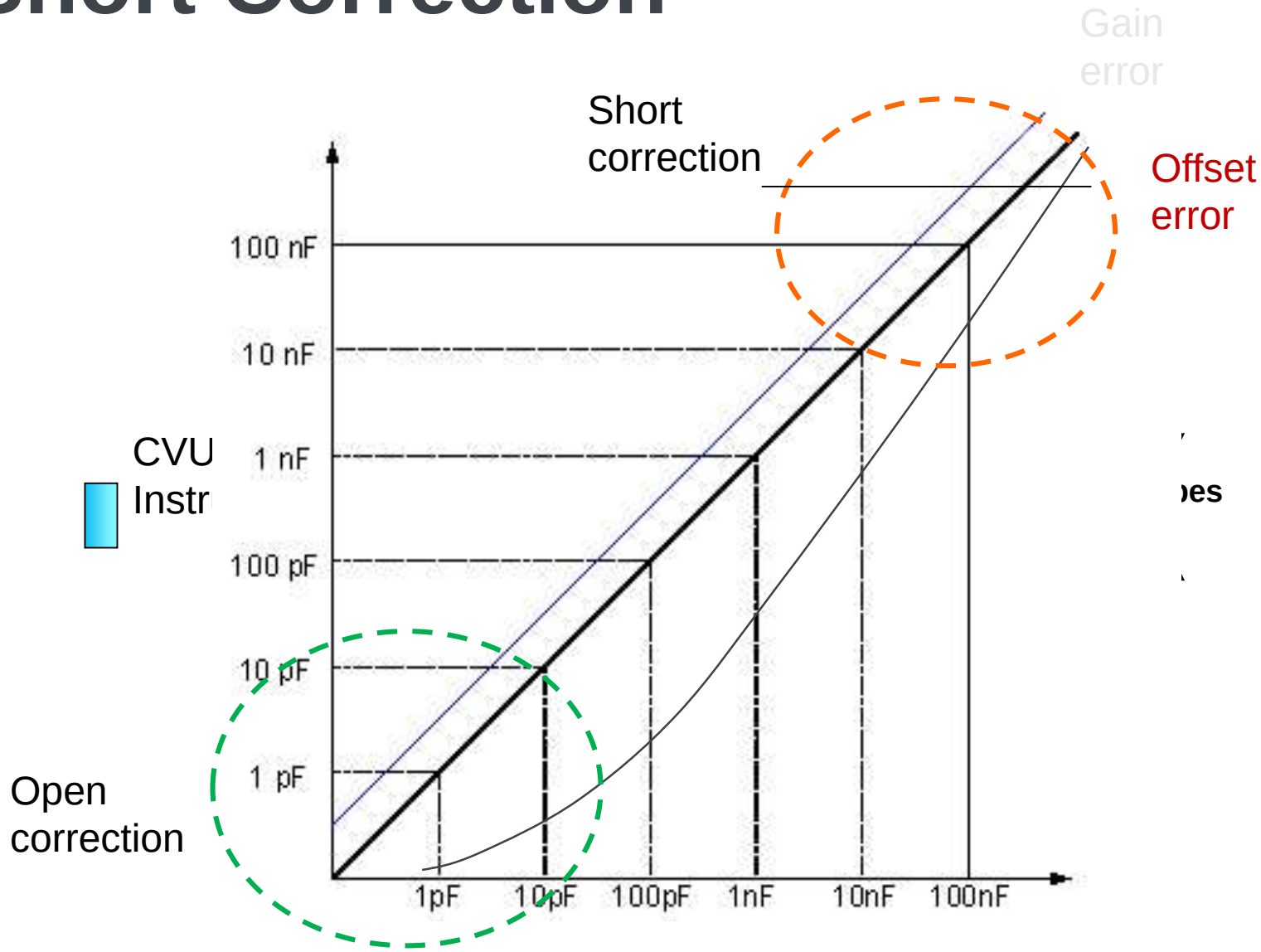



Interconnect Capacitance
800.0E-15
700.0E-15
600.0E-15
500.0E-15
Cp_GB
-6.0E+0
-5.0E+0
-4.0E+0
-3.0E+0
-2.0E+0
-1.0E+0
0.0E+0
1.0E+0
2.0E+0
3.0E+0
4.0E+0
5.0E+0
Voltage (V)

Confidence in Your Measurements

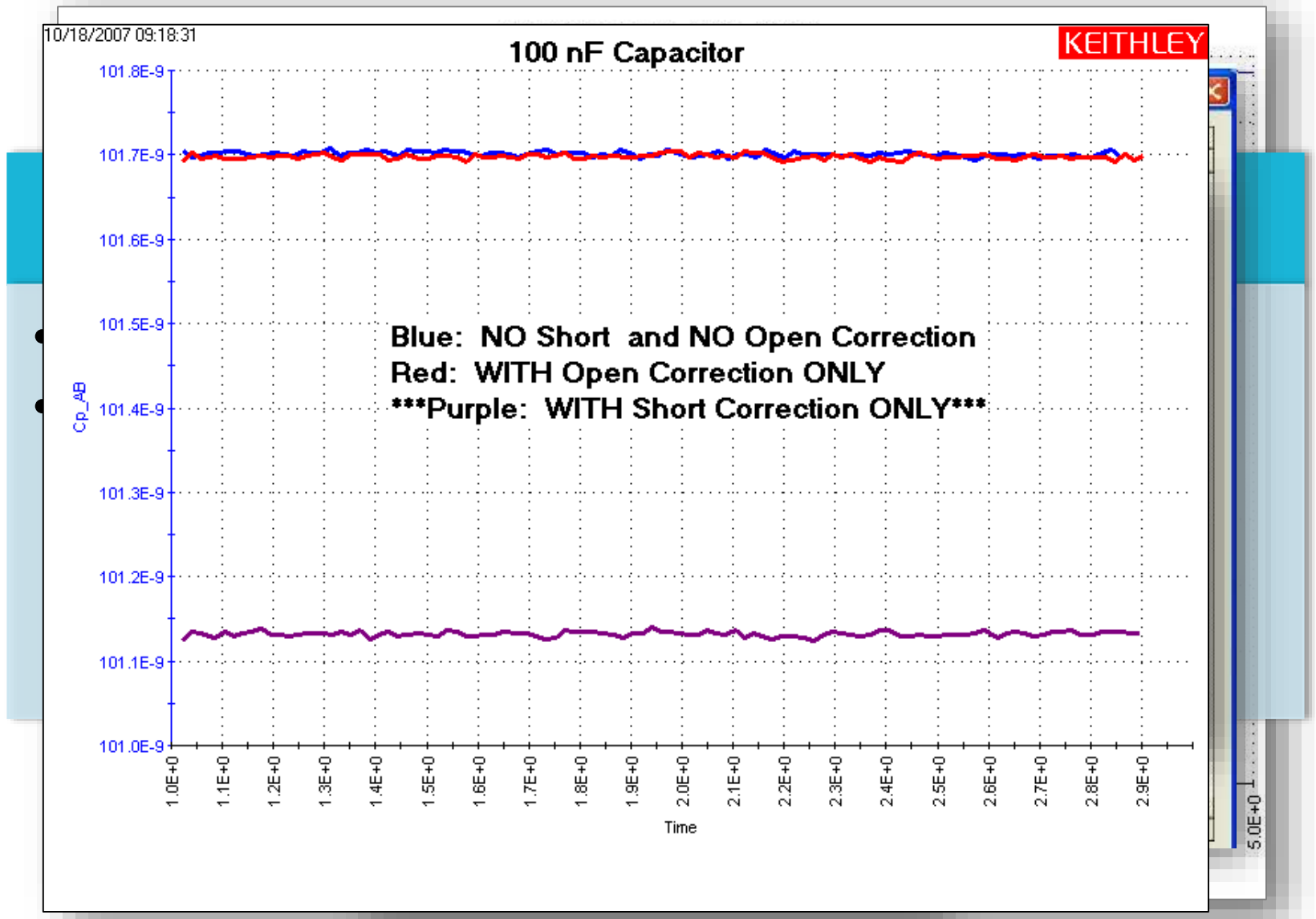


Open/Short Correction



CV Curve of MOSFET

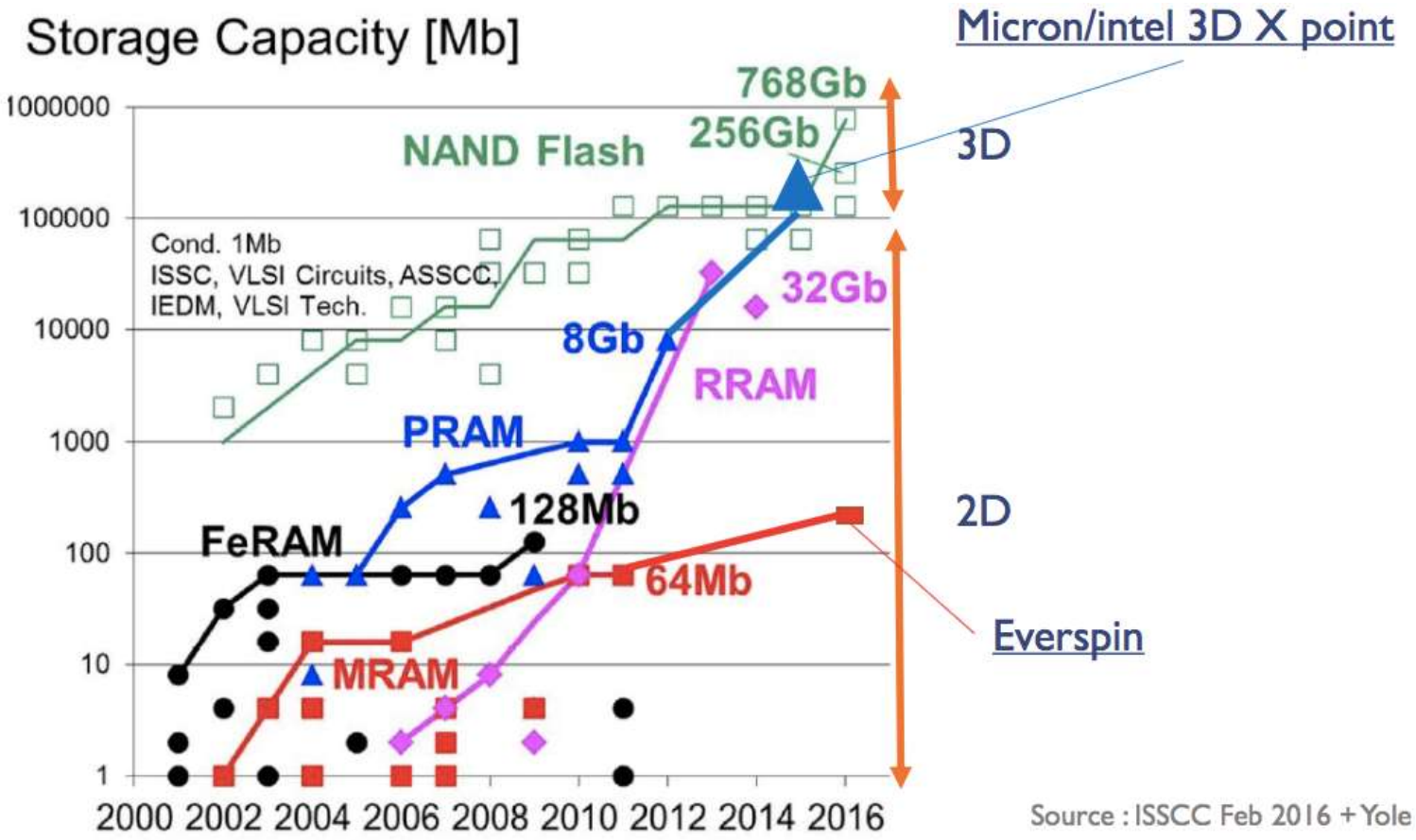
General Rule of Thumb



Confidence Check

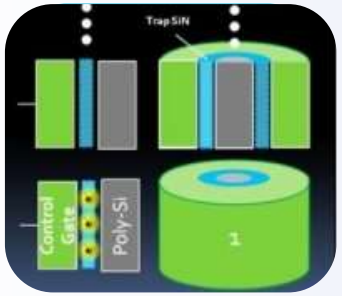
Memory → NVM

Memory: Where are we now



3D X point :

128 Gb chip, a density comparable to NAND, has been directly commercially presented (instead of R&D paper) by Micron/Intel in July 2015 in order keep the technology secret until the last moment.



3D NAND Flash:

15.3 TB single disk is purchasable (released in 2016). Till now, it is the most leading applied memory in the consuming market.

Source: Yole

A few key points about Memory

Speed:

Write/erase/ time should be less than 1ns for single cell operation. (Together with I/O design)

Capacity / Size

Single cell size should be as small as possible, ensure the capability for ultra-mass data/information storage.

Power consumption

Lower operating voltage and leakage current to reduce the power consumption

Cost

Industrially process developing to decrease the cost of production (both for material and tools).

Memory: NVM performance between 2014 and 2016

	Emerging Memory			Established Memory		
2014	**STTMRAM**	**PCM**	**RRAM**	**SRAM**	**DRAM**	**Flash NAND**
Non-Volatile	YES	YES	YES	NO	NO	YES
Endurance (Nb cycles)	High (10^{12})	Medium (10^{8})	Low (10^{6})	High (10^{15})	High (10^{15})	Low (10^{5})
2014 latest technological node produced (nm)	90 nm	45 nm	130 nm	10 nm	30 nm	15 nm
Cell size (cell size in F^2)	Medium (6-12)	Medium (6-12)	Medium (6-12)	Very large (150)	Small (6-10)	Very small (4)
Write speed (ns)	High (10 ns)	Medium (75 ns)	High (20 ns)	High (5-10 ns)	High (10 ns)	Low (10,000 ns)
Power consumption	Medium/low	Medium	Low	Very low	Low	Very high
2014 price ($/Gb)	High ($100-$50/Gb)	Medium (few $/Gb)	Very High ($5,000/Gb)	Low ($1/Gb)	Low ($1/Gb)	Very low ($0.05/Gb)
Suppliers	Everspin	Micron, Samsung	Adesto	Qualcomm, Intel	Samsung, Micron, SK Hynix	Samsung, Micron, Toshiba, SK Hynix

40nm 20nm 1nm

50~100ns 20~250ns

$3000~200/GB $100/GB

In the coming a few years, vast applications will be completely different due to the continues rapid developing of the NVM tech.

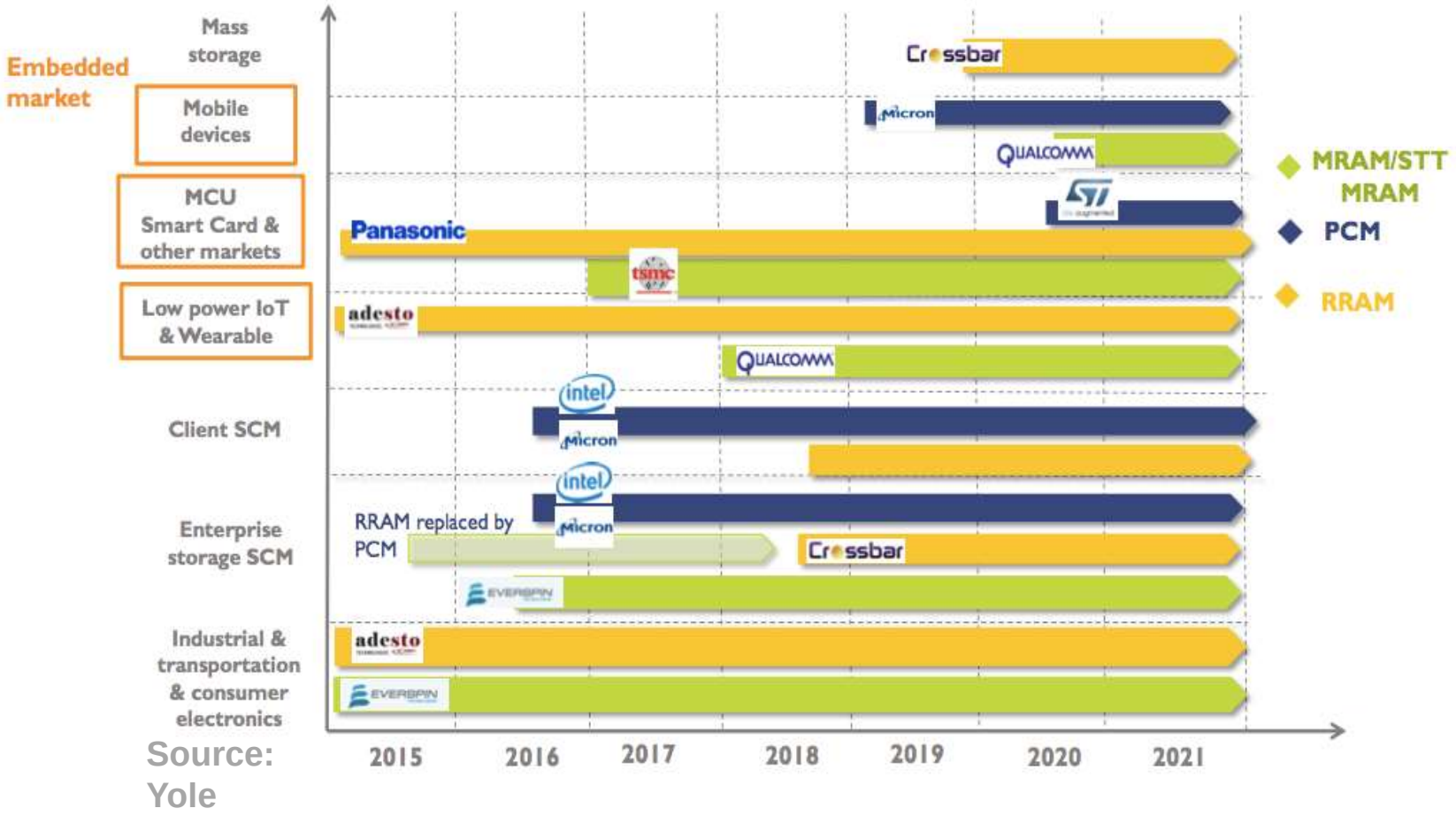
	Emerging Memory			Established Memory	
2016	**STTMRAM**	**PCMS "3D Xpoint"**	**RRAM**	**DRAM**	**Flash NAND**
Non-Volatile	YES	YES	YES	NO	YES
Endurance (Nb cycles)	High (10^{12})	Medium (10^{8})	Low (10^{6})	High (10^{15})	Low (10^{5})
2016 latest technological node produced (nm)	40 nm	20 nm	130 nm	1X nm	15 nm
Cell size (cell size in F^2)	Medium (6-12)	?	Medium (6-12)	Small (6-10)	Very small (4)
Read latency (ns)	Fast (10-20 ns)	Fast (50-100 ns)	Medium (250 ns)	Very fast (few ns)	Slow (100,000 ns)
Power consumption	Medium (50 pJ/bit)	Medium	Medium (6nJ/bit)	Low	Very high
2016 price ($/Gb)	High ($3000-$200/Gb)	Low ($ < 0.5/Gb)	High ($100/Gb)	Low (< $1/Gb)	Very low ($< 0.05/Gb)
Suppliers	Everspin	Micron/Intel	Adesto	Samsung, Micron, SK Hynix	Samsung, Micron, Toshiba, SK Hynix, Intel

The new emerging NVM technology has changing in:
Cell size, Speed and Cost.

Source: Yole*

These performance is all for commercial products and stand alone

Memory: The future market



Source: Yole

Measuring the 6th Wave

Emerging NVM market:

This whole market is just start to develop. No product available until 2015. Estimated : 2017:500M$ → 2021:4500M $

Promising emerging NVM:

Future mainstream technology is still to be chosen by the practical application. But there are two of them which considered as the most promising emerging NVM.

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Memory: Two promising emerging NVM:

Measuring the 6th Wave

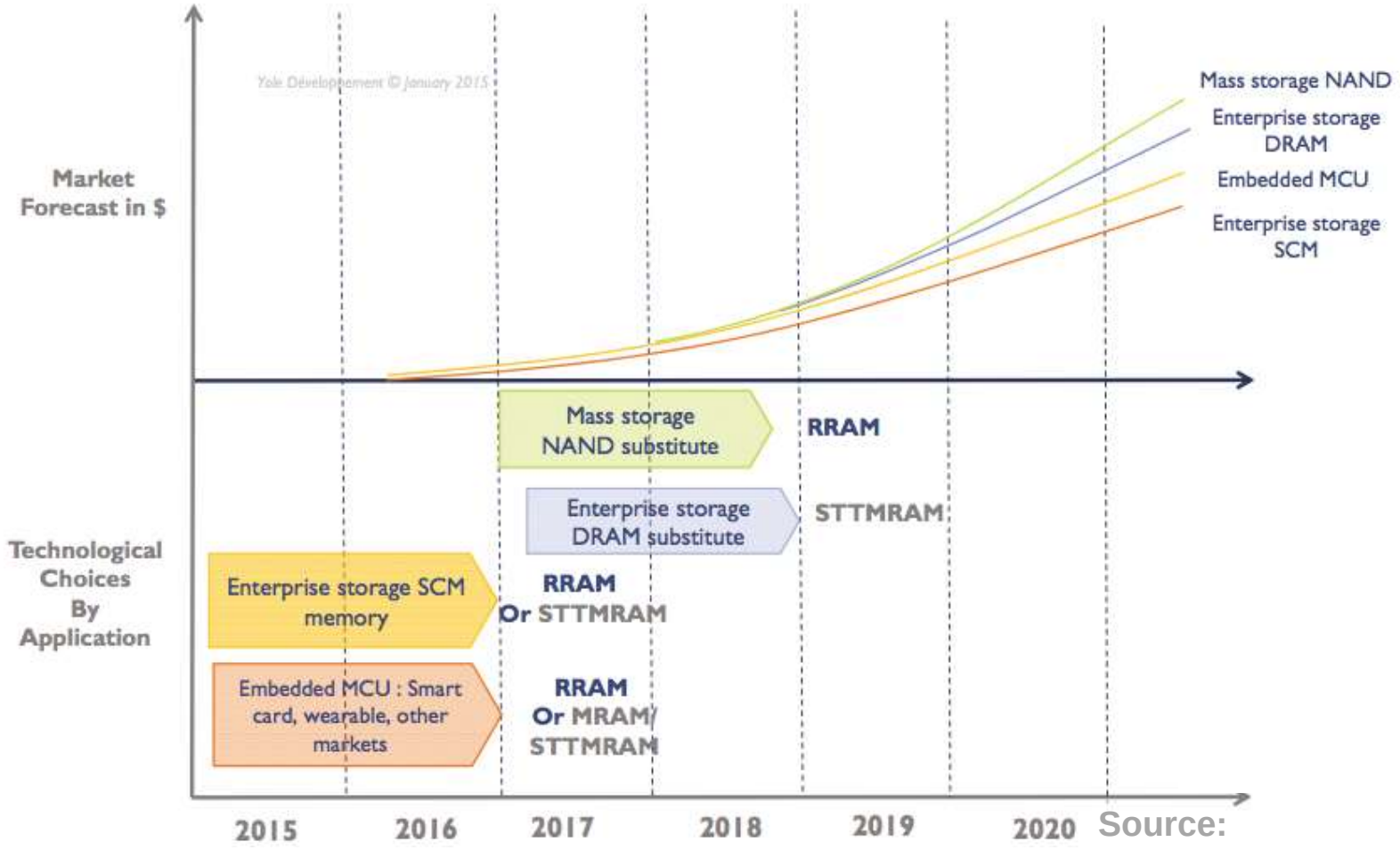
Mass storage

Mass storage purpose Memory and MCU may adopt new emerging NVM firstly within a few years.

Replacement

If the characteristics are confirmed and cost will not a problem, the new emerging NVM may replace SRAM/DRAM

The most promising 2 types of emerging NVM are RRAM ad MRAM



Source: Yole

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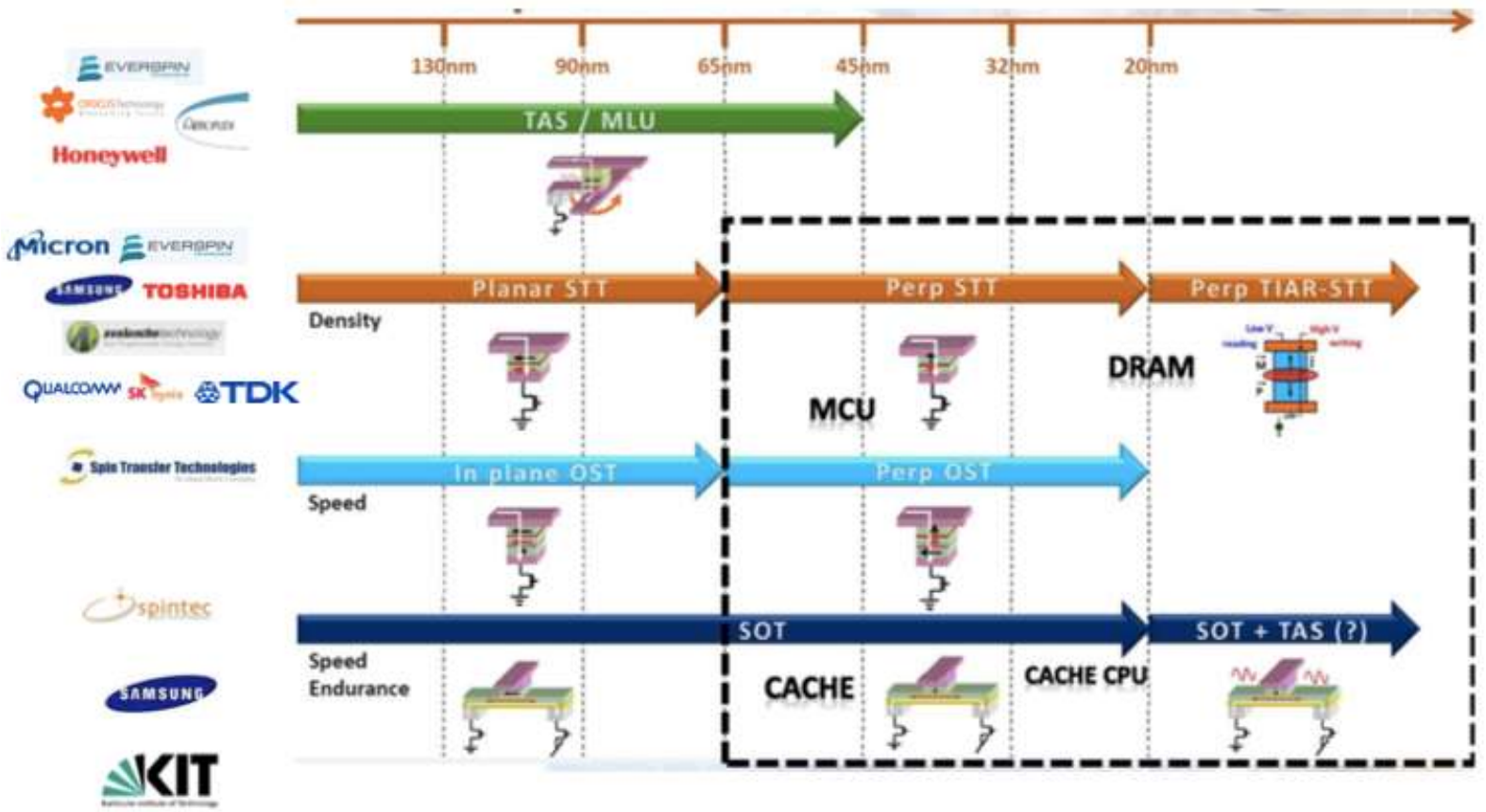
Memory: Two promising emerging NVM:

Measuring the 6th Wave

MRAM AND STTMRAM TECHNOLOGIES

Development status: production for low density, R&D for high density and embedded memory

MRAM market is dominated by Everspin (since 2006), which commercialized the first STTMRAM 64 Mb samples in Nov 2012 and 256 Mb in 2016 with two years delay. Avalanche also introduced with two years delay its 64 Mb product in 2016.



Source :
Spintec June. 2014

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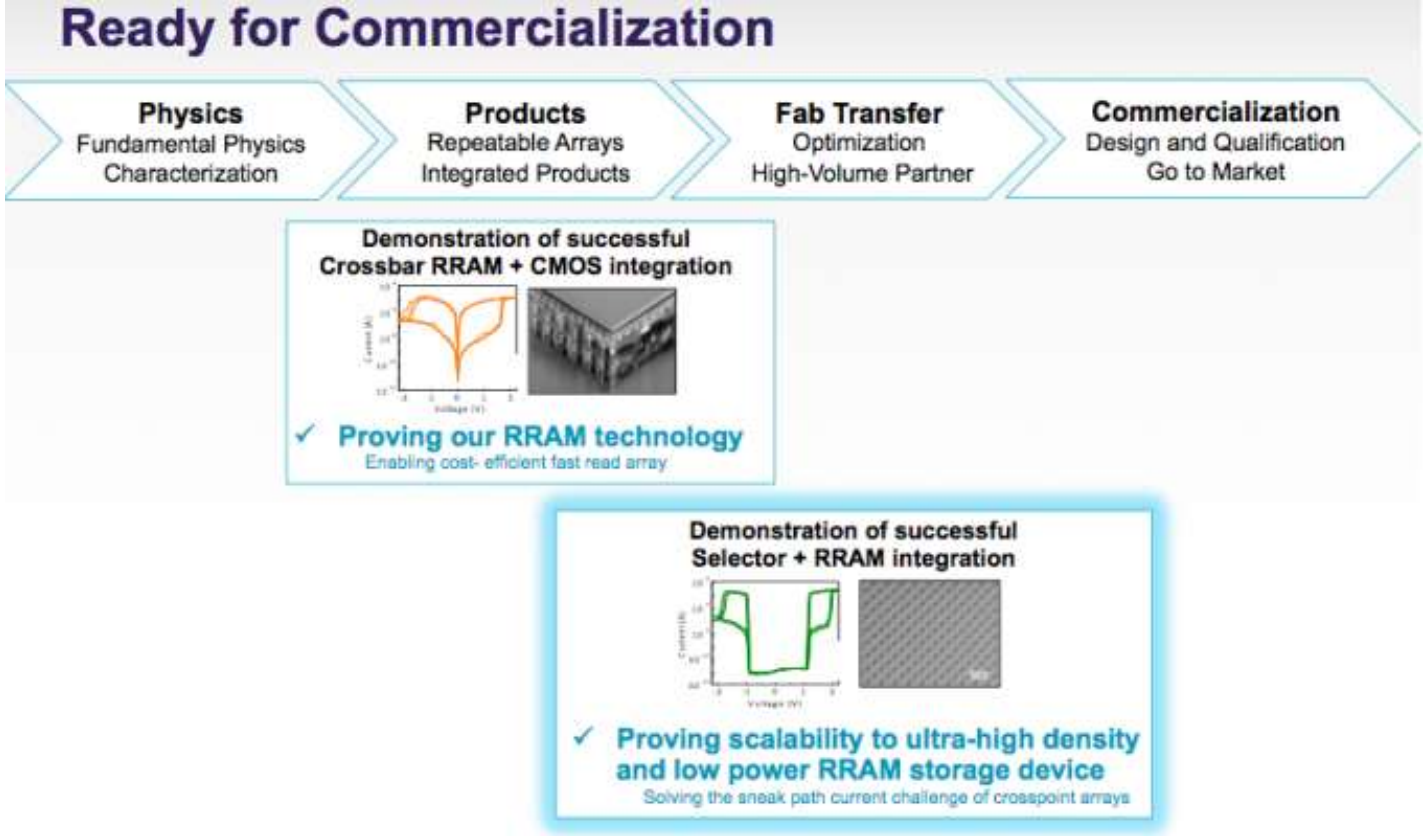
Memory: Two promising emerging NVM:

Measuring the 6th Wave

RRAM TECHNOLOGIES

Development status: Stand-Alone devices : maximum chip density available

Main milestones will be 2018 for SCM enterprise storage with a lower pricing than 3D X point competitor and then, 2020 to compete with NAND



Source: Crossbar

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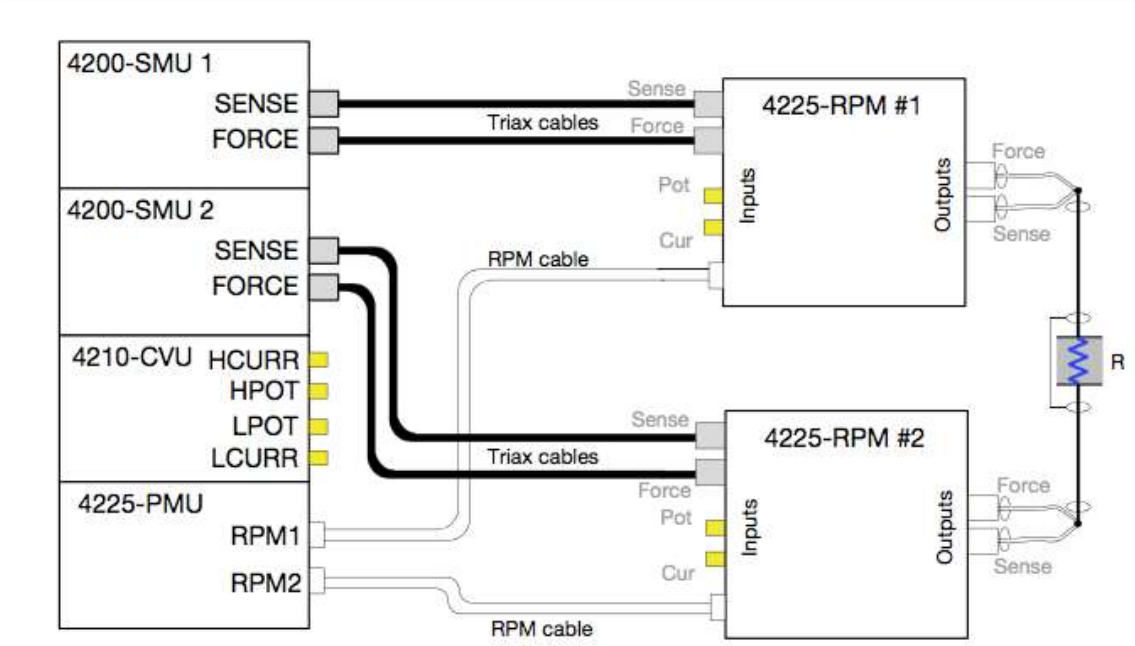
Memory test application example: RRAM test with 4200A



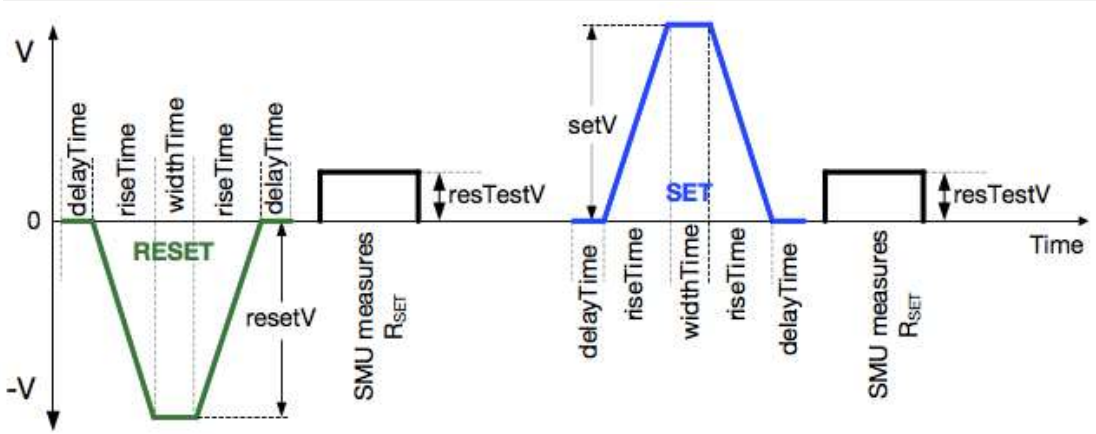


Figure 43. Pulse waveform with measure for *reramSweep* and *reramEndurance*.

Memory test application example: RRAM test with

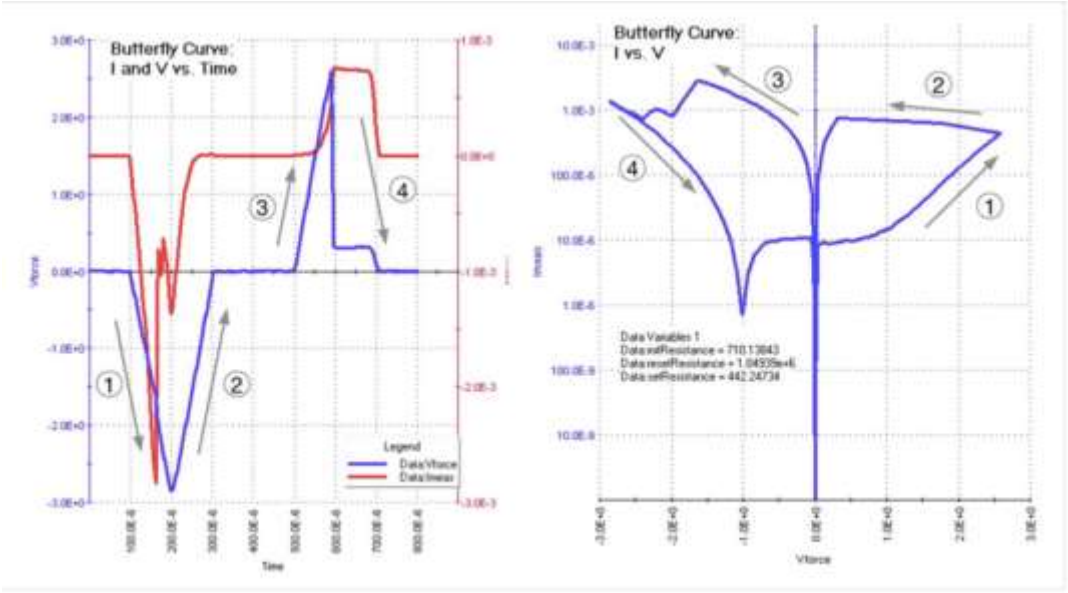


Figure 41. ReRAM "Butterfly" curve.

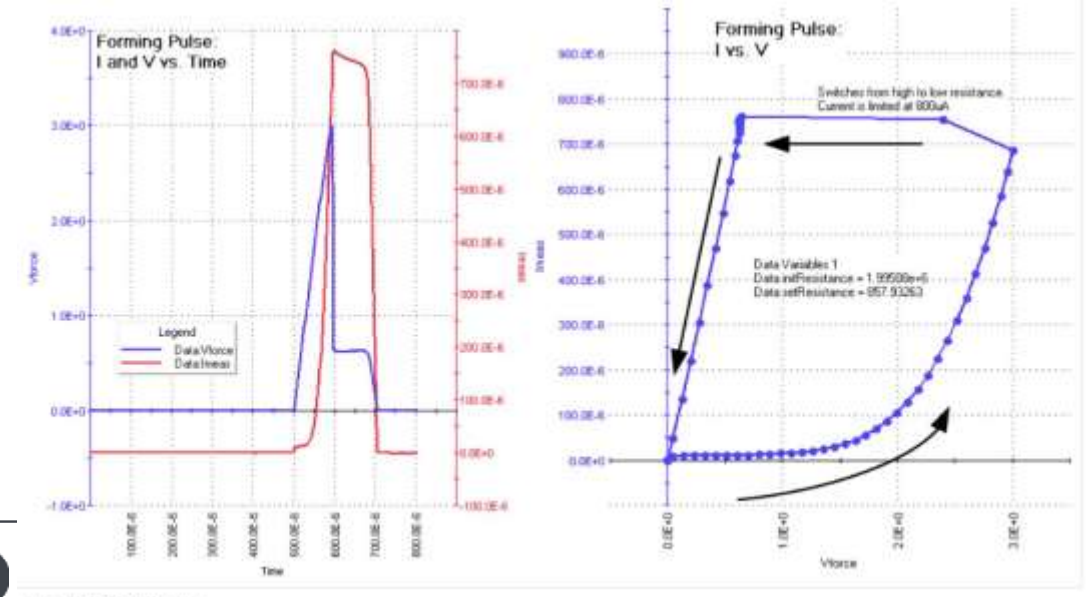


Figure 40. ReRAM forming.

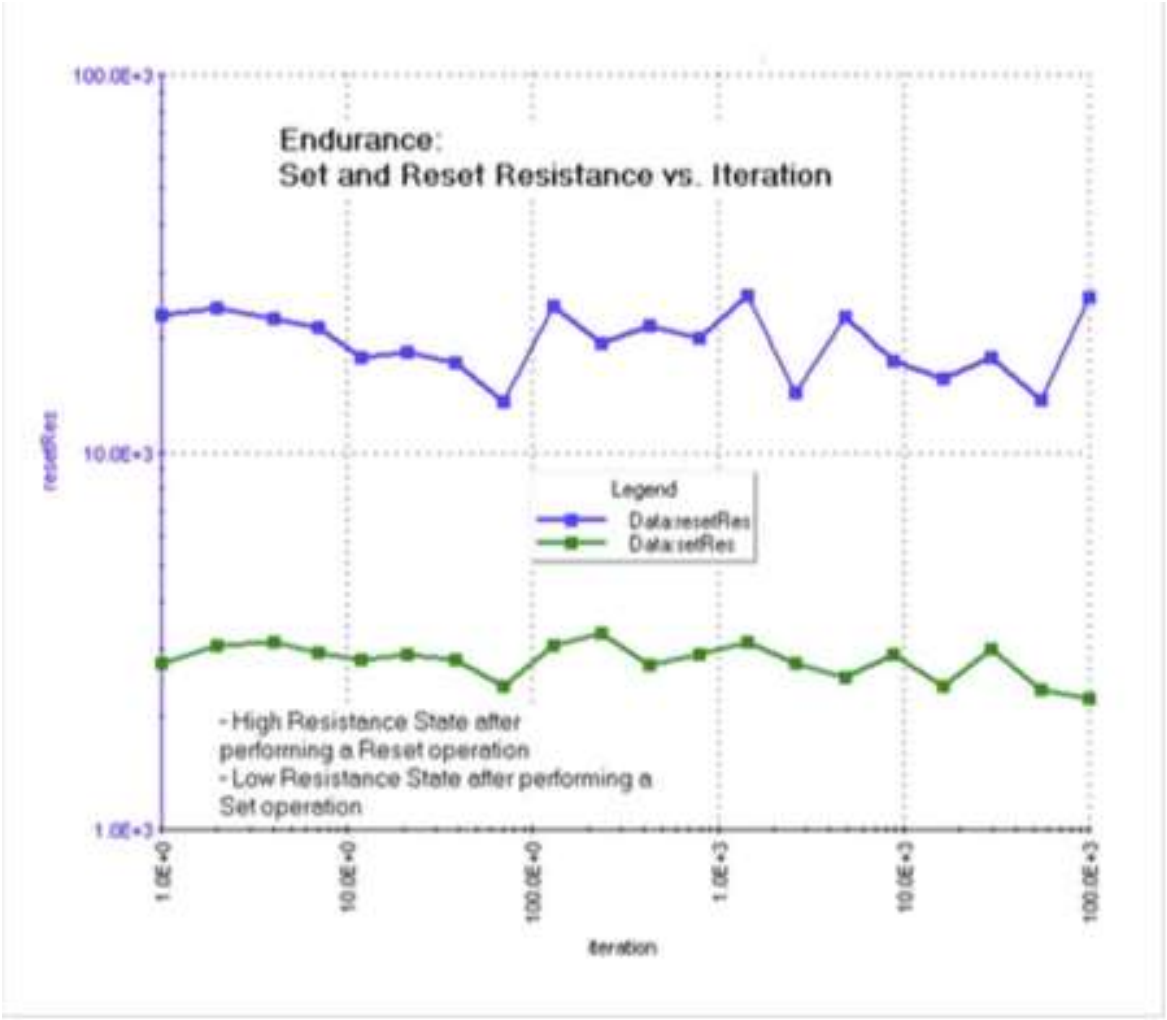
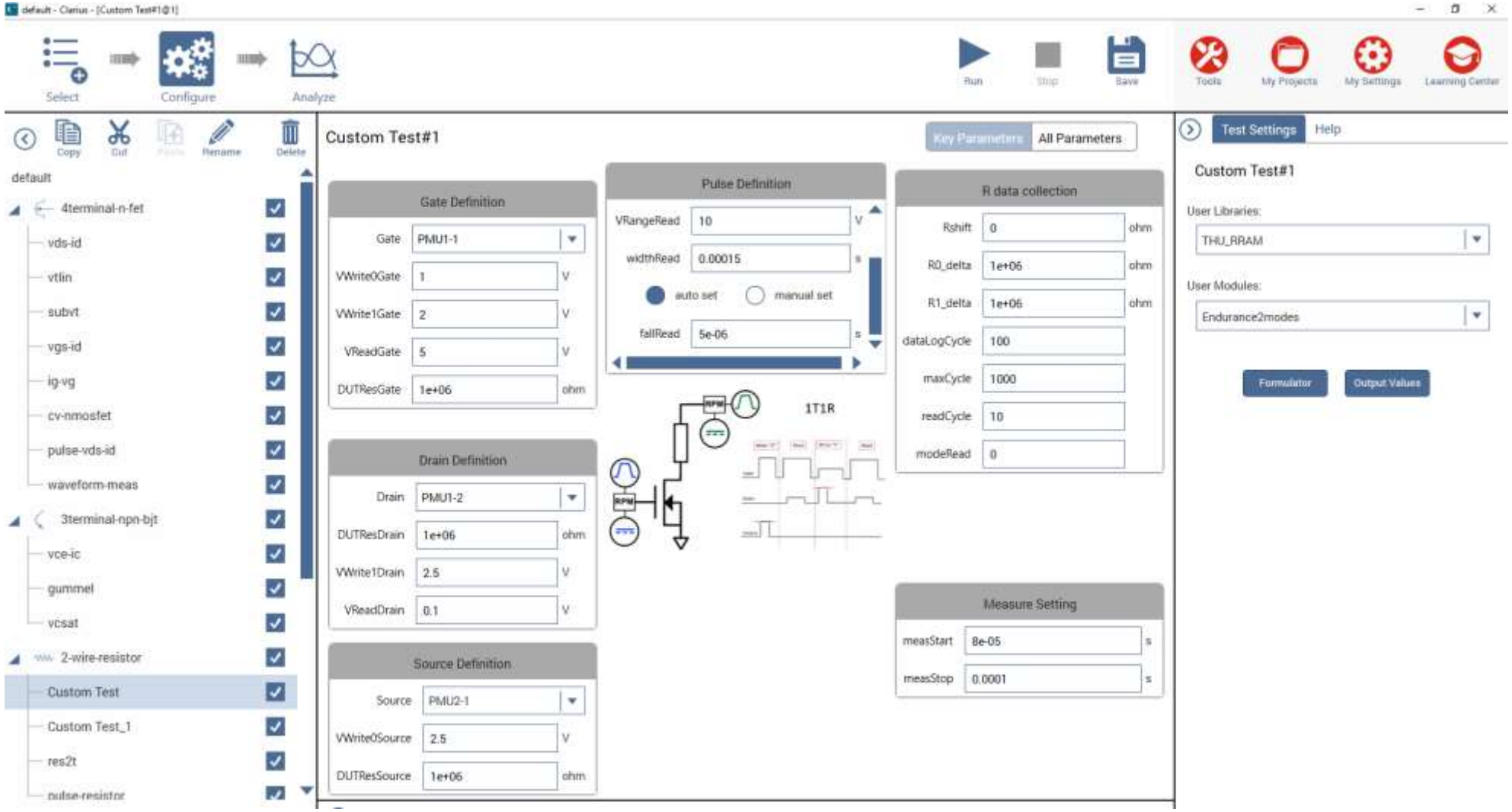


Figure 42: ReRAM endurance test.

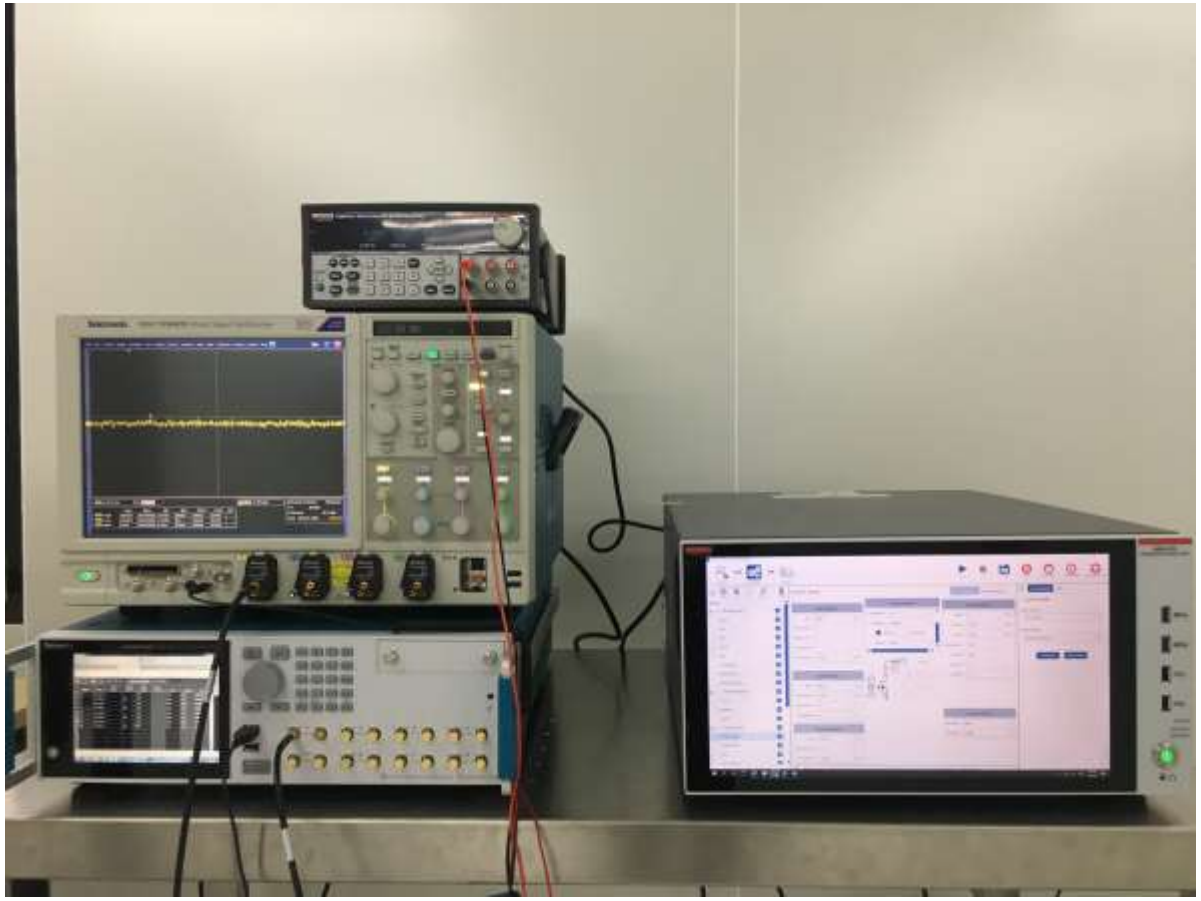
Customized Software for NVM test

KEITHLEY SERVICE FOR SOFTWARE DESIGN



Customized Software for NVM test

KEITHLEY SERVICE FOR SOFTWARE DESIGN



Example

2. 三端器件XXXXXXXX特性测试　G,D,S三端

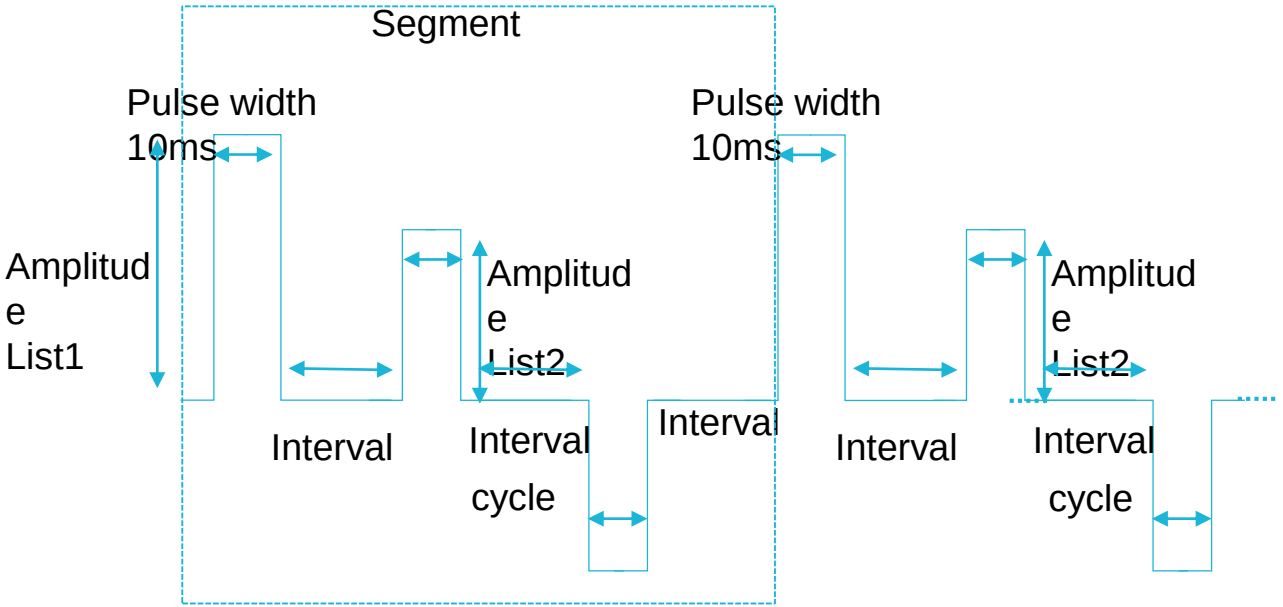
S端施加恒定电压，并不间断测量电流（电流采样频率可调）
G端施加电压脉冲序列（脉冲幅度和脉宽可调）
D端接地；

3. 两端器件 (B-P1, B-P2可响应， 只需设两端。不需硬件接地）

测试内容和三端一致，Top端施加脉冲信号/序列，Bottom端施加恒定电压并能不间断测量电流（电流采样频率可调）

只用PMU
Cycle <1000

B-P2:

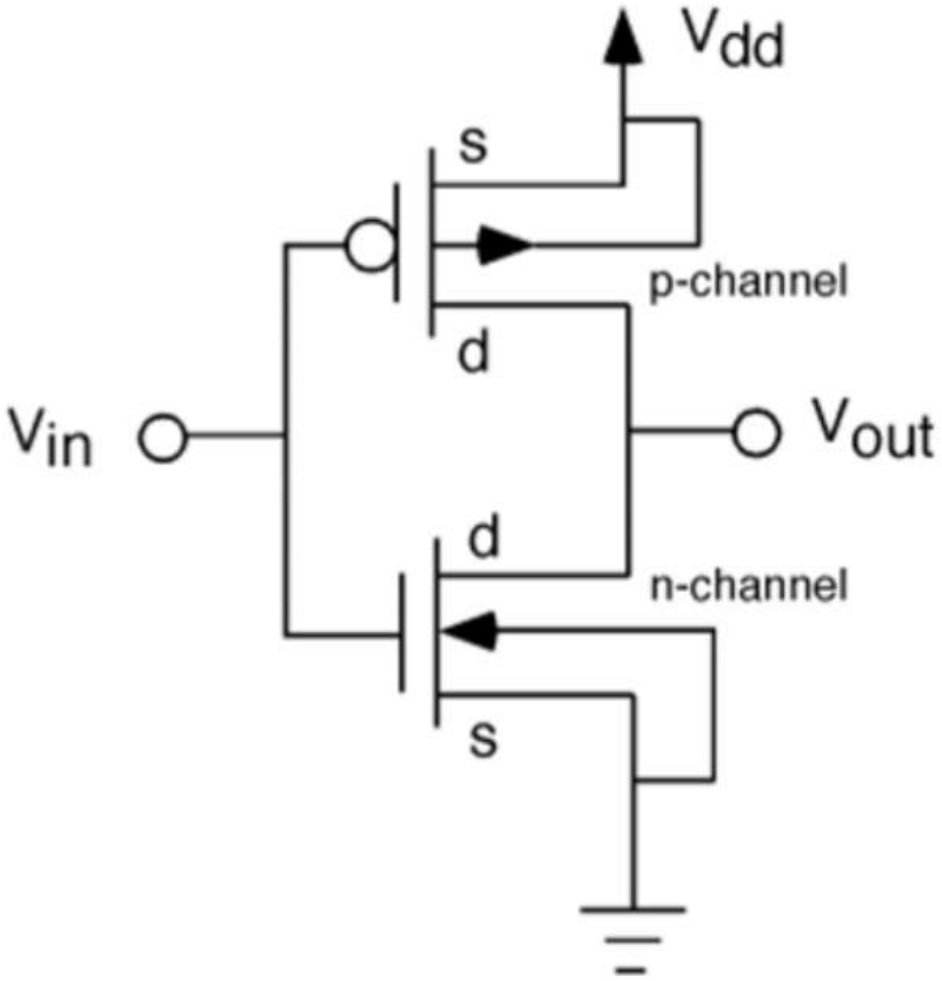


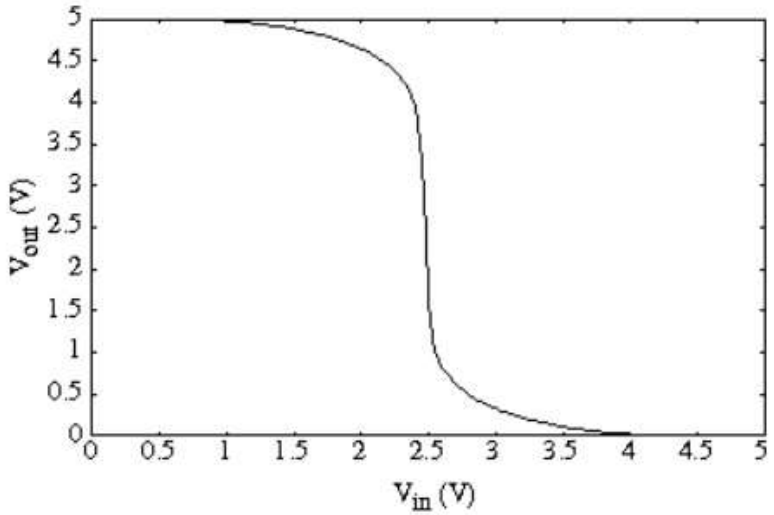
可调参数：
Channel assign→ GDS->CH1,2
a) 脉宽
b) Amplitude list
c) Interval
d) Cycle Number
e) 采样速率（sample/s)
f) S端电压 (另一channel DC)。

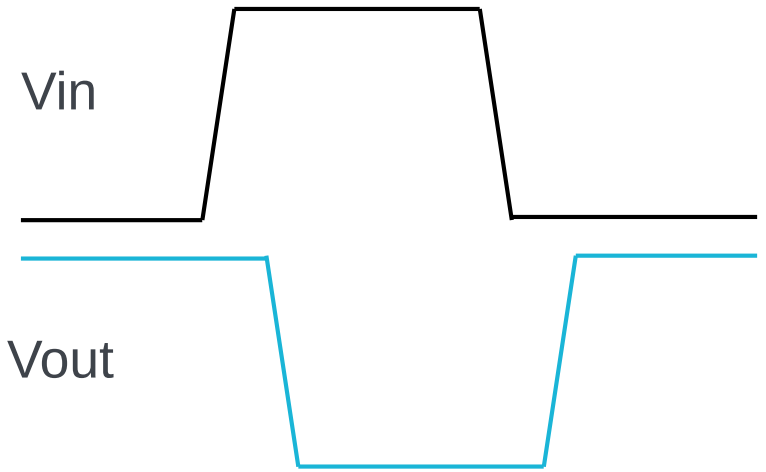
CMOS output character test

I-T/ V-T related test

CMOS test — ? vs. T test

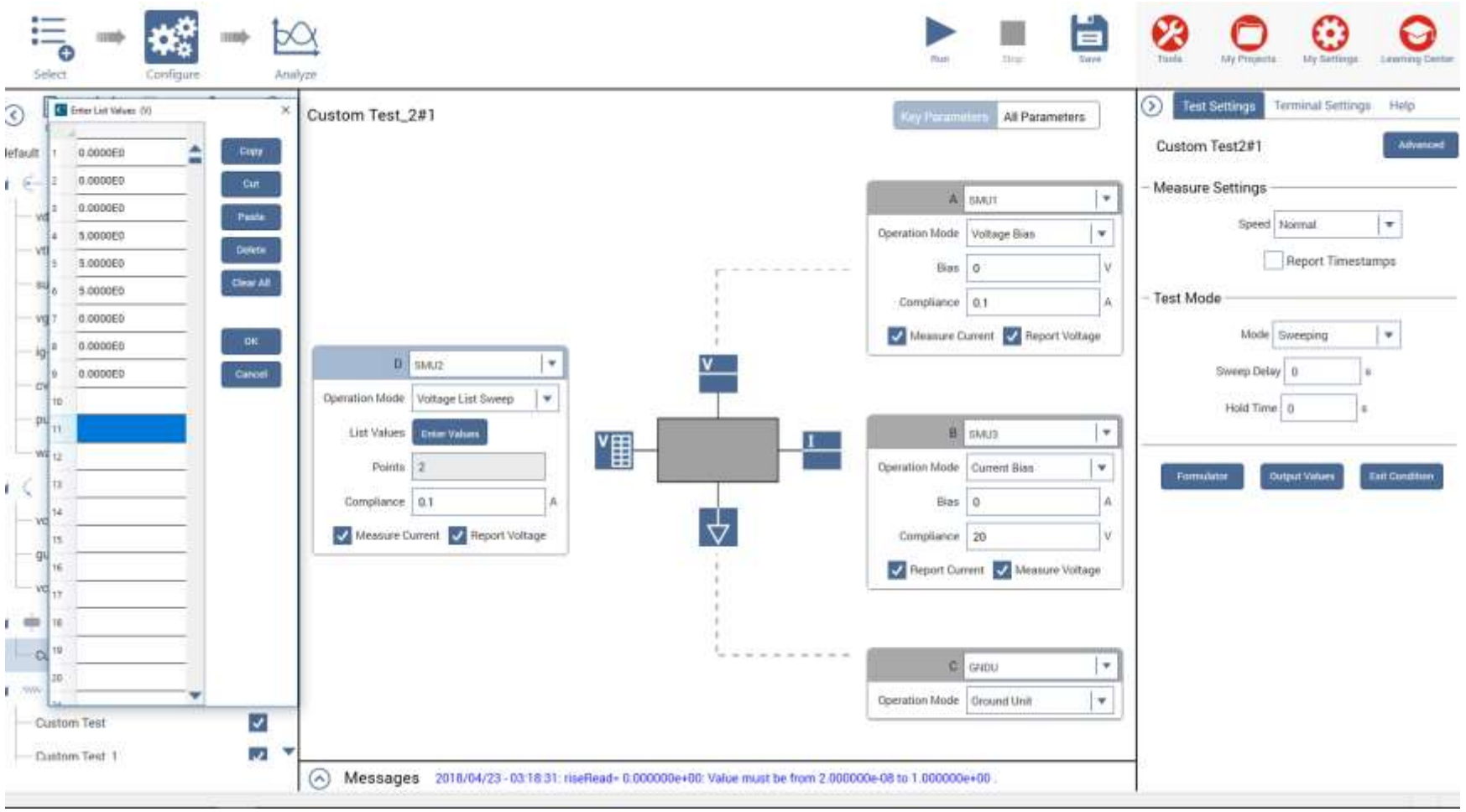






CMOS test — ? vs. T test

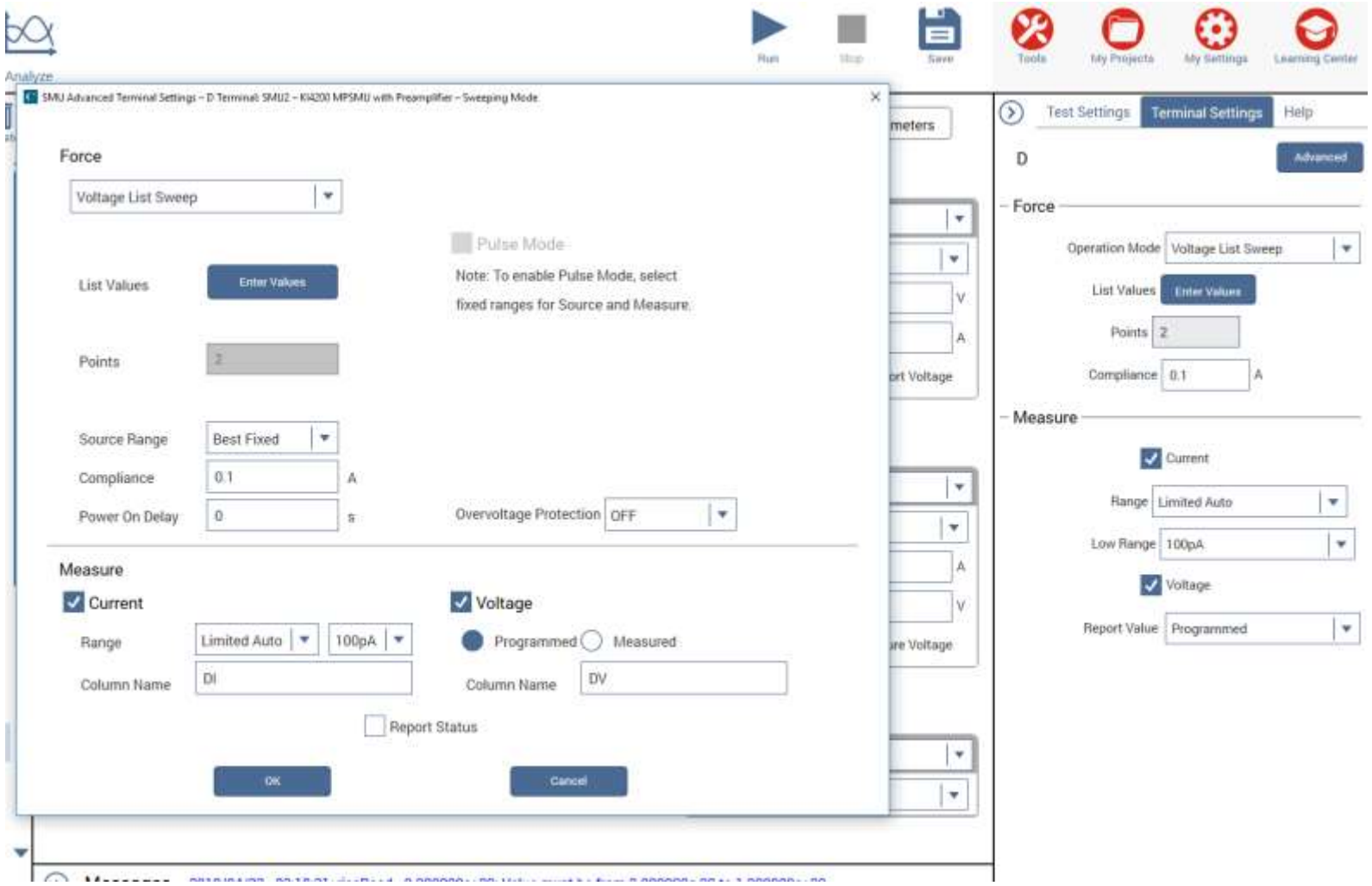
KEY SETTINGS



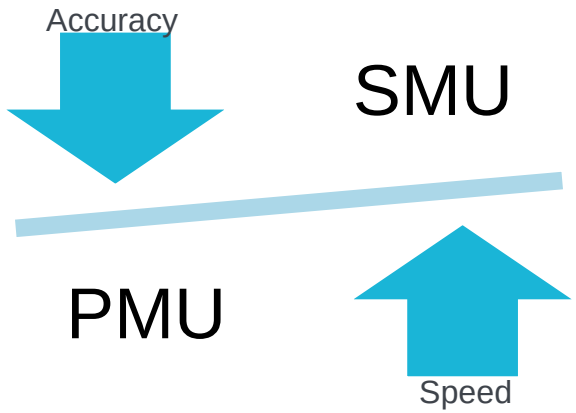
- Time
- List or Linear
- Test setting
- Terminal setting

CMOS test — ? vs. T test

KEY SETTINGS



- Time
- List or Linear
- Test setting
- Terminal setting



WBG (wide band gap)

Wide Bandgap Semiconductors

- Wide bandgap semiconductors are materials that possess bandgaps significantly greater than those of silicon.
- Enable power electronic components to be:
  - Smaller
  - Faster
  - More reliable
  - More efficient

  than their silicon-based counterpart devices.

Semiconductor Materials		
Material	Chemical symbol	Bandgap Energy (eV)
Germanium	Ge	0.7
Silicon	Si	1.1
Gallium Arsenide	GaAs	1.4
Silicon Carbide	SiC	3.3
Zinc Oxide	ZnO	3.4
Gallium Nitride	GaN	3.4
Diamond	C	5.5

End-Use Applications

WBG MARKET SEGMENTATION

As a function of voltage range

While SiC is used for high voltage applications, GaN is mainly used for low voltage applications. 600-900V range will be the battlefield

Low Voltage

PFC/Power Supply

Audio Amplifier

Medium Voltage

PV Inverter

Motor control

EV / HEV

UPS

High Voltage

Ships & Vessels

Smart Power Grid

Wind Mills

Rail Transport

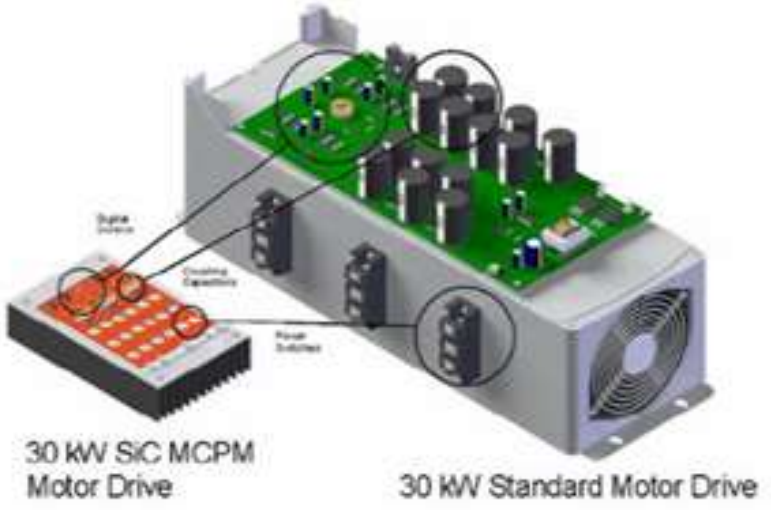
<200 V | **600 V** | **1.7 kV** | **3.3 kV** | **6.5 kV+**

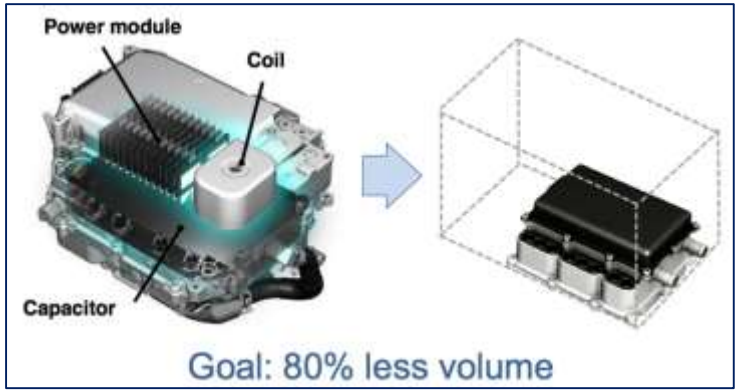
SiC diodes

GaN transistors | Battlefield | **SiC transistors**

Benefits of Wide Bandgap (WBG) Technology

- ~10X power density of Si
- < ½ Size
- Better higher temperature performance reduces or eliminates need for heat sinks
- Higher frequency results in lower losses during switching
- ~ Order of magnitude lower leakage current
- ~ Order of magnitude lower Rds-on





Technology Trends – GaN RF

- Massive increase in data rates is requiring technology updates to wireless network infrastructure (base stations) as well as evolution of cellular standard (movement to 5G)
- GaN RF is able to meet the higher frequency needs and power density needs
- Handheld RF devices
  - Government / Aerospace – GaN RF devices already used 28V – 48V
  - Consumer – Movement to 5G may necessitate research and spend on GaN RF devices in consumer handsets

Traffic essentials	2015	2016	2022 forecast	CAGR 2016 – 2022	Unit
Data traffic per smartphone	1.4	1.9	11	35%	GB/mo
Data traffic per mobile PC	5.7	7.7	23	20%	GB/mo
Data traffic per tablet	2.5	3.5	11	20%	GB/mo
Total mobile data traffic	5.3	8.5	69	45%	EB/mo
Total fixed data traffic	60	70	170	20%	EB/mo

From Ericsson 2016 Mobility Report

WBG Challenges

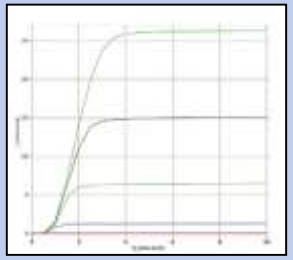
- Substrate size and cost: producing larger diameter wafer at a lower cost is improving but further gains are needed.
- Device design and cost: novel device designs that effectively exploit the properties of WBG materials are needed to achieve current and voltage requirements of certain applications
- Device measurements: requires a wide dynamic range of instrumentation that combine High Speed AC, Low Level DC, and High Power
- System integration: WBG devices are not always suitable drop-in replacements for Si-based devices. Complex systems must be redesigned to integrate WBG.

Typical WBG Tests

Testing WBG power devices requires **better resolution and faster speeds at higher power levels** compared to silicon, however the same basic tests are performed. Testing falls into two main categories that we currently serve:

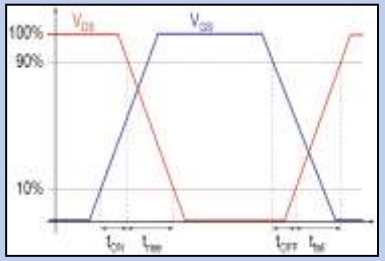
Static (DC) Testing: The customer's design goal is to optimize electrical performance in the ON and OFF states. An SMU instrument, System, or Parametric Curve Tracer is used to perform key tests such as:

- Breakdown Voltage
- Leakage Current
- On Resistance
- Characteristic Curves
- Capacitance

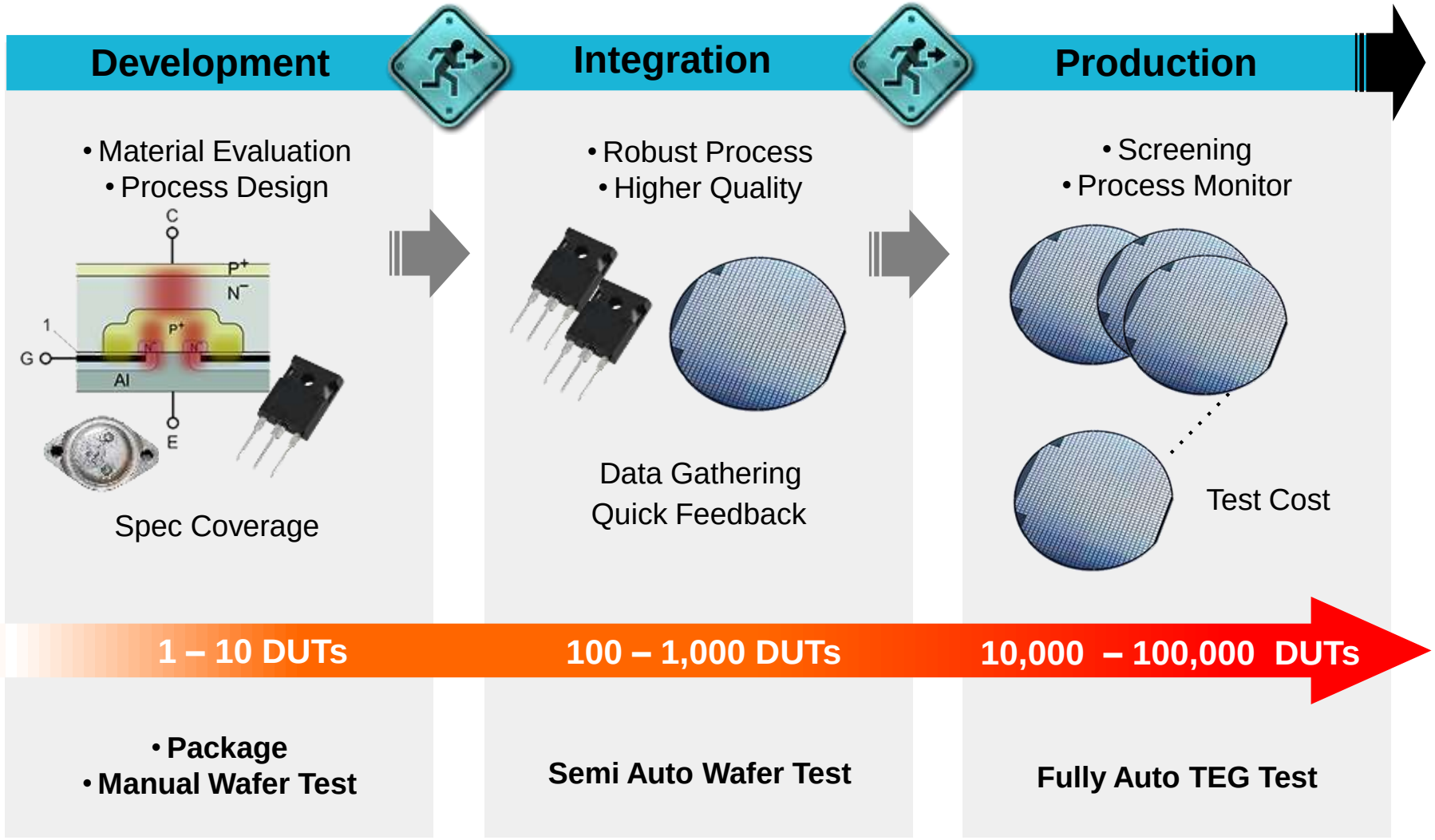


Dynamic (AC or Time Domain) Testing: The customer's design goal is to optimize switching times and perform comprehensive switching loss analysis. An Oscilloscope is used with Power Probes and an AFG to perform key tests such as:

- Turn-on / Turn-off times
- Rise and Fall times
- Recovery time



Path to High Volume Commercialization



S530 And S500

- 自动测试解决方案

软件

KTE

ACS

硬件

S530 Parametric Test System

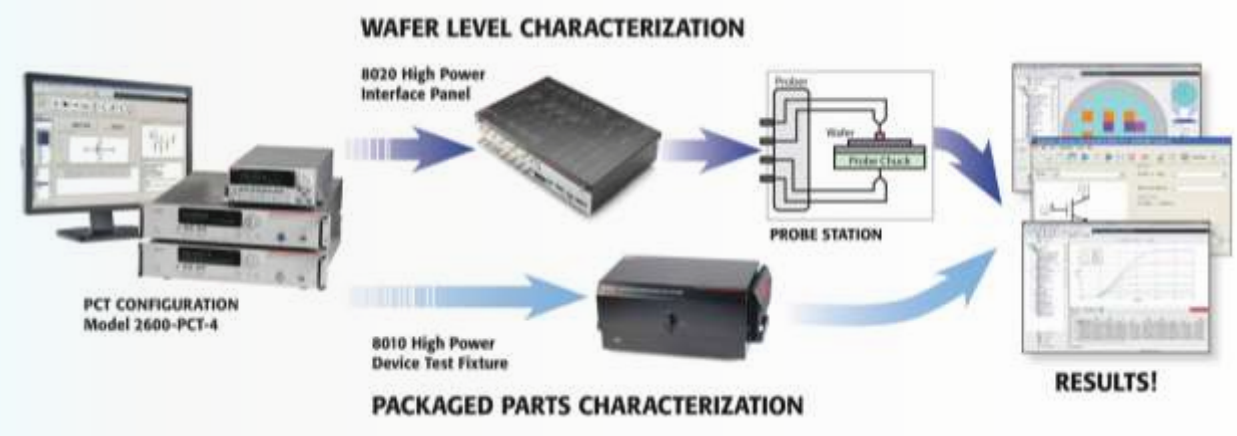
S500 Integrated Test System

Instruments

配置标准化的测试系统

可根据实际情测试需求定制硬件及特殊测试程序

Power: Test application example



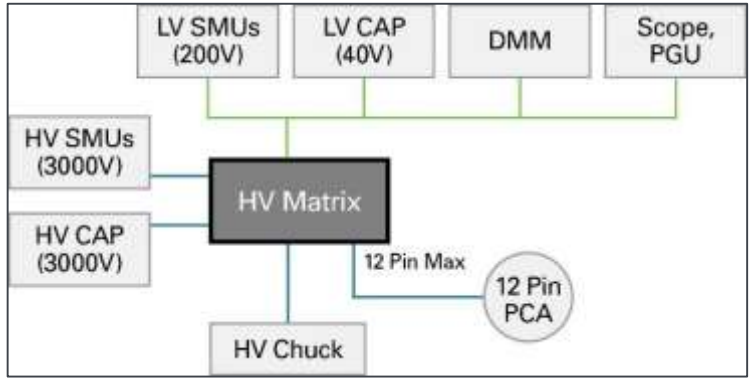
Manual
test for both wafer level and package level

Automated
wafer level parameter test for both R&D research and mass production

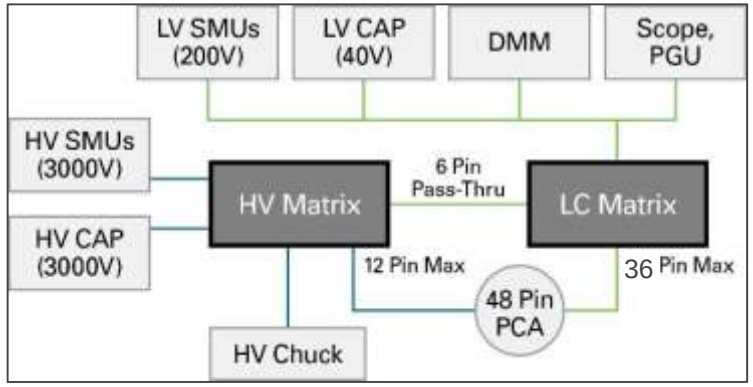
S540 Introduction

Industry's first 3KV automated parametric test system for wafer-level testing of power semiconductor.

- Eliminates the need to re-configure the test setup or use two separate test systems when moving from high voltage to low voltage tests
- Enables fully automated 2- or 3-terminal transistor capacitance measurements
- Delivers sub-pA level measurement performance in a standard, commercially available product.



12 Pin Configuration



24 - 48 Pin Configuration

S540 Introduction

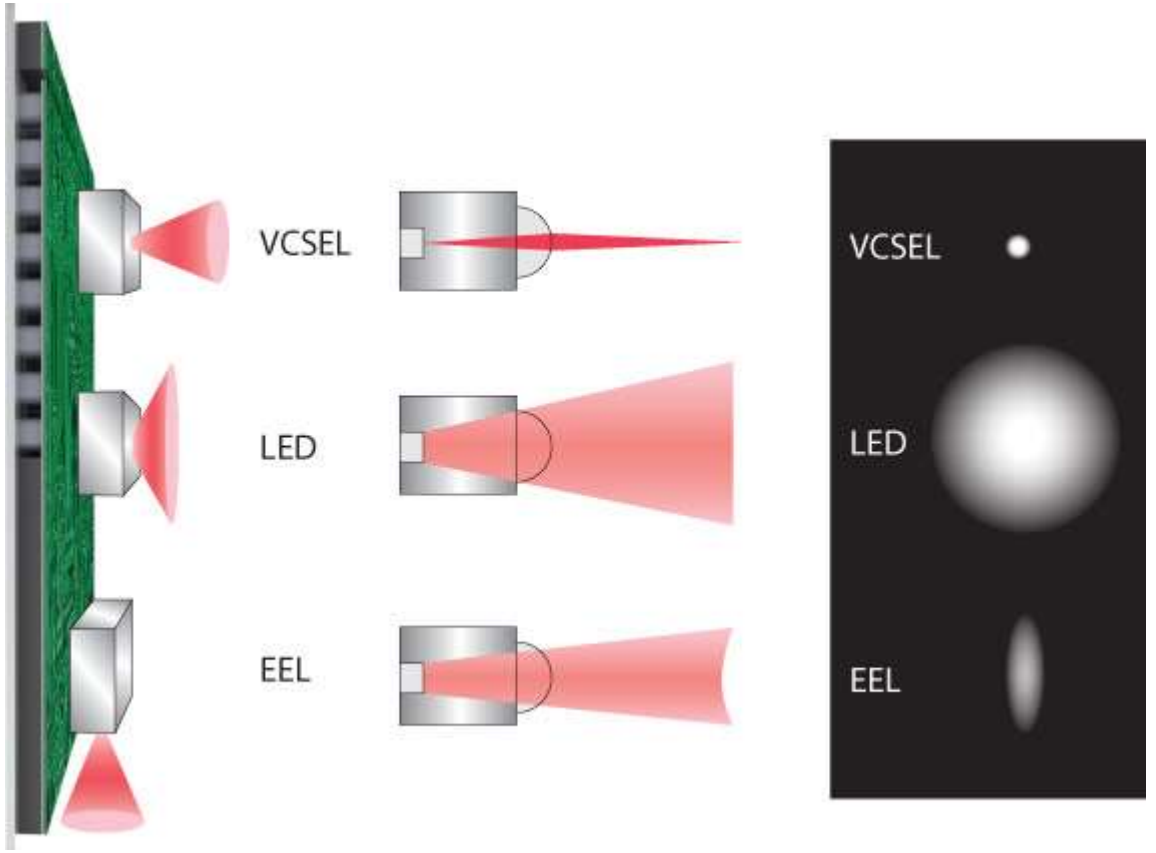
Key Feature	Quantity Available
Number of pins (full force-sense Kelvin):	
High Voltage (up to 3 kV using HV matrix) (includes 6 pin pass-thru from LC matrix)	12
Low Current (up to 200 V using 707B and 7531 matrix cards)	0, 12, 24, or 36
Number of SMU channels	
High Voltage (up to 3 kV using 2657A)	1 or 2
Low Voltage (up to 200 V using 2636B) (includes HV protection modules for each channel)	up to 8
Capacitance Meter (using 4210-CVU)	
High Voltage (up to 3 kV, includes Bias-Ts)	0 or 1
Low Voltage (up to 30 V, includes protection modules)	0 or 1
High Resolution DMM (using 7510)	0 or 1
Pulse Generator (using 4220-PGU)	0 or 1
Oscilloscope (FMTR)	0 or 1
Industrial PC controller with Linux OS	1
KTE System Software	1
37U System cabinet with 100–240 V, 50/60 Hz power distribution (PDU),emergency off (EMO) switch, high voltage interlock, and monitor/keyboard arm	1
Probe Card Adapter	
Keithley 9140 (48 pin maximum – 12 pin HV, 36 pin LV) Celadon (42 pin maximum – 12 pin HV, 30 pin LV) Customer Supplied	Choose One

3D sensing

VCSEL Technology

VERTICAL CAVITY SURFACE EMITTING LASER

- Semiconductor–based laser diode that emits a highly efficient optical beam vertically from its top surface.
- Other common optical sources include Edge Emitting Lasers (EEL) that emit light from the side and Light Emitting Diodes (LED) that emit light from the top and sides.
- LEDs output a wide angle spectrum
- EEL emit elliptical beam

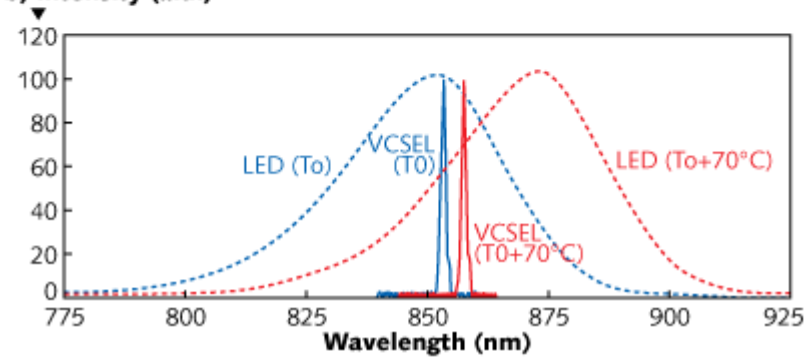


Advantages of VCSEL Technology

- Reliability: VCSELs don't have failure modes of traditional laser structures such as dark line defects.
- Manufacturability: able to use traditional semiconductor manufacturing equipment to keep fabrication costs low.
- Testability: can be completely tested at wafer level This increases yield and lowers cost.

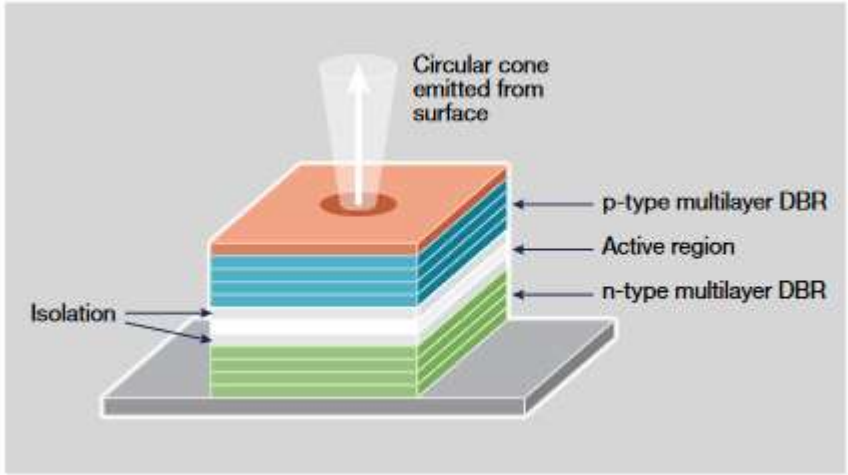
a) Comparison of infrared (IR) illumination sources

Parameter	High-power IR LED	High-power IR VCSEL array	Edge-emitting laser
Low cost and manufacturability	++	+	–
Ease of packaging	+	+	–
Output power	–	+	++
Reliability	+	+	Neutral
Power conversion efficiency	Neutral	Neutral	+
Modulation speed	–	+	+
Emission beam and optics integration	–	+	–
Spectral properties	–	++	+
Speckle-free	+	+	–



VCSEL Technology Advantages

- Because VCSELs emit light perpendicular to the surface of the laser, tens of thousands of VCSELs can be processed on a single 3” wafer.
- VCSELs can also be tested at various stages of the manufacturing process while in wafer form, resulting in a more controlled and predictable yield with lower fabrication costs compared to other laser technologies.



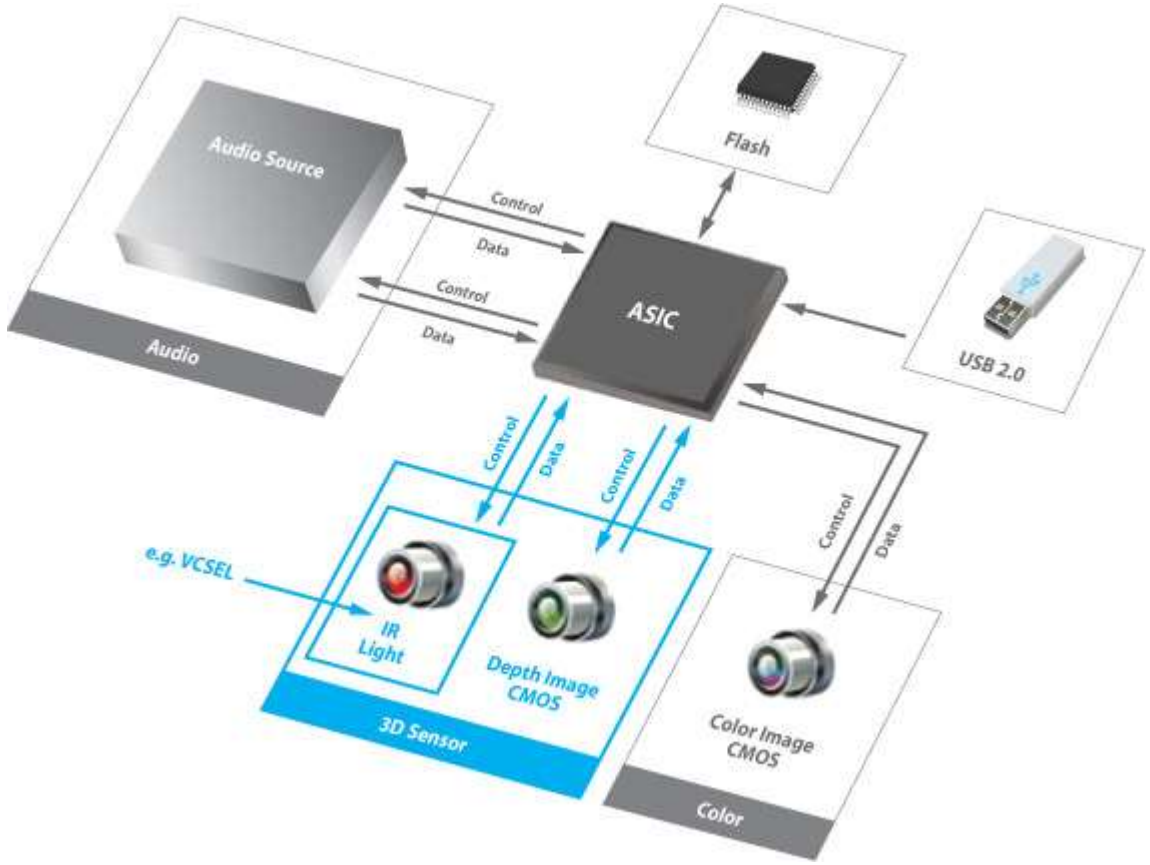
3D Sensing & Gesture Recognition

VCSEL APPLICATION

- 3D sensing enables autonomous, self-driving vehicles and lets the driver control infotainment systems more quickly and safely.
- 3D sensing systems transform the user interface for gaming and facial recognition in smartphones.
- In industrial equipment, 3D sensing allows operators to control computing equipment safely in hazardous environments.
- In future mobile devices, 3D sensing will augment camera capabilities to enable object recognition, depth data, greater precision, and object placement.

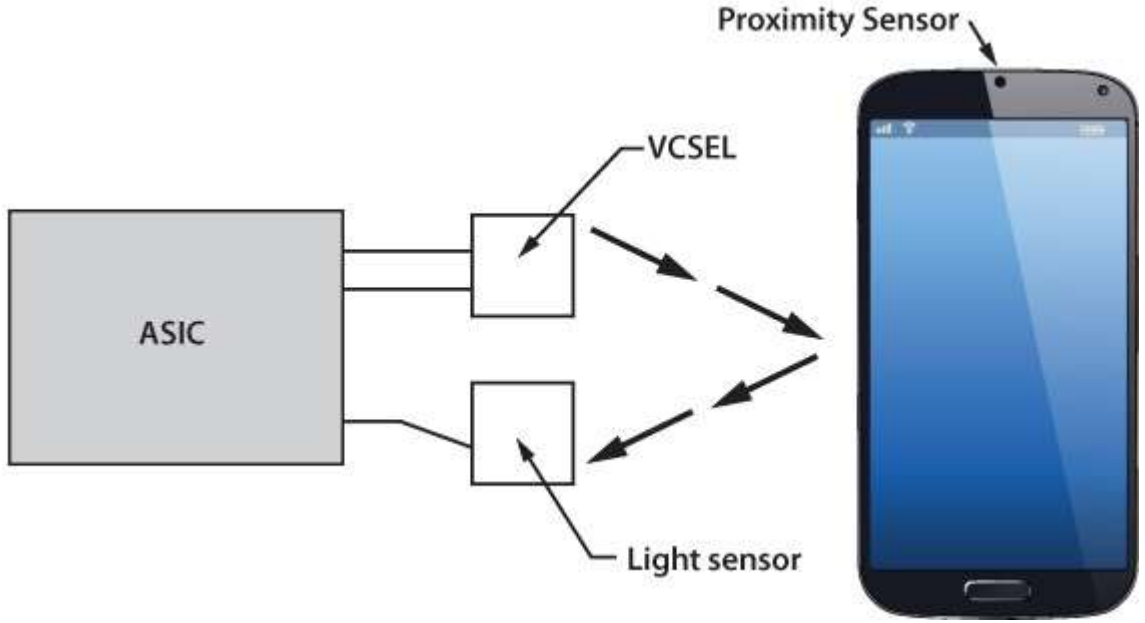
3D Sensing - Time of Flight

- To be able to detect movement across a living room, the detection system needs high power and precision.
- “Time of flight” tracking techniques flash a light pulse and track depth and motion by measuring the travel time of the light pulse from an object to an individual pixel on an image sensor.



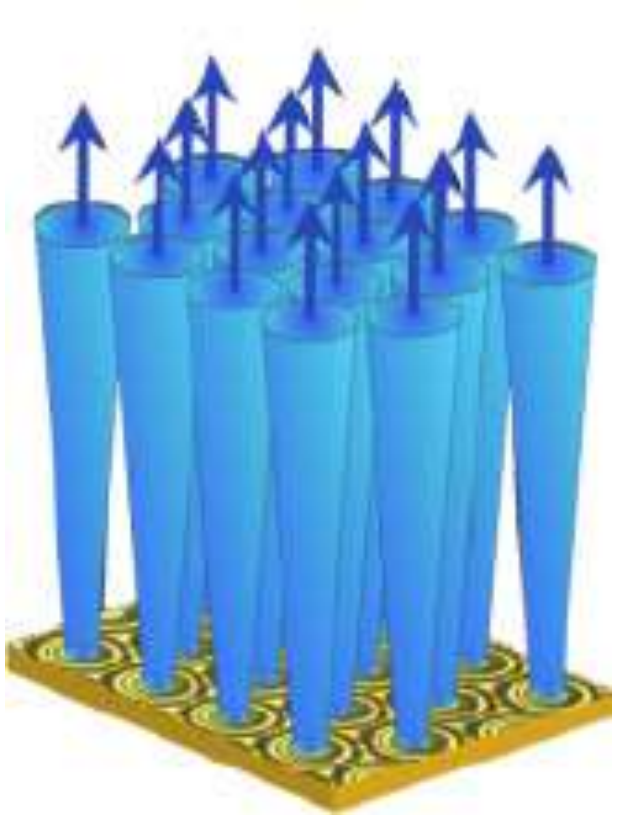
VCSEL Emerging Applications

- Proximity Sensing: measured by transmitting light and sensing reflections from nearby objects.
- Remote Power: use a light source to deliver energy to a sensor optically.
- Atomic Clocks: VCSELs reduce the form factor of a cesium or rubidium atomic clock down to a chip scale package.



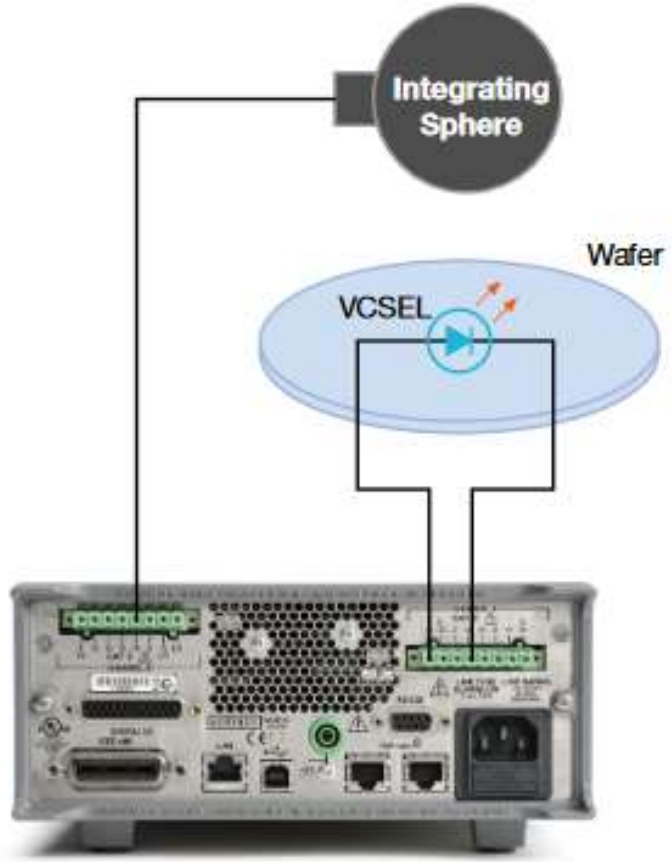
VCSEL Challenges

- Manufacturing cost: with the rapid expansion of VCSEL applications, there is demand for higher performance at a lower cost.
- Device measurements: in production, testing many VCSELs at once, at wafer level, is required to monitor performance and yield. Common measurements are both DC and optical testing.



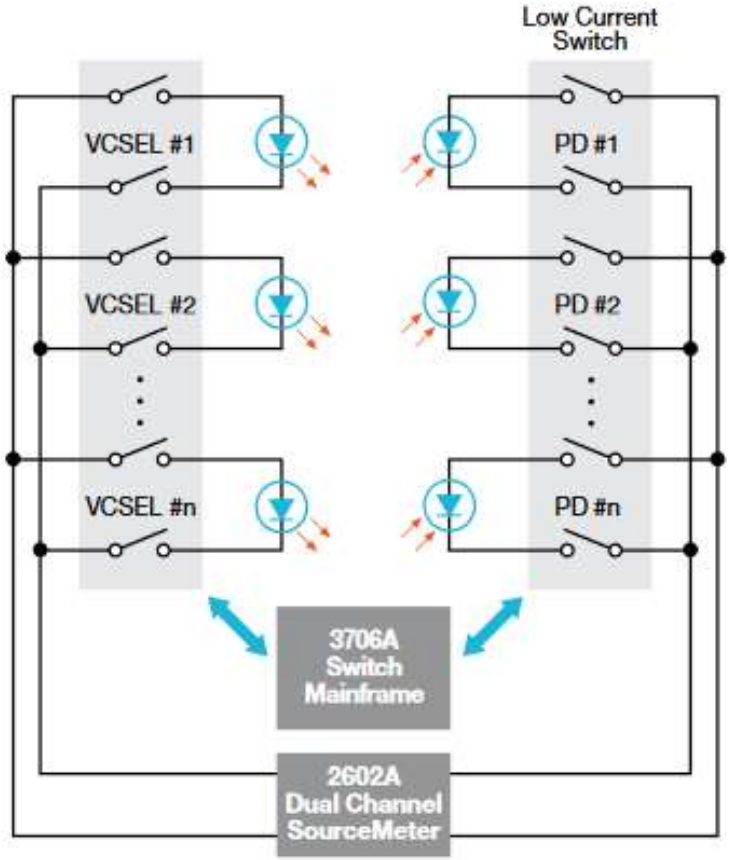
VCSEL Measurements

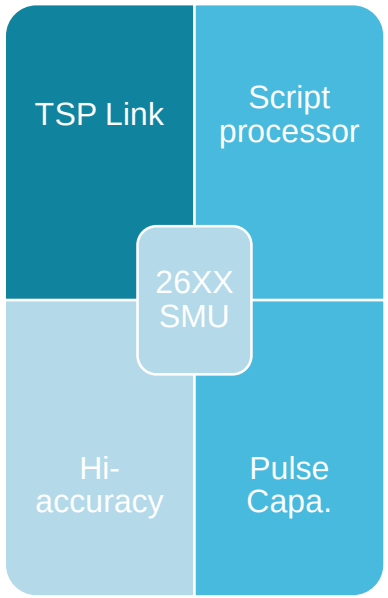
- During DC testing, the specifications of interest for the VCSEL module include:
  - Forward voltage
  - Kink test or slope efficiency (dL/dI)
  - Threshold current
  - Monitor (back facet) reverse-bias voltage
  - Monitor (back facet) current
  - Monitor (back facet) dark current
  - Optical output power

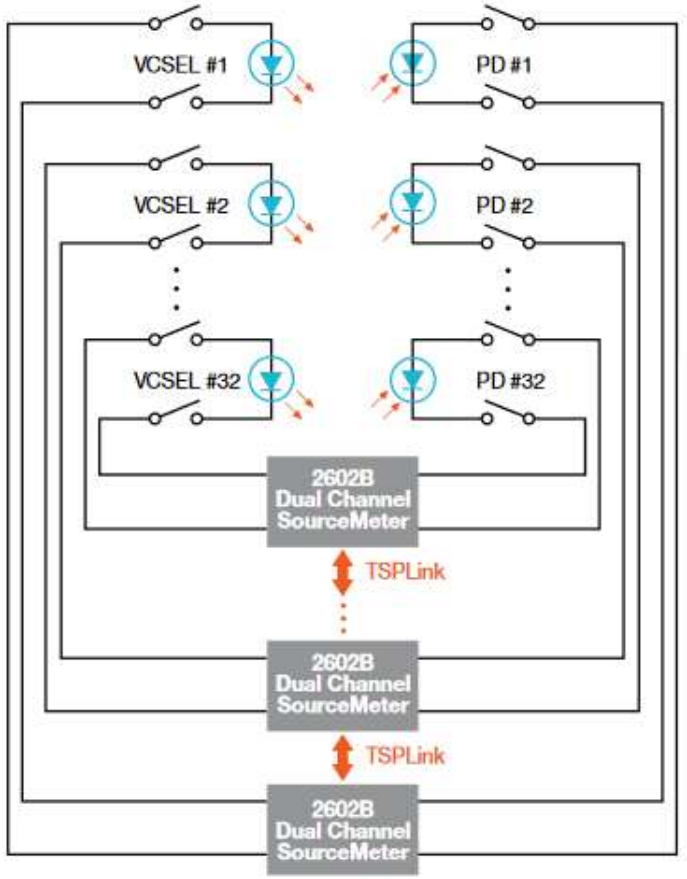


Meeting the Production Challenge

- Test multiple VCSELs using a switch and 2602B Source Measure Units.







- Test multiple VCSELs on wafer using a parallel test configuration using multiple 2602B Source Measure Units.