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NEW MATERIALS—NEW RELIABILITY ISSUES

Semiconductor device reliability can generally be broken into two parts: *infant mortality failures* and *wearout mechanisms*. Infant mortality failures are due to manufacturing defects. The sources of these defects are generally the same as those that cause yield loss, so instrumentation requirements for detecting both are similar.

Wearout failure mechanisms are known physical degradation mechanisms that will eventually cause the device to fail. For the reliability assurance engineer, the challenge is to ensure the degradation rate is slow enough to minimize the probability the device will fail within some specified "useful lifetime."

As semiconductor devices trend towards smaller geometries, denser packing (transistors/cm^2), faster speeds, and lower power consumption, requirements for the instrumentation used to monitor their reliability will become more severe. In many cases, technological advances will simply be continuations of existing industry trends, such as the move towards thinner gate oxides. However, the introduction of new materials into the process will also influence instrumentation requirements.

For most of the industry's history, semiconductor technology has been based on manipulation of silicon, silicon dioxide, and aluminum. As we reach the fundamental limits of these materials, new ones are being developed that will enhance product performance and/or reliability, but may also include additional failure mechanisms that must be addressed.

This paper addresses some of the new processes/materials likely to be introduced into the semiconductor process soon and discusses the impact of these changes on the process monitoring instrumentation required to ensure product reliability.

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Thin Oxides

As oxides grow thinner, reliability assurance engineers continue to need a better understanding of the Time Dependent Dielectric Breakdown (TDDB) phenomena. As gate oxide thickness approaches mono-layer dimensions, TDDB studies are focusing on subatomic level defects. Defects in gate oxides are no longer considered "thin spots" in the gate dielectric, but rather the chemical state of the silicon and oxide atoms in the dielectric [1, 2]. The issue of quasi-breakdown—gates or capacitors that become leaky but do not become shorted—has also become important [3, 4]. As these issues have developed, the value of voltage and current ramp tests long used for gate oxide studies is increasingly limited. Oxides with quasi-breakdown conditions can show sub-picoamp levels of leakage, which would be invisible with many earlier oxide test systems. At the same time, the defect density required for reasonable yield and low infant mortality defects continues to drop. ***Table 1*** shows the impact of defect density on device yield as technology advances.

Table 1. Effect of Defect Density on Yield for Different Technologies

Assume 0.2 defects/cm^2 of gate area and 0.002 defects/m of perimeter

Technology	Number of Transistors	Gate Area (cm^2) (total/die)	Gate Perimeter (m) (total/die)	Projected Yield
1.2µ	500K	0.027	5.1	98.5%
0.8µ	1.5M	0.036	10.2	97.6%
0.5µ	4.5M	0.056	28.35	94.2%
0.35µ	10M	0.065	37.8	92.3%
0.25µ	15M	0.10	100	78%
0.18µ	30M	0.13	143	69.4%
0.13µ	54M	0.19	360	24.2%
0.1	91M	0.25	608	0.8%

Gate oxide defects will always be an important consideration in technology development for several reasons, particularly because of the increasing sensitivity of today's oxide to smaller defects and the simultaneous growth in demand for lower defect density.

As oxides become more sensitive to smaller defects, the ability to characterize these oxides at low fields becomes critical. Small area defects pull relatively little current before they become hard shorts. This makes them difficult to detect in large test capacitors [5] where trap assisted tunneling currents can easily exceed the leakage in a small area defect. Our work has shown that a defect that can reduce the oxide thickness by as much as 50% in an area equivalent to 10% of the area of a 0.5µm × 1.0µm gate will pull only 7.6fA of current at 3V, while trap assisted tunneling can be as high as 1pA/cm^2. In many cases, such defects are

clearly the root cause of gate oxide failure, but the low tunneling currents make these defects invisible when tested in a large capacitor. This has led to the use of voltage ramp and constant current tests to identify defects in the oxide only after they have become hard shorts. These tests generally rely on very high fields to achieve short test times; therefore, they introduce additional uncertainty with respect to the impact of the high fields [6].

The use of an array of smaller test capacitors with the same area as a single large capacitor makes it possible to detect the very low tunneling currents of small defects while still maintaining a short test time [5]. However, this does not address the issue of the changing nature of gate oxide "defects." Today's defects are more likely to be a different chemical state of the atoms in the solid than they are to be macroscopic defects like thinning or metal contamination. This makes detecting an initial low leakage current an insufficient way to gauge the reliability of the semiconductor device. The aging of the oxide must be studied. Again, this aging is more easily studied with low current measurements at lower fields than with higher fields, which cause a catastrophic breakdown. ***Figure 1*** shows the change in the current/voltage plot as a function of the aging of the oxide with a short (10 seconds) tunneling current stress at sequentially higher fields. This "Pronin plot" illustrates:

- The development of defects ("Fowler-Nordheim Walkout" on the right side of the curve).
- The change in trapped change in the oxide (shift in the "0 current crossing point," the shift from positive to negative current).
- The change in trap assisted tunneling current in both directions as a function of time.

These measurements provide a much more sensitive characterization of the changes in the thin oxide as a function of aging stress than a voltage to breakdown histogram would.

Characterizing small area capacitors makes it possible to determine the inherent characteristics of the oxide. Testing large arrays of these capacitors makes it possible to detect and characterize anomalous point defects. The small size of these anomalous defects means that the instrumentation used to detect them must provide femtoamp-level current resolution.

Interlevel Dielectric

The parasitic capacitance of the interconnect lines has taken a dominant role in determining the maximum speed of a semiconductor device [7]. At the same time, the impact of the interlevel dielectric on device reliability has increased. Speed degradation can be a reliability issue—one that is increasingly dependent on changes in the interlevel dielectric.

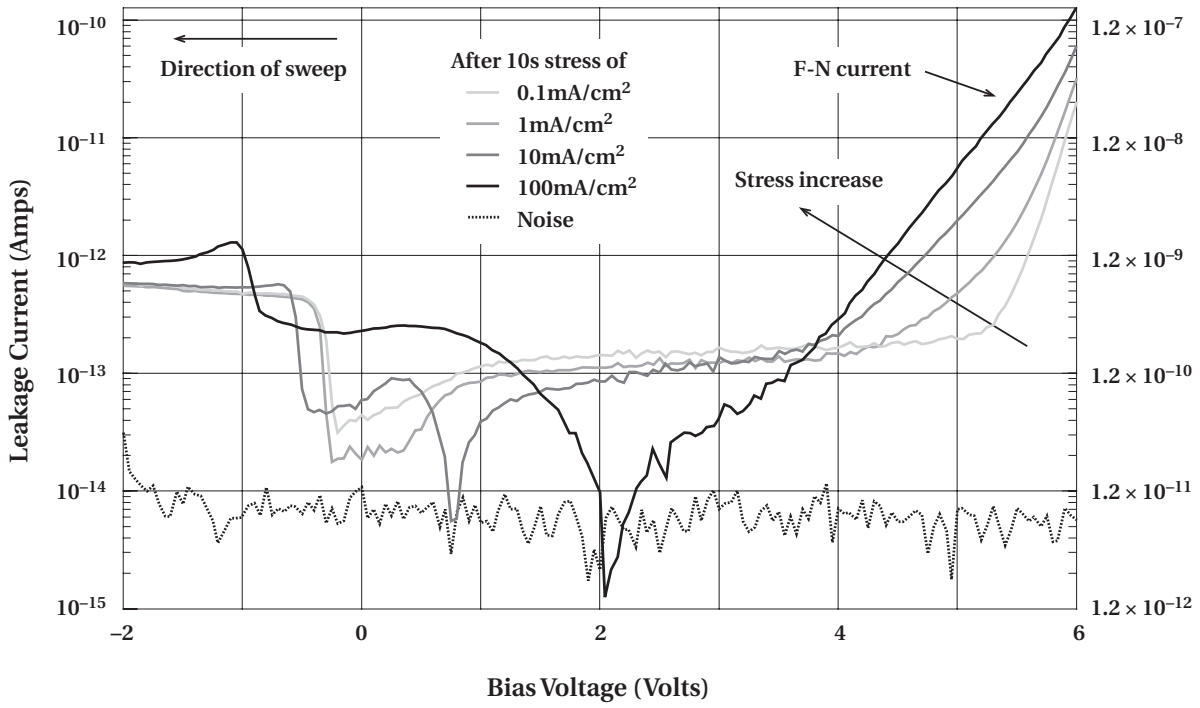

Figure 1. Pronin plot of gate oxide capacitor leakage current, voltage swept from 6V to –2V, 70Å oxide over well, no source or drain implants around capacitor.

Dielectric Absorption

Ions and dipoles in a dielectric material can diffuse in the material when it is exposed to an electric field. This movement of charged particles causes a displacement current in the parasitic interconnect capacitors and changes their capacitance. This change in interconnect capacitance can have a significant impact on the speed of critical nodes in a semiconductor device. Recent work [8] has shown that a displacement current as low as 15fA, measured three seconds after a voltage pulse is applied, can indicate a dielectric absorption effect that can cause a 10% change in the parasitic capacitance over a ten-year period. The ability to detect this small current greatly limits the instrumentation that can be used to measure this effect. Femptoamp-level current resolution is required; also, parasitic instrument dielectric absorption must be much lower than was once possible. The S600 system introduced a picoammeter front-end, per-pin design. This design eliminated the dielectric absorption inherent with traditional tester designs that had a standard probe card, switch matrix, cabling from the probe card to the matrix, and more cabling from the measurement instruments to the switch matrix (***Figure 2***).

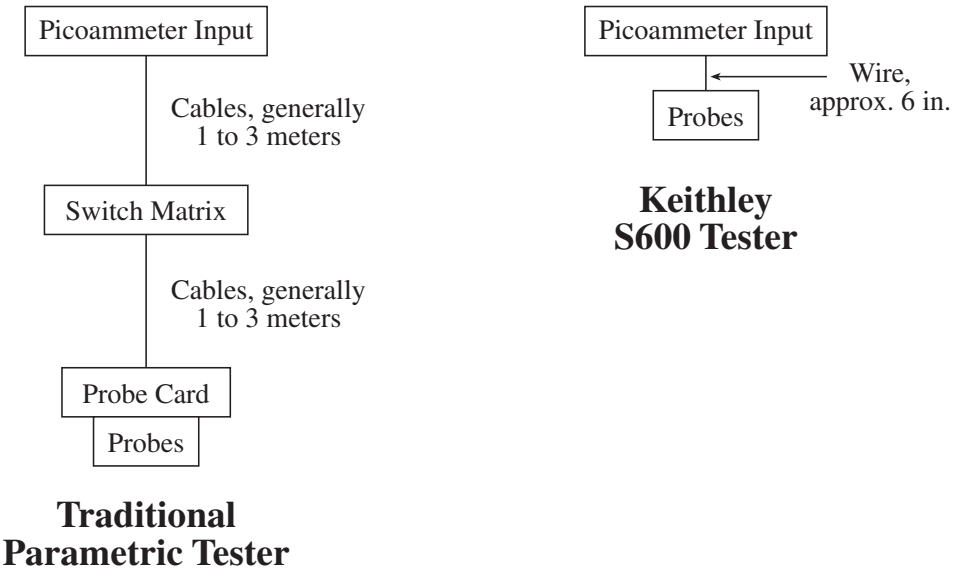

Figure 2. Reducing the length of the signal path between the probes and picoammeter input reduces the test's parasitic dielectric absorption effect and allows measuring the dielectric absorption effect on a typical test structure.

κ Drift

Low κ dielectric materials sometimes show a drift in the measured dielectric constant (κ) as a function of time and temperature. This drift can affect the speed of the product, causing the device to fail at high speed some time in the future. The degradation in speed is due to chemical changes that occur in some low κ dielectrics. The rate of the chemical reaction that causes this degradation in κ can be accelerated by high temperatures.

High temperature aging of a wafer is difficult due to issues with thermal expansion of the probe and hot chuck. However, high temperatures can easily he developed within small test structures using self-heating techniques. ***Figure 3*** shows an interdigitated metal capacitor on top of a poly resistor. Current is forced through the poly resistor, resulting in joule heating of the poly line. The temperature of the metal lines are measured using the long serpentine metal line on the lower edge of the poly heater. A measurement of the change in resistance of this metal line as current is forced through the poly heater resistor provides the measure of the temperature. The change in resistance divided by the TCR (thermal coefficient of resistance) for the metal provides the temperature of the metal lines. The current through the heater resistor is ramped up until the metal resistor shows a change in resistance equivalent to the

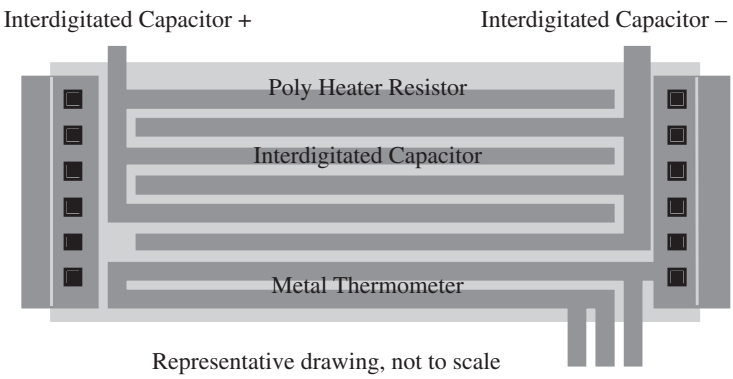

Figure 3. Self-heated capacitor for κ drift measurements for low κ ILD material

desired stress temperature (typically 450–500°C). The capacitor is aged for some period of time (typically 30–120 seconds), then allowed to cool back to room temperature. The small thermal mass of this test structure allows it to be heated to 500°C in less than one second and to cool to room temperature in less than five seconds. Following the cool down, the change in capacitance of the interdigitated capacitor can be calculated and a change in κ computed.

The amount of current required to drive a self-heated resistor is typically between 150mA and 200mA. This provides the power needed for this technology without exceeding the current limitations of the probes. Measuring the change in temperature requires instrumentation able to measure a change in resistance of the TCR of the metal (e.g., the TCR of Cu is 0.36%/°C, so the instrumentation must be able to resolve a 0.36% change in resistance). This measurement is complicated by the fact that the metal line usually has low resistance and the current that can be forced through it must be less than that which will cause joule heating. For a metal line 0.2µm wide and 200µm long with a sheet resistivity of 0.05Ω/□ sitting on 2mm of oxide with a thermal resistance of 0.022°C/watt/µm/cm^2, the maximum voltage drop across the metal thermometer would be 11mV. Therefore, the instrumentation resolution required to measure a change in temperature of the line with 1°C resolution is 0.36% of 11mV or 40µV.

The size of the capacitor is limited by the fact that the current that can be forced through one probe needle is limited. While multiple probe pads could be connected to one self-heated resistor, this greatly increases the silicon area required to make this measurement. Limiting the current limits the width of the self-heated resistor because a certain power density is required to reach any specified temperature. If the test structure is designed to fit into a typical scribe lane and the heater current is limited to the level that can be safely forced through a single probe needle, then the capacitance of the test structure will be very limited. The capacitance of an interdigitated capacitor with 1500µm of perimeter, a space of 0.2µm, a

metal line thickness of 0.5µm and a κ of 3.0 would produce a capacitance of about 100fF. If the ability to resolve a 1% shift in this parameter is desired, the instrumentation must be able to resolve a 1fF shift in the measured capacitance.

Copper Metal Issues

The drive to reduce the parasitic RC delay associated with the metal interconnect lines has led the industry to move away from the traditional aluminum (Al) interconnect metal lines in favor of copper (Cu) based metallization. The sheet resistivity of Cu-based metal lines can be half that of Al-based metal systems. However, the move to Cu will require new process steps and has some new reliability risks associated with it.

Copper Diffuses into SiO_2 at Normal Process Temperatures

Cu diffuses easily into SiO_2 at normal processing temperatures, which increases the metal resistivity and decreases the isolation between adjacent metal lines. To prevent this, most Cu processes (e.g., dual damascene process) add a refractory barrier metal layer (e.g. Ta, W, or TaN), which is more resistive than Al, between the Cu and any SiO_2. For very narrow Cu lines, this can be a very important issue. Thick barrier layers can result in metal line resistance that is higher than Al lines. Therefore, the thickness of the barrier layer must be minimized. At the same time, cracks or holes in the barrier layer will allow the Cu to diffuse into the adjacent dielectric material and may cause leakage issues. This is the sort of "narrow process window" that requires careful process control to provide high-speed performance without the generation of a few defects in every 10,000 devices (10 FIT reliability).

Defects in the barrier layer can be most easily detected through leakage between minimum spaced metal lines. If the space between metal lines is 0.2mm, and the same interdigitated capacitor is used as described in the previous example, then the area of the sidewall capacitor will be 750µm^2. If an electric field of 7.5MV/cm (150V) is applied across this dielectric, the Fowler-Nordheim leakage current will be on the order of 3.7×10^{-16}A (0.37fA) [5]. However, if there were a defect that allowed the dielectric thickness to be reduced by 50% in an area of 2µm^2, the leakage current through the defect would be 72pA. Thus, the instrumentation should be able to generate a voltage sufficient to produce an electric field of at least 7.5MV/cm across the minimum metal space. If defects smaller than a defect which will reduce the equivalnet oxide thickness by 50% must be detected, then the current sensitivity must be greater than the 72pA value shown in the example, or the forced electric field must be increased. The ability to detect a 25% defect at 150V would require the ability to resolve a leakage of 7.5fA in a defect with an area of 2µm^2.

Cu Electromigration

Initial results of electromigration testing on Cu metal lines indicate that the rate of change of the resistance of the Cu metal line under an electromigration stress will be about one-tenth the rate of change of a similarly stressed Al line. This has led to a belief that Cu is inherently less sensitive to electromigration failure than similarly stressed Al lines. However, Cu does have one area of sensitivity not seen in Al based technology. In the damascene process, the Cu is electroplated into refractory metal lined trenches, then coated with a thin silicon nitride layer [7]. The adhesion of the Cu to the silicon nitride is not strong.

When electromigration occurs in a metal line, metal atoms tend to accumulate at the positively biased end of the line. This accumulation generates a compressive stress in the metal line that is proportional to the current density. If the line under stress is wide and is separated by a minimum space from another wide Cu line, a significant tensile stress is transferred to the small oxide layer separating the two lines. This can lead to the silicon nitride delaminating from the oxide between the metal lines and result in a short between the two metal lines.

Early testing of Cu electromigration has reported a significant rate of failure due to adjacent shorts [9]. Electromigration test results can be confounded by the thermal expansion of the metal at high stress temperatures and by the fact that the ultimate stress generated in a metal line is a function of the stress current density. Therefore, highly accelerated electromigration tests can result in pessimistic predictions of interlevel oxide failures if the ultimate stress achieved by the use condition stress is less than the fracture strength of the oxide. This relationship has not been fully explored at this point. However, the possibility does exist for electromigration stress induced failure of the sidewall dielectric. Declining mechanical strength associated with some low κ dielectric materials may increase the frequency of such fractures.

The strength of the sidewall oxide can be tested quickly using joule heating. The thermal expansion coefficient of Cu is 16.2ppm/°C. The thermal expansion coefficient of SiO_2 is close to 0.3ppm/°C. Heating the line by forcing a high current through it causes it to expand and produces tensile stress in the surrounding oxide layers in a manner similar to that accomplished using the accelerated electromigration tests. The temperature of a line can be measured by the change in resistance of that line. The stress generated by the heating of the line can be calculated from the dimensions and the temperature change. A fast current ramp with a consistent measure of the line resistance/temperature, accompanied by the ability to detect leakage to an adjacent metal line, can be used to measure the strength of the sidewall dielectric. This can be an important process control variable for Cu metallization.

The instrumentation required to perform this test must be able to supply a significant current density in the line. Joule heating of 100°C in a 5µm (wider lines mean more stress) Cu metal line with a sheet resistivity of 0.025Ω/□ sitting on 0.5µm of oxide with a thermal resistance of 0.022°C/Watt/µm/cm^2 will require a current of slightly less than 300mA. A current of about 360mA will be required to raise the temperature by 200°C. (Keep in mind that the line resistance will increase as the line temperature increases, causing greater power dissipation.) This measurement will require multiple probe pads for the forced current, but will be able to provide a measure of the strength of the sidewall oxide in a matter of a few seconds.

The instrumentation required to conduct this measurement must be able to source at least half an amp and to measure voltage with a resolution of at least 1mV.

Conclusions

The instrumentation required to assess the reliability of state-of-the-art semiconductor technology must provide better performance than the instruments used even a few years ago. As we approach the fundamental limits of the materials used to build devices, the process box that will allow building reliable material becomes ever tighter. Controlling 0.18 to 0.1µm processes will demand the ability to measure currents of 1fA or less to create reliable gate dielectrics and interlevel dielectric layers. Additionally, modern instrumentation must significantly reduce the parasitic dielectric absorption effects due to the instrumentation itself. The development of lower resistivity materials such as Cu will require higher current source capability. Currents in the range of 0.5–1A will be useful for characterizing the reliability of the Cu material and the interaction between the Cu and the interlevel dielectric layers. The interaction between Cu and SiO_2 creates a demand for high voltage capability. A voltage of at least 150V is required for 0.18µm processes. Lower voltages will be acceptable as the geometries continue to decrease.

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