

Improved Thermal Stability of Copper Vias Using a Cyclical Stress Test[†]

G.B. Alers¹, J.J. Kuo², G. Harm¹, S.R. Weinzierl², G.W. Ray¹

¹Novellus Systems, 4000 N. First St., San Jose, CA 95060

²Keithley Instruments, Inc., 28775 Aurora Road, Cleveland, OH 44139

Abstract

Via stress migration (VSM) occurs when the relaxation of thermal stresses in copper interconnects causes defects to form under a via [1]. Tests for this phenomenon usually involve measurements of the change in via resistance after an extended bake of 100 to 1000 hours at fixed temperature. The long cycle time for VSM testing delays the feedback loop for process optimization. Isothermal VSM tests also depend on the choice of optimum stress temperature. An alternative VSM test is proposed that cycles temperature through the region of largest creep rate. A 12-hour cyclic test was found to give larger via resistance shifts than a 50-hour isothermal test. Further improvements in the VSM test were obtained by tracking smaller resistance shifts to improve the statistics of the failure rate and reduce wafer-wafer variations. Detection of small via resistance shifts required an electrical test that could measure shifts of less than 0.002Ω without excessive current. The improved via stress migration test has been applied to copper/low- κ structures to identify a new type of failure mode associated with resist poisoning.

Introduction

Stress migration involves a balance between diffusion and thermally induced stress in metal interconnects. At low temperatures, the metal is under high tensile stress from differential thermal contraction relative to the

[†] Presented at the UC Berkeley Extension Advanced Metallization Conference (AMC) 2003, October 21-23, in Montreal, Canada.

dielectric. As temperature is increased, the stress relaxation rate from diffusion increases but the absolute stress decreases. A model has been developed by McPherson and Dunn [2] for the stress induced creep of a metal line embedded in a dielectric. An important parameter in the model is the temperature (T_0) at which the metal transitions from tensile to compressive stress. The creep rate from this model is shown in **Figure 1**. It is a strong function of test temperature and T_0 .

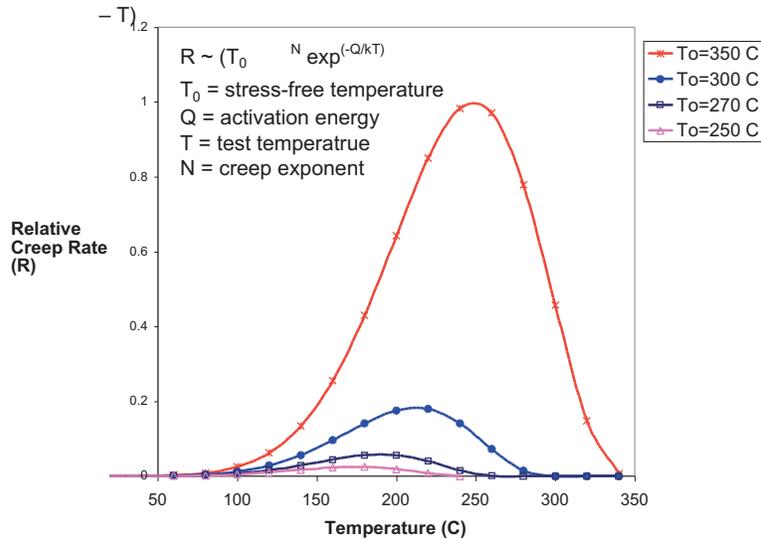


Figure 1: Creep rate and test temperature for a range of stress/temperature cross over points.

The parameter T_0 can depend on the thermal history of the copper and the initial high temperature stress state of the copper [3]. Therefore, the choice of an appropriate test temperature is critical to quantify VSM reliability. Typical test conditions reported in the literature are 168–500 hours [1, 4] at a fixed temperature of 150°C to 300°C. The long anneal time extends the feedback for VSM tests to weeks. A technique that is faster and independent of test temperature would be invaluable to speed the development cycle.

Experiment

In contrast to single temperature tests, a cyclic annealing method can include the full temperature range of high creep rate independent of process condition or thermal history of the copper. The critical temperature range for stress migration is 150°C to 250°C, depending on the stress state of the copper. A furnace was used to cycle temperature slowly four times

from 150°C to 250°C over a period of 12 hours. The heat/cool cycle was dependent on the furnace and was approximately one hour for heating and two hours for the cooling.

The resistance of 120 0.2mm Kelvin vias was measured across a wafer before and after the thermal treatment. A Keithley Instruments S600 Series parametric tester and a fully automatic prober was used for the measurements. The typical via resistance was 0.6Ω and the desired precision for measuring shifts in resistance was 1% or 0.006Ω. This level of precision is a very strict requirement for a parametric tester. The measurement issue is further compounded by limits on the current level per via. Currents larger than ~1mA/cm² risk heating the via and/or damaging it. Requirements for a stress migration test used here were 0.0025Ω/1σ repeatability before and after the thermal stress and less than 0.5mA of current. *Figure 2* shows the repeatability for an optimized Kelvin via resistance test. Repeated measurements of 30 Kelvin via sites were measured over a 30-day period. We find that the repeatability of this Kelvin test is typically within 0.002Ω/1σ. This level of repeatability permits accurate measurement of resistance shifts less than 1% in a via stress migration measurement.

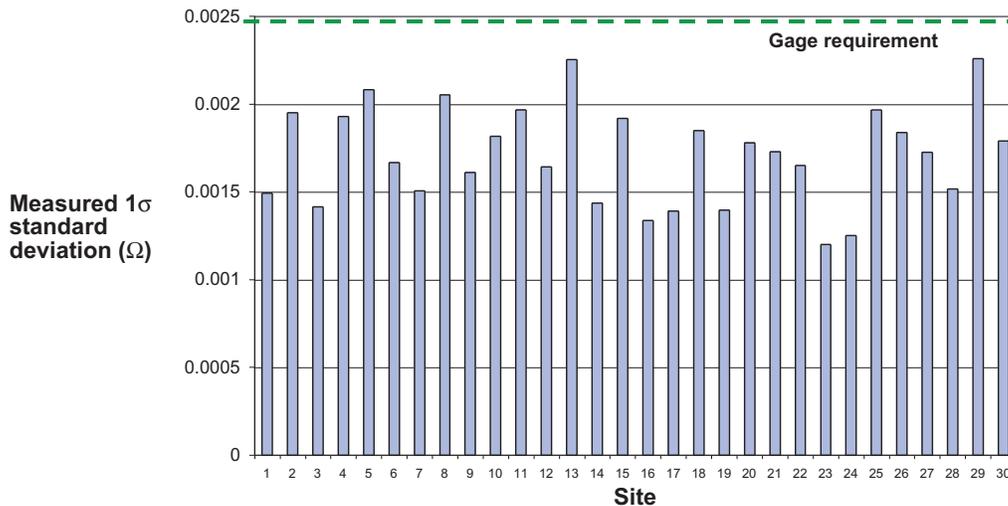


Figure 2: Repeatability of a 30 site/30 day repeatability test for measurements of Kelvin vias with nominal resistance of 0.6Ω.

Using a smaller resistance shift to classify failed vias increases the number of failures and therefore improves the statistics of the test. A single failure criterion helps to compare data from different process variations rapidly and to monitor reliability performance. *Figure 3* shows that adopting a small percent shift (<10%) reduces the wafer-to-wafer spread of the

failure rate because of the increase in number of failed vias. However, the choice of failure criterion can affect conclusions from VSM tests. Limiting the analysis to large resistance shifts (>10%) assures that only large defects contribute to the failure rate but will reduce the number of failed vias. Using a 2% shift as a failure criterion will improve statistics, but might include the wrong types of failures. Failure analysis of vias with large and small resistance shifts is shown in **Figure 4**. The nucleation point of the void is almost always at the lower corner of the via where stress concentration is largest. Once a void nucleates, the driving mechanism for growth is usually the same. Therefore, detection of small resistance shifts early in the VSM process will give an accurate measurement of nucleation density of voids that may eventually grow into open failures.

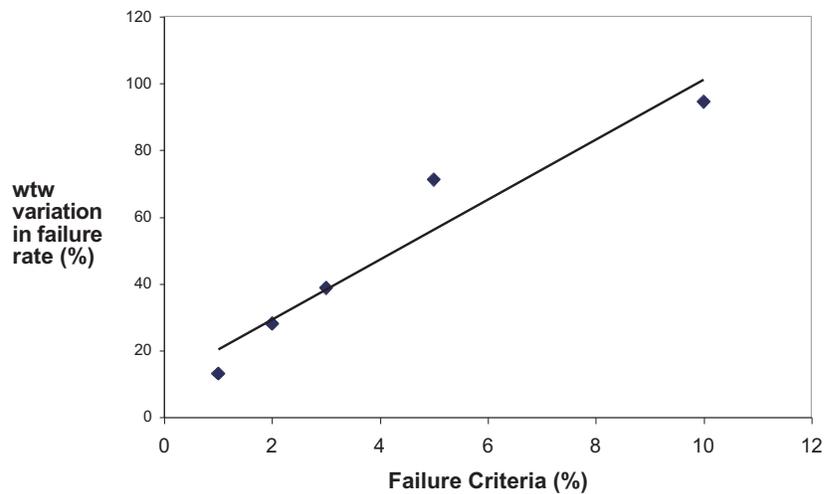


Figure 3: Wafer-to-wafer variation in failure rate as a function of failure criteria for a set of 8 wafers with the same process.

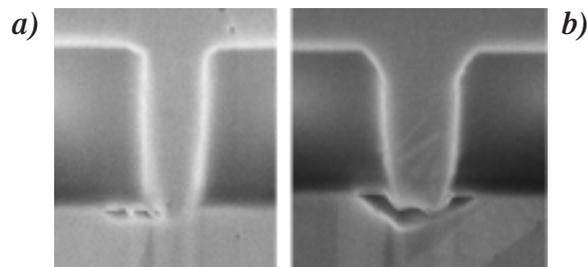


Figure 4: Voids under via after 150°C–250°C cyclic thermal test. Resistance shifts were (a) 1% and (b) 10%. Voids are similar to that observed with static thermal tests.

Results and Discussion

We find that a cyclic test method is able to achieve significant shifts in via resistance after only 12 hours of anneal, whereas a fixed temperature anneal at 200°C shows smaller resistance shifts, even after 50 hours of anneal, as shown in *Figure 5*. Typical VSM voids after the cyclic test are similar to voids observed after static tests as shown in *Figure 4*. The larger resistance shifts with a cyclical test could be a reflection of a non-ideal choice of stress temperature for the isothermal test or that the cyclical test is more effective at creating voids due to the “ratcheting” effect of tensile/compressive stress. Although the cyclic anneal cannot be used to extrapolate lifetime, it does allow for rapid and quantitative screening of stress migration performance.

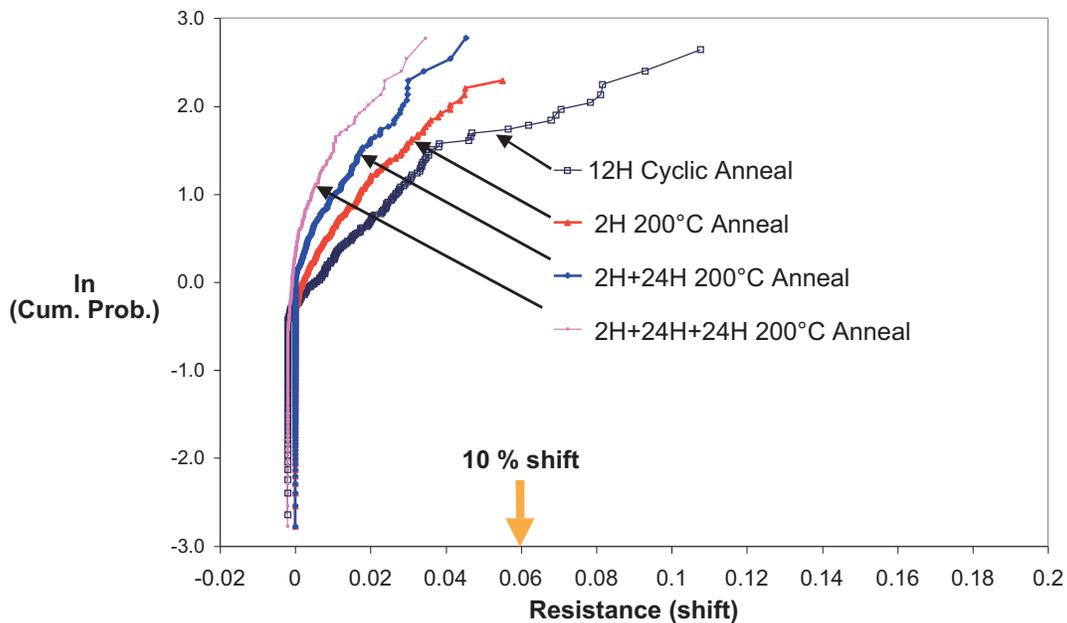


Figure 5: Comparison of a cyclic anneal (150°C–250°C cycle repeated four times over 12 hours) to a fixed temperature anneal at 200°C. Each curve is the sum of three wafers for each test condition.

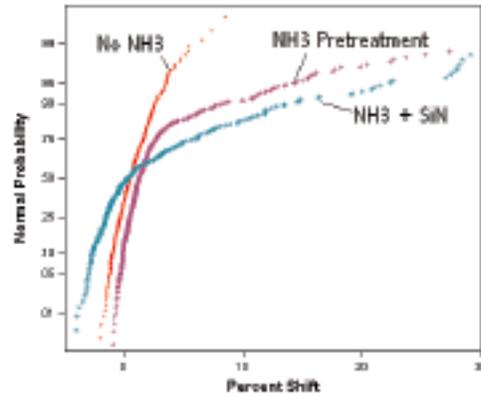


Figure 6: VSM shift for three dielectric diffusion barrier processes with a PECVD low- κ dielectric and isolated Kelvin vias. Each curve is the sum of three wafers.

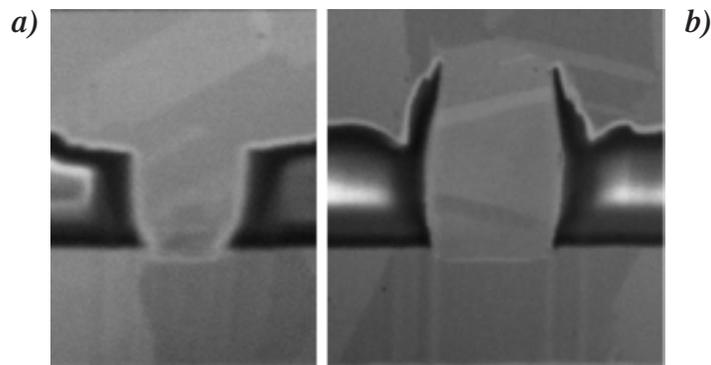


Figure 7: Single Kelvin via profile for the data shown in Figure 4 with no ammonia (a) and ammonia in the bulk film and pretreatment (b). Fence formation around the via is due to poisoned resist near the via.

Another advantage of the cyclical test is that it is less sensitive to the thermal history of the copper. If the low temperature stress state of the copper changes with time (through relaxation) then the zero-stress transition temperature (T_0) will change. This will have a dramatic effect on the creep rate at a fixed temperature as shown in *Figure 1*.

The test procedure described here is sensitive to other process related defects in addition to via voids. *Figure 6* shows the resistance shift of an isolated Kelvin via with copper, PECVD low- κ dielectric and three different dielectric diffusion barrier processes. We find that a barrier process that contains excessive amounts of ammonia has significantly

worse VSM relative to an ammonia free process. Failure analysis showed that the non-optimized barrier process caused poisoning of the photoresist in the region of the via and the formation of “rings” around the via as shown in *Figure 7*. A poor via profile leads to less thermal stability of the via and ultimately a reliability concern. The stress migration test described here was able to detect the presence of problems with the via profile when the via resistance alone did not look anomalous. Subsequent optimization of the ammonia/low-κ process was able to improve the via profile and via stress migration performance was improved.

Conclusion

In conclusion, we have shown that a 12-hour cyclic thermal treatment is as effective as a 50-hour isothermal treatment for inducing resistance shifts in a via stress migration test. These tests require very high precision from the test equipment. We have shown that 0.6Ω Kelvin vias can be measured with a repeatability of better than $0.0025\Omega/1\sigma$ using a low current test. The greater precision of this test allows improved statistics for summarizing via stress migration data by using a smaller failure criterion. We have applied this test to copper/low-κ structures and have identified an additional failure mode associated with via-fence formation.

Acknowledgements

We would like to thank T. Mountsier, M. Sanganeria, R. Shaviv, D. Vitkavage, R. Havemann and M. Kollrack for useful discussions and assistance in processing the wafers.

References

- [1] E.T. Ogawa, J.W. McPherson et al, Proc. Int'l Rel. Phys. Symp., 2002, p. 312.
- [2] J.W. McPherson and C.F. Dunn, J. Vac. Sci. & Tech B5(5), 1987, p.1321.
- [3] S.H. Ree, Y. Du, and P.S. Ho, Proc. Int. Intconnect Tech. Conf. 2001, p 89–92.
- [4] K. Doong, R. Wang et al., Proc. Int'l Rel. Phys. Symp., 2003, p.156.

Specifications are subject to change without notice.

All Keithley trademarks and trade names are the property of Keithley Instruments, Inc. All other trademarks and trade names are the property of their respective companies.



Keithley Instruments, Inc.

28775 Aurora Road • Cleveland, Ohio 44139 • 440-248-0400 • Fax: 440-248-6168
1-888-KEITHLEY (534-8453) • www.keithley.com