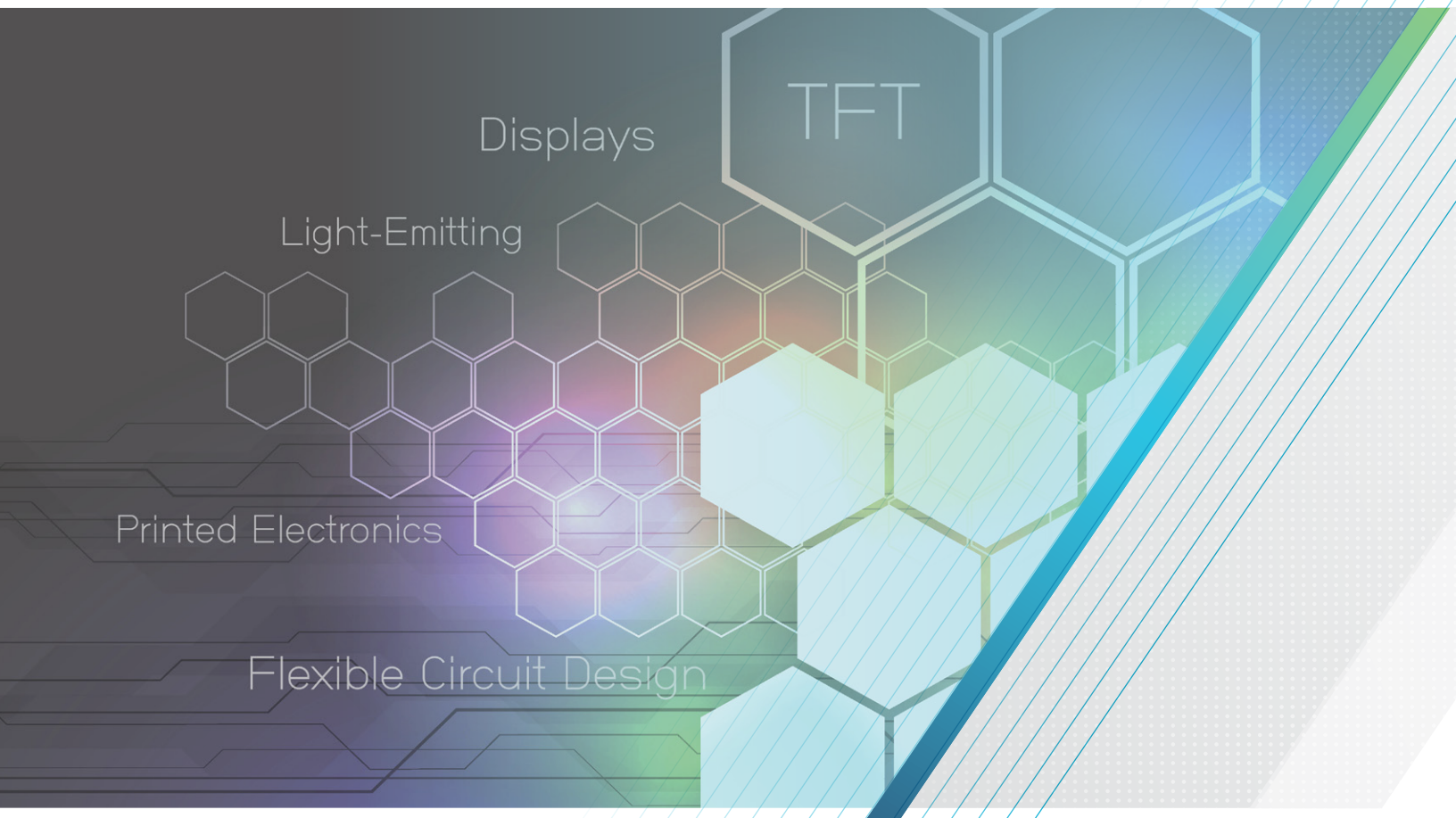
DC I-V and AC Impedance Testing of Organic FETs

APPLICATION NOTE



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Introduction

Organic semiconductor devices have been developed as replacements for traditional semiconductor devices because they use lower cost materials, are less expensive to manufacture, can be printed onto surfaces such as paper and glass, and can be used in flexible circuit designs. These devices are used in a range of applications that includes displays, medical devices, lighting, sensors, memory devices, batteries, and solar cells. One of the most common organic semiconductor devices is the Organic Field Effect Transistor (OFET).

OFET research generally seeks to optimize the performance of the device, such as its carrier mobility and on/off current ratio. DC I-V techniques are used to determine the output and transfer characteristics, hysteresis effects, bias stressing, gate leakage current, etc. AC impedance techniques can reveal critical information about the device, like its carrier mobility, threshold voltage, flat band voltage, and charge effects.

This application note outlines how to optimize DC I-V and AC impedance measurements on OFETs using the 4200A-SCS Parameter Analyzer. Timing parameters, noise reduction, shielding, proper cabling, and other important measurement considerations for achieving the best results will be discussed.

The Organic Field Effect Transistor (OFET)

The OFET is a type of field effect transistor that uses an organic semiconductor material as the channel between the source and drain terminals of the device. The organic thin film transistor (OTFT) is a type of OFET; for this application note, these two FETs will be used synonymously. **Figure 1** illustrates a bottom-gated OFET. The organic semiconductor is placed above a dielectric that sits above the gate terminal. Two metal contacts are located across the top of the organic semiconductor for the source and drain terminals. Connections are made to the three device terminals to perform the electrical measurements.

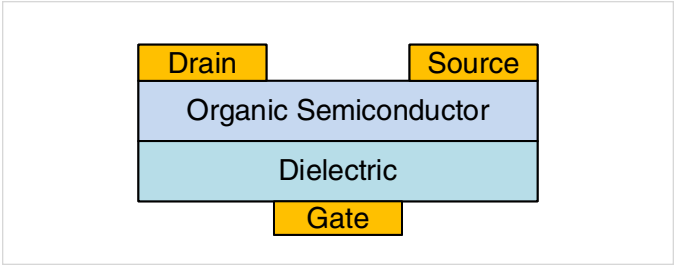

Figure 1. Bottom-gated organic field effect transistor.

Making Electrical Measurements with the 4200A-SCS

The 4200A-SCS system includes tests for making some of the most commonly used electrical measurements on organic FETs. These tests for making DC I-V, very low frequency C-V, and high frequency C-V measurements can be found in the Test Library by searching on the keyword “ofet” or “organic” while in the Select view of the Clarius software. All these tests can also be found in the Organic FET Characterization Project (*ofet*) in the Project Library using the keyword, “ofet” or “organic” in the Search field. **Figure 2** shows a screen capture of this project. In addition to the provided tests, the user can also easily create their own tests and projects based on their application and measurement requirements.

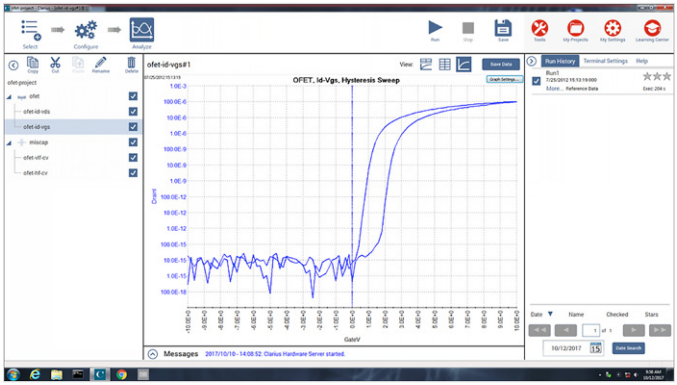

Figure 2. Screen capture of Organic FET Characterization Project.

Current-Voltage Measurements

The I-V characteristics of an organic device can be used to extract many of the device's parameters, study the effects of fabrication processes, and determine the quality of the contacts. The Test Library and Organic FET Characterization project includes tests to measure the output characteristics (I_D-V_{DS}) and transfer characteristics (I_D-V_{GS}) of an OFET.

Figure 3 illustrates a DC I-V test configuration for measuring the transfer characteristics of an OFET using two 4200-SMUs with optional 4200-PA preamps. These SMUs are capable of sourcing and measuring both current and voltage. They have pico-amp sensitivity and can be current-limited to prevent damage to the device. In this diagram, SMU1 is connected to the gate of the OFET and SMU2 is connected to the drain terminal. The source terminal is connected to the ground unit (GNDU) or it can be connected to a third SMU if it is necessary to source and measure from all three terminals of the OFET.

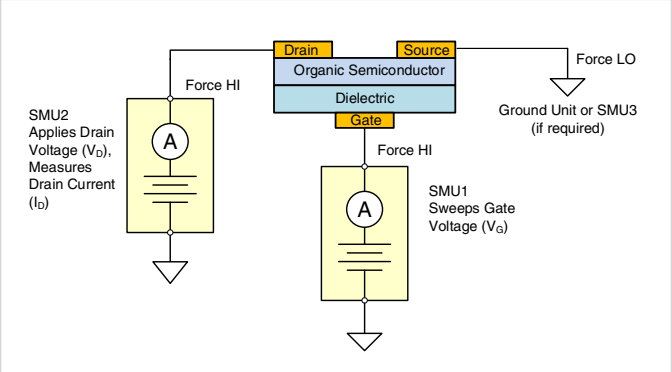

Figure 3. Circuit diagram for measuring the DC I-V characteristics of an OFET.

Once the SMUs are connected to the OFET, the transfer characteristics can be generated using the Organic FET Drain Current vs. Gate Voltage (*ofet-id-vgs*) test in the Test Library. In this test, SMU2 applies a constant drain voltage (V_D) and measures the drain current (I_D) while SMU1 sweeps the gate voltage (V_G). **Figure 4** shows the results of measuring the drain current as a function of the gate voltage of an OFET. The hysteresis sweep is performed using the Dual Sweep function in the software. Notice the many decades of current—from femto-amps to milli-amps—that the 4200-SMUs with preamps can measure.

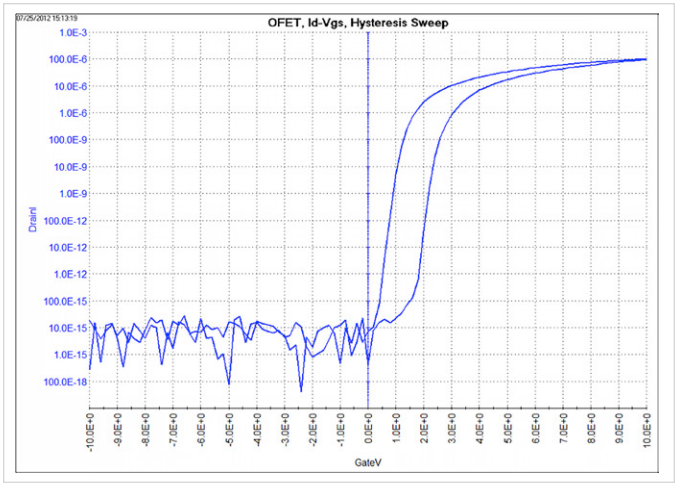

Figure 4. ID-VGS curve of an OFET.

The SMUs connected to each terminal of the OFET can be easily reconfigured in the Clarius software to perform other tests. The output characteristics, I_D vs. V_D, can also be measured by changing the SMU parameters in the software. It's also possible to use the preconfigured Organic FET Output Characteristics (*ofet-id-vds*) test in the Test Library. By stepping the gate voltage and measuring the drain current as a function of drain voltage, a drain family of curves can be generated. **Figure 5** shows the results of measuring I_D-V_{DS} curves of a p-type OFET using the *ofet-id-vd*s test.

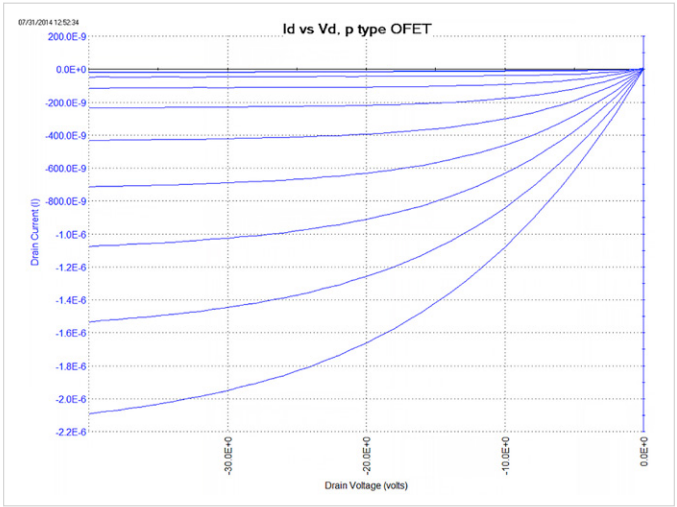

Figure 5. Output Characteristics of a p-type OFET.

Optimizing DC I-V Measurements

The following techniques will improve the quality of DC measurements made on organic FETs with the 4200A-SCS:

Eliminate Lead and Contact Resistance: The series resistance of the cables used to connect the SMU to the device can cause measurement errors. The effects of the cable resistance are particularly detrimental when using long connecting cables and high currents because the voltage drop is significant compared to the measured voltage.

As shown in **Figure 6**, the voltage drop due to the cable resistance is added to the voltage measurement of a DUT when making 2-wire, or local sense, connections. In this case, the current flows across both cables, as well as the DUT, causing three voltage drops that all are measured by the SMU voltmeter. To eliminate the cable resistance from the measurement, a 4-wire or remote sense connection is made to the device, as shown in the right half of **Figure 6**. In this case, only the voltage drop across the DUT is measured by the SMU voltmeter.

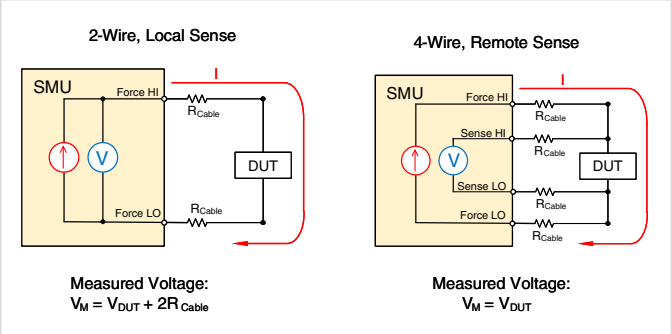

Figure 6. Local vs. Remote Sense.

Minimize Noise in Measurements: Noise may be generated from a variety of sources, including AC pickup and electrostatic interference. Noisy measurements result when a noise source is superimposed on the DC signal being measured. This can result in inaccurate or fluctuating measurements.

The most common form of external noise pickup is 60 Hz (or 50 Hz) line cycle pickup. This can be a common occurrence near fluorescent lights. Millivolts of noise are not uncommon. Keithley uses a technique called Line-Cycle Integration to minimize the effects of 60 Hz (or 50 Hz) line pickup. Line-cycle noise will average out when the integration time, or measurement window, is equal to an integral number of power line cycles. This A/D aperture time (measurement window) can be adjusted using the Speed setting in the Test Settings pane.

Electrostatic interference is another cause of noisy measurements when measuring low currents. This coupling occurs when an electrically charged object approaches the circuit under test. In high impedance circuits, this charge doesn't decay rapidly and can result in unstable measurements. The erroneous readings may be due to either DC or AC electrostatic fields, so electrostatic shielding will help minimize the effects of these fields.

An electrostatic shield can be just a simple metal box that encloses the test circuit. However, this can be difficult when working within a laboratory glove box, which is often used with organic devices. Probe stations often include an electrostatic/EMI shield or optional dark box. As shown in **Figure 7**, the shield surrounds the device and is connected to the measurement circuit LO, which is the Force LO terminal of the SMU. The Force LO terminal is the outside shield of the triax cable of the 4200-SMU and is also located on the rear panel of the 4200A-SCS in the ground unit (GNDU). All cables need to be low noise and shielded. Each 4200-SMU and 4210-SMU comes with two low noise triax cables.

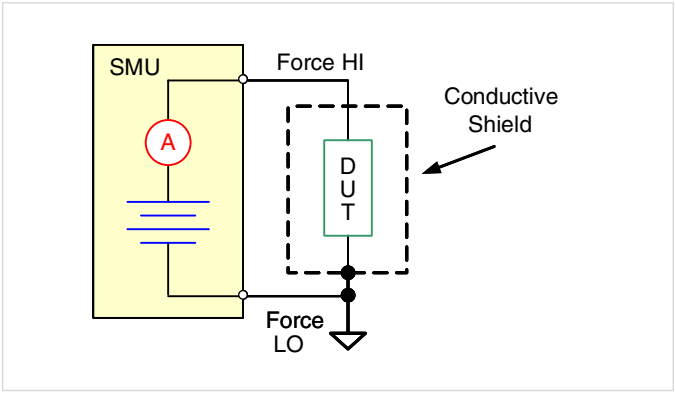

Figure 7. Conductive Shield Surrounds Device Under Test.

Provide Sufficient Settling Time: Because device leakage current usually involves measuring very low current (<1 nA), it is important to allow sufficient settling time to ensure the measurements are stabilized after a voltage bias has been applied. Some of the factors that affect the settling time of

the measurement circuit include the cables, test fixtures, switches, probers, the DUT resistance and capacitance, and the current range of the SMU. To ensure settled readings, additional delay time can be added to the voltage step prior to the measurement. This delay time can be easily adjusted in the Test Settings pane in the Clarius software.

Very Low Frequency Capacitance-Voltage Technique

In addition to measuring very small currents, two SMUs with preamps can be used to measure Very Low Frequency C-V (VLF C-V). C-V sweeps and C-t measurements can be made with test frequencies from 10 mHz to 10 Hz. **Figure 8** is a simplified diagram of the two-SMU configuration used to generate low frequency impedance measurements. This configuration requires a 4200A-SCS Parameter Analyzer with two SMUs and two 4200-PA preamps with one connected to either side of the device under test. SMU1 outputs the DC bias with a superimposed AC signal and measures the voltage. SMU2 measures the resulting AC current while sourcing 0V DC.

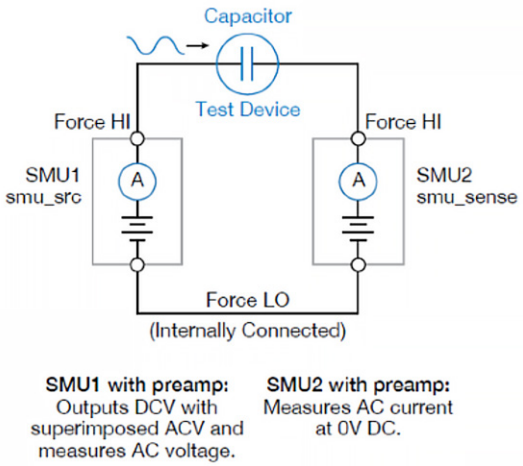

Figure 8. Connections for Very Low Frequency C-V measurements.

While the voltage is forced, voltage and current measurements are obtained simultaneously over several cycles. The magnitude and phase of the DUT impedance is extracted from the discrete Fourier transform (DFT) of a ratio of the resultant voltage and current sinusoids. The narrow-band information can be collected at varying frequencies (10 mHz to 10 Hz) to measure the complex impedance of the DUT. The resulting output parameters include the impedance (Z), phase angle (θ), capacitance (C), conductance (G), resistance (R), reactance (X), and the dissipation factor (D).

Because the very low frequency method works only over a limited frequency range, the capacitance of the device under test (DUT) should be in the range of 1 pF to 10 nF. **Table 1** summarizes the VLF C-V specifications. Complete specifications and more detailed information about this technique can be found in a Keithley application note, "Performing Very Low Frequency Capacitance-Voltage Measurements of High Impedance Devices Using the 4200A-SCS Parameter Analyzer."

Table 1. Typical Measurement Accuracy[2]

Frequency	Measured Capacitance	C Accuracy @ 300 mV rms[1]	C Accuracy @ 30 mV rms[1]
10 Hz	1 pF	10%	13%
	10 pF	10%	10%
	100 pF	5%	5%
	1 nF	5%	9%
	10 nF	5%	5%
1 Hz	1 pF	2%	2%
	10 pF	1%	2%
	100 pF	2%	1%
	1 nF	2%	1%
	10 nF	2%	2%
100 mHz	1 pF	2%	3%
	10 pF	2%	2%
	100 pF	2%	2%
	1 nF	1%	2%
	10 nF	2%	1%
10 mHz	1 pF	5%	10%
	10 pF	1%	2%
	100 pF	1%	1%
	1 nF	1%	1%
	10 nF	2%	2%

NOTES

1. ±20V maximum includes the DC Bias and the AC Test Signal peak voltage. Maximum negative bias voltage = –20 + (AC voltage * $\sqrt{2}$). Maximum positive bias voltage = 20 – (AC voltage * $\sqrt{2}$).
2. Test device must have dissipation factor D_X <0.1. All data shown for DC Bias voltage = 0V.

All specifications apply at 23°C ±5°C, within one year of calibration, RH between 5% and 60%, after 30 minutes of warmup.

VLF C-V Characterization of Organic FETs

The built-in software for performing VLF C-V measurements can be used on different types of devices, including organic FETs and MIS capacitor devices. **Figure 9** shows the results of performing a C-V sweep with a test frequency of 0.25 Hz on an OFET between the gate and drain terminals using the Organic FET Very Low Frequency C-V Sweep (*ofet-vlf-cv*) test in the Test Library.

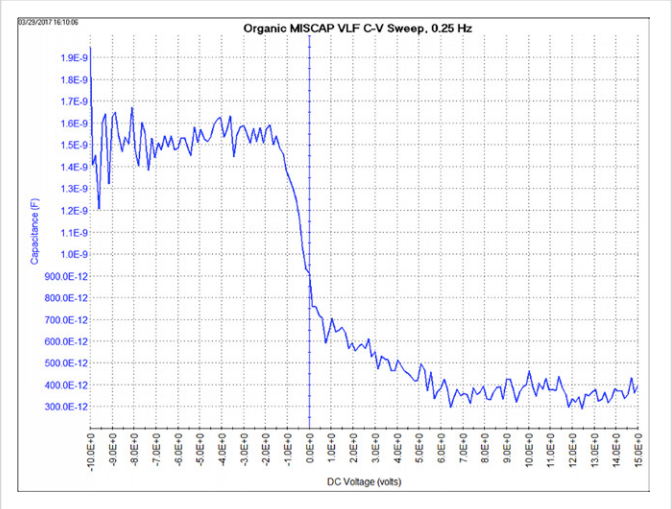

Figure 9. A Very Low Frequency C-V Sweep of an OFET at a Test Frequency of 0.25 Hz.

High Frequency Capacitance-Voltage Measurements

In addition to DC I-V and VLF C-V measurements, measuring the capacitance of an OFET can provide information about the device, including the gate capacitance and the carrier mobility. **Figure 10** shows the connections of the 4210-CVU Capacitance Voltage Unit to an OFET. In this configuration, the gate-to-drain capacitance is measured as a function of the gate voltage.

Figure 10. Connections from the 4210-CVU to an OFET.

Using the Organic FET C-V Sweep (*ofet-hf-cv*) test in the Test Library, a C-V sweep from –10 V to 10 V at 50 kHz was generated on an OFET between the gate and drain terminals. The results of the C-V sweep are shown in **Figure 11**.

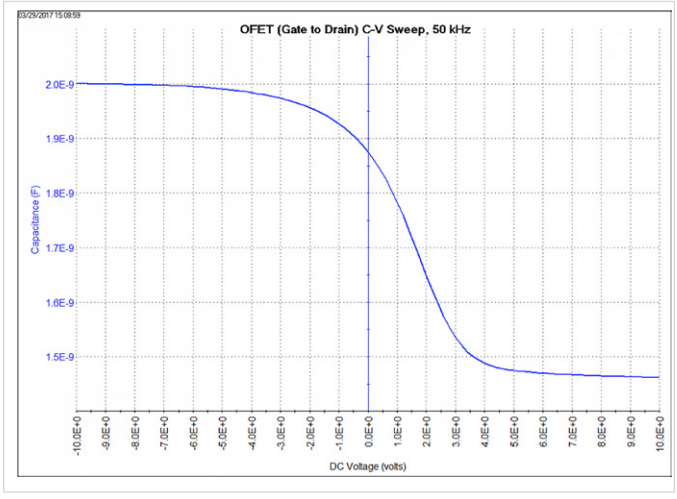

Figure 11. High Frequency C-V Sweep of an OFET.

Optimizing Capacitance Measurements

To improve the quality of capacitance measurements made with the 4200A-SCS, follow these guidelines:

Perform Open Compensation (for measurements <10 pF): The open correction feature compensates for capacitance offsets in the cabling and connections. Performing the correction is a two-part process. The corrections are performed, and then they are enabled within a test.

To perform the corrections in the Clarius software, select *Tools* at the top of the screen and select *CVU Connection Compensation*. For an Open correction, select *Measure Open*. Probes must be up or the DUT removed from the test fixture. Once the correction data is acquired from the Tools menu, the correction is enabled within a test by selecting *Open Compensation* in the Terminal Settings pane.

Choose Appropriate Hold and Sweep Delay Times: The condition of a device when all internal capacitances are fully charged after an applied voltage step is referred to as “equilibrium.” If capacitance measurements are made before the device is in equilibrium, the results of these measurements may be inaccurate.

To choose the appropriate delay times, apply DC voltage to the device using the Sampling Test Mode, and plot the capacitance as a function of time. Observe the settling time from the graph. This observed equilibrium time can be used as the Hold Time, which is the time the Presoak Voltage is output prior to the beginning of the Sweep or Sampling Operation Mode. The observed time can also be used for the Sweep Delay time applied for each step in the sweep. The Sweep Delay time may not need to be as long as the Hold Time. The user will need to experiment to verify the appropriate times to use in the Test Settings pane for a particular test.

Use Proper Shield Connections: When measuring AC impedance at test frequencies greater than 1 MHz, connect the shields of the coax cables together as close as possible to the device. This reduces the loop area of the shields, which minimizes the inductance. This also helps to maintain the transmission line effects. If the shields are not connected together, offsets may occur.

Choose the Appropriate Speed Mode in the Test Settings Window: The Speed Mode function allows adjusting the settling time and measure window (A/D aperture) of the measurements. For small capacitances, use the Quiet or Custom Speed modes for best results.

Conclusion

Appropriate instrumentation and measurement techniques make it possible to achieve optimal electrical characterization of organic FETs. The 4200A-SCS is an ideal tool for performing electrical characterization of OFETs because of its integrated hardware, interactive software, and analysis capabilities. The test system includes built-in tools, such as open correction, informational videos, the Help function, and timing controls to help researchers minimize set-up time and achieve the best measurement results as quickly as possible.

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