Technical Reference

Tektronix

DPOJET Opt. PCE, PCE3, PCE4
PCI Express® Measurements & Setup Library
Methods of Implementation (MOI) for Verification, Debug and Characterization

Version 4.6

077-0267-00

www.tektronix.com

DPOJET PCI Express MOI

Contacting Tektronix

Tektronix, Inc.
14200 SW Karl Braun Drive or P.O. Box 500
Beaverton, OR 97077 USA

For product information, sales, service, and technical support:

- In North America, call 1-800-833-9200.
- Worldwide, visit www.tektronix.com to find contacts in your area.

Revision History			
Version	**Issue Date**	**Pages**	**Nature of Change**
1.0	Dec-2008	All	First released MOI for PCI Express
2.0	Aug-2009	3,8-9,12,18, 34-38,	MXM test points added in setup library. Updated Algorithms for new measurements.
3.0	March-2012		Added PCI Express 3.0 MOI
4.0	March-2013		Updated to support new SDLA
4.1	May-2013		Added R11_RefClk setup details
4.2	July-2013		Added Rev. 2.0 & 3.0 Ref Clock Setup details, VBoost measurement, Gen2 Cable support.
4.3	Oct-2014	36, 10-32, 3-6, 44, 56, 58-61, 66	Updated probing configurations for Rev3.0 CEM Specification System Board in the - Table 16 and DPOJET Settings is modified for Unit interval measurement, updated table 2 and 3 according to Base spec 3.0, PCIe AC Common Mode setup files added.
4.4	Apr-2015	4,5, 33, 35, 40, 42	Added PCI Express 4.0 Base Spec Measurements and limits, Setup files(table 16), Required Equipment, Horizontal setup(4.3.1), Math setup(4.3.3)
4.5	Jun-2015	All	Incorporated review comments
4.6	Mar-2016	78-102, 118	Added Ref Clock Measurement in MOI Added Compliance Pattern description as Appendix d

Contents

Figure Table:

1 Introduction to the DPOJET PCI Express Setup Library[1]

This document provides the procedures for taking PCI Express measurements with Tektronix DPO/DSA70000 Series Oscilloscopes with DPOJET (Jitter and Eye Analysis Tools) and probing solutions.

DPOJET and its PCI Express Setup Library provide transmitter path measurements (amplitude, timing, and jitter), waveform mask, and limits testing described in multiple variants of the PCI Express specifications.

Table 1 – Supported Specifications in the DPOJET Setup Library

PCI Express Specification Title	Test Points Defined
Base Specification	Transmitter & Receiver (Section 4.3)
CEM Specification	System and Add-In Card (Section 4.7) Reference Clock (Section 2.1)
MXM Specification	System and Module(0 & 3.5dB DeEmphasis)(Section 2.4 & 2.5)
Ref Clock Specification	Reference Clock(Section 2.6)
Express Module Specification	Transmitter Path and System Board (Section 5.4)
PCMCIA Express Card Standard	Host System Transmitter Express Card Transmitter (Section 4.2.1.2)
External Cabling Specification	Transmitter and Receiver Path (Section 2.12 & 2.13)
External Cabling Specification	Transmitter and Receiver Path (Section 2.12 & 2.13)

[1] **Disclaimer:** The tests provided in DPOJET (which are described in this document) do not guarantee PCI Express compliance. The test results should be considered "Pre-Compliance". Official PCI Express compliance and PCI-SIG Integrator List qualification is governed by the PCI-SIG (Special Interest Group) and can be achieved only through official PCI-SIG sanctioned testing.

PCI Express Specification Title	Test Points Defined
Base Specification	Transmitter & Receiver (Section 4.4) Mobile Low Power Transmitter (Section 4.4)
CEM Specification	System and Add-In Card (3.5 & 6dB DeEmphasis) (Section 4.7)
MXM Specification	System and Module(0 & 3.5dB DeEmphasis)(Section 2.4 & 2.5)
Base Specification	Transmitter (Table 3)
CEM Specification	System and Add-In Card (Table 5 & 6)
Gen2 & Gen3 Ref Clock Specification	Reference Clock(Section 2.6, Table 7B & 7C)
Gen4 Base Specification	Table 3- Specific PCI Express 4.0 Base transmitter measurements

Refer to http://www.pcisig.com/specifications/pciexpress/ for the latest specifications.

In this document, for all references to the PCI Express Base Specifications and Card Electrical Mechanical (CEM) specifications, refer to all versions of the specifications. (Rev 1.1, 2.0, and 3.0, 4.0). Differences between the specifications are specifically called out when appropriate.

In the subsequent sections, step-by-step procedures are described to help you perform PCI Express measurements. Each measurement is described as a Method of Implementation (MOI). For further reference, consult the Compliance checklists and tools offered to PCI-SIG members at www.pcisig.com.

2 PCI Express Specifications

As shown in Table 2, Electrical Specifications for PCI Express are provided in multiple documents. This section provides a summary of the measurement parameters measured in the DPOJET Setup Library module and how they are related to the symbol and test limits in the specification.

2.1 Differential Transmitter (TX) Output Specifications

The following table shows the available measurements in the PCE Module and their test limits defined in each of the Base Specifications.

Table 2- Supported Base Specification transmitter measurements

Parameter	Symbol(s)	DPOJET Measurement	Specification		
			2.5GT/s Rev1.1/Rev2.0	5.0 GT/s Rev2.0	8.0 GT/s Rev3.0
Clock Recovery	NA	See Setup by Data Rate >>	1st Order PLL Fc: 1MHz *Emulates 1st Order filter at 1.5MHz with 75% edge density of Compliance Pattern*	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz - And - 3rd Order LPF Fc: 1.5MHz *Emulates Step Function Filter at 1.5MHz*	1st Order PLL Fc: 10MHz *Assumes Scrambled Compliance Pattern with 50% Edge Density*
Unit interval	UI	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	124.9625 (min) 125.0375 (max)
Differential p-p TX voltage swing	VTX-DIFF-PP	PCIe T-Tx-Diff-PP	0.8 V (min) 1.2 V (max)	0.8 V (min) 1.2 V (max)	Refer Table 3
Low power differential p-p TX voltage swing	VTX-DIFF-PP-Low	PCIe T-Tx-Diff-PP	0.4 V (min) 1.2 V (max)	0.4 V (min) 1.2 V (max)	Refer Table 3
De-emphasized output voltage ratio of -3.5dB	VTX-DE-RATIO-3.5dB	PCIe T/nT Ratio	-3.0 dB (min) -4.0 dB (max)	-3.0 dB (min) -4.0 dB (max)	Not Specified
De-emphasized output voltage ratio of -6dB	VTX-DE-RATIO-6dB	PCIe T/nT Ratio	Not Applicable	-5.5 dB (min) -6.5 dB (max)	Not Specified
Instantaneous lane pulse width	TMIN-PULSE	PCIe Tmin-Pulse	Not Specified	0.9UI (min) *150 ps (min)*	Not Specified
Transmitter eye including all jitter sources	T_{TX-EYE}	For Rev1.1: Eye Width For Rev2/3: PCIe T-TX	.75 UI (min) *300 ps (min)*	.75 UI (min) *150 ps (min)*	Refer Table 3

Parameter	Symbol(s)	DPOJET Measurement	Specification		
			2.5GT/s Rev1.1/Rev2.0	5.0 GT/s Rev2.0	8.0 GT/s Rev3.0
Maximum time between the jitter median and maximum deviation from the median	TTX-EYEMEDIAN-to-MAXJITTER	PCIe Med-Mx Jitter	.125 UI (min/max)	Not Specified	Not Specified
Deterministic jitter	TTX-DJ-DD	DJ–δδ	Not Specified	0.15 UI (max) *30 ps (max)*	TBD
Tx RMS jitter < 1.5MHz	TTX-LF-RMS	TIE1 Jitter 3rd Order LPF Fc: 1.5 MHz Std. Deviation	Not Specified	3.0 ps (max)	Not Specified
D+/D- TX output rise/fall Time [2]	$T_{TX-RISE}$ $T_{TX-FALL}$	PCIe T-Tx-Rise PCIe T-Tx-Fall	0.125 UI (min) *50 ps (min)*	0.15 UI (min) *30 ps (min)*	Not Specified
Tx rise/fall mismatch	TRF-MISMATCH	PCIe T-RF-Mismch	Not Specified	0.1 UI (max)	Not Specified
Tx AC peak-peak Common mode voltage	VTX-CM-AC-PP	Common Mode Pk-Pk	Not Specified	100 mV (max) (no more than 100 mVPP in 0.03 500 MHz range) or 150 mV (max)	50 mV (max) (no more than 50 mV in 0.03-500 MHz range) or 150 mV (max)
Tx AC peak Common mode voltage	VTX-CM-AC-P	Common Mode Rev1.1 : StdDev	20mV RMS (max)	Not Specified	Not Specified
Absolute delta of DC common mode voltage between D+ and D-	$V_{TX-CM-DC-LINE-DELTA}$	Common Mode Mean	0 V (min) 25 mV (max)	0 V (min) 25 mV (max)	0 V (min) 25 mV (max)
Pk-Pk Refclk jitter for common Refclk Rx architecture, Gen1	TREFCLK	T-REFCLK	86 ps		
RMS Refclk HF jitter for common Refclk Rx architecture, Gen2	TREFCLK-HF-RMSCC	T-HF-RMSCC-RCLK		3.1 ps RMS	
RMS Refclk LF jitter for common Refclk Rx architecture , Gen2	TREFCLK-LF-RMSCC	T-LF-RMSCC-RCLK		4.0 ps RMS	

[2] Rise/Fall time measurements in DPOJET are compliant to the Rev1.0a and Rev1.1 specification. For Gen2, rise and fall time is limited to TF2 and TR2 as defined in section 4.3.3.8 of the Base Specification

Parameter	Symbol(s)	DPOJET Measurement	Specification		
			2.5GT/s Rev1.1/Rev2.0	5.0 GT/s Rev2.0	8.0 GT/s Rev3.0
RMS Refclk HF jitter for data clocked Rx architecture, Gen2	TREFCLK-HF-RMS-DC	T-HF-RMSDC-RCLK		4.0 ps RMS	
RMS Refclk LF jitter for data clocked Rx architecture, Gen2	TREFCLK-LF-RMS-DC	T-LF-RMSDC- RCLK		7.5 ps RMS	
RMS Refclk jitter for common Refclk Rx architecture	TREFCLK-RMS-CC	T-REFCLK-RMS-CC			1.0 ps RMS
RMS Refclk jitter for data clocked Rx architecture	TREFCLK-RMS-DC	T-REFCLK-RMS-DC			1.0 ps RMS
RMS Refclk jitter for separate Refclk independent SSC architecture	TREFCLK-RMS-SRIS	T-REFCLK-RMS-SRIS			0.5 ps RMS

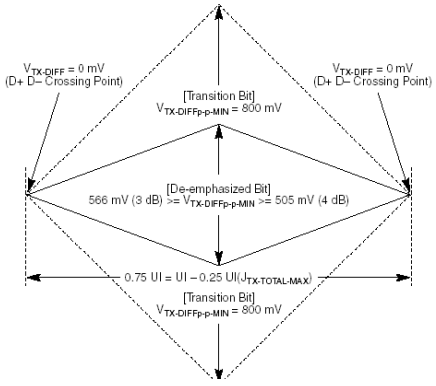
Table 3- Specific PCI Express 4.0 Base transmitter measurements

Parameter	Symbol(s)	DPOJET Measurement	8.0 GT/s Rev3.0	16.0 GT/s Rev0.5
Clock Recovery	NA	See Setup by Data Rate >>	1st Order PLL Fc: 10MHz Assumes Scrambled Compliance Pattern with 50% Edge Density	1st Order PLL Fc: 10MHz Assumes Scrambled Compliance Pattern with 50% Edge Density
Full Swing Tx voltage with noTxEq	VTX-FS-NO-EQ	V-TX-NO-EQ	1300 mV(max) 800 mV(min)	1300 mV(max) 800 mV(min)
Reduced Swing Tx voltage with noTxEq	VTX-RS-NO-EQ	V-TX-NO-EQ	1300 mV(max)	1300 mV(max)
Min swing during EIEOS for full swing	VTX-EIEOS-FS	V-TX-EIEOS	250 mV(min)	250 mV(min)
Min swing during EIEOS for reduced swing	VTX-EIEOS-RS	V-TX-EIEOS	232 mV(min)	232 mV(min)
Pseudo package loss Root device	ps21TXRootdevice	ps21TXRootdevice	-3.0dB(min)	-3.0dB(min)
Pseudo package loss AIC device	ps21TXAICdevice	ps21TXAICdevice	NA	-5.0dB(min)
Tx uncorrelated total jitter	TTX-UTJ	T-TX-UTJ	31.25ps(max)	12.5ps(max)

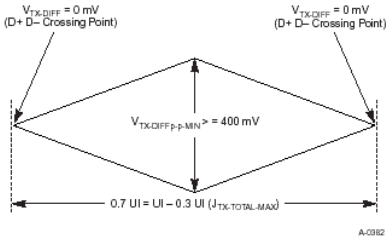
Parameter	Symbol(s)	DPOJET Measurement	8.0 GT/s Rev3.0	16.0 GT/s Rev0.5
Tx uncorrelated deterministic jitter	TTX-UDJDD	T-TX-UDJDD	12ps(max)	6.25ps(max)
Data dependent jitter	TTX-DDJ	T-TX-DDJ	18ps(max)	NA
Total uncorrelated PWJ	TTX-UPW-TJ	T-TX-UPW-TJ	24ps(max)	12.5ps(max)
Deterministic DjDD uncorrelated PWJ	TTX-UPW-DJDD	T-TX-UPW-DJDD	10ps(max)	5ps(max)
Maximum Boost voltage ratio for full swing	V-TX-BOOST-FS	V-TX-BOOST	8dB(min)	8dB(min)
Maximum Boost voltage ratio for reduced swing	V-TX-BOOST-RS	V-TX-BOOST	2.5dB(min)	2.5dB(min)

2.2 Differential Transmitter (TX) Compliance Eye Diagrams

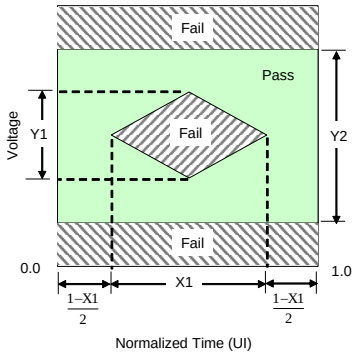
Figure 1a shows the eye mask definitions for the Rev1.1 Base Specification. It provides an example of a transmitter mask for a signal with de-emphasis. Transition and non-transition bits must be separated to perform the mask testing. The amplitude and jitter mask geometries are derived from the amplitude and jitter specifications. Low power transmitter variants in both Gen1 and Gen2 do not use de-emphasis (This is shown in Figure 1b).



1. **Rev1.1/2.0 Transmitter eye masks for transition and non-transition bits**



2. **Rev1.1/2.0 transmitter eye mask for low power variant where de-emphasis is not used**



3. **Rev3.0 transmitter eye mask definition – Mask Geometries TBD for Gen3.**

Figure 1: PCI Express Transmitter Eye Mask Definitions

2.3 Differential Receiver (RX) Input Specifications

The following table shows the available measurements in the PCE Module and their test limits defined in each of the Base specifications.

Table 4 – Supported base specification receiver measurements for Gen1 and Gen2

Parameter	Symbol	DPOJET Measurement	2.5GT/s Rev1.1/Rev2.0	5.0 GT/s Rev2.0
Clock Recovery	NA	See Setup by Data Rate >>	1st Order PLL Fc: 1MHz *Emulates 1st Order filter at 1.5MHz with 75% edge density of Compliance Pattern*	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz - And - 3rd Order LPF Fc: 1.5MHz *Emulates Step Function Filter at 1.5MHz*
Unit interval	*UI*	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	399.88 (min) 400.12 (max)	199.94 (min) 201.06 (max)
Minimum receiver eye height	V_{RX_EYE}	PCIe T-Tx-Diff-PP	.175 V (min) 1.2 V (max)	.120 V (min) 1.2 V (max)
Minimum receiver eye width	T_{RX-EYE}	For Rev1.1: Eye Width For Rev2: PCI T-TX	.40 UI (min) *160ps (min)*	Not Specified
Receiver deterministic jitter – Dj	$T_{RX\_DJ\_DD}$	DJ–δδ	Not Specified	.30 UI (max) *60 ps (max)*
Minimum width pulse at Rx	$T_{RX-MIN-PULSE}$	PCIe Tmin-Pulse	Not Specified	.60 UI (min) *120ps (max)*
Maximum time between the jitter median and maximum deviation from the median.	$T_{TX-EYEMEDIAN-to-MAXJITTER}$	PCIe Med-Mx Jitter	.30 UI (max)	Not Specified
Rx AC common mode voltage	$V_{RX-CM-AC-P}$	Common Mode Rev2/3 : Pk-Pk	150mV	150mV

Differential Receiver (RX) Eye Diagrams

Figure 2 shows the receiver eye mask definitions for the Rev1.1 Base Specification. The amplitude and jitter mask geometries are derived from the amplitude and jitter specifications.

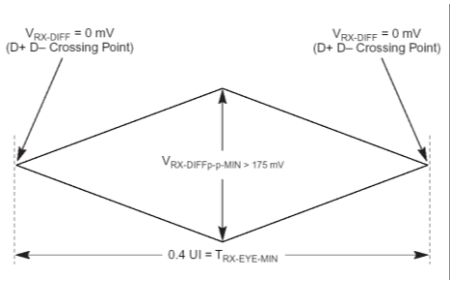


Figure 2: Receiver input eye mask

2.4 Add-In Card Transmitter Path Compliance Specifications

Table 5 is derived from the Card Electrical Mechanical Specifications (CEM). See the CEM Specification for additional notes and test definitions.

Table 5 – Supported CEM add-in card measurements

Parameter	Symbol	DPOJET Measurement	2.5GT/s Rev1.1/Rev2.0	5.0 GT/s Rev2.0	8.0 GT/s Rev3.0
Clock Recovery	NA	See Setup by Data Rate >>	1st Order PLL Fc: 1MHz Emulates 1st Order filter at 1.5MHz with 75% edge density of Compliance Pattern	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz - And - 3rd Order LPF Fc: 1.5MHz Emulates Step Function Filter at 1.5MHz	1st Order PLL Fc: 10MHz
Unit interval	UI	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	399.88 (min) 402.12 (max)	199.94 (min) 200.06 (max)	124.9625 (min) 125.6625 (max)
Differential P-P Voltage	VDiff-PP	PCIe VTx-Diff-PP	Not Specified	Not Specified	50mV (min) 1200mV(max)
Eye height of transition bits	VTXA	Eye Height1	0.514 V (min) 1.2 V (max)	3.5dB De-emphasis .380 V (min) 1.2 V (max) 6.0dB De-emphasis .306 V (min) 1.2 V (max)	50mV (min) 1200mV(max)
Eye height of non-transition bits	VTXA_d	Eye Height2	0.360 V (min) 1.2 V (max)	3.5dB De-emphasis .380 V (min) 1.2 V (max) 6.0dB De-emphasis .260 V (min) 1.2 V (max)	50mV (min) 1200mV(max)
Eye width with sample size of 106 UI	TTXA In Rev1.1	Eye Width	287 ps (min)	Not Specified	Not Specified
Jitter eye opening at BER 10-12	TTXA In Rev2.0	For Rev1.1: Eye Width For Rev2/3: PCIe T-TX	274 ps (min) Informative	123 ps (min) with Crosstalk	45.00ps(min)
Maximum median-max jitter outlier with sample size of 106 UI	JTXA-MEDIAN-to-MAX-JITTER	PCIe Med-Mx Jitter	56.5 ps (max)	Not Specified	Not Specified

Total Jitter at BER 10-12	Tj at BER 10-12	TJ@BER	Not Specified	77 ps (max)	80.00 ps(max)
Deterministic Jitter at BER 10-12	Max Dj	DJ–δδ	Not Specified	57 ps (max)	Not Specified
Random Jitter at BER 10-12	Max Rj	RJ–δδ	Not Specified	Not Specified	3.0 ps (max)

Specific PCI Express Gen3 measurements derived from ***SigTest Compliance*** tool for Add In Card: -

Parameter	**DPOJET Measurement**	**8.0 GT/s Rev3.0**
Clock Recovery	See Setup	1st Order PLL Fc: 10MHz
Min TBit Voltage(Max)	Eye Low	-25mV(max) -600mV(Min)
Min nTBit Voltage(Max)	Eye Low	-25mV(max) -600mV(Min)
Max TBit Voltage(Min)	Eye High	25mV(max) 600mV(Min)
Max nTBit Voltage(Min)	Eye High	25mV(max) 600mV(Min)

Add-In Card Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 5.

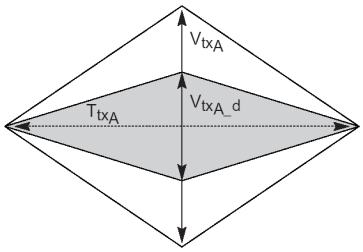


Figure 3: Add-in card compliance eye masks

Load the Add-In Card Setup File in DPOJET:

1. In the scope menu, select Analyze->PCI Express
2. In the DPOJET standard tab, click the select button to choose the Test Point
3. Select Rev3.0 -->SDLA_Add-In-Card->R30_SDLA_Add-in-Card.set
4. In the Math Menu, set Math1 to Channel 1-Channel 2(Data)

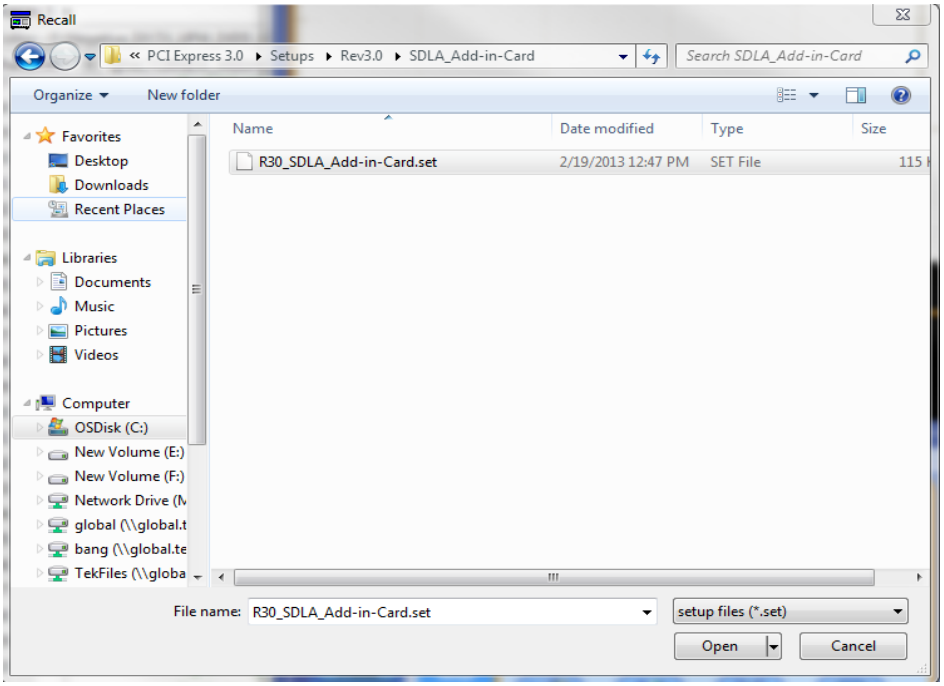


Figure 4: Setup File Selection

Applying Channel and Behavioral Equalizer from SDLA:

(Note: for Windows XP and 32-bit Win 7 Scopes, go to Appendix A and follow the procedure)

These measurements are done using SDLA (Serial Data Link Analysis) behavioral equalizer and channel embedding. Open SDLA from Analyze menu.

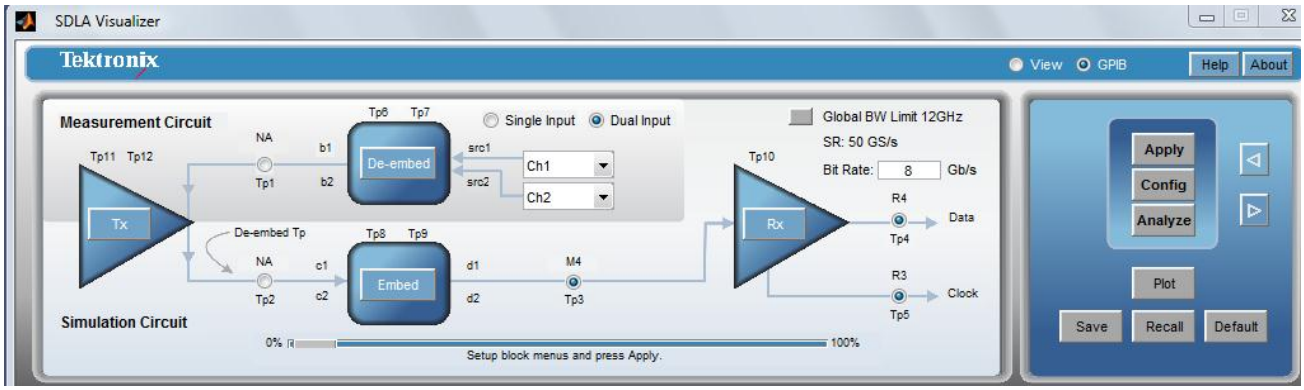


Figure 5: Serial Data Link Analysis window

5. Click Recall and select 'PCIE_R30_SDLA_Add-in-Card.sdl'. It will set Equalizer CTLE and DFE values as per the PCI Express 3.0 specification. For details of the PCI Express Gen 3 De-embedding procedure refer to the following document in http://www.tek.com/method-implementation/pci-express-30-de-embedding-method-implementation-version-10

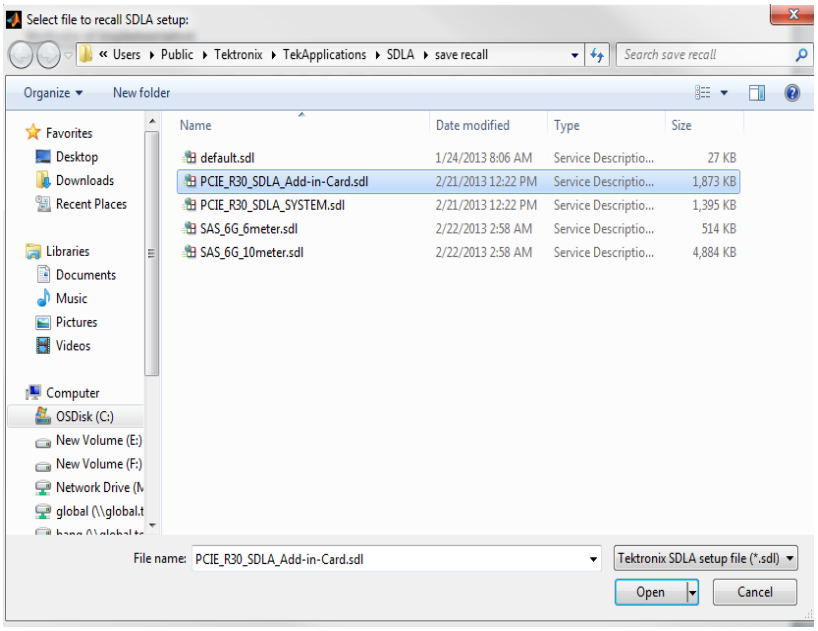
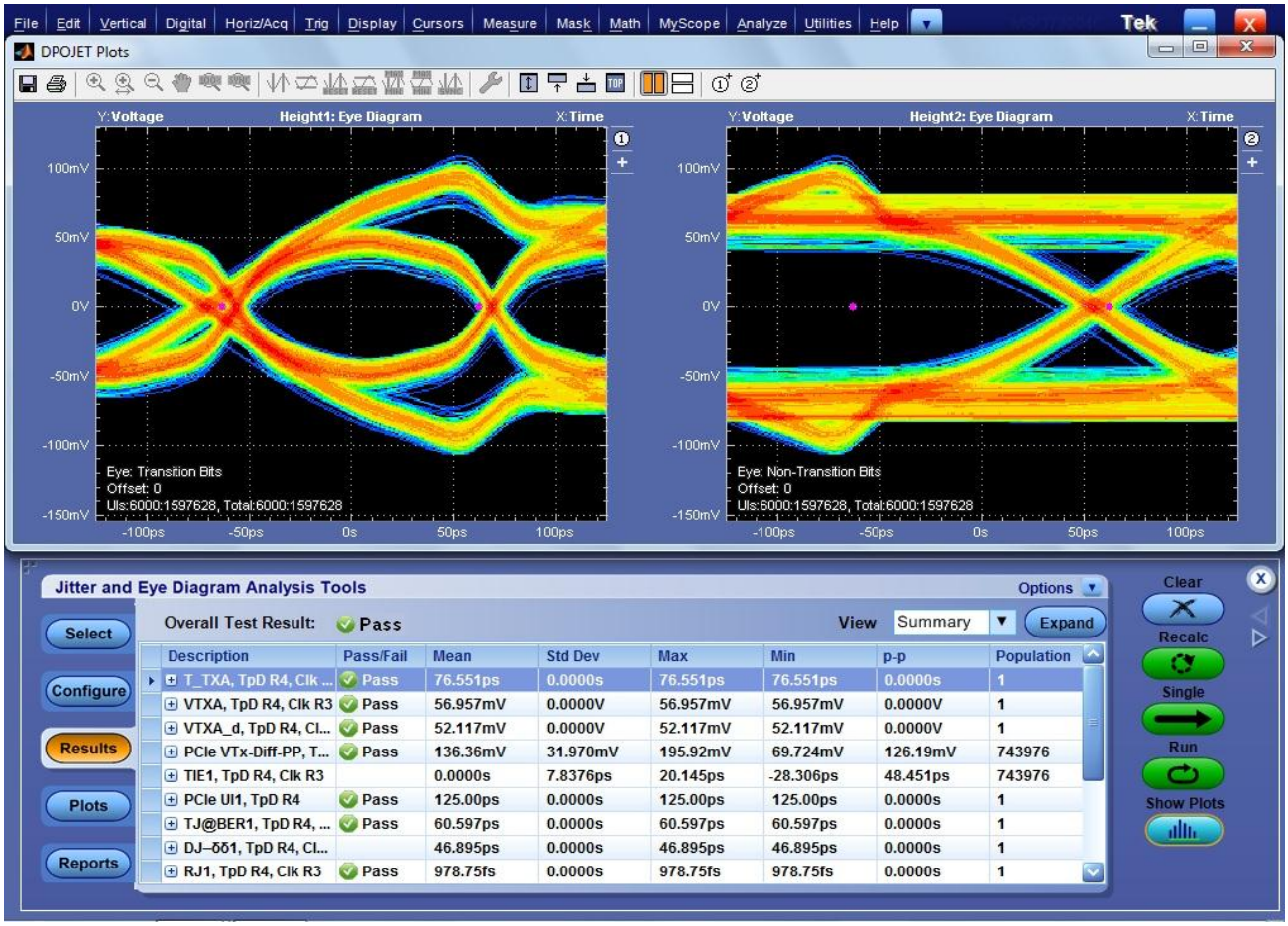


Figure 6: Setup file selection in SDLA

6. Click 'Apply' in SDLA. SDLA will process waveform from DUT by embedding the compliance channel and applying the reference equalizer (CTLE + 1 Tap DFE) and it will also automatically run DPOJET based on the current DPOJET configuration. The resulting waveform is placed in reference memory (Ref4). At the end user can generate a report containing the measurement results and test configuration by selecting the Report tab in DPOJET and clicking the save button.

NOTE: It is critical that the DPOJET setup file is recalled as described above before SDLA is ran.

The results will be displayed as below.



Description	Pass/Fail	Mean	Std Dev	Max	Min	p-p	Population
T_TXA, TpD R4, Clk ...	Pass	76.551ps	0.0000s	76.551ps	76.551ps	0.0000s	1
VTXA, TpD R4, Clk R3	Pass	56.957mV	0.0000V	56.957mV	56.957mV	0.0000V	1
VTXA_d, TpD R4, Cl...	Pass	52.117mV	0.0000V	52.117mV	52.117mV	0.0000V	1
PCIe VTx-Diff-PP, T...	Pass	136.36mV	31.970mV	195.92mV	69.724mV	126.19mV	743976
TIE1, TpD R4, Clk R3		0.0000s	7.8376ps	20.145ps	-28.306ps	48.451ps	743976
PCIe UI1, TpD R4	Pass	125.00ps	0.0000s	125.00ps	125.00ps	0.0000s	1
TJ@BER1, TpD R4, ...	Pass	60.597ps	0.0000s	60.597ps	60.597ps	0.0000s	1
DJ–δδ1, TpD R4, Cl...		46.895ps	0.0000s	46.895ps	46.895ps	0.0000s	1
RJ1, TpD R4, Clk R3	Pass	978.75fs	0.0000s	978.75fs	978.75fs	0.0000s	1

Figure 7: DPOJET Measurement Results

7. To configure SDLA manually, follow procedure described in **Appendix B**.

2.5 System Board Transmitter Path Specifications

Table 6 is derived from the Card Electrical Mechanical Specifications (CEM) and PHY Test Specification. See the CEM and Test Specification for additional notes and test definitions.

Table 6 – Supported CEM System Board Measurements

Parameter	Symbol	DPOJET Measurement	2.5GT/s Rev1.1/Rev2.0	5.0 GT/s Rev2.0	8.0 GT/s Rev3.0
Clock Recovery	NA	See Setup by Data Rate >>	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz - And - 1st Order LPF Fc: 1.5MHz *Emulates 3rd Order 3500:250 Method*	Explicit Clock 2nd Order PLL Clock Multiplier=50 CDR w/ .707 Damping Fc: 1.0MHz *Emulates Step Function Filter at 1.5MHz*	Explicit Clock 2nd Order PLL Clock Multiplier=80 Clock Edge Rising 0 .707 Damping Fc(JTF): 2.0MHz
Unit interval	*UI*	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	399.88 (min) 402.12 (max)	199.94 (min) 201.06 (max)	124.9625 ps (min) 125.6625ps (max)
Eye height of transition bits	V_{TXS}	Eye Height1	0.274 V (min) 1.2 V (max)	0.250 V (min)	46mV (min) 1200mV(max)
Eye height of non-transition bits	V_{TXS_d}	Eye Height2	0.253 V (min) 1.2 V (max)	0.250 V (min)	46mV (min) 1200mV(max)
Eye width with sample size of 10^6 UI	T_{TXS} *In Rev1.1*	Eye Width	246 ps (min)	Not Specified	Not Specified
Jitter eye opening at BER 10^{-12}	T_{TXS} *In Rev2.0*	For Rev1.1: Eye Width For Rev2/3: PCIe T-TX	233 ps (min) Informative	95 ps (min) with Crosstalk	41.25ps(min)
Maximum median-max jitter outlier with sample size of 10^6 UI	$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	PCIe Med-Mx Jitter	77 ps (max)	Not Specified	Not Specified
Total Jitter at BER 10^{-12}	Tj at BER 10^{-12}	TJ@BER	Not Specified	105 ps (max)	83.75 ps(max)
Deterministic Jitter at BER 10^{-12}	Max Dj	DJ–δδ	Not Specified	57 ps (max)	Not Specified
Random Jitter at BER 10^{-12}	Max Rj	RJ–δδ	Not Specified	Not Specified	3.0 ps (max)

Specific PCI Express Gen3 measurements derived from ***SigTest Compliance*** tool for System: -

Parameter	**DPOJET Measurement**	**8.0 GT/s Rev3.0**
Clock Recovery	See Setup	2nd Order PLL Fc: 2MHz
Min TBit Voltage(Max)	Eye Low	-23mV(max) -600mV(Min)
Min nTBit Voltage(Max)	Eye Low	-23mV(max) -600mV(Min)
Max TBit Voltage(Min)	Eye High	23mV(max) 600mV(Min)
Max nTBit Voltage(Min)	Eye High	23mV(max) 600mV(Min)

System Board Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 6.

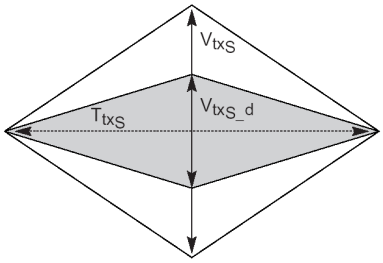


Figure 8: System Board Compliance Eye Masks

Load the System Setup File in DPOJET:

1. In the scope menu, select Analyze->PCI Express
2. In the DPOJET standard tab, click the select button to choose the Test Point
3. Select Rev3.0->SDLA_System->R30_SDLA_SYSTEM.set
4. In the Math Menu, set Math1 to Channel 3-Channel4(Data) and Math2 to Channel 1-Channel2(Clock)

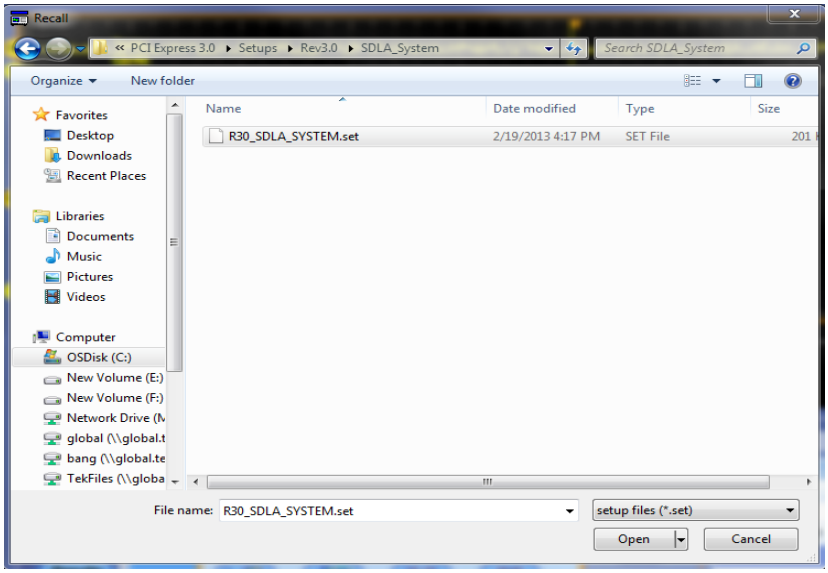


Figure 9: Setup File Selection

Applying Channel and Behavioral Equalizer from SDLA:

(Note: for Windows XP, go to Appendix A and follow the procedure)

These measurements are done using SDLA (Serial Data Link Analysis) behavioral equalizer and channel embedding. Open SDLA from Analyze menu.

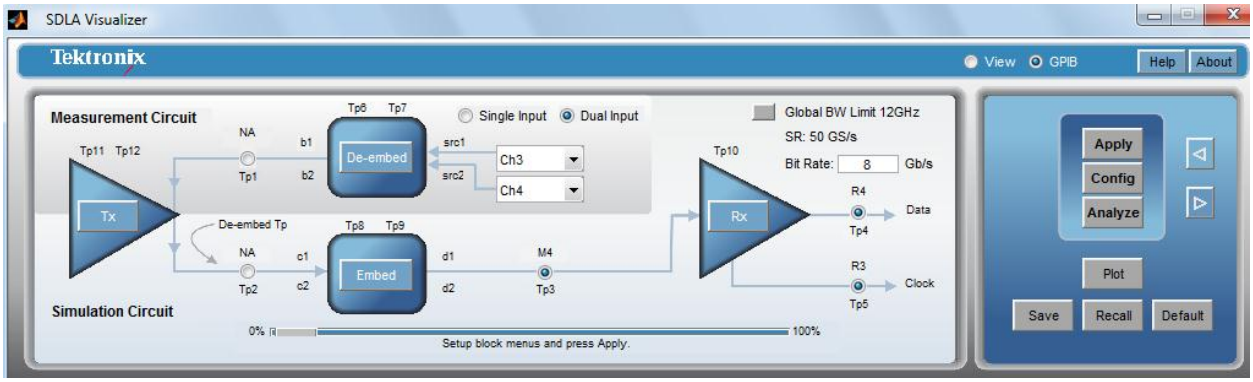


Figure 10: Serial Data Link Analysis window

5. Click Recall and select 'PCIE_R30_SDLA_SYSTEM.sdl'. It will set Equalizer CTLE and DFE values as per the PCI Express 3.0 specification. For details of the PCI Express Gen 3 De-embedding procedure refer to the following document in http://www.tek.com/method-implementation/pci-express-30-de-embedding-method-implementation-version-10

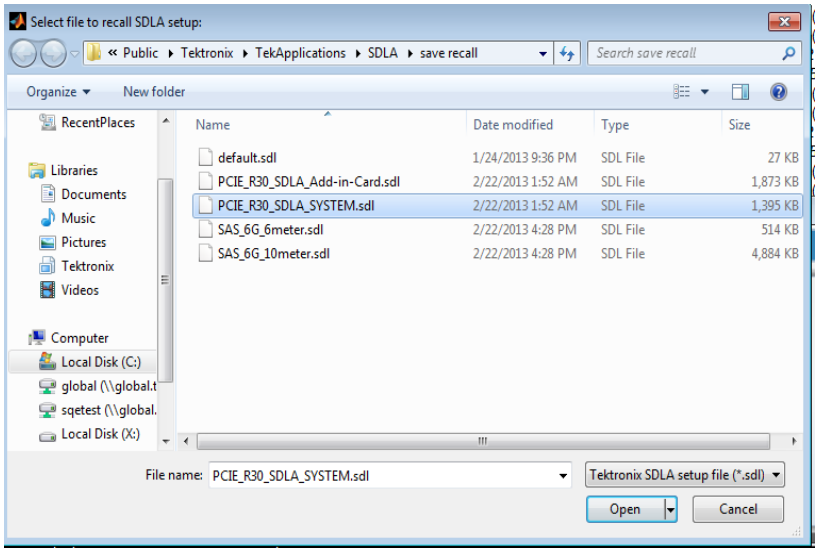


Figure 11: Setup file selection in SDLA

6. Click 'Apply' in SDLA. SDLA will process waveform from DUT and it will also process DPOJET analysis. At the end user will get a complete report of System Board.

The results will be displayed as below.

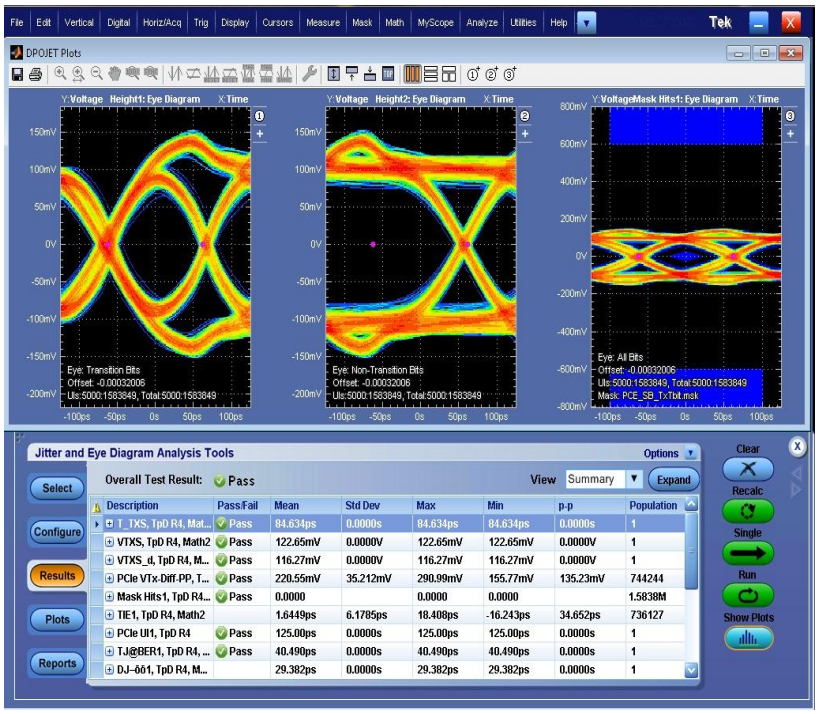


Figure 12: DPOJET Measurement Results

Note: Nominally the PCIe Rev3.0 bit rate is 8 Gb/s. But if a signal with SSC is tested, the bit rate should be set to 7.98 Gb/s. (0.25% lower). Alternatively, use the Auto Detect bit rate feature in SDLA Visualizer that will determine the exact clock frequency near the specified rate.

To repeat measurements, you can clear previous results by pressing Clear in DPOJET and press Apply in SDLA. New acquisition and calculations will be completed automatically. This is necessary when testing different presets.

To configure SDLA manually, follow procedure described in Appendix B**.**

When measuring systems with short channels, or when doing exploratory testing, CTLE equalization may be sufficient. Then use R30_SYSTEM.set in R30_SYSTEM folder. This setup does not require SDLA and sets up a CTLE with -7dB gain as an ArbFilter. It does not embed the channel. Press Single to acquire waveforms and calculate measurements. In this mode Free Run is possible.

To change the CTLE filter, follow the procedure described below:

1. Load R30_SYSTEM.set file from R30_SYSTEM folder.
2. Click on Math menu and go to ‘Editor’ in Math subsystem.

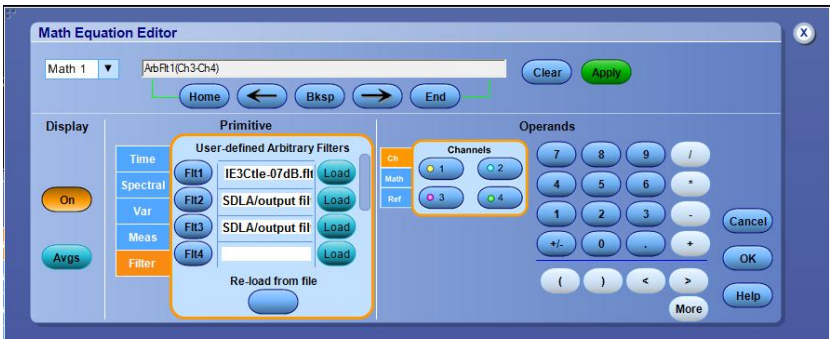


Figure 13: Filter settings in Math menu

3. Select ‘Filter’ tab and click ‘Load’ button in ‘Flt1’ section. It will guide to the desired filters location. Select any of seven filters(-6dB to -12dB CTLE filters) and click Open. It will apply the desired filter to differential data.

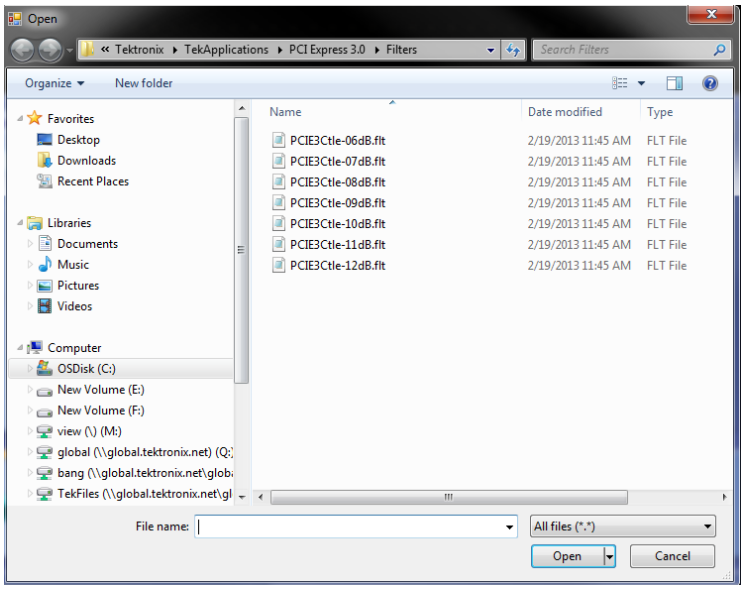


Figure 14: Selecting CTLE Filter

4. Click ‘Single’ in DPOJET.

2.6 Reference Clock Specification

Table 7 is derived from the PCI Express Card Electromechanical Specification for Gen1 Clock and PCI Express Base Specification Rev 3.0 for Gen2 and Gen3.

Table 7A – Supported Ref Clock Rev1.1 Measurements

Gen 1 Clock Setup files			
	Clock Recovery	**Edge**	**Limit**
T -RCLK	Constant Clock(Mean)	Rising	86ps(pk-pk)

Table 7B – Supported Ref Clock Rev2.0 Measurements

Gen 2 Clock Setup files			
	Clock Recovery	**Edge**	**Limit**
T-HF-RMSCC-RCLK	Constant Clock(Mean)	Rising	3.1 ps(RMS)
T-LF-RMSCC-RCLK	Constant Clock(Mean)	Rising	3.0 ps(RMS)
T-HF-RMSDC-RCLK	Constant Clock(Mean)	Rising	4.0 ps(RMS)
T-LF-RMSDC-RCLK	Constant Clock(Mean)	Rising	7.5 ps(RMS)
SRNS	Constant Clock(mean)	Rising	2 ps(RMS)
SRIS	Constant Clock(mean)	Rising	2 ps(RMS)

Table 7C – Supported Ref Clock Rev3.0 Measurements

Gen 3 Clock Setup files			
	Clock Recovery	**Edge**	**Limit**
T-RMSCC-RCLK	Constant Clock(mean)	Rising	1 ps(RMS)
T-WST-RMSCC-RCLK	Constant Clock(mean)	Rising	1 ps(RMS)
T-RMSDC-RCLK	Constant Clock(mean)	Rising	1 ps(RMS)
T-WST-RMSDC-RCLK	Constant Clock(mean)	Rising	1 ps(RMS)
Gen3_SRIS	Constant Clock(mean)	Rising	0.5 ps(RMS)
Gen3_SRNS	Constant Clock(mean)	Rising	0.5 ps(RMS)

Table 7D – Supported Ref Clock Rev4.0 Measurements

Gen 4 Clock Setup files			
	Clock Recovery	**Edge**	**Limit**
PCIE4_T-RMSCC-RCLK	Constant Clock(mean)	Rising	0.7 ps(RMS)
PCIE4_T-WST-RMSCC-RCLK	Constant Clock(mean)	Rising	0.7 ps(RMS)
PCIE4_T-RMSDC-RCLK	Constant Clock(mean)	Rising	0.7 ps(RMS)
PCIE4_T-WST-RMSDC-RCLK	Constant Clock(mean)	Rising	0.7 ps(RMS)
PCIE4_SRIS	Constant Clock(mean)	Rising	0.7 ps(RMS)
PCIE4_SRNS	Constant Clock(mean)	Rising	0.7 ps(RMS)

Table below shows the various requirements from the specification for the reference clock:

Symbol	Description	Limits		Units	Note
		Min	Max		
$T_{REFCLK-HF-RMS}$	> 1.5 MHz to Nyquist RMS jitter after applying Equation 4.3.3		3.1	ps RMS	1
$T_{REFCLK-SSC-RES}$	SSC residual		75	ps	1
$T_{REFCLK-LF-RMS}$	10 kHz - 1.5 MHz RMS jitter		3.0	ps RMS	2
$T_{SSC-FREQ-DEVIATION}$	SSC deviation		+0.0/-0.5	%	
$T_{SSC-MAX-PERIOD-SLEW}$	Maximum SSC df/dt		0.75	ps/UI	3

Notes:

1. $T_{REFCLK-HF-RMS}$ is measured at the far end of the test circuit illustrated in Figure 4-89 after the filter function defined in Table 4-30 for Common Refclk Rx for >1.5 MHz jitter components has been applied.
2. $T_{REFCLK-SSC-RES}$ and $T_{REFCLK-LF-RMS}$ are measured after the filter function defined in Table 4-30 for Common Refclk Rx for >1.5 MHz jitter components has been applied.
3. Defined for a worst case SSC modulation profile such as Lexmark.

Table 7d: Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s (spec Table 4-32)

Symbol	Description	Limits		Units	Note
		Min	Max		
$T_{REFCLK-HF-RMS}$	1.5 - Nyquist MHz RMS jitter after applying Equation 4.3.5		4.0	ps RMS	1
$T_{REFCLK-SSC-FULL}$	Full SSC modulation corresponding to +0 – 0.5%		20	ns	1
$T_{REFCLK-LF-RMS}$	10 kHz - 1.5 MHz RMS jitter		7.5	ps RMS	2
$T_{SSC-FREQ-DEVIATION}$	SSC deviation		+0.0/-0.5	%	
$T_{SSC-MAX-PERIOD-SLEW}$	Max SSC df/dt		0.75	ps/UI	3

Notes:

1. $T_{REFCLK-HF-RMS}$ is measured at the far end of the test circuit illustrated in Figure 4-93 after the filter function defined in Table 4-30 for Data Clocked Rx for >1.5 MHz jitter components has been applied.
2. $T_{REFCLK-SSC-FULL}$ and $T_{REFCLK-LF-RMS}$ are measured after the filter function defined in Table 4-30 for Data Clocked Rx for < 1.5 MHz jitter components has been applied.
3. Defined for a worst case SSC modulation profile such as Lexmark.

Table 7e: Refclk Parameters for Data Refclk Rx Architecture at 5.0 GT/s (spec Table 4-34)

Symbol	Description	Limits		Units
		Min	Max	
F_{REFCLK}	Refclk frequency	99.97	100.03	MHz
$T_{REFCLK-RMS-SRIS}$	RMS Refclk jitter for Separate Refclk Independent SSC architecture[1]		2.0	ps RMS
F_{SSC}	SSC frequency range	30	33	kHz
$T_{SSC-FREQ-DEVIATION}$	SSC deviation		+0.0/-0.5	%

Table 7f: Parameters for Separate Refclk With Independent SSC Architecture (SRIS) at 5.0 GT/s(Spec table 4-35)

Symbol	Description	Limits		Units
		Min	Max	
F_{REFCLK}	Refclk frequency[1]	99.97	100.03	MHz
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk Rx architecture[3]		1.0	ps RMS
F_{SSC}	SSC frequency range	30	33	kHz
$T_{SSC-FREQ-DEVIATION}$	SSC deviation[2]		+0.0/-0.5	%
$T_{TRANSPORT-DELAY}$	Tx-Rx transport delay	12		ns

Table 7g: Parameters for common Refclk at 8.0 GT/s (Spec table 4-37)

Symbol	Description	Limits		Units
		Min	Max	
F_{REFCLK}	Refclk frequency	99.97	100.03	MHz
$T_{REFCLK-RMS-DC}$	RMS Refclk jitter for data clocked Rx architecture[1]		1.0	ps RMS
F_{SSC}	SSC frequency range	30	33	kHz
$T_{SSC-FREQ-DEVIATION}$	SSC deviation		+0.0/-0.5	%

Table 7h: Parameters for data Refclk at 8.0 GT/s (Spec table 4-38)

Symbol	Description	Limits		Units
		Min	Max	
F_{REFCLK}	Refclk frequency	99.97	100.03	MHz
$T_{REFCLK-RMS-SRIS}$	RMS Refclk jitter for separate Refclk independent SSC architecture[1]		0.5	ps RMS
F_{SSC}	SSC frequency range	30	33	kHz
$T_{SSC-FREQ-DEVIATION}$	SSC deviation		+0.0/-0.5	%

Table 7i: Parameters for SRIS Refclk at 8.0 GT/s (Spec table 4-39)

2.7 MXM System Board Specifications

Table 8 is derived from the Mobile PCI Express MXM Electrical Mechanical Specifications. See the MXM Specification for additional notes and test definitions.

Table 8 – Supported MXM System Board Measurements

Parameter	Symbol	DPOJET Measurements	2.5GT/s	2.5GT/s	5GT/s	5GT/s	5GT/s
Clock Recovery	N/A	See Setup by Data Rate >>	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz - And - 1st Order LPF Fc: 1.5MHz *Emulates 3rd Order 3500:250 Method*	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz - And - 1st Order LPF Fc: 1.5MHz *Emulates 3rd Order 3500:250 Method*	Explicit Clock 2nd Order PLL Clock Multiplier=25 CDR w/ .707 Damping Fc: 1.0MHz *Emulates Step Function Filter at 1.5MHz*	Explicit Clock 2nd Order PLL Clock Multiplier=25 CDR w/ .707 Damping Fc: 1.0MHz *Emulates Step Function Filter at 1.5MHz*	Explicit Clock 2nd Order PLL Clock Multiplier=25 CDR w/ .707 Damping Fc: 1.0MHz *Emulates Step Function Filter at 1.5MHz*
Swing			Low	Standard	Low	Standard	Standard
DeEmphasis Setting			0dB	3.5dB	0dB	3.5dB	6.0dB
Unit interval	UI	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	400.12ps(max) 399.88(min)	400.12ps(max) 399.88(min)	200.06 ps(max) 199.94 ps(min)	200.06 ps(max) 199.94 ps(min)	200.06 ps(max) 199.94 ps(min)

Eye height of transition bits	V_{TXS}	Eye Height1	216 mV(min)	232 mV(min)	170 mV(min)	200 mV(min)	200 mV(min)
Eye height of non-transition bits	V_{TXS_d}	Eye Height2	N/A	223 mV(min)	170 mV(min)	200 mV(min)	200 mV (min)
Eye width	T_{TXA}	PCIe T-TX	242 ps (min)	242 ps (min)	95 ps (min)	95 ps (min)	95 ps (min)
Total Jitter at BER 10^{-12}	Tj@BER 10^{-12}	TJ@BER	Not Specified	Not Specified	105 ps (max)	105 ps (max)	105 ps (max)
Deterministic Jitter	Max Dj	DJ–δδ	Not Specified	Not Specified	57 ps(max)	57 ps(max)	57 ps(max)

2.8 MXM System Board Compliance Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 2(a & b).

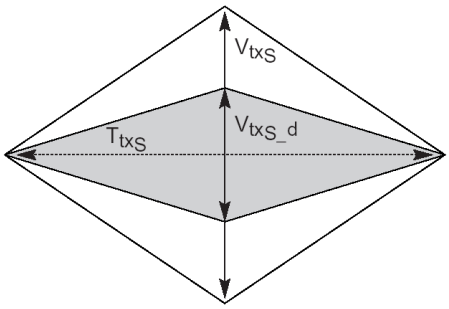


Figure 13: MXM System Board Compliance Eye Masks

2.9 PCI ExpressModule™ Specifications

The specifications in this section are taken from the PCI Express ExpressModule™ specification, which is a companion specification to the PCI Express Base Specification. Its primary focus is the implementation of a modular I/O form factor that is focused on the needs of workstations and servers. Measurements in the PCE module support add-in card and system transmitter path measurements at the PCI Express connector.

ExpressModule Add-In Card Transmitter Path Specifications

Table 9 is derived from Section 5.4.1 of the ExpressModule Electro-Mechanical Specifications Rev. 1.0.

Table 9 – Supported ExpressModule Add-In Card Measurements

Parameter	Symbol	DPOJET Measurement	Rev1.0
Clock Recovery	NA	See Setup by Data Rate >>	1st Order PLL Fc: 1MHz *Emulates 1st Order filter at 1.5MHz with 75% edge density of Compliance Pattern*
Unit interval	*UI*	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	399.98 (min) 400.12 (max)
Eye height of transition Bits	V_{TXA}	. Eye Height1	.514 V (min) 1.2 V (max)
Eye height of non-transition Bits	V_{TXA_d}	Eye Height2	.360 V (min)
Eye width with sample size of 10^6 UI	T_{TXA} In Rev1.1	Eye Width	287 ps (min)
Jitter eye opening at BER 10^{-12}		Eye Width@BER	274 ps (min) Informative
Maximum median-max jitter outlier with sample size of 10^6 UI	$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	PCIe Med-Mx Jitter	56.5 ps (max)

ExpressModule Add-In Card Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 9.

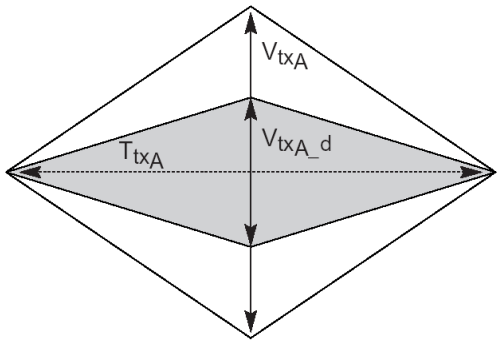


Figure 14: ExpressModule add-in card compliance eye masks

2.10 MXM ExpressModule Specifications

Table 10 is derived from the Mobile PCI Express MXM Electrical Mechanical Specifications. See the MXM Specification for additional notes and test definitions.

Table 10 – Supported MXM Express Module Measurements

Parameter	Symbol	DPOJET Measurements	2.5GT/s	2.5GT/s	5GT/s	5GT/s	5GT/s
Clock Recovery	N/A	See Setup by Data Rate >>	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz - And - 1st Order LPF Fc: 1.5MHz *Emulates 3rd Order 3500:250 Method*	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz - And - 1st Order LPF Fc: 1.5MHz *Emulates 3rd Order 3500:250 Method*	Explicit Clock 2nd Order PLL Clock Multiplier=25 CDR w/ .707 Damping Fc: 1.0MHz *Emulates Step Function Filter at 1.5MHz*	Explicit Clock 2nd Order PLL Clock Multiplier=25 CDR w/ .707 Damping Fc: 1.0MHz *Emulates Step Function Filter at 1.5MHz*	Explicit Clock 2nd Order PLL Clock Multiplier=25 CDR w/ .707 Damping Fc: 1.0MHz *Emulates Step Function Filter at 1.5MHz*
Swing			Low	Standard	Low	Standard	Standard
DeEmphasis Setting			0dB	3.5dB	0dB	3.5dB	6.0dB
Unit interval	UI	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	400.12ps(max) 399.88(min)	400.12ps(max) 399.88(min)	200.06 ps(max) 199.94 ps(min)	200.06 ps(max) 199.94 ps(min)	200.06 ps(max) 199.94 ps(min)
Eye height of transition bits	V_{TXS}	Eye Height1	262 mV(min)	466 mV(min)	170 mV(min)	340 mV(min)	300 mV(min)
Eye height of non-transition bits	V_{TXS_d}	Eye Height2	N/A	314 mV(min)	170 mV(min)	340 mV(min)	260 mV (min)
Eye width	T_{TXA}	PCIe T-TX	254 ps (min)	254 ps (min)	123 ps (min)	123 ps (min)	123 ps (min)
Total Jitter at BER 10^{-12}	$Tj@BER10^{-12}$	TJ@BER	Not Specified	Not Specified	77 ps (max)	77 ps (max)	77 ps (max)
Deterministic Jitter	Max Dj	DJ–δδ	Not Specified	Not Specified	57 ps(max)	57 ps(max)	57 ps(max)

MXM System Board Compliance Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 10 (a & b).

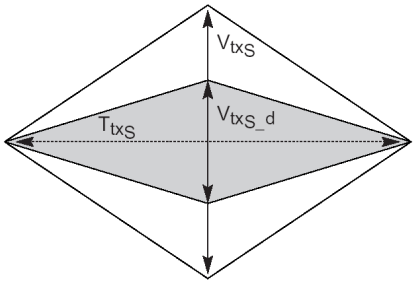


Figure 15: MXM System Board Compliance Eye Masks

2.11 ExpressModule System Board Transmitter Path Specifications

Table 11 is derived from Section 5.4.3 of the ExpressModule Electro-Mechanical Specifications Rev. 1.0.

Table 11 – Supported ExpressModule system board measurements

Parameter	Symbol	DPOJET Measurement	Gen1 Rev1.0
Clock Recovery	NA	See Setup by Data Rate >>	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz - And - 1st Order LPF Fc: 1.5MHz *Emulates 3rd Order 3500:250 Method*
Unit interval	*UI*	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	399.98 (min) 400.12 (max)
Eye height of transition bits	V_{TXS}	. Eye Height1	.274 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{TXS_d}	Eye Height2	.253 V (min)
Eye width with sample size of 10^6 UI	T_{TXS}	Eye Width	246 ps (min)
Jitter eye opening at BER 10^{-12}		Eye Width@BER	233 ps (min)
Maximum median-max jitter outlier with sample size of 10^6 UI	$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	TIE Jitter	77 ps (max)

Express Module System Board Compliance Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table11.

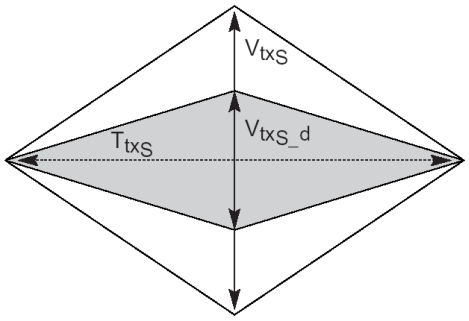


Figure 16: ExpressModule system board compliance eye masks

2.12 PCI Express External Cabling Specifications

The specifications in this section are taken from the PCI Express External Cabling Specification. Its primary focus is the implementation of a cabled interconnects. Measurements in the PCE module support transmitter path and receiver path measurements. These measurements represent the test points at the transmitter end of the cable and the receiver end of the cable respectively.

External Cabling Transmitter Path Specifications

Table 12 is derived from Section 3.3.1 of the External Cabling Specification Rev. 1.0.

Table 12 – Supported external cabling transmitter path measurements

Parameter	Symbol	DPOJET Measurement	Rev1.0	Rev2.0
Clock Recovery	NA	See Setup by Data Rate >>	1st Order PLL Fc: 1MHz *Emulates 1st Order filter at 1.5MHz with 75% edge density of Compliance Pattern*	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz
Unit interval	*UI*	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)
Eye height of transition bits	V_{TXA}	. Eye Height1	.654 V (min) 1.2 V (max)	.612 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{TXA_d}	Eye Height2	.450 V (min)	.369 V (min)
Jitter eye opening at BER 10^{-12}	Trx_A @ BER 10^{-12}	Eye Width@BER	296 ps (min)	149 ps (min)
Eye width with sample size of 10^6 UI	Trx_A @ 10^6 Samples	Eye Width	309 ps (min)	148 ps (min)

Cable (Transmitter Side) Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications.

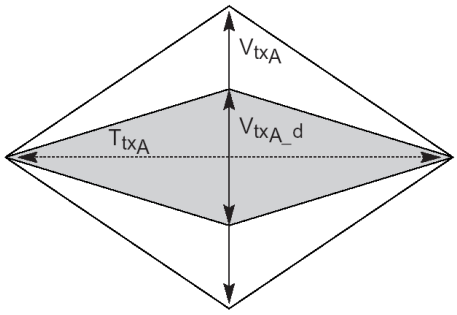


Figure 17: Cable (transmitter side) compliance eye masks

2.13 External Cabling Receiver Path Specifications

Table 13 is derived from Section 3.3.2 of the External Cabling Specification Rev. 1.0.

Table 13 – Supported CEM system board measurements

Parameter	Symbol	DPOJET Measurement	Rev1.0	Rev2.0
Clock Recovery	NA	See Setup by Data Rate >>	1st Order PLL Fc: 1MHz *Emulates 1st Order filter at 1.5MHz with 75% edge density of Compliance Pattern*	2nd Order PLL CDR w/ .707 Damping Fc: 1.0MHz
Unit interval	*UI*	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	399.98 (min) 400.12 (max)	199.94 (min) 200.06 (max)
Eye height of transition bits	V_{RXA}	Eye Height1	.208 V (min) 1.2 V (max)	.203 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{RXA_d}	Eye Height2	.192 V (min)	.203 V (min)
Jitter eye opening at BER 10^{-12}	Trx_A @ BER 10^{-12}	Eye Width@BER	234 ps (min)	122 ps (min)
Eye width with sample size of 10^6 UI	Trx_A @ 10^6 Samples	Eye Width	247 ps (min)	127 ps (min)

Cable (Receive Side) Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications.

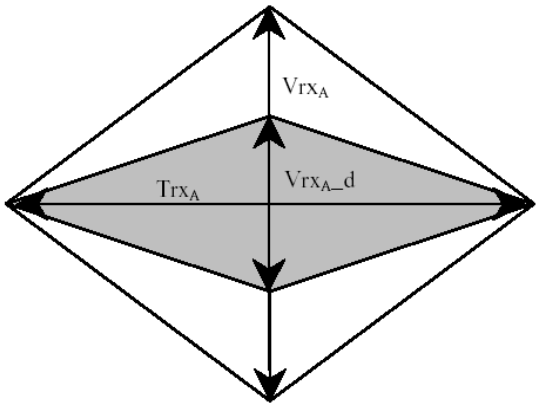


Figure 18: Cable (receiver side) compliance eye masks

2.14 PCMCIA ExpressCard™ Specifications

The specifications in this section are taken from the PCMCIA ExpressCard Standard (Release 1.0).The primary focus is a small modular add-in card technology based on the PCI Express and USB interfaces. Measurements in the PCE module support host system and ExpressCard transmitter path measurements.

ExpressCard - Module Transmitter Path Specifications

Table 14 is derived from Section 4.2.1.3.2 of the ExpressCard Specification Release 1.0.

Table 14 – Supported ExpressCard transmitter path measurements

Parameter	Symbol	DPOJET Measurement	Release 1.0
Clock Recovery	NA	See Setup by Data Rate >>	1st Order PLL Fc: 1MHz *Emulates 1st Order filter at 1.5MHz with 75% edge density of Compliance Pattern*
Unit interval	*UI*	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc =	399.98 (min) 400.12 (max)

		198kHz	
Eye height of transition bits	V_{TXA}	. Eye Height1	538 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{TXA_d}	Eye Height2	.368 V (min)
Eye width across any 250 UIs	T_{TXA}	Eye Width@BER	237 ps (min)

ExpressCard Transmitter Path Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 14.

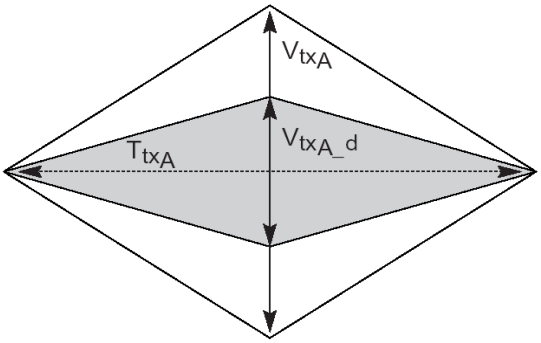


Figure 19: ExpressCard Module Transmitter compliance eye masks

ExpressCard - Host System Transmitter Path Specifications

Table15 from Section 4.2.1.3.2 of the ExpressCard Specification Release 1.0.

Table 15 – Supported ExpressCard Host System Transmitter Path Measurements

Parameter	Symbol	DPOJET Measurement	Release 1.0
Clock Recovery	NA	See Setup by Data Rate >>	2nd Order PLL CDR Damping Fc: 1.0MHz - And - 1st Order LPF Fc: 1.5MHz Emulates 3rd Order 3500:250 Method
Unit interval	UI	PCIe UI (min/max) SSC filtered with 3rd order LPF: Fc = 198kHz	399.98 (min) 400.12 (max)
Eye height of transition bits	V_{txS}	. Eye Height1	.262 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{txS_d}	Eye Height2	.247 V (min)
Eye width across any 250 UIs	T_{TxS}	Eye Width@BER	183 ps (min)

ExpressCard – Host System Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 15.

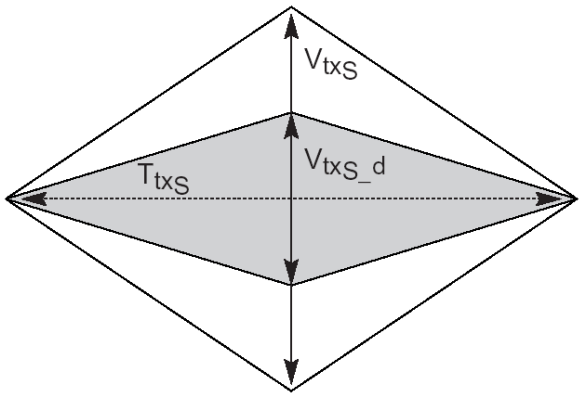


Figure 20: ExpressCard Host System compliance eye masks

3 PCI Express Library Contents

The following table shows a list of the PCI Express standards supported by the DPOJET Setup Library and their default probing configurations. All Rev1.0 and Rev1.1 setup files are for 2.5 GT/s. Rev 2.0 setup files are for 5.0 GT/s and Rev3.0 setup files are for 8.0 GT/s. Revision numbers are made according to the test methods. See Table 1 for more details. The setup file library is located in C:\Users\Public\Tektronix\TekApplications\PCI Express\ for 2.5GT/s and 5.0 GT/s and C:\Users\Public\Tektronix\TekApplications\PCI Express 3.0\ for 8.0 GT/s.

Table 16 – Setup Files and default probing configurations

PCI-SIG Specification	Bit Rate	Setup File Name	Default Probing Configuration
Rev1.1 Base Specification Transmitter and Receiver	2.5GT/s	R11_Tx_Base.set R11_Rx_Base.set	Data = Math1 = Ch1-Ch2
Rev1.1 MXM Specification Module and System	2.5GT/s	R11_MXM_Mod_0dB_Low.set R11_MXM_Sys_0dB_Low.set R11_MXM_Tx_Mod_3.5dB.set R11_MXM_Tx_Sys_3.5dB.set	Data = Math1 = Ch1-Ch2
Rev1.1 CEM Specification Add-In Card and System	2.5GT/s	R11_Tx_ADD_CON.set R11_Tx_SYSTEM_3500-250.set	Data = Math1 = Ch1-Ch2
Rev 1.1 Ref Clock Specification	2.5 GT/s	R11_RefClk.set	RefClk = Math1 = Ch1-Ch2
Rev1.0 Cable Specification Near End and Far End	2.5GT/s	R10_Tx_Cable.set R10_Rx_Cable.set	Data = Math1 = Ch1-Ch2
Rev1.0 ExpressModule Specification Add-In Card and System	2.5GT/s	R10_Tx_ExpMod_ADD_CON.set R10_Tx_ExpMod_SYSTEM.set	Add-In Card: Data = Math1= Ch1-Ch2 System: Data = Math1 = Ch1-Ch2
Rev1.0 ExpressCard Specification Host and Module	2.5GT/s	R10_Tx_ExpressCard_Host.set R10_Tx_ExpressCard_Module.set	Data = Math1 = Ch1-Ch2
Rev2.0 Base Specification Transmitter with 3.5dB and 6.0 dB De-Emphasis and Low Swing	5GT/s	R20_Base_Tx_3.5dB.set R20_Base_Tx_6.0dB.set R20_Base_Tx_Low_Swing.set R20_PCIe_AC_Common_Mode.set R20_PCIe_AC_Common_Mode_bp_33 Khz_500Mhz.set	Data = Math1 = Ch1-Ch2
Rev1.1 MXM Specification Module and System	5GT/s	R20_MXM_Mod_3.5dB_Low.set R20_MXM_Sys_3.5dB_Low.set R20_MXM_Tx_Mod_3.5dB.set R20_MXM_Tx_Mod_6dB.set R20_MXM_Tx_Sys_3.5dB.set R20_MXM_Tx_Sys_6dB.set	Data = Math1 = Ch1-Ch2
Rev2.0 CEM Specification Add-In Card with 3.5dB and 6.0dB De-Emphasis and	5GT/s	R20_Tx_ADD_CON_3.5dB.set R20_Tx_ADD_CON_6.0dB.set R20_Tx_SYSTEM.set	Add-In Card: Data = Math1= Ch1-Ch2 System:

System			Data = Math1 = Ch1-Ch2 RefClk = Math2 = Ch3 – Ch4
Rev2.0 Cable Specification Near End and Far End	5GT/s	R20_Tx_Cable.set R20_Rx_Cable.set	Data = Math1 = Ch1-Ch2
Rev 3.0 Base Specification Transmitter Full and Half Swing	8GT/s	R30_V-TX-FS-NO-EQ.set R30_V-TX-RS-NO-EQ.set R30_V-TX-EIEOS-FS.set R30_V-TX-EIEOS-RS.set R30_T-TX-UTJ.set R30_T-TX-UPW-DJDD.set R30_T-TX-DDJ.set R30_T-TX-UPW-TJ.set R30_T-TX-UDJDD.set R30_ps21Tx.set R30_V-Tx-FS-Boost.set R30_V-Tx-RS-Boost.set R30_BaseMeas_FS.set R30_BaseMeas_RS.set R30_Base_Rx.set R30_PCIe_AC Common_Mode.set R30_PCIe_AC_Common_Mode_bp_33 Khz_500Mhz.set	Data = Math1 = Ch1-Ch2 The following setups are for recalling specific measurement for standalone evaluation These setups are for combined measurements at transmitter or receiver test point
Rev3.0 CEM Specification Add-In Card	8GT/s	R30_ADD_CON.set R30_SDLA_Add-in-Card.set	Data = Math1= Ch1-Ch2 RefClk = Ref3 (From SDLA)
Rev3.0 CEM Specification System Board	8GT/s	R30_System.set R30_SDLA_SYSTEM.set	Data = Math1 = Ch1-Ch2 RefClk = Math2 = Ch3 – Ch4 Data = Ref4 (From SDLA) RefClk=Math2= Ch1-Ch2
Rev3.0 Clock Specification	5GT/s	R21_RMSCC_RefClk.set R21_RMSDC_RefClk.set R21_RMS_SRNS.set R21_RMS_SRIS.set	RefClk = Math1 = Ch1-Ch2 For SRNS/SRIS RefClk1 = Math1 = Ch1-Ch2 RefClk2 = Math2 = Ch3-Ch4
Rev3.0 Clock Specification	8GT/s	R30_RMSCC_RefClk.set R30_RMSDC_RefClk.set R30_SRIS_RefClk.set R30_SRNS_RefClk.set	RefClk = Math1 = Ch1-Ch2 For SRNS/SRIS RefClk1 = Math1 = Ch1-Ch2 RefClk2 = Math2 = Ch3-Ch4
Rev 4.0 Base Specification Transmitter Full and Half Swing	16GT/s	R40_V-TX-FS-NO-EQ.set R40_V-TX-RS-NO-EQ.set R40_V-TX-EIEOS-FS.set R40_V-TX-EIEOS-RS.set R40_T-TX-UTJ.set R40_T-TX-UPW-DJDD.set R40_T-TX-DDJ.set R40_T-TX-UPW-TJ.set	Data = Math1 = Ch1-Ch3 The following setups are for recalling specific measurement for standalone evaluation

		R40_T-TX-UDJDD.set R40_ps21TxRootdevice.set R40_ps21TxAICdevice.set R40_V-Tx-FS-Boost.set R40_V-Tx-RS-Boost.set R40_BaseMeas_FS.set R40_BaseMeas_RS.set	These setups are for combined measurements at transmitter or receiver test point
Rev4.0 Clock Specification	16GT/s	R40_RMSCC_RefClk.set R40_RMSDC_RefClk.set R40_SRIS_RefClk.set R40_SRNS_RefClk.set	RefClk = Math1 = Ch1-Ch2 For SRNS/SRIS RefClk1 = Math1 = Ch1-Ch2 RefClk2 = Math2 = Ch3-Ch4

In the above table DPOJET setup library contains setup files for all individual measurements as well as combined setup files for base measurements and CEM measurements. Individual setup files can run with higher record length up to 50M and combined setup files can run with a record length of 20M. So if user wants to run measurements with the original compliance pattern, he/she can go with individual setup files or else user can go with combined setup file and get an overall result for PCI Express 3.0 measurements.

To change the probing configuration to use differential probes, change the Source of the Data and RefClk as appropriate in the measurement configuration menu in DPOJET. Refer to the DPOJET Online Help for details.

3.1 Retaining Deskew

User can retain his/her own deskew setting unchanged while recalling any setup files. User has to follow the following procedure:

Go to ‘File’ and select ‘Recall’ to recall a PCI Express setup. When the window will appear, select the required setup file from and before clicking ’Recall’, enable the check box saying *“Don’t recall deskew values. Keep existing deskew settings”*.

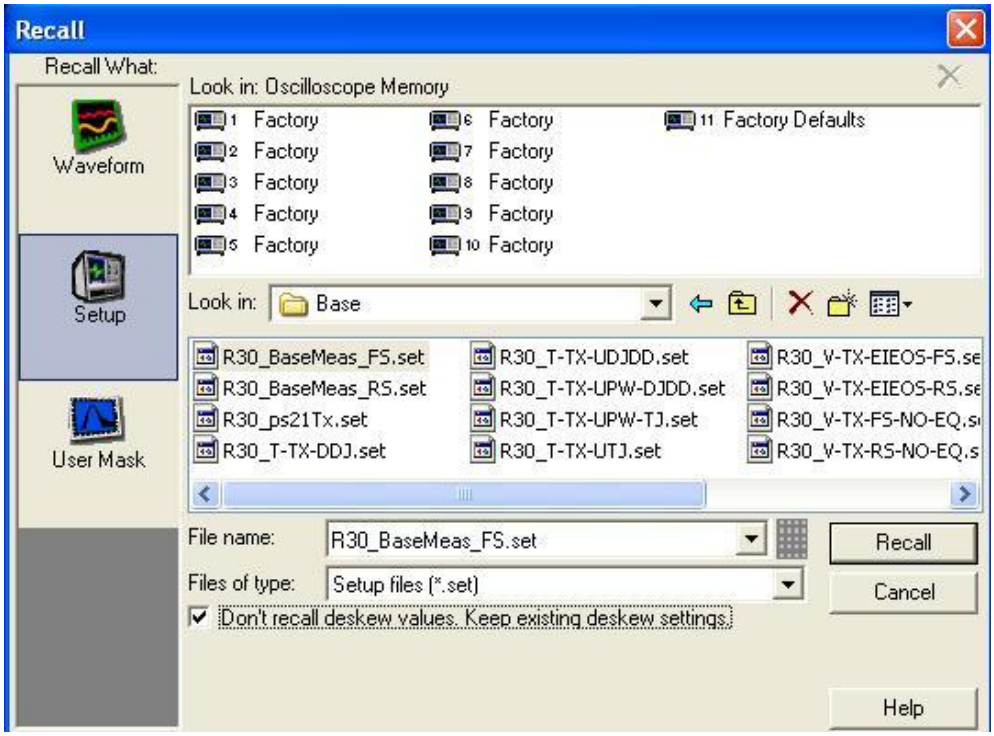


Figure 21: Retaining deskew setting unchanged

4 Preparing to Take Measurements

4.1 Required Equipment

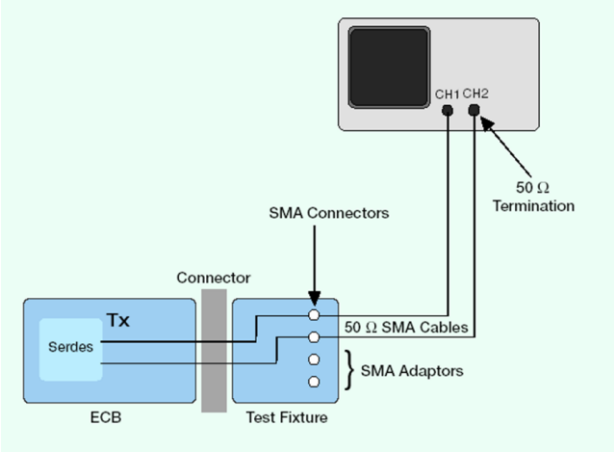
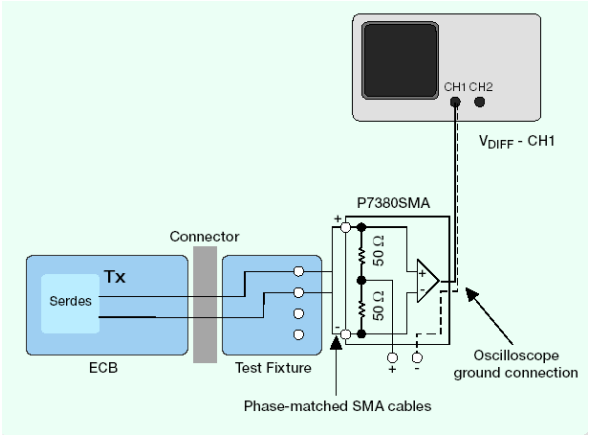
The following equipment is required to take the measurements:

- Oscilloscope:
  - Rev 1.1 (2.5 GT/s) – The PCI-SIG recommends a minimum of 6 GHz system BW for compliance testing. However, some silicon can have rise time in the 50ps range. Thus, Tektronix recommends DPO/DSA70000 8 GHz and above for 2.5 GT/s transmitter measurements.
  - Rev 2.0 (5 GT/s) – DPO/DSA/MSO 70000 12.5 GHz and above are recommended for 5 GT/s and above and required for Base Specification transmitter measurements.
  - Rev 3.0 (8 GT/s) – DPO/DSA/MSO/70000 16 GHz and above are recommended for 8 GT/s measurements.
  - Rev 4.0 (16 GT/s) – DPO/DSA/MSO 70000 25 GHz and above are recommended for 16 GT/s measurements.
  -
- DPOJET software (Version 4.0 or above) with PCI Express Measurements (Opt. PCE, PCE3) installed.
- Probes – See Section 4.2 for probing options.
- Test Fixtures
  - Test Fixtures for System and Add-In card testing are available from the PCI-SIG. Rev1.1 Fixtures (CLB1, CBB1) break transmitter signals out into SMA connections. Rev 2.0 Fixtures (CLB2, CBB2) break transmitter signals out into SMP connections. These fixtures are available at: http://www.pcisig.com/specifications/ordering_information/ordering_information.
  - Test fixtures for ExpressCard testing are available from the following URL: http://www.expresscard.org/web/site/testtools.jsp

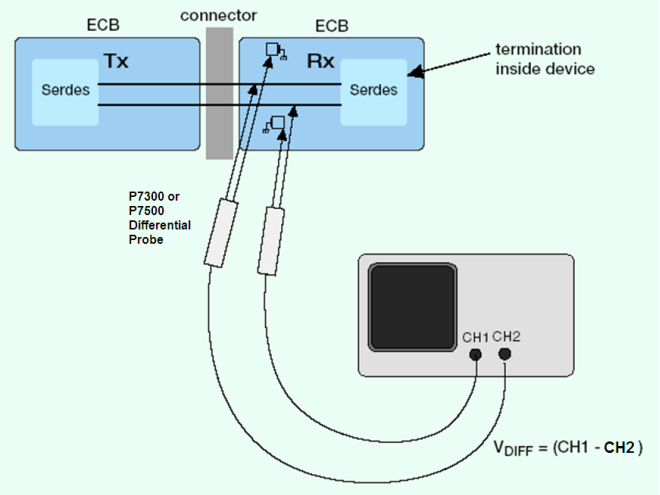
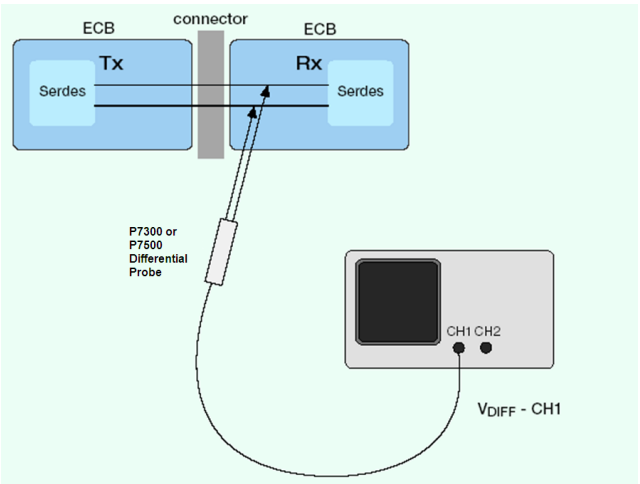
4.2 Probing Options for Transmitter Testing

The first step is to probe the link. Use one of the following four methods to connect probes to the link. Default probing selection is Ch1-Ch2 for single-ended signals, and to create differential signal use Math1=Ch1-Ch2.

4.2.1 SMA Input Connection

Two TCA-SMA inputs using SMA cables (Ch1) and (Ch2) The differential signal is created from the math waveform (Math1 = Ch1-Ch2). The Common mode AC measurement is also available in this configuration from the common mode waveform (Ch1+Ch3)/2. This probing technique requires breaking the link and terminating into a 50 Ω/side termination of the oscilloscope. While in this mode, the PCI Express SerDes will transmit the compliance test pattern. Ch-Ch de-skew is required using this technique because two channels are used. This configuration does not compensate for cable loss in the SMA cables. The measurement reference plane is at the input of the TCA-SMA connectors on the oscilloscope.	 **SMA Pseudo-differential**
One P7300SMA series differential active probe (Ch1) The differential signal is measured across the termination resistors inside the P7300SMA series probe. This probing technique requires breaking the link. While in this mode, the PCI Express SerDes will transmit the compliance test pattern. Matched cables are provided with the probe to avoid introducing de-skew into the system. Only one channel of the oscilloscope is used. The P7300SMA provides a calibrated system at the Test Fixture attachment point, eliminating the need to compensate for cable loss associated with the probe configuration A.	 **SMA Input Differential Probe**

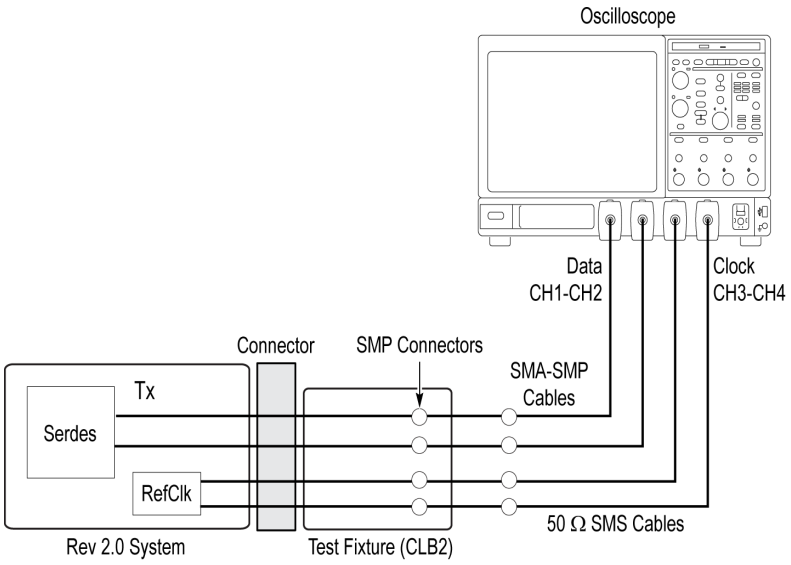
4.2.2 ECB pad connection

Two active probes (Ch1) and (Ch2) The differential signal is created from the math waveform (Math1 = Ch1-Ch2). The Common mode AC/DC measurements are available in this configuration from the common mode waveform (Ch1+Ch3)/2. This probing technique can be used for either a live link that is transmitting data, or a link that has terminated into a "dummy load." In both cases, the single-ended signals should be probed as close as possible to the termination resistors on both sides with the shortest ground connection possible. Ch-Ch de-skew is required using this technique because two channels are used.	
One P7300 or P7500 series Differential probe (Ch1) The differential signal is measured directly across the termination resistors. This probing technique can be used for either a live link that is transmitting data, or a link that is terminated into a "dummy load." In both cases, the signals should be probed as close as possible to the termination resistors. De-skew is not necessary because a single channel of the oscilloscope is used. If using a P7500 Tri-Mode Probe, common mode voltage measurements can be made directly with the probe.	

4.2.3 Dual Port Connection

A. Dual Port

For Rev 2.0 and 3.0 System testing (Described in Section 2.4), the 'Dual Port' method is used to capture differential Data and RefClk. Direct SMA input can be used (where Data =Math1=Ch1-Ch2 and RefClk=Math2=Ch3-Ch4); or Two P7313SMA probes can be used (where Data = Ch1 and RefClk = Ch2).



4.3 SX Scope Support

PCIE solution is supported on Tektronix SX scope models – DPO73304SX, DPO75002SX, DPO75902SX, DPO77002SX. The following are points to note while running measurements on SX scopes

1. When using SX in stacked configuration, always connect both PCIE lanes to the same unit. Do not connect Lane + to one stack and Lane – to another.
2. Setup files need to be manually mapped to the corresponding channels on the SX after they are recalled. Setups can be saved after this to ensure that channels are mapped correctly on subsequent recall.
3. If you are using stacked configurations on the SX with Master and Extension, then the PCIE license needs to be only on Master. If the SX scope is being used as a standalone unit then each scope must have a license.

4.4 Running the Test

The following is a step-by-step procedure on how to run a test in the DPOJET PCI Express Setup Library. Refer to Table 12 for default probing configurations for each Setup.

Source and Reference level Autoset

Below steps are recommended before doing any measurements. However these steps are not required if you are using the setup files.

1. Select the **'Source configuration'** window (Figure below).
2. Press *'**Vertical & Horizontal**'* under **'Source Autoset'.**
3. Press '***Autoset***' under '**Reverence Levels Source Configuration**'

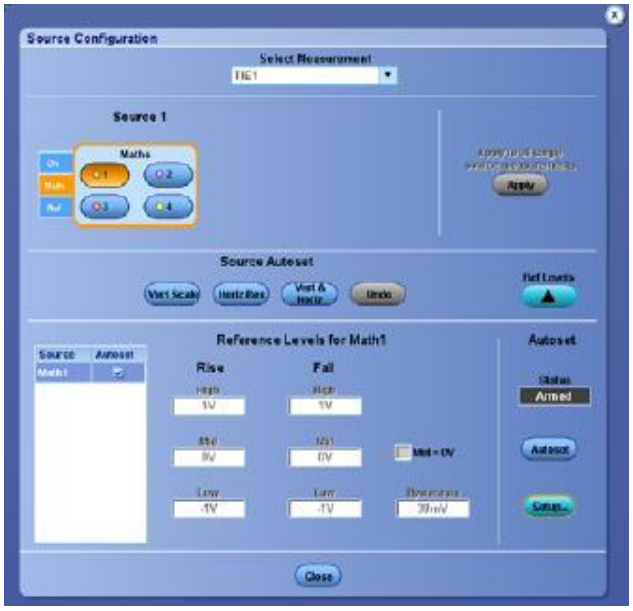


Figure 22: Source Configuration window

4.4.1 Horizontal Setup

Now go to the 'Horiz/Acq' → 'Horizontal /Acquisition Setup' and Select the ***'Manual'*** mode.

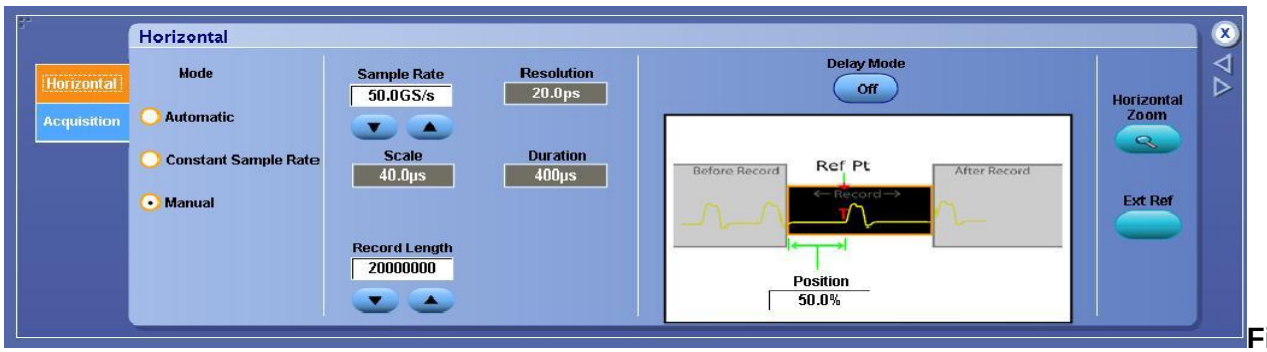


Figure 23: Horizontal setup

Change the 'Record Length' to the required value.

For all the Gen1, Gen 2, Gen 3 measurements 10M record length at 50GS/s sample rate is required to meet the specification.

For all the Gen4 measurements 10M record length at 100GS/s sample rate (we can attain >3 harmonics) is required to meet the specification

From Acquisition, select Acquisition Mode to ‘Sample’ and Sampling Mode to ‘Real Time’.

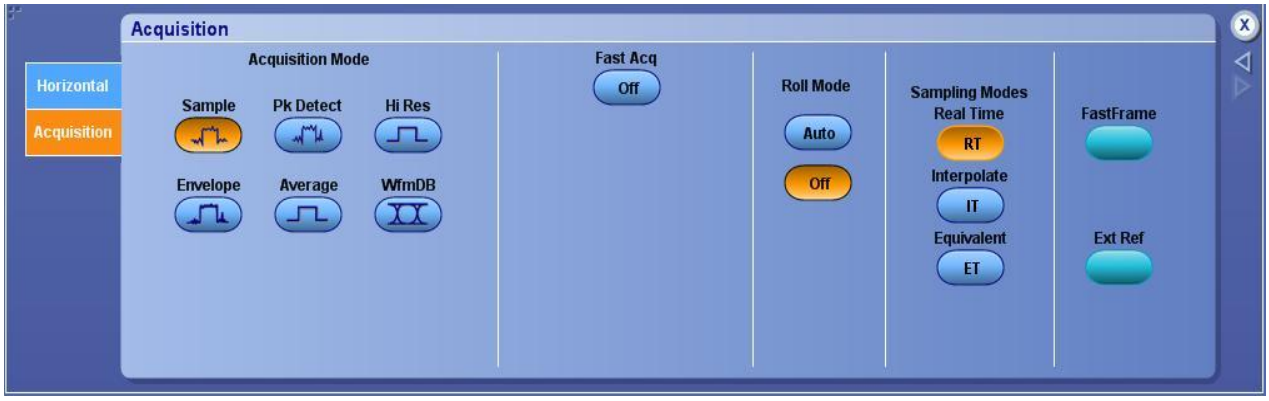


Figure 24: Acquisition setup

4.4.2 Vertical Setup:

Now, from Vertical Settings, Termination→ 50 Ω and Bandwidth to 16GHz if you are using 16GHz or higher BW scopes. Otherwise set it to maximum BW available. Make sure that Digital Filters (DSP) Enabled option is chosen.

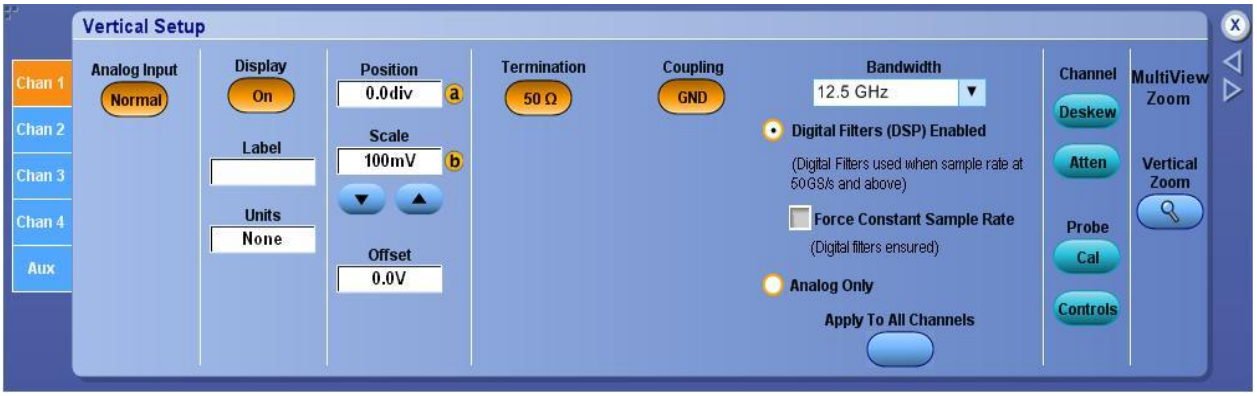


Figure 25: Vertical Setup

On the same window open Channel Deskew and set the following parameters for all the Channels:

Ch<x> Deskew Time →0.0s, External Atten → 1.0 and External Atten(dB)→0.0 dB. These are the default values. If user wants to add Deskew values, select the channel and add Deskew time to align with the other channels.

Figure 26: Channel Deskew

4.4.3 Math Setup:

If user wants to set any specific filter with the Math signal, this is the procedure:

Go to Math → Editor →Filter and then click 'Load'.

Browse required filter file from your saved filters or you can use existing filter files from DPOJET.

Select the filter and then click *'Flt1'* if you have loaded the filter in *'Flt1'*. In the Math Equation Editor, put Math1 = ArbFlt1(Ch1-Ch2) for Gen1, 2.0, 3.0 and Math1 = ArbFlt1(Ch1-Ch3) for Gen 4.0 (then only we can attain 100Gs real time sampling rate in the scope) , if you are using single ended probe.

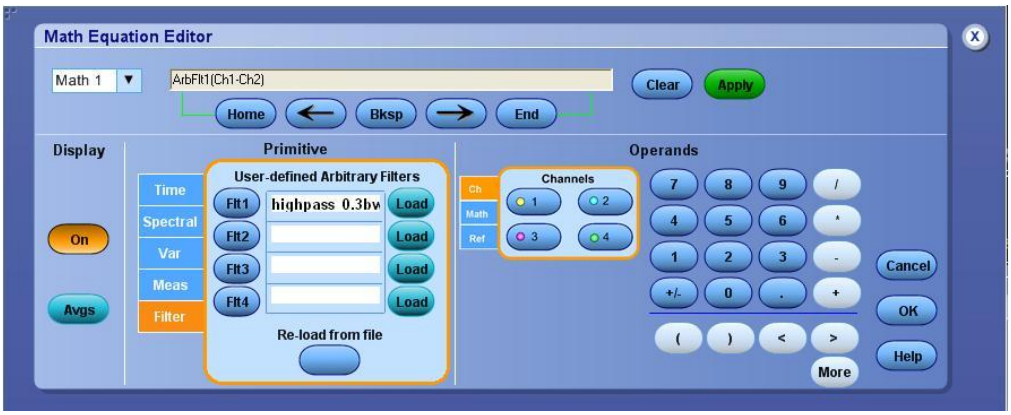


Figure 27: Math Setup

From the DPO/DSA Analysis Menu, Select PCI Express. Allow DPOJET to load.

From the Test Point, Click Setup and navigate to the DPOJET PCIE Setup Library from following path C:\Users\Public\Tektronix\TekApplications\PCI Express\Setups

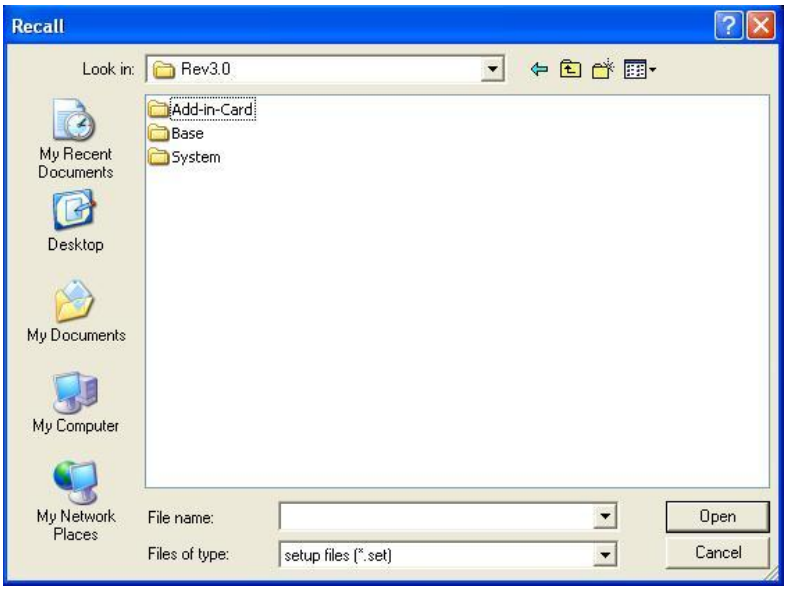


Figure 28: Recall the desired file from the Setup Library.

Press the 'Single' button on the instrument front panel. The screen should look similar to the following image. Adjust Vertical Scale to take full advantage of the A/D range of the oscilloscope enter channel De-Skew values as needed. The Horizontal Scale is set to capture 1 Million UI (10^6 bits) as required by the specifications.

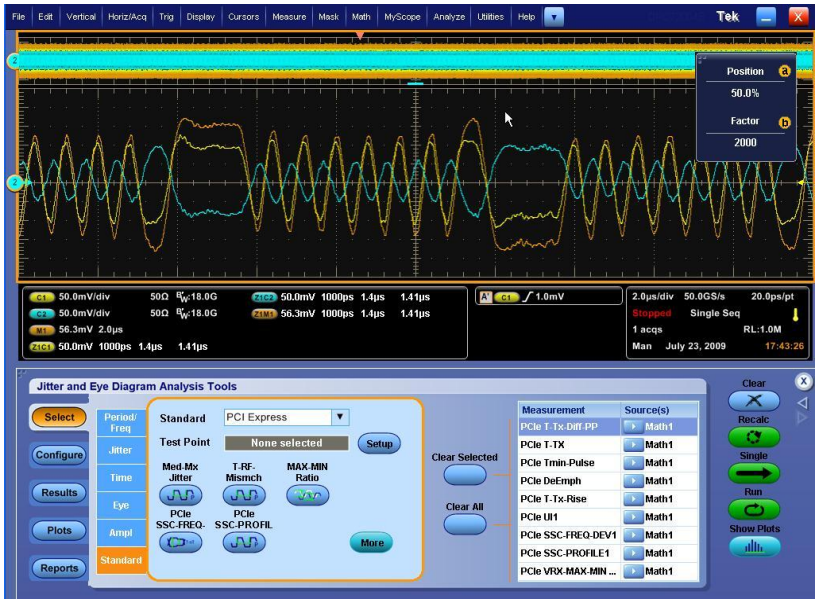


Figure 29: Setting DPOJET measurements

Press the Single Button in DPOJET (Jitter and Eye Analysis Tools) Menu. The end result should look similar to the following screenshot. Pass/Fail results are viewed by expanding the measurement results using the '+' icon next to each measurement.

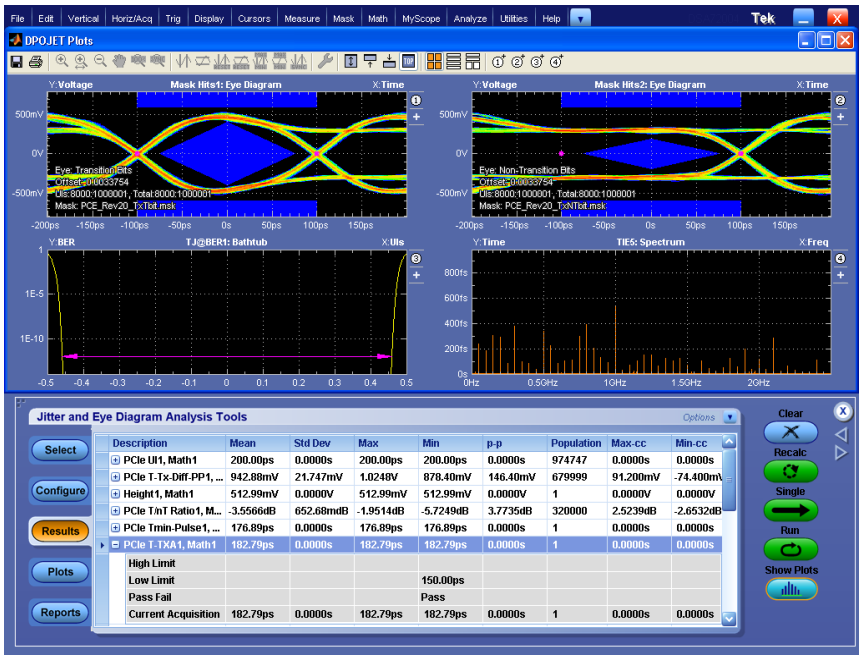


Figure 30: Displaying results in DPOJET panel.

5 Parameter Definitions and Method of Implementation

The DPOJET PCI Express Setup Library combines measurements native to the standard DPOJET package with unique measurements offered in the **Standards > PCI Express** tab of the DPOJET Measurement Select menu. PCI Express specific measurements requires Opt. PCE and DPOJET Version 2.1 or above of is installed on the oscilloscope.

Measurements selected in the setup file are dependent on the specification that is designed to test. Refer to Table 2 through Table 11 for the clock recovery method and for each measurement in the setup file. Refer to the DPOJET OLH (Online Help) for measurement algorithms and setup parameters for measurements native to DPOJET.

The algorithm and setup parameters of the PCI Express specific measurements are described in the following sections.

5.1 UI (Unit Interval) MOI

Definition:

UI (Unit Interval) is defined in the base specification Rev2.0. This measurement is done using the PCIe–UI. The Result panel will display the Unit interval values

Test Definition Notes from the Specification:

The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.

Limits:

Refer to Table 2 thru Table 11 for specified limits on the UI measurement.

Test Procedure:

Ensure that ***PCIe UI*** is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express.

Set the following parameters

Horizontal Record length to at least 500K.

Configure >> Edges >> Auto

Configure >> Filter >> Low pass - 198kHz

Configure >> Global >> off

Measurement Algorithm:

The Unit interval measurement calculates the duration of a cycle as defined by a start and a stop edge. Edges are defined by polarity, threshold, and hysteresis. The application calculates clock period measurement using the following equation:

$$P_n^{Clock} = T_{n+1} - T_n$$

Where:

P^{Clock} is the clock period.

T is the VRefMid crossing time for the selected polarity.

5.2 TX Differential Pk-Pk Output Voltage MOI

Definition:

$V_{TX\text{-}DIFF\text{-}PP}$ (Differential Output Pk-Pk Voltage) is defined in the base specification Rev 2.0. This measurement is done using PCIe T-Tx-Diff-PP. The Result panel would display the Mean , Maximum and Minimum differential output pk-pk voltage.

Test Definition Notes from the Specification:

$$V_{TX-DIFFp-p} = 2*|V_{TX-D+} - V_{TX-D-}|$$

Measured on individual bits, first bit from a sequence in which all bits have same polarity, over specified number of UIs.

Limits:

Refer to Table 2 thru Table 11 for specified limits on the $V_{TX\text{-}DIFF\text{-}PP}$ measurement

Test Procedure:

Ensure that ***PCIe T-Tx-Diff-PP*** is selected in the Jitter and Eye diagram Analysis Tools >> Standard Tab >> PCI Express

Select Configure >> Clock Recovery.

Configure the Clock Recovery to be consistent with the Clock Recovery method shown in Tables 2-13.

Measurement Algorithm:

$V_{TX\text{-}DIFF\text{-}PP}$ is a voltage measurement which measures the absolute difference between the maximum and minimum voltages between similar edges (rise to rise or fall to fall) of the waveform.

5.3 TX De-Emphasis Ratio

Definition:

$V_{TX\text{-}DE\text{-}RATIO}$(De-Emphasized Differential Output Voltage (Ratio)) is defined in the base specification. This measurement uses PCIe DeEmph measurement.

Test Definition Notes from the Specification:

This is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and the following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.

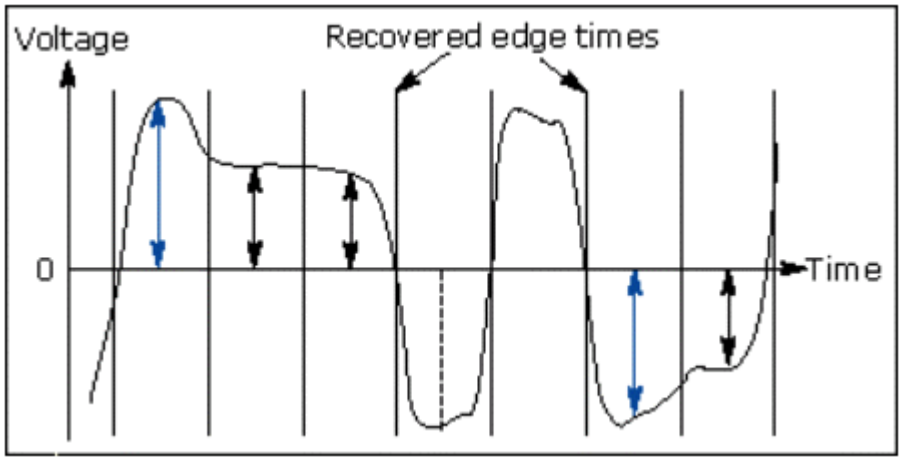
Limits:

Refer to Table 2 thru Table 14 for specified limits on the $V_{TX\text{-}DE\text{-}RATIO}$ measurement.

Measurement Algorithm:

The De-emphasis Ratio measurement reports the amplitude ratio between transition and non-transition bits.

The measurement calculates the ratios of all non-transition eye voltages (2nd and subsequent eye voltages after one edge but before the next) to their nearest preceding transition eye voltage (1st eye voltage succeeding an edge). In the accompanying diagram, it is the ratio of the Black voltages to the Blue voltages. The results are given in dB.



The application calculates the T/nT(transition to non-transition) Ratio using the following equations:

$$DEEM(m) = dB\left(\frac{v_{EYE-HI-NTRAN}(m)}{v_{EYE-HI-TRAN}(n)}\right)$$

following a rising edge.

$$DEEM(m) = dB\left(\frac{v_{EYE-LO-NTRAN}(m)}{v_{EYE-LO-TRAN}(n)}\right)$$

following a falling edge.

Where:

$v_{EYE-HI-TRAN}$ is the High voltage at the interpolated midpoint of the first unit interval following a positive transition.

$v_{EYE-LO-TRAN}$ is the Low voltage at the interpolated midpoint of the first unit interval following a negative transition.

$v_{EYE-HI-NTRAN}$ is the High voltage at the interpolated midpoint of all unit intervals except the first following a positive transition.

$v_{EYE-LO-NTRAN}$ is the Low voltage at the interpolated midpoint of all unit intervals except the first following a negative transition.

m is the index for all non-transition UIs.

n is the index for the nearest transition UI preceding the UI specified by *m*.

In a time trend plot of the measurement results, there is one measurement for each non-transition bit in the waveform (that is the black arrows in the diagram).

NOTE. PCIe DeEmph measurement uses Brick Wall filter.

5.4 TX Minimum Pulse Width MOI

Definition:

$T_{MIN-PULSE}$ (Instantaneous lone pulse width measurement) is defined in the base specification Rev2.0. This measurement uses the PCIe Tmin-Pulse. The Result panel would display the minimum pulse width results.

Test Definition Notes from the Specification:

$T_{MIN-PULSE}$ (Instantaneous lone pulse width measurement) is measured from transition center to the next transition center, and that the transition centers will not always occur at the differential zero crossing point. In particular, transitions from a de-emphasized level to a full level will have a center point offset from the differential zero crossing.

Limits:

Refer to Table 2 thru Table 14 for specified limits on the $T_{MIN-PULSE}$ measurement

Test Procedure:

Ensure that ***PCIe Tmin-Pulse*** is selected in the Jitter and Eye diagram Analysis Tools > Select menu.

Set the following parameters

Select Configure > Clock Recovery. Configure the Clock Recovery to be consistent with the Clock Recovery method shown in Tables 2-14.

Configure > General >Off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

Tmin-Pulse (minimum single pulse width $T_{Min-Pulse}$) is measured from one transition center to the next.

The application calculates $T_{Min-Pulse}$ using the following equation:

$$T_{Min-Pulse} = (T_{n+1} - T_n)$$

Where:

TMin-Pulse is the minimum pulse width

T is the transition center

5.5 TX Rise/Fall Time Mismatch MOI

Definition:

$T_{RF\text{-}MISMATCH}$ (Rise time, Fall time mismatch) is defined in the base specification**.** This measurement uses PCIe T-RF-Mismch. The Result panel would display the Mean , Maximum and Minimum Rise time, Fall time mismatch values.

Limits:

Refer to Table 2 through Table 14 for $T_{RF\text{-}MISMATCH}$ measurement.

Test Procedure:

Ensure that *PCIe T-RF-Mismch* is selected in Jitter and Eye diagram Analysis Tools > Select menu is selected.

Set the following parameters

Select Configure > Clock Recovery. Configure the Clock Recovery to be consistent with the Clock Recovery method shown in Tables 2-14.

Configure > Filter > No filter

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

PCIe T-RF-Mismch (Rise and Fall Time mismatch measurement) is the mismatch between Rise time (TRise) and Fall time(TFall). The application calculates this measurement using the following equation:

$$T_n^{Mismatch} = abs(T_n^{Rise} - T_n^{Fall})$$

Where:

$T^{Mismatch}$ is the rise and fall time mismatch

T^{Rise} is the rise time

T^{Fall} is the fall time

5.6 Minimum TX Eye Width MOI

Definition:

T_{TX-EYE} (Minimum TX Eye Width) is defined in the base specification. . See Section 4.7.2 of PCI Express Card Electromechanical Specification, Rev. 2.0 for the Gen2 definition for both 3.5 dB and 6 dB De-emphasis. The eye diagrams defined in this section represent the compliance eye diagrams that must

be met for both add-in card and a system board interfacing with such an add-in card. A sample size of 10^6 UI is assumed for the measurement.

T_{TX-EYE} is defined to be the Jitter Eye Opening.

Test Definition Notes from the Specification:

Limits:

Refer to Table 2 thru Table 14 on the T_{TX-EYE} measurement.

Test Procedure:

Ensure that the measurement *PCI T-TX* is selected in the Jitter and Eye diagram Analysis Tools > Select menu.

Configure the measurement by setting the following parameters.

Select Configure > Clock Recovery. Configure the Clock Recovery to be consistent with the Clock Recovery method shown in Tables 2-14.

Configure > General > off.

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

The measured minimum horizontal eye opening at the zero reference level as shown in the eye diagram below.

$$T_{EYE-WIDTH} = UI_{AVG} - TIE_{Pk-Pk}$$

Where: UI_{AVG} is the average *UI*

TIE_{Pk-Pk} is the Peak-Peak *TIE*

Where T_{txA} is the Eye width, V_{txA} is the full scale peak to peak voltage and V_{txA_d} is the De-emphasized peak to peak voltage.

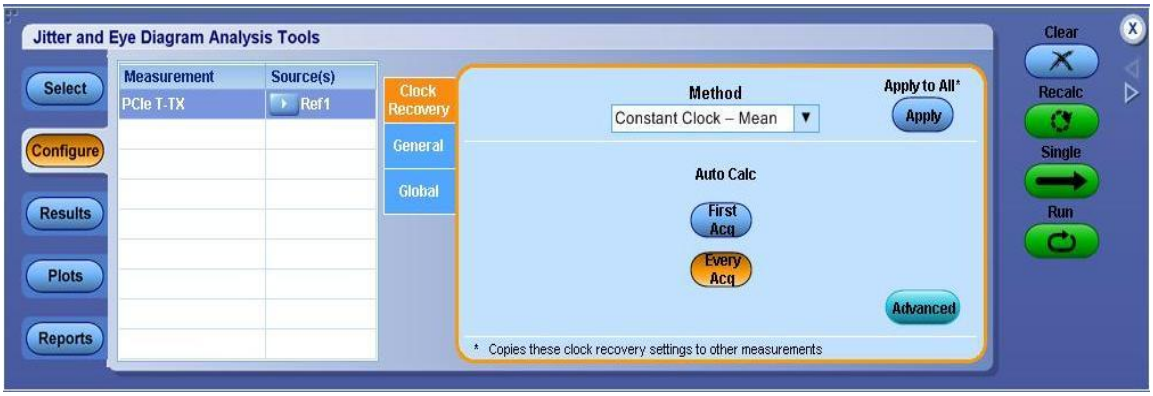


Figure 31: Configure Panel

5.7 TX Median-to-Max Jitter MOI

Definition:

$T_{TX-EYEMEDIAN-to-MAXJITTER}$ (maximum time between the jitter median and maximum deviation from the median). A step response Band pass filter is being used to remove the low frequency jitter as specified in Rev2.0 of the base specification.

Limits:

Refer to Table 2 thru Table 14 for $T_{TX-EYEMEDIAN-to-MAXJITTER}$ measurement.

Test Procedure:

Ensure that *PCIe Med-Mx Jitter* is selected in Jitter and Eye diagram Analysis Tools > Select menu is selected.

Set the following parameters

Configure > Edges > Signal Type > Auto

Select Configure > Clock Recovery. Configure the Clock Recovery to be consistent with the Clock Recovery method shown in Tables 2-14.

Configure > Filter > Brick Wall Filter

Configure > General >Off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

The measured time difference between a data edge and a recovered clock edge.

$tie(n) = t_{R-DAT}(n) - t_{DAT}(n)$

Where:

t_{DAT} is the original data edge

t_{R-DAT} is the recovered data edge (for example, the recovered clock edge corresponding to the UI boundary of t_{DAT})

n is the index of all edges in the waveform

*Med_*T*ie*= median (tie (*n))*

Where:

*Med_*T*ie* is the Median of the tie measured.

$T_{Tx\text{-}EYEMEDIAN\text{-}to\ MAXJitter}$ = *Abs (Med_*T*ie – Maximum deviation of tie (n) from the Med_*T*ie)*

5.8 VRX Max-Min Ratio (Voltage) MOI

Definition:

$V_{RX\text{-}MAX\text{-}MIN\text{-}RATIO}$ defines the voltage range ratio over which a particular receiver must operate for the consecutive UI. Figure 12 shows a typical voltage plot into a reference load that yields a near worst case VRX-MAX-MIN-RATIO. VSWING-MAX is defined in relation to VSWING-MIN over an interval of 2.0 UI. The right hand side of the 2 UI intervals is placed on the peak of the waveform corresponding to VSWING-MIN. The 2 UI separation guarantees that VSWING-MAX. A 2 UI interval guarantees that VSWING-MAX is measured on the flat portion of its curve and accounts for worst case jitter and dispersive channel effects.

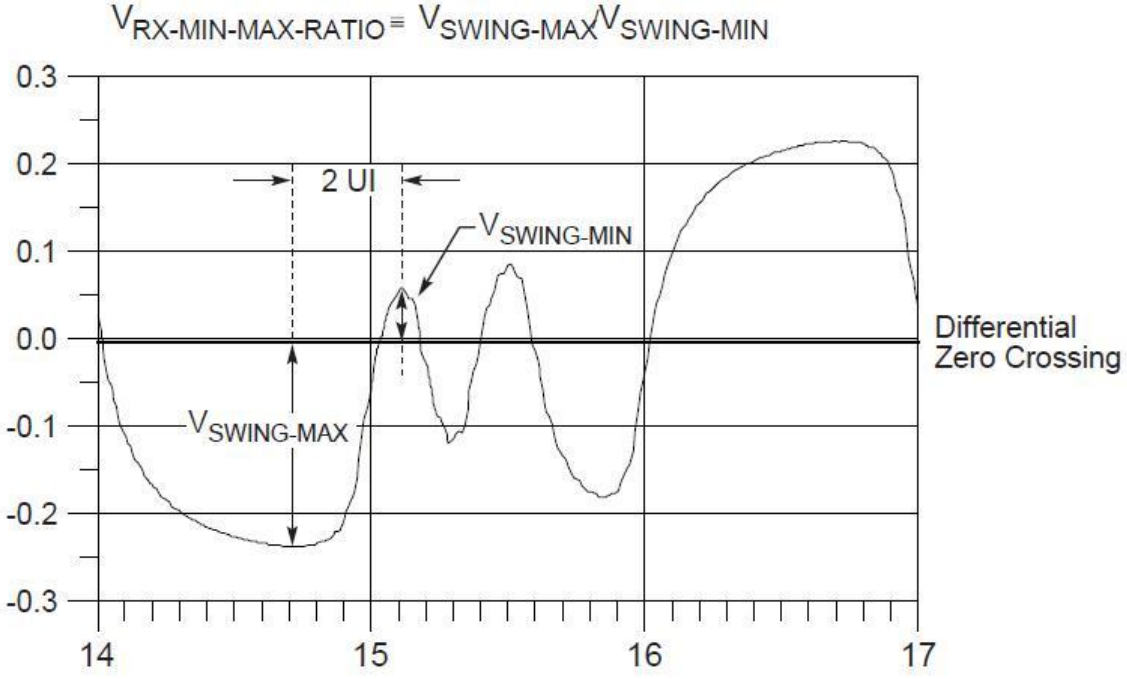


Figure 32: Signal at Receiver Reference Load Showing Min/Max Swing

Limits:

Refer to Table 2 thru Table 14 for VRX-MAX-MIN-RATIO measurement.

Test Procedure:

Ensure that *PCIe MAX-MIN Ratio* is selected in Jitter and Eye diagram Analysis Tools > Select menu is selected.

Set the following parameters

Configure > Edges > Signal Type > Auto

Select Configure > Clock Recovery. Configure the Clock Recovery to be consistent with the Clock Recovery method shown in Tables 2-14.

Configure > General >Off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

Find the 50% edges (this may not give the correct 50% edge, However this value allows to identify the edge, and allows to navigate in forward and backward direction from the 50% level, to find out the peak-to peak voltage)

On the rising edge find the V_{SWING_MIN}

From the V_{SWING_MIN} point trace back 2 unit intervals and find the V_{SWING_MAX}

$V_{RX\text{-}MAX\text{-}MIN\text{-}RATIO}$ ($V_{RX\text{-}MAX\text{-}MIN\text{-}RATIO} = V_{SWING\text{-}MAX} / V_{SWING\_MIN}$)

5.9 TX SSC Frequency Deviation MOI

Definition:

SSC Frequency Deviation (or SSC Modulation Profile), can be defined as the frequency shift as a function of time.

Test Definition Notes from the Specification:

The data rate is modulated from 0 to -5000 ppm for nominal data rate frequency and scales with data rate.

This is measured below 2 MHz only.

Limits:

Refer to Table 2 thru Table 14 for specified limits on $T_{SSC\text{-}FREQ\text{-}DEV}$ measurement.

Test Procedure:

Ensure that PCIe SSC-FREQ-DEV is selected in the **Jitter and Eye diagram Analysis Tools** >>**PCI Express** >> **Select** menu.

Select the **Jitter and Eye diagram Analysis Tools >> Configure** from the panel and set the **Configure** >> **Constant Clock-Mean** and,

Configure >> Filter >> Low pass >> 2nd Order >> Frequency >> 1.98 MHz (Which is elected by default) as shown in figure below.

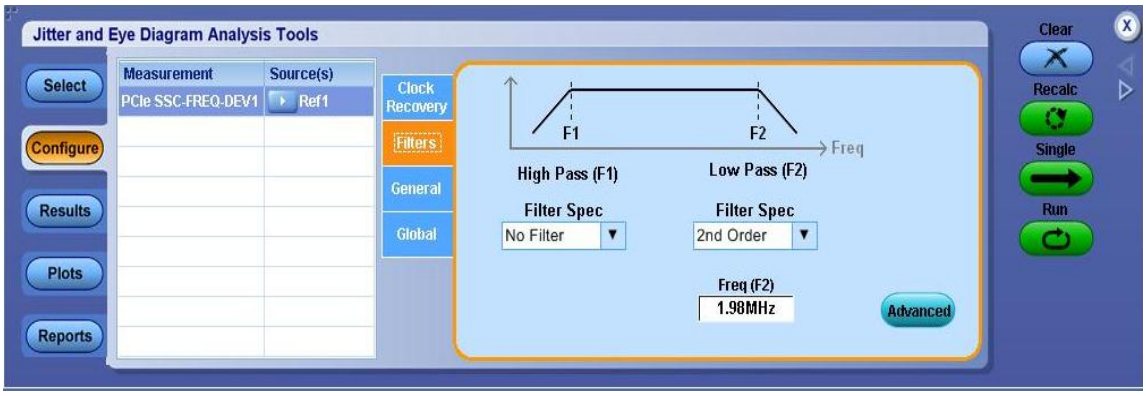


Figure 33: Filter for SSC Frequency Deviation measurement

Configure >> General >>Off

Configure >> Global >> Off

Measurement Algorithm:

Find the 50% edges on the SSC profile

Between the 'n' and 'n+1' th edge find the High value. and also between 'n+1' and 'n+2' edge find the Low.

Find the Frequency deviation as High – Low (FreqDev = High – Low)

Represent the FreqDev in terms of ppm (parts per million)

$FreqDev_{ppm}$ = (nominal data rate – FreqDev)/nominal data rate * 1e6.

5.10 TX Rise Time MOI

Definition:

PCIe T-Tx-Rise is the time difference between the VRefHi(80%) reference level crossing and the VRefLo(20%) reference level crossing on the rising edge of the waveform. The VRefHi and VRefLo are calculated based on the voltage level of the previous UI. There are two distinct thresholds corresponding to de-emphasized transitions from low to high, and full swing transitions for VRefHi and VRefLo.
Limits:

Refer to Table 2 thru Table 14 for TTX-RISE-FALL measurement.

Test Procedure:

Ensure that *PCIe T-Tx-Rise* is selected in Jitter and Eye diagram Analysis Tools >PCI Express > Select menu.

Set the following parameters

Configure > Edges > Signal Type > Auto

Select Configure > Clock Recovery. Configure the Clock Recovery to be consistent with the Clock Recovery method shown in Tables 2-14.

Configure > Bit Config > All Bits(By Default)

Configure > Filter > Brick Wall Filter

Configure > General >Off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

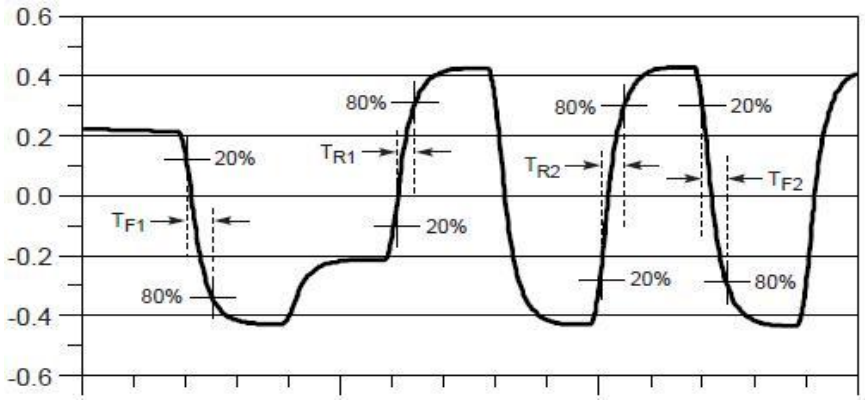


Figure 34. Rise Time Definition

The application calculates this measurement using the following equation:

$$T_n^{Rise} = (T_n^{Hi+} - T_n^{Lo+})$$

Where:

T^{Rise} is the Rise time

T^{Hi+} is the VRefHi crossing on the rising edge

T^{Lo+} is the VRefLo crossing on the rising edge

5.11 TX Fall Time MOI

Definition:

PCIe T-Tx-Fall is the time difference between the VRefLo(20%) reference level crossing and the VRefHi(80%) reference level crossing on the falling edge of the waveform. The VRefLo and VRefHi are calculated based on the voltage level of the previous UI. There are two distinct thresholds corresponding to de-emphasized transitions from high to low, and full swing transitions for VRefLo and VRefHi.

Limits:

Refer to Table 2 thru Table 14 for $T_{TX\text{-}RISE\text{-}FALL}$ measurement.

Test Procedure:

Ensure that *PCIe T-Tx-Fall* is selected in Jitter and Eye diagram Analysis Tools >PCI Express > Select menu.

Set the following parameters

Configure > Edges > Signal Type > Auto

Select Configure > Clock Recovery. Configure the Clock Recovery to be consistent with the Clock Recovery method shown in Tables 2-14.

Configure > Bit Config > All Bits(By Default)

Configure > Filter > Brick Wall Filter

Configure > General >Off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

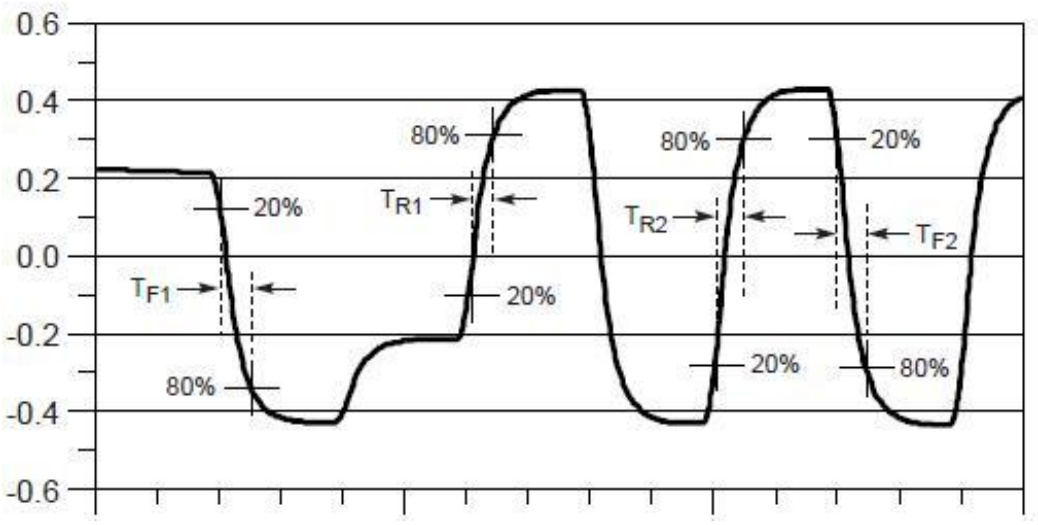


Figure 35. Fall Time Definition

The application calculates this measurement using the following equation:

$$T_n^{Fall} = (T_n^{Lo+} - T_n^{Hi+})$$

Where:

T^{Fall} is the Fall time

T^{Lo-} is the VRefLo crossing on the falling edge

T^{Hi-} is the VRefHi crossing on the falling edge

5.12 Data Dependent Jitter MOI(T_{TX-DDJ})

Definition:

T-TX-DDJ (Data Dependent Jitter) is defined in the Gen3/ Gen4 base specification .This measurement is done using the T-TX-DDJ. The Result panel would display the Data Dependent Jitter values.

Test Definition Notes from the Specification:

Data dependent jitter is defined as the time delta between the PDF's mean for each zero crossing point and the corresponding recovered clock edge.

Limits:

Refer to Table 3 for specified limits on the T-TX-DDJ measurement.

Test Procedure:

Ensure that *T-TX-DDJ* is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0 / PCI Express 4.0.

Set the following parameters:

Horizontal Record length to at least 500K.

Configure >> Clock Recovery >> PLL Custom BW >> Type I >>Loop BW>> 10MHz

Configure >> General >> off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

Separation of jitter into data dependent and uncorrelated components may be achieved by averaging techniques since DDj is bounded a peak to peak measurement is derived. DDj is then the range of the distribution.

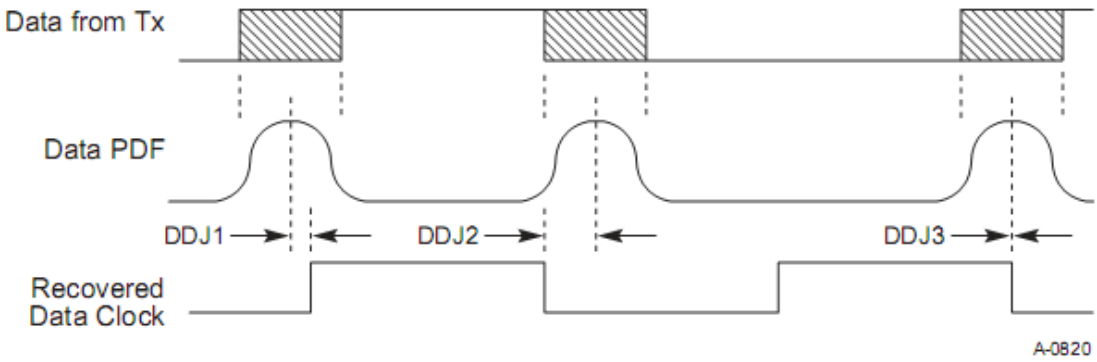


Figure 36: Relation between Data Edge PDF and Recovered Data Clock.

Steps for doing the measurement:

1. Recover the clock and convert to a bit stream.
2. Find the repeating patterns (i.e. compliance pattern in case of gen3 / gen4) and find the *Pattern_Length* and *Pattern_Repeate_Count*
3. Determine the deterministic/correlated jitter.

   For k =0 to *Pattern_Length* find

   For i = 0 to *Pattern_Repeate_Count* find

   $$EdgeJitter_i = Edge_i - RecoveredClockEdge_i$$

   Find $CorrelatedJitter_k$ = mean (EdgeJitter)

   End
4. Calculate Data dependent jitter as

   Datsa dependent jitter = max(*CorrelatedJitter*) - min(*CorrelatedJitter*)

5.13 Uncorrelated Total Jitter (T_{TX-UTJ})

Definition:

T-TX-UTJ (Uncorrelated Total Jitter) is defined in the Gen3/ Gen4 base specification. This measurement is done using the T-TX-UTJ. **The Result panel would display the Uncorrelated Total Jitter values.**

Test Definition Notes from the Specification:

This type of jitter is referenced to a recovered data clock generated by means of a CDR tracking function. Uncorrelated total jitter may be derived after removing the DDJ component from each PDF and combining the PDFs for all edges in the pattern.

Limits:

Refer to Table 3 for specified limits on the T-TX-UTJ measurement.

Test Procedure:

Ensure that *T-TX-UTJ* is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0 / PCI Express 4.0.

Set the following parameters:

Horizontal Record length to at least 500K.

Configure >> Clock Recovery >> PLL Custom BW >> Type I >>Loop BW >> 10MHz

Configure >> BER >> 1E-12

Configure >> General >> off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

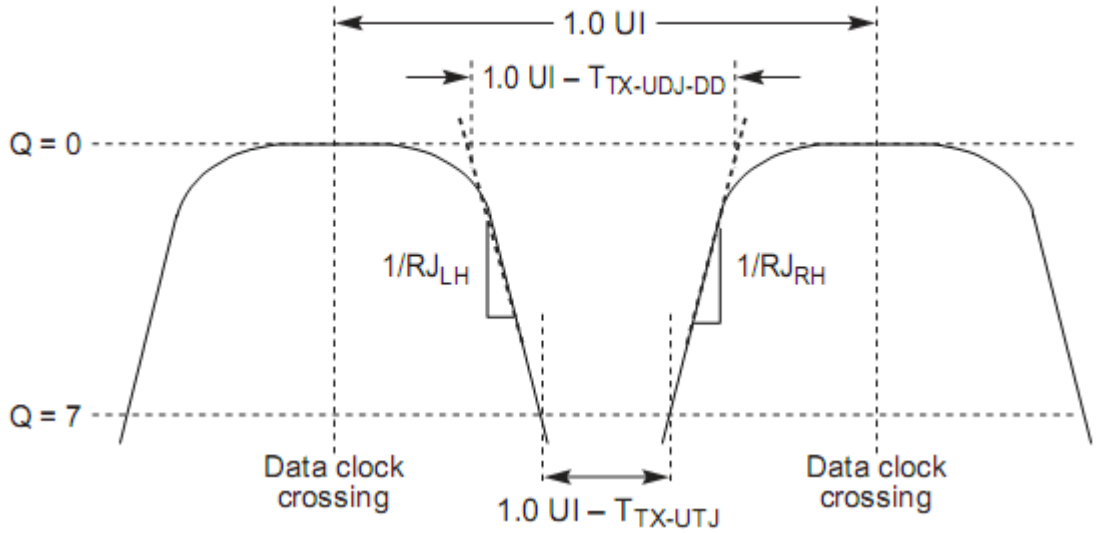


Figure 37: Derivation of T_{TX-UTJ} and $T_{TX-UDJDD}$

Steps for doing the measurement:

1. Recover the clock and convert it bit stream.
2. Find the repeating patterns and find the *Pattern_Length* and *Pattern_Repeate_Count*
3. Determine the deterministic/correlated jitter and eliminate it from the samples.

   For *k* =0 to *Pattern_Length* find

   For *i* = 0 to *Pattern_Repeate_Count* find

   $EdgeJitter_i = Edge_i - RecoveredClockEdge_i$

   Find $CorrelatedJitter_k$ = mean (EdgeJitter)

   //find un-correlated max and min jitter values by removing the correlated jitter values

   //$uncorrelatedJitter_k = EdgeJitter - CorrelatedJitter_k$

   max_uncorrelatedJitter = max(max_uncorrelatedJitter, $EdgeJitter - CorrelatedJitter_k$)

   min_uncorrelatedJitter = max(min_uncorrelatedJitter, $EdgeJitter - CorrelatedJitter_k$)

   End
4. Find the absolute maximum un correlated jitter (*max_abs_uj*)
5. Based on the *max_abs_uj* create a histogram with appropriate bin length (this is used for creating the PDF).
6. Create the PDF and combine all the PDFs for all the edges
7. Convert the PDF into Q scale and draw a Gaussian line(Gaussian Fit) to calculate Vertical opening on left side and right side of the Q-scale curve and use these values to calculate Uncorrelated Total Jitter(T_TX_UTJ) = vertical open left – vertical open right.

5.14 Uncorrelated Deterministic Jitter($T_{TX-UDJDD}$)

Definition:

T-TX-UDJDD (Uncorrelated Total Jitter) is defined in the Gen3/ Gen4 base specification. This measurement is done using the T-TX- UDJDD. **The Result panel would display the Uncorrelated Deterministic Jitter values.**

Test Definition Notes from the Specification:

Uncorrelated deterministic jitter is defined as uncorrelated jitter at the zero crossing point and the corresponding recovered clock edge.

Limits:

Refer to Table 3 for specified limits on the T-TX-UDJDD measurement.

Test Procedure:

Ensure that *T-TX-UDJDD* is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0 / PCI Express 4.0

Set the following parameters:Horizontal Record length to at least 500K.

Configure >> Clock Recovery >> PLL Custom BW >> Type I>>Loop BW >> 10MHz

Configure >> BER >> 1E-12

Configure >> General >> off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

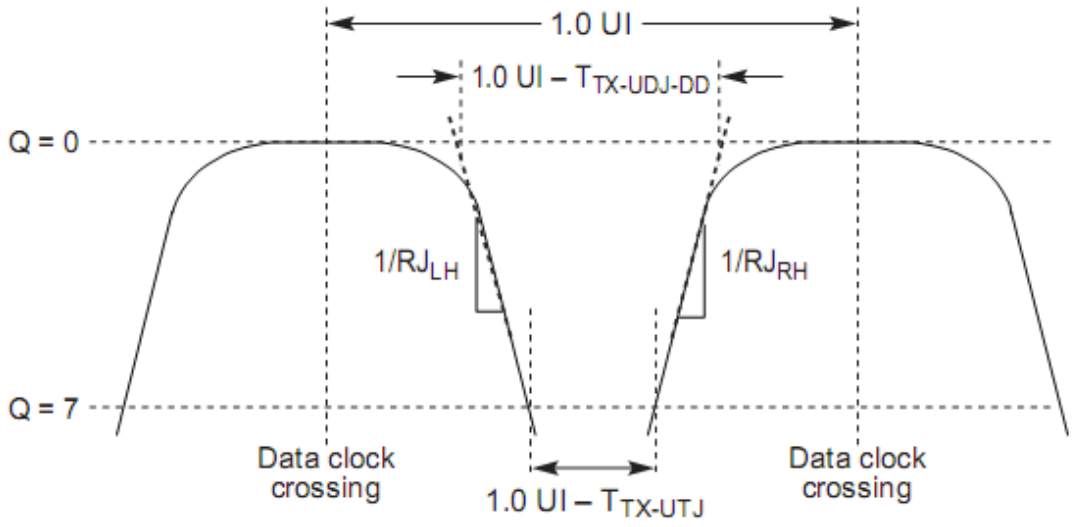


Figure 38: Derivation of TTX-UDJDD

Steps for doing the measurement:

1. Recover the clock and convert it bit stream.
2. Find the repeating patterns and find the *Pattern_Length* and *Pattern_Repeate_Count*
3. Determine the deterministic/correlated jitter and eliminate it from the samples.

For *k* =0 to *Pattern_Length* find

For *i* = 0 to *Pattern_Repeate_Count* find

$EdgeJitter_i = Edge_i – RecoveredClockEdge_i$

Find $CorrelatedJitter_k$ = mean (EdgeJitter)

//find un-correlated max and min jitter values by removing the correlated jitter values

$//uncorrelatedJitter_k = EdgeJitter - CorrelatedJitter_k$

max_uncorrelatedJitter = max(max_uncorrelatedJitter, EdgeJitter - $CorrelatedJitter_k$)

min_uncorrelatedJitter = max(min_uncorrelatedJitter, EdgeJitter - $CorrelatedJitter_k$)

End

4. Find the absolute maximum un correlated jitter (*max_abs_uj*)

5. Based on the *max_abs_uj* create a histogram with appropriate bin length(this is used for creating the PDF).
6. Create the PDF and combine all the PDFs for all the edges
7. Convert the PDF into Q scale and draw a Gaussian line(Gaussian Fit) on left side and right side
8. Find where the Gaussian line intercept with Q=0 for both right and left linear fit and calculate TTX-UDJDD.

5.15 Uncorrelated Total Pulse Width Jitter ($T_{TX\text{-}UPW\text{-}TJ}$)

Definition:

T-TX-UPW-TJ (Uncorrelated Total Pulse Width Jitter) is defined in the Gen3/ Gen4 base specification. This measurement is done using the T-TX- UPW-TJ. **The Result panel would display the Uncorrelated Total Pulse Width Jitter values.**

Test Definition Notes from the Specification:

Pulse width jitter is defined as an edge to edge phenomenon on consecutive edges.

Limits:

Refer to Table 3 for specified limits on the T-TX-UPW-TJ measurement.

Test Procedure:

Ensure that *T-TX-UPW-TJ* is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0 / PCI Express 4.0

Set the following parameters:

Horizontal Record length to at least 500K.

Configure >> Clock Recovery >> PLL Custom BW >> Type I >>Loop BW >> 10MHz

Configure >> BER >> 1E-12

Configure >> General >> off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

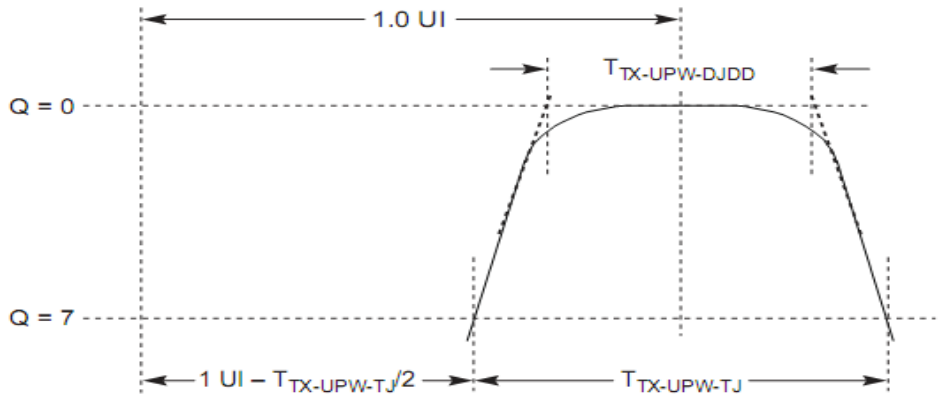


Figure 39: Definition of TTX-UPW-TJ

Steps for doing the measurement:

1. Recover the clock and convert it bit stream.
2. Find the repeating patterns and find the *Pattern_Length* and *Pattern_Repeate_Count*
3. Find the correlated jitter

For *k* =0 to *Pattern_Length* find

For *i* = 0 to *Pattern_Repeate_Count* find

$EdgeJitter_i = Edge_i – RecoveredClockEdge_i$

Find $CorrelatedJitter_k$ = mean (EdgeJitter)

End

4. Calculate the correlated jitter for each of the pattern repeat.
5. Calculate the PWJ referencing to a fixed leading edge and having jitter contributions from both edges appear at the trailing edge and calculate the *median_pwj*.
6. Based on the *median_pwj* find the appropriate histogram and fit all the PWJ in this histogram to create the PDF.
7. Calculate the Q-Scale extrapolation for this PWJ-PDF
8. Vertical opening on left side and right side of the Q-scale curve and use these values to calculate Uncorrelated Total PWJ(TX-UPW-TJ) = vertical open left – vertical open right.

5.16 Uncorrelated Deterministic Pulse Width Jitter ($T_{TX-UPW-DJDD}$)

Definition:

T-TX-UPW-DJDD (Uncorrelated Deterministic Pulse Width Jitter) is defined in the Gen3/ Gen4 base specification. This measurement is done using the T-TX-UPW-DJDD. The Result panel would display the Uncorrelated Deterministic Pulse Width Jitter values.

Test Definition Notes from the Specification:

Uncorrelated Deterministic PWJ is defined as uncorrelated PWJ at the zero crossing.

Limits:

Refer to Table 3 for specified limits on the T-TX-UPW-DJDD measurement.

Test Procedure:

Ensure that T-TX-UPW-DJDD is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0 / PCI Express 4.0

Set the following parameters:

Horizontal Record length to at least 500K.

Configure >> Clock Recovery >> PLL Custom BW >> Type I >>Loop BW >> 10MHz

Configure >> BER >> 1E-12

Configure >> General >> off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

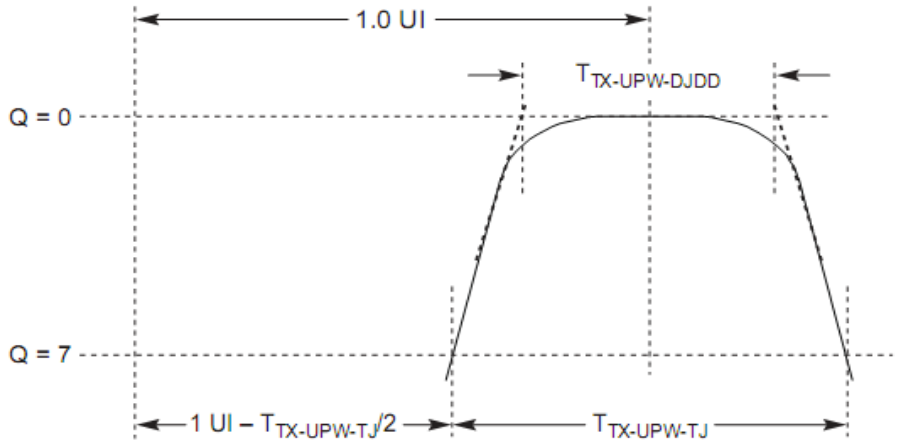


Figure 40: Definition of TTX-UPW-DJDD

Steps for doing the measurement:

1. Recover the clock and convert it bit stream.
2. Find the repeating patterns and find the *Pattern_Length* and *Pattern_Repeate_Count*
3. Find the correlated jitter

   For k =0 to *Pattern_Length* find

   For i = 0 to *Pattern_Repeate_Count* find

   $EdgeJitter_i = Edge_i – RecoveredClockEdge_i$

   Find $CorrelatedJitter_k$ = mean (EdgeJitter)

   End
4. Replicate the correlated jitter for each of the pattern repeat.
5. Calculate the PWJ referencing to a fixed leading edge and having jitter contributions from both edges appear at the trailing edge and calculate the *Median_pwj*.

6. Based on the *Median_pwj* find the appropriate histogram and fit all the PWJ in this histogram to create the PDF.
7. Calculate the Q-Scale extrapolation for this PWJ-PDF
8. Find where the Gaussian line crosses the zero crossing and calculate the uncorrelated Deterministic PWJ(TTX-UPW-DJDD)

5.17 Voltage swing with No Equalizer ($V_{TX\text{-}NO\text{-}EQ}$)

Definition:

V-TX-NO-EQ (Voltage swing with No Equalizer) is defined in the Gen3/ Gen4 base specification. This measurement is done using the V-TX-NO-EQ. The Result panel would display the voltage swing without any equalization values.

Test Definition Notes from the Specification:

VTX-NO-EQ is defined by setting c_{-1} and c_{+1} to zero and measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern.

Limits:

Refer to Table 3 for specified limits on the V-TX-NO-EQ measurement.

Test Procedure:

Ensure that *V-TX-NO-EQ* is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0 / PCI Express 4.0

Set the following parameters:

Horizontal Record length to at least 500K.

Configure >> Clock Recovery >> PLL Custom BW >> Type I>>Loop BW >> 10MHz

Configure >> Global >> off

Configure >> Global >> off

Measurement Algorithm:

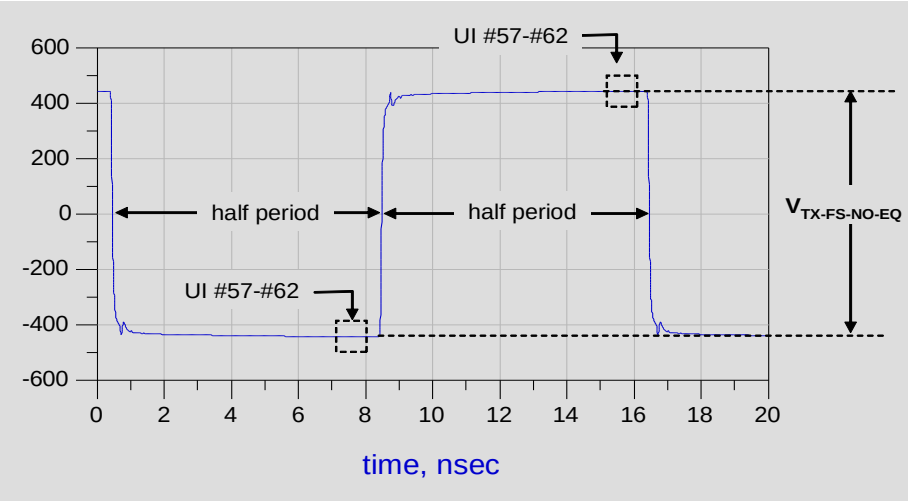


Figure 41: No Equalization PP Tx Voltage definition

1. Find the 64 zeros/64 ones between two consecutive edges.
2. Find the voltage between 57th UI to 62nd UI of positive cycle and negative cycle.
3. Calculate the average voltage of the positive and negative cycle.
4. Find the voltage difference between positive and negative cycles.

5.18 P-P voltage swing in EIEOS sequence ($V_{TX-EIEOS}$)

Definition:

V-TX-EIEOS (P-P voltage swing in EIEOS sequence) is defined in the Gen3/ Gen4 base specification.This measurement is done using the V-TX-EIEOS. The Result panel would display the voltage swing in EIEOS sequence.

Test Definition Notes from the Specification:

VTX-EIEOS is defined by measuring the p-p voltage on the EIEOS sequence (8-ones/8-zeroes segment of the compliance pattern), where the pattern is repeated for a total of 128 UI.

Limits:

Refer to Table 3 for specified limits on the V-TX-EIEOS measurement.

Test Procedure:

Ensure that V-*TX-EIEOS* is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0 / PCI Express 4.0.

Set the following parameters:

Horizontal Record length to at least 500K.

Configure >> Clock Recovery >> PLL Custom BW >> Type I >>Loop BW >> 10MHz

Configure >> General >> off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

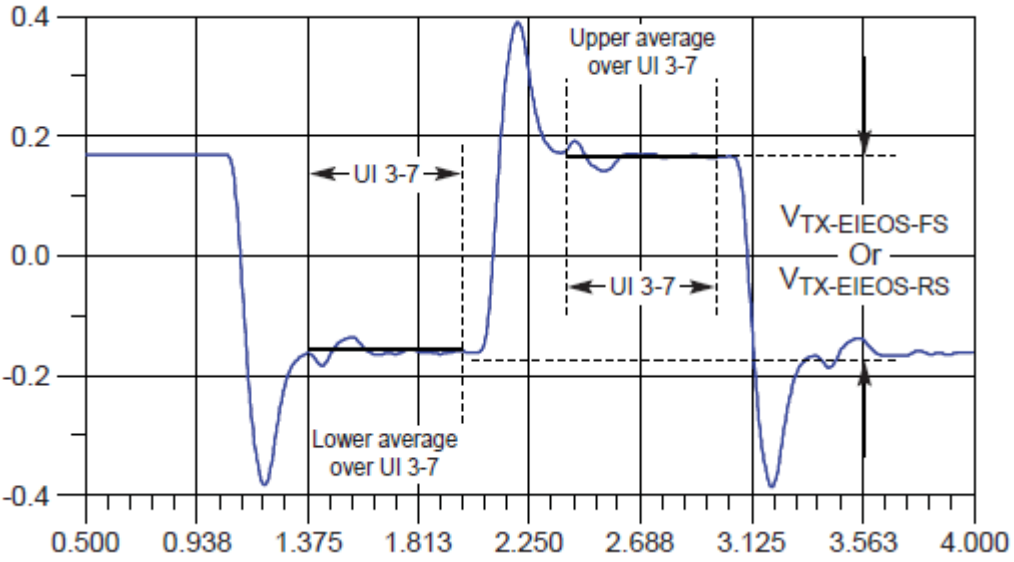


Figure 42: EIEOS PP Tx Voltage definition.

1. Find the 8 zeros/8 ones between two consecutive edges.
2. Find the voltage between 3rd UI to 7th UI of positive cycle and negative cycle.
3. Calculate the average voltage of the positive and negative cycle.
4. Find the voltage difference between positive and negative cycles.

5.19 Effective Tx package Loss ratio($Ps21_{TX}$)

Definition:

Ps21Tx (P-P voltage swing in EIEOS sequence) is defined in the Gen3/ Gen4 base specification. This measurement is done using the ps21Tx. The result panel would display

Test Definition Notes from the Specification:

Package loss is measured by comparing the 64-zeroes/64-ones voltage swingPP voltage (V111) against a 1010 pattern (V101). Tx package loss measurement is made with c-1 and c+1 both set to zero.

Limits:

Refer to Table 3 for specified limits on the Ps21Tx measurement.

Test Procedure:

Ensure that *ps21Tx* is selected in the Jitter and Eye diagram Analysis Tools >> >> Select Standard Tab >> PCI Express 3.0 / PCI Express 4.0

Set the following parameters:

Horizontal Record length to at least 500K.

Configure >> Clock Recovery >> PLL Custom BW >> Type I>>Loop BW >> 10MHz

Configure >> General >> off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

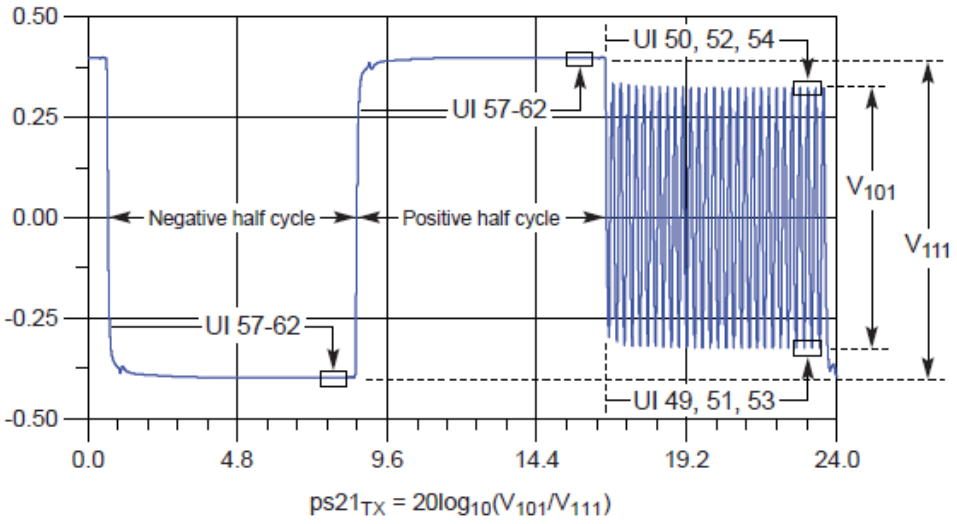


Figure 43: Effective Tx package Loss Ratio definition.

1. Find the 1010 bit pattern (V_{101}) for 128 UI in the compliance pattern.
2. Find 64 ones/64zeros bit pattern (V_{111}) adjacent to 1010 pattern.
3. Find the 50,52 and 54th bits from positive UIs and 49,51 and 53rd bits from negative UIs of 1010 bit pattern.
4. Calculate the peak to peak voltage difference between positive and negative UIs.
5. Find the voltage between 57th UI to 62nd UI of positive cycle and negative cycle in V_{111} pattern.
6. Calculate the average voltage of the positive and negative cycle.
7. Find the voltage difference between positive and negative cycles.
8. Calculate the Package Loss Ratio = $20\log_{10}(V_{101}/V_{111})$.

5.20 Maximum Boost Ratio(V-Tx-Boost)

Definition:

V-Tx-Boost (P-P voltage swing after low frequency sequence) is defined in the Gen3/ Gen4 base specification. This measurement is done using the V-TX-BOOST. **The Result panel would display the voltage ratio.**

Test Definition Notes from the Specification:

V-Tx-Boost is defined when c_{-1} and c_{+1} are non-zero and measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern and with immediate single transition bit voltage.

Limits:

Refer to Table 3 for specified limits on the V-Tx-Boost measurement.

Test Procedure:

Ensure that V-Tx-Boost is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0 / PCI Express 4.0.

Set the following parameters:

Horizontal Record length to at least 500K.

Configure >> Clock Recovery >> PLL Custom BW >> Type I >>Loop BW >> 10MHz

Configure >> General >> off

Configure > Global > Gating >Off

Configure > Global > Qualify >Off

Configure > Global > Population >Off

Measurement Algorithm:

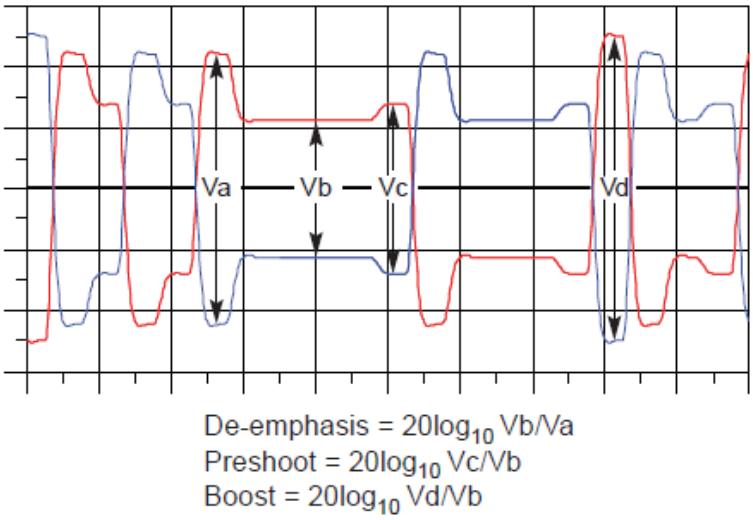


Figure 44: Maximum Boost Ratio definition.

1. Find 64 ones/64zeros bit pattern
2. Find the voltage between 57th UI to 62nd UI of positive cycle and negative cycle in V_{111} pattern.
3. Calculate the average voltage of the positive and negative cycle (V_{111}) in each 4680 pattern.
4. Add all averaged voltage for entire waveform.
5. Average again by number of repetitions of 4680 bit patterns in entire waveform, this is Vb
6. Find Single UI pulse after 64 ones/64 zeros.
7. Calculate the peak to peak voltage difference between positive and negative UI (V_{1UI}).
8. Average all V_{1UI} for entire waveform, this Vd
9. Calculate the VBoost = $20\log_{10}(V_d/V_b)$.

5.21 Pk-Pk RefClk Jitter for Common RefClk architecture, Gen1

Definition:

T-RefClk is defined in the Rev 3.0 CEM specification. This measurement is done using the acquired clock signal. The Result panel will display the Pk-Pk Jitter.

Test Definition Notes from the Specification:

Common Refclk Rx architectures are characterized by the Tx and Rx sharing the same Refclk source. The jitter seen by the Rx CDR is a function of the difference between the Tx and Rx PLL transfer functions, with a transport delay term (e^{-sT}), multiplied by the CDR's transfer function.

Limits:

Refer to Table 3 for specified limits on the T-RefClk measurement.

Test Procedure:

Ensure that T-REFCLK is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise

Measurement Algorithm:

The measurement algorithm for RefClk Common clocked architecture is implemented according to the following block diagram:

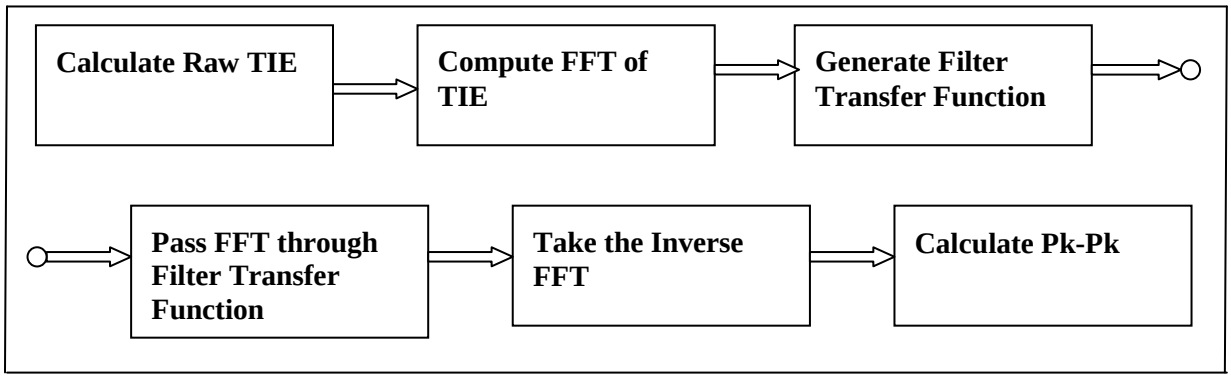


Figure 46: Measurement algorithm block diagram

The Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, in Figure 46, is computed according to the following equations, depicted in Figure 47:

$$H(s) = \left[H_1(s) - H_2(s) * e^{-s*t\_delay}\right] \cdot H_3(s)$$

where:

$$H_1(s) = \frac{2s\zeta\omega_1 + \omega_1^2}{s^2 + 2s\zeta\omega_1 + \omega_1^2},$$

$$H_2(s) = \frac{2s\zeta\omega_2 + \omega_2^2}{s^2 + 2s\zeta\omega_2 + \omega_2^2},$$

$$H_3(s) = \frac{s}{s + \omega_3},$$

$$\zeta = 0.54$$

$$\omega_1 = \frac{2 * \pi * 22 \cdot 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad / s$$

$$\omega_2 = \frac{2 * \pi * 1.5 \cdot 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad / s$$

$$\omega_3 = 2 * \pi * 1.5 \cdot 10^6 \; Rad / s$$

$$t\_delay = 10 \cdot 10^{-9} \; s$$

Figure 47: Filter transfer function for Gen1 Common Clock Architecture.

In the calculation of each of $H_1(s)$ and $H_2(s)$ the bandwidth, damping, and delay are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express\RefClock\RefClockConfig.txt files.

The plot below shows the different filter transfer function and the phase jitter relationship between filtered TIE and raw TIE.

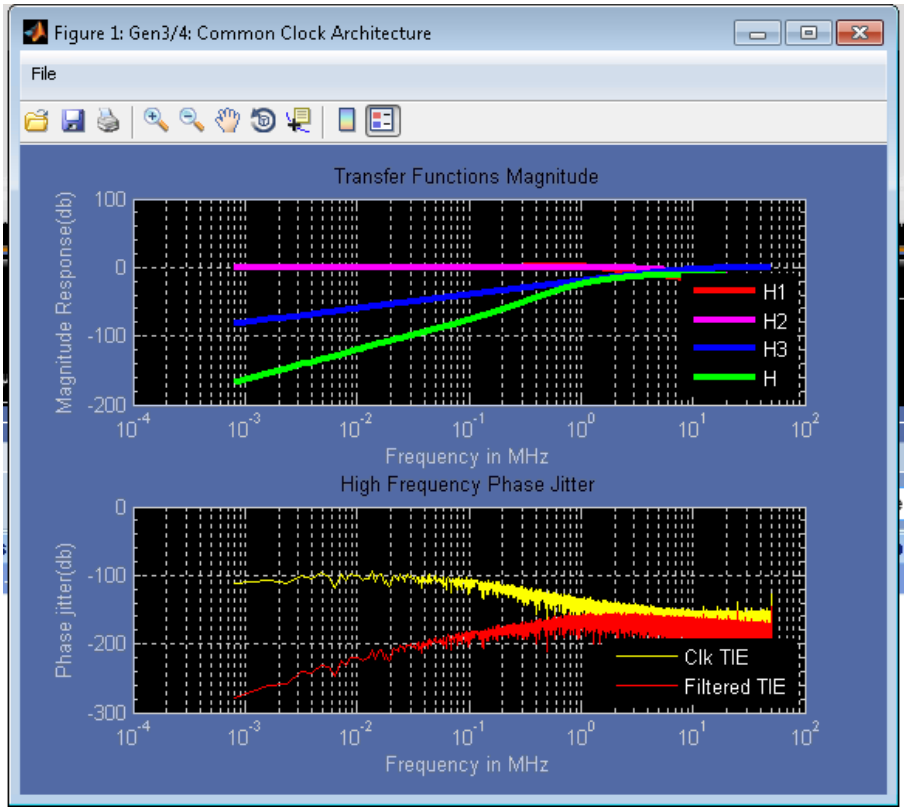


Figure 48: Raw TIE versus Filtered TIE

5.22 RMS RefClk HF Jitter for Common RefClk architecture, Gen2

Definition:

T-HF_RMSCC-RCLK is defined in the Gen3/ Gen4 base specification for 5GT/s. This measurement is done using the acquired clock signal. The Result panel will display the RMS Jitter.

Test Definition Notes from the Specification:

Common Refclk Rx architectures are characterized by the Tx and Rx sharing the same Refclk source. The jitter seen by the Rx CDR is a function of the difference between the Tx and Rx PLL transfer functions, with a transport delay term (e^{-sT}), multiplied by the CDR's transfer function. A 1.5MHz High Pass Filter is applied as well to remove low frequency jitter components.

Limits:

Refer to Table 3 for specified limits on the T-HF_RMSCC-RCLK measurement.

Test Procedure:

Ensure that T-HF_RMSCC-RCLK is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise

Edge Filtering:

Bandwidth is limited to 5GHz as follows:

Vertical>>VerticalSetup>>Chan Selection>>Bandwidth>>5 GHz

Measurement Algorithm:

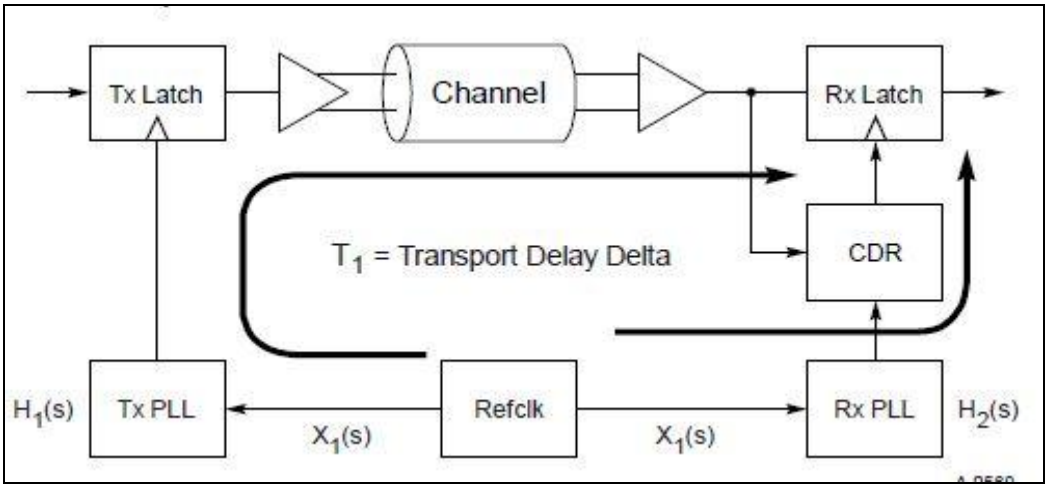


Figure 49: Common RefClk Architecture, 5GT/s

The measurement algorithm for RefClk Common clocked architecture is implemented according to the following block diagram:

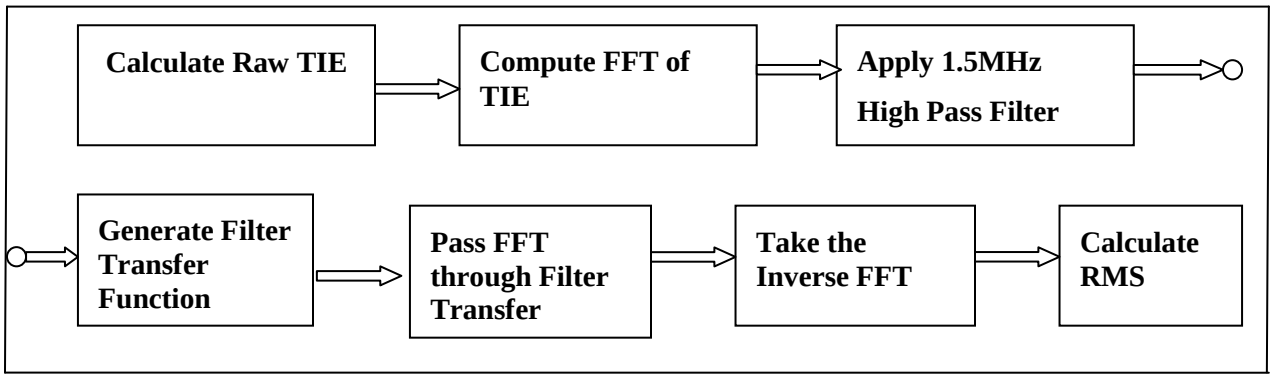


Figure 50: Measurement algorithm block diagram

The Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, is computed according to the following equations:

$$X_{CC}(s) = X_1(s) * H_{CC}(s)$$

$$H_{CC}(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} e^{-sT_1} - \frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \right]$$

Jitter contribution from H_1 Jitter contribution from H_2

Figure 51: Filter transfer function for Common Clock Architecture.

In the calculation of each of $H_1(s)$ and $H_2(s)$, the bandwidth, damping, and delay are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express\RefClock\ RefClockConfigGen2.txt files. The different combinations of bandwidth, delay and damping as described in the standards, is shown in Figure below:

Symbol	Parameter	Min	Max	Units
T_1	Data/clock transport delay delta		12	ns
ω_1	PLL #1 natural frequency	4.31*2π or 1.82*2π		Mrad/s
ζ_1	PLL #1 damping factor	0.54 or 1.16	1.75 (0.5 dB)	
ω_2	PLL #2 natural frequency		8.61*2π	Mrad/s
ζ_2	PLL #2 damping factor	0.54 or 1.16	1.75 (0.5 dB)	

Figure 52: Common Refclk bandwidth and damping for 5GT/s

The plot below shows the different filter transfer function and the phase jitter relationship between filtered TIE and raw TIE.

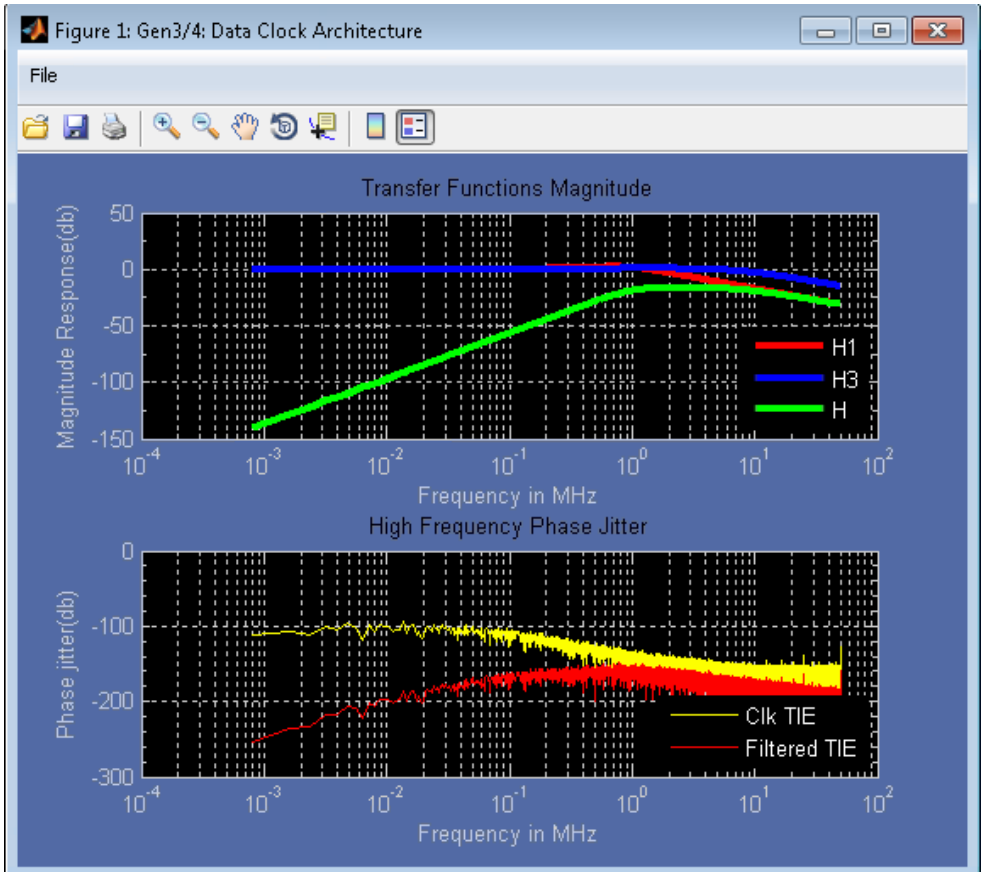


Figure 53: Raw TIE versus Filtered TIE

5.23 RMS RefClk LF Jitter for Common RefClk architecture, Gen2

Definition:

T-LF_RMSCC-RCLK is defined in the Gen3/ Gen4 base specification for 5GT/s. This measurement is done using the acquired clock signal. The Result panel will display the RMS Jitter.

Test Definition Notes from the Specification:

Common Refclk Rx architectures are characterized by the Tx and Rx sharing the same Refclk source. The jitter seen by the Rx CDR is a function of the difference between the Tx and Rx PLL transfer functions, with a transport delay term (e^{-sT}), multiplied by the CDR's transfer function. A 0.01-5MHz Band Pass Filter is applied as well, to remove high frequency jitter components.

Limits:

Refer to Table 3 for specified limits on the T-LF_RMSCC-RCLK measurement.

Test Procedure:

Ensure that T-LF_RMSCC-RCLK is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise

Edge Filtering:

Bandwidth is limited to 5GHz as follows:

Vertical>>VerticalSetup>>Chan Selection>>Bandwidth>>5 GHz

Measurement Algorithm:

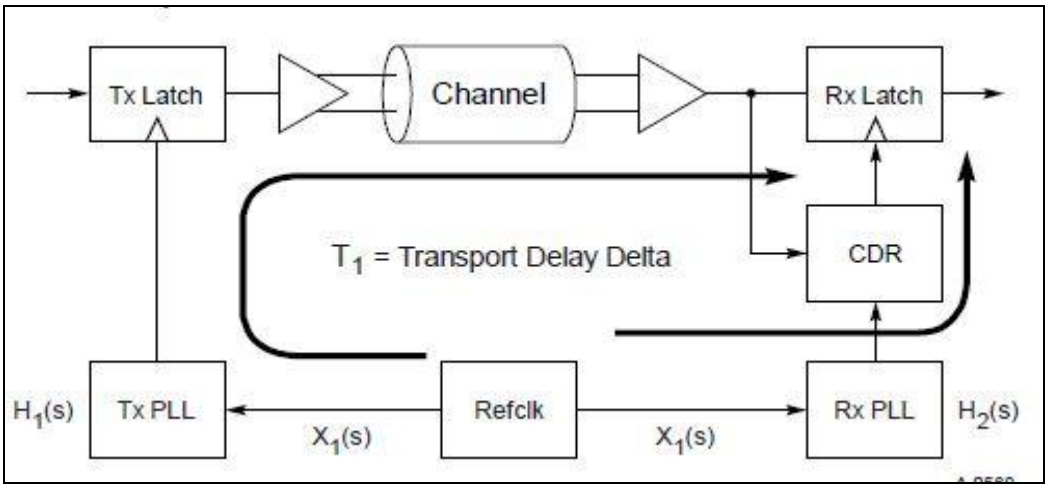


Figure 54: Common RefClk Architecture

The measurement algorithm for RefClk Common clocked architecture is implemented according to the following block diagram:

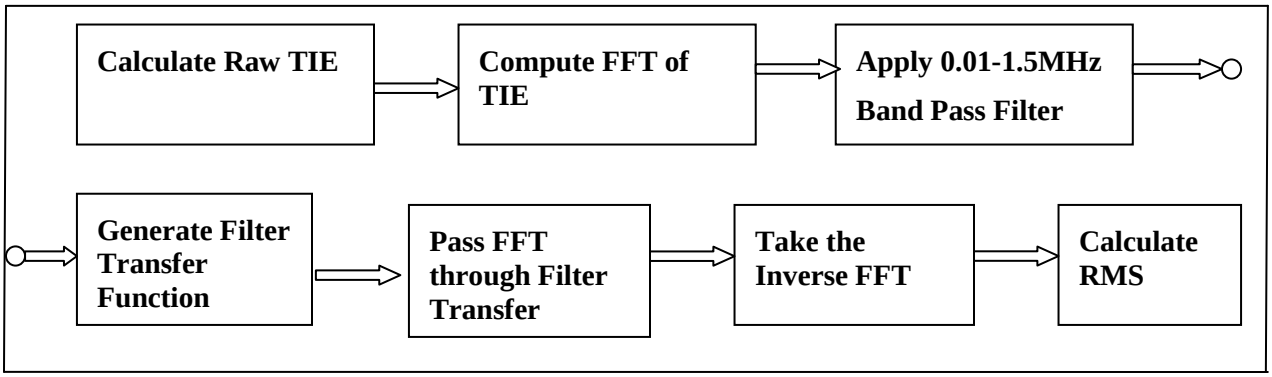


Figure 55: Measurement algorithm block diagram

The Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, is computed according to the following equations:

$$X_{CC}(s) = X_1(s) * H_{CC}(s)$$

$$H_{CC}(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} e^{-sT_1} - \frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \right]$$

Jitter contribution from H_1 Jitter contribution from H_2

Figure 56: Filter transfer function for Common Clock Architecture.

In the calculation of each of $H_1(s)$ and $H_2(s)$, the bandwidth, damping, and delay are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express\RefClock\ RefClockConfigGen2.txt files. The different combinations of bandwidth, delay and damping as described in the standards, is shown below:

Symbol	Parameter	Min	Max	Units
T_1	Data/clock transport delay delta		12	ns
ω_1	PLL #1 natural frequency	$4.31*2\pi$ or $1.82*2\pi$		Mrad/s
ζ_1	PLL #1 damping factor	0.54 or 1.16	1.75 (0.5 dB)	
ω_2	PLL #2 natural frequency		$8.61*2\pi$	Mrad/s
ζ_2	PLL #2 damping factor	0.54 or 1.16	1.75 (0.5 dB)	

Figure 57: Common Refclk bandwidth and damping for 5GT/s

The Raw TIE versus the Filtered TIE is also plotted as follows:

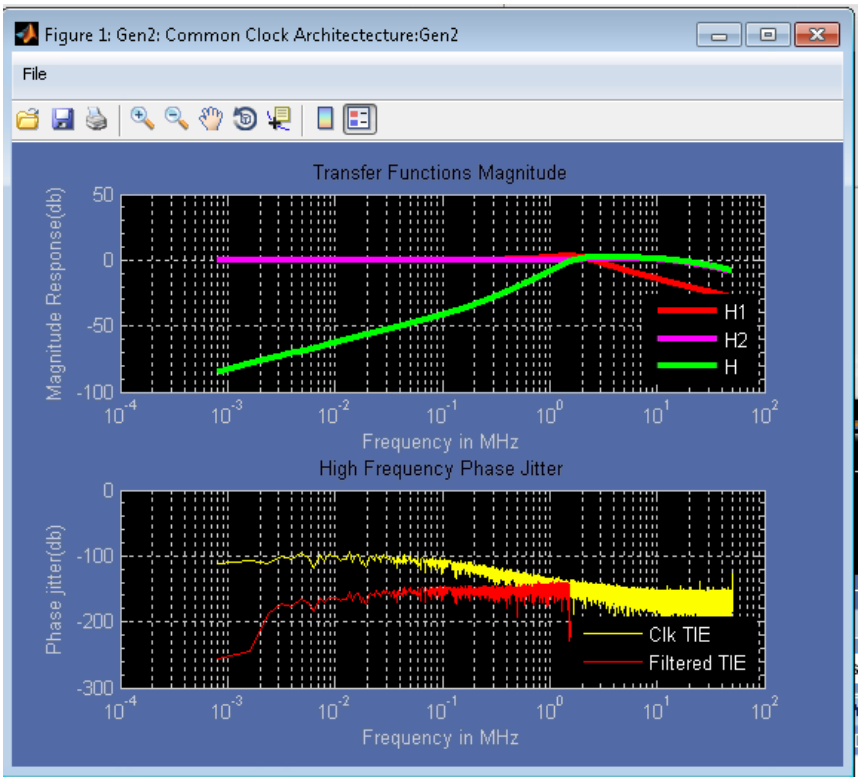


Figure 58: Raw TIE versus Filtered TIE

5.24 RMS RefClk HF Jitter for Data Clocked Rx RefClk architecture, Gen2

T-HF_RMSDC-RCLK is defined in the Gen3/ Gen4 base specification for 5GT/s. This measurement is done using the acquired clock signal. The Result panel will display the RMS Jitter.

Test Definition Notes from the Specification:

A data clocked Rx architecture is characterized by requiring the receiver's CDR to track the entirety of the low frequency jitter, including SSC. In the data clocked Rx architecture, for 5GT/s the amount of Refclk jitter propagated depends on the maximum PLL bandwidth of the Tx PLL. A 1.5MHz High Pass Filter is applied as well, to remove low frequency jitter components.

Limits:

Refer to Table 3 for specified limits on the T-HF_RMSDC-RCLK measurement.

Test Procedure:

Ensure that T-HF_RMSDC-RCLK is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise

Edge Filtering:

Bandwidth is limited to 5GHz as follows:

Vertical>>VerticalSetup>>Chan Selection>>Bandwidth>>5 GHz

Measurement Algorithm:

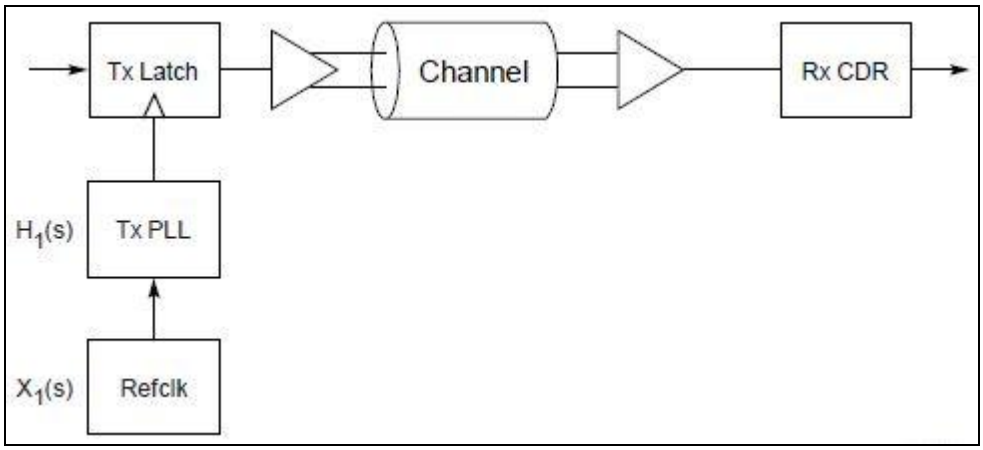


Figure 59: Data Clocked RefClk Architecture

The measurement algorithm for RefClk Data clocked architecture for 5GT/s is implemented according to the following block diagram:

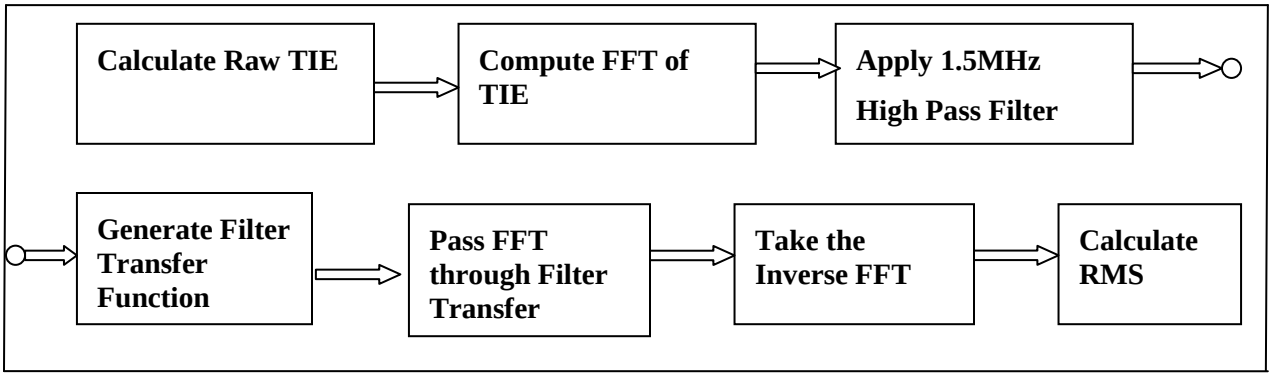


Figure 60: Measurement algorithm block diagram

The Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, in Figure 46, is computed according to the following equations:

$$X_{DC}(s) = X_1(s) * H_1(s)$$

$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} \right]$$

Figure 61: Filter transfer function for Common Clock Architecture.

In the calculation of each of H1(s), the bandwidth and damping are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express\RefClock\ RefClockConfigGen2.txt files. The different combinations of bandwidth, delay and damping as described in the standards, is shown below:

Symbol	Parameter	Min	Max	Units
ω_1	Tx PLL natural frequency		8.61*2π	Mrad/s
ζ_1	Tx PLL damping factor	0.54 (3.0 dB)	1.75 (0.5 dB)	

Figure 62: Data Clocked Refclk bandwidth and damping for 5GT/s

The Raw TIE versus the Filtered TIE are also plotted as follows:

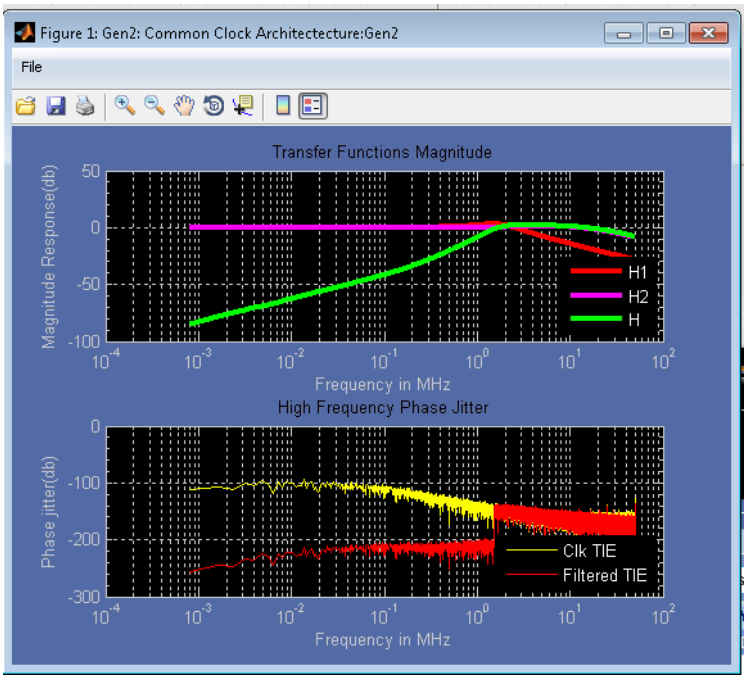


Figure 63: Raw TIE versus Filtered TIE

5.25 RMS RefClk LF Jitter for Data Clocked Rx RefClk architecture, Gen2

T-LF_RMSDC-RCLK is defined in the Gen3/ Gen4 base specification for 5GT/s. This measurement is done using the acquired clock signal. The Result panel will display the RMS Jitter.

Test Definition Notes from the Specification:

A data clocked Rx architecture is characterized by requiring the receiver's CDR to track the entirety of the low frequency jitter, including SSC. In the data clocked Rx architecture, for 5GT/s the amount of Refclk jitter propagated depends on the maximum PLL bandwidth of the Tx PLL. A 0.01-5MHz Band Pass Filter is applied as well, to remove high frequency jitter components.

Limits:

Refer to Table 3 for specified limits on the T-LF_RMSDC-RCLK measurement.

Test Procedure:

Ensure that T-LF_RMSDC-RCLK is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise

Edge Filtering:

Bandwidth is limited to 5GHz as follows:

Vertical>>VerticalSetup>>Chan Selection>>Bandwidth>>5 GHz

Measurement Algorithm:

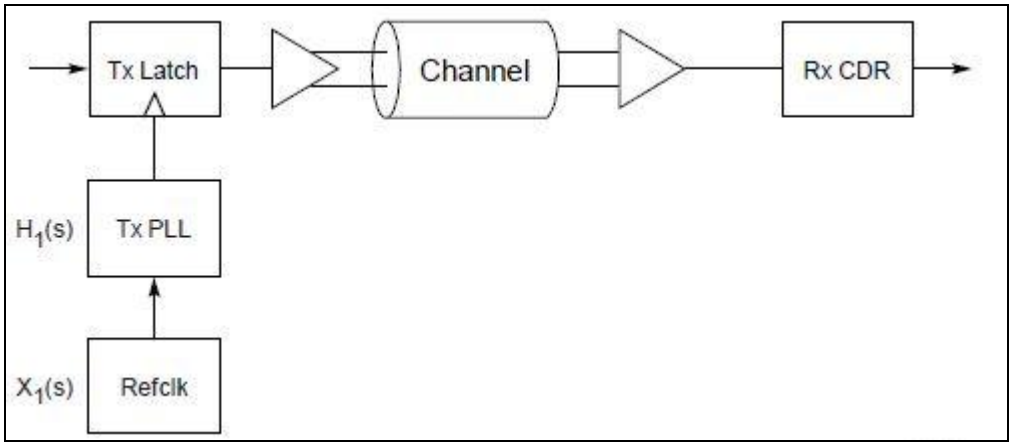


Figure 64: Data Clocked RefClk Architecture

The measurement algorithm for RefClk Data clocked architecture for 5GT/s is implemented according to the following block diagram:

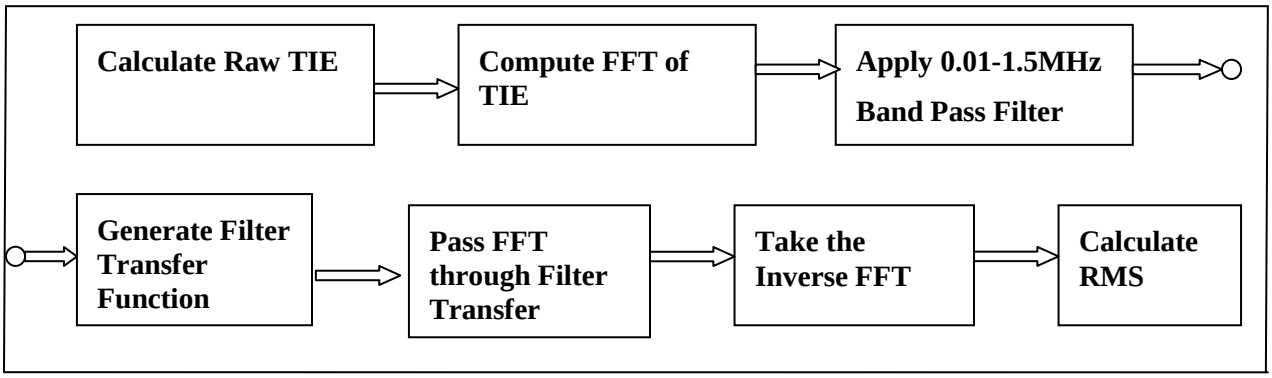


Figure 65: Measurement algorithm block diagram

The Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, is computed according to the following equations:

$$X_{DC}(s) = X_1(s) * H_1(s)$$

$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} \right]$$

Figure 66: Filter transfer function for Common Clock Architecture.

In the calculation of each of $H_1(s)$, the bandwidth and damping are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express\RefClock\ RefClockConfigGen2.txt files. The different combinations of bandwidth, delay and damping as described in the standards, is shown below:

Symbol	Parameter	Min	Max	Units
ω_1	Tx PLL natural frequency		8.61*2π	Mrad/s
ζ_1	Tx PLL damping factor	0.54 (3.0 dB)	1.75 (0.5 dB)	

Figure 67: Data Clocked Refclk bandwidth and damping for 5GT/s

The Raw TIE versus the Filtered TIE are also plotted as follows:

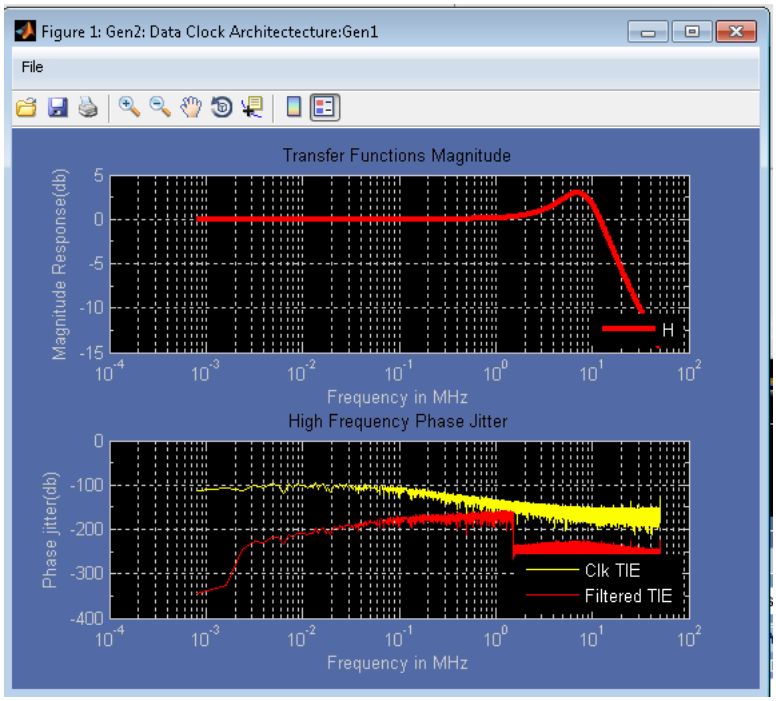


Figure 68: Raw TIE versus Filtered TIE

5.26 RMS RefClk Jitter for Common RefClk architecture, Gen3

Definition:

T-RefClk-RMSCC is defined in the Gen3/ Gen4 base specification. This measurement is done using the acquired clock signal. The Result panel will display the RMS Jitter.

Test Definition Notes from the Specification:

Common Refclk Rx architectures are characterized by the Tx and Rx sharing the same Refclk source. The jitter seen by the Rx CDR is a function of the difference between the Tx and Rx PLL transfer functions, with a transport delay term (e^{-sT}), multiplied by the CDR's transfer function.

Limits:

Refer to Table 3 for specified limits on the T-RefClk-RMSCC measurement.

Test Procedure:

Ensure that T-REFCLK-RMSCC is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise or Fall

Measurement Algorithm:

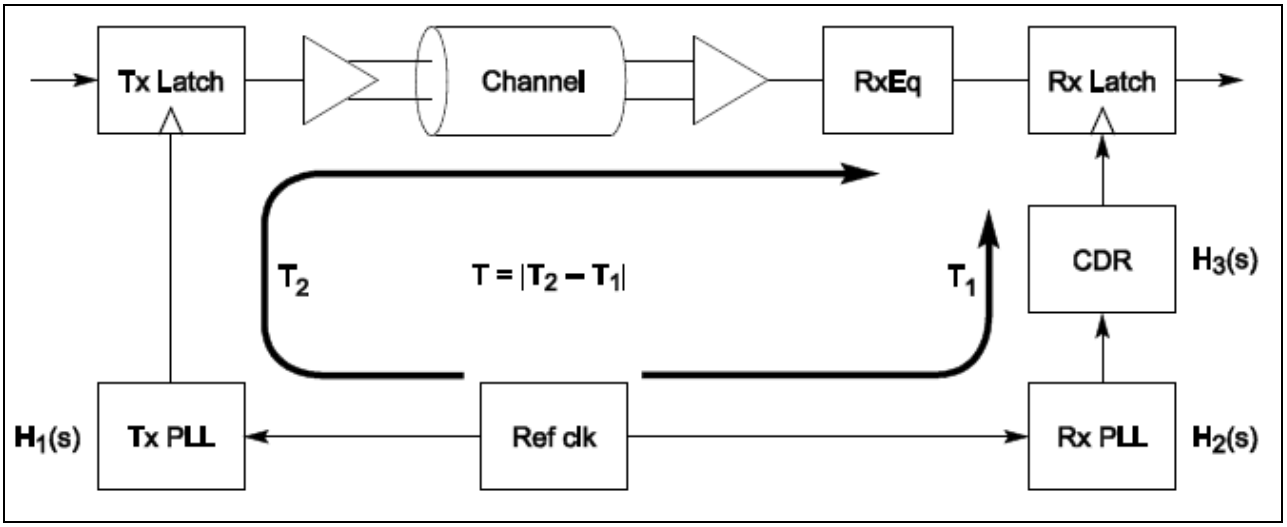


Figure 69: Common RefClk Architecture

The measurement algorithm for RefClk Common clocked architecture is implemented according to the following block diagram:

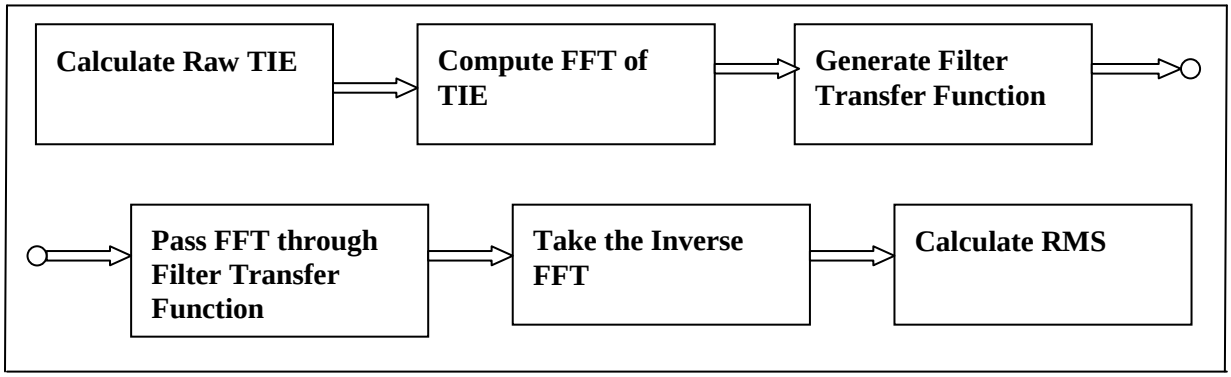


Figure 70: Measurement algorithm block diagram

The Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, is computed according to the following equations, below:

$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2}\right] \quad H_2(s) = \left[\frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2}\right] \quad H_3(s) = \frac{s}{s + \omega_3}$$

$$\left.\begin{aligned} H(s) &= [H_1(s)e^{-sT} - H_2(s)]H_3(s) \text{ or} \\ H'(s) &= [H_2(s)e^{-sT} - H_1(s)]H_3(s) \end{aligned}\right\} \text{Need to compute both}$$

Figure 71: Filter transfer function for Common Clock Architecture.

In the calculation of each of H(s) and H' (s), the bandwidth, damping, peaking and delay are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express 3.0\RefClock\RefClockConfig.txt files. The different combinations of bandwidth and peaking as described in the standards, is shown below:

	0.01 dB Peaking	2.0 dB Peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1} = 0.448 Mrad/s ζ_1 = 14	ω_{n1} = 6.02 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 4.0 MHz	ω_{n1} = 0.896 Mrad/s ζ_1 = 14	ω_{n1} = 12.04 Mrad/s ζ_1 = 0.73

	0.01 dB Peaking	1.0 dB Peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n2} = 0.448 Mrad/s ζ_2 = 14	ω_{n2} = 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 5.0 MHz	ω_{n2} = 1.12 Mrad/s ζ_2 = 14	ω_{n2} = 11.53 Mrad/s ζ_2 = 1.15

A-0842

Figure 72: Common Refclk Rx Architecture with ω_n, ζ Limits

5.27 RMS RefClk Worst Case Jitter for Common RefClk architecture, Gen3

Definition:

T-RefClk-WST-RMSCC is done using the acquired clock signal. The Result panel will display the Worst case RMS Jitter.

Test Definition Notes from the Specification:

Common Refclk Rx architectures are characterized by the Tx and Rx sharing the same Refclk source. The jitter seen by the Rx CDR is a function of the difference between the Tx and Rx PLL transfer functions, with a transport delay term (e^{-sT}), multiplied by the CDR's transfer function.

Limits:

Refer to Table 3 for specified limits, which is the same as for the T-RefClk-RMSCC measurement.

Test Procedure:

Ensure that T-REFCLK- WST-RMSCC is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise or Fall

Measurement Algorithm:

Refer to section 'Pk-Pk RefClk Jitter for Common RefClk architecture, **Gen1**

Definition:

T-RefClk is defined in the Rev 3.0 CEM specification. This measurement is done using the acquired clock signal. The Result panel will display the Pk-Pk Jitter.

Test Definition Notes from the Specification:

Common Refclk Rx architectures are characterized by the Tx and Rx sharing the same Refclk source. The jitter seen by the Rx CDR is a function of the difference between the Tx and Rx PLL transfer functions, with a transport delay term (e-sT), multiplied by the CDR's transfer function.

Limits:

Refer to Table 3 for specified limits on the T-RefClk measurement.

Test Procedure:

Ensure that T-REFCLK is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise

Measurement Algorithm:

The measurement algorithm for RefClk Common clocked architecture is implemented according to the following block diagram:

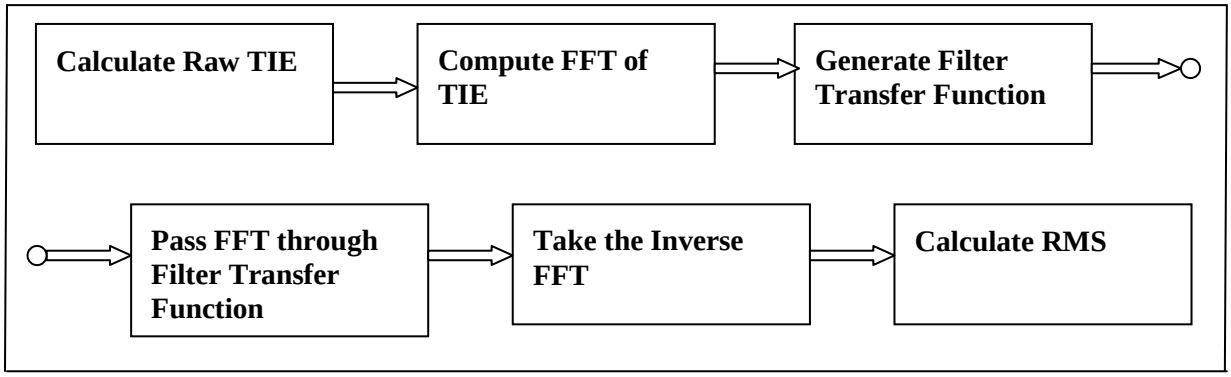


Figure 46: Measurement algorithm block diagram

The Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, in Figure 46, is computed according to the following equations, depicted in Figure 47:

$$H(s) = \left[H_1(s) - H_2(s) * e^{-s*t\_delay}\right] \cdot H_3(s)$$

where:

$$H_1(s) = \frac{2s\zeta\omega_1 + \omega_1^2}{s^2 + 2s\zeta\omega_1 + \omega_1^2},$$

$$H_2(s) = \frac{2s\zeta\omega_2 + \omega_2^2}{s^2 + 2s\zeta\omega_2 + \omega_2^2},$$

$$H_3(s) = \frac{s}{s + \omega_3},$$

$$\zeta = 0.54$$

$$\omega_1 = \frac{2 * \pi * 22 \cdot 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad/s$$

$$\omega_2 = \frac{2 * \pi * 1.5 \cdot 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad/s$$

$$\omega_3 = 2 * \pi * 1.5 \cdot 10^6 \; Rad/s$$

$$t\_delay = 10 \cdot 10^{-9} \; s$$

Figure 47: Filter transfer function for Gen1 Common Clock Architecture.

In the calculation of each of H1(s) and H2(s) the bandwidth, damping, and delay are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express\RefClock\RefClockConfig.txt files.

The plot below shows the different filter transfer function and the phase jitter relationship between filtered TIE and raw TIE.

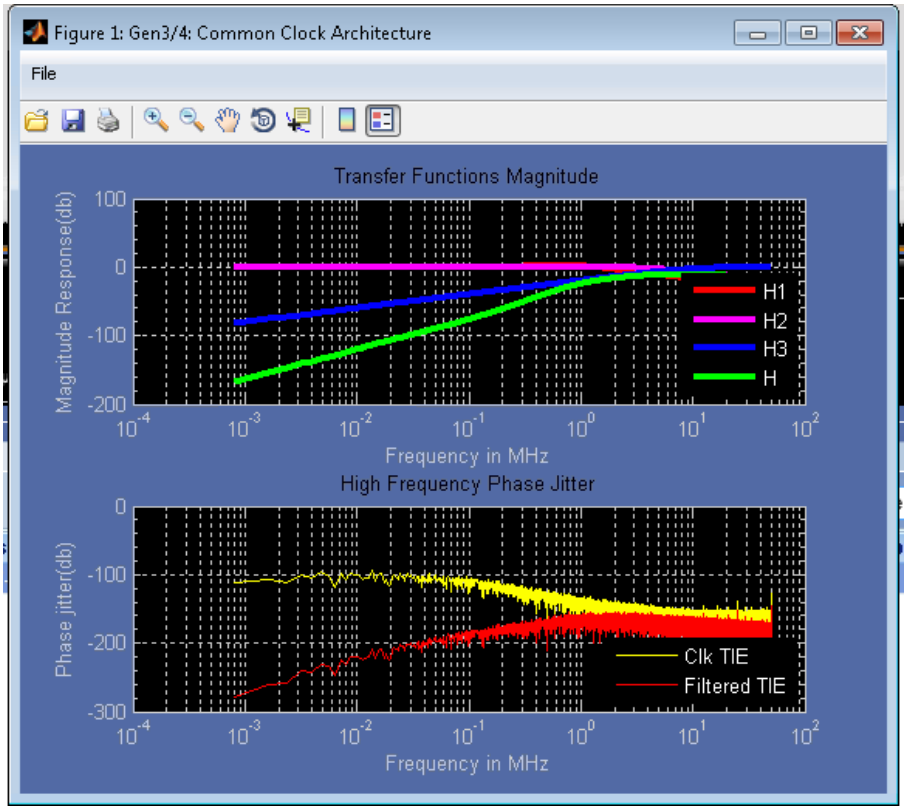


Figure 48: Raw TIE versus Filtered TIE

5.28 RMS RefClk Jitter for Data Clocked Rx architecture, Gen3

Definition:

T-RefClk-RMSDC is defined in the Gen3/ Gen4 base specification. This measurement is done using the acquired clock signal. The Result panel will display the RMS Jitter.

Test Definition Notes from the Specification:

A data clocked Rx architecture is characterized by requiring the receiver's CDR to track the entirety of the low frequency jitter, including SSC. Since the Tx and Rx do not share a common Refclk, the jitter transfer function includes only the Tx PLL transfer function plus the lowpass characteristics of the CDR.

Limits:

Refer to Table 3 for specified limits on the T-RefClk-RMSDC measurement.

Test Procedure:

Ensure that T-REFCLK-RMSDC is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise or Fall

Measurement Algorithm:

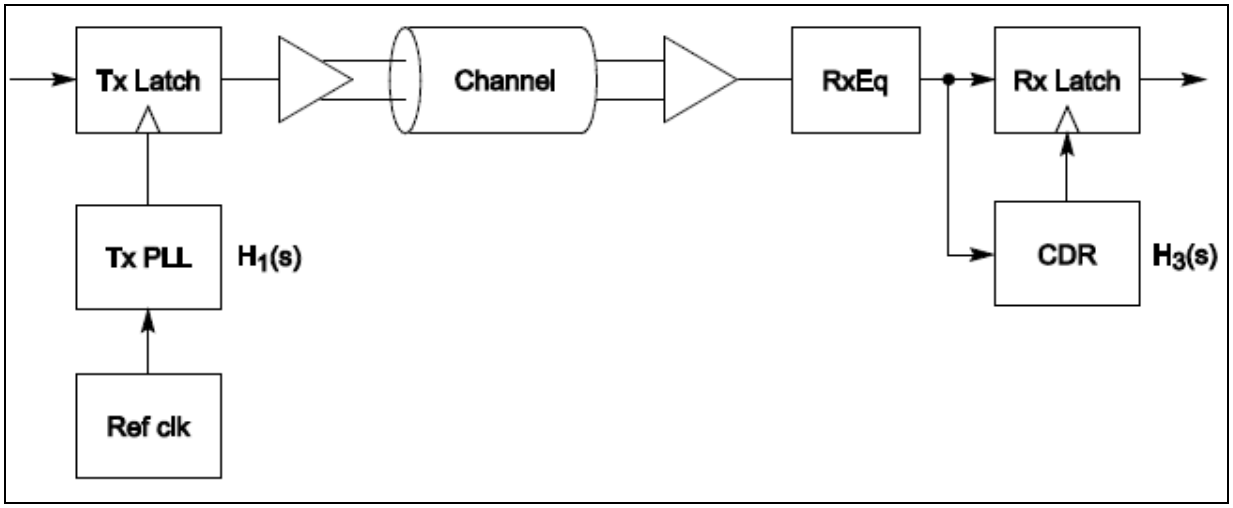


Figure 74: Data Clocked Rx Architecture

The measurement algorithm for RefClk Data clocked architecture is implemented according to the block diagram described in Figure 70. Measurement algorithm block diagram. However, the Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, is computed according to the following equations, depicted below:

$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2}\right] \qquad H_3(s) = \left[\frac{2s\zeta_3\omega_{n3} + \omega_{n3}^2}{s^2 + 2s\zeta_3\omega_{n3} + \omega_{n3}^2}\right]$$

$$H(s) = H_1(s)[1 - H_3(s)]$$

Figure 75: Filter transfer function for Data Clocked Architecture.

In the calculation of H(s), the bandwidth, damping, peaking and delay are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express 3.0\RefClock\RefClockConfig.txt files. The different combinations of bandwidth and peaking as described in the standards, is below:

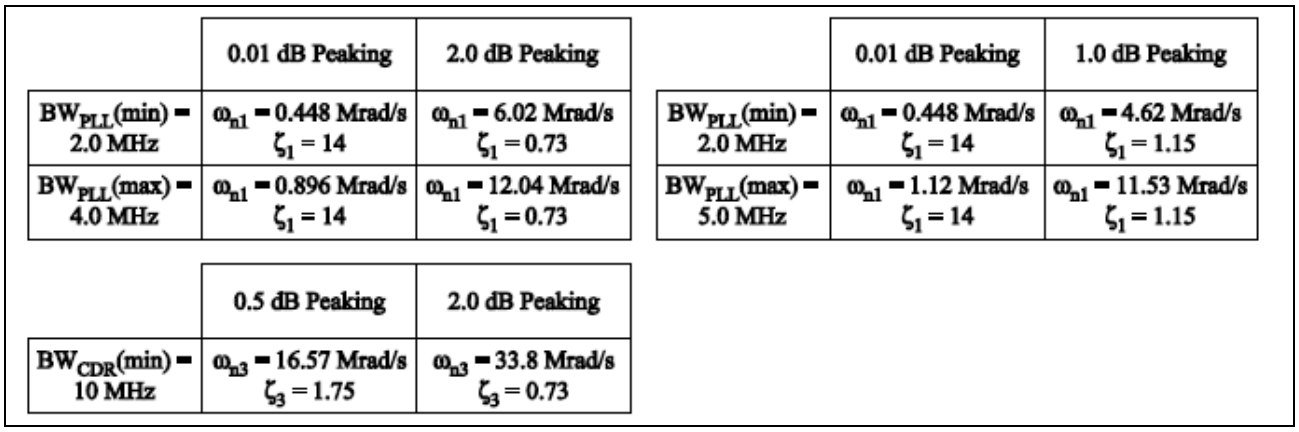


Figure 76: Data Clocked Rx Architecture with ω_n, ζ Limits

The Raw TIE versus the Filtered TIE are also plotted as described in **Figure 73.**

5.29 RMS RefClk Worst Case Jitter for Data Clocked Rx architecture, Gen3

Definition:

T-RefClk-WST-RMSDC is done using the acquired clock signal. The Result panel will display the Worst case RMS Jitter.

Test Definition Notes from the Specification:

A data clocked Rx architecture is characterized by requiring the receiver's CDR to track the entirety of the low frequency jitter, including SSC. Since the Tx and Rx do not share a common Refclk, the jitter transfer function includes only the Tx PLL transfer function plus the lowpass characteristics of the CDR.

Limits:

Refer to Table 3 for specified limits, which is the same as for the T-RefClk-RMSDC measurement.

Test Procedure:

Ensure that T-REFCLK- WST -RMSDC is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0.

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise or Fall

Measurement Algorithm:

Refer to section 'RMS RefClk Jitter for Data Clocked Rx architecture, Gen3' for details of the measurement algorithm. In the calculation of each of H(s), the bandwidth, damping, peaking and delay are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express 3.0\RefClock\RefClockBulkConfigDC.txt files. The Worst case jitter is calculated from different sets of

values of bandwidth, damping, peaking and delay. The Raw TIE versus the Filtered TIE are also plotted as described in Figure 73.

5.30 RMS RefClk Jitter for Separate RefClk with Independent SSC Gen3/4

Definition:

Separate Ref Clock with Independent SSC (SRIS) is defined in the Gen3/ Gen4 base specification. This measurement is done using the acquired clock signal for both Tx and Rx. The Result panel will display the RMS Jitter.

Test Definition Notes from the Specification:

This architecture employs two independent clock sources. The Receiver must be able to track and reject the phase drift due to the two independent SSC clocks. The CDR needs to have a second order high-pass behavior to reject the extra phase drift due to independent SSC.

Limits:

Refer to Table 3 for specified limits on the T-RefClk-RMS-SRIS measurement.

Test Procedure:

Ensure that either Gen3_SRIS is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0

Or

PCIE4_SRIS is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 4.0

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise or Fall

Measurement Algorithm:

The below figure shows the architecture for SRIS

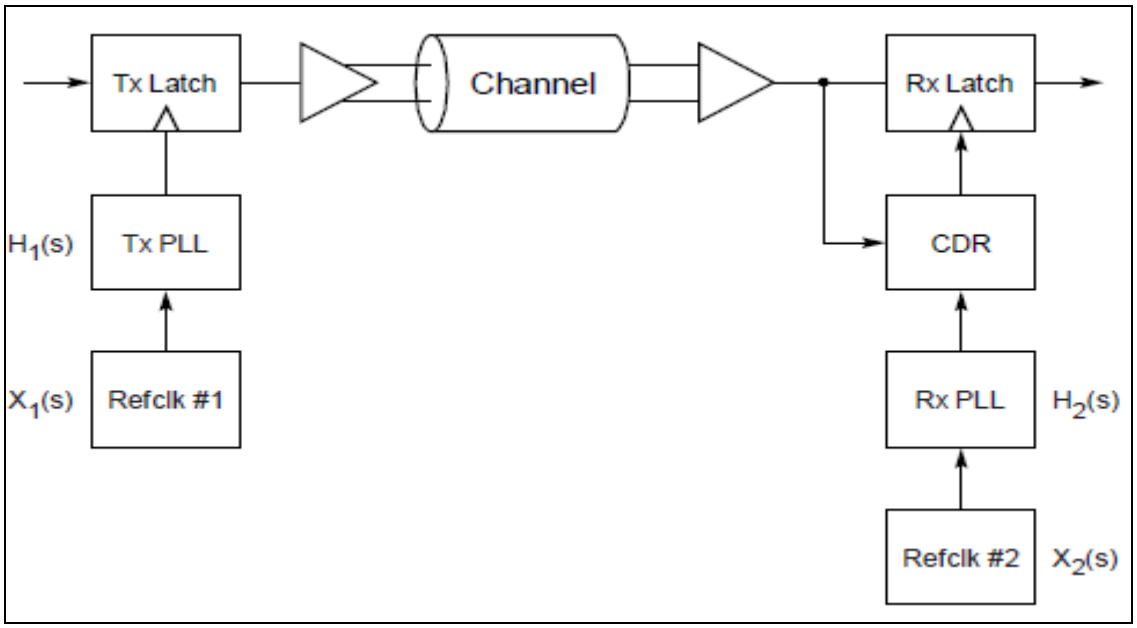


Figure 77: Separate RefClk with Independent SSC Architecture

As can be seen from the architecture we have two different Ref Clock here. Since Refclk #1 and Refclk #2 are independent from each other, their respective jitter at the Rx Latch are simply $X_1(s)*H_1(s)*H\_CDR(s)$ and $X_2(s)*H_2(s)*H\_CDR(s)$; where H_CDR(s) is the CDR's jitter transfer function. However, since Refclk jitter is primarily Rj, their combined impact should be the Root Sum Square (RSS) of the individual terms.

$$H_1(s)=\left[\frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2}\right] \quad H_2(s)=\left[\frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2}\right]$$

$$X_{SC}(s)=\sqrt{\left[X_1(s)*H_1(s)\right]^2+\left[X_2(s)*H_2(s)\right]^2}$$

The measurement algorithm for Separate RefClk with independent SSC architecture is implemented according to the block diagram described below.

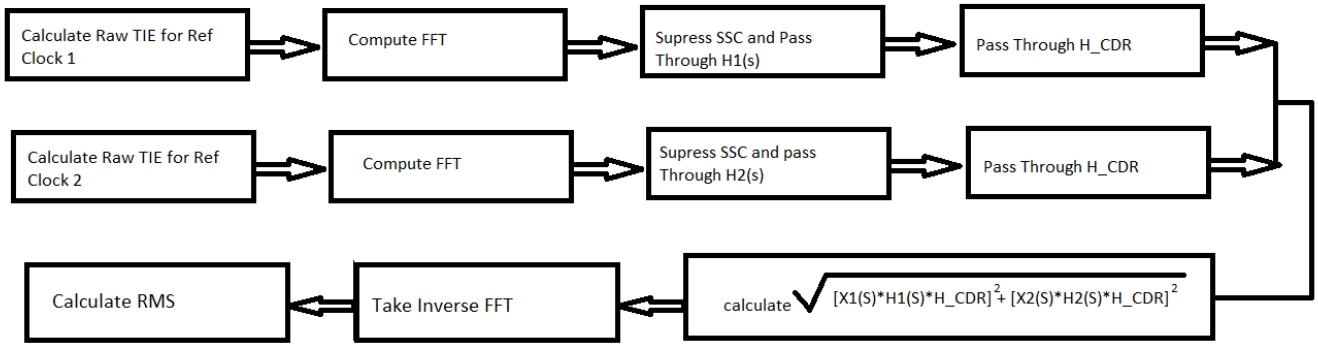


Figure 78: Measurement algorithm block diagram

The Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, is computed according to the following equations, depicted below:

$$H(s) = \frac{s^2}{s^2+sA+B} \cdot \frac{s^2+2\zeta_2\omega_0 s+\omega_0^2}{s^2+2\zeta_1\omega_0 s+\omega_0^2}$$

where

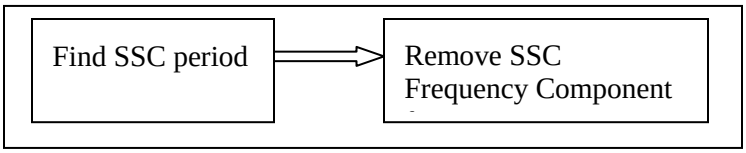
$$\zeta_1 = \frac{1}{\sqrt{2}}; \zeta_2 = 1;\ \omega_0 = 10^7 \times 2\pi$$

$$A = 10^7 \times 2\pi; B = 2.2 \times 10^{12} \times (2\pi)$$

Figure 79: Filter transfer function for Separate RefClk with Independent SSC Architecture.

In the calculation of H(s), the bandwidth and damping are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express 3.0\RefClock\RefClockConfig.txt files.

The SSC Suppression block is described below:



5.31 RMS RefClk Jitter for Separate RefClk with no SSC Gen3/4

Definition:

Separate Ref Clock with No SSC (SRNS) is defined in the Gen3/ Gen4 base specification. This measurement is done using the acquired clock signal for both Tx and Rx. The Result panel will display the RMS Jitter.

Test Definition Notes from the Specification:

This architecture employs two independent clock sources. The Receiver must be able to track and reject the phase drift due to the two independent SSC clocks. The CDR needs to have a second order high-pass behavior to reject the extra phase drift due to independent SSC.

Limits:

Refer to Table 3 for specified limits, which is the same as for the T-RefClk-RMS-SRNS measurement.

Test Procedure:

Ensure that either Gen3_SRNS is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 3.0

Or

PCIE4_SRNS is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express 4.0

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise or Fall

Measurement Algorithm:

The measurement algorithm is exactly same as SRIS in section 5.30. The only difference is that since there is no SSC we do not need to suppress SSC.

5.32 RMS RefClk Jitter for Separate RefClk with Independent SSC Gen2

Definition:

Separate Ref Clock with Independent SSC (SRIS) is defined in the Gen2 base specification. This measurement is done using the acquired clock signal for both Tx and Rx. The Result panel will display the RMS Jitter.

Test Definition Notes from the Specification:

This architecture employs two independent clock sources. The Receiver must be able to track and reject the phase drift due to the two independent SSC clocks. The CDR needs to have a second order high-pass behavior to reject the extra phase drift due to independent SSC.

Limits:

Refer to Table 3 for specified limits on the T-RefClk-RMS-SRIS measurement.

Test Procedure:

Ensure that either SRIS is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise or Fall

Measurement Algorithm:

The below figure shows the architecture for SRIS

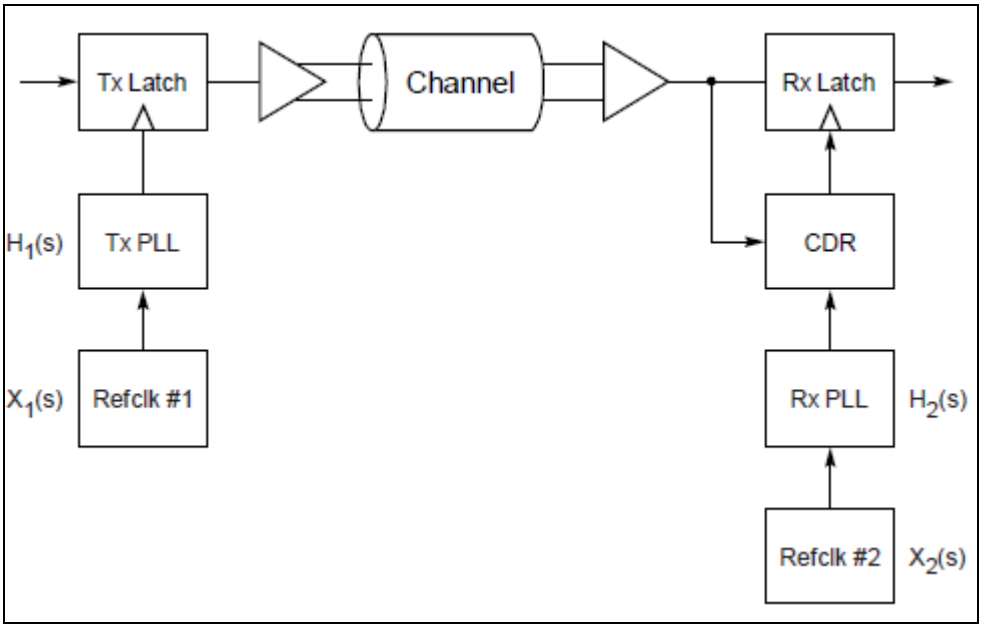


Figure 77: Separate RefClk with Independent SSC Architecture

As can be seen from the architecture we have two different Ref Clock here. Since Refclk #1 and Refclk #2 are independent from each other, their respective jitter at the Rx Latch are simply $X_1(s)*H_1(s)*H\_CDR(s)$ and $X_2(s)*H_2(s)*H\_CDR(s)$; where H_CDR(s) is the CDR's jitter transfer function. However, since Refclk jitter is primarily Rj, their combined impact should be the Root Sum Square (RSS) of the individual terms.

$$H_1(s)=\left[\frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2}\right] \quad H_2(s)=\left[\frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2}\right]$$

$$X_{SC}(s)=\sqrt{\left[X_1(s)*H_1(s)\right]^2+\left[X_2(s)*H_2(s)\right]^2}$$

The measurement algorithm for Separate RefClk with independent SSC architecture is implemented according to the block diagram described below.

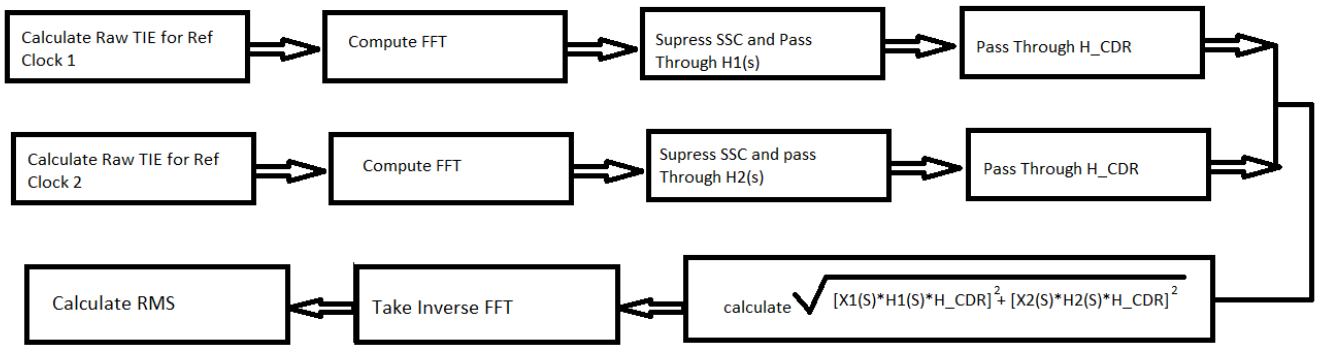


Figure 78: Measurement algorithm block diagram

The Filter transfer function depicted in the block 'Generate Filter Transfer Function' described above, is computed according to the following equations, depicted below:

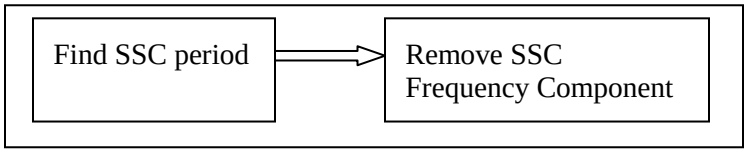
$$H_{JTF}(s) = \frac{s^2}{s^2+2\zeta\omega_m s+\omega_m{}^2}$$

$$\text{where } f_m = \frac{2*5.0\ \text{MHz}}{\sqrt{1+2\zeta^2+\sqrt{1+(1+2\zeta^2)^2}}}\ \zeta = .707 \text{ and } \omega_m = 2\pi f_m.$$

Figure 79: Filter transfer function for Separate RefClk with Independent SSC Architecture.

In the calculation of H(s), the bandwidth and damping are taken from the C:\Users\Public\Tektronix\TekApplications\PCI Express 3.0\RefClock\RefClockConfig.txt files.

The SSC Suppression block is described below:



5.33 RMS RefClk Jitter for Separate RefClk with no SSC Gen2

Definition:

Separate Ref Clock with No SSC (SRNS) is defined in the Gen3/ Gen4 base specification. This measurement is done using the acquired clock signal for both Tx and Rx. **The Result panel will display the RMS Jitter.**

Test Definition Notes from the Specification:

This architecture employs two independent clock sources. The Receiver must be able to track and reject the phase drift due to the two independent SSC clocks. The CDR needs to have a second order high-pass behavior to reject the extra phase drift due to independent SSC.

Limits:

Refer to Table 3 for specified limits, which is the same as for the T-RefClk-RMS-SRNS measurement.

Test Procedure:

Ensure that SRNS is selected in the Jitter and Eye diagram Analysis Tools >> Select Standard Tab >> PCI Express

Set the following parameters:

Configure >> Clock Recovery>> Constant Clock-Mean

Configure>> Edges>>Signal Type>>Clock

Configure>>Clock Edge>>Rise or Fall

Measurement Algorithm:

The measurement algorithm is exactly same as SRIS in section 5.32. The only difference is that since there is no SSC we do not need to suppress SSC.

6 Appendix A

Add-In Card Eye Diagrams

PCI Express Gen 3 testing using SDLA version 1.2. Available on 32-bit Windows XP and Windows 7 scopes. The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 4.

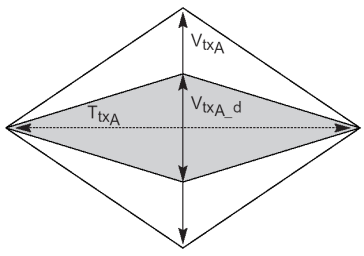


Figure A1: Add-in card compliance eye masks

Load the Add-In Card Setup File in DPOJET:

1. In the scope menu, select Analyze->PCI Express
2. In the DPOJET standard tab, click the select button to choose the Test Point
3. Select Rev3.0->SDLA_Add-In-Card->R30_SDLA_Add-in-Card.set
4. +
5. +In the Math Menu, set Math1 to Channel 1-Channel 2(Data)

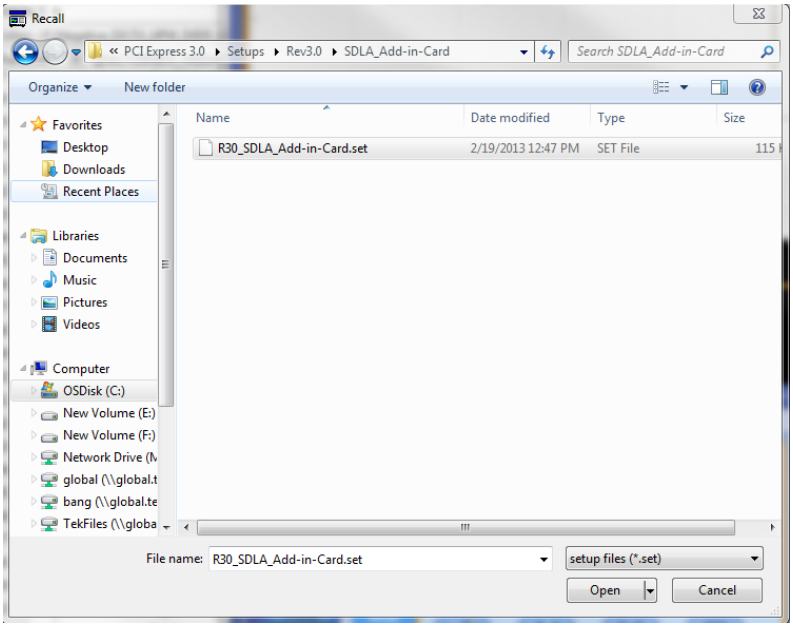


Figure A2: Setup File Selection

Applying Channel and Behavioral Equalizer from SDLA:

These measurements are done using SDLA (Serial Data Link Analysis) behavioral equalizer and channel embedding. Open SDLA from Analyze menu. Select 'Equalizer' and set the CTLE and DFE values as per the PCI Express 3.0 specification. For details of the PCI Express Gen 3 De-embedding procedure refer to the following document in http://www.tek.com/method-implementation/pci-express-30-de-embedding-method-implementation-version-10

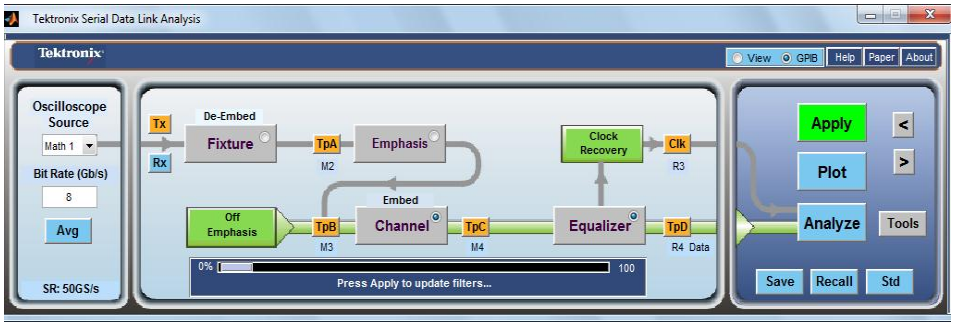


Figure A3: Serial Data Link Analysis window

6. Embed the Compliance Channel
    a. Select the Channel Block on the main SDLA window
    b. +Under Data Input Type Select S-Parameter and click browse. Select AicTx_Test_Embed01_SigTest_Mixed.s4p

       (File is available on *C:\Users\Public\Tektronix\TekApplications\SDLA\input S parameters*)
    c. Select 4-port as the Touchstone format
    d. In the S-Parameter Specification section, select Differential as the Derive Filter From Selection
    e. Under Bandwidth Limit Click Apply
    f. Select Ok
7. Apply the PCI Express Reference Equalizer
    a. Select the Equalizer Block on the main SDLA window
    b. Select the CTLE and PcieC checkboxes
    c. Select the FFE/DFE and PcieD checkboxes
    d. Select Ok (Note: Run EQ can be selected if the channel model has already been applied. Otherwise the waveform needs to be processed by using the Apply button in the main SDLA window)
8. Process waveform
    a. Select the TpB button on the main SDLA window. This will ensure that Math3 is not overwritten as the Clock is assigned to Math3
    b. Select Math 1 as the input to SDLA
    c. Select 8Gb/s as the data rate
    d. Select Apply on the main SDLA window
    e. SDLA will automatically apply the channel model and determine the optimal CTLE and DFE settings. This process must be re-run anytime a new acquisition is needed.

+

Figure A4: SDLA Equalizer Setup Menu

After SDLA is done processing, go to DPOJET and hit "Clear" and "ReCalc" to run the measurements. The results will be displayed as below:

++

Figure A5: DPOJET Measurement Results

System Board Eye DiagramsP

+CI Express Gen 3 testing using SDLA version 1.2. Available on 32-bit Windows XP and Windows 7 scopes. The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 5.

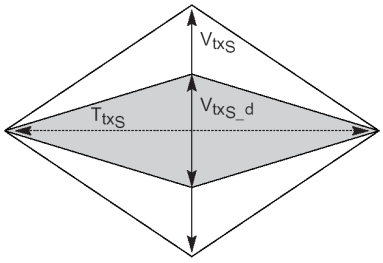


Figure A6: System Board Compliance Eye Masks

Load the System Setup File in DPOJET:

1. In the scope menu, select Analyze->PCI Express
2. In the DPOJET standard tab, click the select button to choose the Test Point
3. Select Rev3.0->SDLA_System->R30_SDLA_SYSTEM.set
4. Go to Horiz/Acq menu and change Record Length to 4M.
5. In the Math Menu, set Math1 to Channel 3-Channel4(Data) and Math2 to Channel 1-Channel2(Clock)

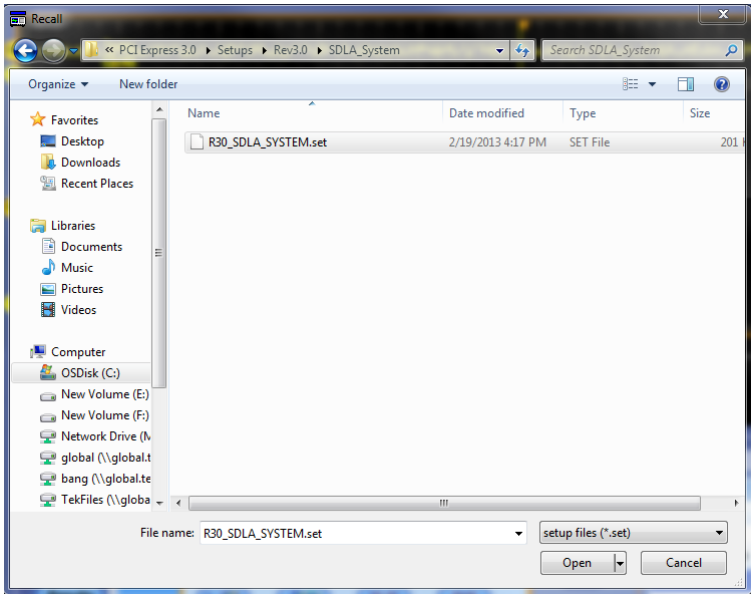


Figure A7: Setup File Selection

Applying Channel and Behavioral Equalizer from SDLA:

These measurements are done using SDLA (Serial Data Link Analysis) behavioral equalizer and channel eme+dding. Open SDLA from Analyze menu. Select ‘Equalizer’ and set the CTLE and DFE values as per the

PCI Express 3.0 specification. For details of the PCI Express Gen 3 De-embedding procedure refer to the following document in http://www.tek.com/method-implementation/pci-express-30-de-embedding-method-implementation-version-10

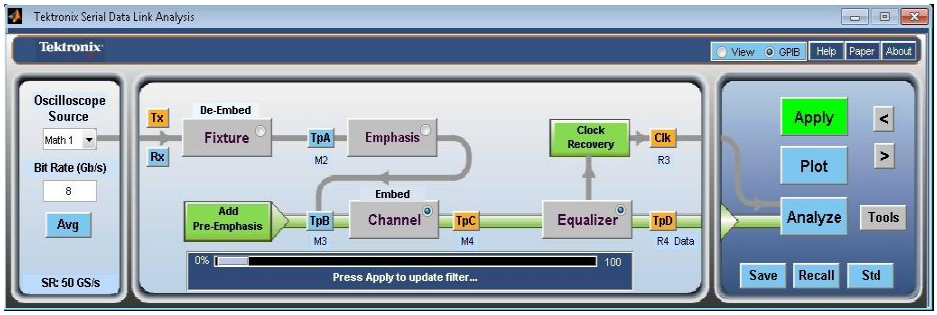


Figure A8: Serial Data Link Analysis window

6. Embed the Compliance Channel

    a. Select the Channel Block on the main SDLA window

    b. Under Data Input Type Select S-Parameter and click browse. Select SystemTx_Embed01_SigTest_Mixed.s4p

    (File is available on *C:\Users\Public\Tektronix\TekApplications\SDLA\input S parameters*)

    c. Select 4-port as the Touchstone format

    d. In the S-Parameter Specification section, select Differential as the Derive Filter from Selection

    e. Under Bandwidth Limit Click None

    f. Select Ok

7. Apply the PCI Express Reference Equalizer

    a. Select the Equalizer Block on the main SDLA window

    b. Select the CTLE and PcieC checkboxes

    c. Select the FFE/DFE and PcieD checkboxes

    d. Select Ok (Note: RunEq can be selected if the channel model has already been applied. Otherwise the waveform needs to be processed by using the Apply button in the main SDLA window)

8. Process waveform

    a. Select Math1 as the input to SDLA

    b. Select 8Gb/s as the data rate

    c. Select Apply on the main SDLA window

    d. SDLA will automatically apply the channel model and determine the optimal CTLE and DFE settings. This process must be re-run anytime a new acquisition is needed.

Note: Nominally the PCIe Rev3.0 bit rate is 8 Gb/s. But if a signal with SSC is tested, the bit rate should be set to 7.98 Gb/s. (0.25% lower)

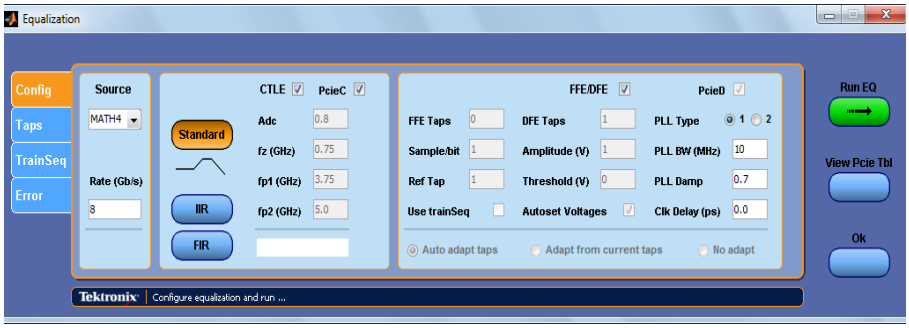


Figure A9: SDLA Equalizer

After SDLA is done processing, go to DPOJET and hit "Clear" and "ReCalc" to run the measurements. The results will be displayed as below.

To repeat measurements press Apply in SDLA and once the new acquisition and calculations are complete, press Recalc in DPOJET for analysis. Optionally, you can clear previous results by pressing Clear. This is necessary when testing different presets.

When measuring systems with short channels, or when doing exploratory testing, CTLE equalization may be sufficient. Then use the setup in R30_SYSTEM folder. This setup does not require SDLA and sets up a CTLE with -7dB gain as an ArbFilter. It does not embed the channel. Press Single to acquire waveforms and calculate measurements. In this mode Free Run is possible.

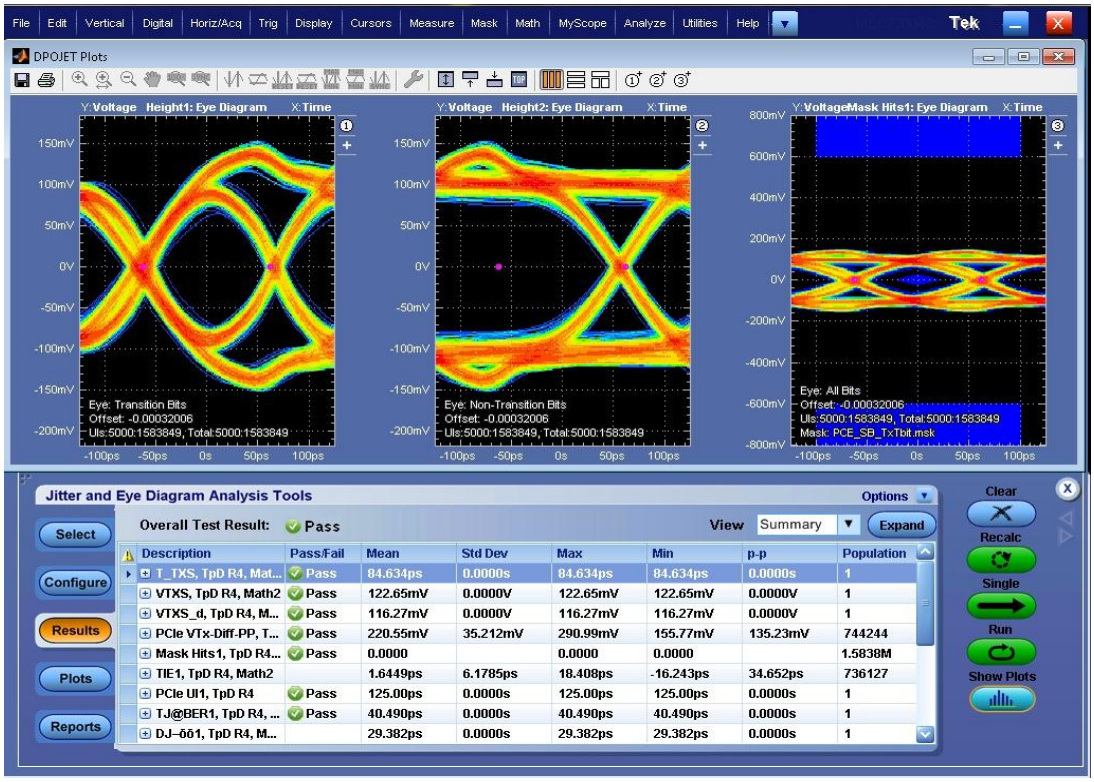


Figure A10: DPOJET Measurement Results

7 Appendix B

To run SDLA in Win7 64 bit manually, user can follow the following steps:

Add-In Card Eye Diagrams

PCI Express Gen 3 testing using SDLA version 2.0. Available on Windows7 64 bit scopes. The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 5.

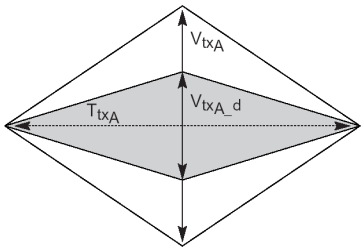


Figure B1: Add-in card compliance eye masks

Load the Add-In Card Setup File in DPOJET:

1. In the scope menu, select Analyze->PCI Express
2. In the DPOJET standard tab, click the select button to choose the Test Point
3. Select Rev3.0->SDLA_Add-In-Card->R30_SDLA_Add-in-Card.set
4. In the Math Menu, set Math1 to Channel 1-Channel 2(Data)

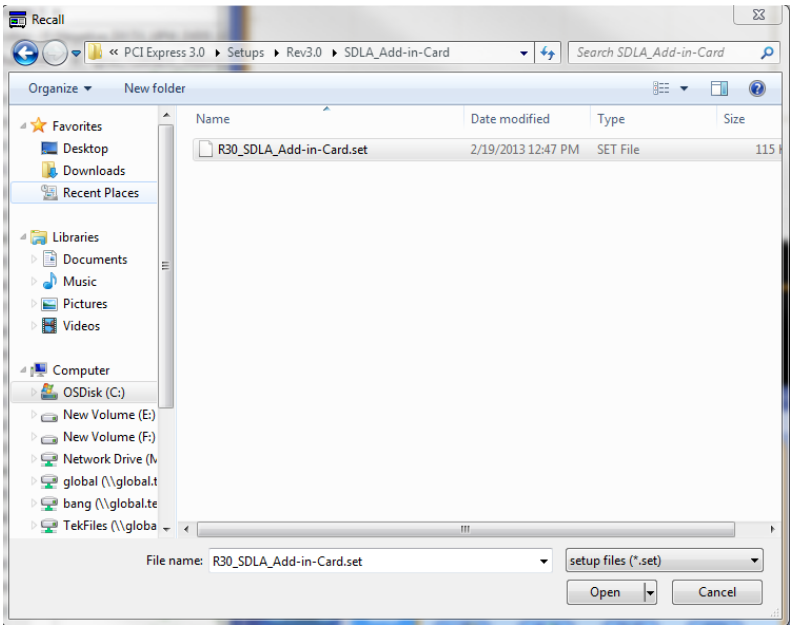


Figure B2: Setup File Selection

Applying Channel and Behavioral Equalizer from SDLA:

These measurements are done using SDLA (Serial Data Link Analysis) behavioral equalizer and channel embedding. Open SDLA from Analyze menu. Select 'Equalizer' and set the CTLE and DFE values as per the PCI Express 3.0 specification. For details of the PCI Express Gen 3 De-embedding procedure refer to the following document in http://www.tek.com/method-implementation/pci-express-30-de-embedding-method-implementation-version-10

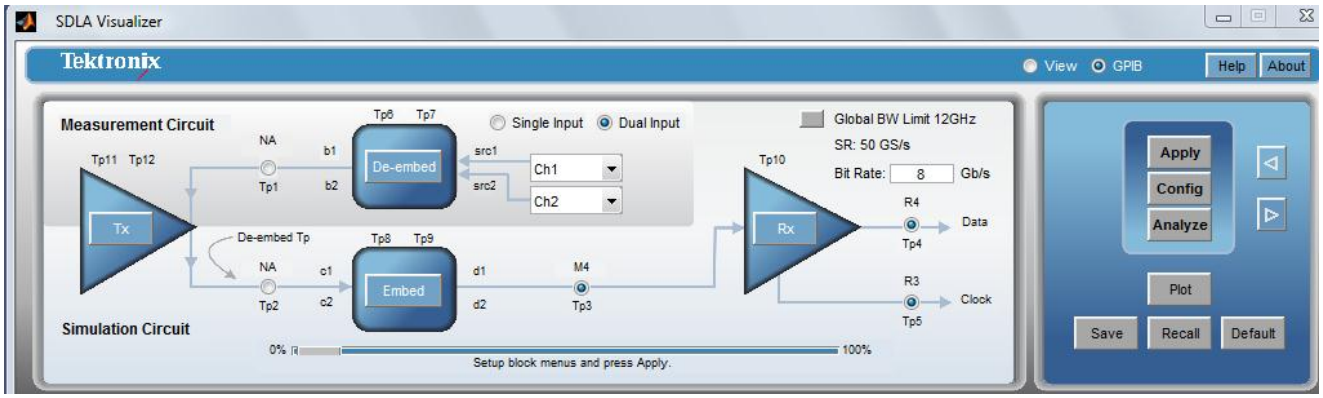


Figure B3: Serial Data Link Analysis window

5. Embed the Compliance Channel
    a. Select Dual Input on the main SDLA window and select Ch1 and Ch2 as input.
    b. Select Embed block on the main SDLA window
    i. Under Embed block, click 'File'. In Model parameter, select '4-Port Differential' type. Click 'Browse' and Select 'AicTx_Test_Embed01_SigTest_Mixed.s4p'

    (File is available on *C:\Users\Public\Tektronix\TekApplications\SDLA\input S parameters*)

    c. Select Ok

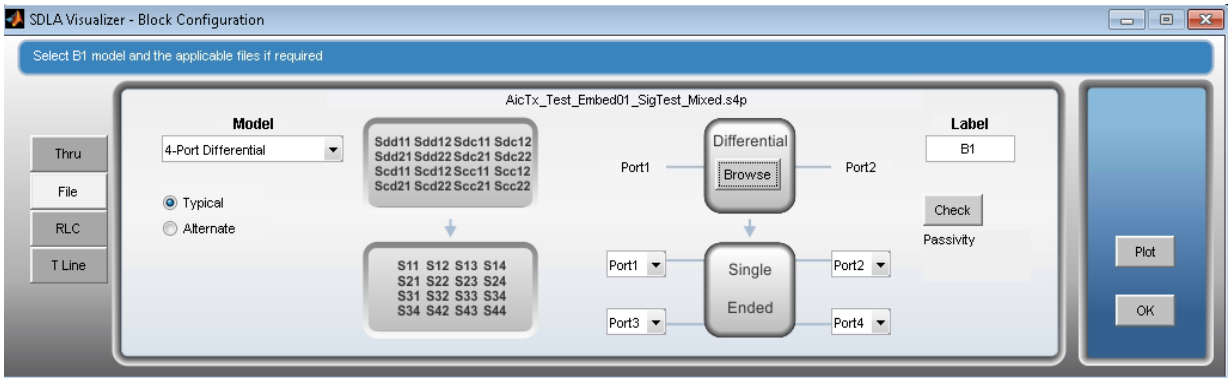


Figure B4: Embadding Channel configuration

6. Apply the PCI Express Reference Equalizer
    a. Select the Rx Equalizer Block on the main SDLA window
    b. Select 'User' button and set 'On'. Select CTLE type as PCIE3.
    c. In Clock Recovery, select Bit Rate as 'Auto Detect'.

d. FFE/DFE set it to 'On'.

e. Select Ok (Note: Run EQ can be selected if the channel model has already been applied. Otherwise the waveform needs to be processed by using the Apply button in the main SDLA window)

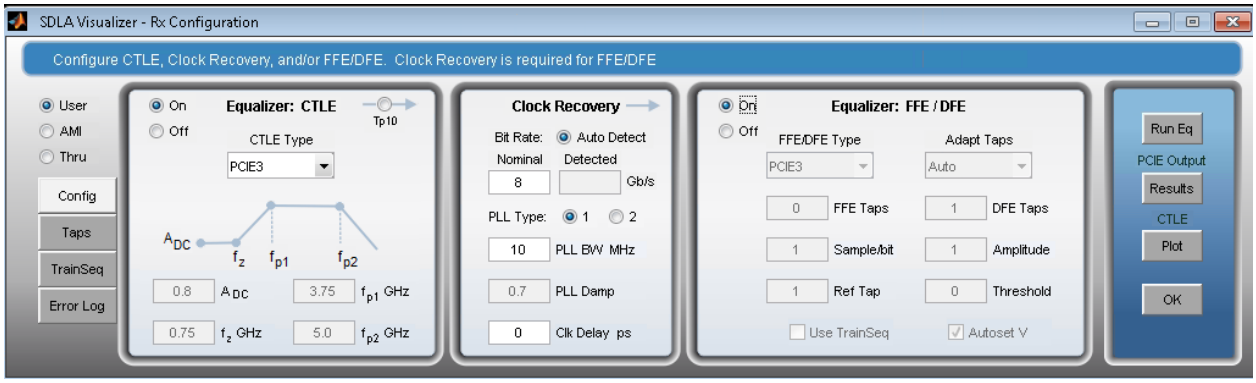


Figure B5: Equalizer settings

7. Process waveform

a. Select the Tp3 button on the main SDLA window and select Math3 as Tp3.

b. Also enable Tp5 (Ref3) for recovered Clock and Tp4 (Ref4) for Data.

c. Select Apply on the main SDLA window

d. SDLA will automatically apply the channel model and determine the optimal CTLE and DFE settings. This process must be re-run anytime a new acquisition is needed.

After SDLA is done processing, go to DPOJET and hit "Clear" and "ReCalc" to run the measurements. The results will be displayed as below:

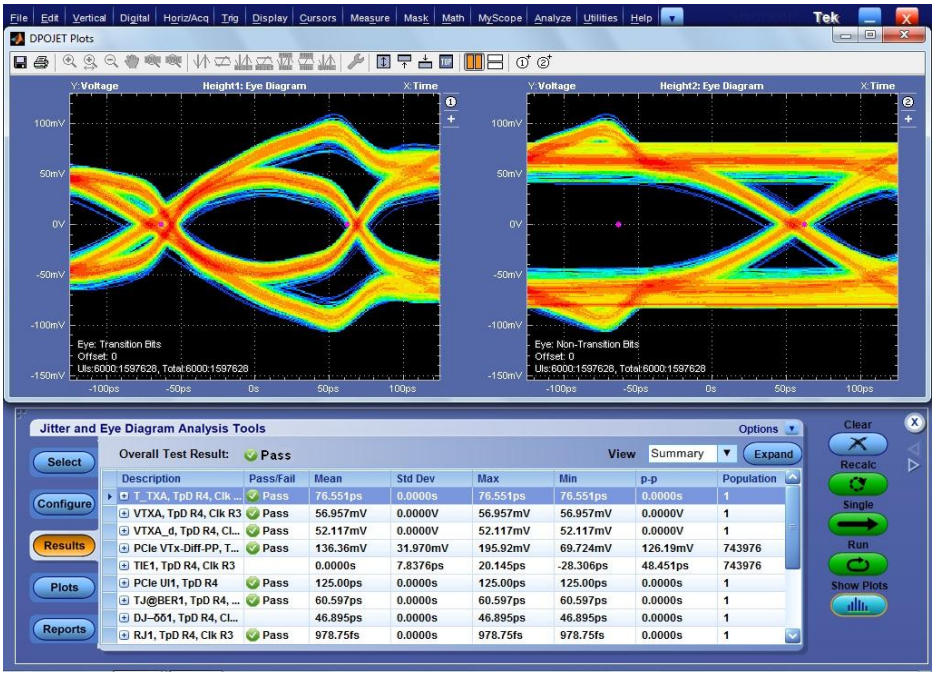


Figure B6: DPOJET Measurement Results

System Board Eye Diagrams

PCI Express Gen 3 testing using SDLA version 2.0. Available on 64-bit Windows 7 scopes. The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 6.

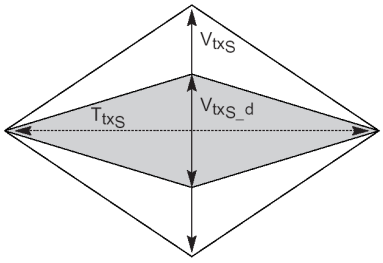


Figure B7: System Board Compliance Eye Masks

Load the System Setup File in DPOJET:

1. In the scope menu, select Analyze->PCI Express
2. In the DPOJET standard tab, click the select button to choose the Test Point
3. Select Rev3.0->SDLA_System->R30_SDLA_SYSTEM.set
4. In the Math Menu, set Math1 to Channel 3-Channel4(Data) and Math2 to Channel 1-Channel 2(Clock)

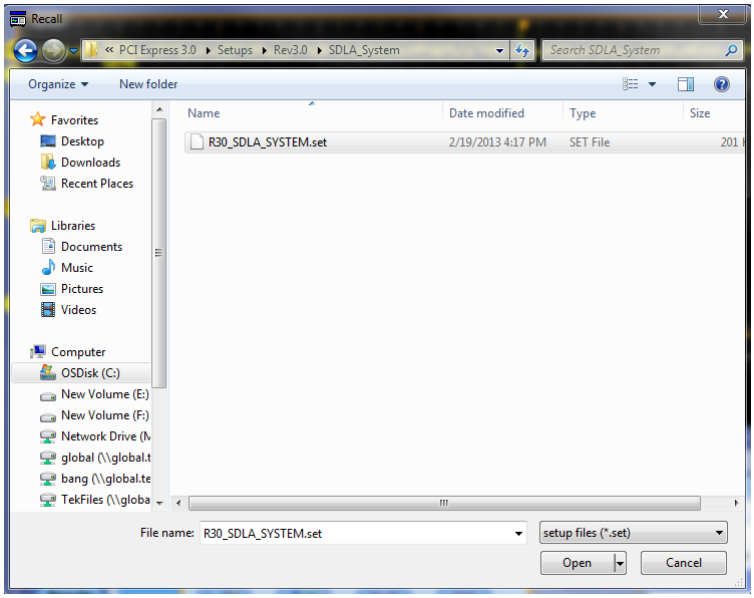


Figure B8: Setup File Selection

Applying Channel and Behavioral Equalizer from SDLA:

These measurements are done using SDLA (Serial Data Link Analysis) behavioral equalizer and channel embedding. Open SDLA from Analyze menu. Select 'Equalizer' and set the CTLE and DFE values as per the PCI Express 3.0 specification. For details of the PCI Express Gen 3 De-embedding procedure refer to the

following document in http://www.tek.com/method-implementation/pci-express-30-de-embedding-method-implementation-version-10

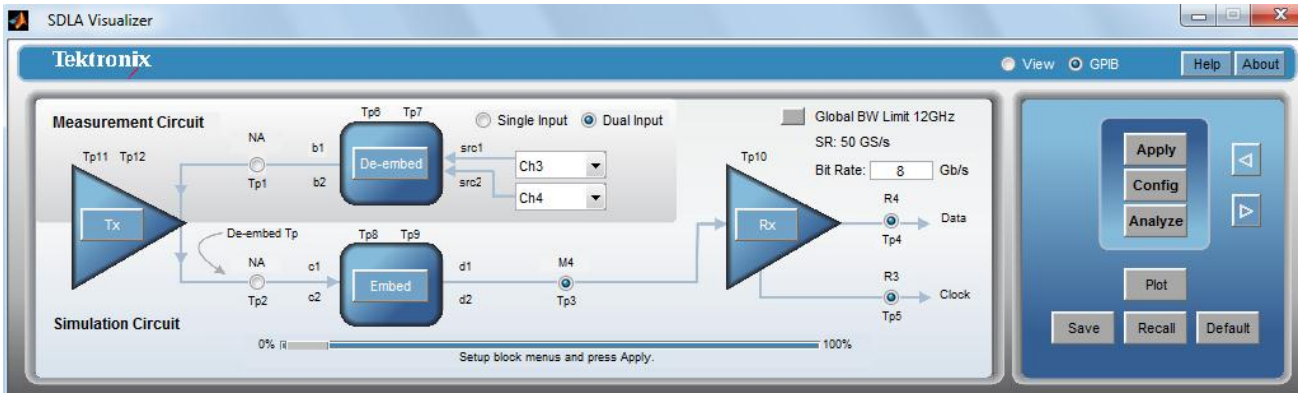


Figure B9: Serial Data Link Analysis window

1. Embed the Compliance Channel
    a. Select Dual Input on the main SDLA window and select Ch1 and Ch2 as input.
    b. Select Embed block on the main SDLA window
    c. Under Embed block, click ‘File’. In Model parameter, select ‘4-Port Differential’ type. Click ‘Browse’ and Select ‘SystemTx_Embed01_SigTest_Mixed.s4p’

        (File is available on C:\Users\Public\Tektronix\TekApplications\SDLA\input S parameters\)

    d. Select Ok

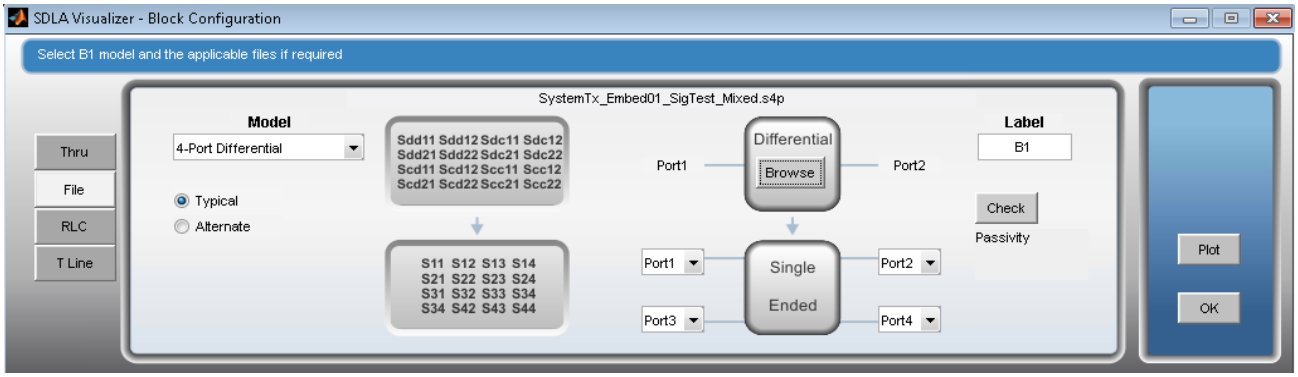


Figure B10: Embedding compliance channel

2. Apply the PCI Express Reference Equalizer
    a. Select the Rx Equalizer Block on the main SDLA window
    b. Select ‘User’ button and set ‘On’. Select CTLE type as PCIE3.
    c. In Clock Recovery, select Bit Rate as ‘Auto Detect’.
    d. FFE/DFE set it to ‘On’.
    e. Select Ok (Note: Run EQ can be selected if the channel model has already been applied. Otherwise the waveform needs to be processed by using the Apply button in the main SDLA window)

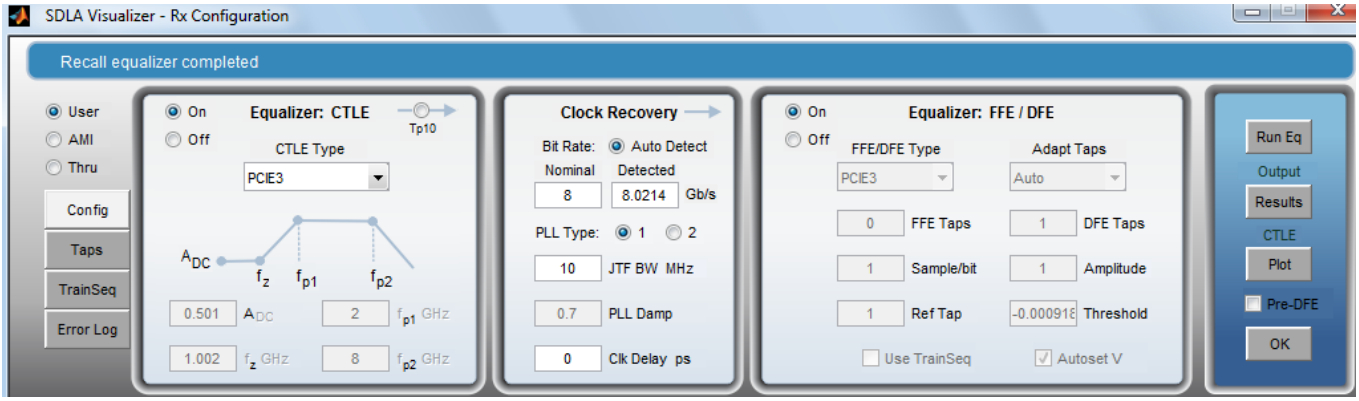


Figure B10: Equalizer settings

3. Process waveform

   a. Select the Tp3 button on the main SDLA window and select Math3 as Tp3.

   b. +lso enable Tp5 (Ref3) for recovered Clock and Tp4 (Ref4) for Data.

   c. Select Apply on the main SDLA window

   d. SDLA will automatically apply the channel model and determine the optimal CTLE and DFE settings. This process must be re-run anytime a new acquisition is needed.

   e. After SDLA is done processing, go to DPOJET and hit "Clear" and "ReCalc" to run the measurements. The results will be displayed as below:

Note: Nominally the PCIe Rev3.0 bit rate is 8 Gb/s. But if a signal with SSC is tested, the bit rate should be set to 7.98 Gb/s. (0.25% lower)

After SDLA is done processing, go to DPOJET and hit "Clear" and "ReCalc" to run the measurements. The results will be displayed as below.

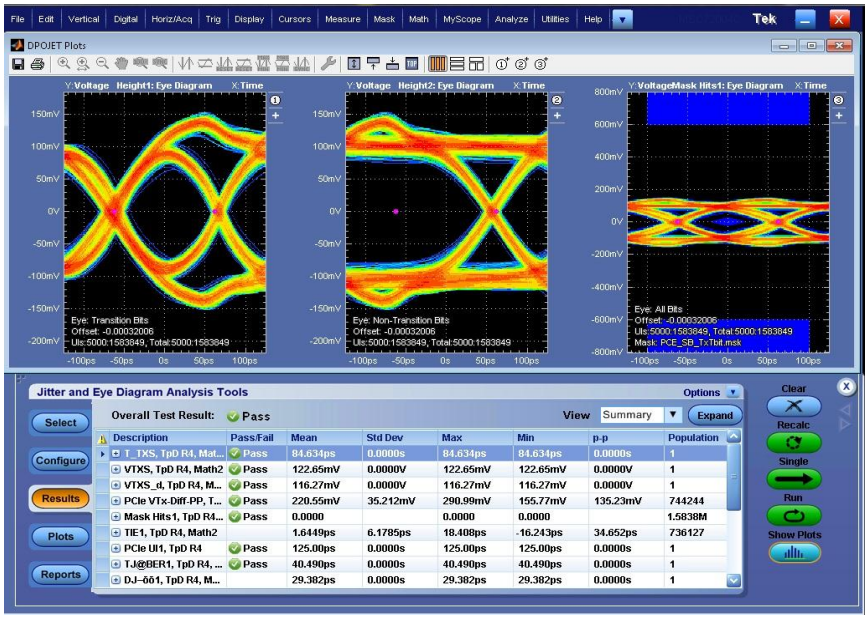


Figure B11: DPOJET Measurement Results

8 Appendix C

8.1 Updated Limit Files

The table shows the update to the limits of certain measurements in the specified limit files. All the other limits not specified in this table remain the same. The changes have been made based on latest limits extracted from SigTest

Limit File Name	Measurement	Old Limit	New Limit
R30_Tx_ADD_CON.xml	T_TXA(Min) (in s)	0	0
		4.125E-11	4.500E-11
	PCIe VTx-Diff-PP(Mean) (in V)	1.200E+00	1.200E+00
		3.400E-02	5.000E-02
	VTXA(Men (in V)	1.200E+00	1.200E+00
		3.400E-02	5.000E-02
	VTXA_d(Mean)(in V)	1.200E+00	1.200E+00
		3.400E-02	5.000E-02
	Min TBit Voltage(Max)(in V)	-2.300E-02	-2.500E-02
		-6.000E-01	-6.000E-01
	Min nTBit Voltage(Max)(in V)	-2.300E-02	-2.500E-02
		-6.000E-01	-6.000E-01
	Max TBit Voltage(Min)(in V)	6.000E-01	6.000E-01
		2.300E-02	2.500E-02
	Max nTBit Voltage(Min)(in V)	6.000E-01	6.000E-01
		2.300E-02	2.500E-02
	TJ@BER1(Mean)(in s)	8.375E-11	8.000E-11
		0	0
	PCIe UI1(Mean) (in s)	1.813E-10	1.26E-10
		8.125E-11	1.25E-10
R30_Tx_SDLA_Add-in-Card.xml	T_TXA(Min) (in s)	0	0
		4.125E-11	4.500E-11
	PCIe VTx-Diff-PP(Mean) (in V)	1.200E+00	1.200E+00
		3.400E-02	5.000E-02
	VTXA(Mean) (in V)	1.200E+00	1.200E+00
		3.400E-02	5.000E-02
	VTXA_d(Mean) (in V)	1.200E+00	1.200E+00

		3.400E-02	5.000E-02
	Min TBit Voltage(Max) (in V)	-2.300E-02	-2.500E-02
		-6.000E-01	-6.000E-01
	Min nTBit Voltage(Max) (in V)	-2.300E-02	-2.500E-02
		-6.000E-01	-6.000E-01
	Max TBit Voltage(Min) (in V)	6.000E-01	6.000E-01
		2.300E-02	2.500E-02
	Max nTBit Voltage(Min) (in V)	6.000E-01	6.000E-01
		2.300E-02	2.500E-02
	TJ@BER1(Mean) (in s)	8.375E-11	8.000E-11
		0	0
	PCIe UI1(Mean) (in s)	1.813E-10	1.257E-10
		8.125E-11	1.250E-10
R30_Base_Rx.xml	TJ@BER(Max) (in s)	N.A	8.125E-11
			0
	DJ–δδ(Max) (in s)	N.A	3.925E-11
			0

8.1 New Limit Files and Limits

The following table shows the limit values from new limit files need to be added to perform PCI Express measurement with SSC.

Limit File Name	Measurement	Limit Value
R11+_Tx_ADD_CON_SSC.xml	PCIe UI (Mean) (in s)	4.02E-10
		4.00E-10
	Height1(Min) (in V)	1.20E+00
		5.14E-01
	Height2(Min) (in V)	1.20E+00
		3.60E-01
	Width(Min)(in s)	0.00E+00
		2.87E-10
	PCIe Med-Mx Jitter(Max)(in s)	5.65E-11
		0.00E+00
R11_Tx_SYSTEM_SSC.xml+	PCIe UI (Mean) (in s)	4.02E-10
		4.00E-10
	Height1(Min)(in V)	1.20E+00

		2.74E-01
	Height2(Min) (in V)	1.20E+00
		2.53E-01
	Width(Min)(in s)	0.00E+00
		2.33E-10
	PCIe Med-Mx Jitter(Max)(in s)	7.70E-11
		0.00E+00
	TJ@BER(Max)(in s)	8.13E-11
		0.00E+00
	DJ–δδ(Max) (in s)	3.93E-11
		0.00E+00

9 Appendix D: Compliance Pattern

The specification shows two different type of pattern which are called

a. Compliance pattern

b. Modified Compliance Pattern

In this MOI we always talk about Compliance Pattern which is defined as repeating sequence of 36 Blocks

1. One block with a Sync Header of 01b followed by a 128-bit unscrambled payload of 64 1's followed by 64 0's
2. One block with a Sync Header of 01b followed by a 128-bit unscrambled payload of the 5 following:

	Lane No modulo 8 = 0	Lane No modulo 8 = 1	Lane No modulo 8 = 2	Lane No modulo 8 = 3	Lane No modulo 8 = 4	Lane No modulo 8 = 5	Lane No modulo 8 = 6	Lane No modulo 8 = 7
Symbol 0	55h	FFh	FFh	FFh	55h	FFh	FFh	FFh
Symbol 1	55h	FFh	FFh	FFh	55h	FFh	FFh	FFh
Symbol 2	55h	00h	FFh	FFh	55h	FFh	FFh	FFh
Symbol 3	55h	00h	FFh	FFh	55h	FFh	F0h	F0h
Symbol 4	55h	00h	FFh	C0h	55h	FFh	00h	00h
Symbol 5	55h	00h	C0h	00h	55h	E0h	00h	00h
Symbol 6	55h	00h	00h	00h	55h	00h	00h	00h
Symbol 7	{P,~P}	{P,~P}	{P,~P}	{P,~P}	{P,~P}	{P,~P}	{P,~P}	{P,~P}
Symbol 8	00h	1Eh	2Dh	3Ch	4Bh	5Ah	69h	78h
Symbol 9	00h	55h	00h	00h	00h	55h	00h	F0h
Symbol 10	00h	55h	00h	00h	00h	55h	00h	00h
Symbol 11	00h	55h	00h	00h	00h	55h	00h	00h
Symbol 12	00h	55h	0Fh	0Fh	00h	55h	07h	00h
Symbol 13	00h	55h	FFh	FFh	00h	55h	FFh	00h
Symbol 14	00h	55h	FFh	FFh	7Fh	55h	FFh	00h
Symbol 15	00h	55h	FFh	FFh	FFh	55h	FFh	00h

Key: P: Indicates the 4-bit encoding of the Transmitter preset being used.
~P: Indicates the bit-wise inverse of P.

3. One block with a Sync Header of 01b followed by a 128-bit unscrambled payload of the following:

	Lane No modulo 8 = 0	Lane No modulo 8 = 1	Lane No modulo 8 = 2	Lane No modulo 8 = 3	Lane No modulo 8 = 4	Lane No modulo 8 = 5	Lane No modulo 8 = 6	Lane No modulo 8 = 7
Symbol 0	FFh	FFh	55h	FFh	FFh	FFh	55h	FFh
Symbol 1	FFh	FFh	55h	FFh	FFh	FFh	55h	FFh
Symbol 2	FFh	FFh	55h	FFh	FFh	FFh	55h	FFh
Symbol 3	F0h	F0h	55h	F0h	F0h	F0h	55h	F0h
Symbol 4	00h	00h	55h	00h	00h	00h	55h	00h
Symbol 5	00h	00h	55h	00h	00h	00h	55h	00h
Symbol 6	00h	00h	55h	00h	00h	00h	55h	00h
Symbol 7	{P,~P}	{P,~P}	{P,~P}	{P,~P}	{P,~P}	{P,~P}	{P,~P}	{P,~P}
Symbol 8	00h	1Eh	2Dh	3Ch	4Bh	5Ah	69h	78h
Symbol 9	00h	00h	00h	55h	00h	00h	00h	55h
Symbol 10	00h	00h	00h	55h	00h	00h	00h	55h
Symbol 11	00h	00h	00h	55h	00h	00h	00h	55h
Symbol 12	FFh	0Fh	0Fh	55h	0Fh	0Fh	0Fh	55h
Symbol 13	FFh	FFh	FFh	55h	FFh	FFh	FFh	55h
Symbol 14	FFh	FFh	FFh	55h	FFh	FFh	FFh	55h
Symbol 15	FFh	FFh	FFh	55h	FFh	FFh	FFh	55h

Key: P: Indicates the 4-bit encoding of the Transmitter preset being used.
~P: Indicates the bit-wise inverse of P.

4. One EIEOS Block
5. 32 Data Blocks, each with a payload of 16 IDL data Symbols (00h) scrambled

10 Appendix D: AC Common Mode Filter Design

The PCIe spec has a specification for Gen2 and Gen3 for AC common mode voltage limited between 30 kHz and 500 MHz. This implies that we need to pass the waveform through a Bandpass filter between 30kHz and 500 Mhz. This can be achieved using SDLA tool as follows:

1. In SDLA Use custom bandwidth, set 0.5Ghz as the bandwidth and 0.8 as the stopband frequency. Use tp1 and assign it to Math2.
2. You shall see an updated filter file in C:\Users\Public\Tektronix\TekApplications\SDLA\output filters\sdlatp1.flt

It may be noted that **SDLA applies the bandwidth limit filter to each test point**, whether any waveform transformation occurs or not. If the Global BW Limit setting is None then obviously no filtering occurs.

The filter hereby designed can be used as an Arbflt in Math definition to pass the full bandwidth data through it and filtering waveform at 500 Mhz.