The Need for a New Margin Testing Solution in PCIe® Testing

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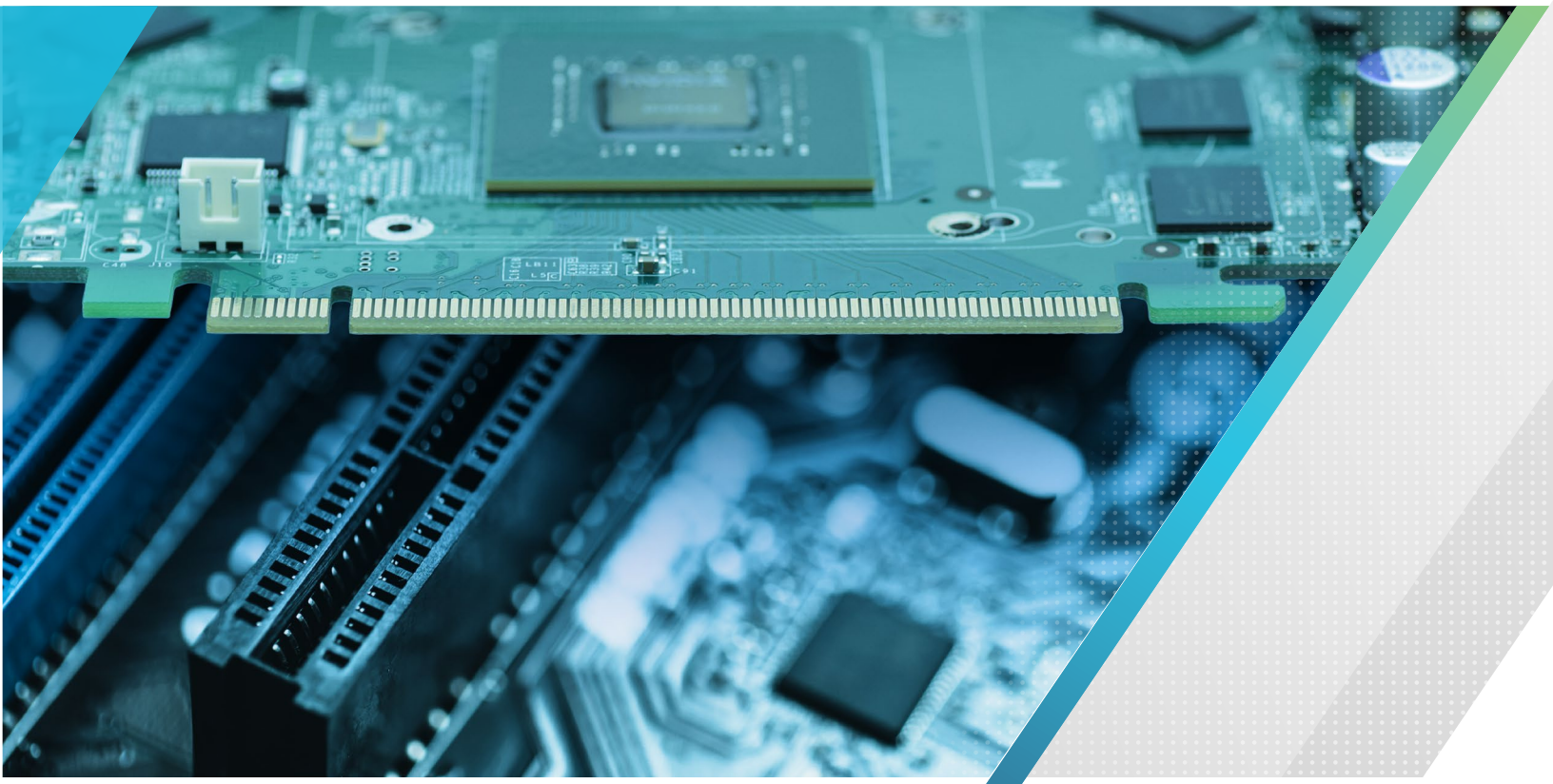
WHITE PAPER



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Introduction

As the world continues to progress towards faster and faster data rates, the time and complexity of validating new technologies has risen exponentially. Development bottlenecks resulting from increased testing times and limited resources are slowing product time-to-market cycles, yet companies expect the same development cycles from their engineering teams in today's world using the same legacy test and measurement solutions.

Not only are the testing times and complexities increasing, but consumers continue to hold high expectations for product performance and interoperability. End users of PCIe-compatible devices expect to plug any PCI Special Interest Group (PCI-SIG®) compliant add-in card (AIC) into any PCI-SIG compliant system board of the same generation or older. This expectation means that testing must be stringent, and that each vendor must have adequate design margins to ensure interoperability with all other PCI-SIG compliant products.

The major problems consumers face when two products do not work together is who to blame. Is it the system board manufacturer? The add-in-card manufacturer? Both? Who does the consumer go to when there is a problem? Unfortunately, issues like this can cause both vendors to undergo cost-intensive investigations into who is at fault, and these investigations can take months, and cost upwards of millions of dollars to fully resolve.

While slim design margins are not the *only* way in which two boards may struggle to interoperate with one another, having adequate design margins significantly reduces the risk of not being interoperable with other PCI-SIG compliant products. This can save vendors both time and money in reducing the number of situations where they need to resolve interoperability issues.

Margin Testing Today

Today, there are 2 common methods to test for design margins in HSIO designs, and both come with associated pros and cons.

1. **Scope/BERT** – test systems consisting of an oscilloscope, Bit Error Rate Tester (BERT), and Sigtest software available from the PCI-SIG. This solution can cost a half million dollars or more.

2. On-chip Lane Margining (**LM**) – tools offered by silicon manufacturers to board manufacturers. This option is free starting with the PCIe Gen 4 standard.

The most comprehensive testing toolset is the combination of the Scope/BERT. This solution can complete all validation and compliance testing needed to satisfy the standard and certify compliance of PCIe devices, but it comes with high levels of complexity, and a price tag that smaller manufacturers often cannot justify or afford. At a cost of a half-million dollars or more per system, even larger vendors have a limited number of systems to perform their testing.

Even experienced engineers may need several days to get these test systems fully operational, and full testing of 16-lane links can take weeks beyond initial setup if issues arise. These test systems are superior to any on-chip LM tools available from silicon manufacturers, but they are expensive, time consuming, and often require high levels of expertise to operate properly. This equipment is required for full compliance and extensive silicon validation, whereas the LM tools can be used for limited-scope checks without the overhead.

While free LM tools provide some performance insight at no cost and are less complex than Scope/BERT systems, they have numerous limitations. Firstly, LM tools are only capable of lane margining at their own receivers. The user is capable of only investigating margins of the DUT receiver path (Rx), but unable to margin the DUT transmitter (Tx) path.

Another drawback of LM tools is they vary vendor to vendor, requiring a learning curve for engineers to familiarize themselves with each tool. This repeated ramp-up could be overcome with a consistent third party method. Finally, the inherent unit-to-unit variability that is inextricably linked to chip variability will exist. This often requires multiple testing cycles to increase the measurement population and rely on measures of central tendency.

Notably the testing methodologies between these methods differ. The Scope Tx approach (**Figure 2**) uses real-time sampling to construct eye diagrams, where on-chip LM tools rely on sweeping the Rx sample location until errors are observed (to determine eye width). Some LM implementations also determine eye height with vertical sampler adjustments (**Figure 1**). Real-time signaling is the better option as engineers see an independently constructed eye diagram. The LM approach is a trade-off with a loss of accuracy and consistency when cost and complexity of the Scope/BERT cannot be justified.

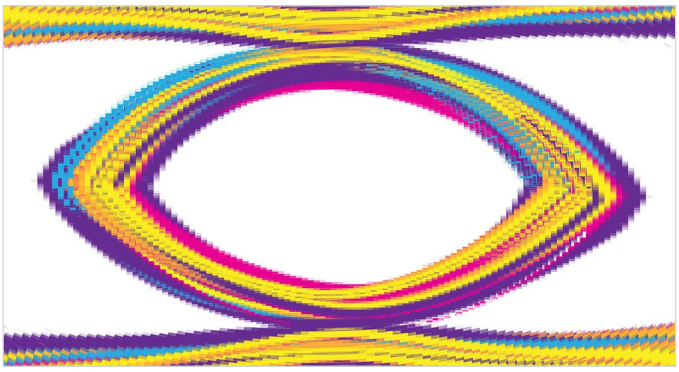

Figure 1: Example On-Chip Receiver Eye Diagram

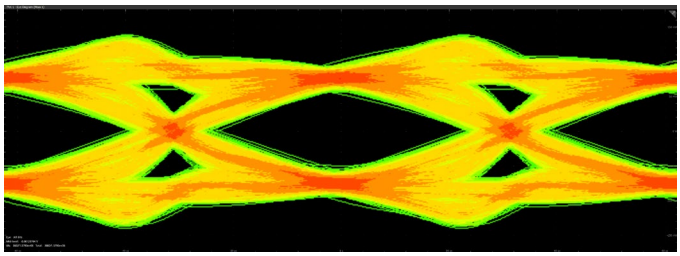

Figure 2: Real Time Analog Eye Diagram

Bringing consistency between true link operation and the test environment is key, with two key considerations being the type of traffic (signal pattern) and the type of receiver used. Scope/BERT systems use a model receiver with repetitive signal patterns to stress and test the transceivers as outlined in the PCIe standards. On-chip LM tools use a physical receiver with real traffic on the link. The nature of these tests causes the discrepancy. The Scope/BERT systems are not built with a PCI Express receiver and have memory/storage and signal post processing limitations. The LM tools rely on a physical receiver implementation acting as a link partner with true traffic flow instead of artificial signal patterns.

Both methods have pros and cons. Importantly, the only solution allowed for full validation and compliance testing is the Scop/BERT methodology. LM tools are not capable of addressing all required tests to ensure validation and compliance to the PCIe standard.

Pros and cons for existing testing methods

Scope/BERT System (Oscilloscope + BERT + SigTest software)	
Advantages: • Provides a comprehensive suite of tests suitable for full validation and compliance testing • Test specifications are written with the scope as the reference • Capable of constructing full channel Tx eye diagram, jitter decomposition, and receiver stressed eye calibration • Uses real-time sampling to construct eye diagrams • General purpose test equipment limited to testing one technology	**Disadvantages:** • Cost-prohibitive • Test times can be days to weeks depending on testing requirements • Testing complexities level often requires senior-level engineering expertise • Complexities of the system can lead to errors and incorrect conclusions • Artificial signal patterns don't properly capture multiple crosstalk impacts from real aggressors

On-Die Lane Margining Tool	
Advantages: • Standardized tool starting with the PCI Express 4.0 standard • Provided free to designers from silicon vendors • Developed specifically for identifying margins at the vendor's receivers • Easy to use if familiar with PCIe • Rx margin data available in minutes, not days or weeks	**Disadvantages:** • Do not use real-time analog signals • Are not often offered on devices below 16 GT/s • Cannot be used for complete validation or compliance testing • Introduces unit to unit variability • Difficult to vary design or test parameters in a significant way • Software interface non-standardized

Coming Soon: A New Margin Testing Alternative

PCIe link health evaluation solutions today have their trade-offs, and there have not been any tools that help alleviate the big disadvantages from each solution, while maximizing the advantages.

Engineers who are testing PCIe Gen 3 and Gen 4 devices today understand these testing gaps, but do not have a solution available to help address them.

Tektronix will soon launch a new class of test and measurement product that addresses the major pain points associated with margin testing today. We believe for PCIe Gen 3 and Gen 4 margin testing customers will find this new approach offers:

1. Out-of-the-box ease of use for junior engineers or technicians with little-to-no PCIe experience
2. Evaluation of link health with Tx and Rx testing that takes minutes, not days
3. A margin testing tool that is cost-effective for all

More detail will be made available at the launch. So sign up now to be the first learn about our new solution.

About the Author

Michael Seaholm is a Product Manager for Performance Oscilloscopes at Tektronix, Inc. He has spent 4 years as a Product Manager in the Test and Measurement industry, including 3 years at Fluke Corporation in their Electrical Calibration Business and over a year at Tektronix. Michael has a BSEE in Electrical Engineering from Montana State University and has spent his career in Product Management focused on bringing new innovations to test and measurement through consistent engagement with customers.

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