PCI Express Rx-Tx-Protocol Solutions



Customer Presentation
December 13, 2013

Tektronix

Agenda

- PCIe Gen4 Update
- PCIe Gen3 Overview
- PCIe Gen3 Tx Solutions
- Tx Demo
- PCIe Gen3 Rx Solutions
- Rx Demo
- PCIe Gen3 Protocol Solutions

PCIe Gen4 Update



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Gen4 Update

- Key attributes/requirements of PCIe 4.0
  - 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  - Maintains compatibility w/ PCIe installed base
  - Connector enhanced electrically (no mechanical changes)
  - Limited channel: ~12”, 1 connector; repeater for longer reach
- Uniform measurement methodology applied across all data rates
- New ‘SRIS’ independent RefClk modes
  - SRIS – Separate RefClk Independent SSC Architecture
- Rev 0.3 Base spec just introduced in PCI-SIG (June 2013)
  - Rev 0.9 no earlier than 1H/2015
  - Rev 1.0 no earlier than 2H/2015

Gen4 Update

Latest Gen4 Update @ PCIe DevCon on Tue/Wed, June 25-26

- Tx Jitter – Analysis solution available today with PCE3.
- Tx EQ – CEM and Embedded will have limited change. Base might require Sampling solution.
- Rx – Similar approach at 16Gb/s.

Transmitter Jitter Spec

- PCIe 4.0 uses same jitter parameters as PCIe 3.0
  - ✓ $T_{TX-UPW-TJ}$, $T_{TX-UPW-DJDD}$, T_{TX-DDJ}, T_{TX-UTJ} and $T_{TX-UDJDD}$
  - ✓ Jitter will need to scale approximately with bitrate
  - ✓ De-embedding approach will likely remain the same
- PCIe 1.x and PCIe 2.x jitter parameters will be recast into the same form as the PCIe 3.0 parameters
  - ✓ Backward compatibility will be guaranteed
  - ✓ Some PCIe 1.x/2.x parameters will be effectively tightened
  - ✓ Example: PCIe 2.x $T_{MIN-PULSE}$ parameter will be converted into $T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$

PCIe 4.0 Rx Specification

- Will continue to rely upon a stressed eye approach where both EH and EW are stressed
  - ✓ Calibration channels IL will need to be reduced to yield ~24 dB at 8 GHz
  - ✓ Behavioral package model needs to comprehend reduced C_{PAD} or include T-coil models
  - ✓ Behavioral DFE model to have increased number of taps, at least 2
  - ✓ More capable CTLE model

Transmitter Equalization

- Max PCIe 4.0 channel IL remains approx the same s for PCIe 3.0
- Plan is to retain same equalization presets
  - ✓ Training will require that only a subset of the presets be used (P7 and P8)
- Equalization coefficient range and resolution also are intended to remain unchanged
- EIEOS signaling will likely change such that no TxEQ is applied during the EIEOS interval

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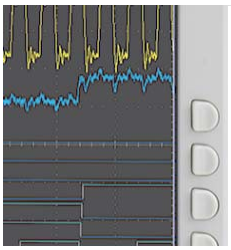
PCIe Gen3 Overview



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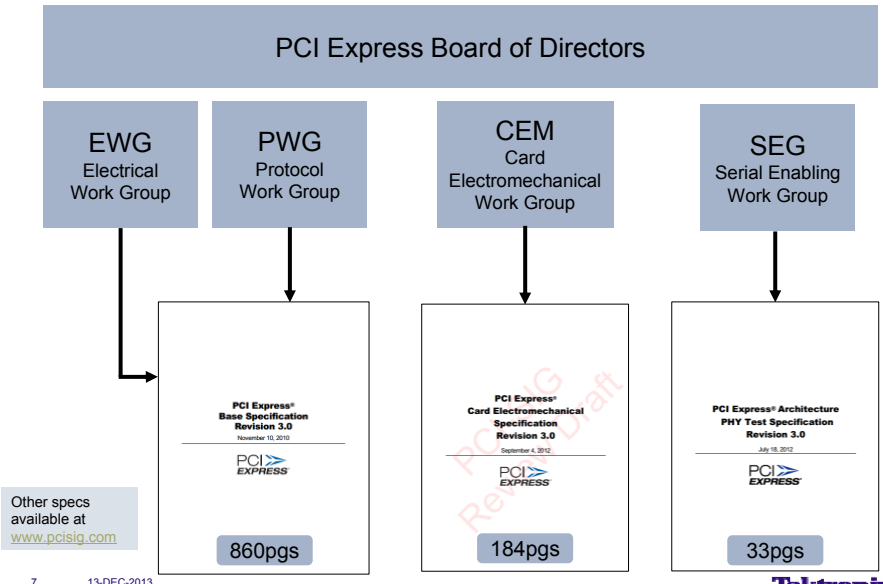
PCI-SIG PCI Express Standards Organization



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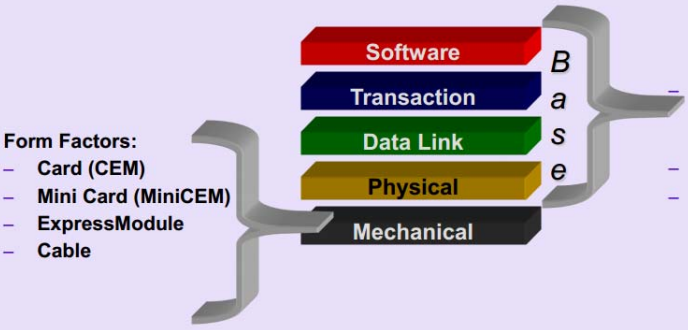
PCIe Specifications



Form Factors:
- Card (CEM)
- Mini Card (MiniCEM)
- ExpressModule
- Cable

- **Base**
  - Electrical
  - Protocol
  - Configuration
- **Bridge**
- **I/O Virtualization**
  - Single Root
  - Multi-Root
  - Address Translation Services

PCI-SIG Developers Conference 25

PCI-SIG DevCon June 2012, "PCI-SIG Architecture Overview"

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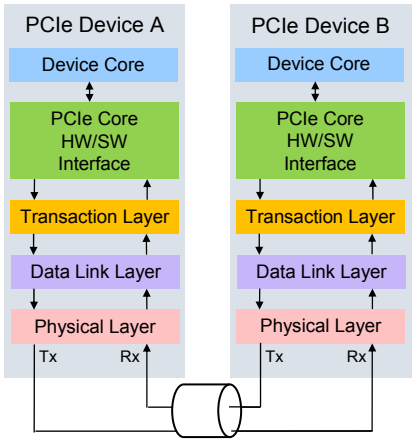
Testing Challenges with PCI Express 3.0



Transaction Layer
- Creates Request/Completion Transactions
- Messaging
- TLP Flow Control

Data Link Layer
- Flow control information
- Data Integrity, Error Checking/Correction
- Calculates/Check TLP Sequence Number
- Calculate/Check CRC

Physical Layer – Logical Sub Block
- Link Initialization and Training
- Distribution of packet information over multiple lanes
- Power management and link power state

Physical Layer – Electrical Sub Block
- Transmitter Signal Quality and Ref Clock Testing
- Receiver Testing
- Interconnect Testing
- PLL Loop BW
- TX/RX equalization
- Faster Bit Rates
- Separate Jitter Budget

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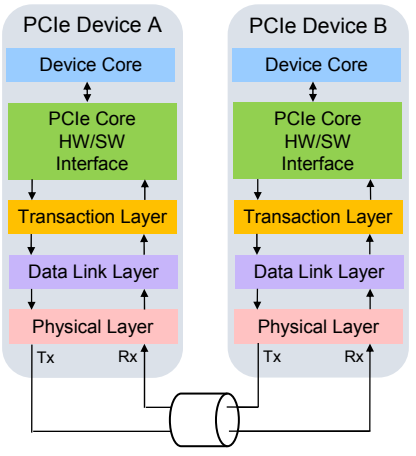
Testing Challenges with PCI Express 3.0



Logic Protocol Analyzer

Oscilloscope
Tx

BERTScope
Rx

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PCIe Gen3 Tx Solutions



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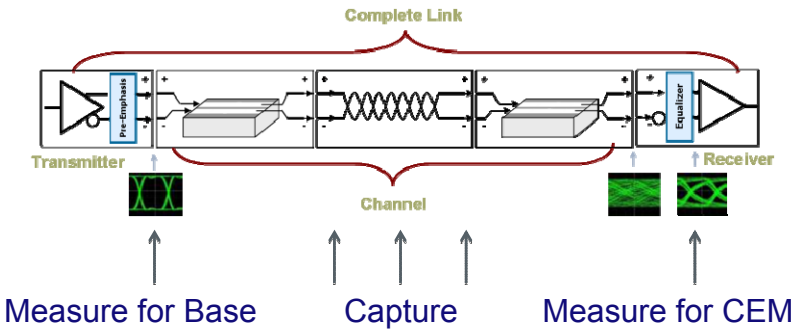
PCIe Base vs CEM Testing

- What test point each type of testing addresses?
- How do we get to see the signal at the point of interest?



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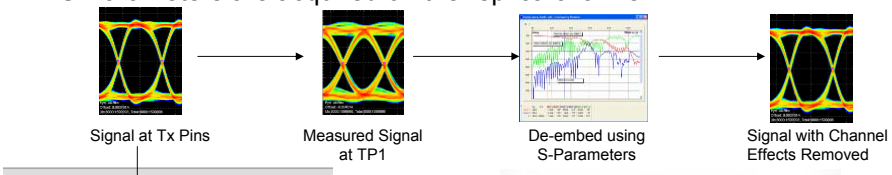
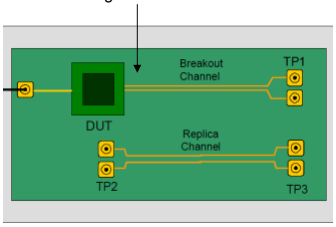
System (Base Spec) Tx Testing

- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not possible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- S-Parameters are acquired on the replica channel

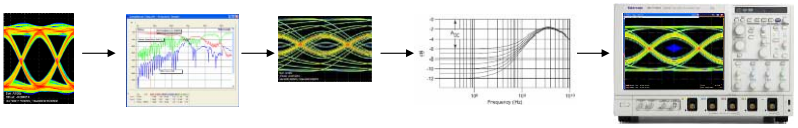


Signal at Tx Pins | Measured Signal at TP1 | De-embed using S-Parameters | Signal with Channel Effects Removed



Add-In Card (CEM Spec) Tx Testing

- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements

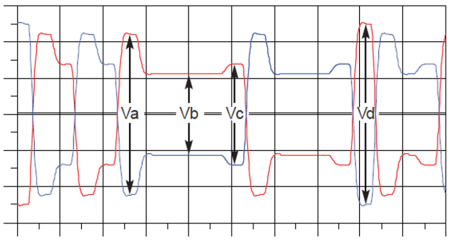


Signal Acquired from Compliance Board | Embed Compliance Channel and Package | Closed Eye due to the Channel | Apply CTLE + DFE | Open Eye for Measurements

Compliance Patterns

- Once in compliance mode, bursts of 100MHz clock can used to cycle through various settings of compliance patterns to perform, Jitter, voltage, timing measurements.

Data Rate	Preshoot	De-emphasis
2.5 GT/s,		-3.5 dB
5.0 GT/s,		-3.5 dB
5.0 GT/s,		-6.0 dB
8.0 GT/s,	P0 = 0.0	-6.0±1.5dB
8.0 GT/s,	P1 = 0.0	-3.5±1.5dB
8.0 GT/s,	P2 = 0.0	-4.4±1.5dB
8.0 GT/s,	P3 = 0.0	-2.5±1dB
8.0 GT/s,	P4 = 0.0	0.0dB
8.0 GT/s,	P5 = 1.9±1dB	0.0dB
8.0 GT/s,	P6 = 1.9±1dB	0.0dB
8.0 GT/s,	P7 = 1.9±1dB	-6.0±1.5dB
8.0 GT/s,	P8 = 1.9±1dB	-3.5±1dB
8.0 GT/s,	P9 = 1.9±1dB	0.0dB
8.0 GT/s,	P10 = 1.9±1dB	Test Max Boost Limit



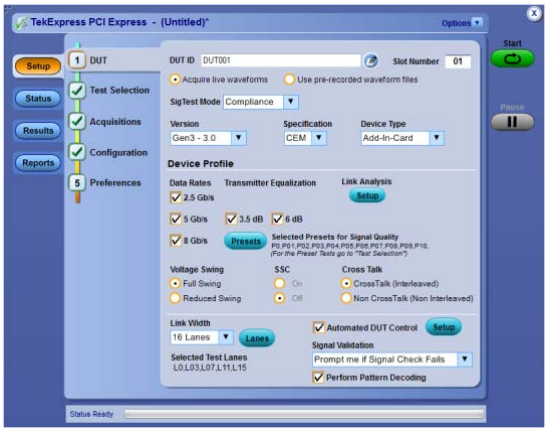
De-emphasis = $20\log_{10}$ Vb/Va
Preshoot = $20\log_{10}$ Vc/Vb
Boost = $20\log_{10}$ Vd/Vb

Testing Challenges in Tx

- Meet the requirements for effective testing
  - √ Compliance mode support, proper patterns and toggling mechanism
  - √ Correct Tx equalization settings and preset and Lane ID encoding in Tx compliance pattern
- Why so many presets? How to capture so many lanes?
  - √ The answer is test automation, RF switch
- Measurement algorithms
  - √ Implemented in SigTest, or scope specific software
- How to achieve required confidence level and beyond?
  - √ Length and number of waveforms (for Tx)

Introducing the NEW Opt PCE3

- TekExpress Automation for Tx Compliance with unique features including:
  - √ Sets up the Scope and DUT for testing
  - √ Toggles thru and verifies the different Presets and Bit Rates
  - √ Tests multiple slots and lanes
  - √ Acquires the data
  - √ Processed with PCI-SIG SigTest
  - √ Provides custom reporting



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What's New in Option PCE3 Release 2?

- Supports a faster, Python-based sequencer
  - Much faster program launch with the test time reduced by ~50%
  - 64-bit only application (requires 70K C/D oscilloscopes with Win7 64-bit)
    - Will maintain earlier 32-bit release for 70K A/B oscilloscopes with WinXP 32-bit on www.tek.com
  - Smaller installer
- SigTest.exe (Command-Line) integration
  - Supports PCI-SIG recommended SigTest.exe testing
  - User can switch between DLL and Command-Line (.exe) modes
  - All result are populated in Tektronix result/report format in command line mode
- Support multiple versions of SigTest
  - User option to select required version and run
  - Broader AWG/AFG support for automatic DUT toggle *(Min 2ch & 100MHz Burst mode)*
  - AFG3252/C
  - AWG5002B/C, AWG5012B/C, AWG5014B/C
  - AWG7082B/C, AWG7122B/C
  - AWG70001A/2A
- Incorporates customer & field feedback
  - Crosstalk option is added
  - Gen2 System-Board limit issue fixed
  - Addresses 6 customer-reported issues & ~30 PCIe Workshop-reported issues

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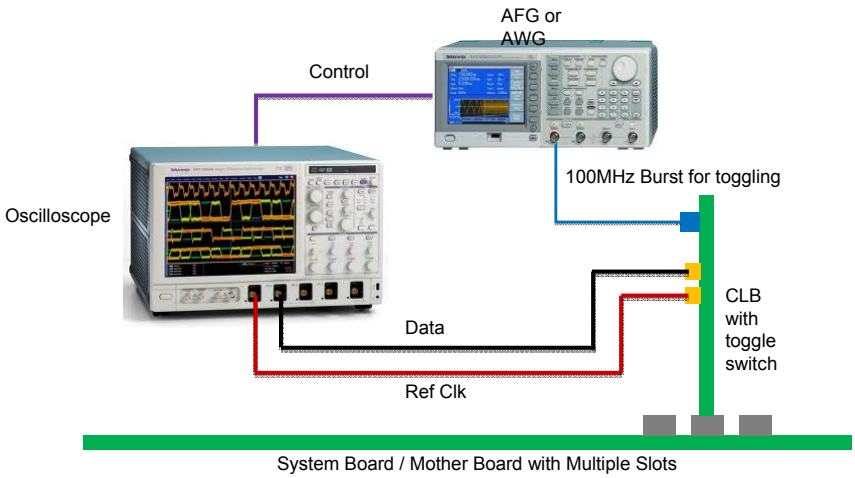
Automation Simplifies Tx Testing

- While convenient single capture capability is essential, automation makes the testing practical
- Iterate over multiple presets and lanes
- Gather results in a single report
- Provide means for quick switch to debugging and additional measurements
- Remove test fixture effects by using de-embedding

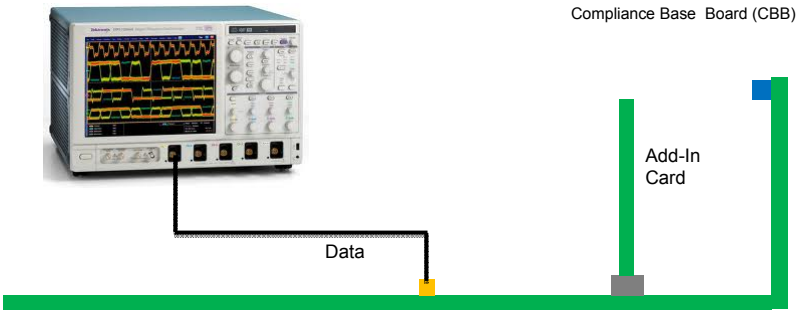
Automated DUT Control



Add-In Card Test Fixture

- Compliance Base Board (CBB)
  - Used for Testing Add-In cards
  - All Tx / Rx Lanes are routed to SMP
  - Compliance Mode Toggle Switch
  - Low Jitter Clean Reference Clock
  - Separate CBB for Gen 1/2/3

Compliance Base Board (CBB)



CBB with Multiple Slots of different widths and toggle switch

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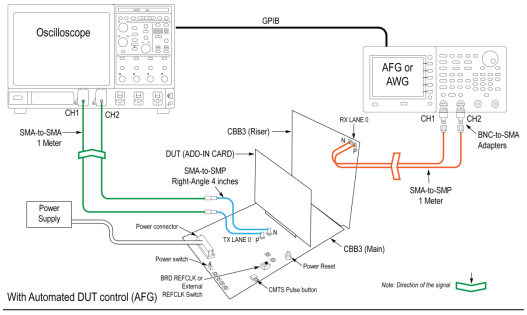
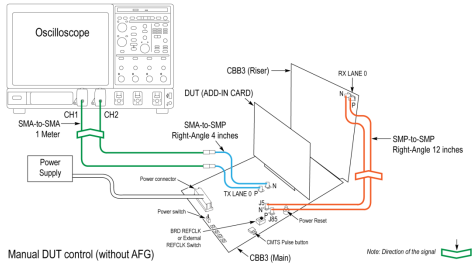
CBB3 Config for Automatic & Manual DUT Control



With Automated DUT control (AFG)



Manual DUT control (without AFG)

Refer to "PCIe 3.0 Compliance Base Board (CBB3.0) Test Fixture User's Document", www.pcisig.com

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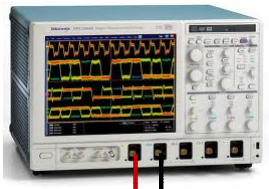
System Test Fixtures

- Compliance Load Board (CLB)
  - Used for testing System Boards
  - All Tx / Rx Lanes and Ref Clk routed to SMP
  - Compliance Mode Toggle Switch
  - Various types of Edge Connectors to support different types of Slots on System Boards
  - Separate CLB's for Gen1/2/3

Compliance Load Board (CLB)



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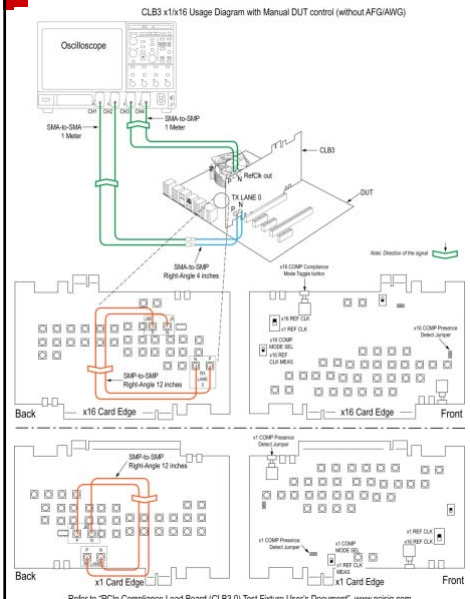
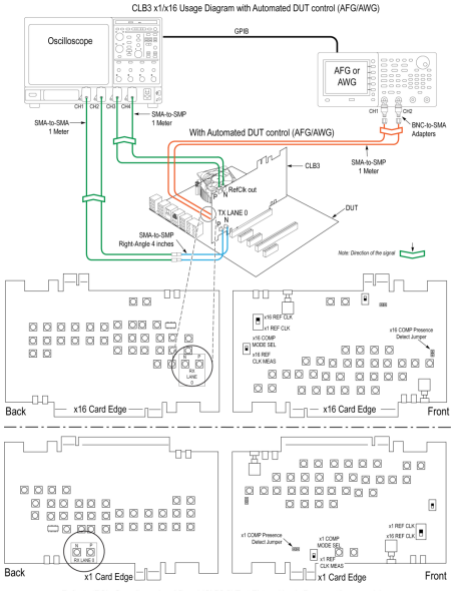
x1/x16 CLB3 Config for Automatic & Manual DUT Control





Refer to "PCIe Compliance Load Board (CLB3.0) Test Fixture User's Document", www.pcisig.com

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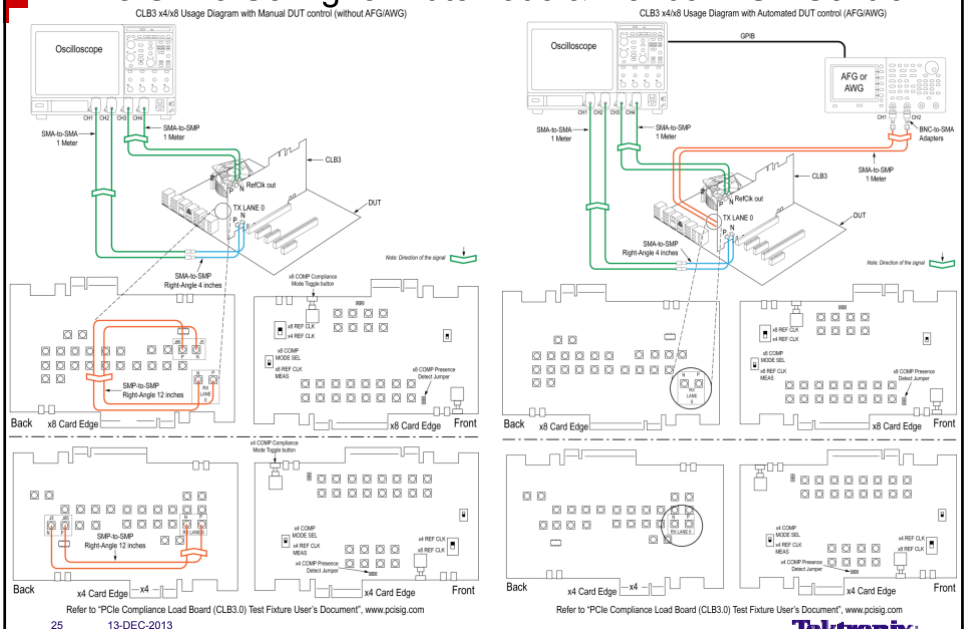
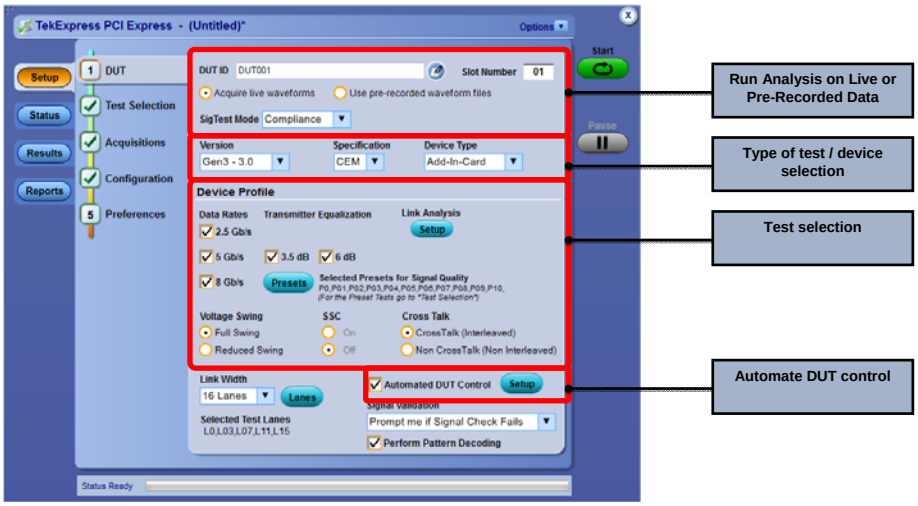
x4/x8 CLB3 Config for Automatic & Manual DUT Control



TekExpress Automation for Tx Compliance - Setup



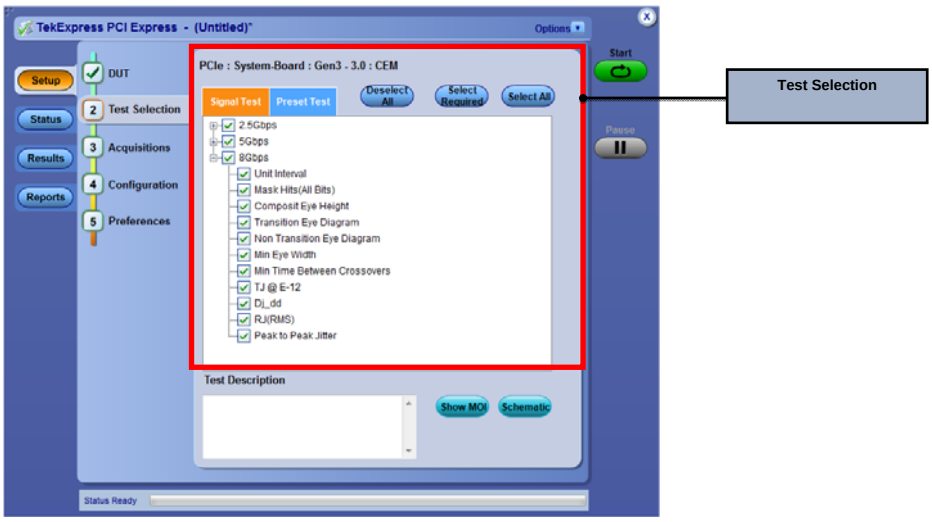
Run Analysis on Live or Pre-Recorded Data

Type of test / device selection

Test selection

Automate DUT control

TekExpress Automation for Tx Compliance – Test



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TekExpress Automation for Tx Compliance – Reports

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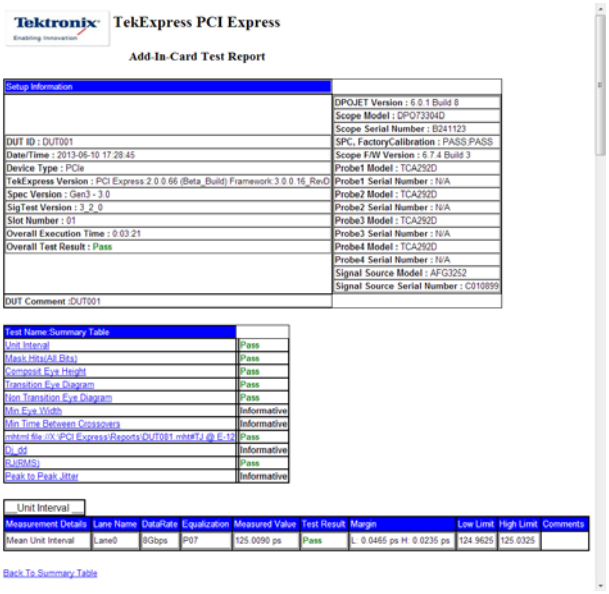
TekExpress Automation for Tx Compliance – Reports



Tektronix TekExpress PCI Express

Add-In-Card Test Report

Setup Information	
	DPOJET Version : 6.0.1 Build 8
	Scope Model : DPO73304D
	Scope Serial Number : B241123
DUT ID : DUT001	SPC, FactoryCalibration : PASS,PASS
Date/Time : 2013-06-10 17:28:45	Scope F/W Version : 6.7.4 Build 3
Device Type : PCIe	Probe1 Model : TCA292D
TekExpress Version : PCI Express 2.0.0.66 (Beta_Build) Framework 3.0.0.16_RevD	Probe1 Serial Number : N/A
Spec Version : Gen3 - 3.0	Probe2 Model : TCA292D
SigTest Version : 3_2_0	Probe2 Serial Number : N/A
Slot Number : 01	Probe3 Model : TCA292D
Overall Execution Time : 0:03:21	Probe3 Serial Number : N/A
Overall Test Result : Pass	Probe4 Model : TCA292D
	Probe4 Serial Number : N/A
	Signal Source Model : AFG3252
	Signal Source Serial Number : C010899
DUT Comment :DUT001	

Test Name Summary Table	
Unit Interval	Pass
Mask Hits(All Bits)	Pass
Composit Eye Height	Pass
Transition Eye Diagram	Pass
Non Transition Eye Diagram	Pass
Min Eye Width	Informative
Min Time Between Crossovers	Informative
mhtml:file ///X:/PCI Express/Reports/DUT001.mht#TJ @ E-12	Pass
DJ_dd	Informative
RJ(RMS)	Pass
Peak to Peak Jitter	Informative

Unit Interval

Measurement Details	Lane Name	DataRate	Equalization	Measured Value	Test Result	Margin	Low Limit	High Limit	Comments
Mean Unit Interval	Lane0	8Gbps	P07	125.0090 ps	Pass	L: 0.0465 ps H: 0.0235 ps	124.9625	125.0325	

Back To Summary Table

Transition Eye Diagram

Transition Eye - Lane0 8Gbps P07

Back To Summary Table

Non Transition Eye Diagram

Non Transition Eye - Lane0 8Gbps P07

Back To Summary Table

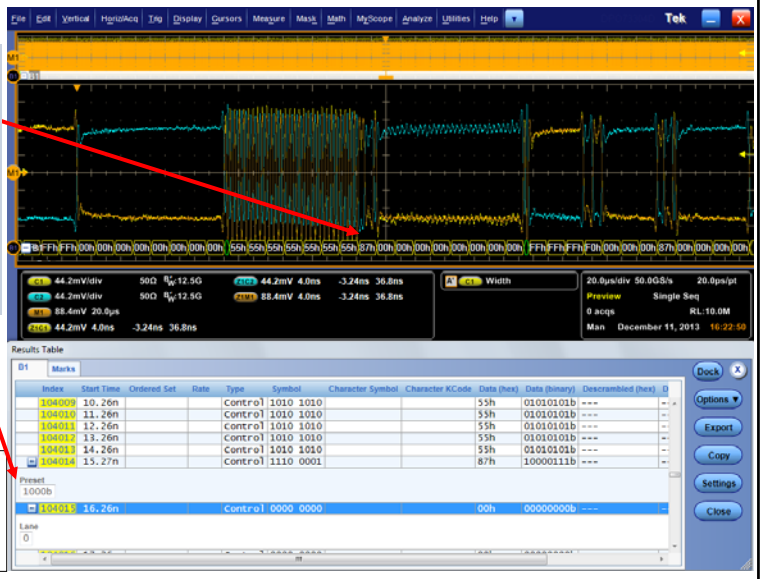
PCIe Decoder (Opt SR-PCIe)

- Decodes and displays PCIe data using characters and names that are familiar from the standard, such as:
  - SKP
  - Electrical Idle
  - EIEOS
- Easily configured through “Bus Setup” under “Vertical” menu with a variety of user-adjustable settings
- Results table shows time-correlated listing of events time-correlated with waveform view
- Integrated search with marks
- Triggering up to 6.25Gbs (Gen1 & Gen2 only)

PCIe Decoder (Opt SR-PCIe)

Decoding of PCIe Gen3 compliance pattern Tx preset encoding

Decode results show correct value of “87h” or “1000b” (as shown in Results Table) for Transmitter Preset **P8** (-3.5dB de-emphasis with +3.5dB preshoot) on Lane 0



Reference: PCI Express Base Spec, Rev 3.0 (10-NOV-2010), Section 4.2.3.2 Encoding of Presets, p.225.

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RF Switch and Auto Toggling

- Use RF switch to handle multiple lanes without reconnections
  - √ Must provide termination to maintain compliance mode
  - √ Use programmatic interface to control from automation software
  - √ While switches typically have good signal quality at 4GHz, extra cables must be accounted for by de-embedding
  - √ Design you device so that automatic toggling works for all presets

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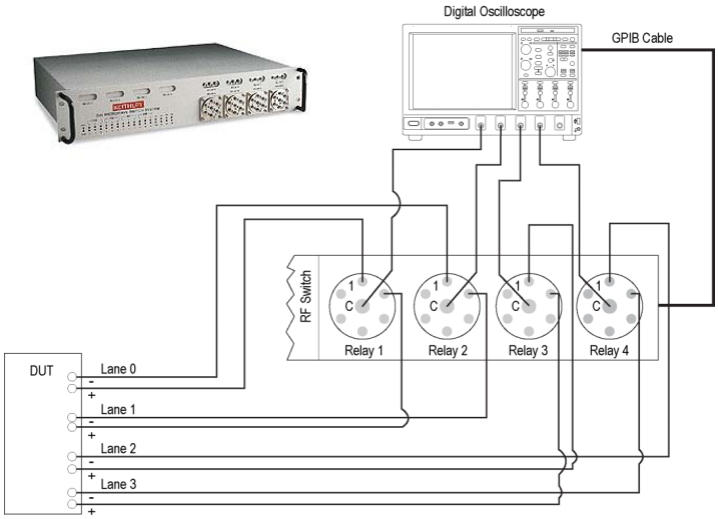
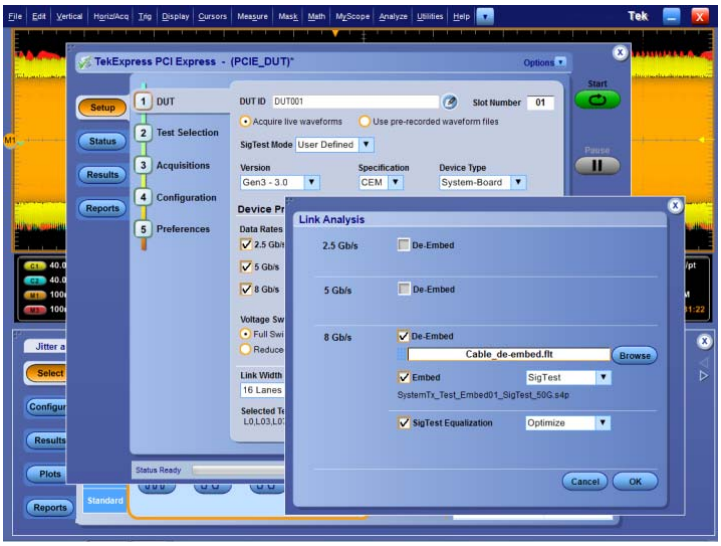
PCI Express Tx Test with RF Switch



Cable and RF Switch De-embed



Comparison of De-embedding: Add-In Card

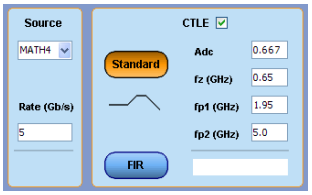
Add-In-Card (P7)	With de-embed	Without de-embed	Diff
SigTest Measurement	Switch & extra cable effects removed	Switch and cable effects present	
Max Peak to Peak Jitter	43.167ps	42.212ps	2.26%
Minimum eye width	83.028ps	83.236ps	-0.19%
Deterministic Jitter d-d	35.605ps	35.436ps	0.48%
Random Jitter	0.453ps	0.450ps	0.67%
Composit Eye height	0.110V	0.101V	8.91%
Min Transition Eye Height	0.111V	0.103V	7.77%
Min Non-transition Eye Height	0.115V	0.109V	5.50%

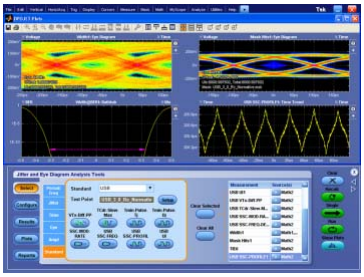
Comparison of De-embedding: System

System Board (P7)	With de-embed	Without de-embed	Diff
SigTest Measurement	Switch & extra cable effects removed	Switch and cable effects present	
Max Peak to Peak Jitter	42.614ps	41.619ps	2.39%
Minimum eye width	81.566ps	82.443ps	-1.06%
Deterministic Jitter d-d	31.261ps	31.653ps	-1.24%
Random Jitter	0.865ps	0.775ps	11.61%
Composit Eye height	0.132V	0.129V	2.33%
Min Transition Eye Height	0.165V	0.152V	8.55%
Min Non-transition Eye Height	0.141V	0.134V	5.22%

Testing Beyond Compliance

- What happens if a measurement fails Compliance ?
- Could it be the channel?
  - Measurements can be taken before the channel to evaluate results
  - Different channel models can be created using SDLA Visualizer
- How does the optimized RX setting compare to other settings?
  - Easily compare the results of multiple Equalization settings
- Does deeper analysis of the waveform need to be done?
  - PCIe specific measurements can be taken in Tektronix' measurement system DPOJET
  - Determine if data dependent, uncorrelated or pulse width jitter is in spec
  - Measurements filters and settings can be adjusted to get to root cause, but remember you must pass SigTest to be certified for compliance
- Is the TX compliant?
  - NEW PCIe 3.0 base spec measurements are available to verify Tx compliance





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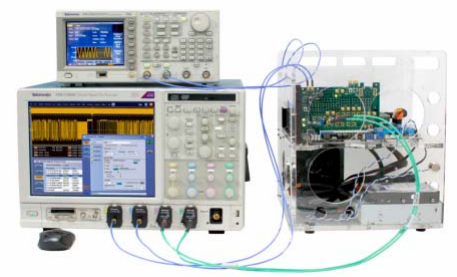
Tx Demo



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PCIe Gen3 Rx Solutions



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Essentials of Rx Testing

- PCIe 3.0 introduced formal Rx testing
- Based on stress testing of the DUT in loopback
  - Looped back data must be the same as stressed data
- DUT must support loopback initialization and **training**
- Impairments in stress must be **controlled** and **repeatable**
- DUT must receive stressed signals without errors (errors below specified ratio 10^{-12})

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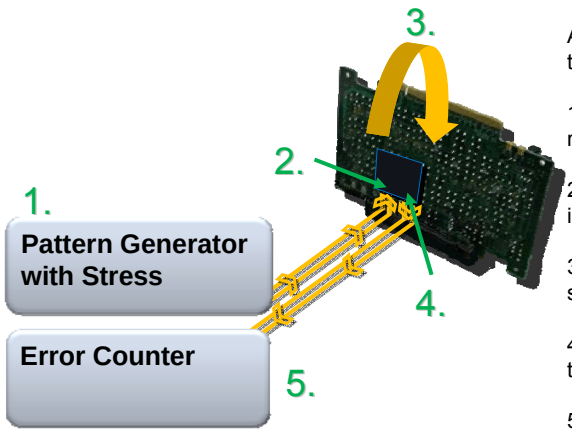
Testing Challenges in Rx

- Rx: Support of loopback
  - √ Loopback initialization
  - √ Proper training conditions
  - √ Correct stress and signal impairment levels
- How to achieve required confidence level and beyond?
  - √ Length of test (Rx)

Basic Receiver Testing



At the simplest level, receiver testing is composed of:

1.Send impaired signal to the receiver under test

2.The receiver decides whether the incoming bits are a one or a zero

3.The chip loops back the bit stream to the transmitter

4.The transmitter sends out exactly the bits it received

5.An error counter compares the bits to the expected signal and looks for mistakes (errors)

PCIe 3.0 Stress Recipe

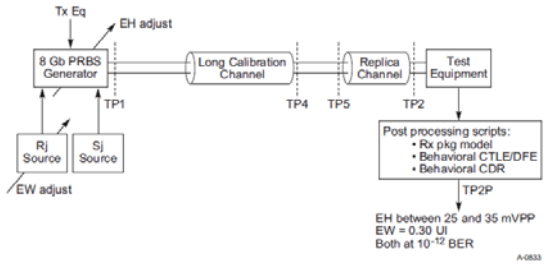


Figure 4-73: Layout for Calibrating the Stressed Jitter Eye

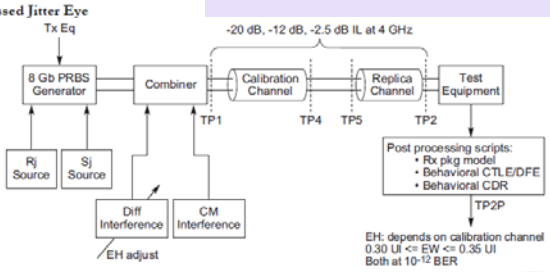


Figure 4-71: Setup for Calibrating the Stressed Voltage Eye

*From PCI Express Base Spec

Test Setup and Results

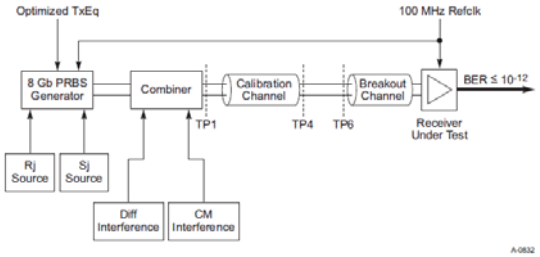


Figure 4-72: Layout for Stressed Voltage Testing of Receiver

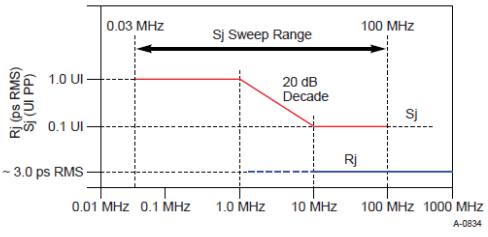
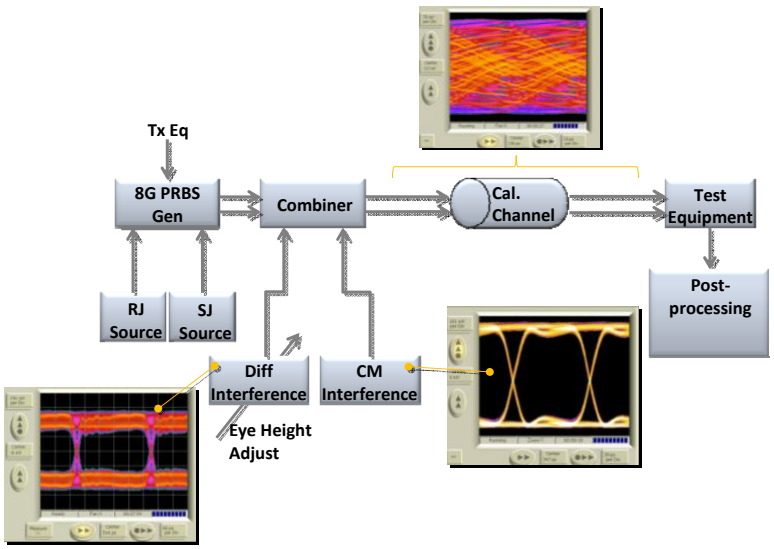


Figure 4-74: Swept Sj Mask

*From PCI Express Base Spec

Stress Composition



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Components of a PCIe3 Receiver Test Solution

- BERTScope C Model
  - PG, stressed eye sources, ED
- New! DPP125C Option ECM
  - Eye opener, Clock doubler/Multiplier
- New! BSAITS125
  - CM/DM interference
  - ISI for Gen2 & Gen3
  - Option EXP for variable ISI
- New! CR125A Opt PCIE8G
  - PLL analysis for Gen1/2/3
    - New! BSAPCI3 SW
  - Auto calibration, Link training, and test
- Cables, adapters, compliance boards
- DSA/DPO/MSO70K Series Oscilloscope
  - Stressed Eye Calibration

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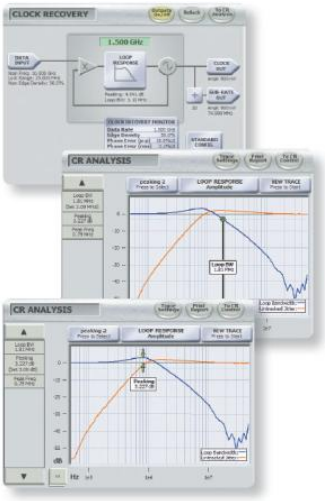
DPP125C with Option ECM

- Integrated reference clock multiplication to PCIe compliant 2.5 GHz, 5 GHz, and 8 GHz.
- Integrated eye opener functionality for testing DUTs with long channels.
- New microcontroller to provide more processing power.
- RS-232 interface enhancement to speed-up PCIe receiver equalization link training.
- SW to accommodate channel de-embedding and ISI fine adjustments.

BSAITS125 Interference Test Set

- Programmable, variable ISI for automated testing and precision setting
- Built-in compliant PCIe2 and PCIe3 Medium and Long ISI channels
- Integrated PCIe3 CM and DM interference combiner
- Integrated PCIe3 Base Spec CM interference calibration
- Continuously Variable, Expanded ISI for automated testing of multiple standards with Option EXP

CR125A Opt PCIE8G



- PLL Loop BW Analysis for Gen1/2/3
- Uses CR125A and Test SW
  - Similar to Gen1/2 PLL Loop BW solution

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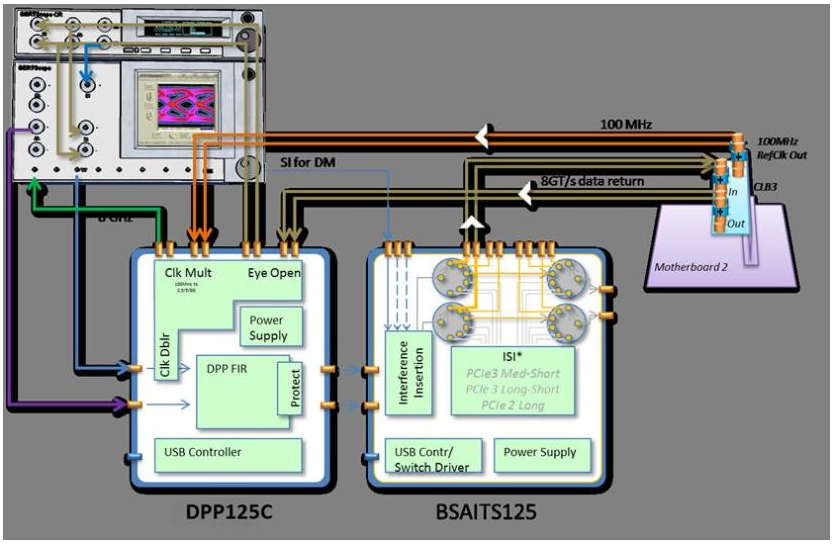
Typical PCIe3 Rx Test Configuration



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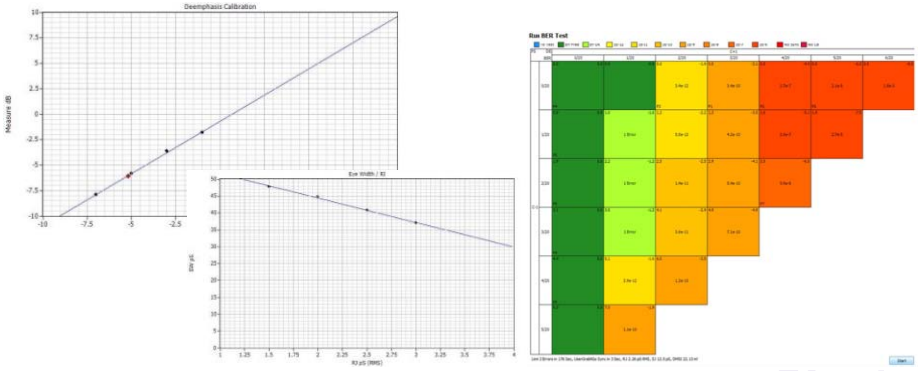
BSAPCI3 PCIe 3.0 Automation SW

- Automated calibration, link training, loopback initiation, and testing.
- BER Map feature for TxEQ optimization.
- Reduces the time and minimizes the skill-set required to perform the calibration and testing.
- Increases the reliability and accuracy by removing inconsistencies with manual calibration.



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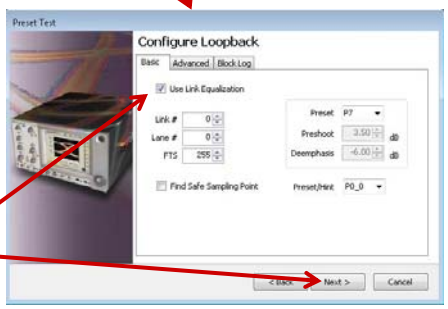
Automated Link Equalization

Figure 4-22: Main State Diagram for Link Training and Status State Machine

- State diagram from PCIe Gen3 specification
  - Implemented in Tektronix PCIe Rx test hardware and automation software



- Set-up for loopback initiation with automated link equalization
  - Step 1: select “use link eq.”
  - Step 2: initiate loopback

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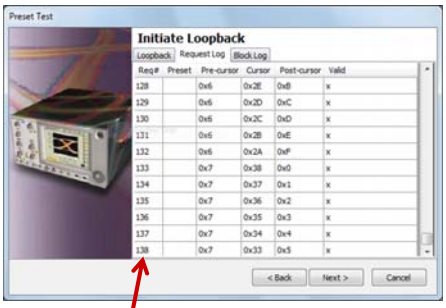
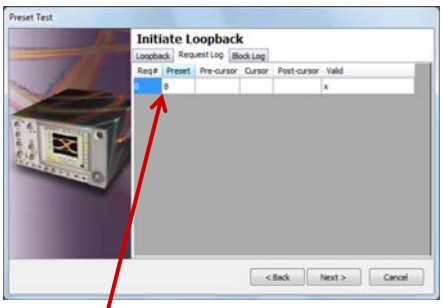
Automated Link Equalization

- Loopback results: automation software provides complete equalization request log



- DUT 1 makes many equalization setting requests



- DUT 2 requests only one equalization preset

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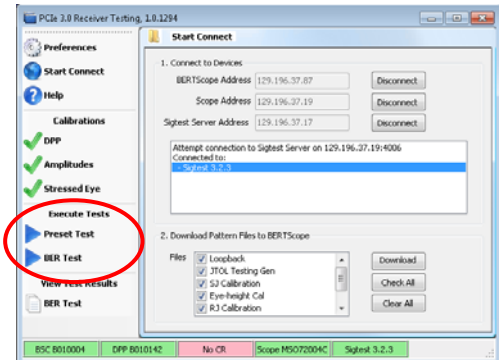
Automation test options

- Automation software provides two options for testing:
  1. "Preset test" uses either negotiated link equalization or user selected preset for test
  2. "BER test" provides the option to test a matrix of preshoot and de-emphasis settings



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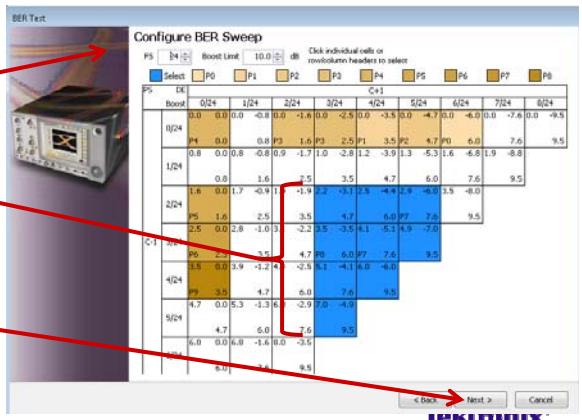
Automated Tx equalization matrix testing

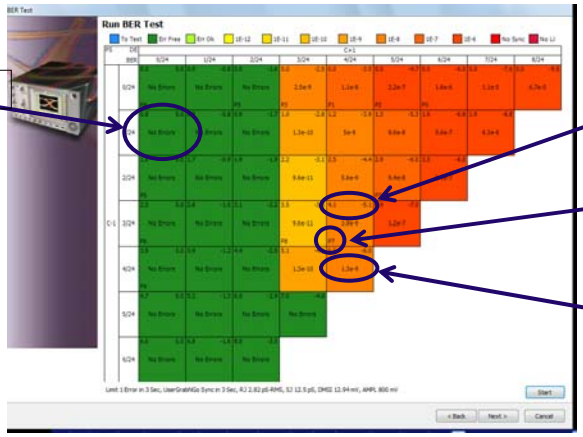
- Automation software “BER test” provides the option to sweep a matrix of pre-shoot and de-emphasis settings
  - Quickly find the range of values that work well with the DUT
  - Ideal for debugging purposes

- Select test matrix resolution
- Click on equalization combinations desired for test
- Initiate test



Automated Equalization Sweep testing

- BER results matrix for preshoot and de-emphasis settings provides an in-depth view of Rx sensitivity to Tx equalization



Green = pass

Preshoot and de-emphasis setting

Equivalent preset number

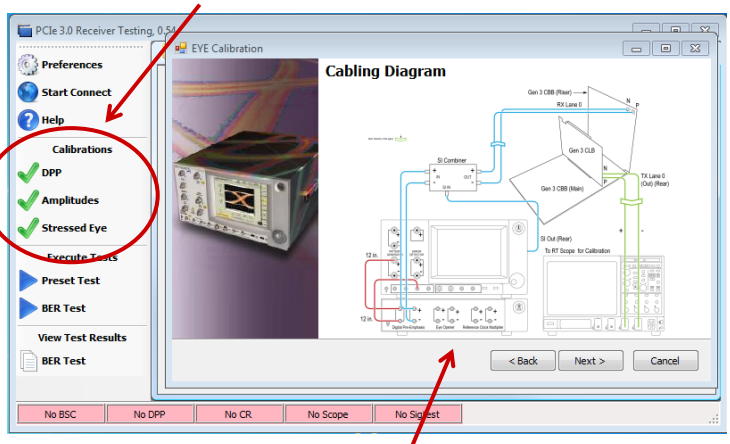
BER result for each combination of preshoot and de-emphasis

Automatic Calibration

- Due to complex test setup and variations in DUTs and test equipment just dialing up the settings on the signal source is not sufficient
- Stress must be measured and adjusted
- Automatic calibration is used to achieve the right amount of stress
- Margin testing complements the compliance testing
  - Help understand your device's margins.
  - How much additional stress does it tolerate?

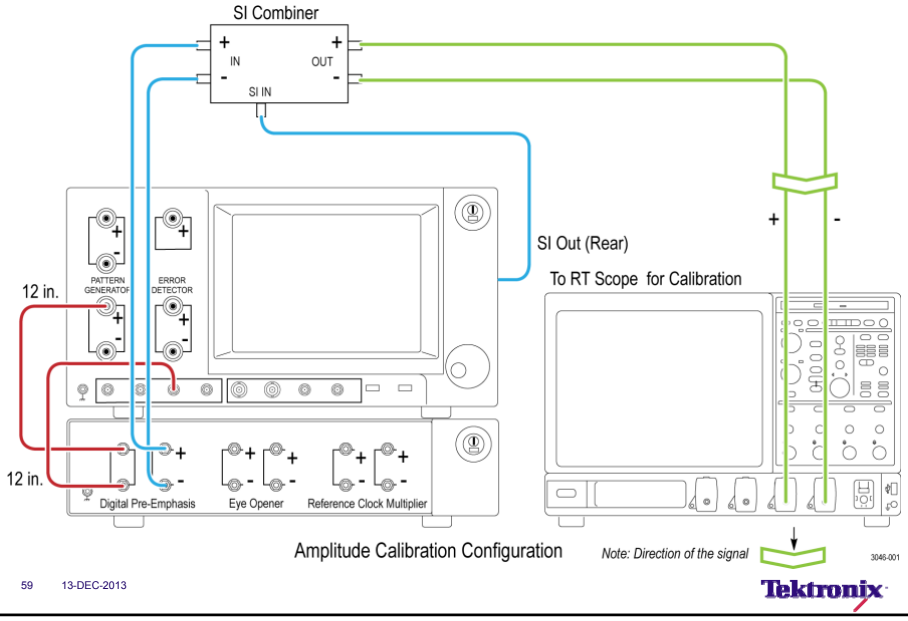
Stressed Eye Calibration Setup

- Three required calibrations are fully automated



- Detailed cabling diagrams are provided for each calibration step

Amplitude Calibration Configuration



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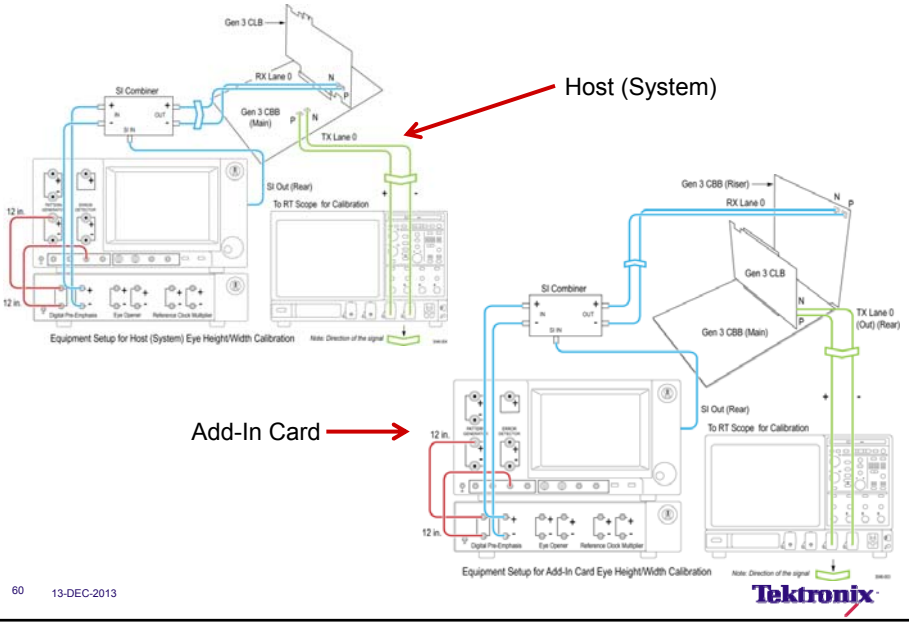
Eye Height/Width Calibration Connections



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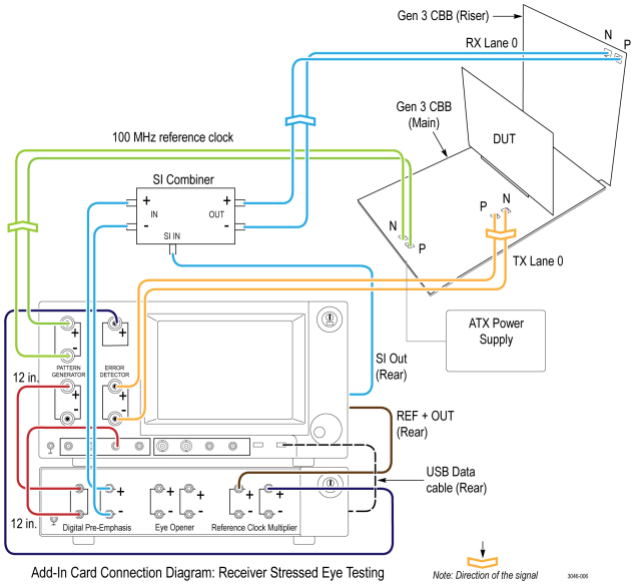
Add-In Card: Receiver Stressed Eye Testing



Add-In Card Connection Diagram: Receiver Stressed Eye Testing

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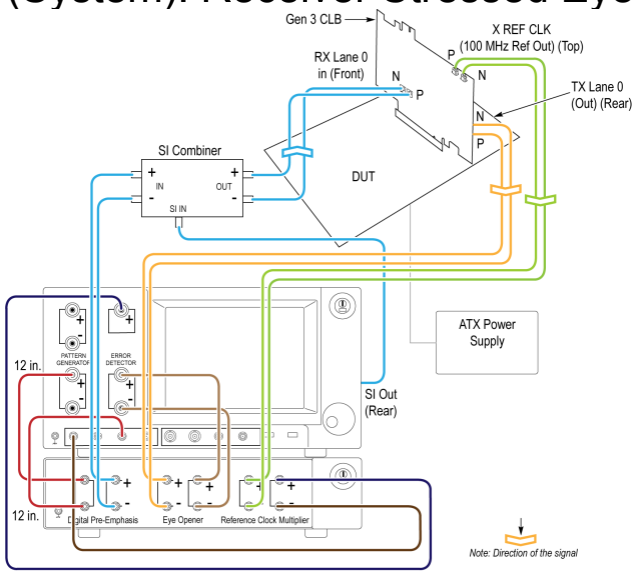
Host (System): Receiver Stressed Eye Testing



Equipment (Host) Connection Diagram: Receiver Stressed Eye Testing

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Rx Testing Summary

- Certainly the most complex type of testing
  - Due to complexity of equipment and procedures
- Extensive correlation studies in PCI-SIG have helped to streamline solutions
  - Similar stress signals
  - Guided calibration and test execution
  - Good correlation on the latest workshop
- Link Equalization detail and BER test matrix go beyond compliance testing and give visibility into DUT behavior and margins
- Successful Rx compliance and margin test gives you the confidence that the device passes when you get to the workshop

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Tx PLL Loop Bandwidth & Peaking

	2.5 GT/s	5 GT/s [1]		8 GT/s	
Loop Bandwidth (MHz)	1.5 – 22	8 - 16	5 - 16	2 – 4	4 – 5
Peaking (db)	0 - 3	0 – 3	0 - 1	0 – 2	0 -1
		[1] - PLL Test software implementation is 5-8 MHz LBW, allowed 0 – 1 dB peaking. Above 8 MHz LBW, allowed 0 – 3 dB peaking			

Excerpt from PCIe Base Specification 3.0 detailing Tx PLL requirements

4.3.3.12. Transmitter PLL Bandwidth and Peaking

4.3.3.12.1. 2.5 GT/s and 5.0 GT/s Tx PLL Bandwidth and Peaking

PLL bandwidth and peaking are defined for both the Transmitter and Receiver in order to place an upper limit on the amount of Refclk jitter that is propagated to the transmitted data and to the CDR. Defining PLL BW and peaking limits also guarantees a minimum degree of Tx/Rx jitter tracking in those systems utilizing a common Refclk Rx architecture.

Two sets of bandwidth and peaking are defined for 5.0 GT/s: 8-16 MHz with 3 dB of peaking and 5-16 MHz with 1 dB of peaking. This gives the designer the option of trading off between a low peaking PLL design vs. a low bandwidth design. For 2.5 GT/s, a single PLL bandwidth and peaking range is specified at 1.5-22 MHz with 3.0 dB of peaking.

4.3.3.12.2. 8.0 GT/s Tx PLL Bandwidth and Peaking

The Tx and Rx PLL bandwidth for 8.0 GT/s signaling is 2 – 5 MHz. Peaking may be from 0 to 2 dB for bandwidths up to 4 MHz and 0 to 1 dB for bandwidths up to 5 MHz. The 8.0 GT/s PLL BW range is substantially lower than the PLL bandwidths specified for 5.0 GT/s or 2.5 GT/s operation to reduce the amount of Refclk jitter at the sample latch of the receiver.

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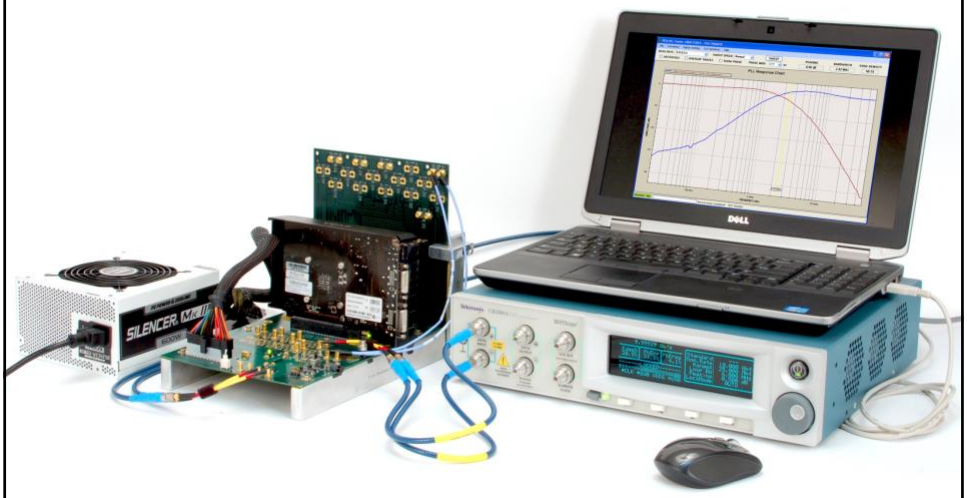
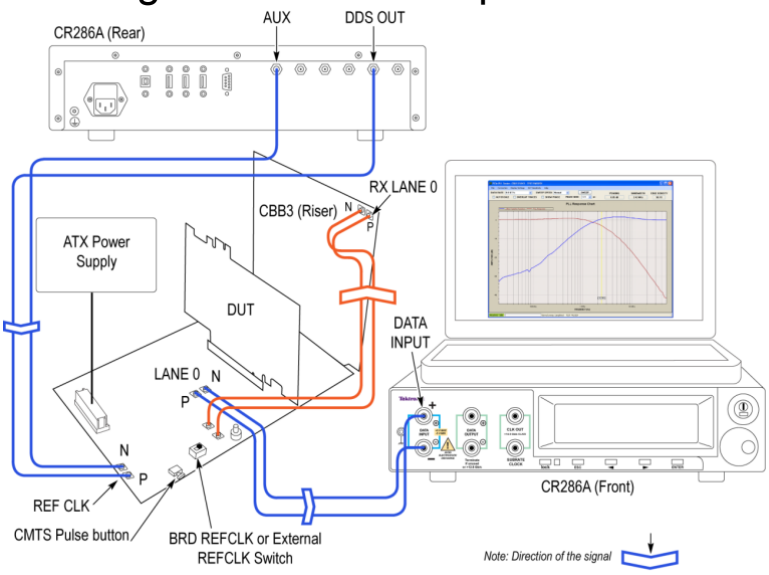
Effective Instrument for PLL Testing

- For PLL testing use a setup that requires single instrument
- The method is based on modulating the 100MHz reference clock and measuring the bandwidth with clock recovery unit.
- The limits for bandwidth are 2-4MHz with 2dB peaking
  - If BW 4-5MHz, peaking must remain under 1dB

PLL Testing with CRU



PLL Testing with CRU - Setup



A **CBB2** can be used instead where the PCIe 2.0 compliance toggle circuit creates a 1ms duration pulse of a 100 MHz refclk directly into the RX0 lane of the DUT to generate the stimulus to switch signal speed and/or de-emphasis levels, without the need for the two (2) 12" orange cables shown in the **CBB3** diagram above.

0850-004

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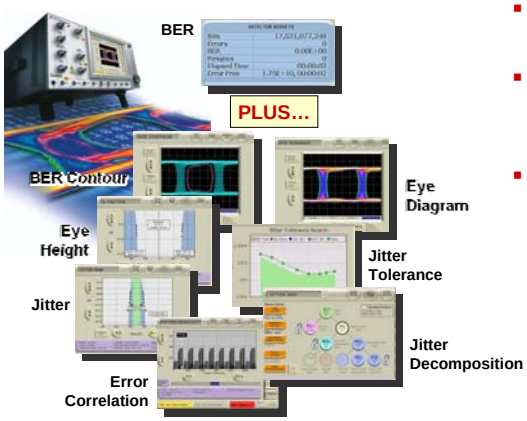
Beyond Compliance: BERTScope Analysis Tools

- Besides being a BERT, the BERTScope's **"Scope" functionality** brings benefits that complement those of the Tektronix scopes
- Analysis tools are full featured and easy to use



- Frees up the scope for other tasks
- **Eye diagram for quick diagnosis** of synchronization and BER failure issues
- **Debug** challenging **signal integrity problems**
  - Error Location Analysis
  - Pattern Capture
  - Jitter Map
  - BER Contour

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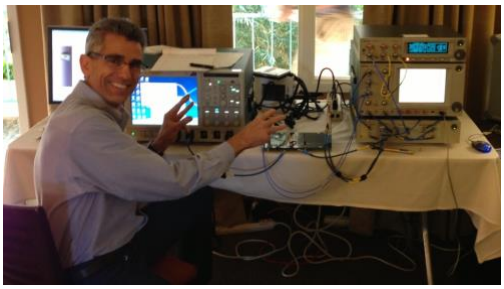
Rx
Demo



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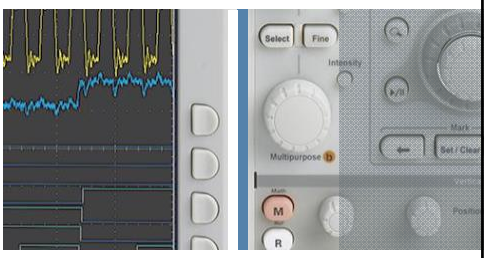
PCIe 3.0 Protocol Solutions

Supplemental



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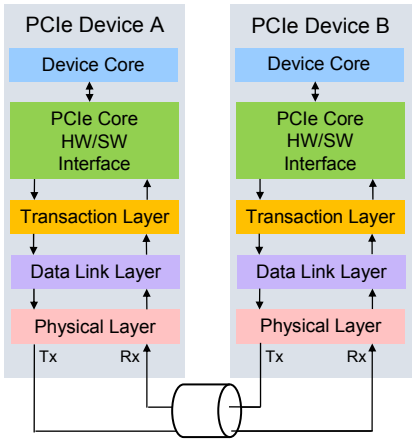
Testing Challenges with PCI Express 3.0



Transaction Layer

- Creates Request/Completion Transactions
- Messaging
- TLP Flow Control

Data Link Layer

- Flow control information
- Data Integrity, Error Checking/Correction
- Calculates/Check TLP Sequence Number
- Initialization – DLLP

Physical Layer – Logical Sub Block

- Link Initialization and Training
- Distribution of packet information over multiple lanes
- Power management and link power state transitions

Physical Layer – Electrical Sub Block

- Transmitter Signal Quality and Ref Clock Testing
- Receiver Testing
- Interconnect Testing
- PLL Loop BW
- TX/RX equalization
- Faster Bit Rates
- Separate Jitter Budget

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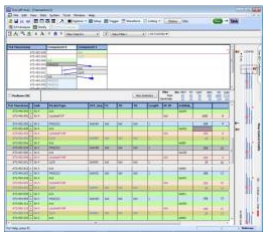
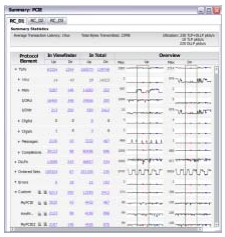
Logic Protocol Analyzer for PCI Express

TLA7SA00 Series supporting PCIe Gen 1 through Gen 3, Protocol through Physical layer





- Information Density for Rapid Analysis
  - Transaction Window with BEV Flow control
  - Summary Profile Window
  - Lane-by-Lane decode with Listing Window
- Shortened Time to Confidence
  - Front panel status LEDs
  - Auto Configure capability
- Powerful Triggering and Filtering
  - Trigger on Events from Physical to Protocol
  - Real-time Filtering
- Recognized Probing Leadership
  - Probe anywhere on the bus using OpenEYE technology
  - Flexible probing solutions including legacy probe support
  - ScopePHY provides PHY layer access to oscilloscope through LPA probes
  - Link Tracking including superior ASPM support with FastSYNC
- Multi Bus visibility for system level debug
  - Support multiple PCIe links used in switch or bridge applications
  - Cross Bus correlation/triggering
  - DDR, QPI, DMI, PCIe & others
- Accelerated Time to Actionable Information
  - <20 mins from setup to ready for Acquisition
  - Immediate visibility of data at any depth
  - HW Accelerated search and data displays

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PCI Express Protocol Test Solution

Software

- Module setup & trigger
- PCIe decoders
- Data windows:
  - Summary Profile
  - Transaction with BEV Flow control
  - Listing
  - Waveform

Modules

- 8, 5, 2.5 GTs
- x8 & x4
- 8 State Triggering
- 8 GB memory
  - 16 GB for x16
- OpenEYE
- FastSYNC

Probes

- x8 & x4 midbus
- x16, x8, x4, x1 slot interposers with Lane Converters
- Solder-down probe
- Gen2 probes for x8 & x4 midbus footprints rated to 5 GTs
- All probes rated to 8 GTs
- 6' probe cables
- ScopePHY

Mainframes

- 2 module portable mainframe with integrated 15" display & PC controller
- 6 module benchtop with GbE controller (requires PC)
- Single GUI & frame for system level debug of multi-buses

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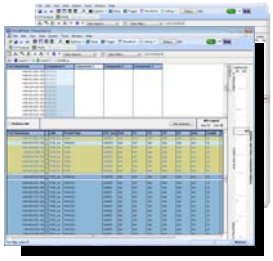
Time to Actionable Information



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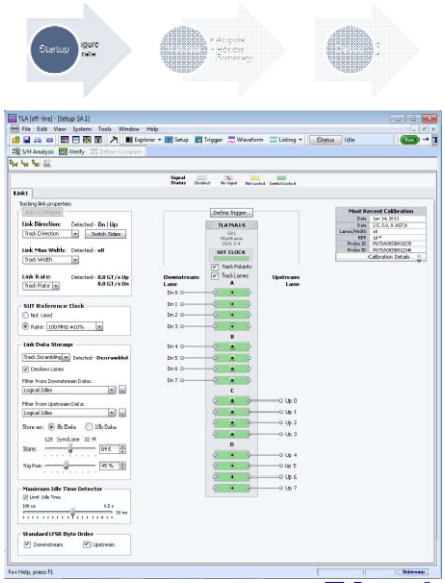
Startup

Configure and Calibrate your system

- On start up of new system, LPA application displays module Setup screen by default
- Signal integrity and link health issues are immediately apparent from onscreen indicators
- Calibration results are remembered for module/probe sets from one session to another



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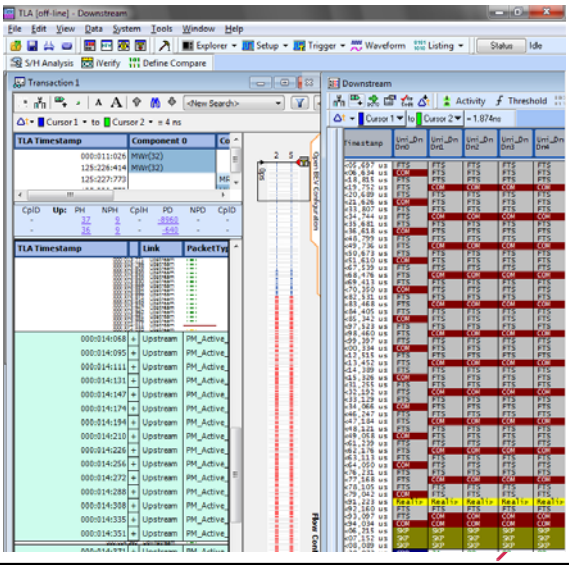
Validate

Acquire and Review Summary

- Automatic display of Transaction Window with Listing Window
- Errors with timestamps and link direction
- Expanded Training sets with all of the TS data
- Default columns in Listing window



Debug

Analyze / Explore - Visibility across entire acquisition

- Flow Control analysis shows buffer overflows across entire acquisition
- Summary statistics hyperlink to 1st instance of credit value
- Allow user defined combination of credits:
  - All credits can be individually selected or combined with any other credits
  - Up and Down directions can be separated or combined
  - *Multiple links can be combined or isolated*

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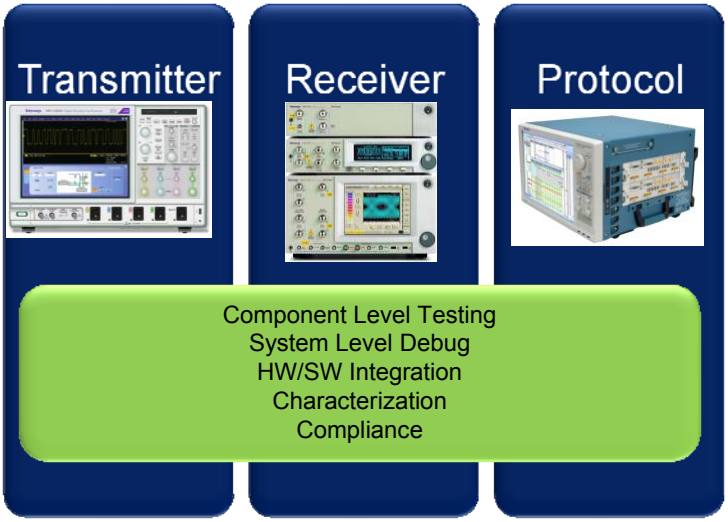
Comprehensive PCI Express Solution



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Thank You!

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Enabling Innovation

PCI Express 3.0 Trends and Implications

Industry/Technology Trends

- 8GB/s using the same board material (FR4) and connectors results in increased channel loss
- Probing access at the silicon transmitter pins is typically not available
- Receiver equalization can only compensate for channel loss
- Receiver Testing is a requirement and is critical to ensure system interoperability
- Energy efficiency (Lower mW/Gb/s)

Implications

- Link Analysis, de-embedding, embedding and RX equalization is required post process
- Closed data eyes requiring new techniques for transmitter and receiver equalization
- Higher data rate signals have less margin – requires de-embedding for base specification measurements
- New Jitter Separation Measurements are required
- Back channel negotiation to equalize the receiver
- Link training and power management continue to be the most difficult logic layer challenges

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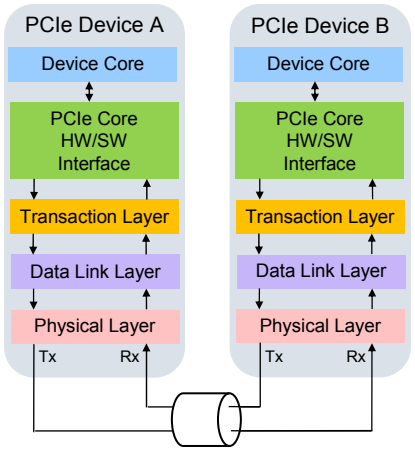
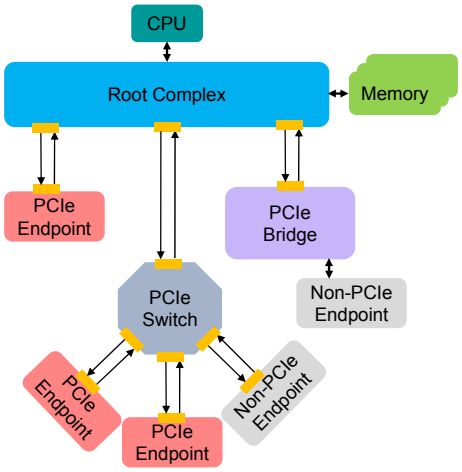
PCI Express Architecture & Terminology



Link Width	# Lanes	# Differential Pairs	# Wires
x1	1	2	4
x4	4	8	16
x8	8	16	32
x16	16	32	64

Lane = Two (2) differential pairs (4 wires): one Tx & one Rx
Link = Connection between two ports & their interconnecting lanes



Root Complex = Head or root of the connection of the I/O system to the CPU & memory
Endpoint = Device that can request/complete PCIe transactions for itself
Switch = Device used to fan out a PCIe hierarchy
Bridge = Device that has one PCIe port and one or multiple non-PCIe endpoints

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Base Specification vs. CEM Test Philosophies

- CEM Testing is primarily focused on Compliance
  - Ensure Interoperability of Systems (Root Complex) and Add-In Cards (Endpoints)
  - Pass/Fail
  - Margin Testing mainly to verify manufacturability
- Base Specification Testing is generally focused on Characterization
  - Verify chip performance across a wide range of operating conditions
    - Voltage, Temperature, Eye Height, Eye Width, Equalization, etc.
  - Margining is Key
    - Increase OEM's latitude in choice of backplane material and PCB layout
    - Reduce system power requirements and thermal footprint

NOTE: PHY Test Specification for PCIe 3 is analogous to CEM Specifications from previous generations of PCIe

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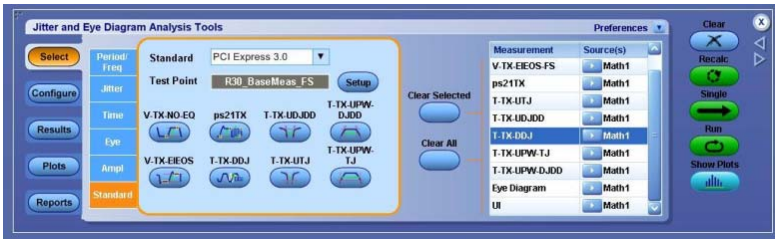
PCI Express Base Specification Measurements



- Voltage
- Package Loss
- Transmitter Equalization
- Jitter

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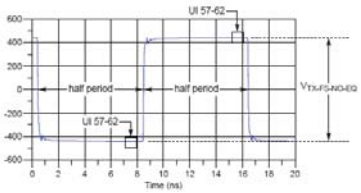
Transmitter Equalization Measurements VTX-BOOST-FS / VTX-BOOST-RS

- What's new for Gen 3.0
  - De-Emphasis (Va) and pre-shoot (Vc)
  - Transmitters must support 11TX equalization pre-sets
- The high frequency nature of 8.0 GT/s signaling makes measurement of single UI pulse heights impractical due to attenuation by the package and breakout channel
  - Amplitude measurements are taken on low frequency waveforms (64 ones/ 64 zeros in the compliance pattern) using last few UI of each half period
  - Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Preset Number	Preshoot (dB)	De-emphasis (dB)
P4	0.0	0.0
P1	0.0	-3.5 ± 1 dB
P0	0.0	-6.0 ± 1.5 dB
P9	3.5 ± 1 dB	0.0
P8	3.5 ± 1 dB	-3.5 ± 1 dB
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB
P5	1.9 ± 1 dB	0.0
P6	2.5 ± 1 dB	0.0
P3	0.0	-2.5 ± 1 dB
P2	0.0	-4.4 ± 1.5 dB
P10	0.0	See Note 2.

Preset Number	De-emphasis (dB) $20\log_{10}(Vb(i)/Vb(j))$	Preshoot (dB) $20\log_{10}(Vb(i)/Vb(j))$
P4	N/A	N/A
P1	P1/P4	N/A
P0	P0/P4	N/A
P9	N/A	P4/P9
P8	P8/P6	P3/P8
P7	P7/P5	P2/P7
P5	N/A	P4/P5
P6	N/A	P4/P6
P3	P3/P4	N/A
P2	P2/P4	N/A
P10	P10/P4	N/A

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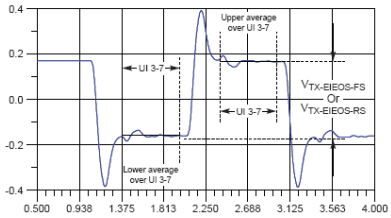
Transmitter Voltage Measurements
VTX-EIEOS-FS / VTX-EIEOS-RS

- Launch Voltage of Electrical Idle Exit Ordered Set
- Required to ensure that the RX can properly detect an exit from electrical idle
- Taken on a pattern of eight ones followed by eight zeros repeated 128 times included in the compliance pattern
  - Taken on the middle five UI to reduce attenuation effects of the channel
- VTX-EIEOS-FS - Full Swing Signaling
  - Measured by Preset 10
- VTX-EIEOS-RS – Reduced Swing Signaling
  - Measured by Preset 1



$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 (min)	mVPP
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232 (min)	mVPP

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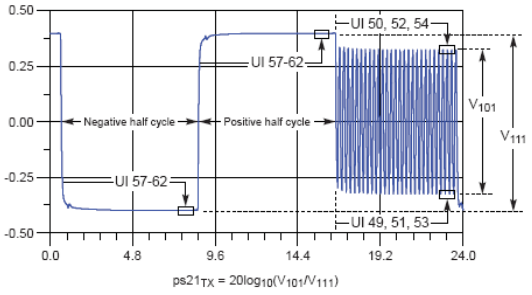
Package Loss Measurements
PS21

- Can be taken at TP1 while capturing silicon package loss and drive characteristics, but due to the high frequency content of the 1010 pattern the measurement must be de-embedded back to the TX pins
- Measured by comparing 64 zeros and 64 ones PP voltage against a 1010 pattern
- Measured with de-emphasis and pre-shoot set to 0 at the end of each interval to minimize ISI and low frequency effects



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Transmitter Jitter Measurements

- Necessary to take transmitter jitter measurements with all lanes operating in order to capture crosstalk effects
- Measurements are taken at TP1 and de-embedded back to the pins of the TX
- Necessary to separate uncorrelated and data dependent jitter in order to ensure that jitter that can be recovered is not budgeted as uncorrelated jitter

Jitter Measurements	Data Dependent Jitter	Uncorrelated Jitter
Cause	Due to package loss and reflections (dynamics in the channel, ISI)	Uncorrelated - PLL jitter, crosstalk, noise conversion (amplitude to phase)
How to Compensate	Can be reduced by equalization	Difficult to remove (better components, layout)

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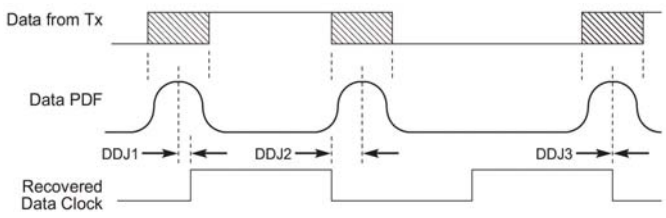
Transmitter Jitter Measurements: Data Dependent Jitter TTX-DDJ

DDJ Measurement Process

T_{TX-DDJ}	Data dependent jitter	18 (max)	ps PP

- Measurement taken on multiple repeats of the compliance pattern using a 1st order CDR function representing a high pass filter
- A PDF is created for each edge crossing of the compliance pattern
- DDJ is calculated as the difference of the mean of each PDF and the recovered clock edge
- Measurement is defined as the absolute value of DDJ(max) – DDJ(min)



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Uncorrelated Jitter Example
TTX-UTJ / TTX-UDJDD

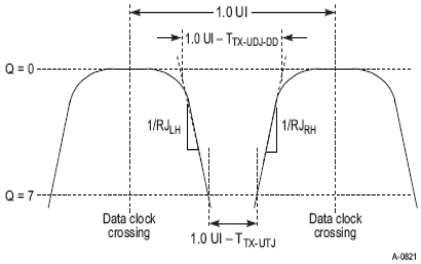
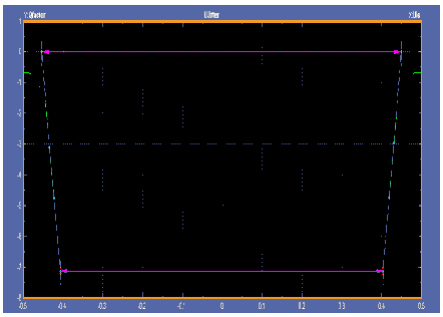


Figure 4-53: Derivation of T_{TX-UTJ} and $T_{TX-UDJDD}$



- DDJ is removed from the PDF of each edge
- Data is converted to Q-Scale
- Uncorrelated Deterministic Jitter Dual Dirac (UDJDD)
  - Accounts for Periodic Jitter and Crosstalk Convert the PDF to Q-Scale
- Random Jitter is implied by subtracting UDJDD from UTJ

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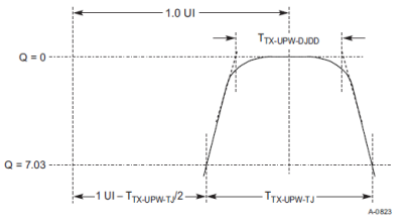
Uncorrelated Total and Deterministic PWJ
TTX-UPW-TJ / TTX-UPW-DJDD

- Pulse Width Jitter
  - Addresses lone bits that are attenuated the most in lossy channel and could likely cause bit errors
- DDJ is removed to accurately quantify PWJ
- Calculate edge-to-edge jitter
- Construct Q-scale PDF curve and Extrapolate to BER = 10^{-12} (Q= 7.03) to determine Uncorrelated Pulse Width Jitter (containing F/2 or Odd/Even Jitter) and Deterministic Pulse Width Jitter
- Final measurements are calculated by looking at the left hand side of the PDF curve



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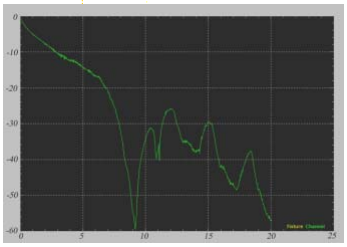
De-embedding Considerations

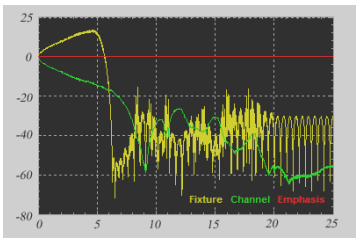
- De-embedding amplifies high frequency noise, thus requiring a bandwidth filter
  - This also impacts the required bandwidth for a RT Scope
  - Bandwidth is dependent on board material
- Successful de-embedding starts with good quality board design and S-Parameter data
  - Matched impedance, low loss structures
  - No gain, significant resonances, or large dips
- Quality of de-embedding
  - Eye height and jitter
  - Signal to Noise Ratio

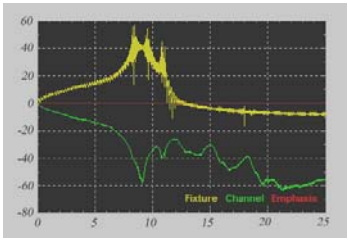
5 GHz 10 GHz



10GHz Filter -> Noise amplification

5GHz Filter





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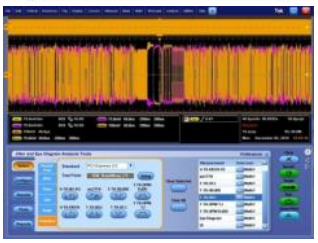
Considerations for Test Equipment Selection

- Test solutions need to go beyond compliance to enable enable root cause analysis
- Channel Embedding and Receiver equalization require new solutions that enable characterizing the optimal settings
- Solutions need to evolve as the test specifications are under development
- Tektronix has the solutions you need to begin your PCIe 3.0 testing today
  - Active participation in industry working groups enable software updates as the specification evolves
  - PCE3 is not just a compliance solution - spans multiple tasks from Compliance, Characterization, and Debug
  - Complete tools for channel modeling (embedding / de-embedding) and receiver equalization Serial Data and Link Analysis Software (SDLA)
  - New DPO/DSA/MSO70000C Series Oscilloscopes
    - Provides lower noise and jitter with 100GS/s acquisition
    - New Compute Platform reduces overall test time



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Recommended Bandwidth for PCI Express 3.0

- Balance instrument bandwidth with application requirements
  - Noise increases with bandwidth, too much bandwidth reduces the accuracy and the margin of your measurements
    - PCIe requires the analysis of signals with amplitudes as low as 34mV for compliance testing
  - Ensure enough bandwidth to capture the high frequency content of the signal
    - Need to consider how the channel effects the harmonic content and rise time of the signal
    - De-embedding requires bandwidth limit to reduce the effect of high frequency noise amplification
  - Flexibility for different tasks
    - Characterization and debug vs. compliance
- Recommended bandwidth
  - 16 GHz best balance for PCI Express 3.0 Measurements
  - Minimum: 12 GHz