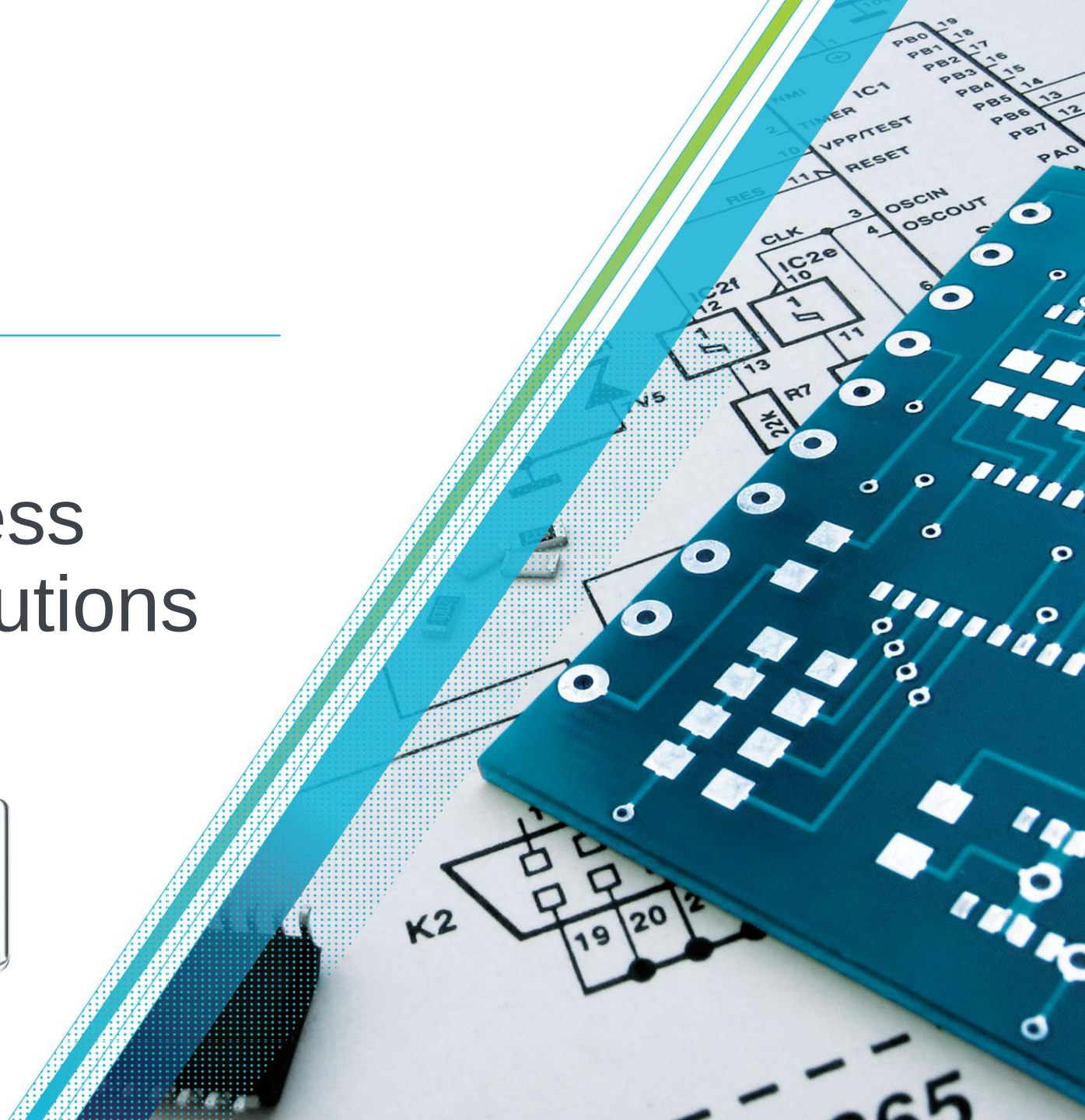
Tektronix

PCI Express Tx/Rx Solutions

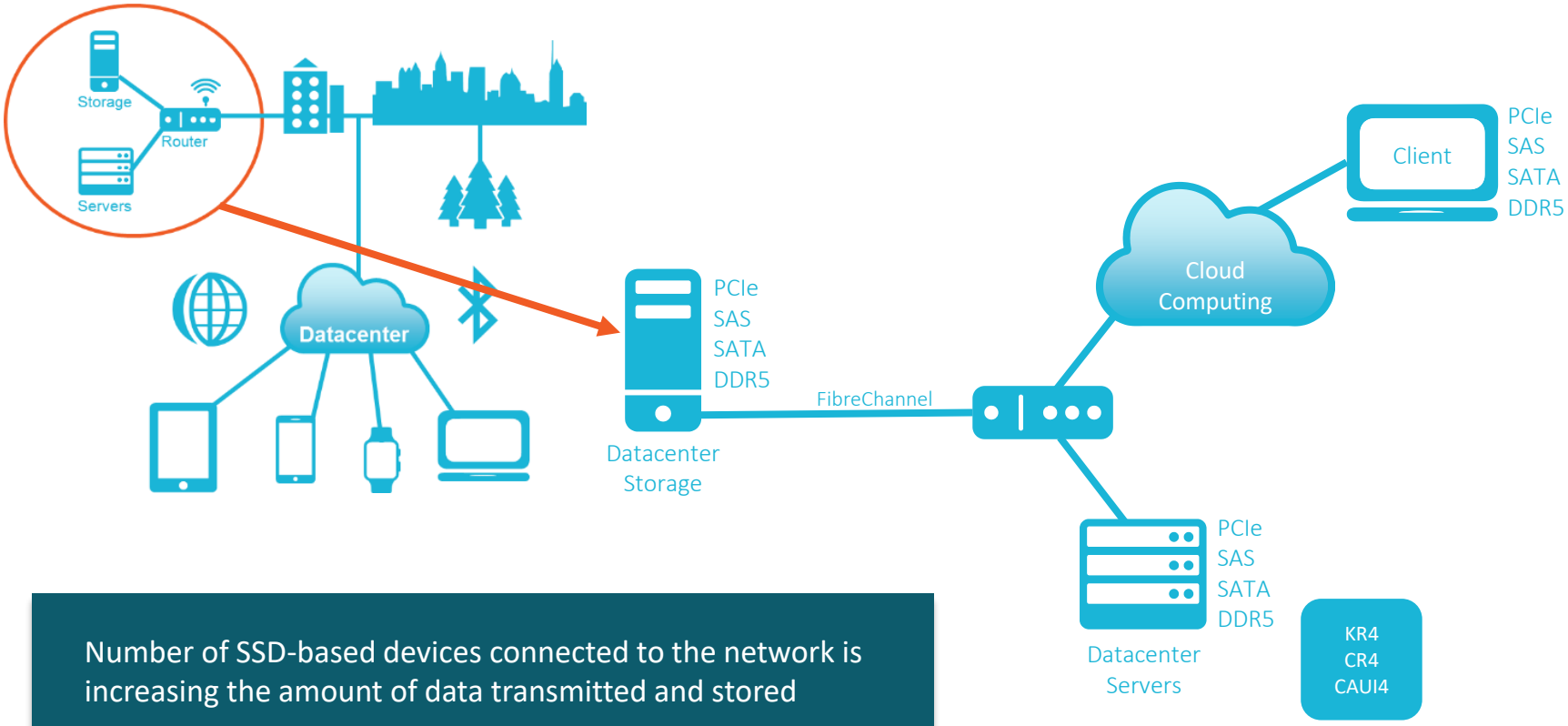


Agenda

1. Market Overview
2. Gen3 Overview
3. Gen3 Tx
4. Gen4 Overview
5. Gen4 Tx
6. Gen3 Rx
7. Gen4 Rx

Technology Overview

BIG DATA, IOT AND ANALYTICS DRIVING NEED FOR COMPUTE POWER, STORAGE CAPACITY, AND NETWORK BANDWIDTH



Number of SSD-based devices connected to the network is increasing the amount of data transmitted and stored

PCIe Market Intro

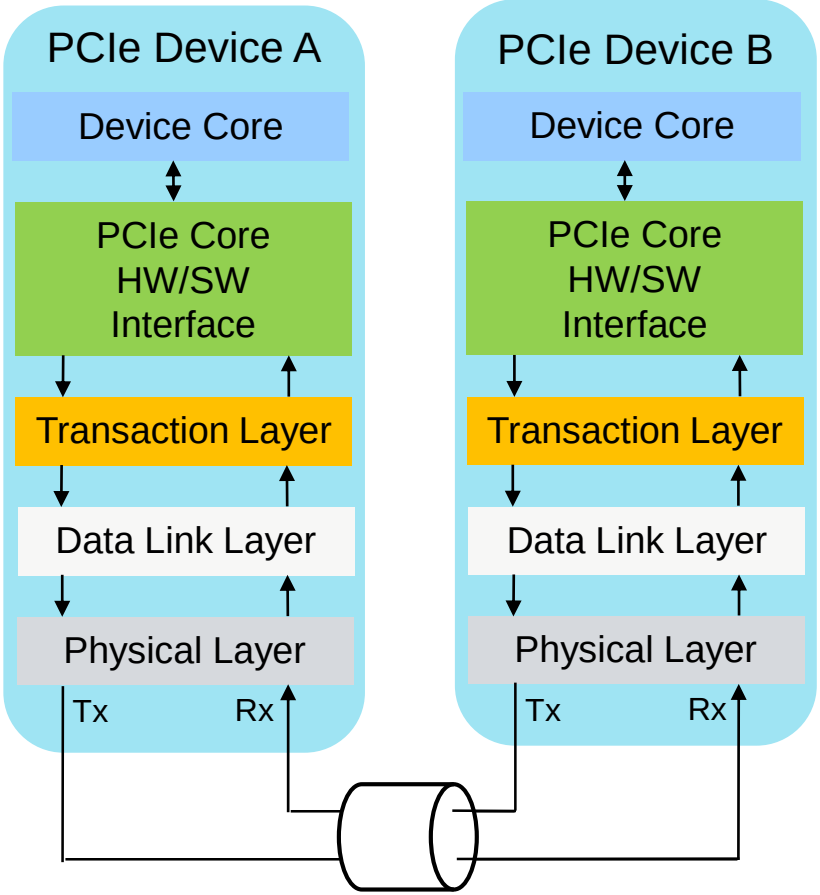
- PCI Express is a **high performance, general purpose I/O interconnect** used in a wide variety of computing & communications products. It has become especially popular for NVME SSD applications
- PCIe is based upon a **point-to-point bus topology** between a root-complex (system/host) & an end-point (add-in card) that supports full-duplex communications.
- The PCIe physical layer consists of:
  - Differential low-voltage signaling
  - **100MHz RefClk is either Common or Separate** (SRIS/SRNS)
  - **Scalable widths:** x1, x2, x4, x8, x12, x16, x32
  - **Scalable speeds**: 2.5GT/s (Gen1), 5GTs (Gen2), 8GT/s (Gen3), 16GT/s (Gen4)
  - **Utilizes connectors**, e.g., CEM, U.2 (SFF-8639), M.2 or soldered directly to PCB
- Specifications are developed & maintained by the **PCI-SIG,** a consortium of >900 companies.

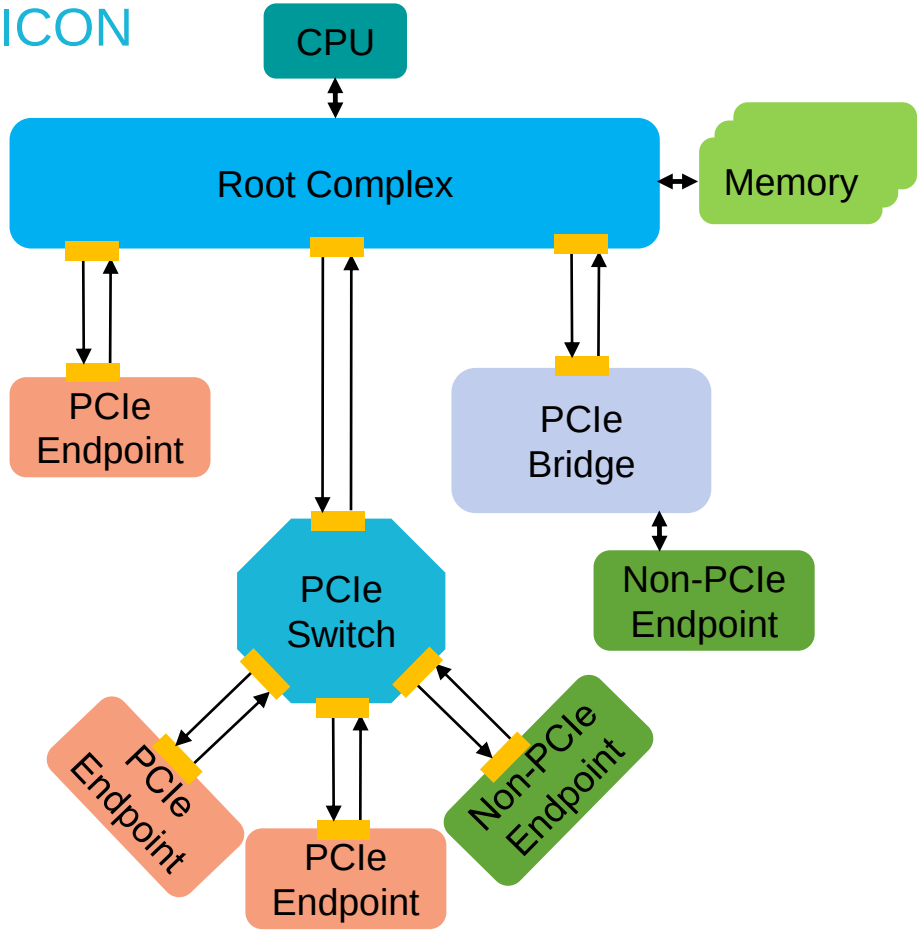
PCI Express Terminology

- Silicon
  - Referred to as “Base”
  - No compliance testing
- Form Factors
  - CEM
  - U.2 (SFF-8639)
  - M.2
- Interoperability → Compliance
  - “If you don’t own both ends of the link, then you are in the world of interoperability”
  - Compliance measurements → PCI-SIG Fixtures + SigTest (Pass/Fail only)
  - Full measurements → DPOJet + SDLA64
- Chip-to-Chip (Embedded)
  - No Interoperability → No Compliance
  - Full measurements → DPOJet + SDLA64
    - SigTest isn’t used since it is assumes PCI-SIG fixtures

PCIe Architecture and Terminology

ROOT COMPLEX vs ENDPOINT SILICON





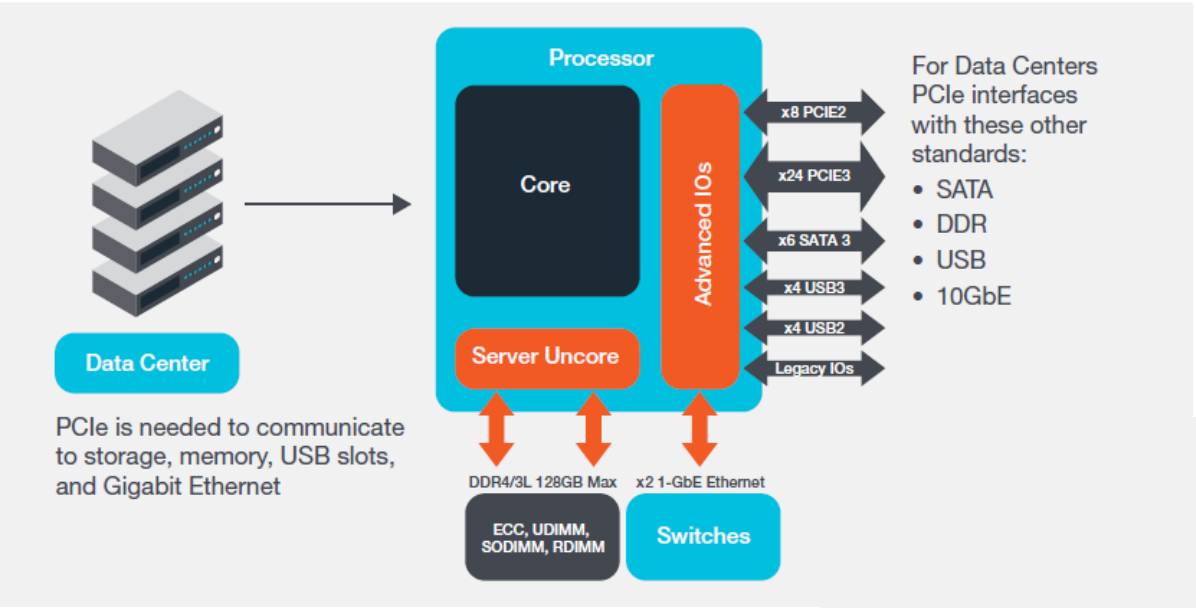
Link Width	# Lanes	# Differential Pairs	# Wires
x1	1	2	4
x4	4	8	16
x8	8	16	32
x16	16	32	64

Root Complex = Head or root of the connection of the I/O system to the CPU & memory
Endpoint = Device that can request/complete PCIe transactions for itself
Switch = Device used to fan out a PCIe hierarchy
Bridge = Device that has one PCIe port and one or multiple non-PCIe endpoints

Lane = Two (2) differential pairs (4 wires): one Tx & one Rx
Link = Connection between two ports & their interconnecting lanes

PCI Express Overview

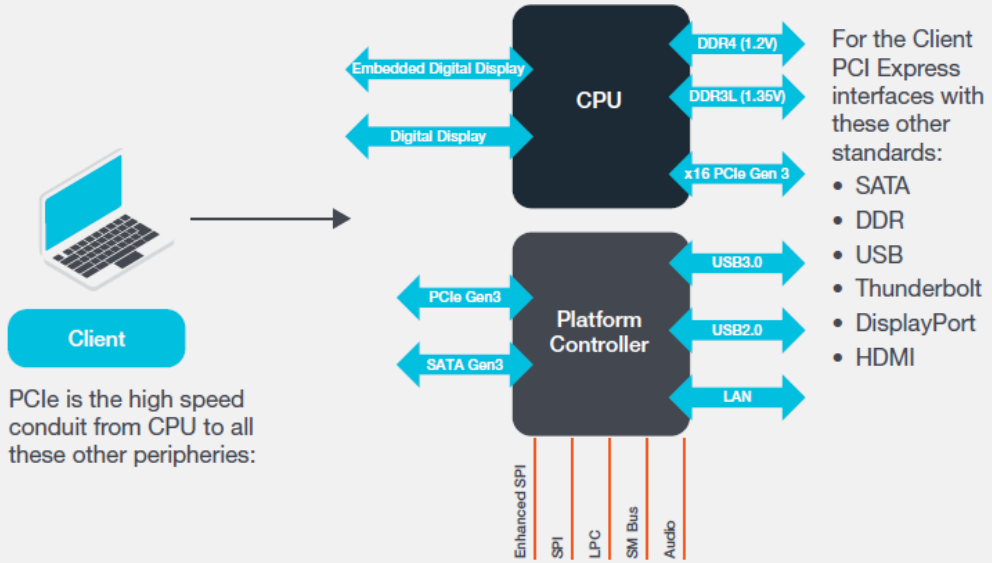
Architecture and Neighboring Technologies



PCIe is needed to communicate to storage, memory, USB slots, and Gigabit Ethernet

For Data Centers PCIe interfaces with these other standards:

- SATA
- DDR
- USB
- 10GbE



PCIe is the high speed conduit from CPU to all these other peripheries:

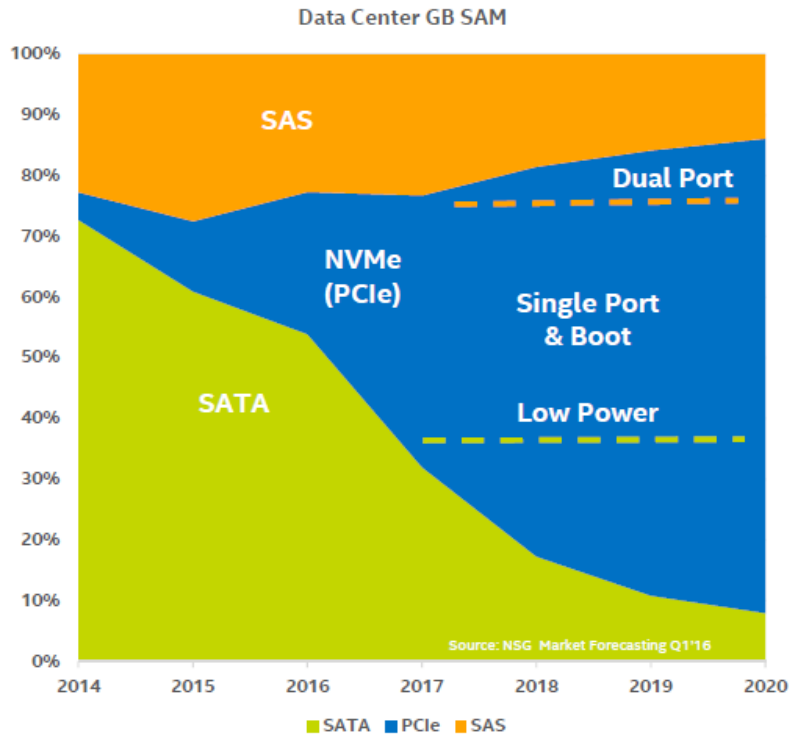
For the Client PCI Express interfaces with these other standards:

- SATA
- DDR
- USB
- Thunderbolt
- DisplayPort
- HDMI

PCI Express is emerging as the primary, high-performance storage bus and SSD Interface

PCIe SSD Forecasted to Lead in Datacenter

EXPECTED TO OVERTAKE SAS IN 2017 & SATA IN 2018

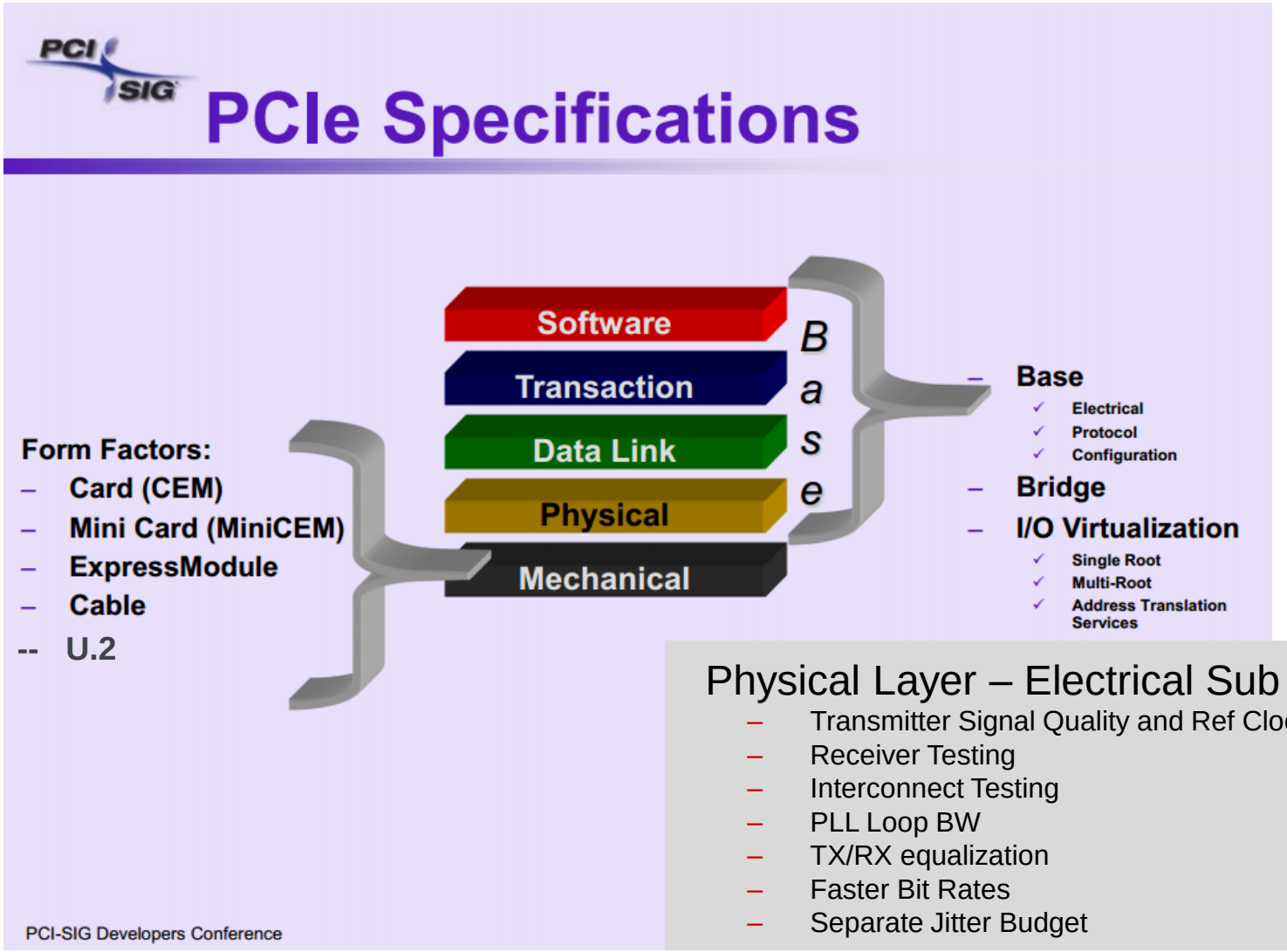


Source: Q1'16 Intel NSG Market Forecasting

- PCI Express (PCIe) projected as leading SSD interface in DC by 2017
- PCIe bandwidth is significantly higher than SATA
- NVM Express (NVMe--SW interface) has lower latency than SAS or SATA
- Increasing focus on *scalability* using protocol-driven dynamic cloud management and virtual storage--decreasing CPU overhead and improving performance

PCIe Spec Overview

PCI EXPRESS TERMINOLOGY



Physical Layer – Electrical Sub Block

- Transmitter Signal Quality and Ref Clock Testing
- Receiver Testing
- Interconnect Testing
- PLL Loop BW
- TX/RX equalization
- Faster Bit Rates
- Separate Jitter Budget

PCI-SIG DevCon June 2012, "PCI-SIG Architecture Overview"

PCI-SIG & Gen3 Specs

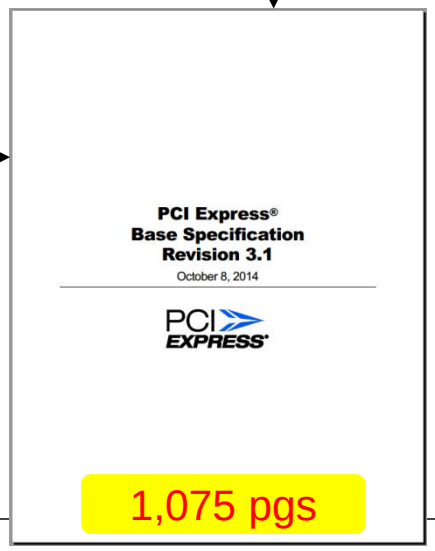
PCI Express Board of Directors

EWG
Electrical
Work Group

PWG
Protocol
Work Group

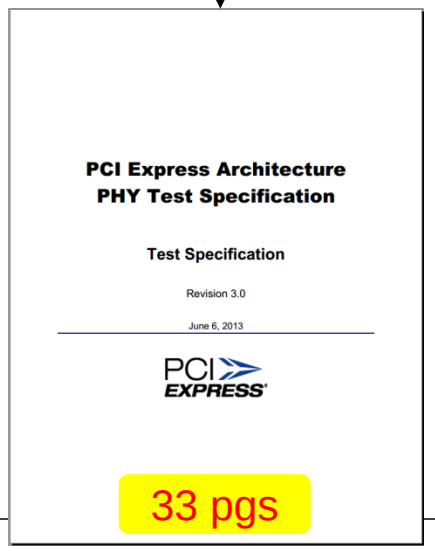
CEM
Card
Electromechanical
Work Group

SEG
Serial Enabling
Work Group



1,075 pgs

169 pgs



33 pgs

Other specs available at www.pcisig.com

PCI-SIG & Gen4 Specs

PCI Express Board of Directors

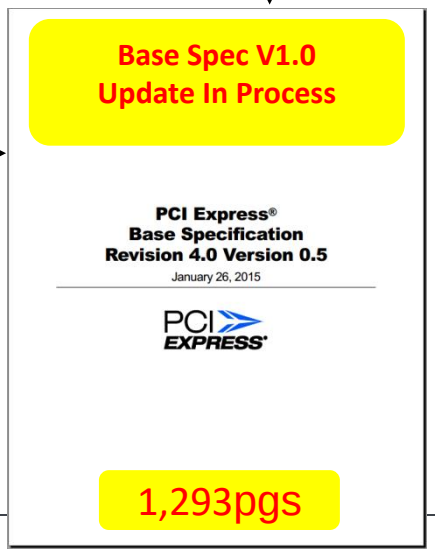
EWG
Electrical
Work Group

PWG
Protocol
Work Group

CEM
Card
Electromechanical
Work Group

SEG
Serial Enabling
Work Group

Base Spec V1.0
Update In Process



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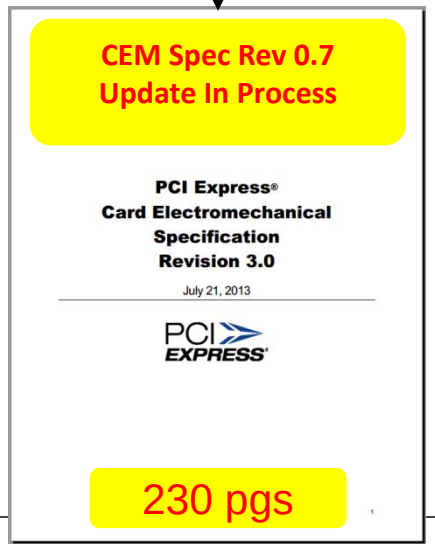
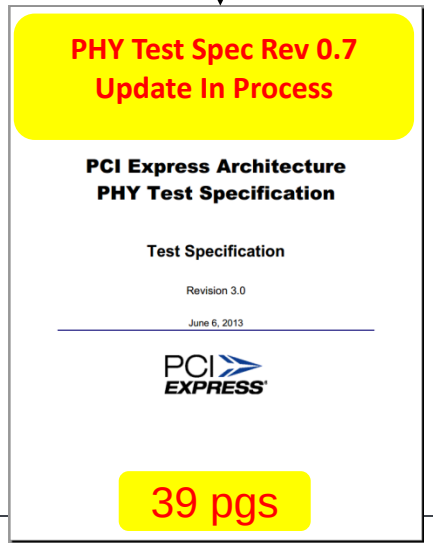
CEM Spec Rev 0.7
Update In Process



230 pgs

PHY Test Spec Rev 0.7
Update In Process



39 pgs

Other specs
available at
www.pcisig.com

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6. Gen3 Rx
7. Gen4 Rx

PCIe Compliance Testing

PCIe COMPLIANCE TESTING FOR INTEROPERABILITY

- PCIE holds regular compliance workshops/plugfests to certify individual devices' compliance and interoperability, typically 4x/yr
- Vendors who desire to be on PCI-SIG Integrator's List plan to attend PCI-SIG workshops where they must pass all four electrical tests & 80% of interoperability tests
- These vendors look at tests and test equipment and assume that if they buy & use the same equipment, they will pass the workshop electrical tests

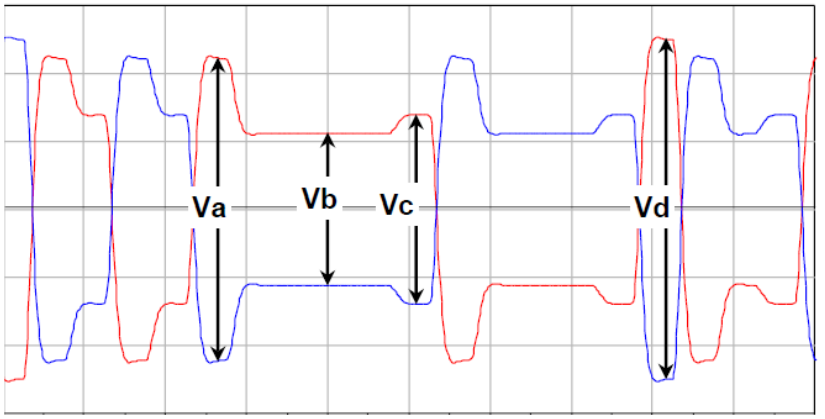
PCIE 3.0 Electrical PHY Compliance Tests
Transmitter Testing
Receiver Jitter Tolerance Testing
Tx/Rx Link Equalization Testing
PLL Loop Bandwidth Testing

For more details visit PCI Compliance program:
http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library#electrical30

Compliance Equalization Presets

- Once in compliance mode, bursts of 100 MHz clock can be used to cycle through various settings of compliance presets to perform **automated** jitter, voltage, timing measurements.
- 11 presets for both Gen3 and Gen4 (22 total). All preset values must be supported by DUT.
- For Rx AIC testing, BER < 1E-12 while receiving any valid preset/TXEQ, or < 1E-4 while receiving either P7 or P8

Preset #	Preshoot (dB)	De-emphasis (dB)
P4	0.0	0.0
P1	0.0	-3.5 ± 1 dB
P0	0.0	-6.0 ± 1.5 dB
P9	3.5 ± 1 dB	0.0
P8	3.5 ± 1 dB	-3.5 ± 1 dB
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB
P5	1.9 ± 1 dB	0.0
P6	2.5 ± 1 dB	0.0
P3	0.0	-2.5 ± 1 dB
P2	0.0	-4.4 ± 1.5 dB
P10	0.0	Variable[1]



De-emphasis = 20 $\log_{10}$Vb/Va
Preshoot = 20$\log_{10}$Vc/Vb
Boost = 20$\log_{10}$ Vd/Vb

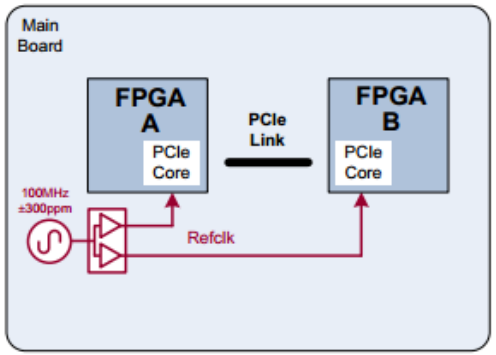
1. P10 levels are not fixed; its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used to test the boost level of the Tx during full swing

Gen3 TX Gold Suite Test Plan

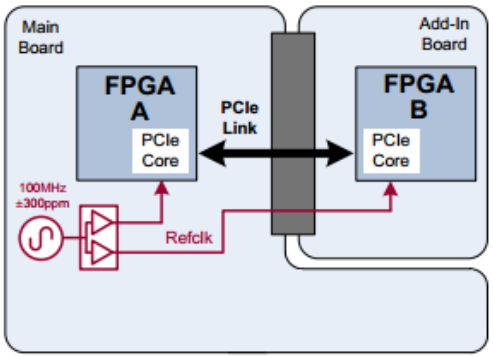
Toggle Preset	Signal Quality (Jitter, Eye) Up to the width of the port				Preset Eq
	Ln 0	Ln 3	Ln 7	Ln15	Ln 0
P0	✓	✓	✓	✓	✓
P1					✓
P2					✓
P3					✓
P4					✓
P5					✓
P6					✓
P7	✓	✓	✓	✓	✓
P8	✓	✓	✓	✓	✓
P9					✓
P10					✓
Pass condition	One preset per lane must pass				All must pass

PCIE Reliance Upon Stable RefClk

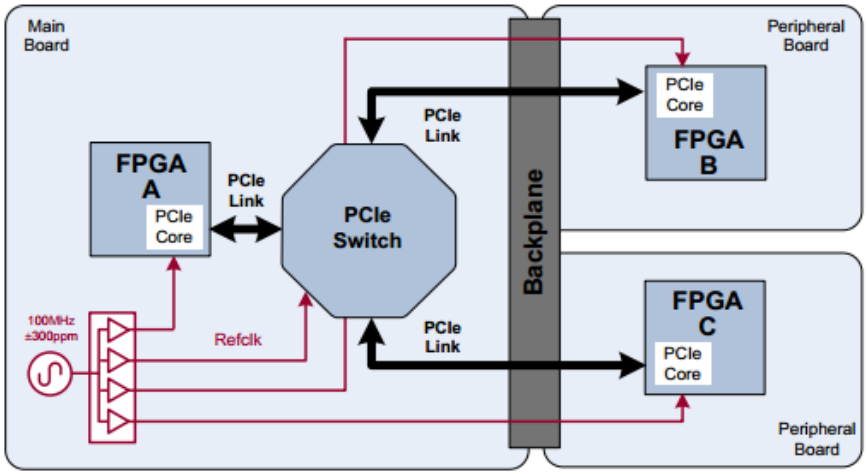
Data transfer between two devices on the same PCB



Data transfer between main board and add-in board



Data transfer between multiple boards over a backplane

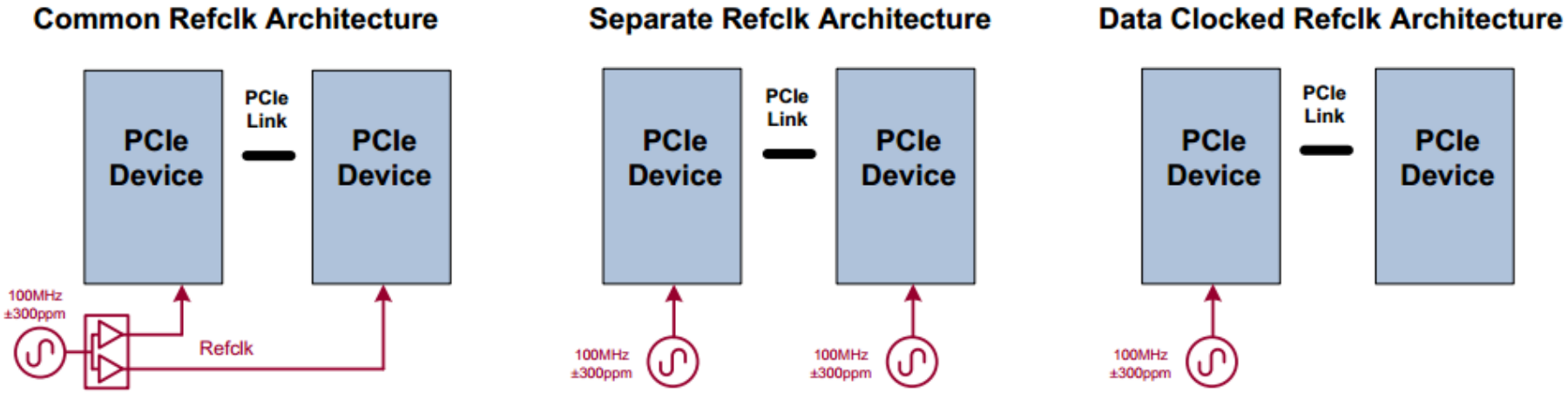


- PCIe RefClk provides a stable timing reference for the high-speed serial data transmission between two PCIe devices
- For reliable operation, RefClk must have low jitter

"Selecting the Optimum PCI Express Clock Source", Figure 2, page 2, Silicon Laboratories, Inc.

PCIe RefClk Architectures

- PCIe standard specifies a 100 MHz clock (Refclk) with greater than ±300 ppm frequency stability at both the transmitting and receiving devices and support for three distinct clocking architectures:



- **Common** – most popular, supports SSC; same clock must be connected to all devices while maintaining skew <= 12 ns between devices
- **Separate/independent** – used for cabled applications; SSC not historically used prior to Gen4; now becoming increasingly used via SRIS
- **Data Clocked** – simplest to implement, but not very common

"Selecting the Optimum PCI Express Clock Source", Figure 3 page 3, Silicon Laboratories, Inc.

DPOJet for PCIe 1/2/3 RefClk

IMPORTANCE OF ACCURATE PCIE REFCLK MEASUREMENTS

- PCIe RefClk signal has very tight jitter requirements even though it only operates @ 100MHz
- RefClk jitter has direct impact on the quality of the data transfer between PCIe Tx & Rx
- Clock-data recovery (CDR) process must be able to track those jitter frequencies that are within it's bandwidth, & limit those it cannot track
- The PCIe Base Spec defines the:
  - Untrackable jitter spectrum using multiple transfer functions (H1, H2, H3, etc.) that represent the loop bandwidths of the CDR & PLLs that affect the data recovery process
  - Overall transfer function, parameters (peaking & bandwidth), & jitter limits for each of the 3 clocking architectures (common, data clocked, & separate)

PCIe 1/2/3 RefClk Specs

Common

	Description	Symbol	Limit	Units
PCIe 1.1	Random Jitter	R_j	4.7	ps pk-pk
	Deterministic Jitter	D_j	41.9	ps pk-pk
	Total Jitter where Tj = Dj + 14.069 x Rj (for BER 10^{-12})	T_j	108	ps pk-pk
PCIe 2.1	High Frequency RMS Jitter Measured from 1.5 MHz to Nyquist (or $f_{REFCLK} \div 2$)	J_{RMS-HF}	3.1	ps RMS
	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	J_{RMS-LF}	3.0	ps RMS
PCIe 3.1	Random Jitter	J_{RMS}	1.0	ps RMS

Note: All jitter measurements are filtered using the overall transfer function(s) defined in Figure 4 after all combinations of parameters have been exercised. See Appendix A–D.

Data Clocked

	Description	Symbol	Limit	Units
PCIe 1.1	Not defined in PCIe standards			
PCIe 2.1	High Frequency RMS Jitter Measured from 1.5 MHz to Nyquist (or $f_{REFCLK} \div 2$)	J_{RMS-HF}	4.0	ps RMS
	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	J_{RMS-LF}	7.5	ps RMS
PCIe 3.1	Random Jitter	J_{RMS}	1.0	ps RMS

Note: All jitter measurements are filtered using the overall transfer function(s) defined in Figure 4 after all combinations of parameters have been exercised. See Appendix A.

Separate

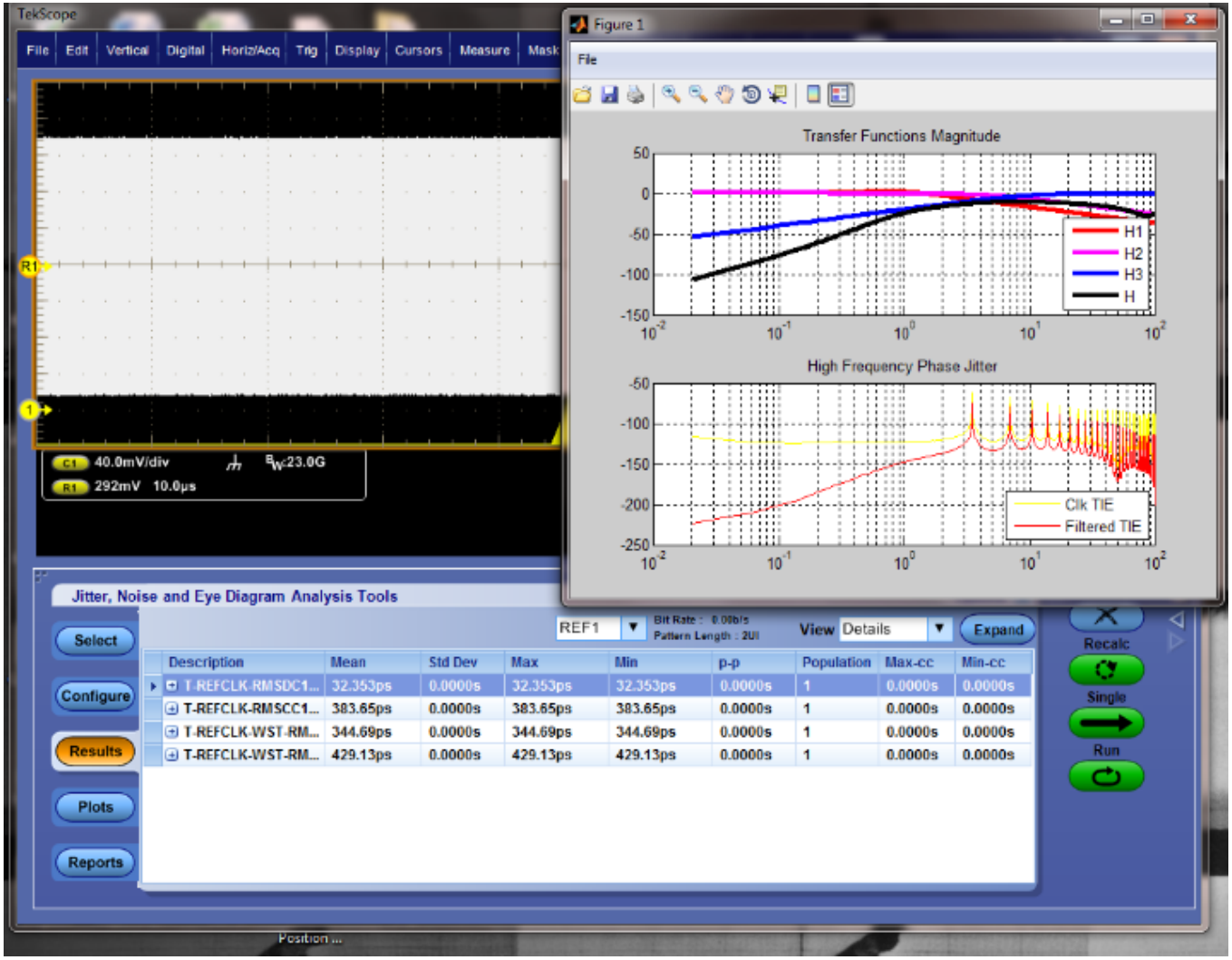
	Description	Symbol	Max Limit	Units
PCIe Gen2	RMS Refclk jitter for SRIS architecture at 5.0Gb/s (Gen2)	$T_{REFCLK-RMS-SRIS}$	2.0	ps RMS
PCIe Gen3	RMS Refclk jitter for SRIS architecture at 8.0Gb/s (Gen3)	$T_{REFCLK-RMS-SRIS}$	0.5	ps RMS

- PCIe RefClk Rj (Random Jitter) spec has shrunk from 4.7ps (Gen1) to 1.0ps (Gen3)
- Gen4 target spec is <1.0ps (possibly 700fs)

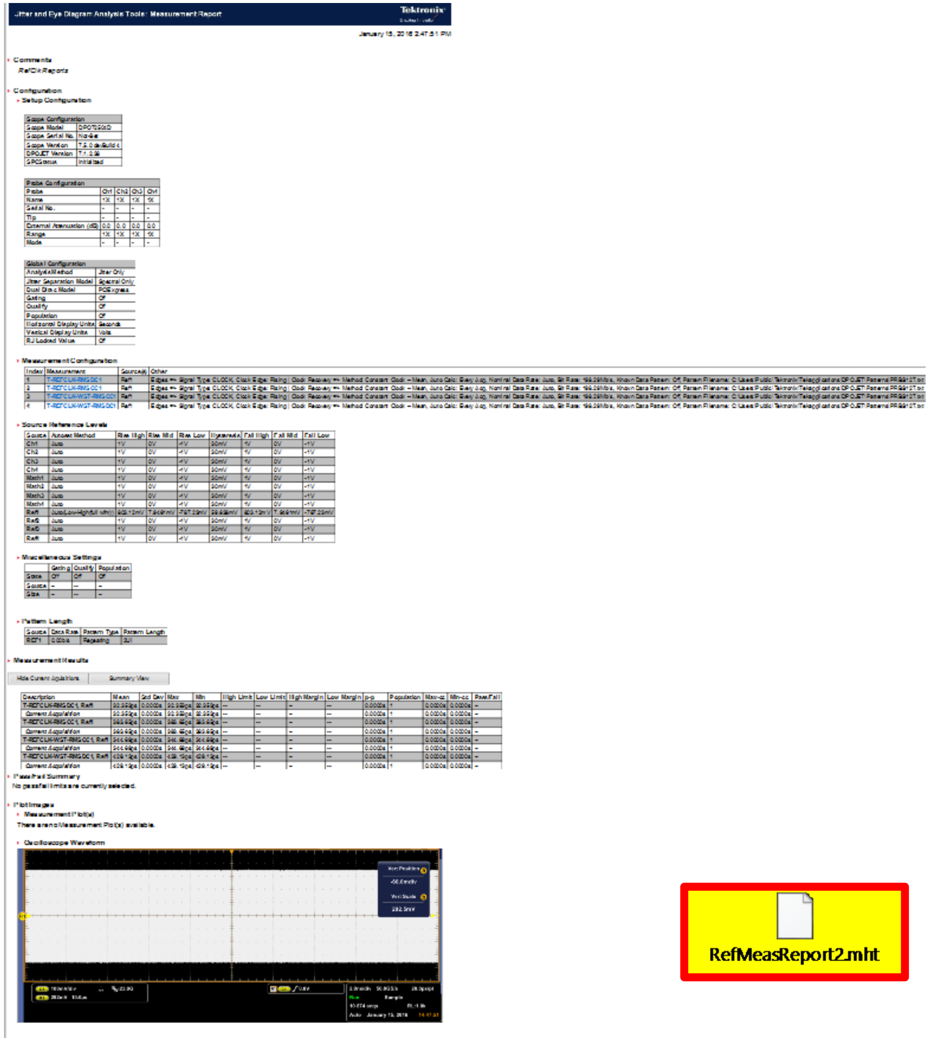
"Selecting the Optimum PCI Express Clock Source", Table 1, 2, 3, pages 6, 8, 9, Silicon Laboratories, Inc.

DPOJet for PCIe 1/2/3 RefClk

MEASUREMENTS



DPOJet for RefClk - Reports



- Detailed reports with scope configuration and measurement results including plots are available

RefMeasReport2.mht

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PCI Express Form Factors

CEM Add-In-Card (AIC)

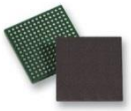
U.2 (SFF-8639)

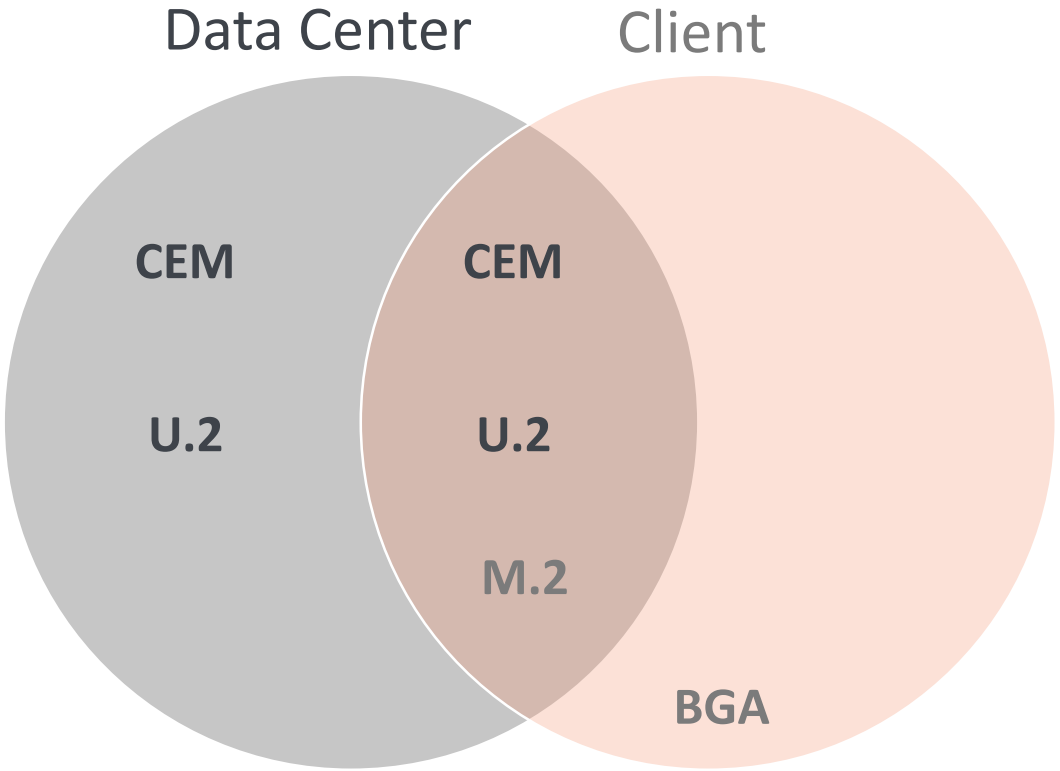
U.2-to-CEM Adapter

M.2

M.2-to-CEM Adapter

BGA *(Embedded)*

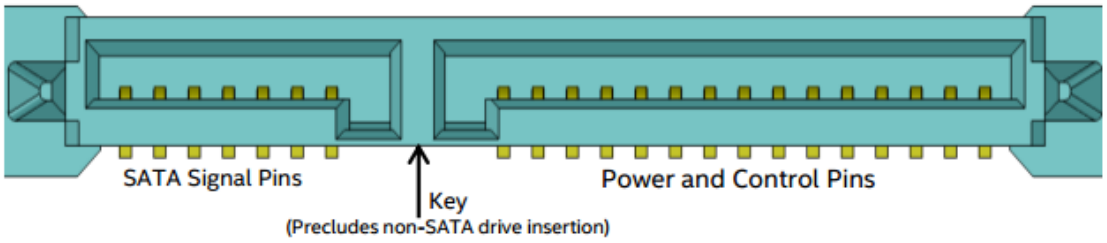




SFF-8639 Connector → U.2 Connector

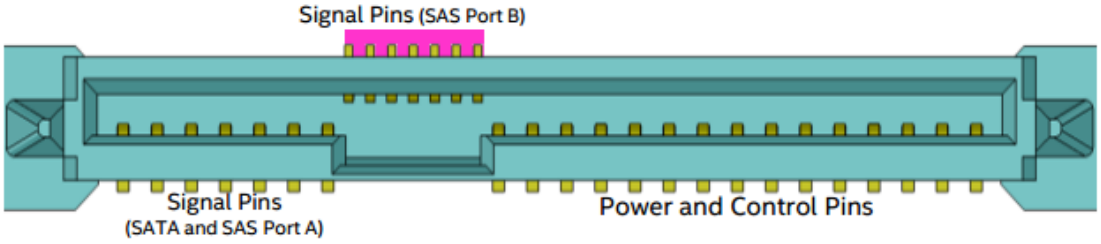
Current SATA Connector

- Uses legacy SATA pin pitch
- Keyed to preclude the insertion of a non-SATA drive



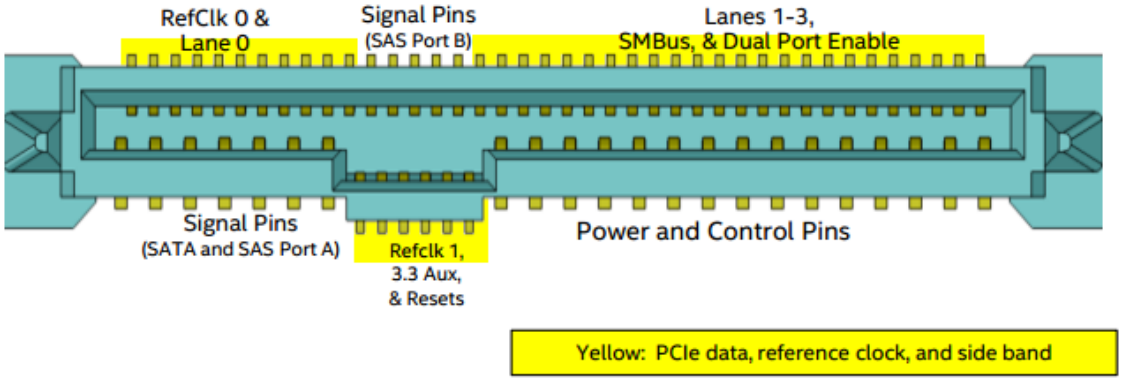
Current SAS Connector

- Added additional signaling pins for a secondary port option at with a tighter, modern, pin pitch
- Supports both SATA and SAS drives



SFF 8639 Connector

- Fills out all remaining pin capacity of the legacy form factor
- Designed to support many protocols
- Enterprise mapping supports legacy SATA, SAS, and modern PCIe* drives simultaneously
  - Both single port X4 and dual port X2 drives
  - PCI-SIG Specification now at rev. 0.7

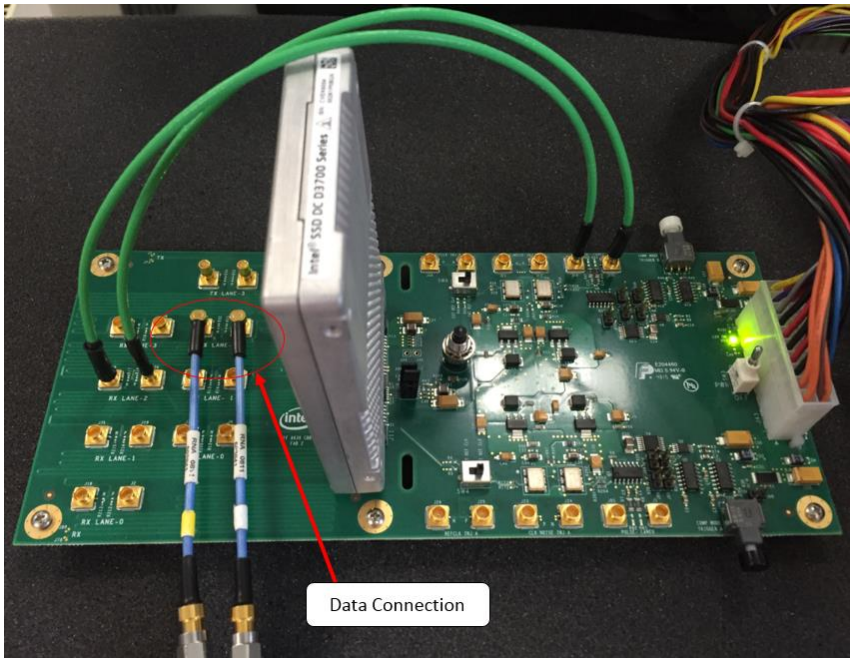


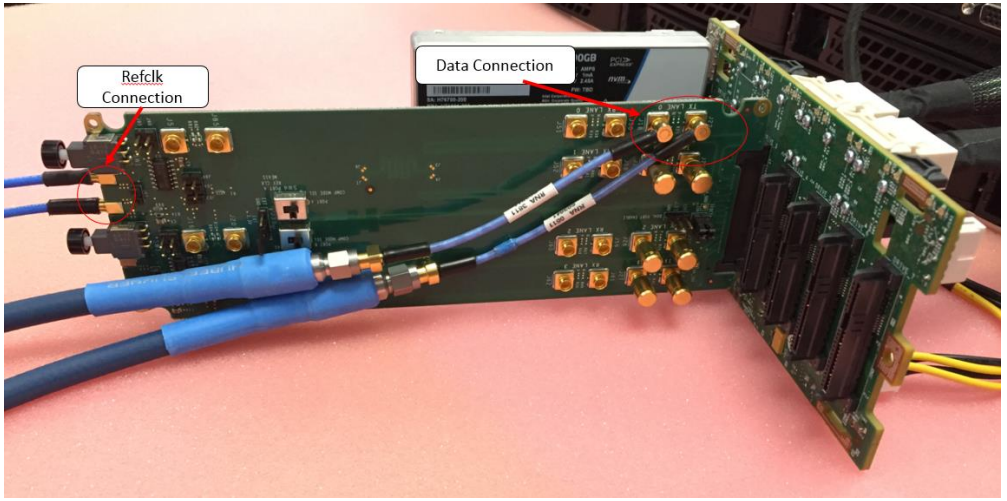
SSF 8639 connector expected to meet same CEM electrical requirements as standard PCIe connector

Source:SFF-8639 PCIe* SSD Ecosystem Readiness and Electrical Testing Update, Flash Memory Summit 2014

New PCI-SIG U.2 Compliance Fixtures

SUPPORTED IN TEKEXPRESS





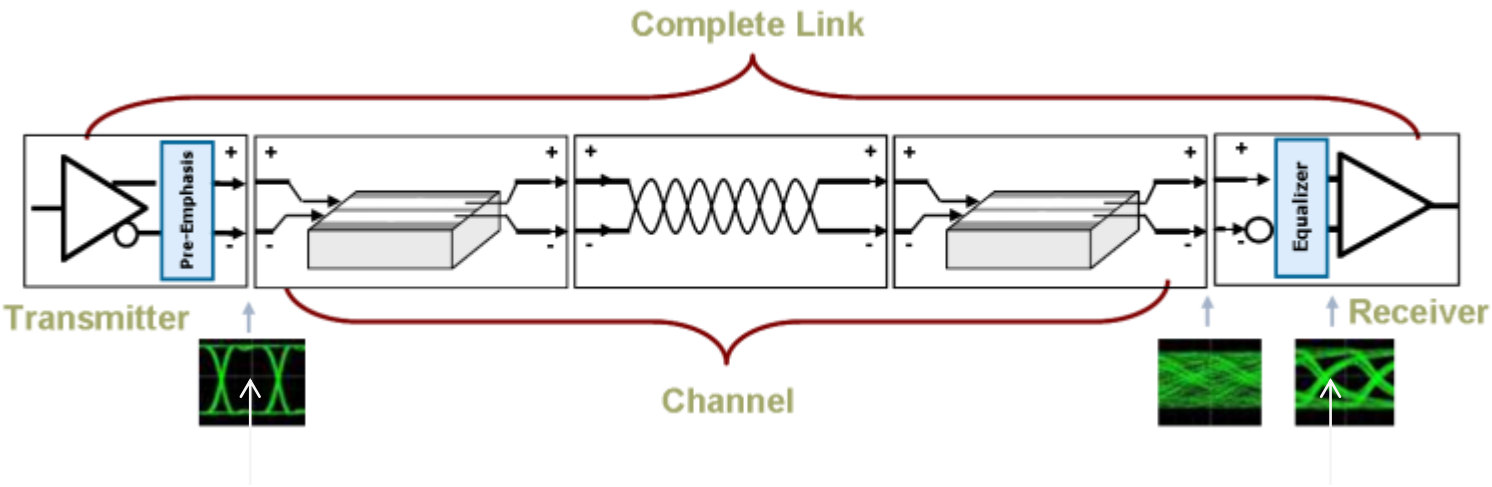
- Similar to CBB3
- Tests add-in cards
- 4 lanes

- Similar to CLB3
- Tests systems
- 4 lanes

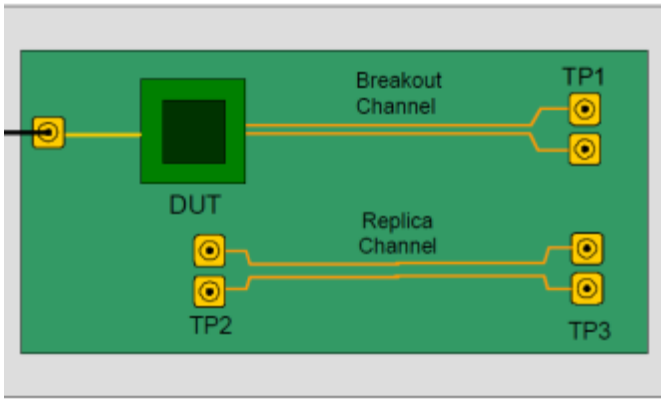
Tektronix PCIE3 Tx Solution

APPROVED FOR PCI-SIG INTEGRATOR'S LIST TESTING

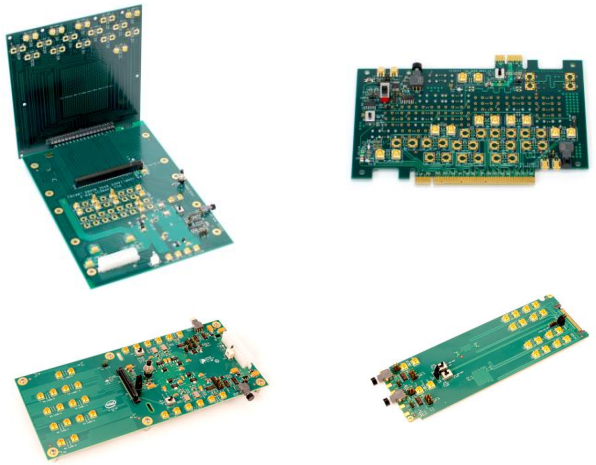
PCIe Base vs Form Factor (CEM/U.2)



Measure for Base

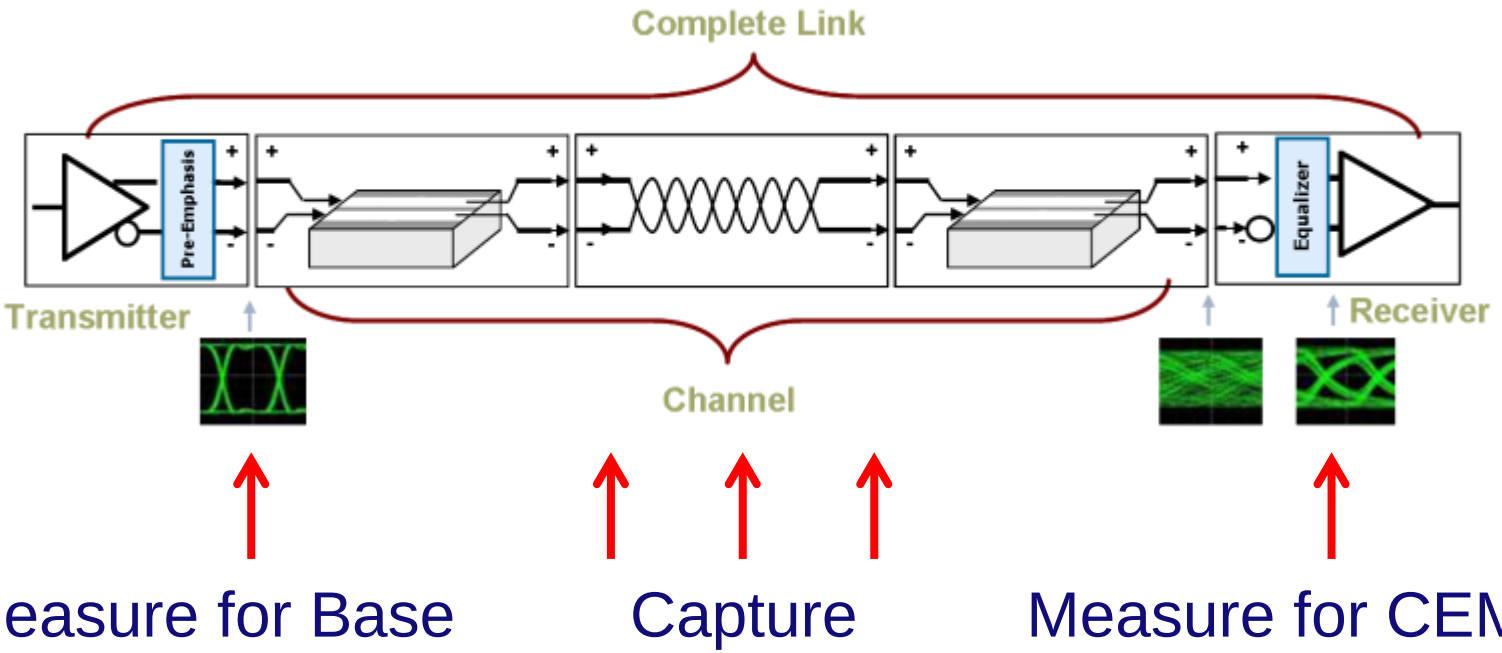


Measure for CEM & U.2



PCIe Base vs CEM Testing

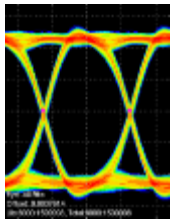
- What test point each type of testing addresses?
- How do we get to see the signal at the point of interest?



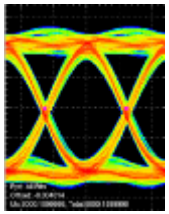
Base Spec Tx Testing

SILICON LEVEL

- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not possible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- S-Parameters are acquired on the replica channel
- Measurement at TX pins can also be enabled by high fidelity probes, eg P7700

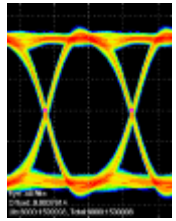


Signal at Tx Pins

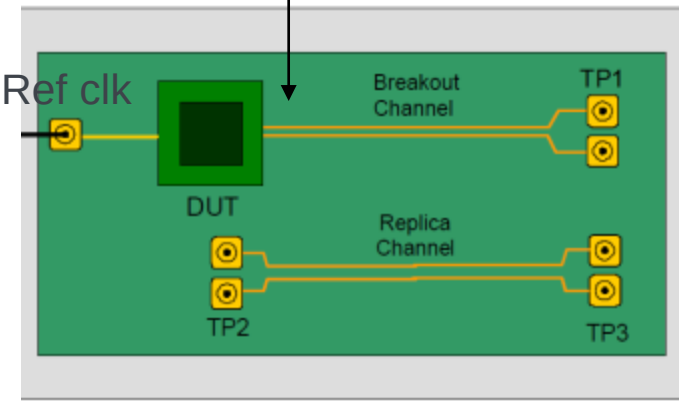


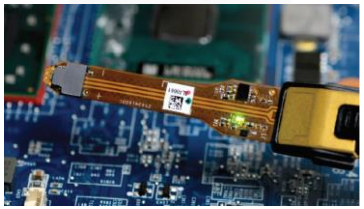
Measured Signal at TP1

De-embed using S-Parameters



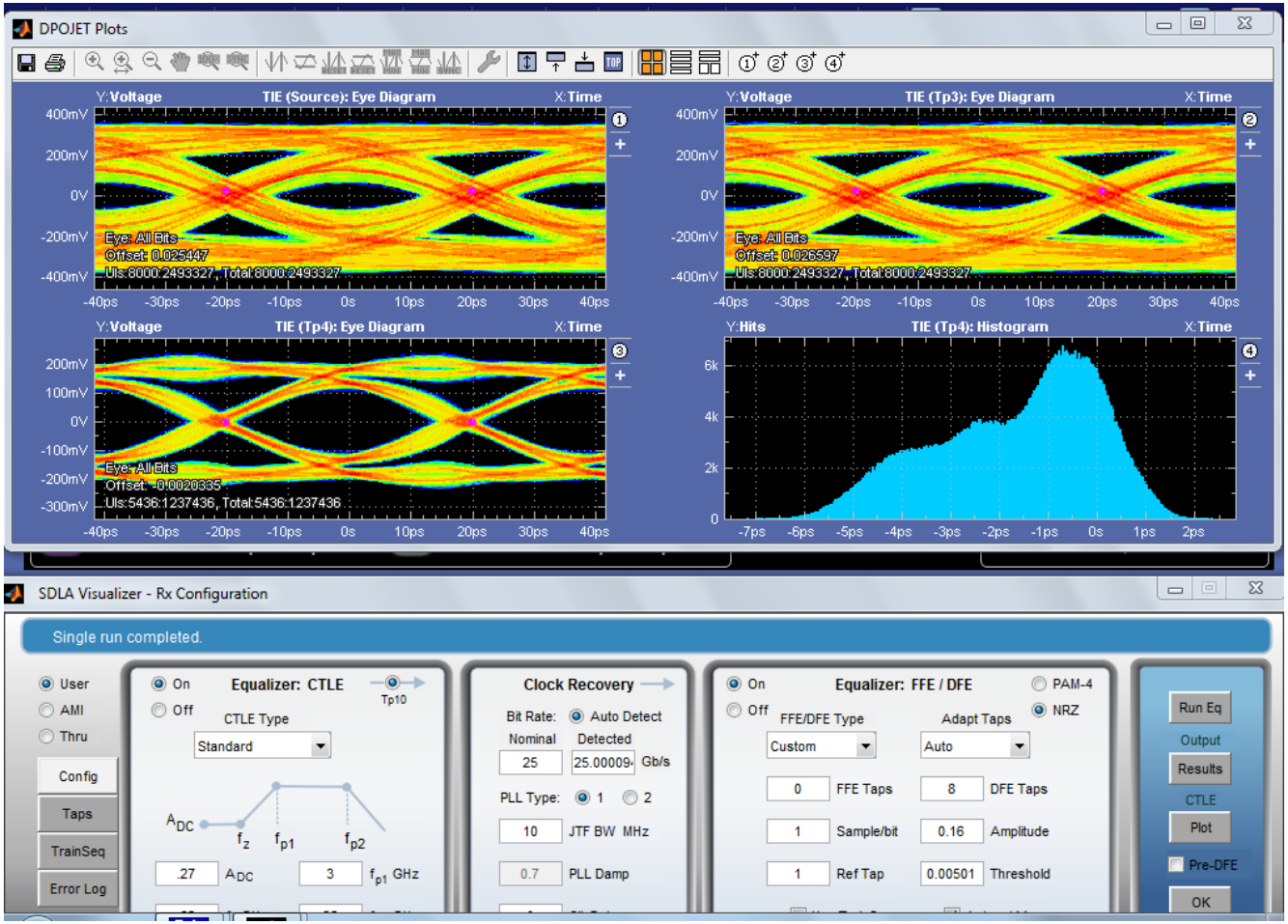
Signal with Channel Effects Removed





SDLA

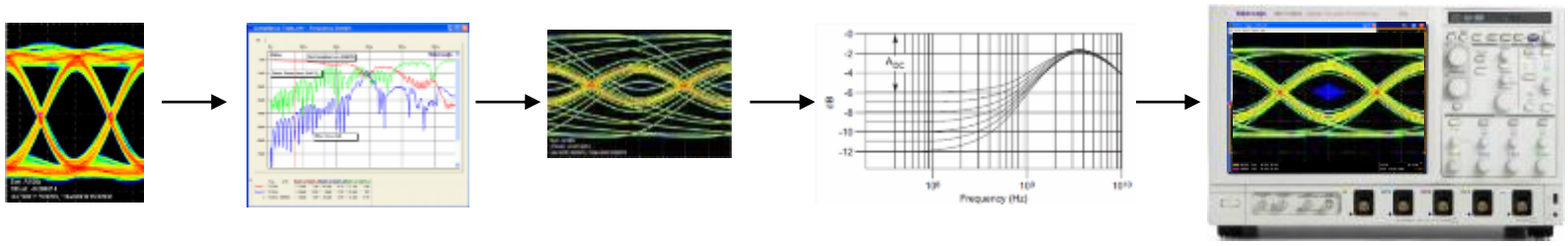
SERIAL DATA LINK ANALYSIS



CEM & U.2 Spec Tx Testing

System & Add-In Card

- CEM Specification Measurements are defined at the slicer of a receiver
- Signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required
- SigTest or custom software like DPOJET will perform the embedding and calculate measurements



Signal Acquired from Compliance Board

Embed Compliance Channel and Package

Closed Eye due to the Channel

Apply CTLE + DFE

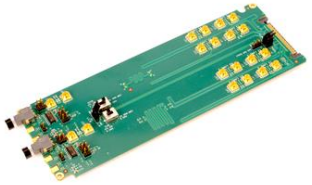
Open Eye for Measurements

Testing Challenges in Tx

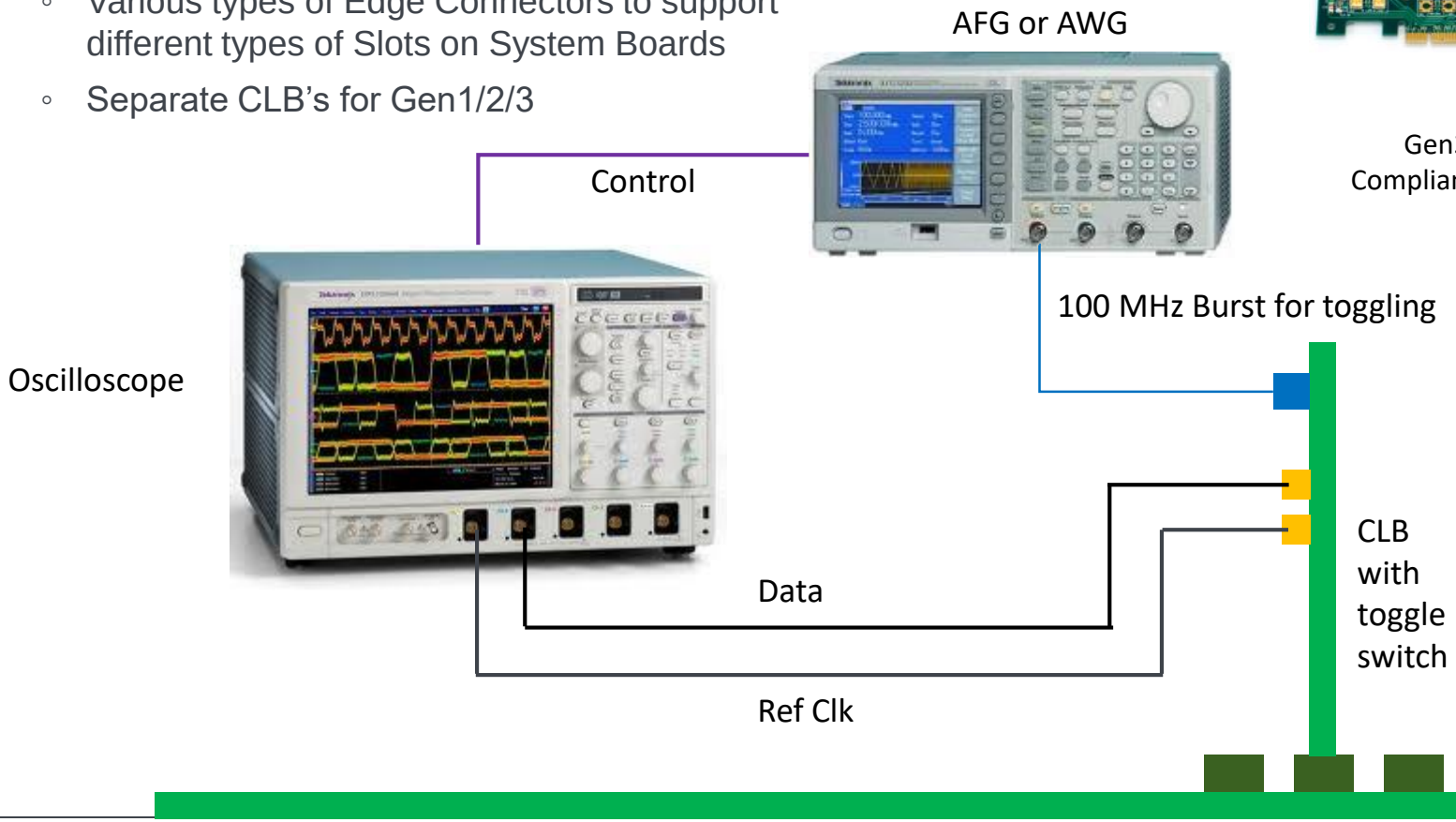
- Meet the requirements for effective testing
  - √ Compliance mode support, proper patterns and toggling mechanism
  - √ Correct Tx equalization settings and preset and Lane ID encoding in Tx compliance pattern
- Why so many presets? How to capture so many lanes?
  - √ The answer is test automation, RF switch
- Measurement algorithms
  - √ Implemented in SigTest, or scope specific software
- How to achieve required confidence level and beyond?
  - √ Length and number of waveforms (for Tx)

System/Host Test Fixture

- Compliance Load Board (CLB)
  - Used for testing System Boards
  - All Tx / Rx Lanes and Ref Clk routed to SMP
  - Compliance Mode Toggle Switch
  - Various types of Edge Connectors to support different types of Slots on System Boards
  - Separate CLB's for Gen1/2/3



Gen3 CEM/U.2 Compliance Load Board (CLB3)

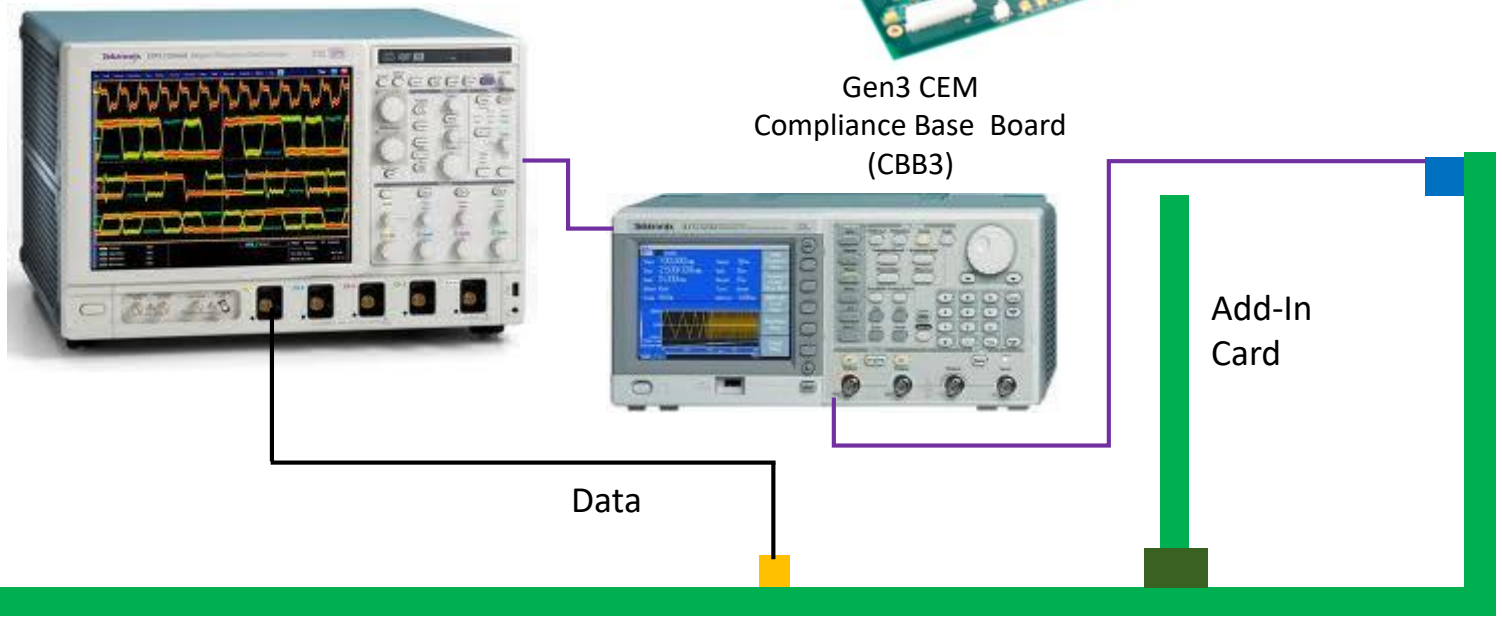


Add-In Card Test Fixture

- Compliance Base Board (CBB)
  - Used for Testing Add-In cards
  - All Tx / Rx Lanes are routed to SMP
  - Compliance Mode Toggle Switch
  - Low Jitter Clean Reference Clock
  - Separate CBB for Gen 1/2/3

Gen3 CEM
Compliance Base Board
(CBB3)

Gen3 U.2
Compliance Base Board
(CBB3)



CBB with Multiple Slots of different widths and toggle switch

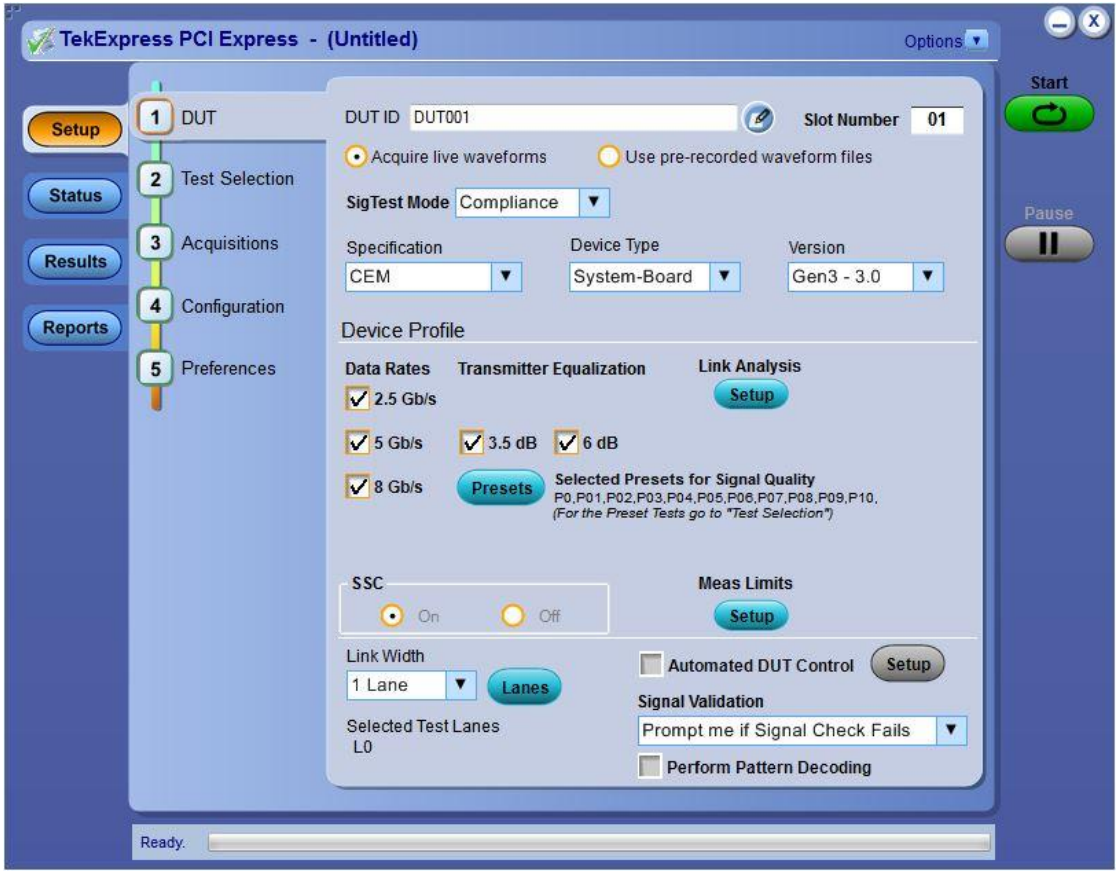
Automation Simplifies Tx Testing

- While convenient single capture capability is essential, automation makes the testing practical
- Iterate over multiple presets and lanes
- Gather results in a single report
- Provide means for quick switch to debugging and additional measurements
- Remove test fixture effects by using de-embedding

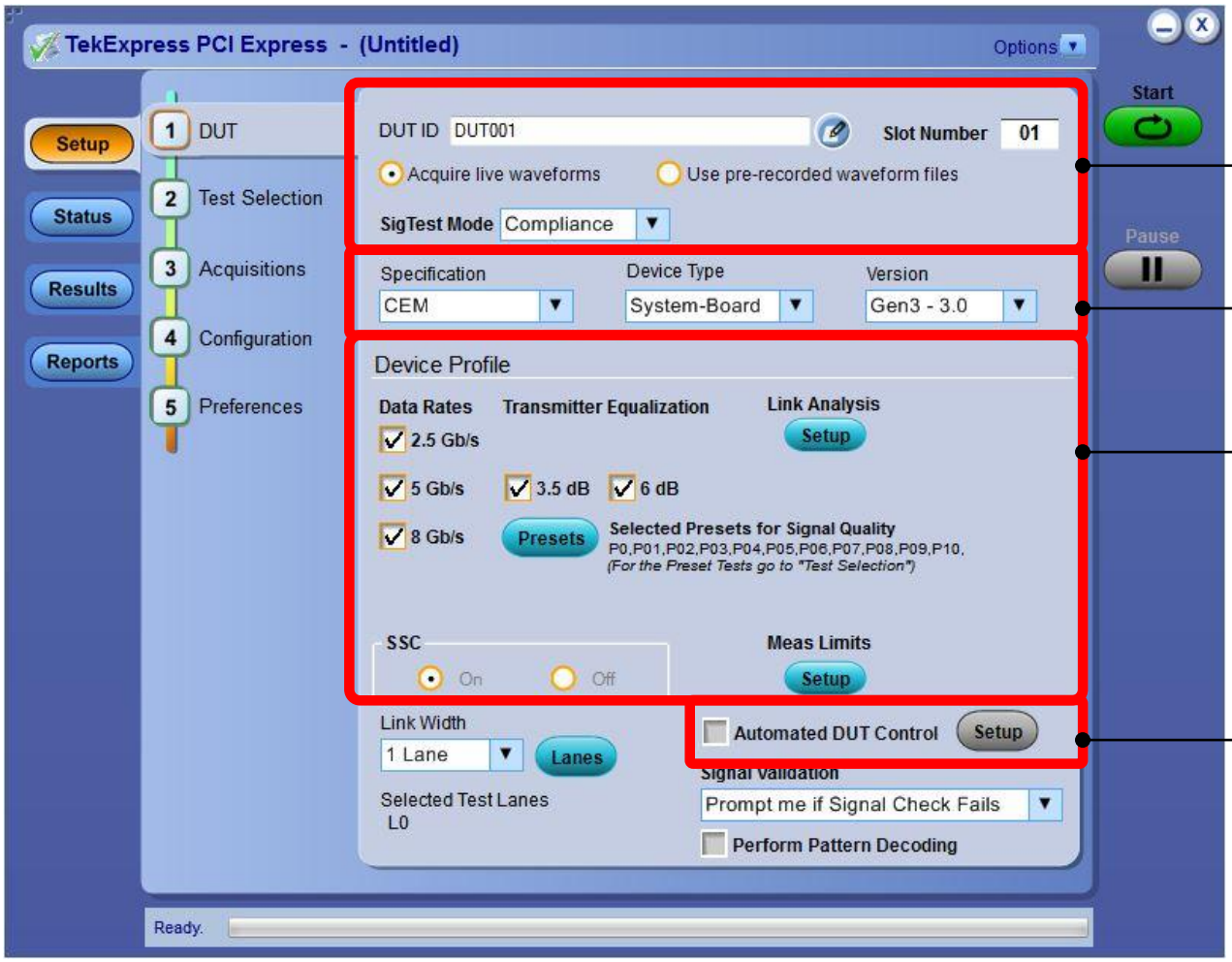
TekExpress for PCIe (Opt PCE3)

- TekExpress Automation for Tx Compliance with unique features including:

  - √ Sets up the Scope and DUT for testing
  - √ Toggles thru and verifies the different Presets and Bit Rates
  - √ Tests multiple slots and lanes
  - √ Acquires the data
  - √ Processed with PCI-SIG SigTest
  - √ Provides custom reporting



TekExpress - Setup



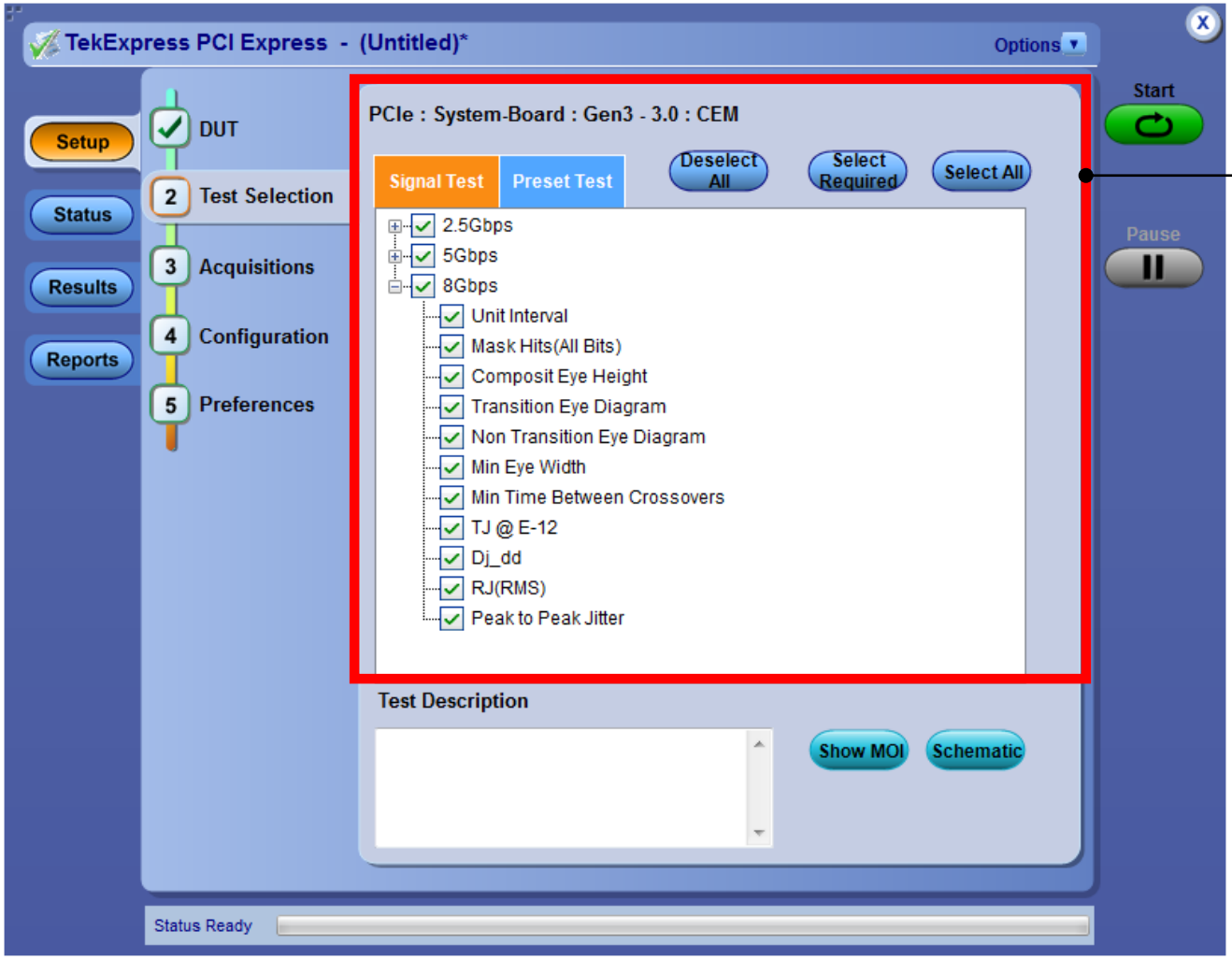
Run Analysis on Live or Pre-Recorded Data

Type of test / device selection

Test selection

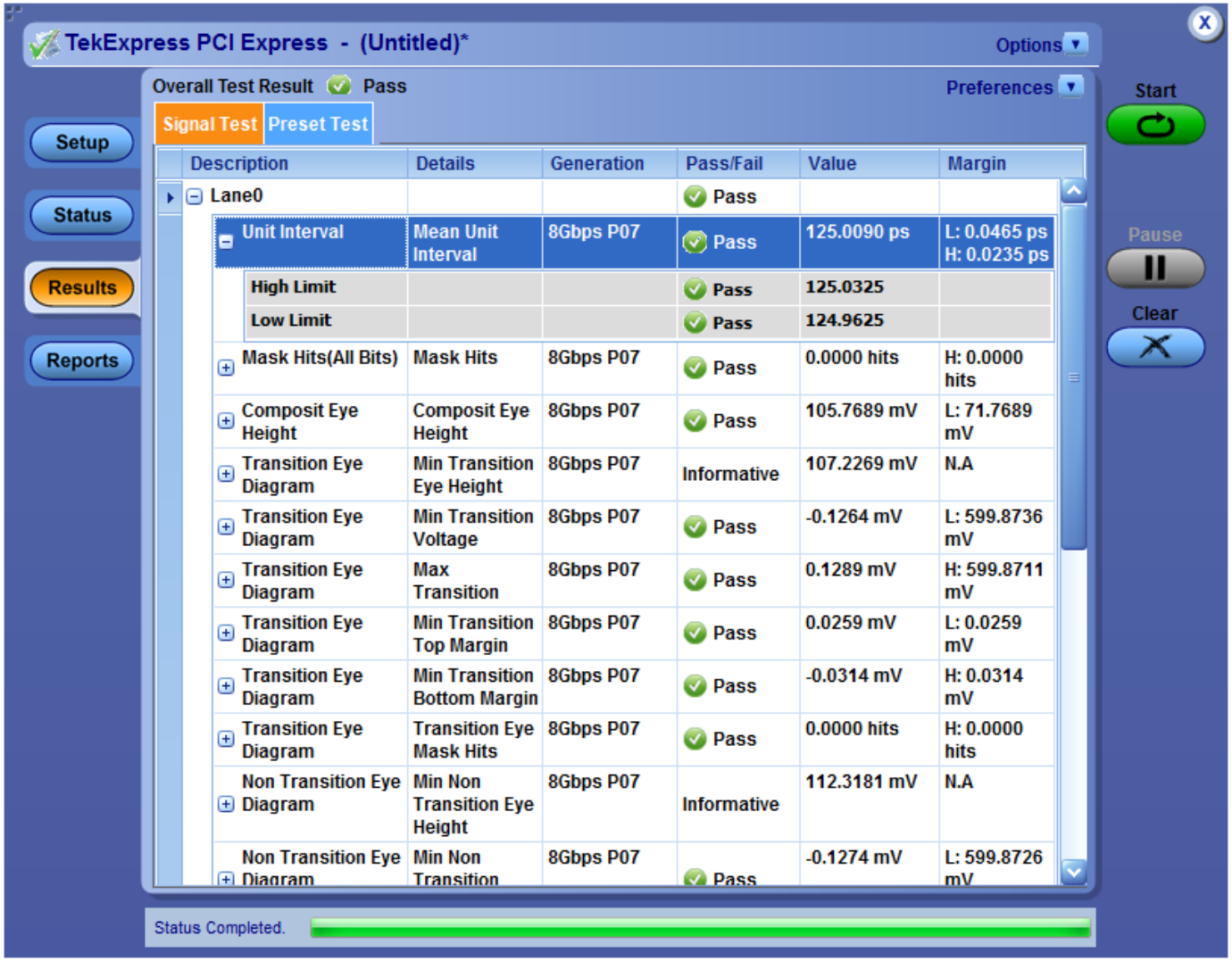
Automate DUT control

TekExpress – Test



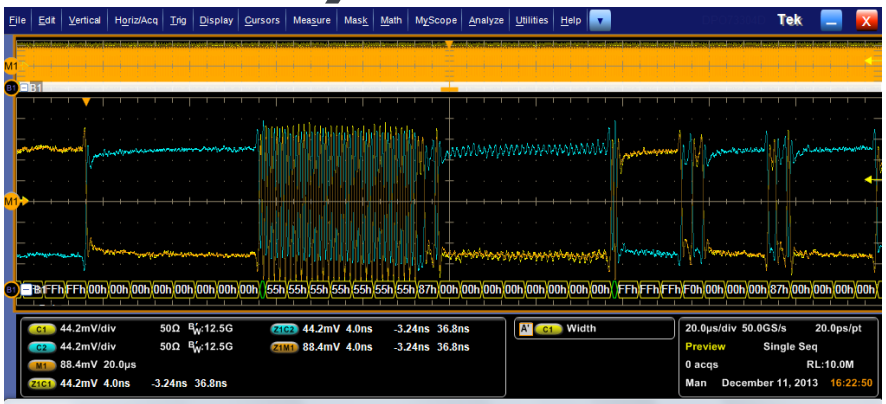
Test Selection

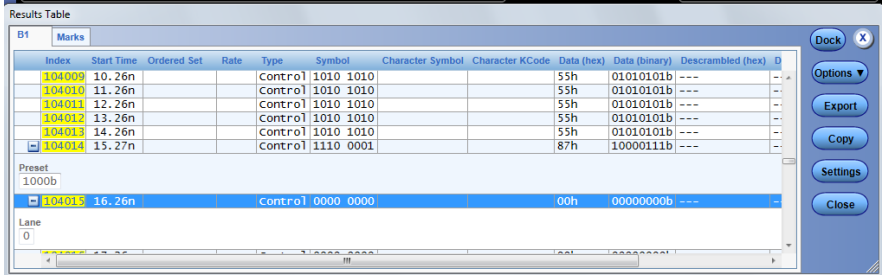
TekExpress – Reports

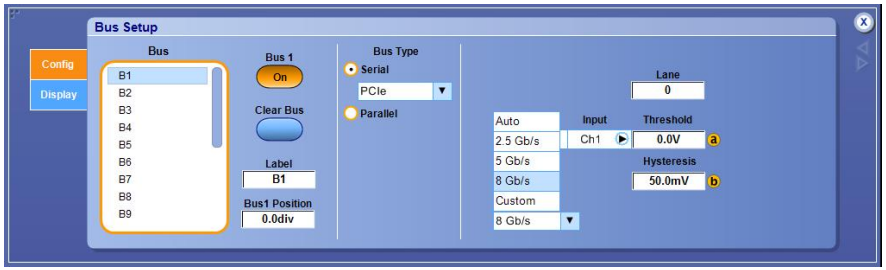


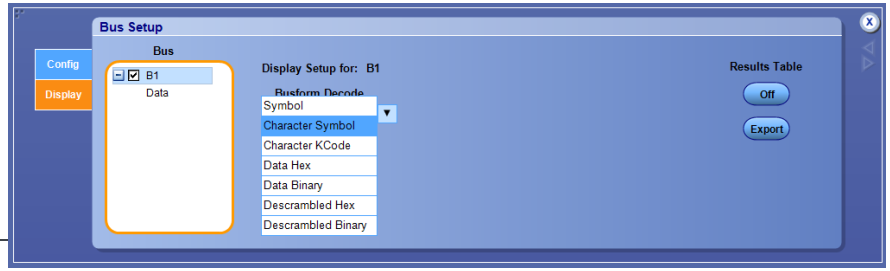
PCIe Decoder (Opt SR-PCIe)

- Decodes and displays PCIe data using characters and names that are familiar from the standard, such as:
  - SKP
  - Electrical Idle
  - EIEOS
- Easily configured through “Bus Setup” under “Vertical” menu with a variety of user-adjustable settings
- Results table shows time-correlated listing of events time-correlated with waveform view
- Integrated search with marks
- Triggering up to 6.25Gbs (Gen1 & Gen2 only)









PCIe Decoder (Opt SR-PCIe)

Decoding of PCIe Gen3 compliance pattern Tx preset encoding

Decode results show correct value of “87h” or “1000b” (as shown in Results Table) for Transmitter Preset **P8** (-3.5dB de-emphasis with +3.5dB preshoot) on Lane 0

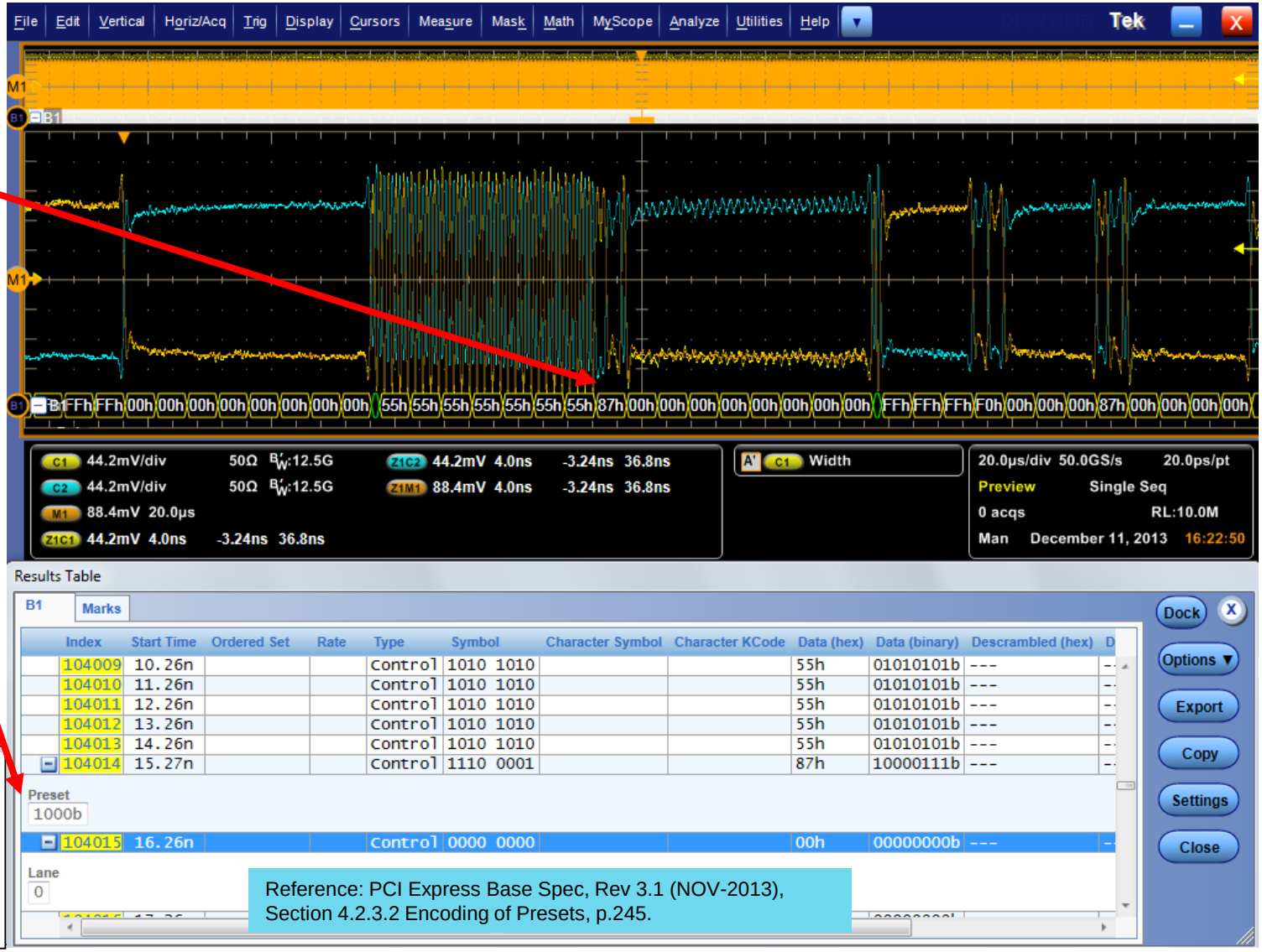


Table 4-3: Transmitter Preset Encoding

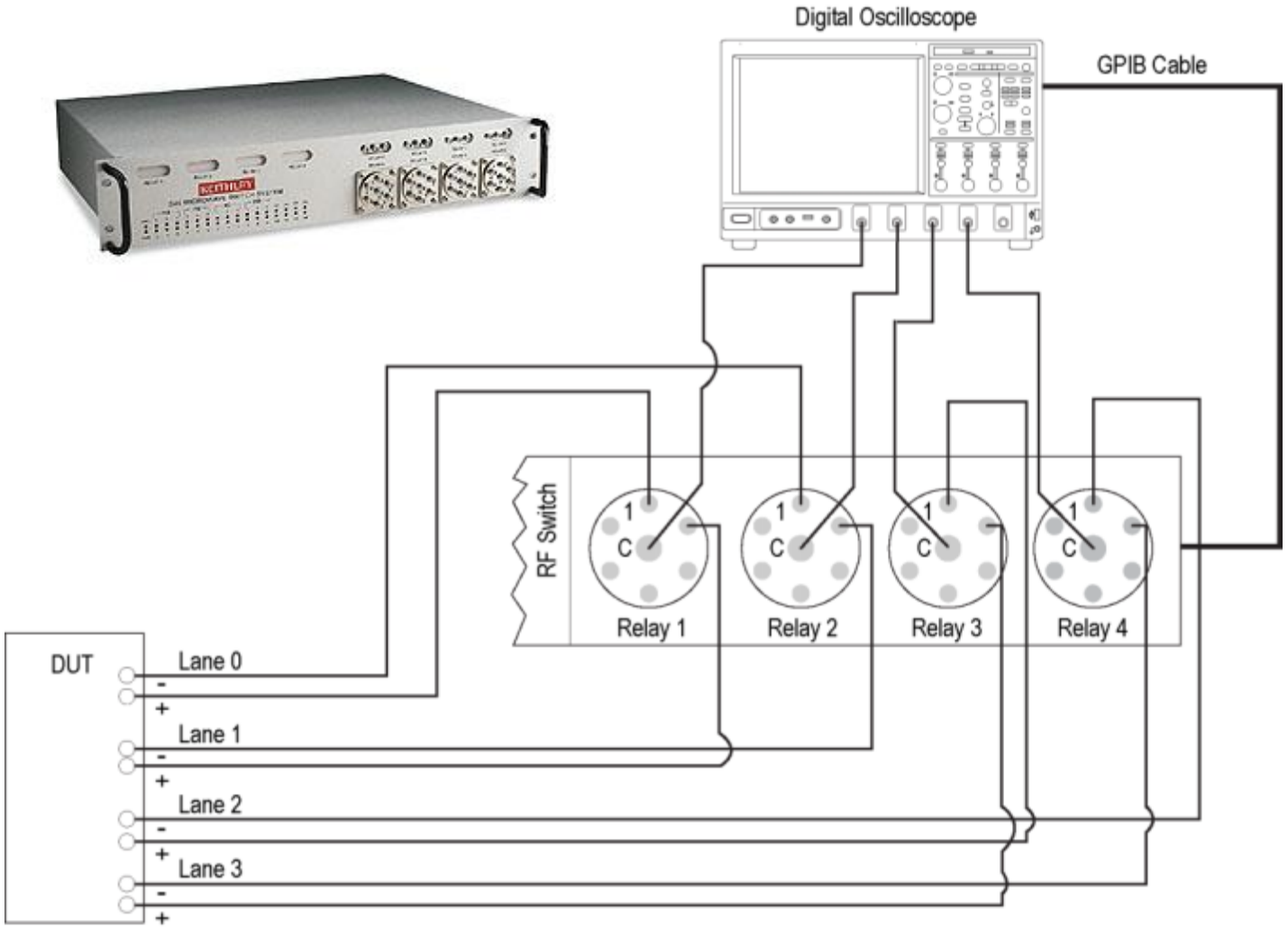
Encoding	De-emphasis (dB)	Preshoot (dB)
0000b	-6	0
0001b	-3.5	0
0010b	-4.5	0
0011b	-2.5	0
0100b	0	0
0101b	0	2
0110b	0	2.5
0111b	-6	3.5
1000b	-3.5	3.5
1001b	0	3.5
1010b	See description above.	See description above.
1011b through 1111b	Reserved	

Reference: PCI Express Base Spec, Rev 3.1 (NOV-2013), Section 4.2.3.2 Encoding of Presets, p.245.

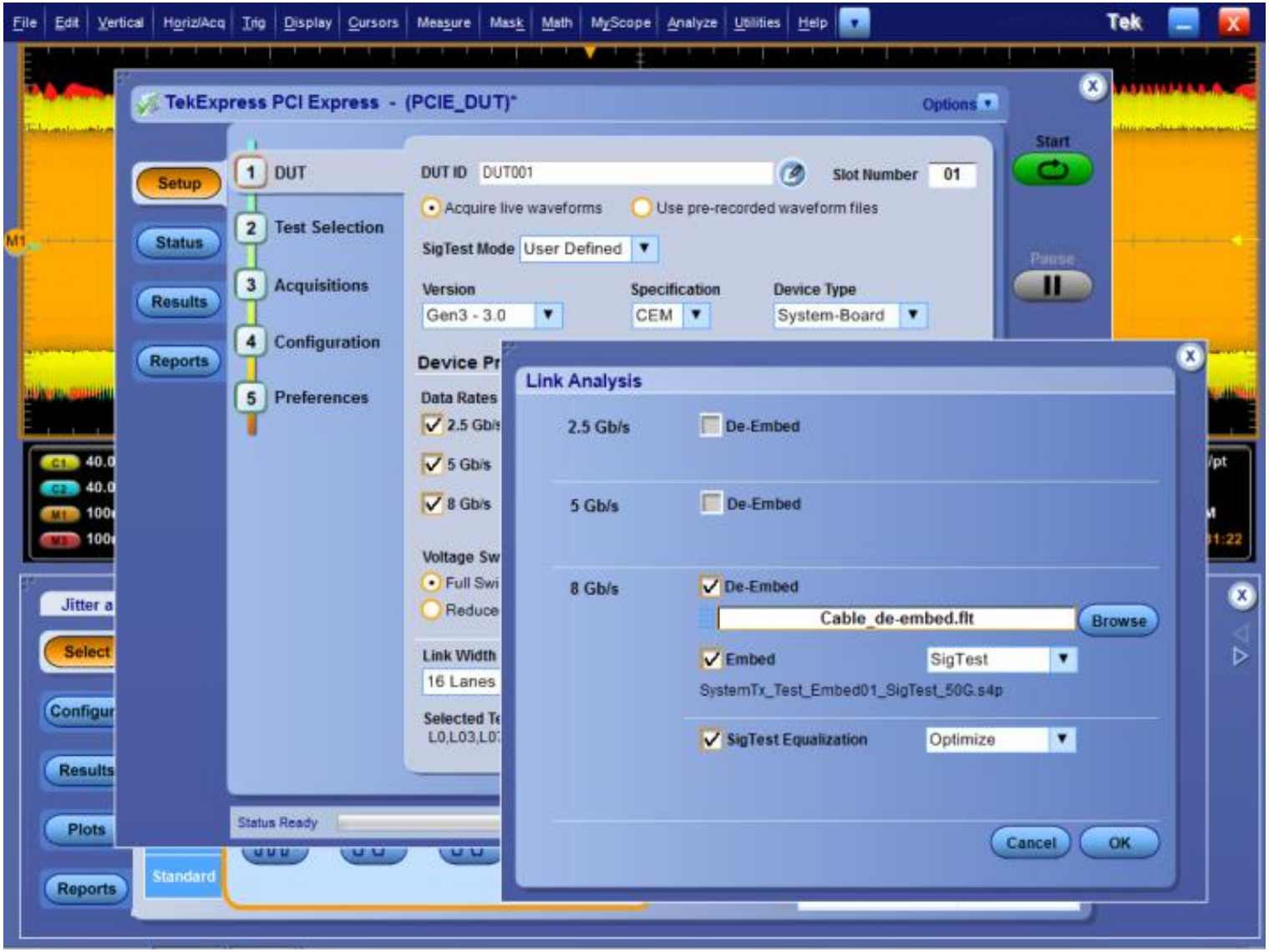
RF Switch and Auto Toggling

- Use RF switch to handle multiple lanes without reconnections
  - √ Must provide termination to maintain compliance mode
  - √ Use programmatic interface to control from automation software
  - √ While switches typically have good signal quality at 4GHz, extra cables must be accounted for by de-embedding
  - √ Design you device so that automatic toggling works for all presets

PCI Express Tx Test with RF Switch



Cable and RF Switch De-embed



Comparison of De-embedding: Add-In Card

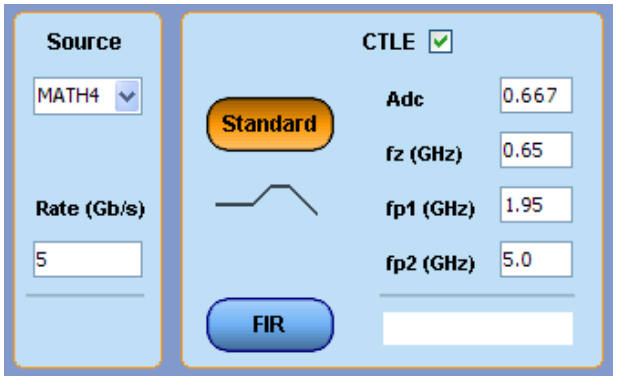
Add-In-Card (P7)	With de-embed	Without de-embed	Diff
SigTest Measurement	Switch & extra cable effects removed	Switch and cable effects present	
Max Peak to Peak Jitter	43.167ps	42.212ps	2.26%
Minimum eye width	83.028ps	83.236ps	-0.19%
Deterministic Jitter d-d	35.605ps	35.436ps	0.48%
Random Jitter	0.453ps	0.450ps	0.67%
Composit Eye height	0.110V	0.101V	8.91%
Min Transition Eye Height	0.111V	0.103V	7.77%
Min Non-transition Eye Height	0.115V	0.109V	5.50%

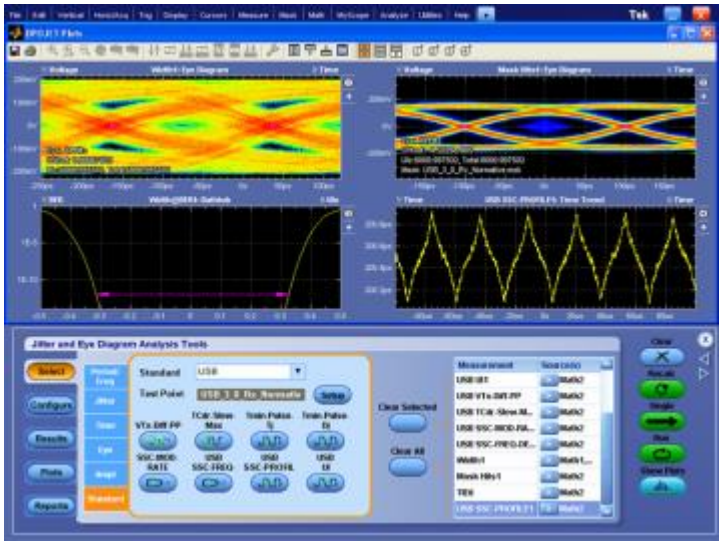
Comparison of De-embedding: System

System Board (P7)	With de-embed	Without de-embed	Diff
SigTest Measurement	Switch & extra cable effects removed	Switch and cable effects present	
Max Peak to Peak Jitter	42.614ps	41.619ps	2.39%
Minimum eye width	81.566ps	82.443ps	-1.06%
Deterministic Jitter d-d	31.261ps	31.653ps	-1.24%
Random Jitter	0.865ps	0.775ps	11.61%
Composit Eye height	0.132V	0.129V	2.33%
Min Transition Eye Height	0.165V	0.152V	8.55%
Min Non-transition Eye Height	0.141V	0.134V	5.22%

Testing Beyond Compliance

- What happens if a measurement fails Compliance?
- Could it be the channel?
  - Measurements can be taken before the channel to evaluate results
  - Different channel models can be created using SDLA Visualizer
- How does the optimized Rx setting compare to other settings?
  - Easily compare the results of multiple Equalization settings
- Does deeper analysis of the waveform need to be done?
  - PCIe specific measurements can be taken in Tektronix' measurement system DPOJET
  - Determine if data dependent, uncorrelated or pulse width jitter is in spec
  - Measurements filters and settings can be adjusted to get to root cause, but remember you must pass SigTest to be certified for compliance
- Is the Tx compliant?
  - NEW PCIe 3.0 base spec measurements are available to verify Tx compliance





Agenda

1. Market Overview
2. Gen3 Overview
3. Gen3 Tx
4. Gen4 Overview
5. Gen4 Tx
6. Gen3 Rx
7. Gen4 Rx

Gen4 Overview

Key Enhancements From PCIe Gen3

- Key attributes/requirements of PCIe 4.0
  - 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  - Reduction in Rj (random jitter) from 3ps (PCIe3) to ~1ps (PCIe4) *[PCIe Base Spec, Table 9.8]*
  - Maintains compatibility w/ PCIe installed base
  - Connector enhanced electrically
    - Gen4 connector backwards-compatible with Gen1/2/3
    - Gen1/2/3 connector, however, will not accept Gen4 add-in cards
  - Limited channel: ~12”, 1 connector; repeater (both redriver & retimer) for longer channels and/or 2nd connector
- New ‘SRIS’ independent RefClk modes
  - SRNS – Separate RefClk Independent with No SSC Architecture
  - SRIS – Separate RefClk Independent with SSC Architecture
- New Rx Lane Margining feature
- Rev 1.0 Base spec released in Oct 2017
- Rev 0.7 Base spec draft

Agenda

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7. Gen4 Rx

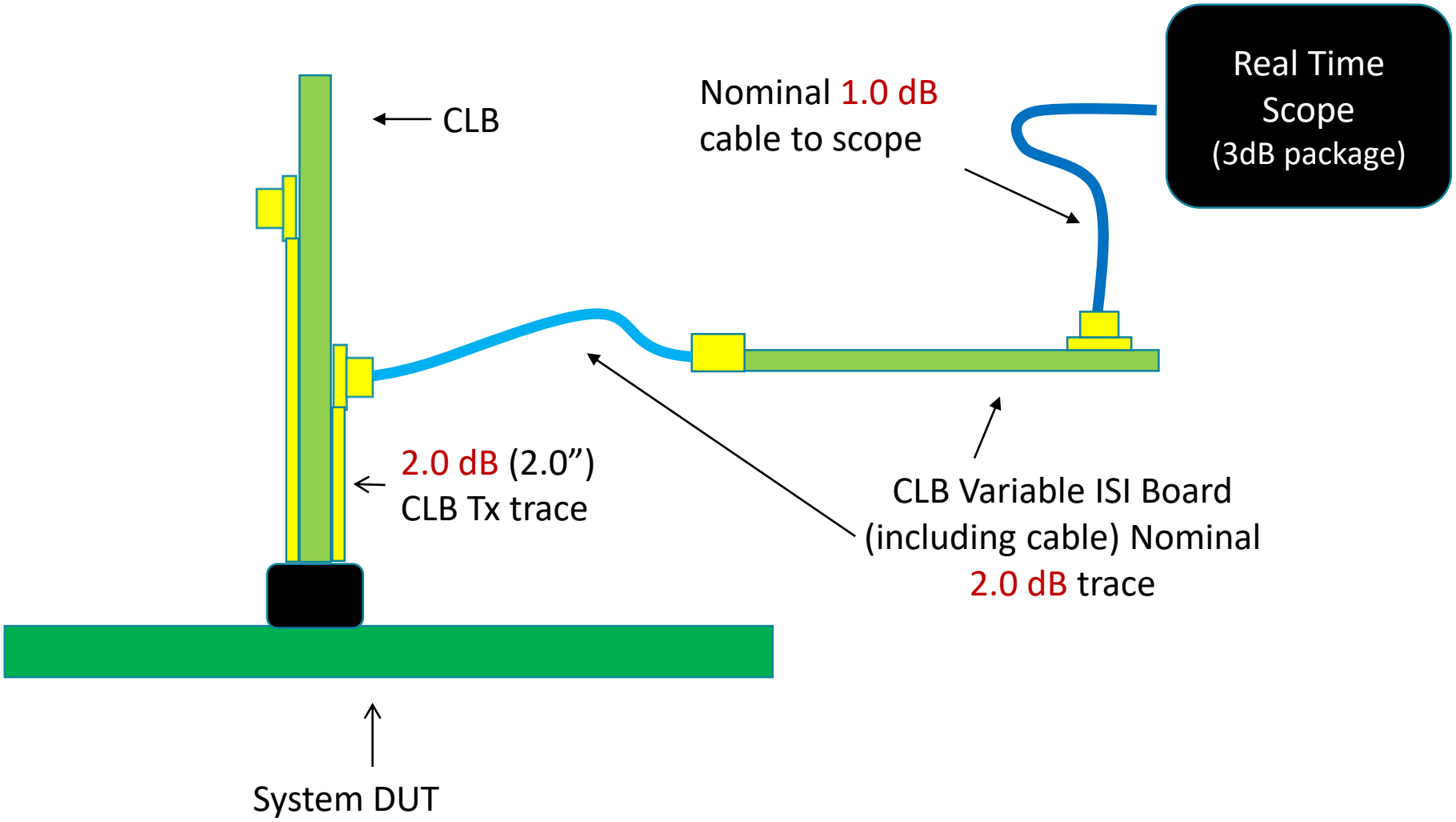
PCIe 4.0
Electrical Tests Under Development

- **Tx signal quality test at 16GT/s**
  - End of channel eye diagram
- **Tx preset equalization test at 16GT/s**
  - Preset 0 – Preset 10
- **16.0GT/s receiver test**
  - Stressed eye receiver loopback test
- **Link equalization handshaking at 16GT/s**
  - Tx starts with correct preset requested through protocol
  - Tx responds to protocol changes and adjusts
  - Rx correctly adjusts the link Tx and operates with a stressed eye
- **All 2.5/5.0/8.0GT/s Testing Still Required for 4.0 Integrators List for a 16GT/s Capable Device**

PCIe 4.0 (System)
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - CLB plugs into system -> Variable ISI Board -> Scope
  - 8dB at 8GHz of additional loss (including package embedding)
- **Power on System**
- **Scope bandwidth = 25GHz**
- **3dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Ref clock captured with data waveform and used for clock recovery
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)

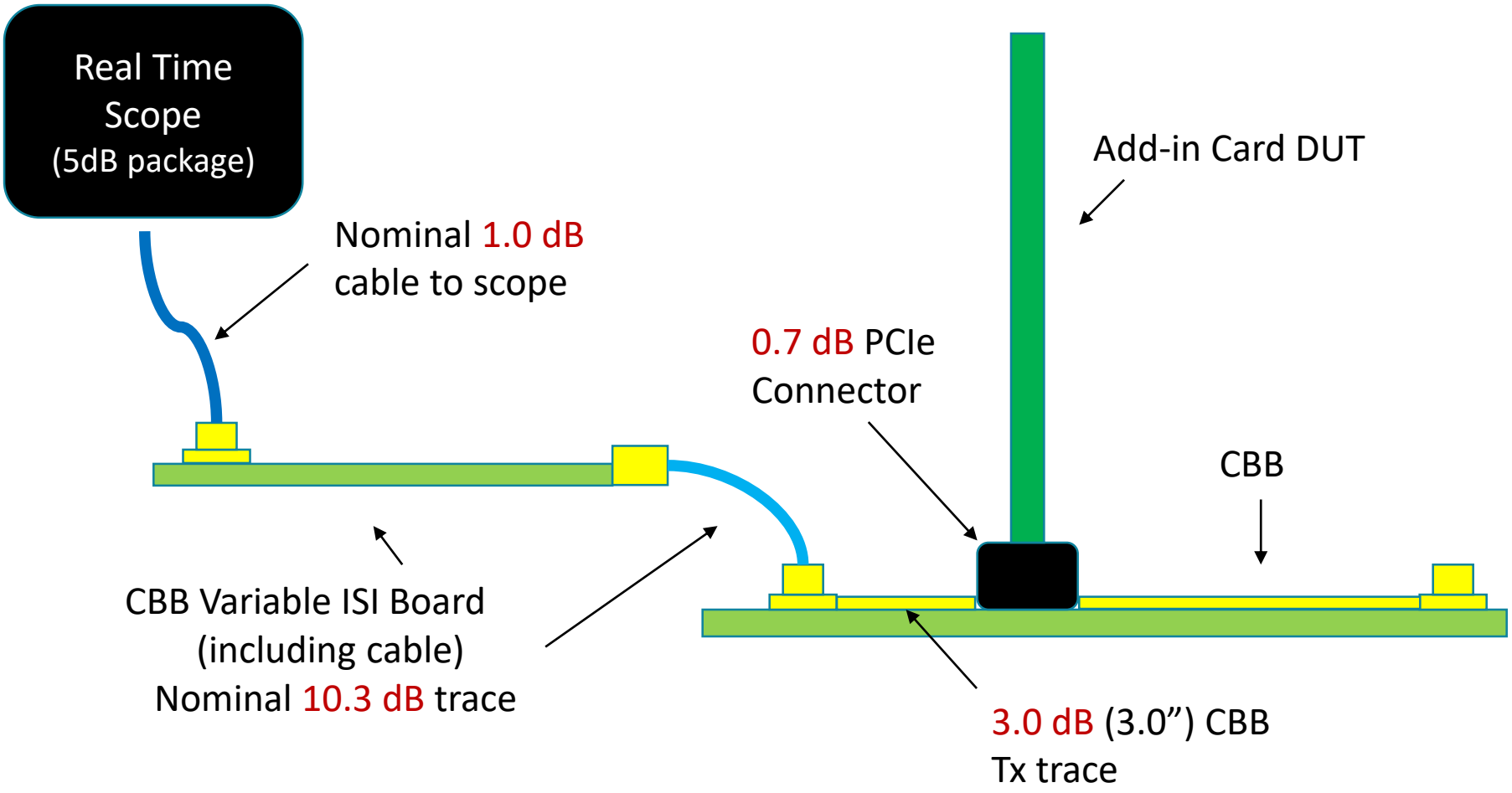
Gen 4 System Tx Test



PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16 GT/s

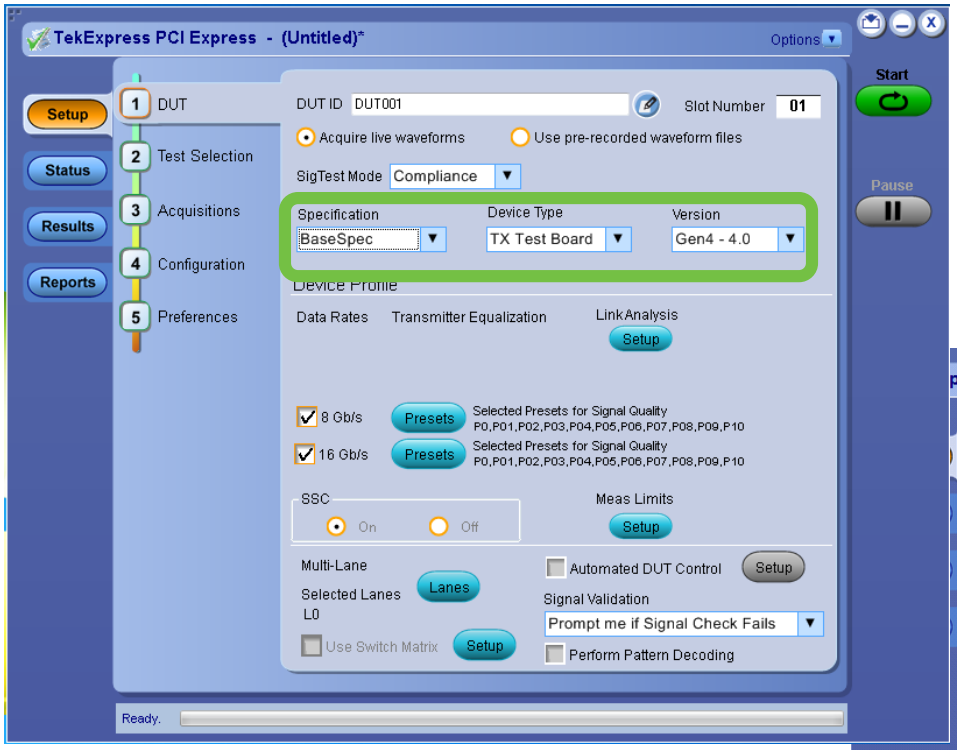
- **Channel Setup**
  - Add-in Card plugs into CBB -> Variable ISI Board -> Scope
  - 20dB at 8GHz of additional loss (including package embedding)
- **Power on CBB**
- **Scope bandwidth is 25GHz**
- **5dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Time Domain CDR algorithm used to recover clock
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)

Gen 4 Add-in Card Tx Test

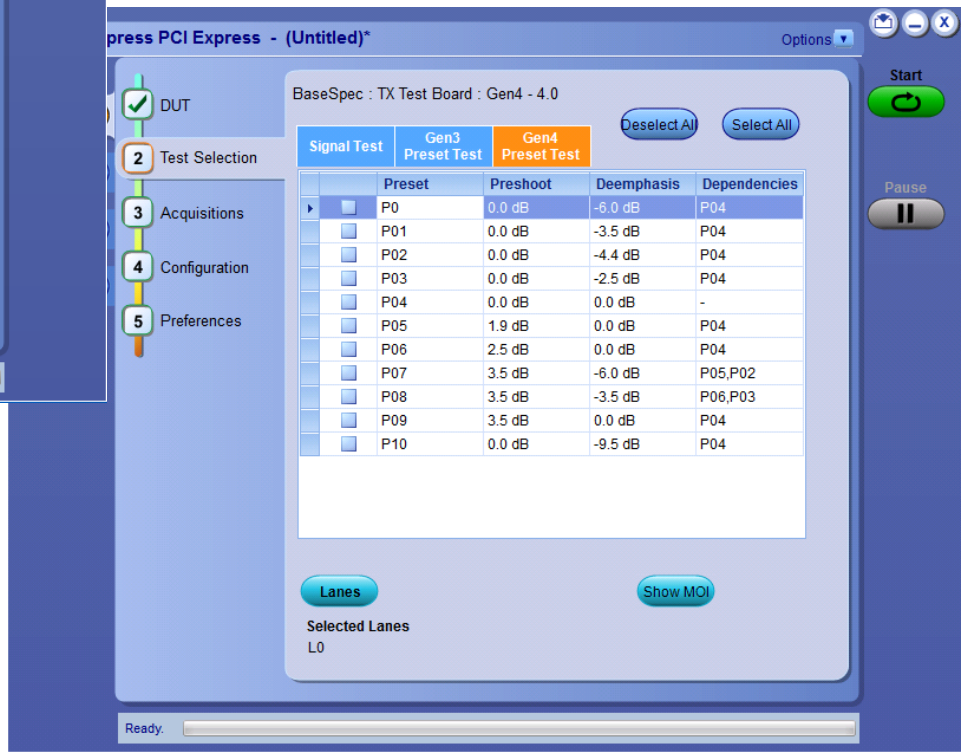


NEW Tx Gen4 Base Automation Solution

via TekExpress Automation Tool



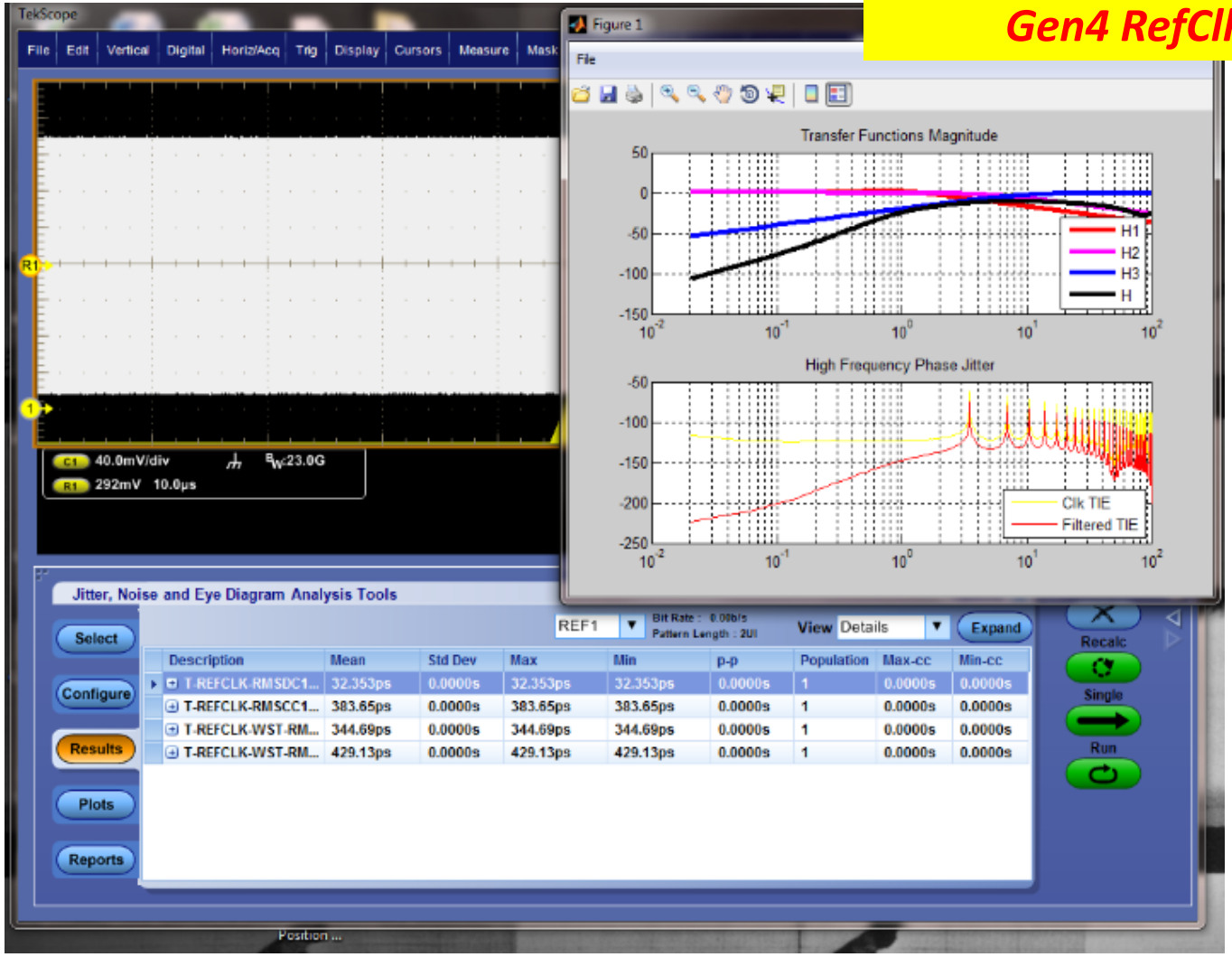
Allows users to perform Gen4 Base silicon automated test and validation per the Gen4 PCIe Base spec, using either SigTest or DPOJET/SDLA characterization tools.
Available through existing **Opt PCE4** for applicable 70K DX and SX scopes



DPOJet for PCIe1/2/3/4 RefClk

MEASUREMENTS

Same as Gen3 RefClk but with Gen4 RefClk limits



PCIe Decoder (Opt SR-PCIe) for Gen1-4

- Decodes and displays PCIe data using characters and names that are familiar from the standard, such as:
  - SKP
  - Electrical Idle
  - EIEOS
- Easily configured through “Bus Setup” under “Vertical” menu with a variety of user-adjustable settings
- Results table shows time-correlated listing of events time-correlated with waveform view
- Integrated search with marks
- **Tek BSX BERTScope protocol/pattern match can be used to cross-trigger scope, which can use SR-PCIe for Tx/Rx link training test and debug**
- **Decoding available for PCIe Gen1-4**
- Serial triggering for debug available for PCIe Gen1-2

16GT/s Gen4 Capable!

Tektronix PCIe Tx Solution

Instrument Needed	
8GT/s:	DPO71254C Minimum Bandwidth: 12.5GHz
16GT/s:	DPO72504DX or DPO73304SX Minimum Bandwidth: 25GHz

AFG3252

SX Scope utilizes patented ATI (asynchronous time interleaving) technology to provide best-in-class noise floor performance including 32GT/s (PCIe Gen5)

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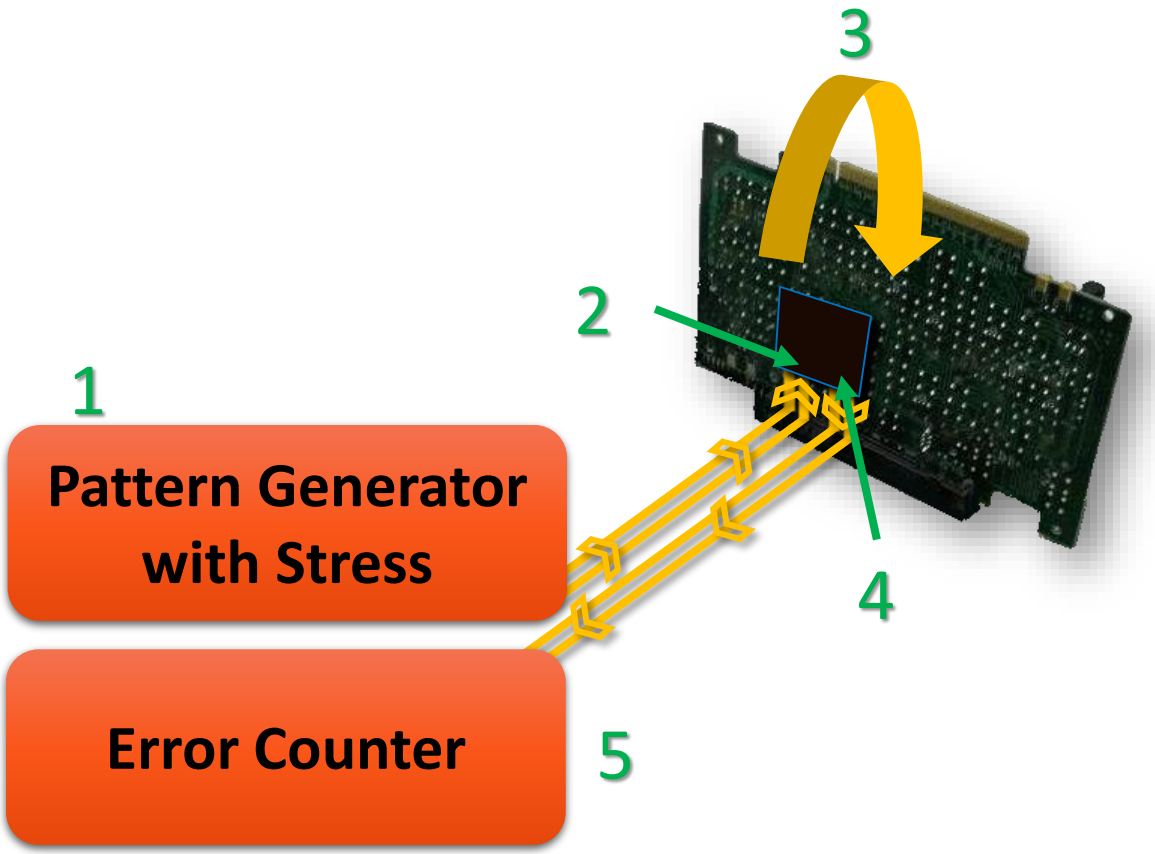
Essentials of Rx Testing

- PCIe 3.0 introduced formal Rx testing
- Based on stress testing of the DUT in loopback
  - Looped back data must be the same as stressed data
- DUT must support loopback initialization and **training**
- Impairments in stress must be **controlled** and **repeatable**
- DUT must receive stressed signals without errors (errors below specified ratio 10^{-12})

Testing Challenges in Rx

- Rx: Support of loopback
  - √ Loopback initialization
  - √ Proper training conditions
  - √ Correct stress and signal impairment levels
- How to achieve required confidence level and beyond?
  - √ Length of test (Rx)

Basics of Rx Testing

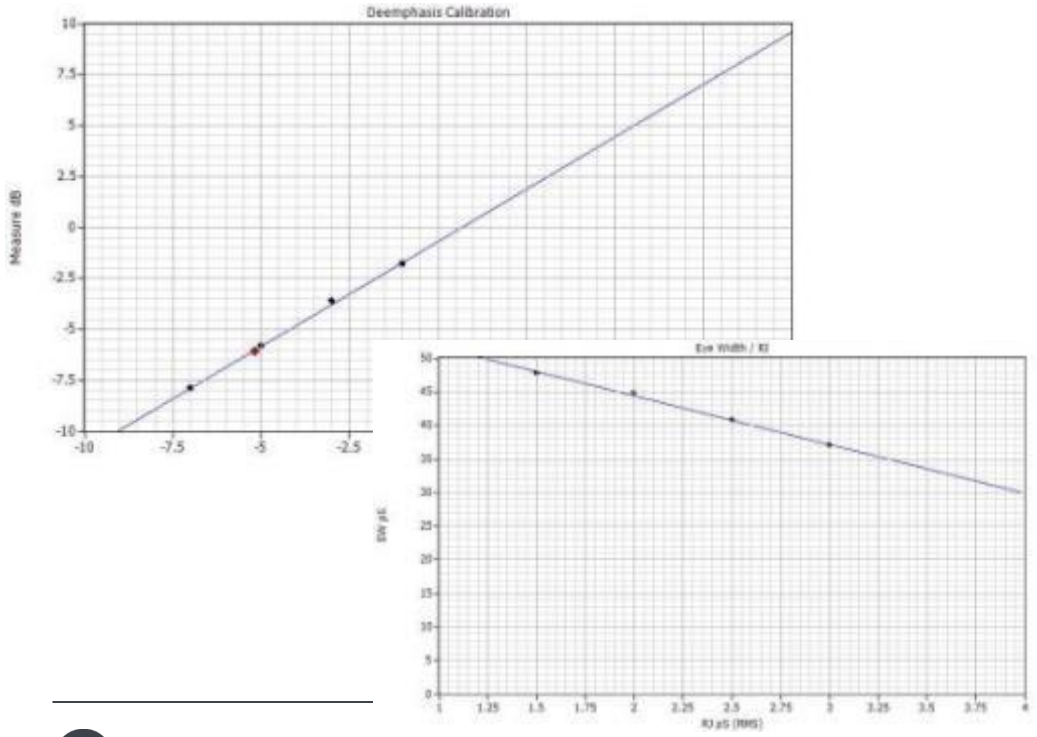


At the simplest level, receiver testing is composed of:

1. Send impaired signal to the receiver under test
2. The receiver decides whether the incoming bits are a one or a zero
3. The chip loops back the bit stream to the transmitter
4. The transmitter sends out exactly the bits it received
5. An error counter compares the bits to the expected signal and looks for mistakes (errors)

BSAPCI3 PCIe 3.0 Automation SW

- Automated calibration, link training, loopback initiation, and testing.
- BER Map feature for TxEQ optimization.
- Reduces the time and minimizes the skill-set required to perform the calibration and testing.
- Increases the reliability and accuracy by removing inconsistencies with manual calibration.



Automated Link Equalization

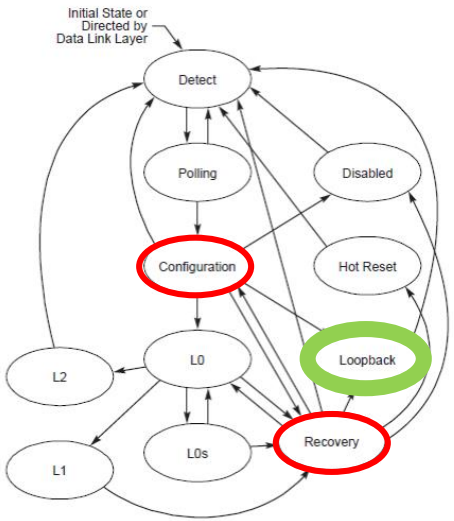
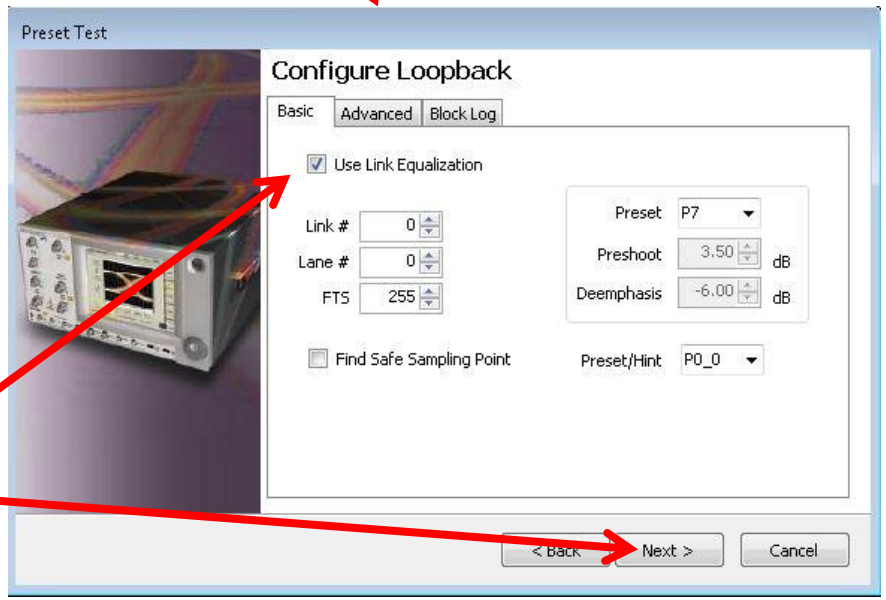


Figure 4-22: Main State Diagram for Link Training and Status State Machine

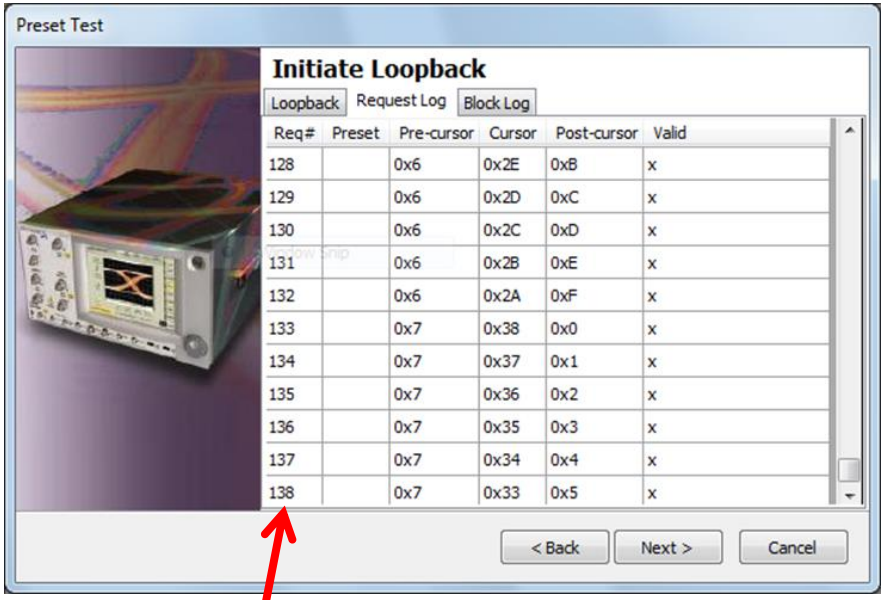
- State diagram from PCIe3 spec
  - Implemented in Tektronix PCIe Rx test hardware and automation software
  - 2 paths to Loopback, either via Configuration or Recovery

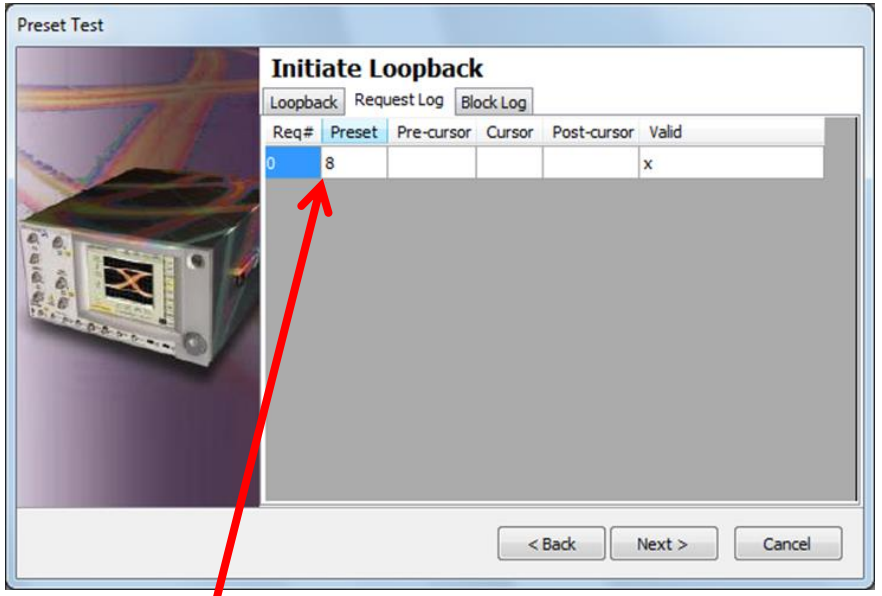


- Set-up for loopback initiation with automated link equalization
  - Step 1: select “use link eq.”
  - Step 2: initiate loopback

Automated Link Equalization

- Loopback results: automation software provides complete equalization request log

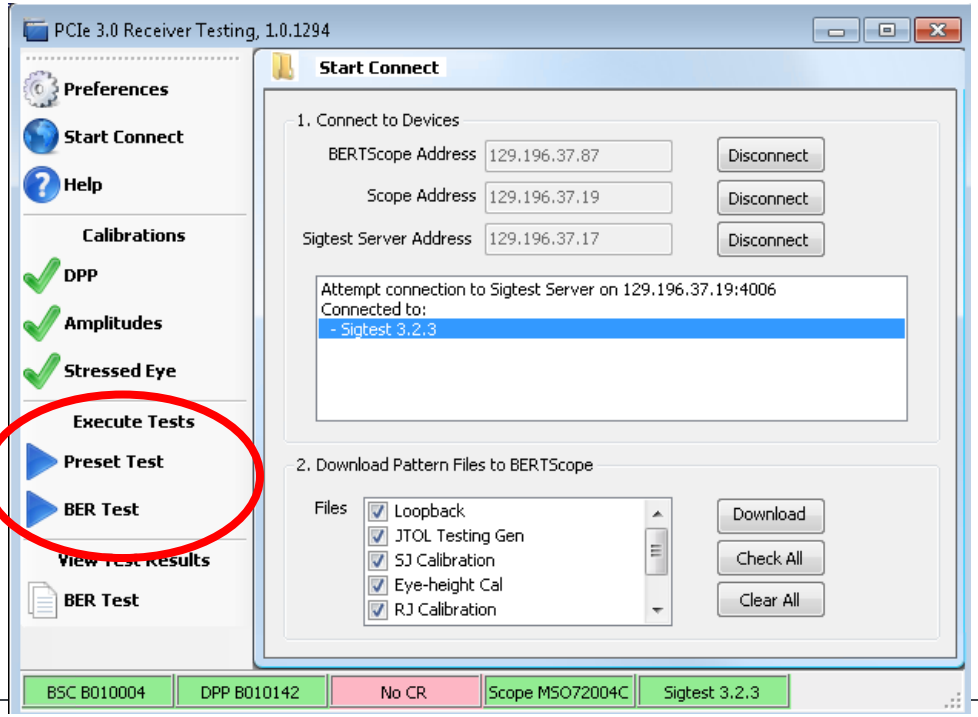




- DUT 1 makes many equalization setting requests
- DUT 2 requests only one equalization preset

Automation Test Options

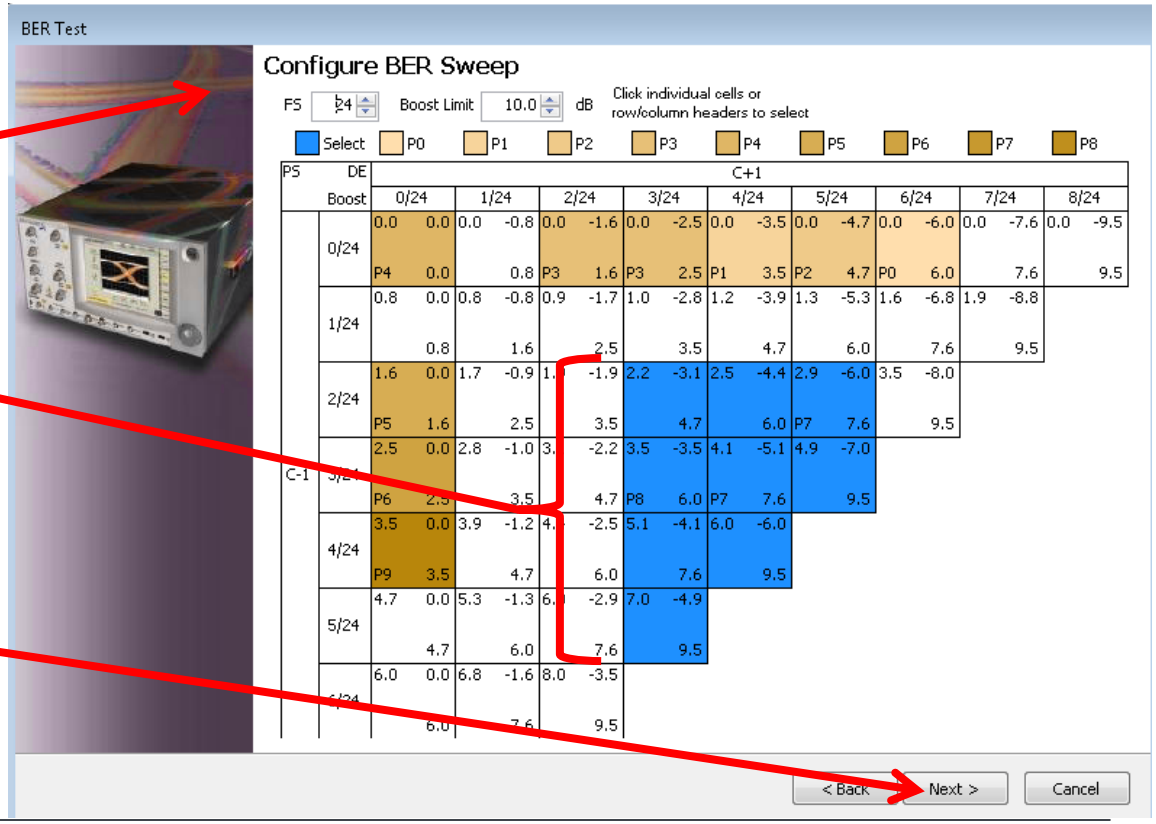
- Automation software provides two options for testing:
  1. “Preset test” uses either negotiated link equalization or user selected preset for test
  2. “BER test” provides the option to test a matrix of preshoot and de-emphasis settings



Automated Tx EQ Matrix Testing

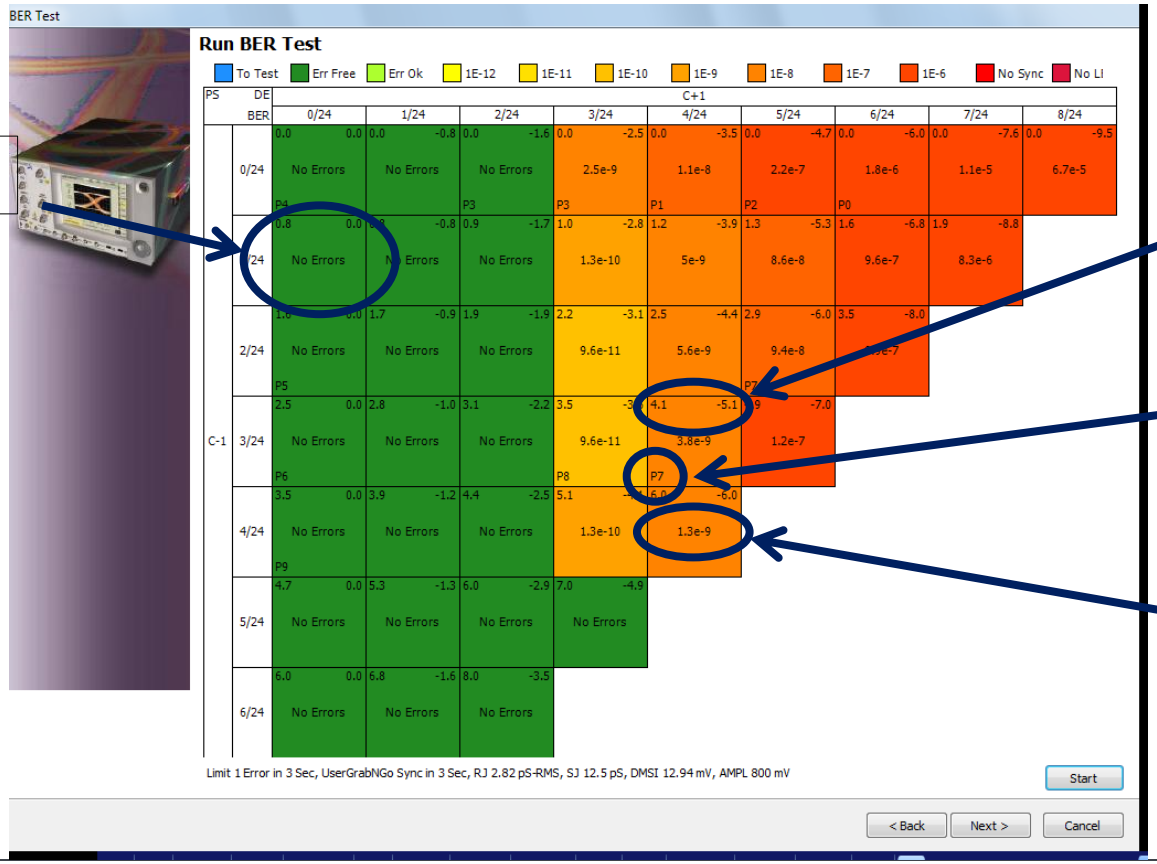
- Automation software “BER test” provides the option to sweep a matrix of pre-shoot and de-emphasis settings
  - Quickly find the range of values that work well with the DUT
  - Ideal for debugging purposes

- Select test matrix resolution
- Click on equalization combinations desired for test
- Initiate test



Automated Equalization Sweep testing

- BER results matrix for preshoot and de-emphasis settings provides an in-depth view of Rx sensitivity to Tx equalization



Green = pass

Preshoot and de-emphasis setting

Equivalent preset number

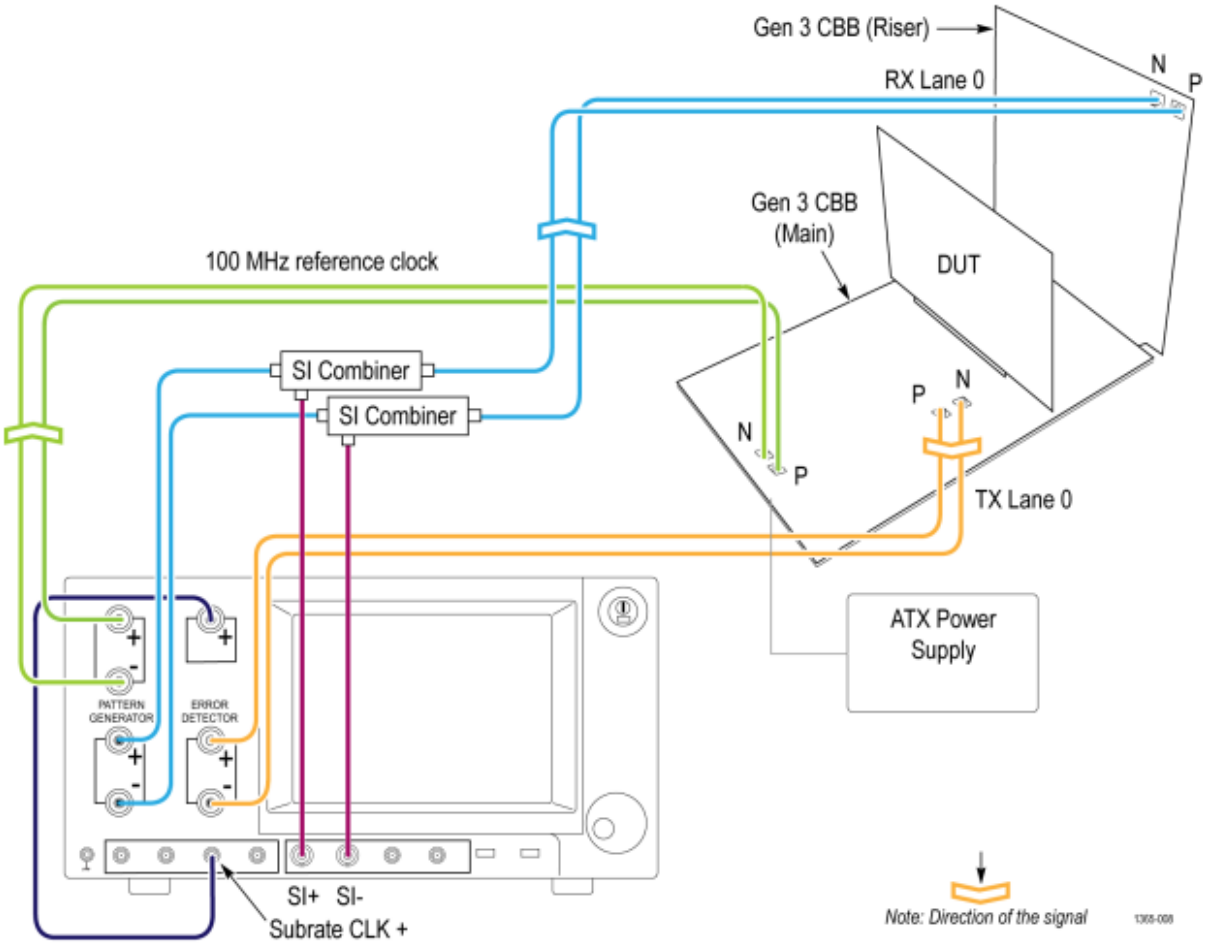
BER result for each combination of preshoot and de-emphasis

Automatic Calibration

- Due to complex test setup and variations in DUTs and test equipment just dialing up the settings on the signal source is not sufficient
- Stress must be measured and adjusted
- Automatic calibration is used to achieve the right amount of stress
- Margin testing complements the compliance testing
  - Help understand your device's margins.
  - How much additional stress does it tolerate?

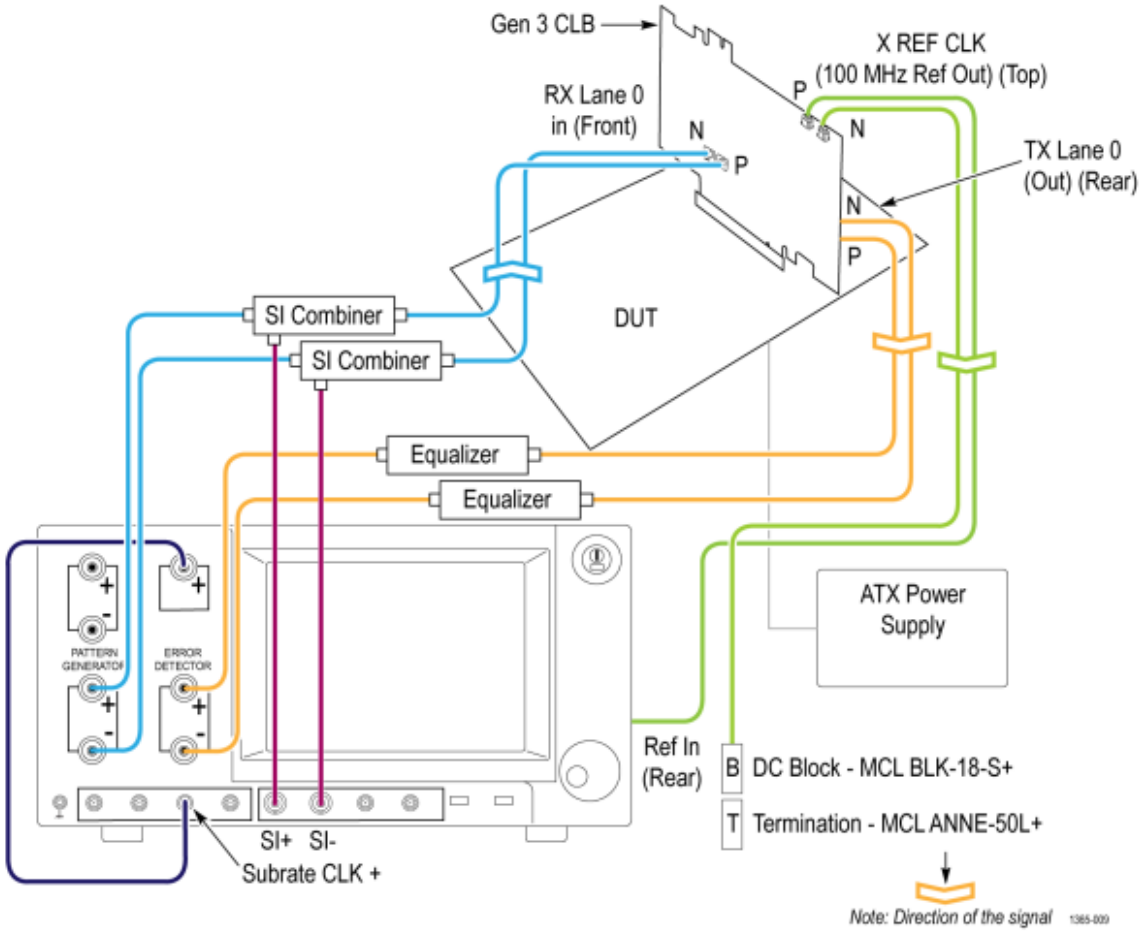
Add-In Card: Rx Stressed Eye Testing

Connect Test Equipment and DUT



Host (System): Rx Stressed Eye Testing

Connect Test Equipment and DUT



Rx Testing Summary

- Certainly the most complex type of testing
  - Due to complexity of equipment and procedures
- Extensive correlation studies in PCI-SIG have helped to streamline solutions
  - Similar stress signals
  - Guided calibration and test execution
  - Good correlation on the latest workshop
- Link Equalization detail and BER test matrix go beyond compliance testing and give visibility into DUT behavior and margins
- Successful Rx compliance and margin test gives you the confidence that the device passes when you get to the workshop

Agenda

1. Market Overview
2. Gen3 Overview
3. Gen3 Tx
4. Gen4 Overview
5. Gen4 Tx
6. Gen3 Rx
7. Gen4 Rx

Challenges of Rx Testing for Gen4 Devices

Requires Protocol Awareness

1. Putting device into loopback
2. Performing Link Equalization

Need Automated Solutions for Gen3 and Gen4 Standards

3. Easy Setup
4. Auto calibration of stresses.
5. Making accurate and repeatable measurements for large number of test cases

Go beyond compliance

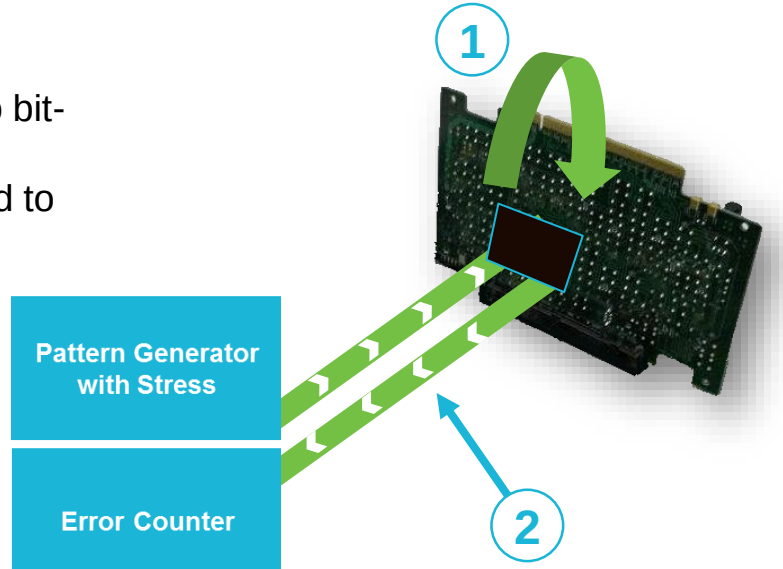
6. Root-causing factors leading to bit-error or link training problems. Uncertain debug times can lead to product development delays.

3

SAS3	SAS4
1. Calibrate ISI for Vpp, eye opening, cal coefficients per standard	1. Run live traffic
2. Calibrate crosstalk source for noise peak-to-peak	2. Ensure test equipment complies with signal specs such as Vpp, impedance, rise/fall, UUGJ, UBHPJ, DCD, and TJ
3. Apply ISI and crosstalk to DUT	3. Calibrate channel to be compliant to worst-case standards (-30dB at 11.25GHz)
4. Run live traffic	4. Load training patterns and train Rx/Tx
5. Load training patterns and train Rx/Tx	5. Configure SJ
6. Configure RJ	6. Configure BERT to transmit PRBS31
7. Configure SJ	7. Ensure that Rx DUT has BER less than 1E-6 with level of 95%
8. Configure BERT to transmit CJTPAT	8. If desired, confirm BER of 1E-15 using FEC
9. Ensure that Rx DUT has BER less than 1E-12 with level of 95%	

6

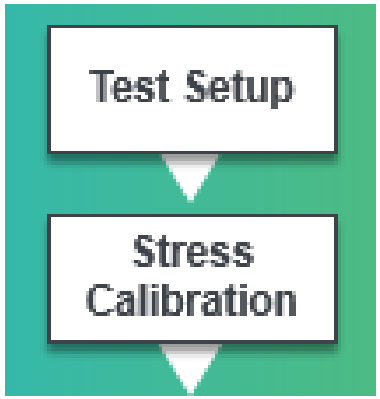
ERROR BIT LOCATION	EXPECTED BIT
200,457	0
1,247,356	1
1,447,890	0
3,885,245	0
4,001,876	1
8,233,191	0
...	



Simplify equipment setup for RX test

NEW BSX-SERIES OUTPUT STAGE WITH BUILT-IN 4-TAP TXEQ

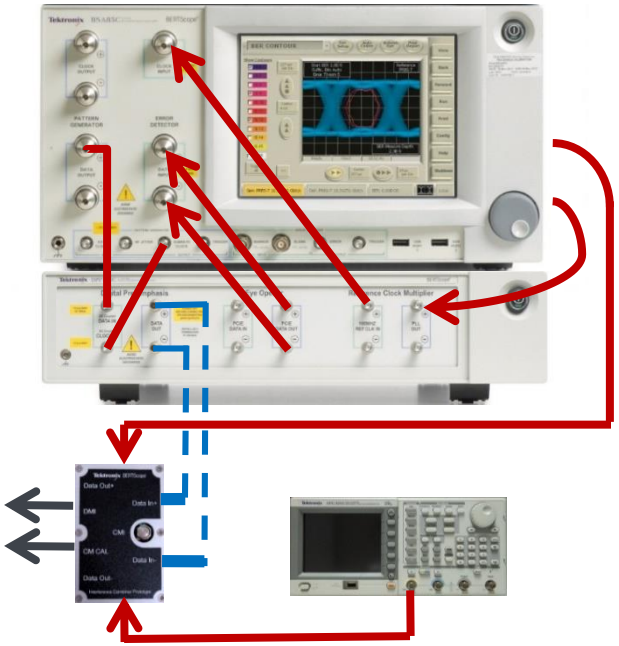
- Internal 4-tap digital de-emphasis processor
  - Replaces external module and simplifies test interconnects
- Tx equalization operates up to 32 Gb/s
  - A single instrument supports TXEQ for the broadest range of standards
  - No external mux-demux required at any data rate
- Supports in-band link training handshaking beyond 16 Gb/s
  - Sub-500ns response time provides compliant timing for PCIe Gen3/4/5
  - Supports DUT handshaking for SAS4 @ 22.5 Gb/s and beyond



No Mux/Demux add-on is required for operation up to 32 Gb/s. A single BSX configuration is all that is required for current and upcoming Rx test requirements, including PCIe Gen5

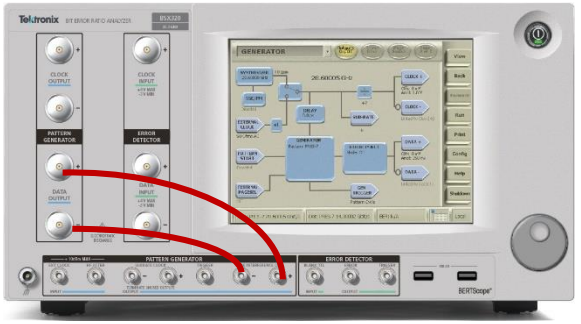
Simplify equipment set-up for RX test

Current BERTScope Gen3 BASE Solution



Drop two boxes and 6 external cables

BSX-series BERTScope Gen3/4 BASE



Reducing the box count saves time by simplifying test set-up and calibration time

Simplify getting the DUT into the proper test condition

- Loopback: complete the handshaking sequence required to put the device in loopback mode
  - BSX series supports handshaking for a broad range of standards beyond 16 Gb/s
  - Provides feedback into current status of loopback state machine for quick confidence

- Link training
  - Performs handshaking with DUTs to support equalization link training to optimize the TX equalization prior to performing tests

Provide unprecedented DUT handshaking flexibility

- Goal: Allow customers to create their own protocol-based patterns and link state traversals via stimulus-response feedback (protocol handshaking)
- Key protocol features support debugging and proprietary standards:
  - Bit-oriented and protocol-oriented memory sequencer
  - Real-time data processing at 32 Gb/s
  - User defined stimulus-response feedback (handshaking)
    - User-defied Detector protocol pattern match -> Generator sequence advancement
    - Detector can match up to 16 user defined blocks.
    - Stimulus/response trigger output allows cross-triggering of scope

Flexible handshaking enables support for proprietary protocols and creation of protocol message test cases for debugging.

Memory Sequencer – Protocol-Aware Mode

- In Protocol-Aware mode, pattern memory words are treated as protocol blocks or groups of symbols instead of bits.
- Words are fetched from memory and processed according to the selected protocol or encoding including:
  - Packaging of symbols into protocol blocks
  - Symbol encoding (ex: 8b/10b)
  - Data scrambling (all protocols)
  - DC balancing (PCIe Gen3/4, USB 3.1 SSP)

No need to find protocol experts to create protocol-compliant test patterns.

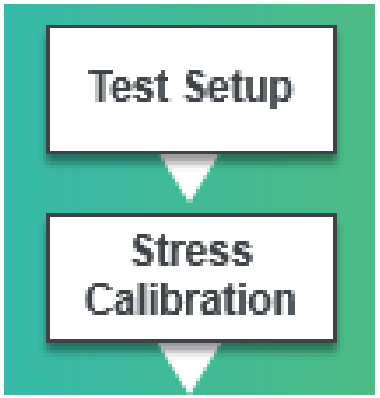
Reduce debug uncertainty

- Time-correlated and flexible eye diagram
  - Diagnose detector input issues with one click
- Knob-based control supports quick parametric changes
  - Quickly identify DUT limits
- User defined handshaking allows rapid debug of DUT configuration issues
- Error Location Analysis provides unique visibility into the underlying cause of errors
- Forward Error Correction Emulation option provides before and after correction BER
  - Test-drive FEC codes against actual error patterns

Failing DUTs lead to schedule slips. BERTScope debugging tools can help keep schedules on-track.

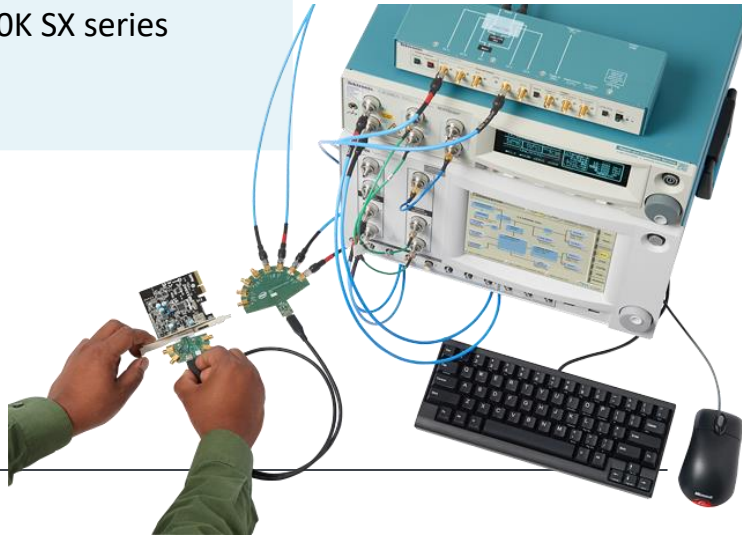
Simplify equipment set-up for RX test

- Automation solutions to provide test configuration and calibration support for a broad range of standards:
  - PCIe Gen3 and Gen4
  - USB 3.1 Gen1 and Gen2
  - DisplayPort
  - Thunderbolt
- Configuration Wizard simplifies instrument set-up
- Automation of both scope and BERT to provide quick and accurate calibrations



BSX series models and applications

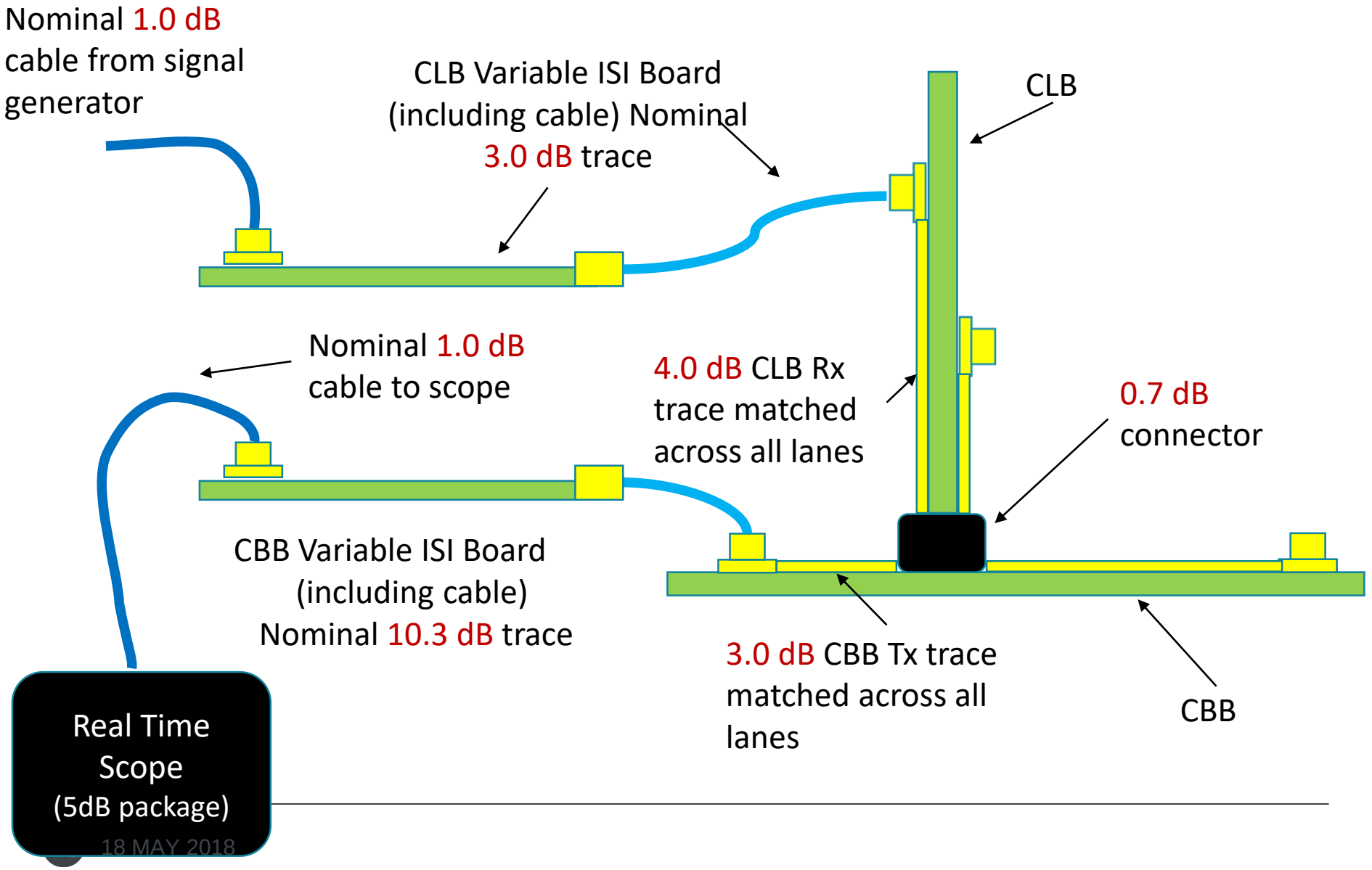
	Legacy Standards USB 3.1, SAS3, PCIe3	Gen4 Standards PCIe Gen4, SAS4, Thunderbolt	25-28G and future standards up to 32 Gb/s
BSX125 BERTScope up to 12.5 Gb/s	✓		
BSX240 BERTScope up to 24 Gb/s	✓	✓	
BSX320 BERTScope up to 32 Gb/s	✓	✓	✓
Recommended Tek Scope for RX stress calibration	70K DX series	70K DX series or 70K SX series	70K SX series



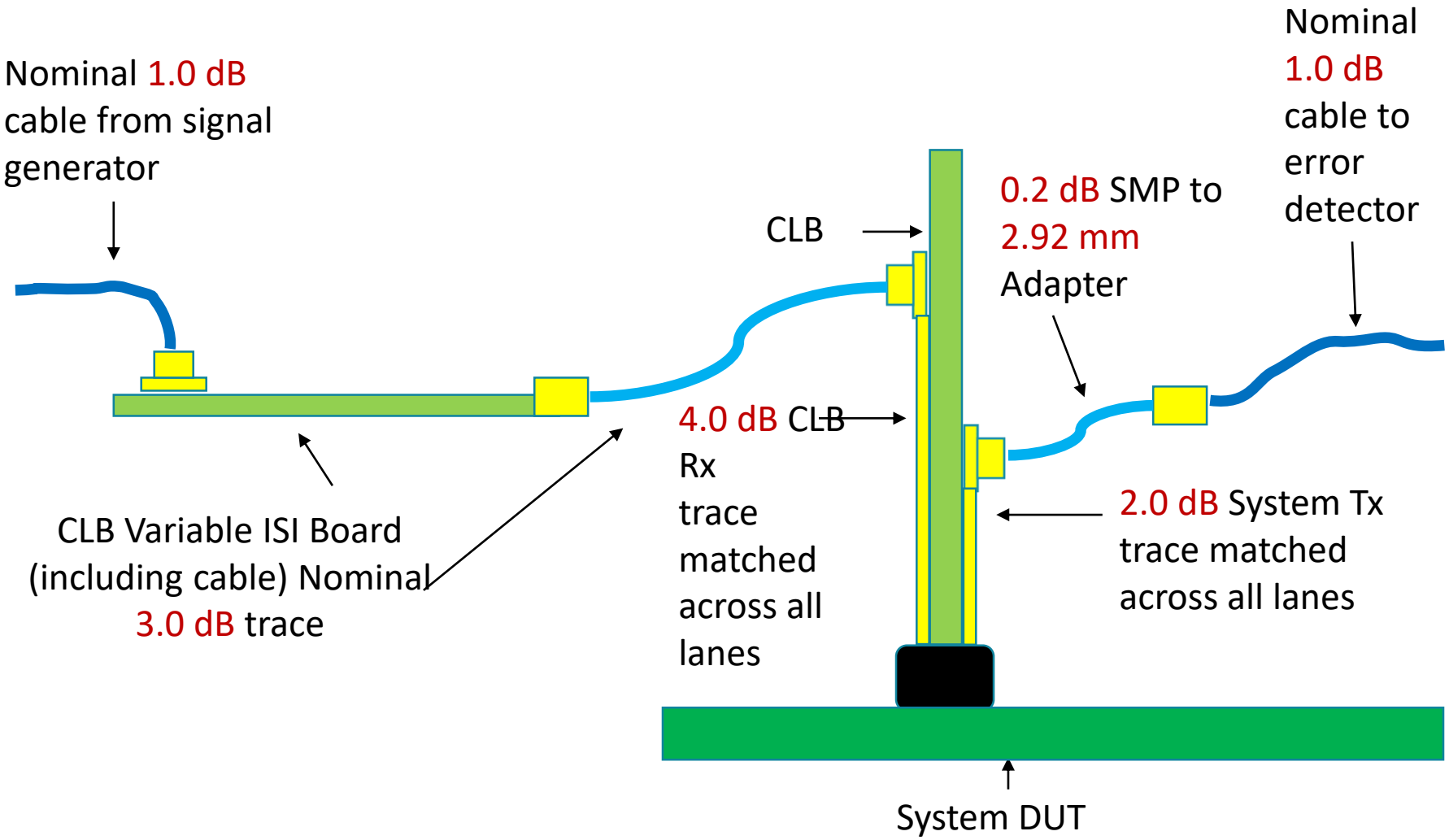
Additional hardware changes & features

- Built-in programmable reference clock multiplier
  - *Provides clocking flexibility to support a broad range of forwarded clock configurations. Eliminates the need for external multipliers*
- Maximum phase modulation frequency increased to 4 MHz
  - *High amplitude SJ over a broader frequency range allows stressing DUT to it's limits*
- 50 mV to 1.8V (single-ended) output amplitude
  - *High dynamic range supports extended receiver sensitivity testing without attenuators.*
- Built-in two channel interference synthesizer
  - *More flexibility for inserting two interference tones (CM+DM, DM+DM, CM+CM) means more ways to stress your receiver*
- BSX-series is code compatible with BSA-series
  - *Preserves automation investment for current BSA users*
- Direct detector clock input
  - *Ability to bypass a CR in the TX path means more accurate results in Data Clocked Refclock configurations*

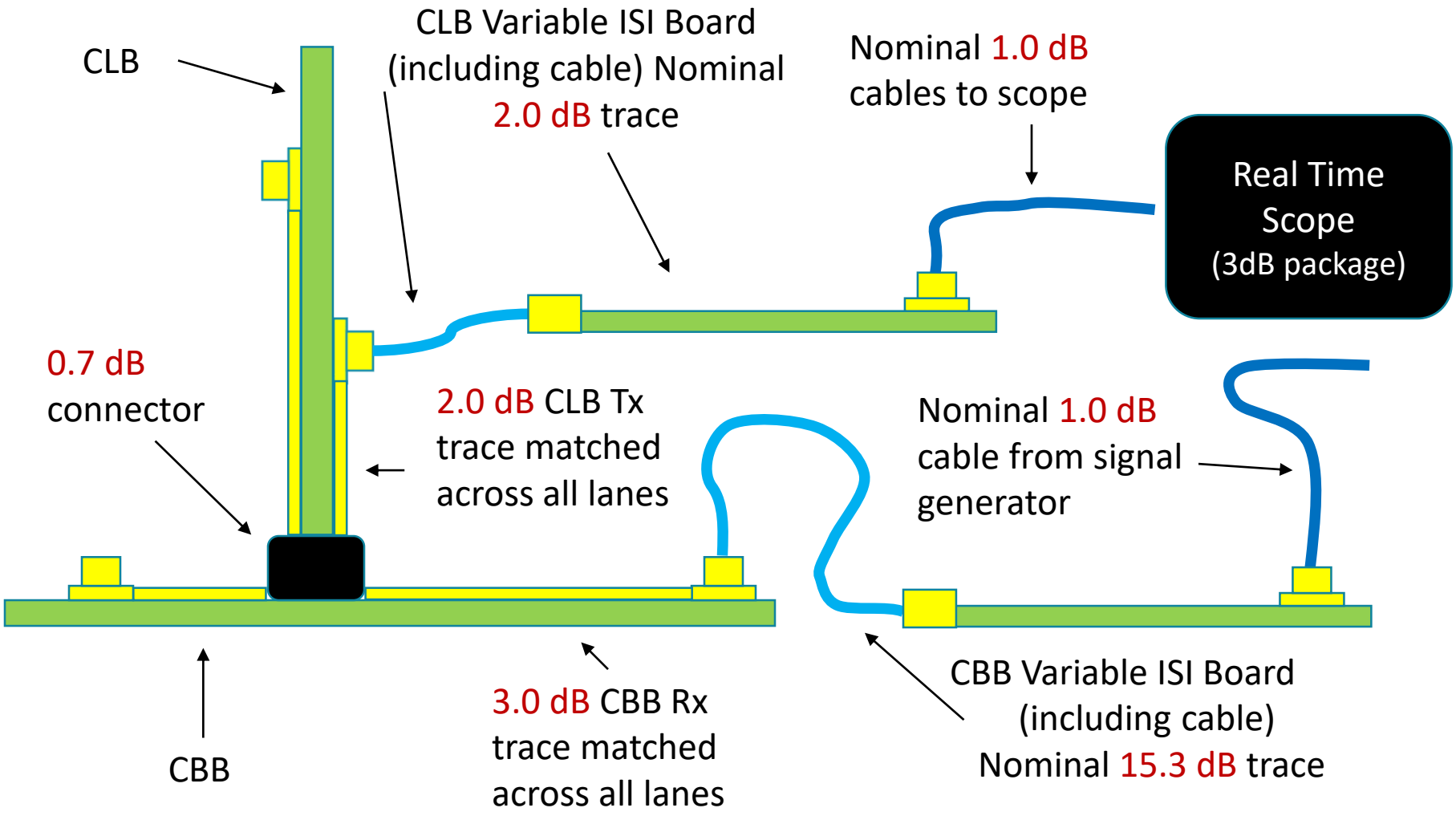
Gen 4 System Rx Calibration



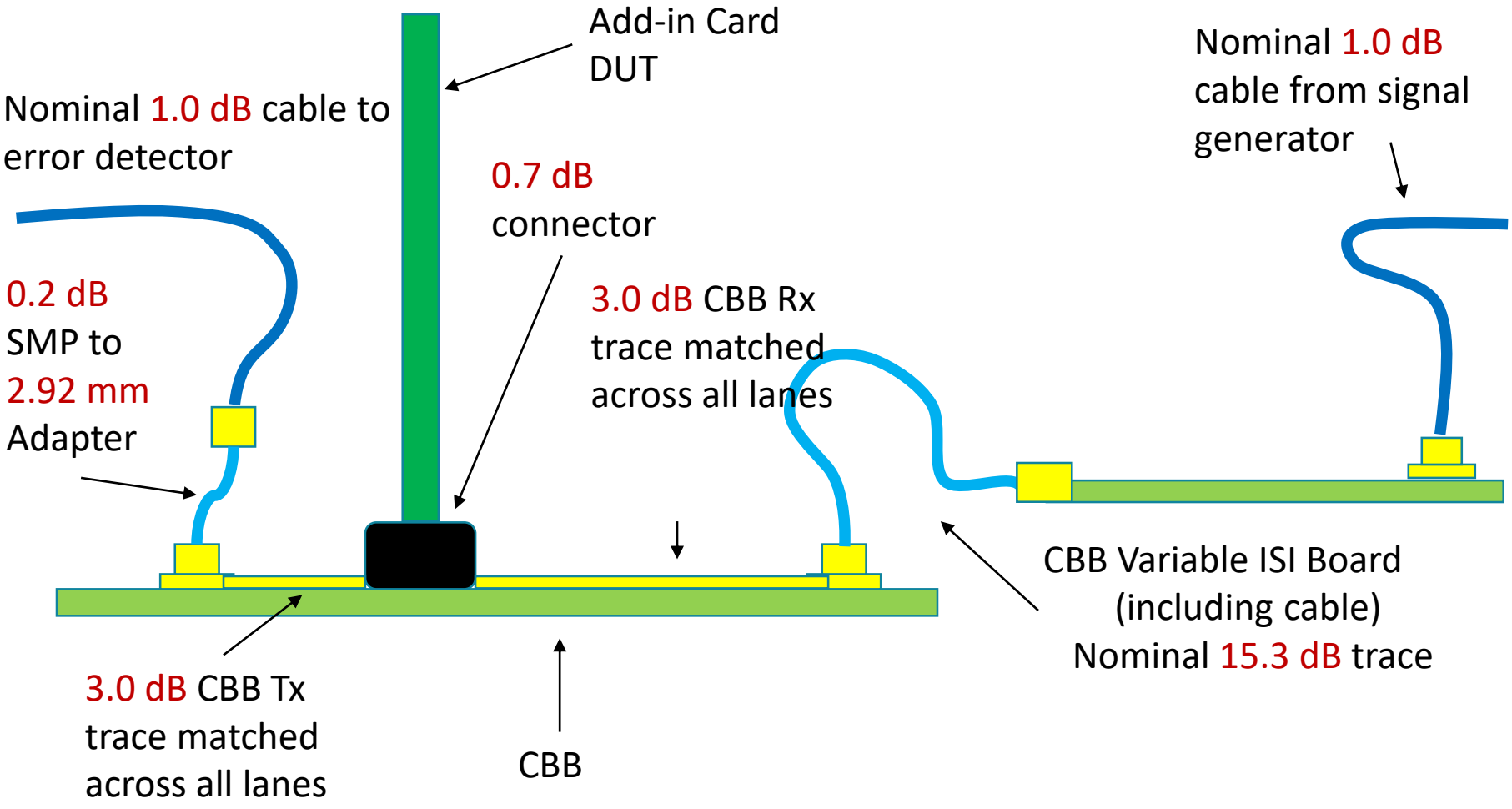
Gen 4 System Rx Test



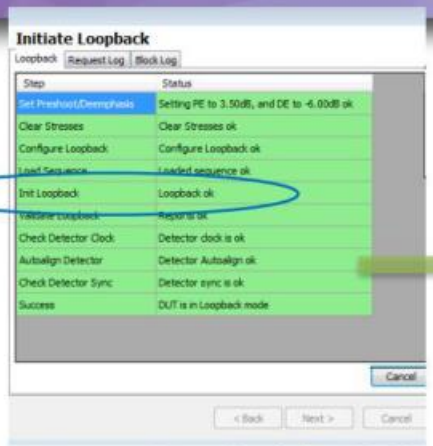
Gen 4 Add-in Card Rx Calibration

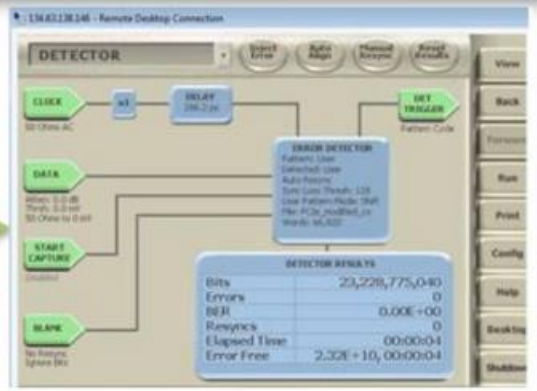


Gen 4 PCIe Add-in Card Rx Test



Compliance Workshop Use Case—PCIe 4.0 Broadcom AIC DUT





Sequencer Loaded for PCIe Loopback Initiation and Debug—PCIe 3.0 -> PCIe 4.0

Iterative requests from the DUT for TXEQ tuning

LTSSM Recovery loopback achieved and BER SJ stress test initiated

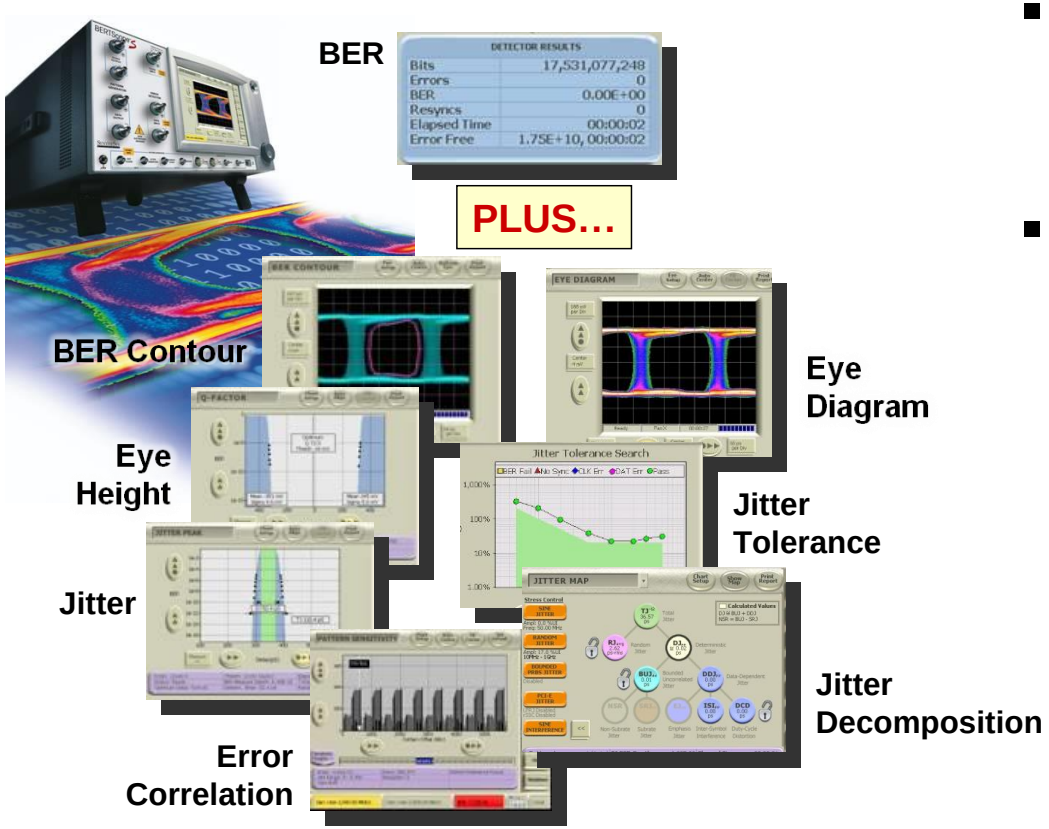
Special thanks to Broadcom Ft Collins team for their collaboration!

BERT Debug tools observed protocol traffic to identify handshaking issues

DUT initial preset was modified based on feedback from BERT to facilitate LTSSM Recovery loopback

Beyond Compliance: BERTScope Analysis Tools

- Besides being a BERT, the BERTScope's **"Scope" functionality** brings benefits that complement those of the Tektronix scopes
- Analysis tools are full featured and easy to use



- **Eye diagram for quick diagnosis** of synchronization and BER failure issues
- **Debug** challenging **signal integrity problems**
  - Error Location Analysis
  - Pattern Capture
  - Jitter Map
  - BER Contour

Bertscope的调试分析功能

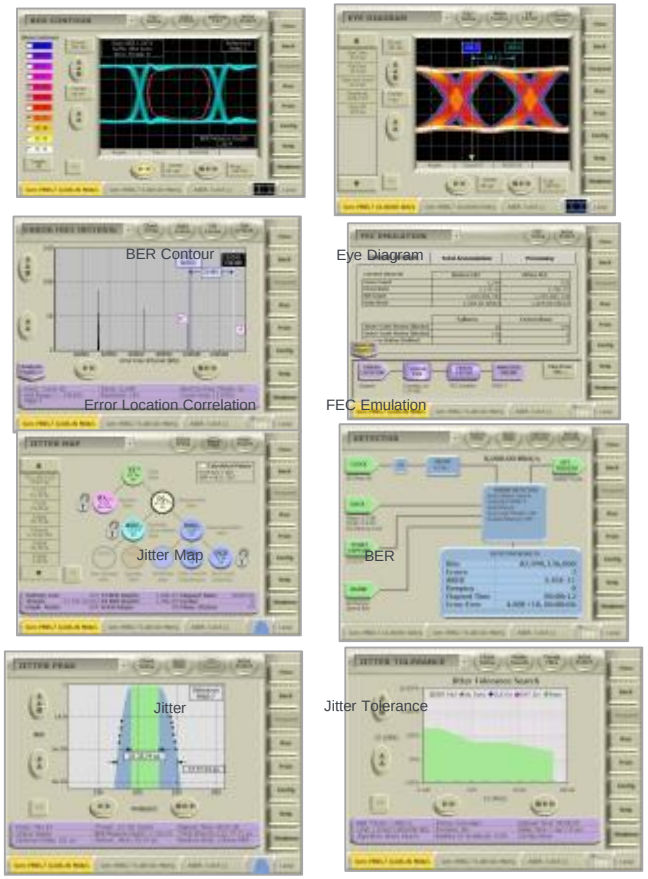
BERTSCOPE ANALYSIS TOOLS

User Challenge:

- Need more than a bit-error rate (BER) number
- Need to understand factors leading to bit error problems in order to debug issues

BSX Series BERTScope provides:

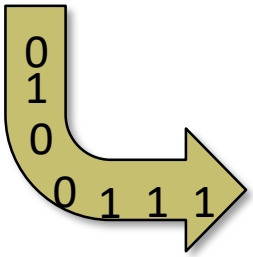
- “Scope” functionality that complement those of the Tektronix scopes
- Full-featured and easy to use analysis tools
- Eye diagram for quick diagnosis of synchronization and BER failure issues
- Debug challenging signal integrity problems
  - Error Location Analysis
  - Pattern Capture
  - Jitter Map
  - BER Contour
  - FEC Emulation

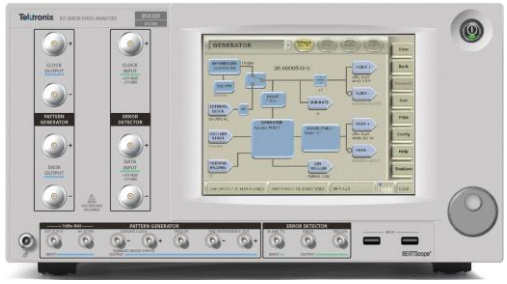


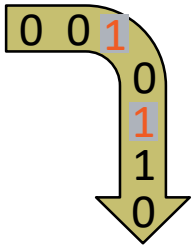
Only with Tek can you obtain Rx failure insight using BERT error location analysis

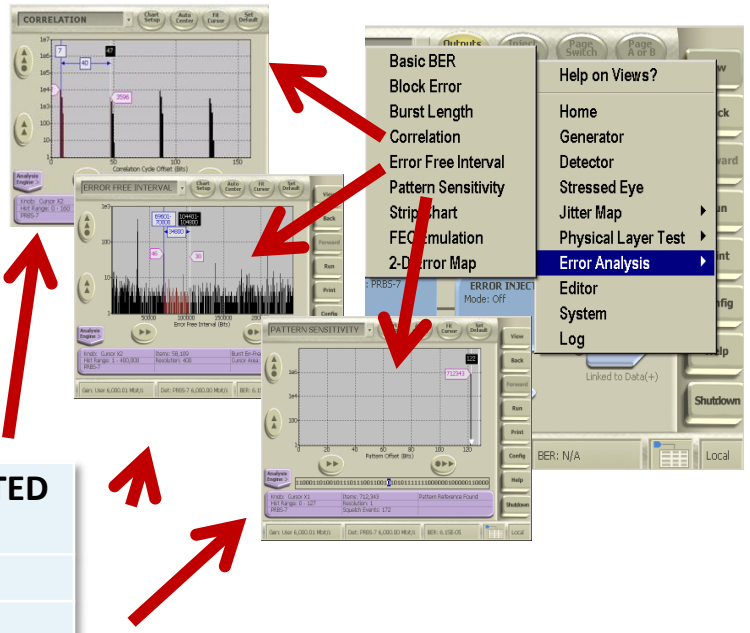
物理层调试分析功能

只有泰克提供了错误位置分析功能









BER = 3.9×10^{-9}

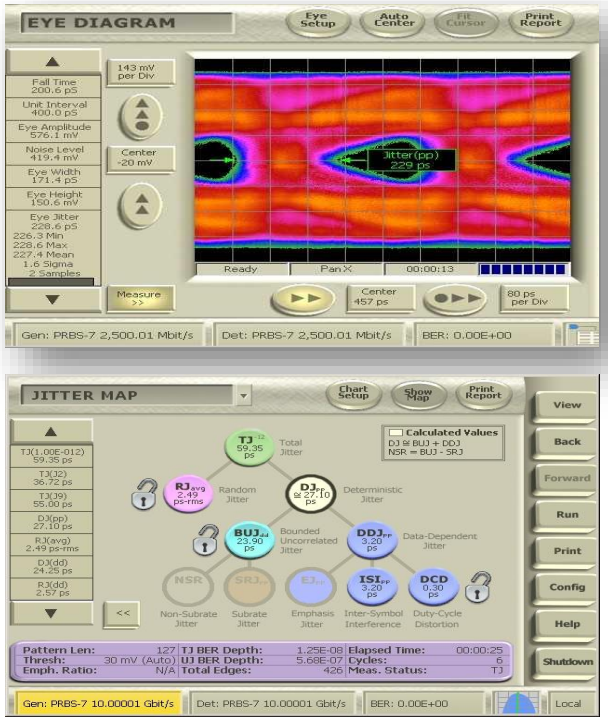
ERROR BIT LOCATION	EXPECTED BIT
200,457	0
1,247,356	1
1,447,890	0
3,885,245	0
4,001,876	1
8,233,191	0
…	

- BERTScope记录每个误码的确切位置:
  - 错误位置 → 错误码型 → 独特的调试信息
  - FEC仿真提供了前向纠错前和前向纠错后的BER

Bertscope的调试分析功能

Bertscope对于抖动和眼图的分析能力：能够对高速信号准确的进行抖动和眼图分析。

1.Bertscope能够精确的测量信号输出的总体抖动，我们一般上称为Tj(Total jitter),Tj一般是用来衡量芯片的信号输出的最重要的指标。由于Tj定义为10^12次方的比特下的抖动值，只有误码仪能够准确测量连续的10^12比特下的抖动，而传统的示波器由于存储深度的限制，都是测量10^5-10^6下的抖动，然后通过各种算法去推算10^2次方下的抖动的，并不是真正测试出来的.

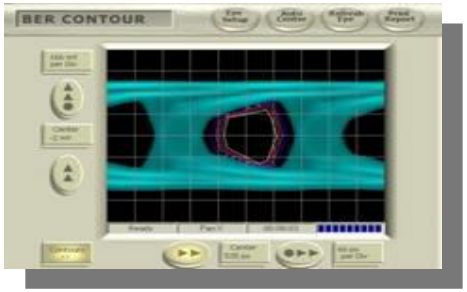


2.Bertscope能够对信号的抖动成分进行分离，可以分离出信号里面的Sj,Rj,DDj等等，供调试者能够知道信号的抖动成分来至于哪一方面。并且能够根据抖动的特性描绘出抖动浴盆曲线。

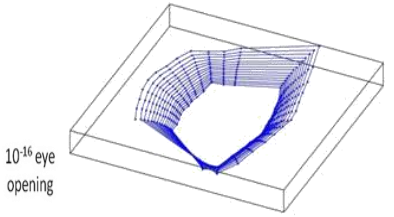
3.Bertscope能够分析出抖动频谱，供调试者分析抖动来自于那个频率，以快速的查找干扰源。

Bertscope的调试分析功能

4.对于眼图测试Bertscope能够快速的描绘出信号的眼图，由于Bertscope采用两个非常精确的采样头，所以能够实现精确快速的眼图测试。其眼图测试结果与实时示波器和采样示波器有非常好的一致性。速度比它们要快5-10倍。当然眼图测试也支持标准的通信模版和用户自定义模版。

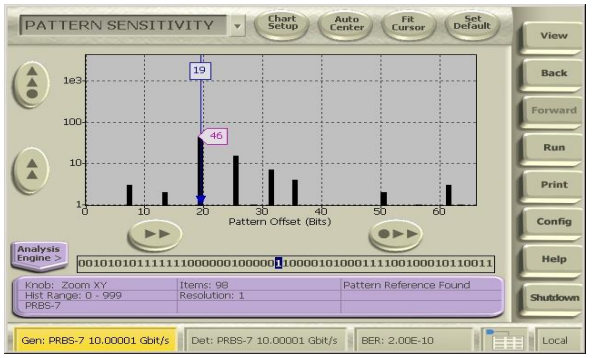


5.由于Bertscope的采样头可以在水平和垂直方向任意精确可调，所以Bertscope能够描绘误码率等高线图，可以从三维的角度去看信号由于样本数量的增加劣化的程度，而示波器一般只能从水平方向去看信号的劣化程度

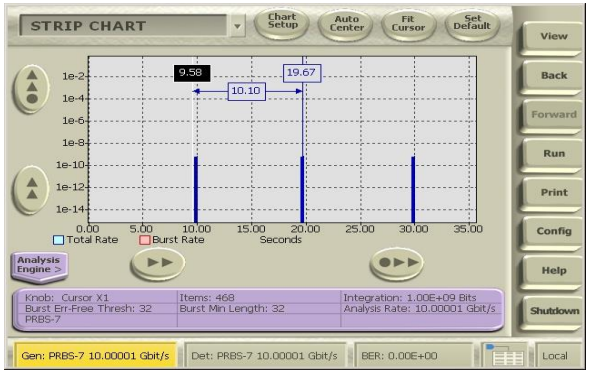


Bertscope的调试分析功能

1.Bertscope Pattern sensitivity 能够定位PRBS里面每一个出现误码的比特，并告知其除于PRBS中的哪一位，比如PRBS7的信号出现误码的时候，可以定位出其是第22位还是第23位出现误码，并统计出每一个位出现误码的数量。

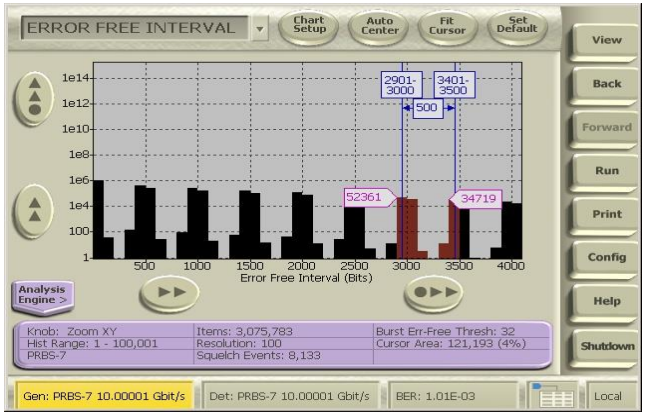


2.Bertscope的Strip Chart分析能够追踪长时间老化测试的时候每个误码出现的准确时间，并统计误码在不同时间里出现的数量。比如24小时不间断的高低温老化测试，误码仪能够统计出误码是出现在那个时间点，误码是间隔出现还是连续出现，都能够准确统计追踪出来。可以观察误码随温度的变化而变化的情况，判断温度高低对系统稳定性的影响。

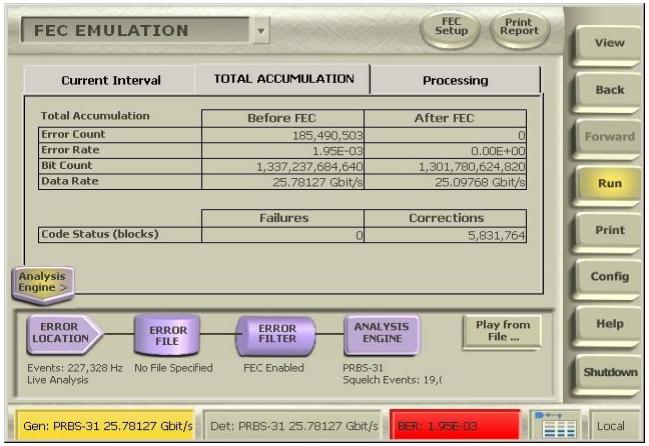


Bertscope的调试分析功能

3. Bertscope Error free interval 的误码分析功能能够分析误码出现的时间及其规律（即是误码间隔出现的频率），根据时间规律则可以推算出引起误码的可能原因，比如电源纹波或者噪声引起芯片工作不稳定引起的误码，这这个误码间隔的频率必然与电源的变化频率相关。如果是其他高速信号的串扰引起的，必然与串扰源有关。



4.FEC emulation的功能能够模拟芯片的输出经过长链路后，通过接受端芯片FEC纠正后能够修正的误码率，客户在做链路的调试的时候不需要搭建这个发送和接受的整个链路环境，只需要将链路的发送连接到误码仪的输入端即可，可以节省大量的时间快速的验证在进行发送端参数修改后的效果，经过用户的多次验证，其结果与真正的芯片接受后进行FEC修正后的效果在误码率的量级上非常一致。

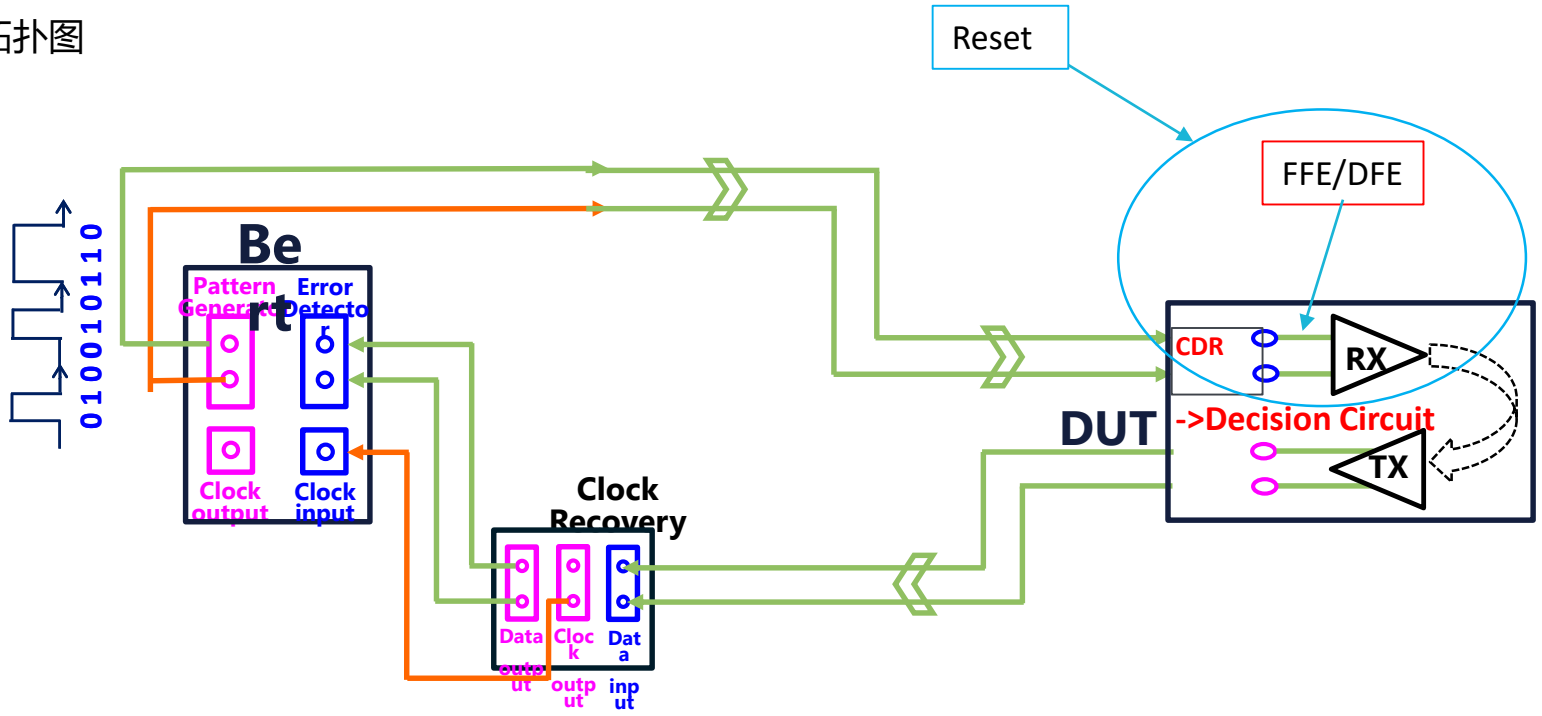


客户实际应用案例-误码分析功能

- 芯片自适应响应时间测试
- 芯片FEC模拟
- 长时间误码率老化测试

芯片的自适应时间测试

连接拓扑图



测试目标参数和方法

- 芯片的接收端的CDR,FFE/DFE的自适应时间：涉及到芯片的时钟恢复的锁定时间，FFE、DFE的自动调节时间，一般为几百微妙到几百毫秒补不等。

- 1.先按照第一页的连接图连接好，将被测芯片设置为环回模式，设置Bertscope的PG输出为被测速率，码型设置为PRBS31，确认泰克CDR模块可以正确锁定，Error Detector能够正确的Sync码型，并且测试没有误码。记得要将ED端设置为Auto-resync。

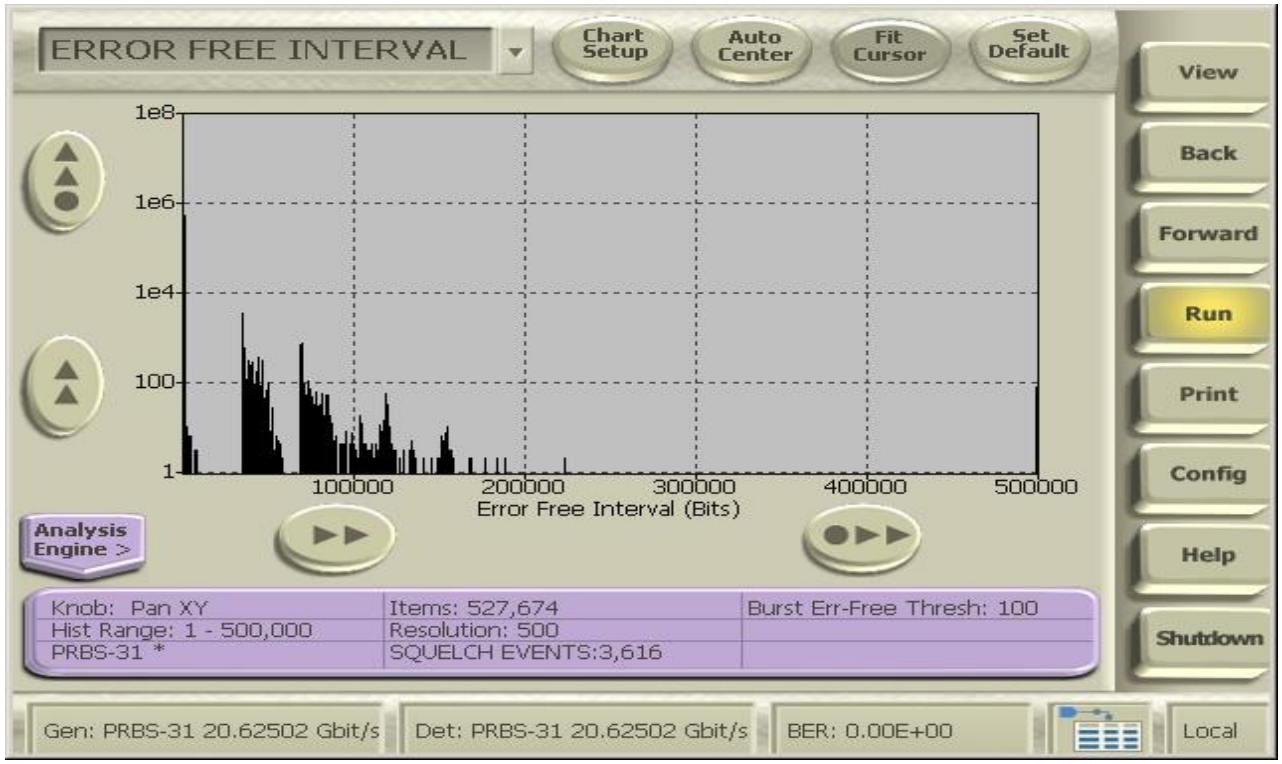
- 2.点击View里面的Error analysis，选择Error free interval。点击Error free interval界面，设置,Hist的end 为500000(bit)，这个参数需要根据芯片的特性灵活调节，如果芯片的自适应时间较长，则可以适当增加，以保证整个自适应过程的误码变化情况都能够在所选的时间范围之内。这个界面的横轴是bit，可以根据信号的速率转化为绝对的时间，纵轴是误码个数。我们可以根据误码的变化从而计算出自适应的收敛时间。设置好以后点击auto center。然后点击Run。

测试目标参数和方法

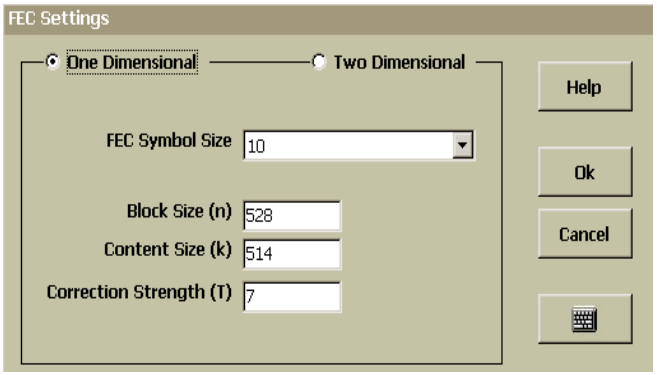
- 3.设置好误码仪后，用命令将芯片的RX部分进行一次hot reset，这时候芯片会进行一次时钟恢复的同步，重新调节DFE，FFE，在Bertscope的Error Free interval里面就可以看到出现大量误码然后在慢慢减少到没有误码的过程。在300000bit左右就不再出现误码，我们认为这个时候自适应过程就已经完成。为了保证测试结果的重复性和一致性，建议将这个hot reset的过程做十次，Error free interval会自动将这十次的结果进行叠加。从测试的结果看，芯片的自适应时间约为300000X(1/20.62G)约为15us左右。

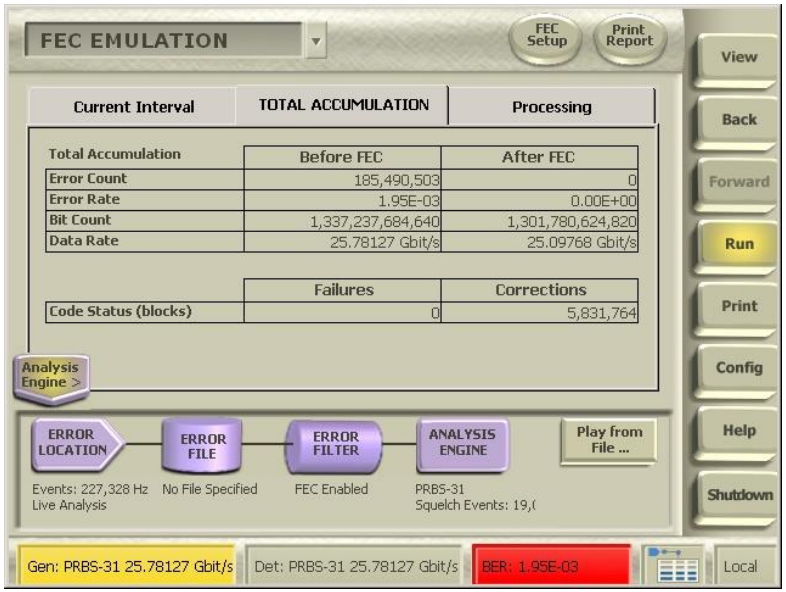
误码分析功能应用：

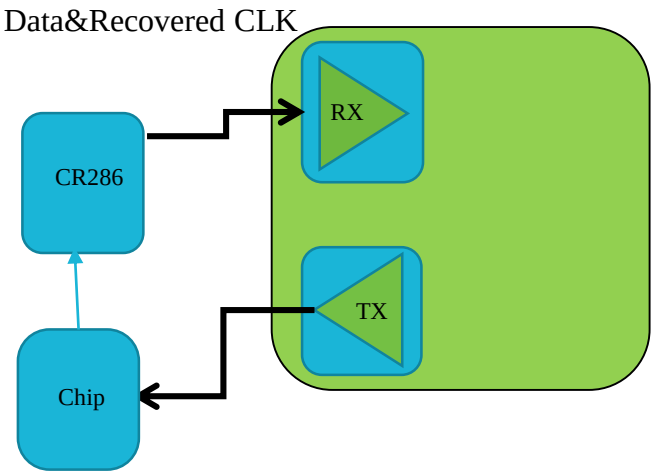
使用Error free interval的功能来测试芯片的自适应时间



误码分析功能应用-FEC emulation

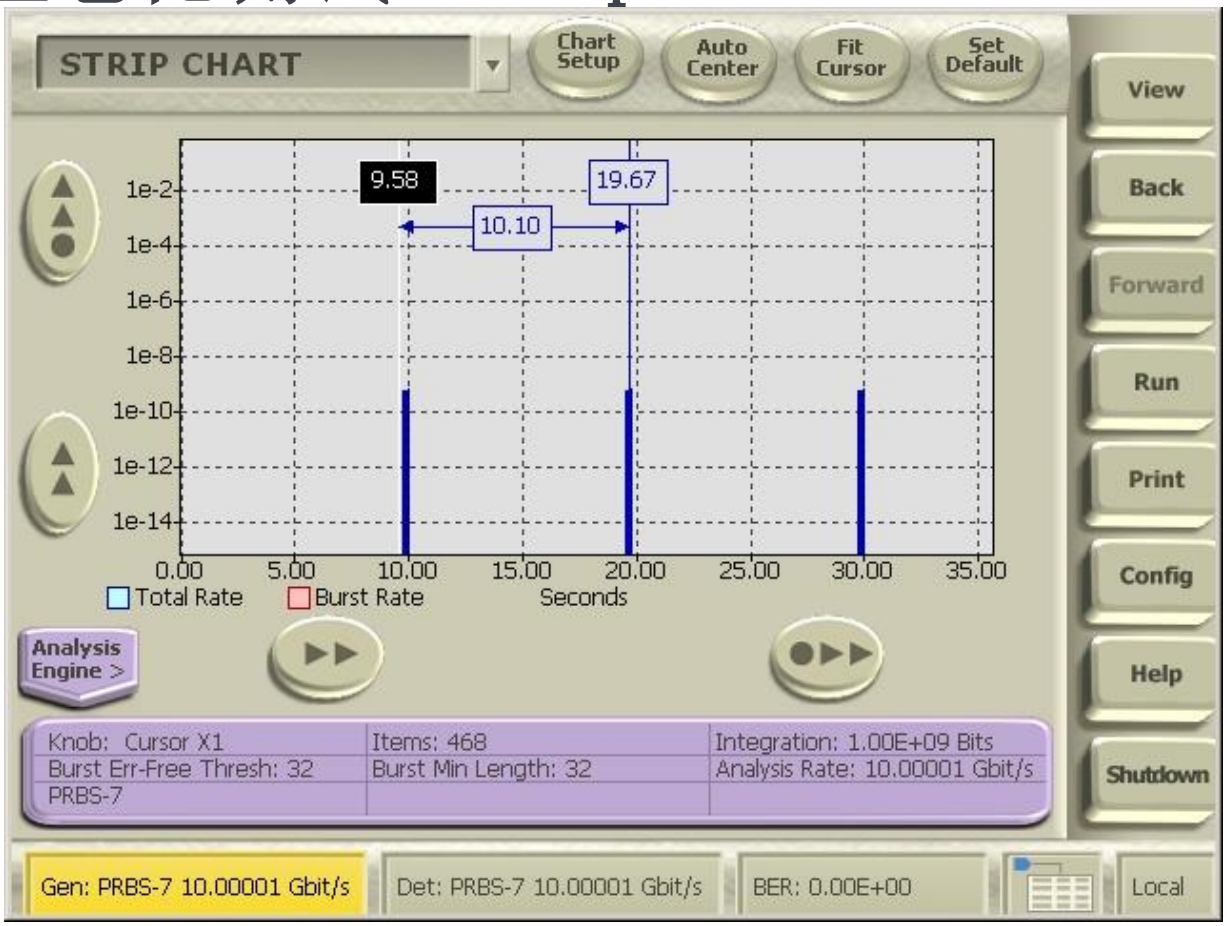






Tx setting:
25.78125Gbps
PRBS31 pattern
1V differential output
Rx setting:
Auto pattern and resync

误码分析功能应用：
高低温老化测试-strip chart



Tx PLL Loop Bandwidth & Peaking

	2.5 GT/s	5 GT/s [1]		8 GT/s	
Loop Bandwidth (MHz)	1.5 – 22	8 - 16	5 - 16	2 – 4	4 – 5
Peaking (db)	0 - 3	0 – 3	0 - 1	0 – 2	0 -1
		[1] - PLL Test software implementation is 5-8 MHz LBW, allowed 0 – 1 dB peaking. Above 8 MHz LBW, allowed 0 – 3 dB peaking			

Excerpt from PCIe Base Specification 3.0 detailing Tx PLL requirements

4.3.3.12. Transmitter PLL Bandwidth and Peaking

4.3.3.12.1. 2.5 GT/s and 5.0 GT/s Tx PLL Bandwidth and Peaking

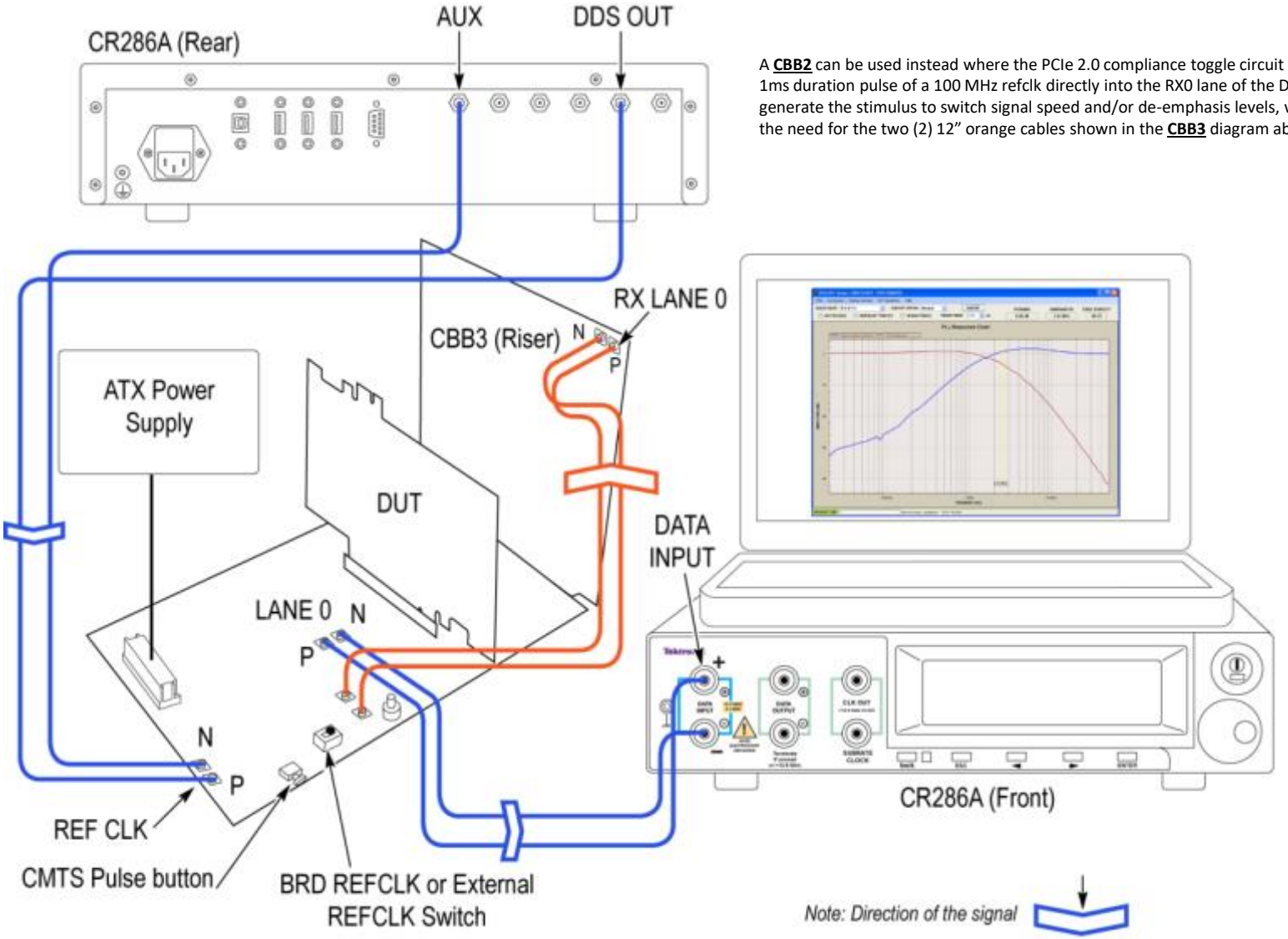
PLL bandwidth and peaking are defined for both the Transmitter and Receiver in order to place an upper limit on the amount of Refclk jitter that is propagated to the transmitted data and to the CDR. Defining PLL BW and peaking limits also guarantees a minimum degree of Tx/Rx jitter tracking in those systems utilizing a common Refclk Rx architecture.

Two sets of bandwidth and peaking are defined for 5.0 GT/s: 8-16 MHz with 3 dB of peaking and 5-16 MHz with 1 dB of peaking. This gives the designer the option of trading off between a low peaking PLL design vs. a low bandwidth design. For 2.5 GT/s, a single PLL bandwidth and peaking range is specified at 1.5-22 MHz with 3.0 dB of peaking.

4.3.3.12.2. 8.0 GT/s Tx PLL Bandwidth and Peaking

The Tx and Rx PLL bandwidth for 8.0 GT/s signaling is 2 – 5 MHz. Peaking may be from 0 to 2 dB for bandwidths up to 4 MHz and 0 to 1 dB for bandwidths up to 5 MHz. The 8.0 GT/s PLL BW range is substantially lower than the PLL bandwidths specified for 5.0 GT/s or 2.5 GT/s operation to reduce the amount of Refclk jitter at the sample latch of the receiver.

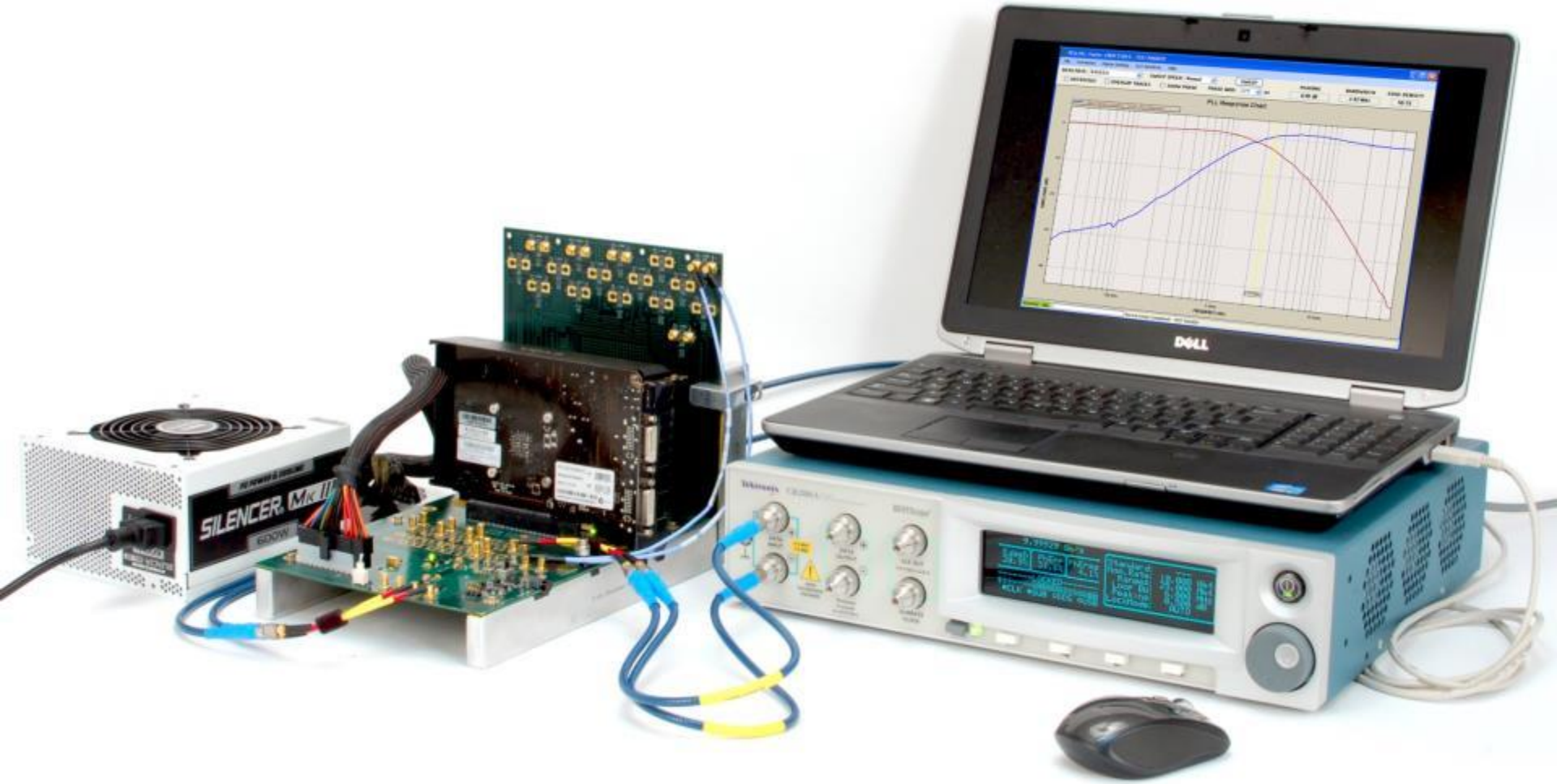
PLL Testing with CRU - Setup



A **CBB2** can be used instead where the PCIe 2.0 compliance toggle circuit creates a 1ms duration pulse of a 100 MHz refclk directly into the RX0 lane of the DUT to generate the stimulus to switch signal speed and/or de-emphasis levels, without the need for the two (2) 12" orange cables shown in the **CBB3** diagram above.

0850-004

PLL Testing with CRU



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