Version 1.0
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Tektronix Method of Implementation for PCI Express Gen 4.0 CEM Add-In Card PLL Bandwidth Test Procedure

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MODIFICATION RECORD

Version	Date	Changes done
0.7 Draft	21-Jan-2019	All
1.0	11-Feb-2019	Grammatical

References

The following documents are referenced in this document:

- *PCI Express® Card Electromechanical Specification Revision 4.0, Version 0.9*
- *PCI Express® Architecture PHY Test Specification Revision 4.0, Version 0.9*
- *PCI Express® Base Specification Revision 4.0 Version 1.0*

Software

- BERTScope PCIe PLL Tester - Automated test solution support PCI Express Add-In card PLL Bandwidth Test for Gen1 to Gen4.

REQUIRED EQUIPMENTS

Equipment	Details	Qty	P/N	Vender
CR286A or CR175A	Clock Recovery Unit with PCIe PLL software option PCIE8G	1	CR286A or CR175A & PCIE8G	Tektronix
Gen4 CEM Fixture	CBB/CLB/ISI Board of PCIE 4.0 Rev2.0	1	N/A	PCI-SIG
SMA-SMA Cable	1m SMA-SMA Phase Matched Cable Pair	1	PMCABLE1M	Tektronix
SMA-SMP Cable	1m SMA-SMP Phase Matched Cable Pair	1	174-6659-01	Tektronix
SMA-SMP connector	SMA - SMP cable matched pair, 2.5 inches, <1psec skew	1	80350960	Huber-Suhner
SMP-SMP Cable	SMP-SMP cable pair, 12 inches, <1psec skew	1	80345501	Huber-Suhner
SMA 50Ω terminator	Terminator for CR175A or CR286A data and clock SMA output	4	321-8010-xx	Tektronix
SMP-F 50Ω terminator	Some Add-In Card require termination for unused lanes.	6/14/30	ST2645	Fairview Microwave
ATX Power Supply	Compatible ATX power supply	1	Generic	Generic

1. INTRODUCTION

This MOI (Method of Implementation) provides the information for using the Tektronix BERTScope Clock Recovery instrument to test PCI Express PLL Bandwidth for Add-In Cards using PCI-SIG CEM (Card ElectroMechanical) Gen4 CBB (Compliance Base Board).

The purpose of the document is to provide the approved test equipment, procedure, connections and setup, for the PCI Express Gen4 CEM PLL BW tests as per *PCI Express® Architecture PHY Test Specification Revision 4.0*.

The PLL Loop Response test measures the bandwidth and peaking of the PLL used in Add-in cards for generating the Tx clock from the distributed 100 MHz REF_CLK signal. The loop response is determined by substituting a test clock for the locally generated REF_CLK which contains a calibrated level of sinusoidal jitter. The Tektronix clock recovery instrument measures the transferred jitter by applying the transmitted compliance pattern output from the Add-in card DUT (Device Under Test) into a reference PLL. The phase deviation is digitized and analyzed within the instrument to determine its spectral components. The frequency of the modulating sinusoidal jitter is incrementally swept, with measurement data taken at each frequency step. The instrument automatically computes the PLL magnitude and phase, along with jitter transfer function.

In addition to measuring the loop response, the clock recovery instrument contains the synthesizer used to generate the jitter modulated REF_CLK. The jitter appears as true phase modulation in the REF_CLK output, maintaining a 50% duty factor at all times. This allows the clock recovery instrument to be used with all types of clock generation PLLs, including those which incorporate dual edge phase detectors.

Incorporating the synthesizer within the instrument facilitates internal self-calibration, eliminating the need to manually normalize the test setup calibration. Once the cabling to the PCIe Gen4 CEM fixture is connected, you can begin testing immediately.

An external PC provides host system control and report generation software. This program plots the PLL Loop Response, compares the measured bandwidth and peaking against the specification limits, and can generate a test report in PDF or HTML file format.

2. PRE-REQUISITES

2.1 Software

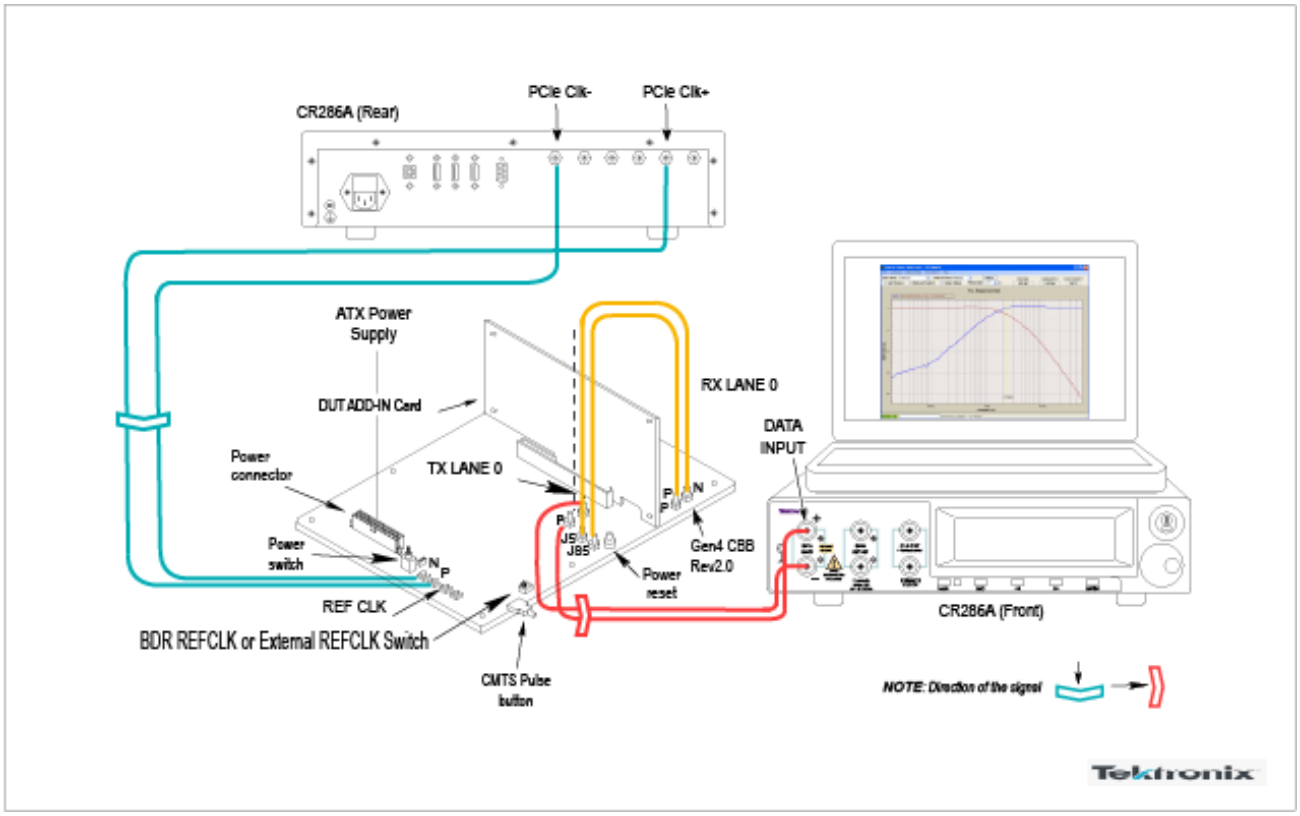
Install the BERTScope PLL Test software, on a host PC (Windows 7/10). The software supplied with Tektronix Clock Recovery instrument or can be downloaded from the Tektronix web site.

Software will prompt to install the USB driver once the Clock recovery unit is connected to the host PC. The driver will need to be installed only once.

3. CONNECTION DIAGRAM

In this section you can see the connection diagrams to run the Gen4 CEM Add-in Card PLL Bandwidth test as defined in the PCI Express Architecture PHY Test Specification.

3.1 PLL BW Test for Add-In-Card – Connection Diagram



4. Add-In Card PLL BW Tests

4.1 Configuration

1. Ensure CBB is Off (no power)
2. Connect the CR286A (Clock Recovery) using a USB cable to the host PC.
3. Connect the CR286A PCIe clock+- Output (on Rear panel) to the CBB Reference Clock input.
4. Connect the Tx Lane 0 on CBB to the CR286A Data Input.
5. Connect the 50Ω SMA terminators on the CR286A data and clock outputs.

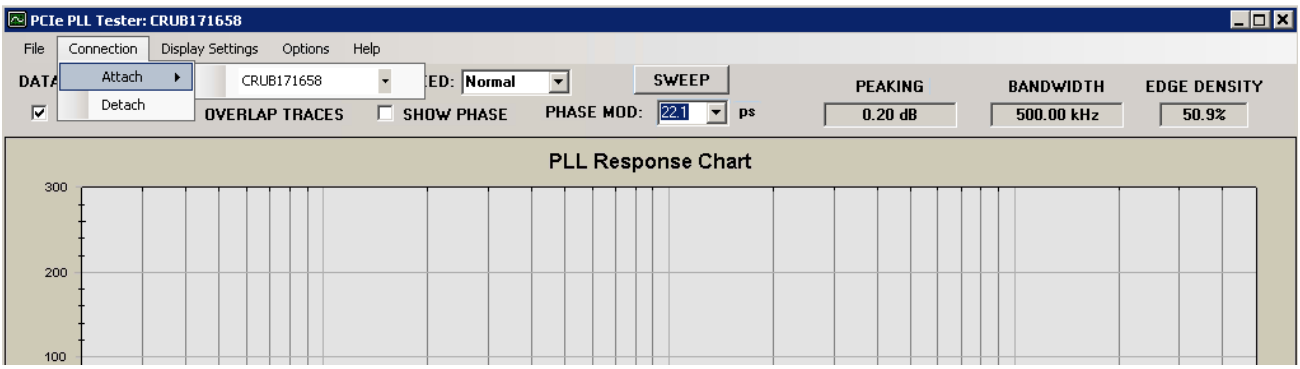
6. If required terminate the unused Tx lanes with SMP-F 50Ω terminators.
7. Insert the Add-in card under test into the CBB (no power).
   Note: If this test is performed at 8 GT/s the 3.0 CBB or 4.0 CBB must be used. If this test is performed at 16 GT/s the 4.0 CBB must be used.
8. Make sure that the compliance toggle outputs (SMP connectors J85 and J5) on the CBB main board are connected to RX LANE 0 (SMP connectors J1 and J8) on the CBB card via appropriate SMP to SMP cables.
9. Power on the CBB.
10. Push the compliance toggle button on the CBB (inject a 1ms pulse of a 100 MHz clock signal into RX LANE 0 of the Add-in card under test) until the compliance pattern at the desired data rate and with the desired TX EQ Preset is selected.

4.2 Toggle to Gen4

The Add-In Card must output the compliance pattern at the desired data rate of 16 GT/s with the desired TX EQ Preset. Use the compliance toggle button on the CBB (inject a 1ms pulse of 100MHz clock signal into Rx Lane 0) to toggle the Add-In Card under test from Gen1 to Gen4 with different Tx EQ Presets. Refer to the appendix for toggle sequence. For 16 GT/s a passing result with any TX EQ Preset is sufficient to pass the PLL BW test, but it is recommended to start with P7.

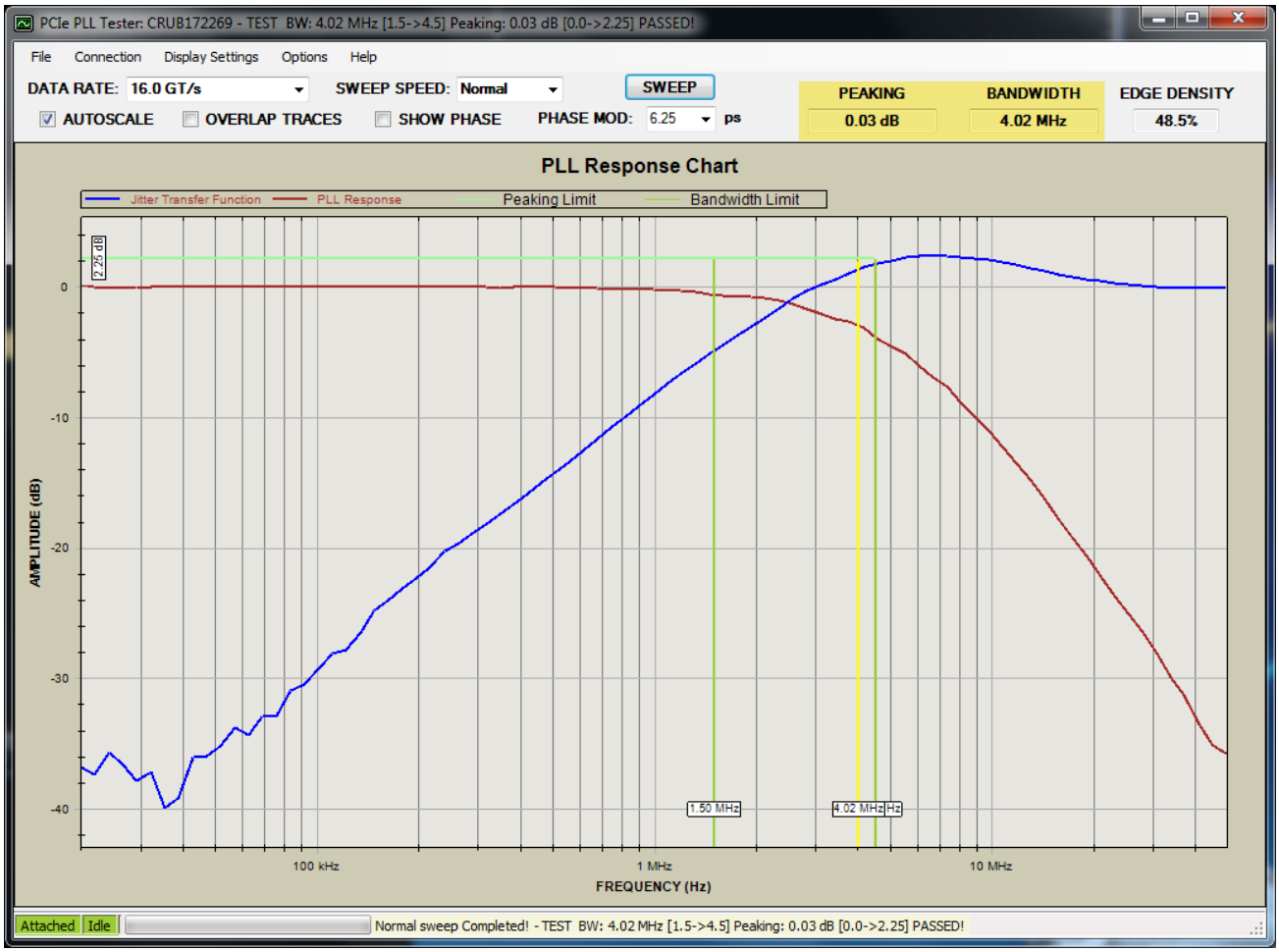
4.3 Test

1. Power on the CR286A and launch the PCIe PLL Tester software on the host PC.
2. Under the “Connection” drop down menu select “Attach” then “CR286A”. After connection is achieved the CR serial number will be shown in the PCIe PLL Tester software.



3. Select the DATA RATE as 16 GT/s.

4. Make sure the DUT is in Gen4 compliance mode and transmitting desired Preset P<x>. The LED will turn green once the CR286A is locked to the data.
5. The CR286A is pre-calibrated the Reference clock phase jitter as per the limits define in the *PCI Express® Architecture PHY Test Specification Revision 4.0*. The Phase Mod drop down option shows the phase modulation values.
6. To execute the test, click on the Sweep button. Test will take ~60 sec to complete.
7. At the completion of the test sweep the measured Loop bandwidth and peaking values will be displayed in the software.



8. The software also compares the result against the compliance limits and displays the Pass and Fail as shown above.

   Below are the test limits from *PCI Express® Base Specification Revision 4.0 Version 1.0* section 8.3.8 with tolerances (+/-0.5 MHz for Bandwidth & +0.25dB for Peaking) added per an ECN to the Base Specification.

Test	2.5 GT/s	5 GT/s		8 GT/s or 16 GT/s	
Loop Bandwidth (MHz)	1.0 – 22.5	4.5 - 7.5	7.5 – 16.5	1.5 - 3.5	3.5 – 5.5
Peaking (dB)	0.01 – 3.25	0.01 - 1.25	0.01 – 3.25	0.01 - 2.25	0.01 – 1.25

9. To generate a test report, select Print from the File menu. Select the file format option PDF or HTML to save the report.

PCIe PLL Analyzer Test Report **DATA RATE: 16.0 GT/s**

Date:	1/25/2019	**Time:**	11:28:26 AM
Device ID:		**Barcode:**	
Test Operator:		**PLA Serial #:**	B172269
Sweep Speed:	Normal	**Phase Modulation:**	6.25 ps

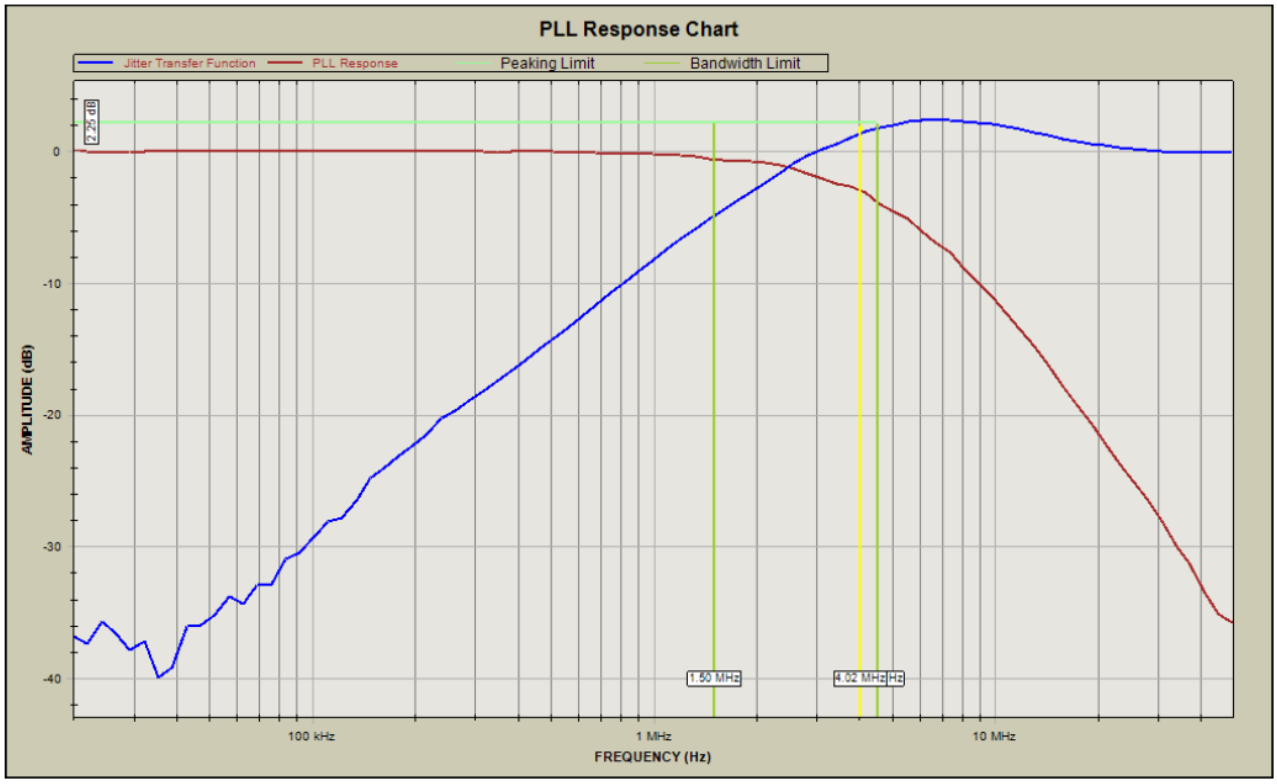
Notes:

TEST RESULT: PASSED

Bandwidth: 4.02 MHz **Peaking:** 0.03 dB **Edge Density:** 48.6%

The Table:

PCI Base Spec 4.0	Value	Limit (Low, High)	Margin (Low, High)	Result
Bandwidth (MHz)	4.02	1.5, 4.5	7.29, 13.21	Pass
Peaking (dB)	0.03	0, 2.25	0.45, 2.55	Pass



5. Appendix

5.1 Toggle Sequence Table

Toggle Sequence	Setting#	Compliance Pattern from the DUT	Data Rate (GT/s)
Power ON	1	Gen1	2.5
1	2	Gen2 - 3.5dB	5
2	3	Gen2 - 6.0dB	5
3	4	Gen3 - P0	8
4	5	Gen3 - P1	8
5	6	Gen3 - P2	8
6	7	Gen3 - P3	8
7	8	Gen3 - P4	8
8	9	Gen3 - P5	8
9	10	Gen3 - P6	8
10	11	Gen3 - P7	8
11	12	Gen3 - P8	8
12	13	Gen3 - P9	8
13	14	Gen3 - P10	8
14	15	Gen4 - P0	16
15	16	Gen4 - P1	16
16	17	Gen4 - P2	16
17	18	Gen4 - P3	16
18	19	Gen4 - P4	16
19	20	Gen4 - P5	16
20	21	Gen4 - P6	16
21	22	Gen4 - P7	16
22	23	Gen4 - P8	16
23	24	Gen4 - P9	16
24	25	Gen4 - P10	16
25	26	Jitter Measurement Pattern on all Lanes.	16
26	27	Jitter Measurement Pattern on Lanes 0/8/16/24 and Compliance pattern on all other Lanes	16
27	28	Jitter Measurement Pattern on Lanes 1/9/17/25 and Compliance pattern on all other Lanes	16
28	29	Jitter Measurement Pattern on Lanes 2/10/18/26 and Compliance pattern on all other Lanes	16
29	30	Jitter Measurement Pattern on Lanes 3/11/19/27 and Compliance pattern on all other Lanes	16
30	31	Jitter Measurement Pattern on Lanes 4/12/20/28 and Compliance pattern on all other Lanes	16
31	32	Jitter Measurement Pattern on Lanes 5/13/21/29 and Compliance pattern on all other Lanes	16
32	33	Jitter Measurement Pattern on Lanes 6/14/22/30 and Compliance pattern on all other Lanes	16
33	34	Jitter Measurement Pattern on Lanes 7/15/23/31 and Compliance pattern on all other Lanes	16