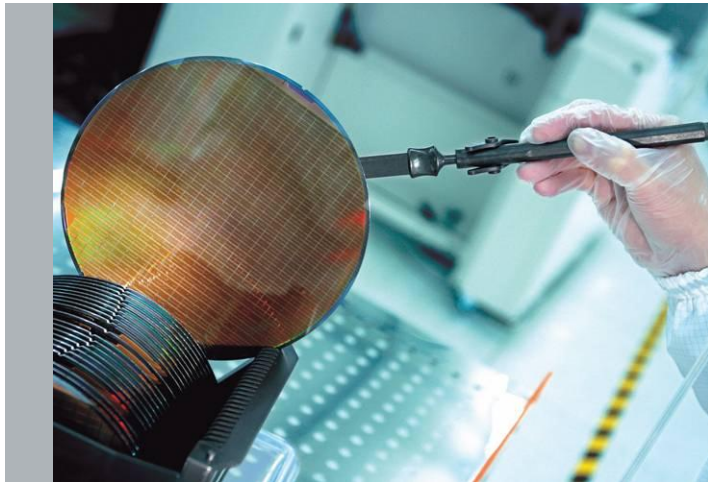# Detailed DDR Memory Interface and Test Solutions

- Visual Trigger, DDRA

YJ.PARK

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AGENDA

- **DRAM Technologies**

    - **DDR Memory Trends**
    - **DDR theory**
    - **Visual trigger**
    - **DDRA**

DDR Memory Trends

Memory Technology – Quick Overview

- **DRAM - dominant memory technology**
  - Computer system memory
    - Server, desktop, laptop
    - Dynamic, volatile memory, plug-in DIMMs
  - Embedded systems
    - Cell phones, printers, cars
    - Fixed memory configuration
  - DRAM driven by faster processors, faster data rates
    - DDR3 now available at 1600 (1.6Gb/s) data rates
    - DDR3 over 2000 emerging(overclocked)
    - DDR4 ~3200MT/S

- **DRAM variants**
  - LPDDR – Low Power DDR
    - Power savings for portable computing
  - GDDR – Graphic DDR
   - Optimized for Speed - faster access

SDRAM Standards			
SDRAM	Data Rate MT/S	Clock MHz	VDD V
DDR-266	266	133	2.5
DDR-333	333	166	2.5
DDR-400	400	200	2.5
DDR2-400	400	200	1.8
DDR2-533	533	267	1.8
DDR2-667	667	334	1.8
DDR2-800	800	400	1.8
DDR2-1066	1066	533	1.8
DDR3-800	800	400	1.5
DDR3-1066	1066	533	1.5
DDR3-1333	1333	667	1.5
DDR3-1600	1600	800	1.5

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SDRAM Standards

|	SDR DRAM	DDR SDRAM	DDR2 SDRAM	Qimonda DDR3 SDRAM
Data rate [Mb/s per pin]	PC66, PC100, PC133	DDR200, 266, 333, 400	DDR2-400, 533, 667, 800	DDR3-800, 1066, 1333, 1600
I/O organization	x4, x8, x16	x4, x8, x16	x4, x8, x16	x4, x8, x16
VDD = VDDQ/[V]	3.3 (+/- 0.3)	2.5 (+/- 0.2)	1.8 (+/- 0.1)	1.5 (+/- 0.075)
Interface	LVTTL	SSTL_2	SSTL_18	SSTL_15
Number of Banks	2/4	4	4 / 8	8
Prefetch	1	2	4	8
Burst length	1, 2, 4, 8 (page)	2, 4, 8	4, 8	8 (chop 4)
Bidirectional strobe	None	Single Ended (SE)	SE and Differential	Differential only
DQ driver strength	Wide envelope	Narrow envelope	18 Ω, OCD calibration	34 Ω, ZQ-pin cal
Termination		MoBo	MoBo/ODT	DIMM/Dynamic ODT
Read Latency Additional Latency	CL = (1), 2, 3 -	CL = (1.5), 2, 2.5, (3) -	CL = (2), 3, 4, 5 AL = 0, 1, 2, 3, 4	CL = 5, 6, 7, 8, 9, 10, (11) AL = 0, CL-1, CL-2
Write Latency	0	1	RL-1	5, 6, 7, 8 + AL
Data mask	Yes	Yes	Yes	Yes
Interrupts	Yes	Yes	Wr-Wr, Rd-Rd 4n only	Burst Chop for Rd and Wr
Package	TSOP-54	TSOP-66/BGA	BGA	BGA

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DDR Memory Trends
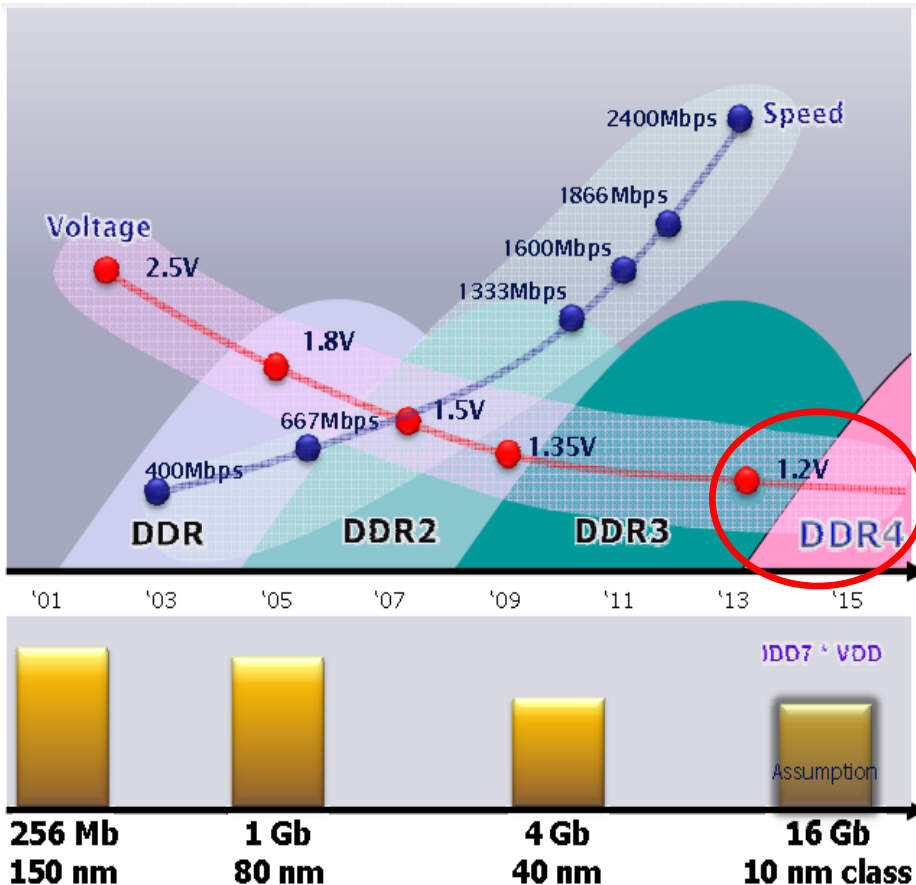
- DDR Market Adoption
  - DDR2 Widely available in many speeds, densities, form factors
  - DDR3 speeds from 800MT/s to 1600MT/s(over 2000MT/s)
  - DDR3 higher rates under development

- DDR4 specification expected to be released by Mid to late 2012 timeframe

- High speed measurements techniques and higher performance measurement tools need to be applied

- Parallel buses reaching the speeds of serial technology :
  Memory Clock speeds reaching >1GHz

  - Tighter timing margins
  - Crosstalk, impedance, and jitter management

Courtesy Samsung

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DDR Analog Verification & Debug

Signal Access - Probing
- Requires easy but reliable physical connectivity
  - Access to various measurement points on DRAM or Memory
- Requires maximum signal integrity
 - Sufficient performance for signal speeds
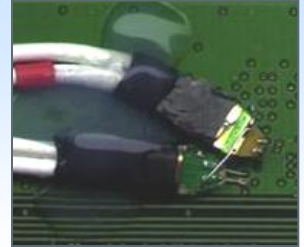
Signal Acquisition
- Automatically trigger and capture DDR signals
  - Identify and trigger directly on DQ, DQS in real-time to isolate Reads/Writes
  - Automatically set voltage levels and data rates
- Capture long time duration at high resolution
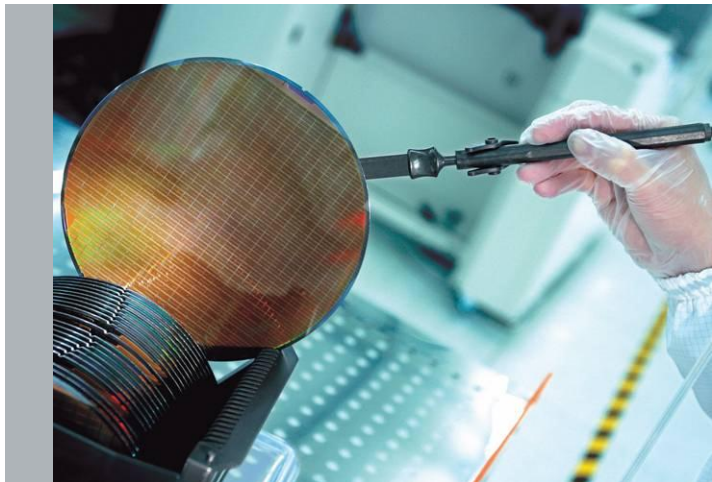 - Direct connection to DPOJET for signal analysis

Signal Analysis
- **Visual Trigger** – EASY function of Trigger!!
- **DDRA** – Automated setup, read/write burst detection, JEDEC pass/fail meas.
- DPOJET – The most powerful Jitter, Eye and Timing analysis tool

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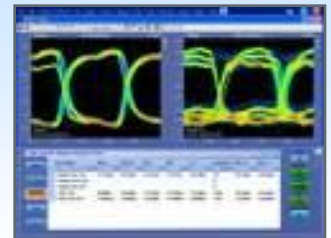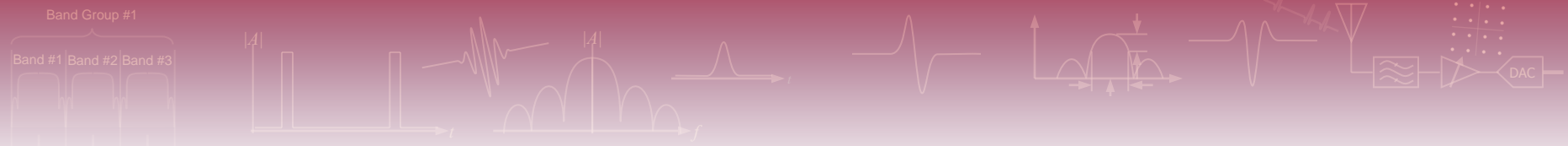
DDR theory

DDR Architecture

FEATURES

- DDR (Double Data Rate)

  – **Double-data-rate architecture; two data transfers per clock cycle**
  – **Bidirectional,** data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
  – DQS is **edge-aligned** with data **for READs; center- aligned** with data **for WRITEs**
  – **Differential clock inputs**
  – **Commands** entered on **each positive CK edge; data and data mask** referenced to **both edges of DQS**
  – Read and write accesses to the DDR SDRAM are **burst oriented.**
  – An **AUTO PRECHARGE** function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.
  – **An auto refresh mode** is provided, along with a **power-saving, power-down mode.**

- Component
  – **DATA, STROBE, Control, Address, Clock, Power and GND**

- The **double data rate architecture** is essentially a **2nd prefetch architecture** with an interface designed to transfer **two data words per clock cycle** at the I/O pins**.**

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DDR2 Consideration

Feature/Option	DDR	DDR2	DDR2 Advantage
Package	TSOP (66 pins)	FBGA only	Enables better electrical performance and speed
Voltage	2.5V 2.5V I/O	1.8V 1.8V I/O	Reduces memory system power demand
Densities	128Mb–1Gb	256Mb–2Gb	High-density components enable large memory subsystems
Internal Banks	4	4 and 8	1Gb and higher DDR2 devices will have 8 banks for better performance
Prefetch (MIN WRITE Burst)	2	4	Provides reduced core speed dependency for better yields
Speed (Data Pin)	200 MHz, 266 MHz, 333 MHz, and 400 MHz	400 MHz, 533 MHz, and 667 MHz	Migration to higher bus speed
READ Latency	2, 2.5, 3 CLK	CL + AL CL = 3, 4, 5	Eliminating one-half clock settings helps speed internal DRAM logic and improves yields
Additive Latency (Posted CAS)	N/A	AL options 0, 1, 2, 3, 4	Mainly used in server applications to improve command bus efficiency
WRITE Latency	1 clock	READ latency - 1	Improves command bus efficiency
Termination	Motherboard parallel to VTT	DRAM on-die termination (ODT), optional on-motherboard termination	ODT for both memory and controller improves signaling and reduces system cost
Data Strobes	Single-ended	Differential or single-ended	Improves system timing margin by reducing strobe crosstalk
Modules	184-pin DIMM unbuffered registered 200-pin SODIMM 172-pin MicroDIMM	240-pin DIMM unbuffered registered 200-pin SODIMM 214-pin MicroDIMM	Improved layout and power delivery design
Chipset Support	All DTs, NBs, and servers	All DTs, NBs, and servers	All major chipset providers

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DDR2 SDRAM
Advantages over DDR memory

- **Faster memory**
  - DDR2 operates at 200 MHz to 400 MHz clock rates
  - Faster data rates 400 Mb/s/pin to 800 Mb/s/pin

- **Improved signal integrity with On-Die Termination (ODT)**
  - Increased voltage margin
  - Reduced over shoot
  - Increased slew rate
  - Reduced ISI (Inter-Symbol Interference)
  - Larger data eye diagram

- **Increase DRAM access flexibility**
  - 8 banks
  - Additive latency

- **Reduced power**
  - DDR2 @ 1.8 V versus DDR @ 2.5 V
  - Smaller page size reduces active power

DDR3 SDRAM

- DDR3 SDRAM is a performance evolution and enhancement of SDRAM technology starting at 800 Mb/s.
    - DDR3-800/1066/1333/1866/2133
    - Operating voltage 1.5 V(83% of DDR2)Increased slew rate
    - Eight banks (DDR2 has four/eight banks upon the memory size)
    - Use all four mode registers.
      (DDR2 defined the first two mode registers two were reserved for future use.)

- DDR3 data strobes DQS are differential
  (DDR2 strobes could be programmed to be single-ended or differential)

- Active low asynchronous RESET# pin :
    - Improve system stability by putting the SDRAM in a known state regardless of the current state.

- Uses the same type of FBGA packages as DDR2 SDRAM.

DDR4 Overview

- DDR4 specification expected to be released by Mid to late 2012 timeframe

- Primary benefits compared to DDR3 include
  - Higher range of clock frequencies and data transfer rates
    - DDR4-1600 MT/s
    - DDR4-1866 MT/s
    - DDR4-2133 MT/s
    - DDR4-2400 MT/s
    - DDR4-2666 MT/s
    - DDR4-3200 MT/s

  - Significantly lower voltage 1.05–1.2 V(DDR4) Vs1.2–1.5 V (DDR3).
  - In a notebook, the DDR4 module reduces power consumption by 40% compared to a 1.5V DDR3 module

- Commercial products that support DDR4 are expected to be available in 2013

- Three signal integrity improvements
  - Memory controller Tx and Rx Equalization.
  - Connector improvements reduce crosstalk.
  - Simulation is based on statistical analysis rather than an absolute eye.

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1Gb DDR SDRAM
Functional block diagram (256 Meg x 4)

4K Columns x 16K Rows x 4banks x DATA 4 outputs
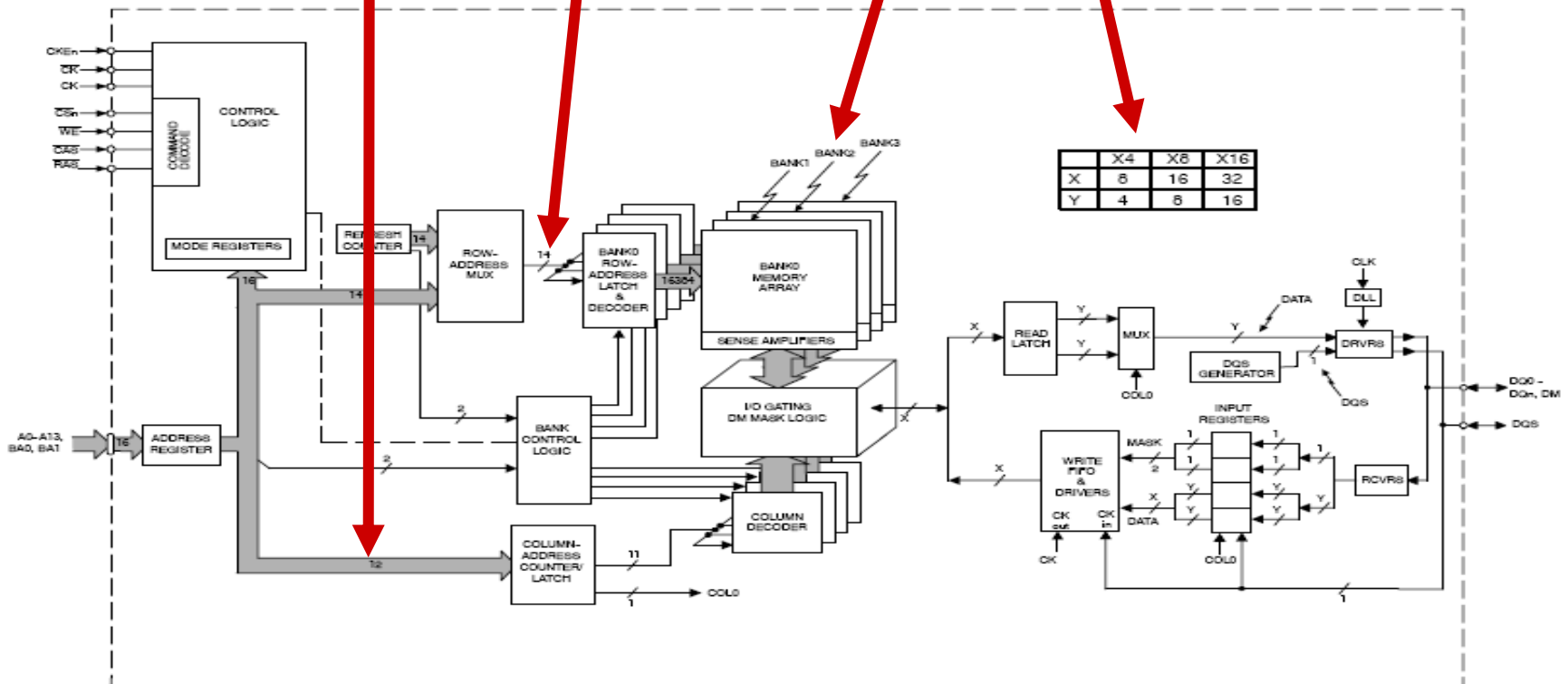
Note 1: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note 2: DM is a unidirectional signal (input only) but is internally loaded to match the load of the bidirectional DQ and DQS signals.

Note 3: Not all address inputs are used on all densities.

- ROW Address : A0~A13 (14EA)
- Column Address : A0~A9,A11,A12 (12EA)

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1Gb DDR2 SDRAM Example
Functional block diagram (256 Meg x 4)

2K columns x 16K rows x 8 banks x 4 outputs = 1Gb

Image courtesy of Micron Technology, Inc.

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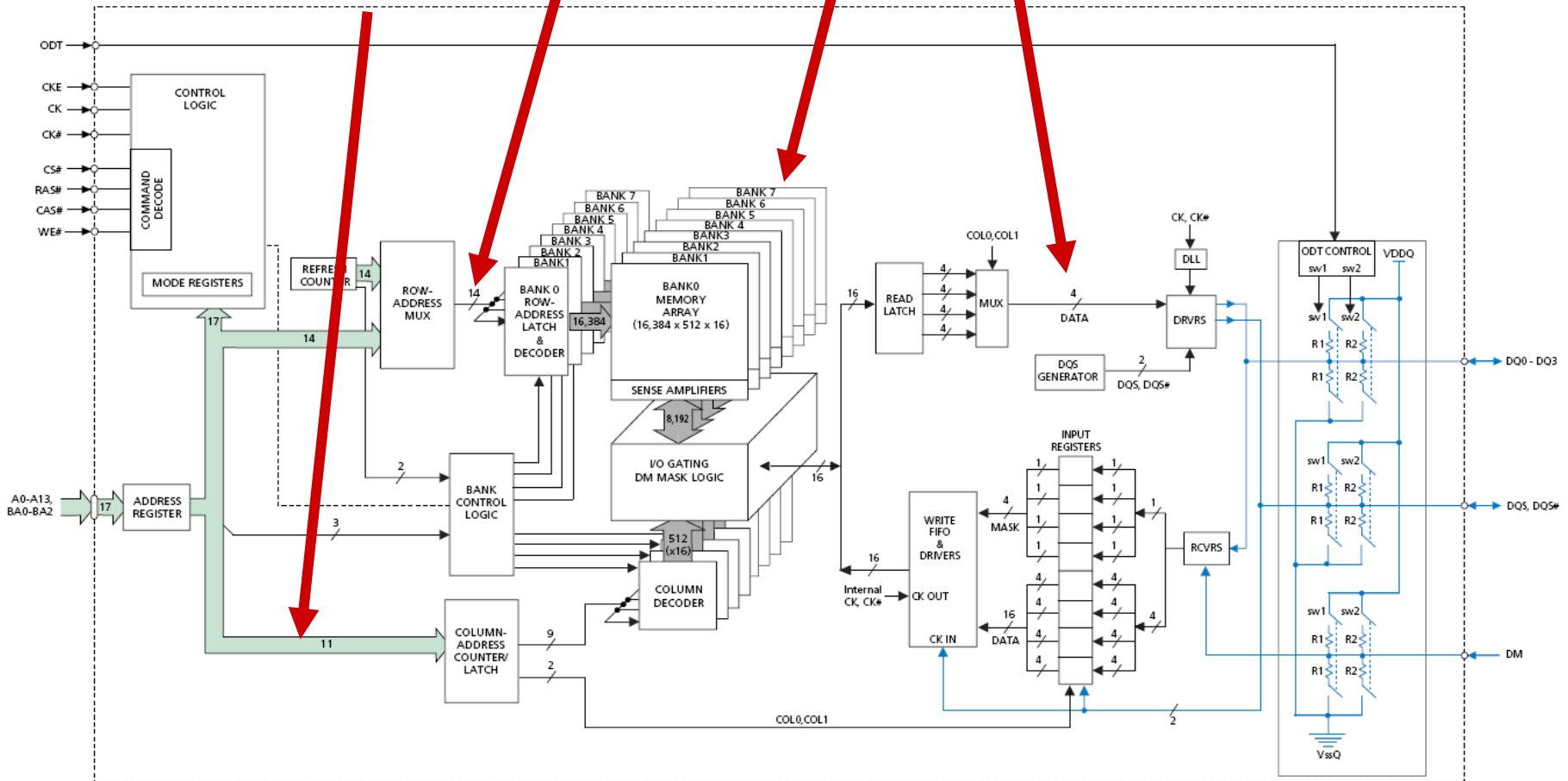
Banks

Multiple Banks in a DRAM

Address the internal banks with Bank Address (BA0-BA1) pins
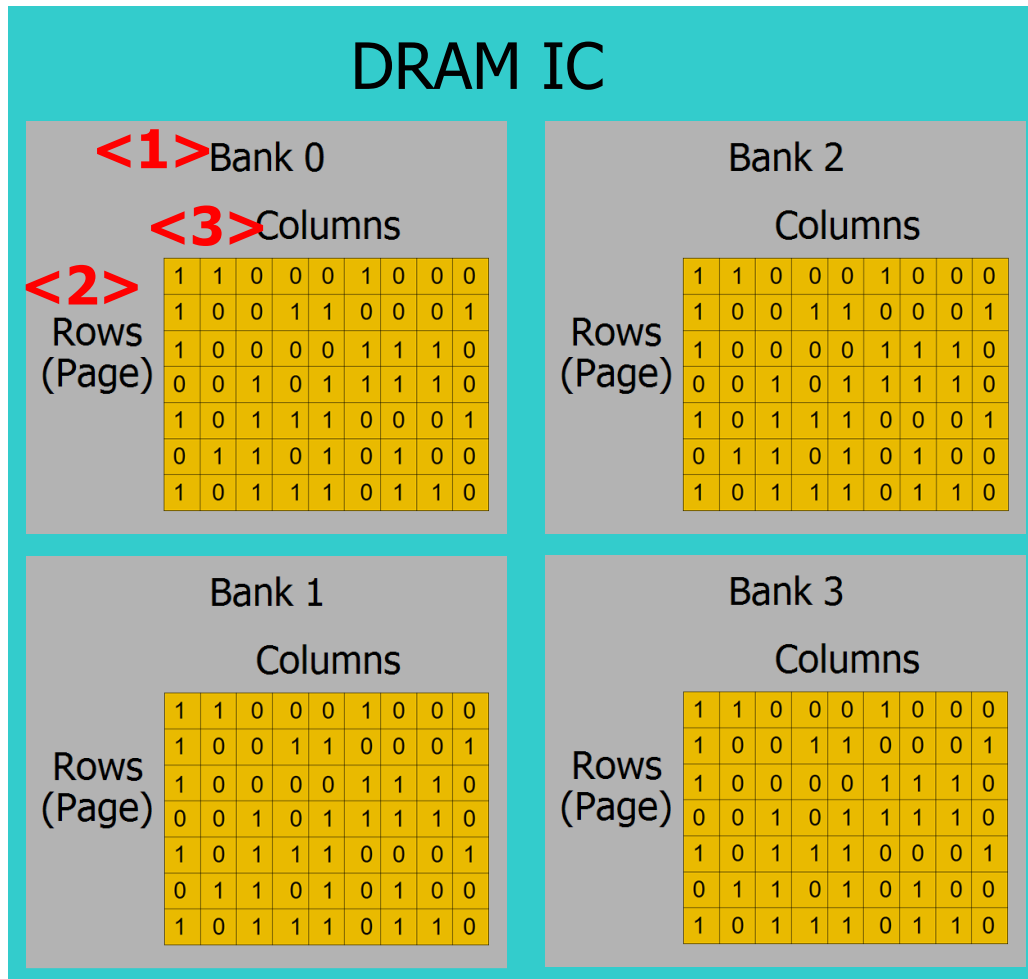
<1> , <2> : For row active

<3>: For operation read and write

DDR (State Diagram)
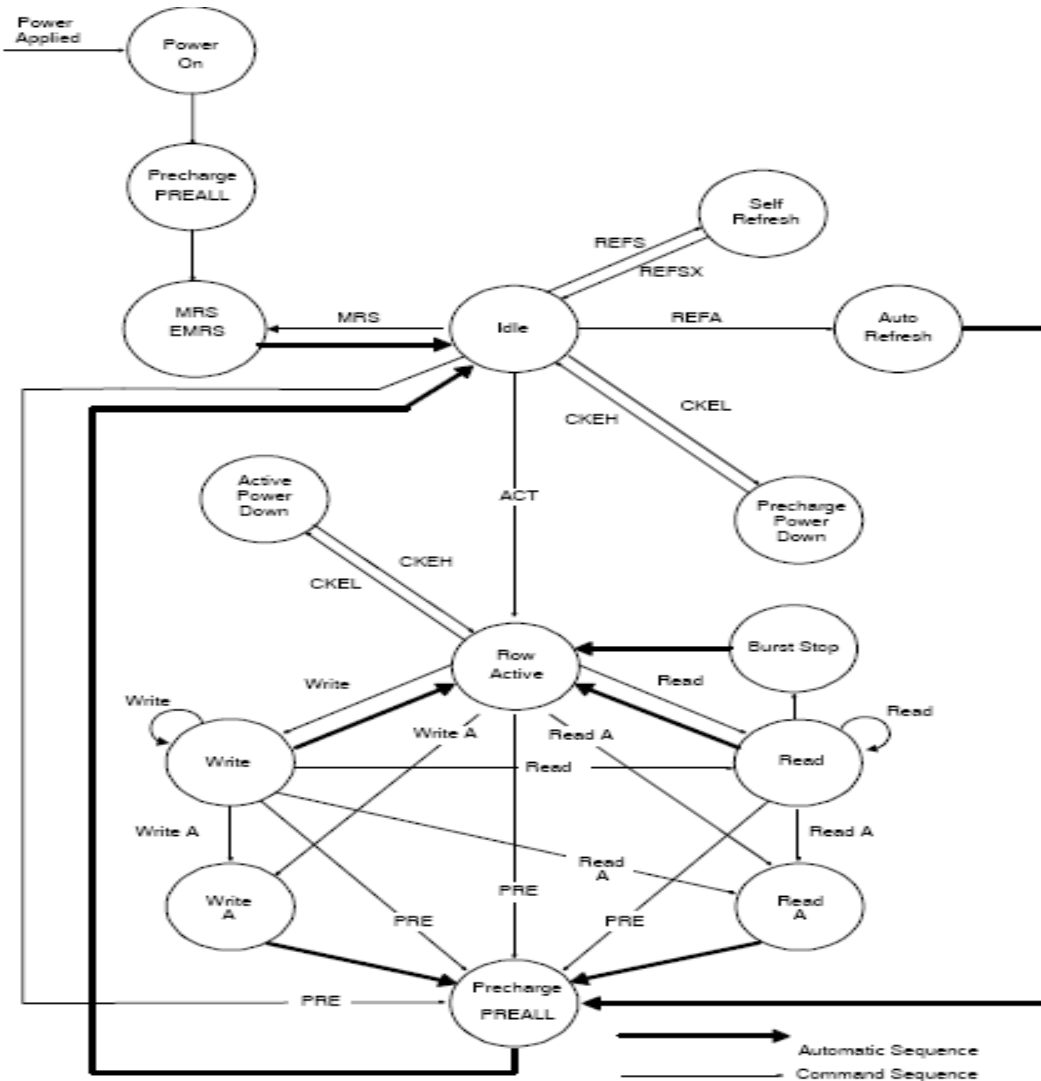
Procedure

- **Initialization**

- **Register Definition**
  - Mode Register
  - Extended Mode register

- **Commands**
  - Deselect
  - No Operation (NOP)
  - Mode register set
  - Active
  - Read
  - Write
  - Auto Precharge
  - Refresh

- **Operations**
  - Bank/Row Activation
  - Reads
  - Writes

- **Power Down**

DDR Procedure

< 1 > Initialization

- **POWER UP**

  - VDDQ(DQ Power Supply) : +2.5 V $\pm$0.2 V. for DDR 200, 266, or 333
                                        +2.6 $\pm$0.1 V for DDR 400
  - VDD(Power Supply): +3.3 V $\pm$0.3 V or +2.5 V $\pm$0.2 V for DDR 200, 266, or 333
                                        +2.6 $\pm$0.1 V for DDR 400

- **After all power supply** and reference voltages are stable, and the clock is stable,
  the DDR SDRAM requires a 200 µs delay prior to applying an **executable command**.

- DESELECT or NOP command should be applied, and **CKE should be brought HIGH.**

- **All BANK To be Idle**
  - Following the NOP command, a PRECHARGE ALL command should be applied.

DDR Procedure

< 2 > Register Definition
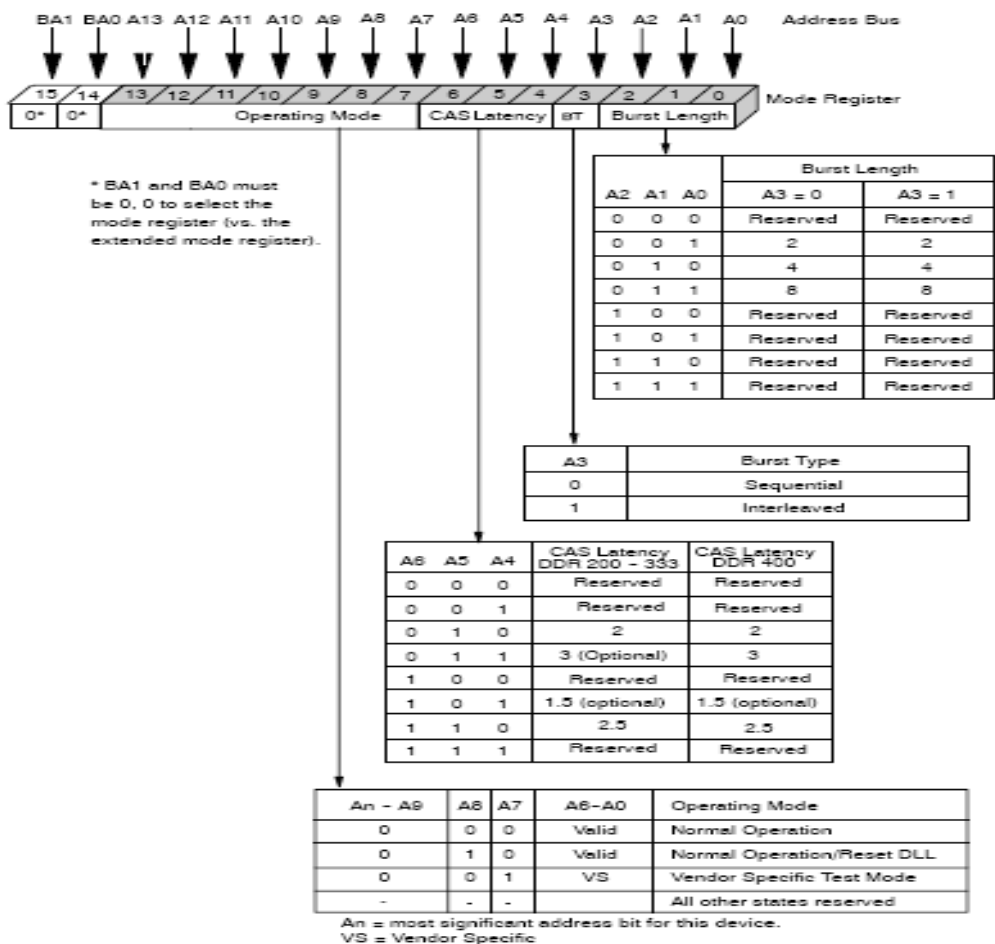
- **Mode Register**
  (BA0 = 0 and BA1 = 0)

  - The Mode Register is used to define the specific **mode of operation of the DDR SDRAM.**

  - **Mode Register** must be loaded **when all banks are idle** and **no bursts** are in progress

1. **Burst length   : A0~A2**
2. **Type of burst   : A3**
   (sequential or interleaved)
3. **CAS latency   : A4~A6**
4. **Operating mode :A7~A13**
   (A12 on 256Mb/512Mb, A13 on 1Gb)

DDR Procedure

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:
1. For a burst length of two, A1–Ai selects the two–data–element block; A0 selects the first access within the block.
2. For a burst length of four, A2–Ai selects the four–data–element block; A0–A1 selects the first access within the block.
3. For a burst length of eight, A3–Ai selects the eight–data–element block; A0–A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

1. Burst length   : A0~A2

- Read and write accesses to the DDR SDRAM are **burst oriented**

- The **burst length** determines the **maximum number of column locations** (for a READ or WRITE command)

- Burst lengths of 2, 4, or 8 locations are available for both the **sequential** and the **interleaved** burst types.

2. Burst Type

- **Burst type** is selected via **bit A3**
- **Sequential(0) or interleaved(1)**

DDR Procedure

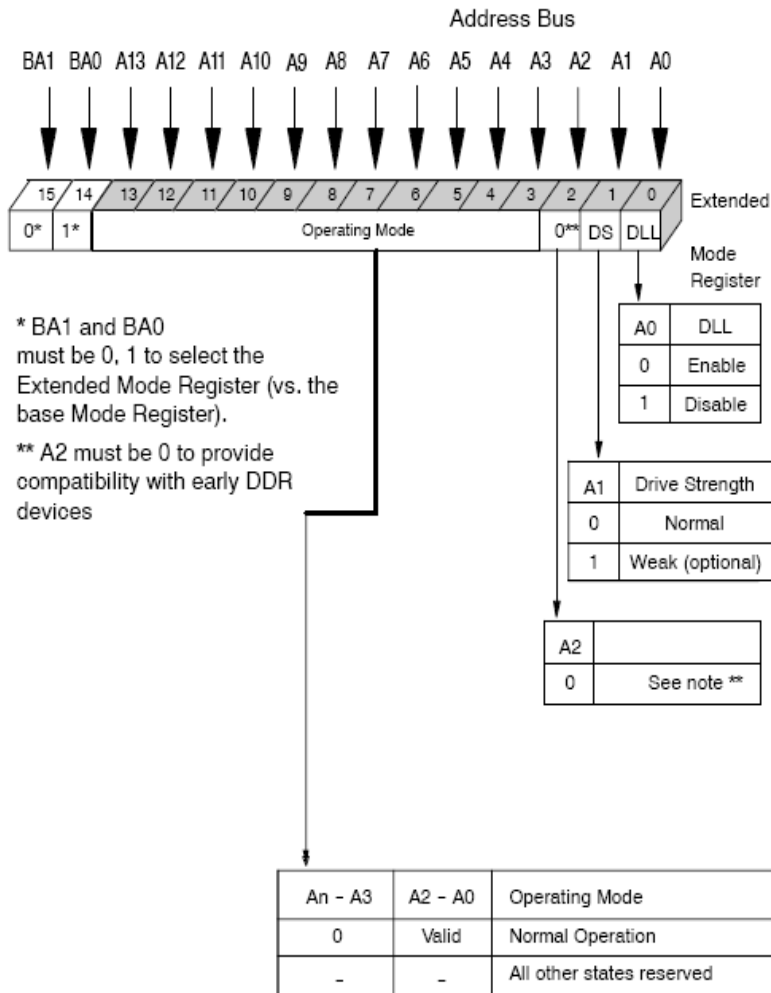## 3. Read Latency (CAS Latency)- A4~A6

- The READ latency is the delay, **in clock cycles,** between **the registration of a** READ command and **the availability of the** first piece of output data.

- For DDR200, DDR266, and DDR333 : 2 or 2.5 clocks

- For DDR400: 3 clocks

Burst Length = 4 in the cases shown
Shown with nominal tDQSCK

DON'T CARE
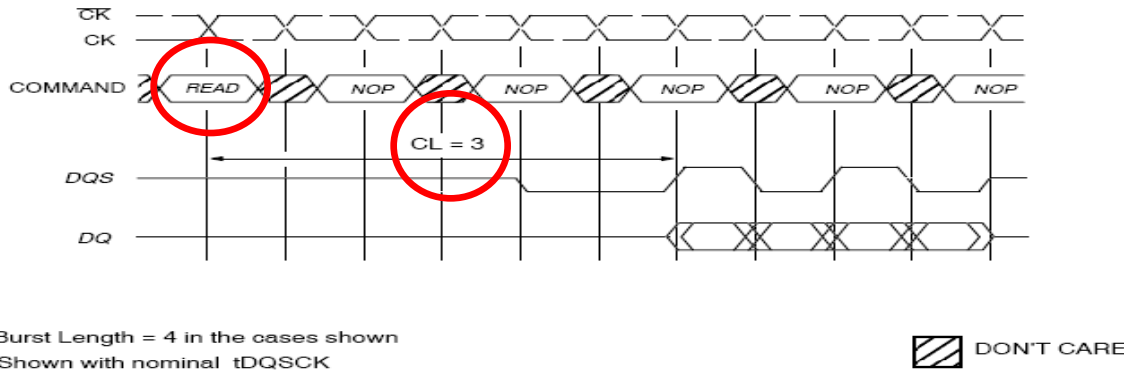
4. Operating Mode

- **The normal operating mode is selected by issuing a Mode Register Set command with bits** A7~A13 each set to zero**, and bits** A0~A6 set to the desired values**.**

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DDR Procedure

Address Bus

BA1 BA0 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Extended
0*	1*				Operating Mode								0**	DS	DLL	Mode Register

* BA1 and BA0 must be 0, 1 to select the Extended Mode Register (vs. the base Mode Register).

** A2 must be 0 to provide compatibility with early DDR devices

A0	DLL
0	Enable
1	Disable

A1	Drive Strength
0	Normal
1	Weak (optional)

A2	
0	See note **

An – A3	A2 – A0	Operating Mode
0	Valid	Normal Operation
–	–	All other states reserved

- **Extended Mode Register**
  (BA0 = 1 and BA1 = 0)

  - These additional functions include
    DLL enable/disable (for locking),
    output drive strength selection
    (optional)
  - **Mode Register** must be loaded **when
    all banks are idle** and **no bursts** are in
    progress

1. DLL Enable/Disable
  - The DLL must be enabled for normal operation.
  - DLL enable is required during power up
    initialization
  - DLL Reset : 200 clock cycles must occur
    before any executable command

2. Output Drive Strength *
  - Normal / Weak (optional)

* Output drive strength: about V-I characteristics spec.

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DDR2 Procedure

< 2 > Register Definition
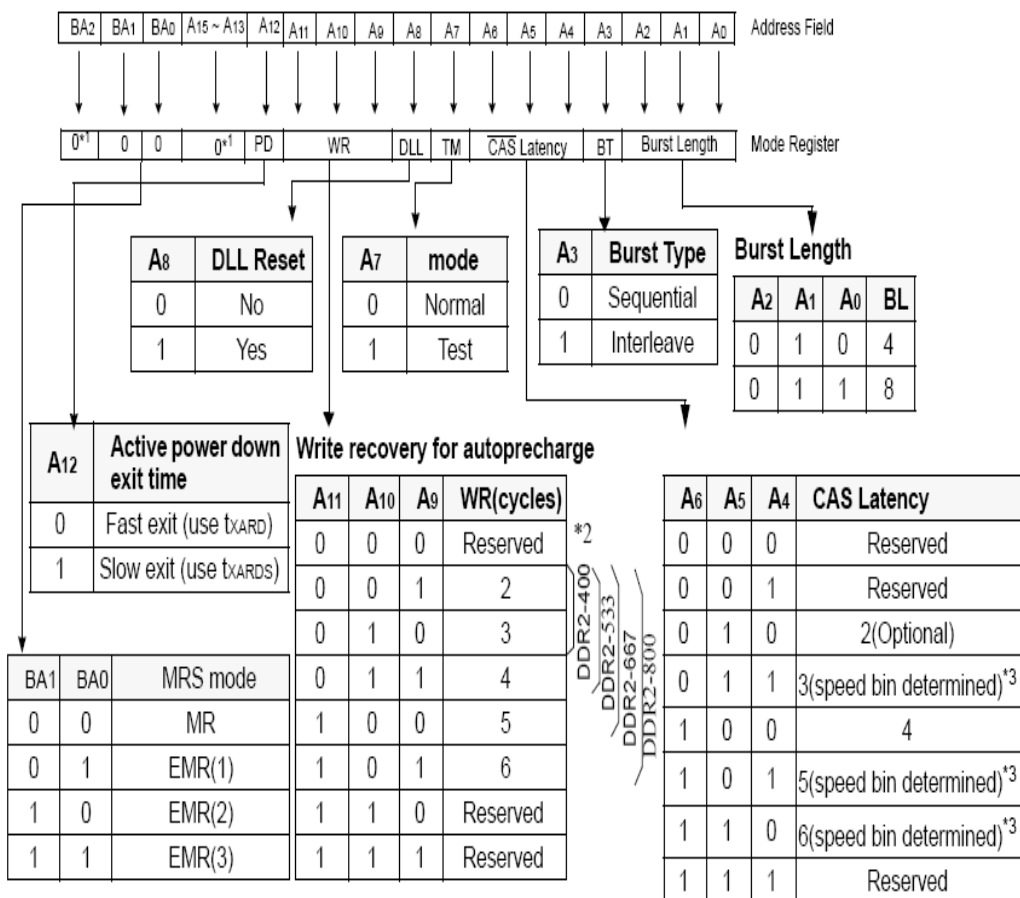
- **Mode Register**
  (BA0 = 0 and BA1 = 0)

  1. Burst length   : A0~A2

  2. Type of burst   : A3
     (sequential or interleaved)

  3. CAS latency   : A4~A6

  4. Test Mode   : A7

  5. DLL Rest   : A8

  6. Write Recovery Time :A9~A11

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DDR2 Procedure

EMR(1)
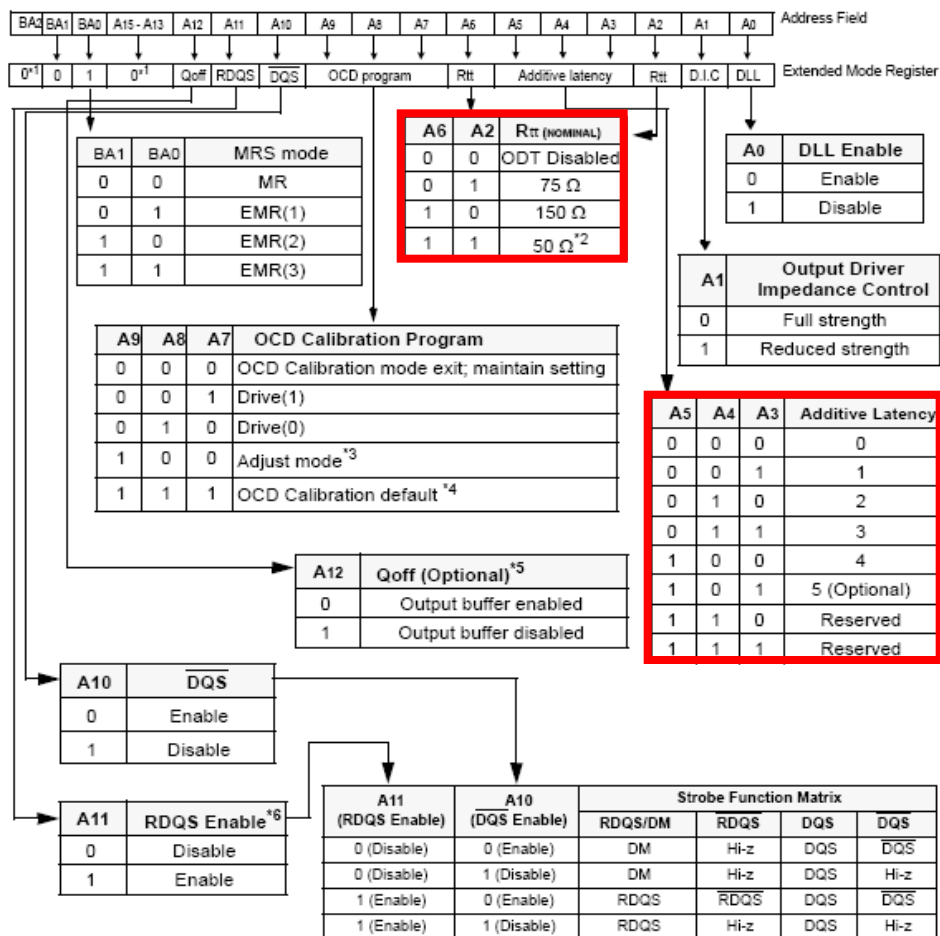
- **EMR(1)**
  (BA0 = 1 and BA1 = 0)

  1. DLL enable or disable : A0

  2. Strength output drive :A1

  3. Additive latency: A3 - A5
     (sequential or interleaved)

  4. OCD control: A7 - A9

  5. ODT setting: A2 and A6

- **DLL enable is required during power-up and initialization**

- **EMR(2)**
  - High Temperature Self-Refresh
    Rate Enable mode

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DDR2 Procedure

ODT (on-die termination)

- **ODT feature is designed to improve** signal integrity.
- **For DQ, DQS, DM signal**
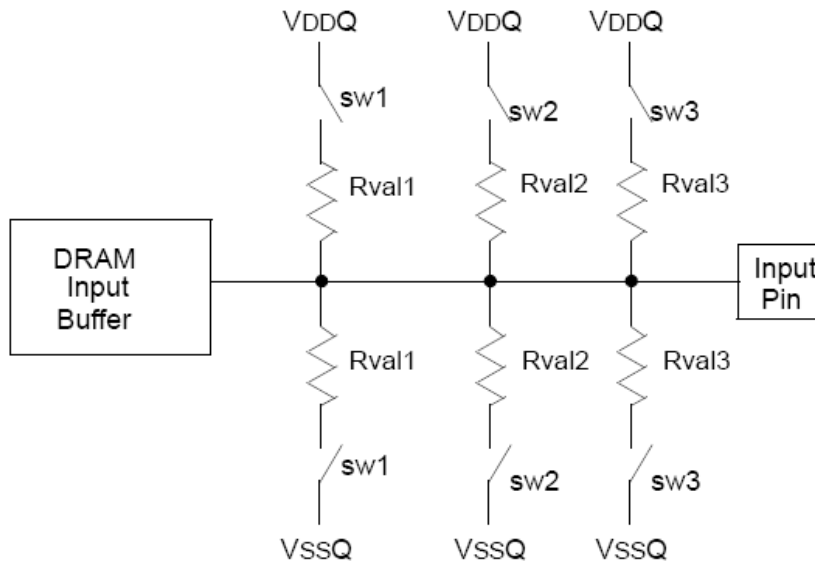
EMR(1)

A6	A2	R_{tt} (NOMINAL)
0	0	ODT Disabled
0	1	75 Ω
1	0	150 Ω
1	1	50 Ω^{*2}

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DDR Procedure

Initialization and Mode Register Sets

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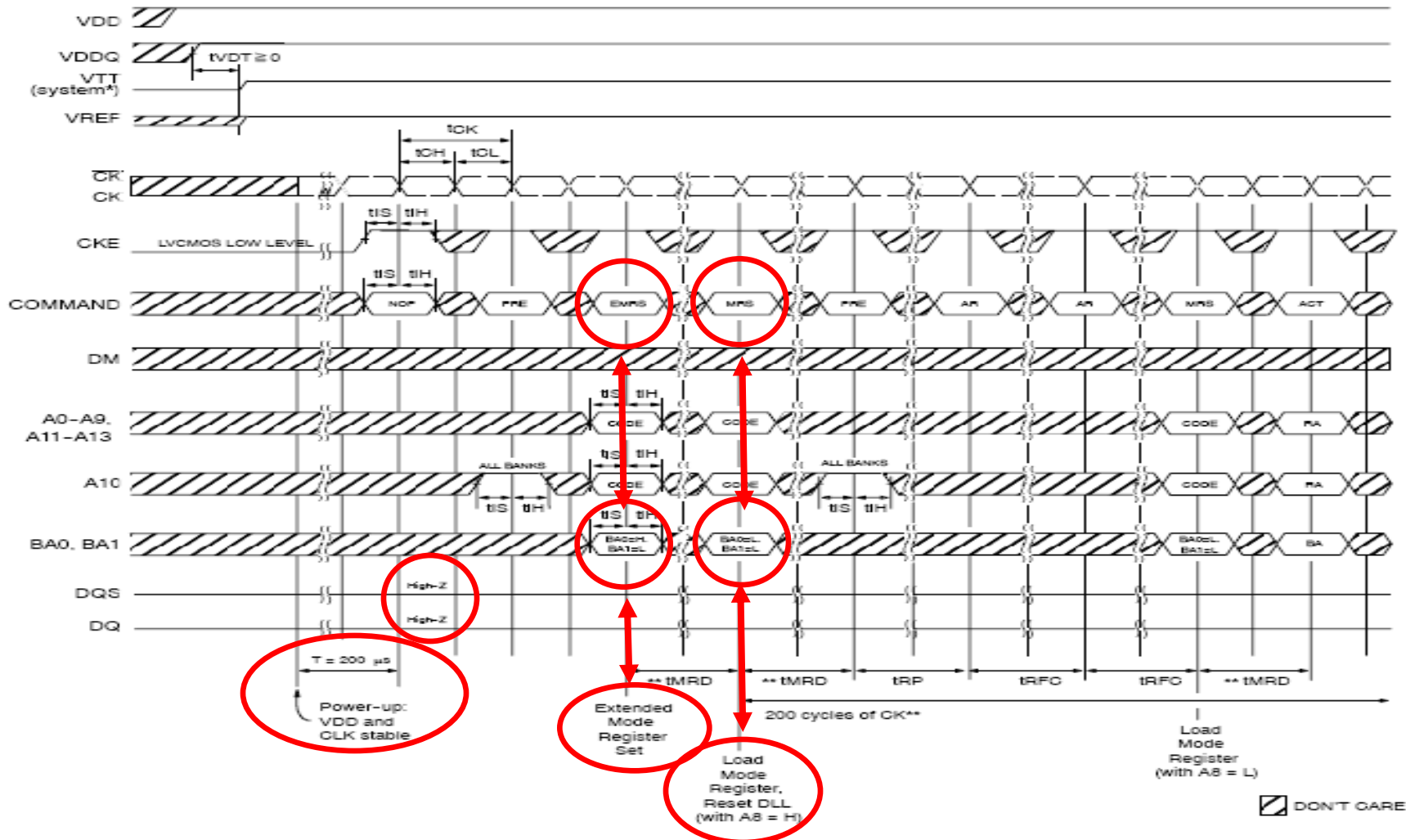
DDR Procedure

< 3 > Commands

TRUTH TABLE 1a - Commands
(Notes: 1, 11)

NAME (Function)	$\overline{CS}$	RAS	CAS	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO refresh or Self Refresh (Enter self refresh mode)	L	L	L	H	X	6, 7, 12
MODE REGISTER SET	L	L	L	L	Op-Code	2

TRUTH TABLE 1b - DM Operation

NAME (Function)	DM	DQs	NOTES
Write Enable	L	Valid	10
Write Inhibit	H	X	10

- **CKE** is **HIGH** for all commands shown **except SELF REFRESH.**

- **BA0~BA1** provide **bank address** and **A0~A13** provide **row address and column address**

- **A10 LOW:** BA0~BA1 determine **which bank** is **precharged.**
  A10 HIGH: All banks are **precharged** and **BA0~BA1** are **"Don't Care."**

- **CKE is HIGH : AUTO REFRESH**
- **CKE is LOW : SELF REFRESH**

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DDR Procedure

Consideration of Commands (Truth table1)

- **DESELECT**

  - The DESELECT function (CS = High) **prevents new commands** from being executed by the DDR SDRAM.

- **NO OPERATION (NOP)**

  - The NO OPERATION (NOP) command is used to perform a NOP to a DDR SDRAM which is selected **(CS is LOW)**

- **MODE REGISTER SET**

  - The MODE REGISTER SET command can only be issued **when all banks are idle and no bursts are in progress**

- **ACTIVE**

  - The ACTIVE command is used to **activate a row** in a **particular bank** for a subsequent access.**(BA0,BA1 and A0-A13 for ROW)**

- **READ command**

  - **To initiate a burst read** access to an active row.
  - **Selects** the **starting column** location.
  - **A10 determines** whether or not **auto precharge** is used.
  - **If auto precharge is selected,** the **row** being accessed **will be precharged** at the end of the read burst
  - **if auto precharge is** not **selected, the row will remain open for subsequent accesses.**

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DDR Procedure

Consideration of Commands (Truth table1) cont'

- **WRITE command**
  - **To initiate a burst write** access to an active row.
  - **Selects the starting column location.**
  - **A10 determines** whether or not **auto precharge** is used**.**
  - **If auto precharge is selected,** the **row** being accessed will be **precharged** at the **end of the write burst**
  - if **auto precharge is not selected,** the row will remain open for **subsequent accesses**
  - **.DM (Data mask) : LOW**
    Data will be written to memory
    .DM (Data mask) : HIGH
    Data inputs will be ignored

Density	Column Address			Row Address
	X16	X8	X4	
64 Mb	A0⇒A7	A0⇒A8	A0⇒A9	A0⇒A11
128 Mb	A0⇒A8	A0⇒A9	A0⇒A9,A11	A0⇒A11
256 Mb	A0⇒A8	A0⇒A9	A0⇒A9,A11	A0⇒A12
512 Mb	A0⇒A9	A0⇒A9,A11	A0⇒A9,A11,A12	A0⇒A12
1 Gb	A0⇒A9	A0⇒A9,A11	A0⇒A9,A11,A12	A0⇒A13

Table 4
ROW-COLUMN ORGANIZATION BY DENSITY

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DDR Procedure

Consideration of Commands (Truth table1) cont'

= DON'T CARE

BA = Bank Address (if A10 is LOW, otherwise 'don't care')
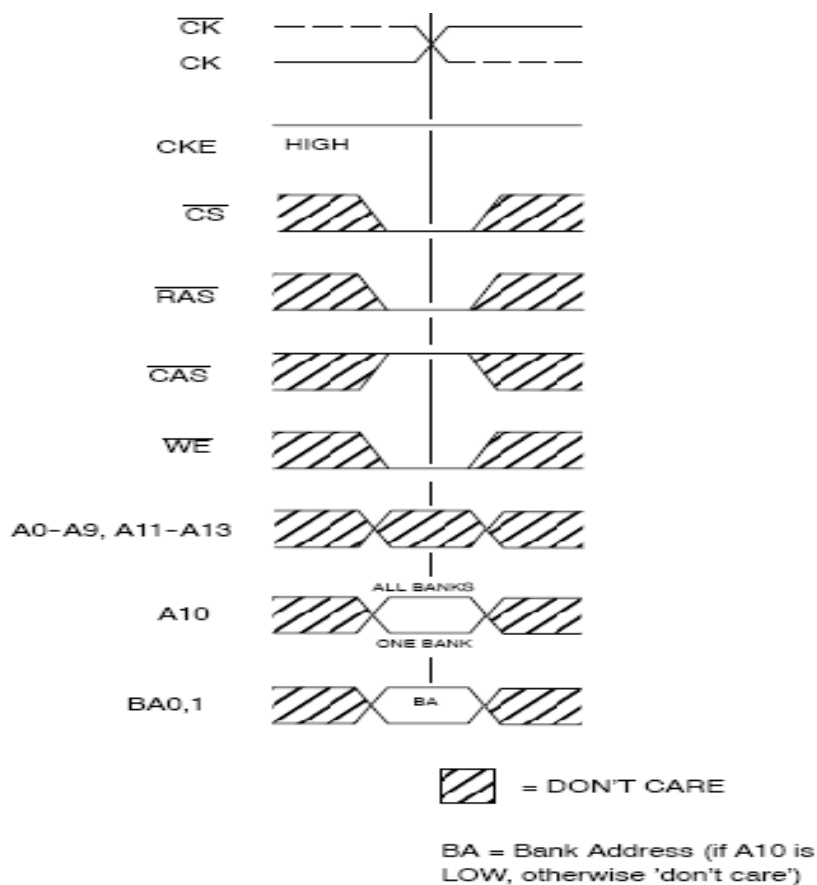
Figure 31
PRECHARGE COMMAND

■ **PRECHARGE**

- **To deactivate the open row** in a particular bank or the open row in all banks.

- **A10** determines : one or all bank

- **Once** a bank has been **precharged,** it is **in the idle state** and **must be activated** prior to any READ or WRITE commands

■ **AUTO PRECHARGE**

- **Without requiring an explicit command.**

- This is accomplished by **using A10** to enable AUTO PRECHARGE in conjunction **with a specific READ or WRITE command.**

DDR Procedure

Consideration of Commands (Truth table1) cont'

- **REFRESH REQUIREMENTS**

  - The DRAM memory cell needs to refresh **to avoid losing its data contents**.

  - This requires **refresh of the capacitor before it loses its charge.**

  - DDR SDRAMs require a refresh of all rows in any rolling **64 ms interval**.

  - **For example,** a 256MbDDRSDRAMhas **8192 rows** resulting in a tREFI of **7.8 µs**. (To avoid excessive interruptions to the memory controller : maintain 7.8 µs average refresh time)

- **AUTO REFRESH**

  - The refresh addressing is generated **by the internal refresh controller.**
  - This makes the address bits **"Don't Care"** during an AUTO REFRESH command.

- **SELF REFRESH**

  - To **retain data** in the DDR SDRAM, even if the rest of the system is powered down.
  - The SELF REFRESH command is initiated like an AUTO REFRESH command **except CKE is disabled (LOW)**
  - **To save power** (as like power down mode)

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DDR Procedure
Commands

CA = column address
BA = bank address
EN AP = enable auto precharge
DIS AP = disable auto precharge

Activate command sets the **row** address

Read or Write command sets the **column** address

Activate Command
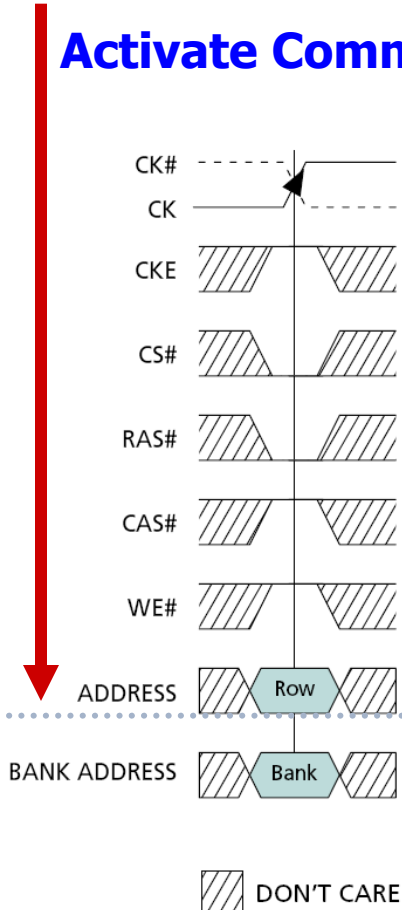
Read Command
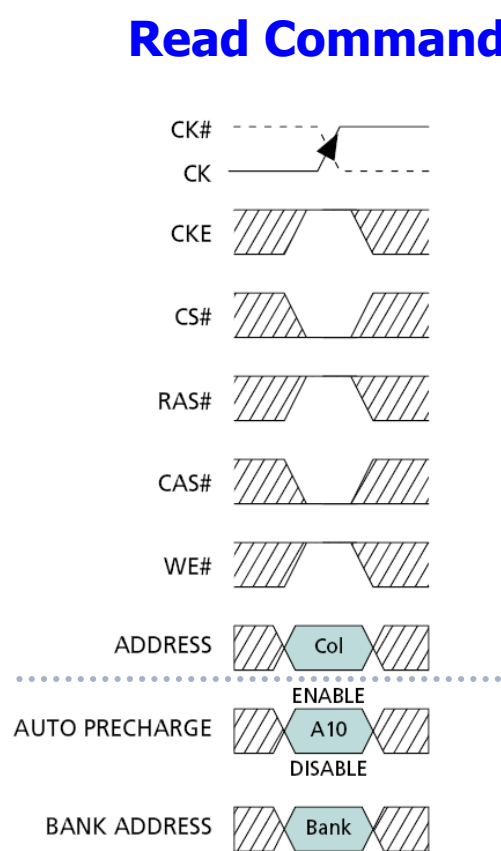
Write Command
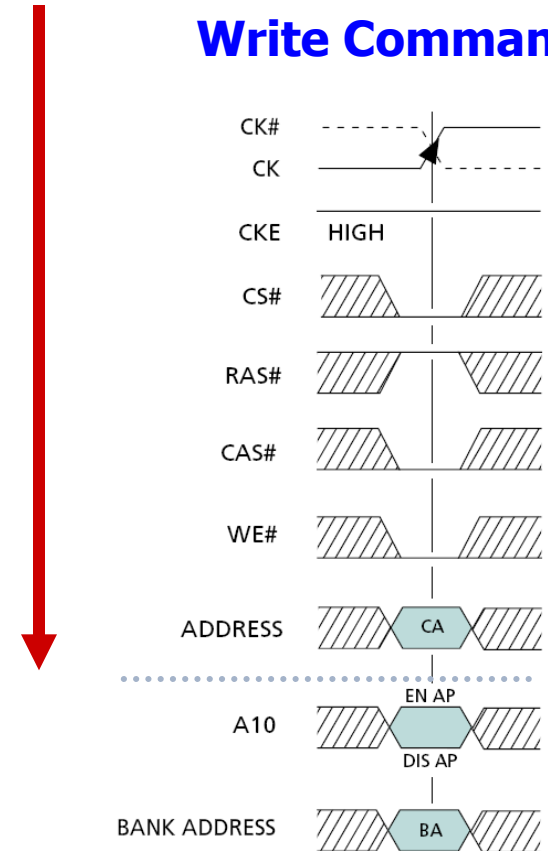
Image courtesy of Micron Technology, Inc.

DDR Procedure

< 4 > Operation

BANK/ROW ACTIVATION

Activate Command

$\overline{CK}$, CK — Clock

CKE — HIGH — Clock Enable

$\overline{CS}$ — Chip Select

$\overline{RAS}$ — Row Address Select

$\overline{CAS}$ — Column Address Select

$\overline{WE}$ — Write Enable

A0–A13 — RA — Address Inputs: A0-A13

BA0,1 — BA — Bank Address Input: 0, 1 for 4 banks
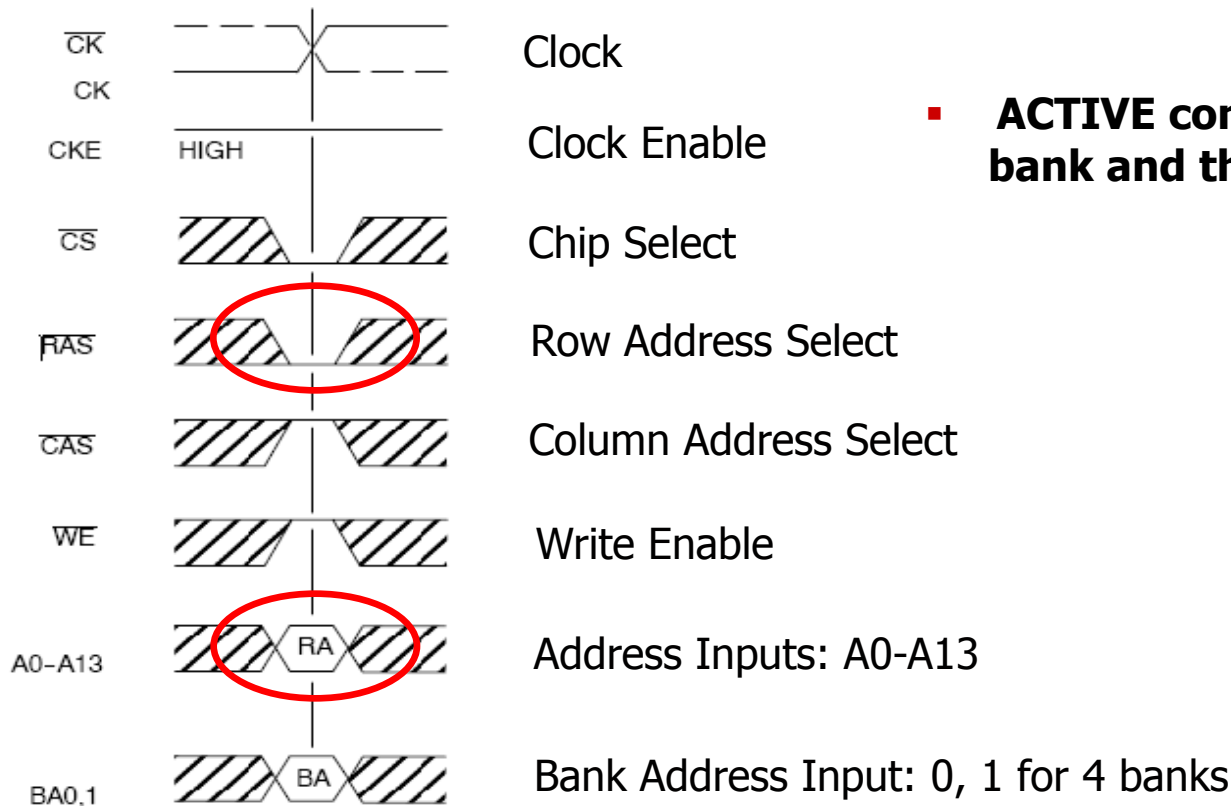
- **ACTIVE command** selects both the **bank and the row to be activated.**

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DDR Procedure

Reads

Reads Command   **Read Burst(DDR2)**

Reads Burst

Two data transfers per clock cycle

BL = 4
Shown with nominal ^tAC, ^tDQSCK, and ^tDQSQ

CL = 3
AL = 2
WL = AL + CL = 5

Burst length of 4 or 8 data bits per read command
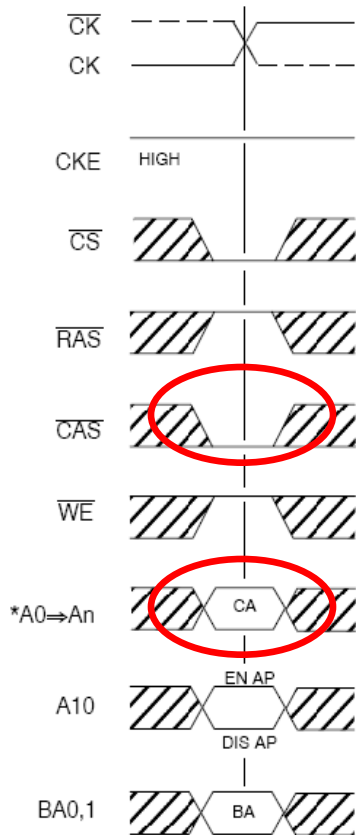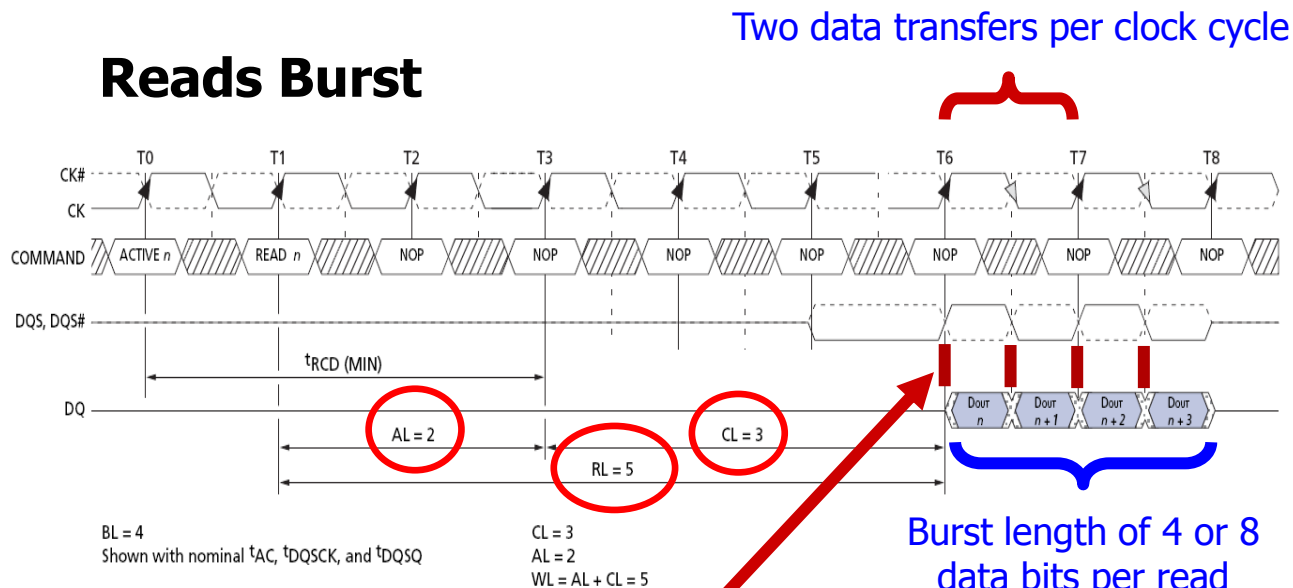
Edge aligned read data with data strobes DQS

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DDR Procedure

Writes

writes Command   **Write Burst(DDR2)**

Two data transfers per clock cycle

Write command
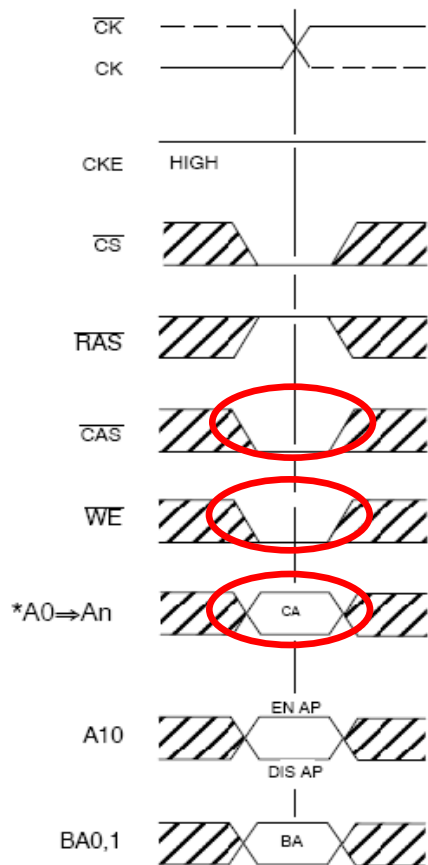
Burst length of 4 or 8 data bits per read command
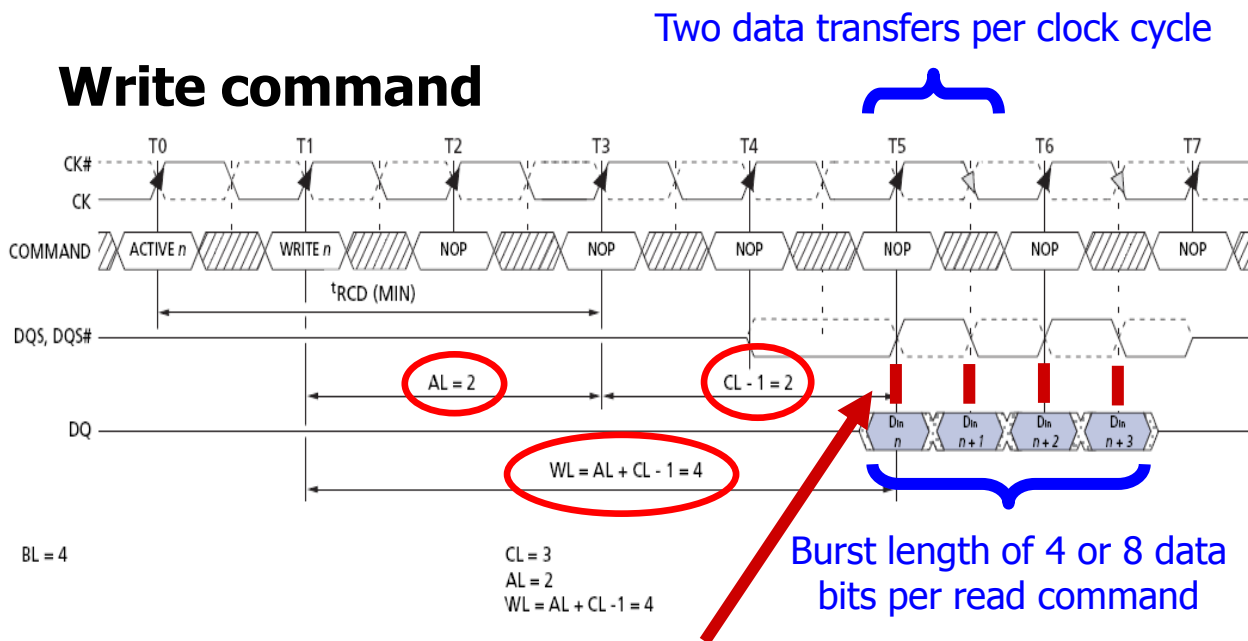
Center aligned write data with data strobes DQS

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DDR Procedure

Reads Burst

- **Read Burst (Normal)**
- **Consecutive Read Burst**
- **Non-consecutive Read Burst**
- **Random read Accesses**
- **Read to Write**
- **Read to Precharge**

Writes Burst

- **Write Burst (Normal)**
- **Write to Write**
- **Write to Write (non-consecutive)**
- **Random Write**
- **Write to Read (non-interrupting)**
- **Write to Read (interrupting)**
- **Write to Precharge**

Power Down

- CKE LOW and a stable
  clock signal must be maintained.

- **The power-down state is synchronously**
  exited when **CKE is registered HIGH**
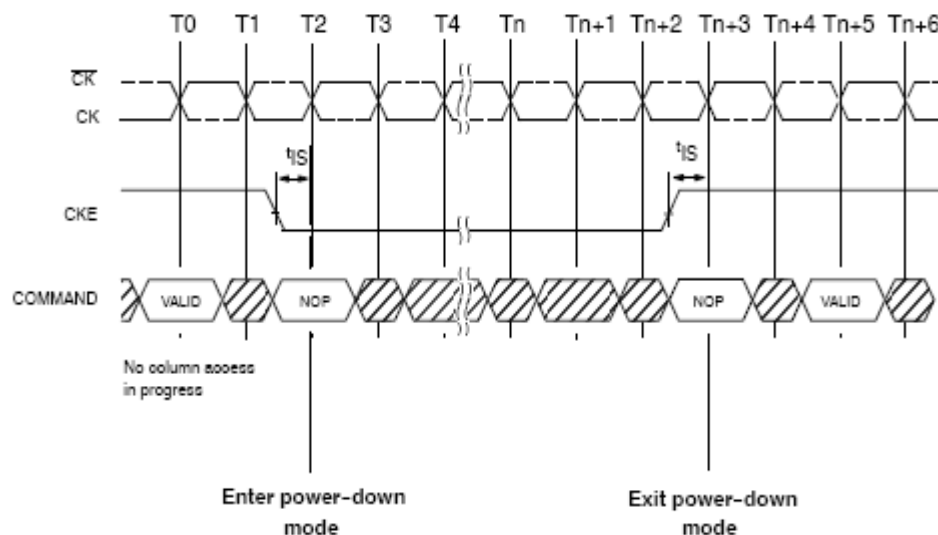
JEDEC Standards

- Electrical Timing Parameters

AC CHARACTERISTICS		DDR400A (2.5-3-3)		DDR400B (3-3-3)		DDR400C (3-4-4)			
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min (tCL, tCH)		min (tCL, tCH)		min (tCL, tCH)		ns	24, 25
Clock cycle time CL = 3	tCK	5	7.5	5	7.5	5	7.5	ns	30
CL = 2.5 CL = 2	tCK	5	12	6	12	6	12	ns	30
	tCK	7.5	12	7.5	12	7.5	12	ns	30
DQ and DM input hold time	tDH	0.4		0.4		0.4		ns	31
DQ and DM input setup time	tDS	0.4		0.4		0.4		ns	31
DQS-DQ Skew (for DQS and TSOP Package	tDQSQ		+0.4		+0.4		+0.4	ns	26
associated DQ signals) BGA Package	tDQSQ		+0.4		+0.4		+0.4	ns	26
Data Hold Skew Factor (for DQS TSOP Package	tQHS		+0.5		+0.5		+0.5	ns	25
and associated DQ Signals) BGA Package	tQHS		+0.5		+0.5		+0.5	ns	25
Write preamble	tWPRE	max(0.25* tCK, 1.5 ns)		max(0.25 *tCK, 1.5 ns)		max(0.25 *tCK, 1.5 ns)		ns	
Address and Control input hold time (fast slew rate)	tIH	0.6		0.6		0.6		ns	19, 21-23
Address and Control input setup time (fast slew rate)	tIS	0.6		0.6		0.6		ns	19, 21-23
Address and Control input hold time (slow slew rate)	tIH	0.7		0.7		0.7		ns	20-23
Address and Control input setup time (slow slew rate)	tIS	0.7		0.7		0.7		ns	20-23
Read preamble CL=3	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	28, 33
CL = 2.5		0.9	1.1	0.9	1.1	0.9	1.1	tCK	28, 33
CL = 2.0		0.9	1.1	0.9	1.1	0;9	1.1	tCK	28, 33
CL = 1.5		N/A	N/A	N/A	N/A	N/A	N/A		

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		min	max	min	max		
Clock cycle time, CL=x	tCK	5000	8000	3750	8000	ps	15
CK HIGH pulse width	tCH	0.45	0.55	0.45	0.55	tCK	
CK LOW pulse width	tCL	0.45	0.55	0.45	0.55	tCK	
Write command to DQS associated clock edge	WL	RL - 1		RL - 1		tCK	
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	- 0.25	0.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK	
Write preamble	tWPRE	0.35	x	0.35	x	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Address and control input setup time	tIS(base)	350	x	250	x	ps	5,7,9,22
Address and control input hold time	tIH(base)	475	x	375	x	ps	5,7,9,23
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input setup time (differential strobe)	tDS(base)	150	x	100	x	ps	6,7,8,20, 28
DQ and DM input hold time (differential strobe)	tDH(base)	275	x	225	x	ps	6,7,8,21, 28
DQ and DM input setup time (single-ended strobe)	tDS1(base)	25	x	- 25	x	ps	6,7,8,25
DQ and DM input hold time (single-ended strobe)	tDH1(base)	25	x	- 25	x	ps	6,7,8,26
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
DQ output access time from CK/CK	tAC	- 600	+ 600	- 500	+ 500	ps	
DQS output access time from CK/CK	tDQSCK	- 500	+ 500	- 450	+ 450	ps	
Data-out high-impedance time from CK/CK	tHZ	x	tAC max	x	tAC max	ps	18
DQS(/DQS) low-impedance time from CK/CK	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18
DQ low-impedance time from CK/CK	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	ps	13
CK half pulse width	tHP	min(tCL, tCH)	x	min(tCL, tCH)	x	ps	11,12
DQ hold skew factor	tQHS	x	450	x	400	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	19

JEDEC Standards

- Clock Parameters

Parameter	Symbol	min	max	Units
Absolute clock period	tCK(abs)	tCK(avg),min + tJIT(per),min	tCK(avg),max + tJIT(per),max	ps
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min x tCK(avg),min + tJIT(duty),min	tCH(avg),max x tCK(avg),max + tJIT(duty),max	ps
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min x tCK(avg),min + tJIT(duty),min	tCL(avg),max x tCK(avg),max + tJIT(duty),max	ps

Parameter	Symbol	DDR2-667		DDR2-800		Units	Notes
		min	max	min	max		
Clock period jitter	tJIT(per)	- 125	125	-100	100	ps	35
Clock period jitter during DLL locking period	tJIT(per,lck)	- 100	100	-80	80	ps	35
Cycle to cycle clock period jitter	tJIT(cc)	- 250	250	-200	200	ps	35
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	- 200	200	-160	160	ps	35
Cumulative error across 2 cycles	tERR(2per)	- 175	175	-150	150	ps	35
Cumulative error across 3 cycles	tERR(3per)	- 225	225	-175	175	ps	35
Cumulative error across 4 cycles	tERR(4per)	- 250	250	-200	200	ps	35
Cumulative error across 5 cycles	tERR(5per)	- 250	250	-200	200	ps	35
Cumulative error across n cycles, n = 6 ... 10, inclusive	tERR(6-10per)	-350	350	-300	300	ps	35
Cumulative error across n cycles, n = 11 ... 50, inclusive	tERR(11-50per)	-450	450	-450	450	ps	35
Duty cycle jitter	tJIT(duty)	- 125	125	-100	100	ps	35
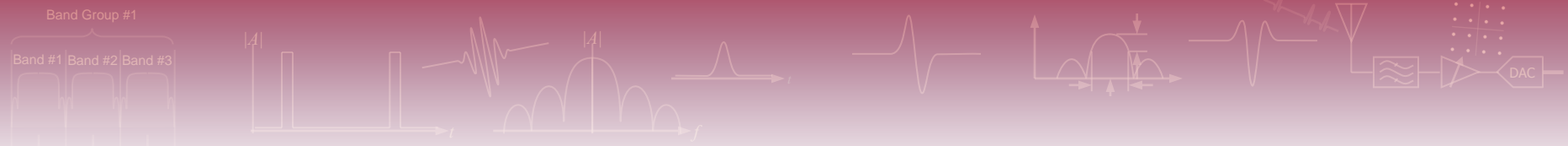
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Tektronix Visual Trigger Feature
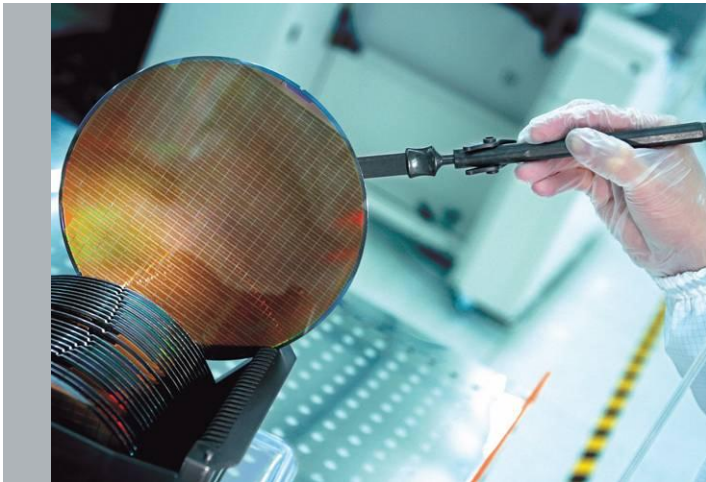
DDR Signal Separation

Hard work for Read/Write separate

DDR2-800 DQS

DQS WRITE READ DQ
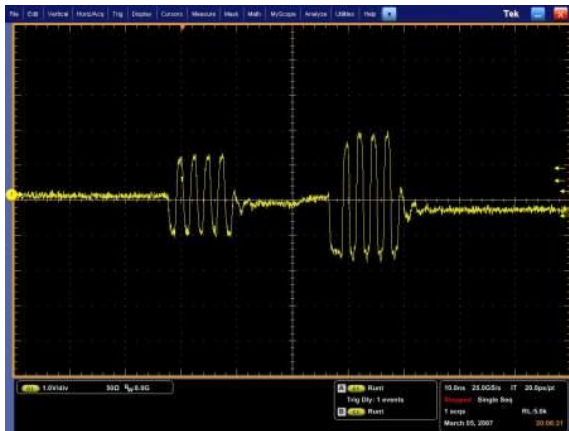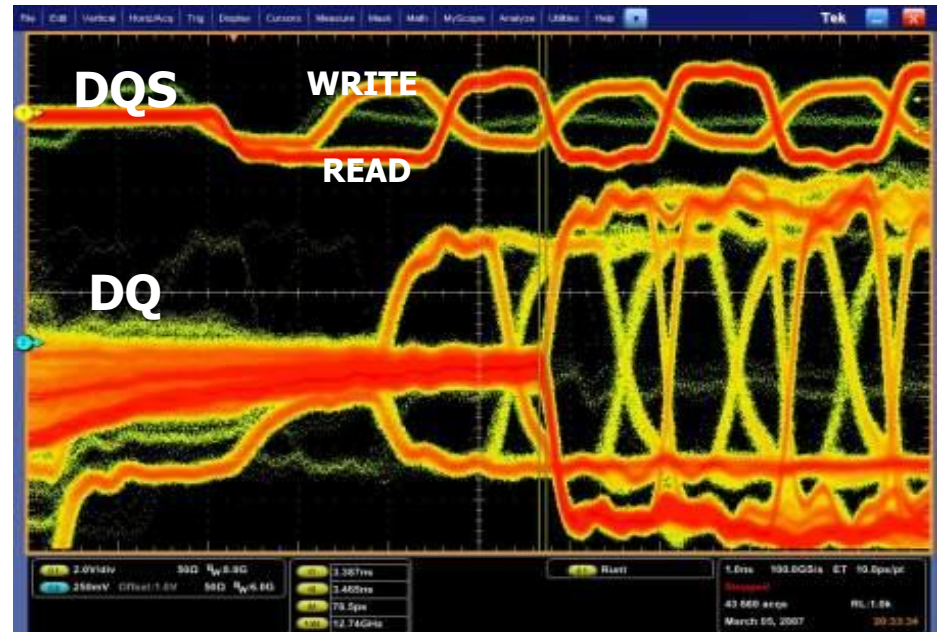
Complexity of DDR DQS,DQ with DPX

- **Complex Command Structure**
  - Column/row activate followed by reads or writes *but not always*
  - Refresh commands mimic read access
  - 4, 8, 12, 16+ bit reads/writes intermixed
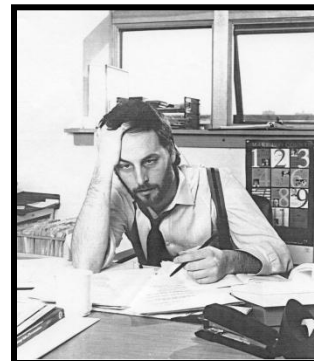
Debugging Harder, Not Smarter

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DDR Signal Separation

DDR1,2 READ/Write separate – H/W Trigger [Pin Point Trigger (Runt + Runt)]

DDR Signal Separation

DDR 3 Read/ Write separate – H/W Trigger [Window]

- **Trigger directly on DQ, DQS in real-time to isolate Reads/Writes**
- **Window trigger polarity control easily separates DDR3 Reads/Writes**
  - **DDR3 Reads are identifiable by the Strobe leaving tri-state and going low**
  - **DDR3 Writes are identifiable by the Strobe leaving tri-state and going high**
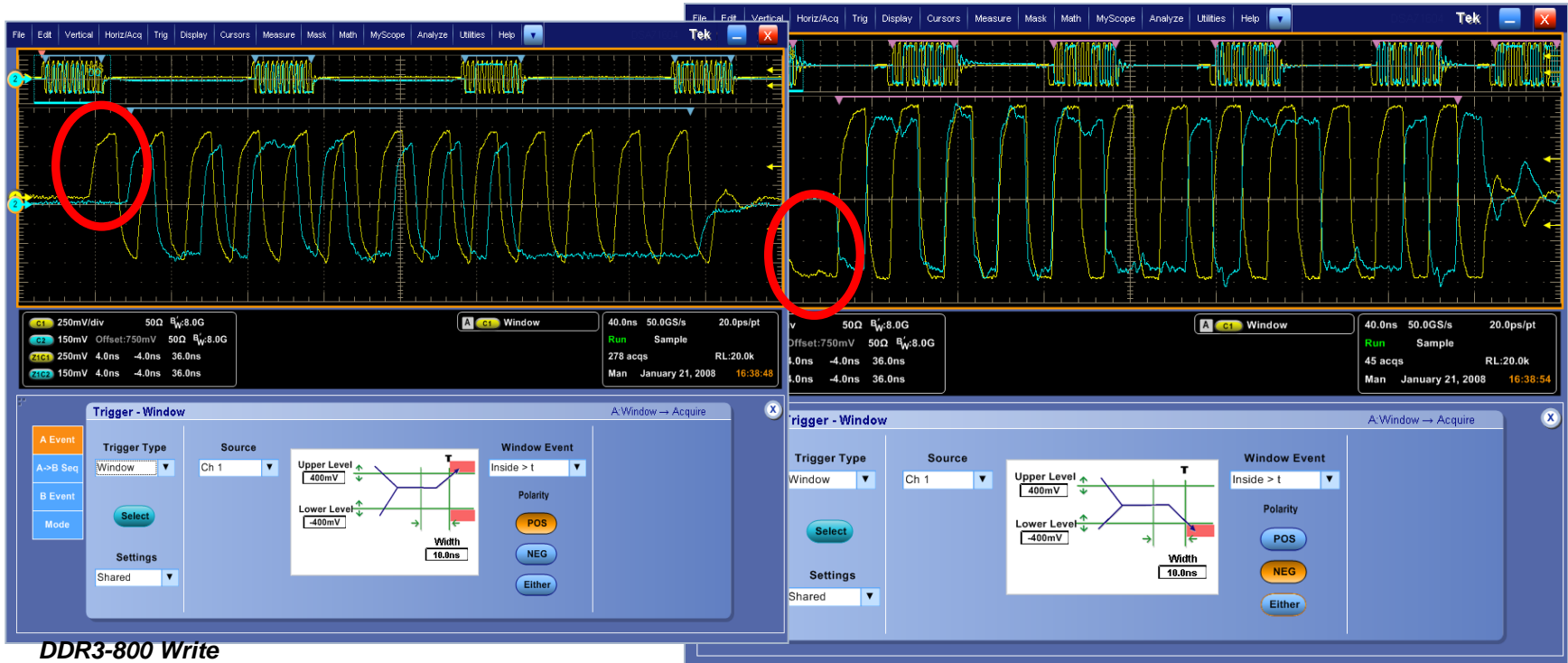
DDR3-800 Write

DDR3-800 Read

New - Visual Trigger Concept:

- User Request: I want to easily "draw" on my scope graticule to define an area of interest & set up trigger conditions

- Assign channel inputs to areas, and relationship between Areas
  - **Four analog input channels currently supported**
    (Future enhancements *may* also include Math, Ref, Digital waveforms and/or Bus (TBD))
  - **Each Area may be defined as *"Must Exist / Keep In" or "Must Not Exist / Keep Out"***
  - **Boolean equation editor defines relationship between multiple areas**
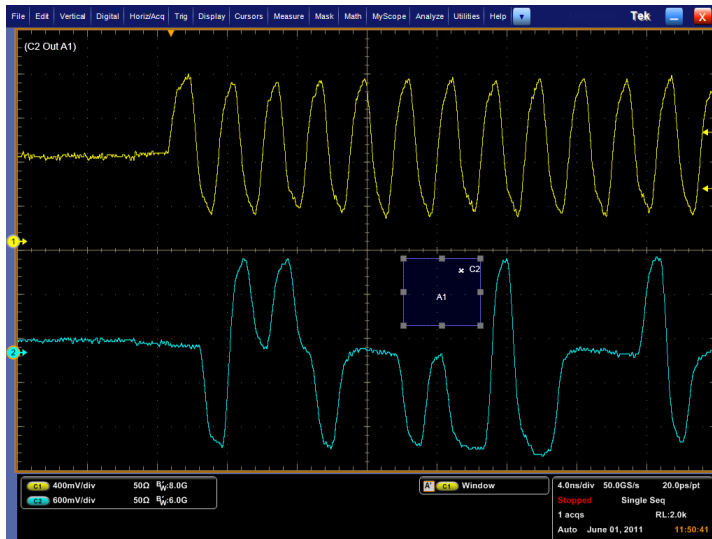
Want to easily "draw" !!!!

TRIG = Width(C1) **AND** (**[**C1 **IN** A1**] XOR [**C1 **IN** A2**]**)

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New - Visual Trigger Feature

- An area drawn on the graticule can be used for:
  - Zoom
  - Histogram
  - Gating
  - Defining a Visual Trigger Area
  - Note: Visual Trigger acts as a qualifier to a hardware trigger (e.g., Edge or Window trigger)

- Currently a "box" drawn on the scope graticule
  (with mouse or touch-screen) defines an area for:
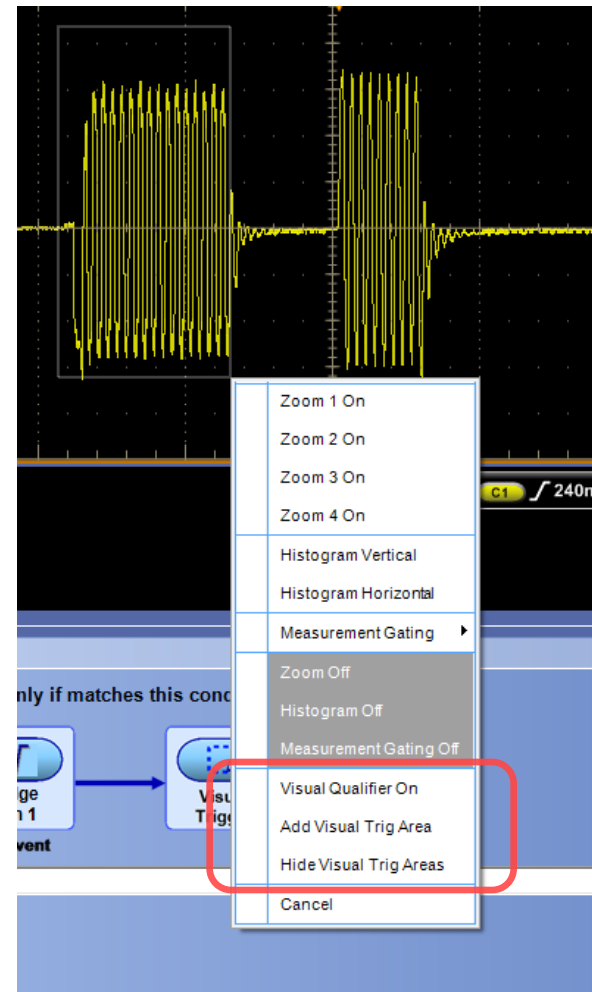
New - Visual Trigger (Unique Features)

- Right click on Area for control menu

- Areas can be easily moved or re-sized after drawing

  - **Grab corner with mouse or touch screen**

  - **Vertices are shown in Time (horiz.) and Volts (vert.) while re-sizing**

Right click on Area!!!

Easly Moved or re-sized !!!

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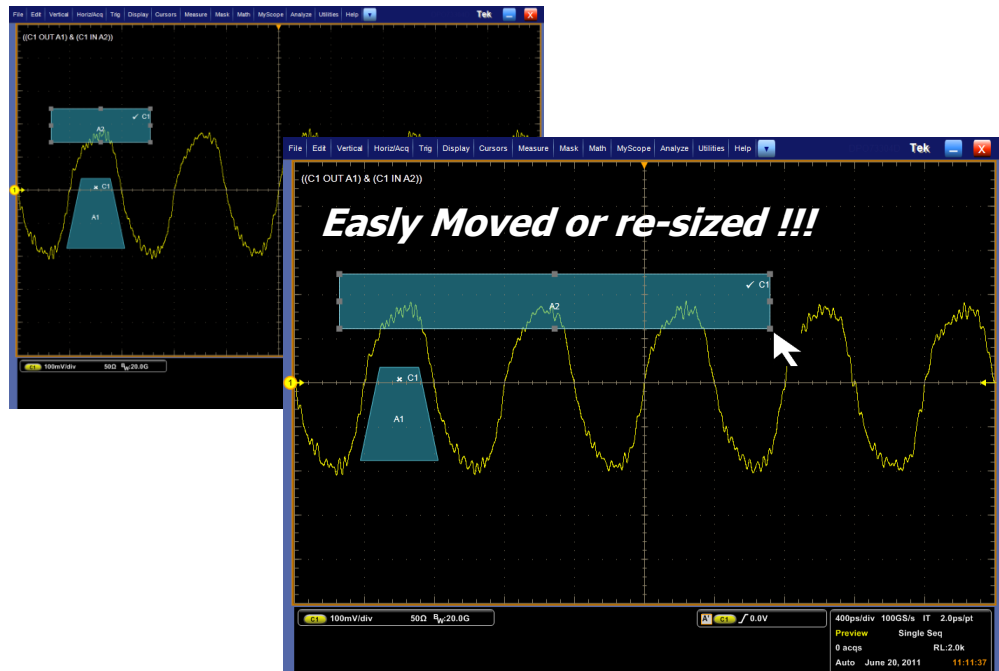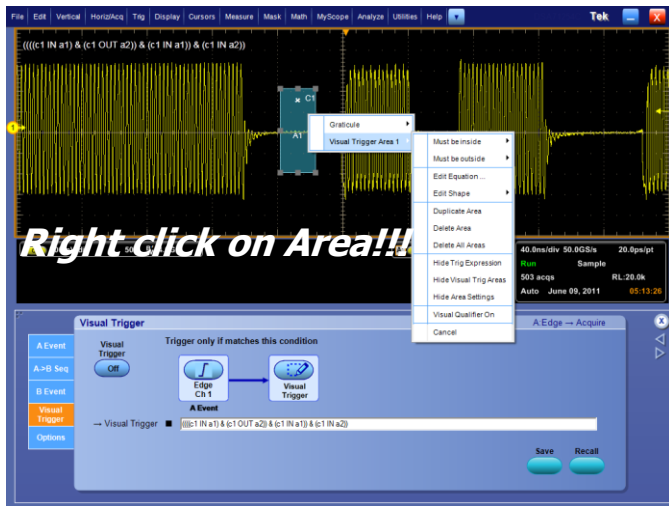
New - Visual Trigger (Unique Features)

- Up to 8 areas may be used at once
  - **One input channel assigned per Area**
  - **Multiple shape types available :**
    - **Rectangle**
    - **Triangle**
    - **Hexagon**
    - **Trapezoid**
- Equation Editor Control Window – select from right-click menu
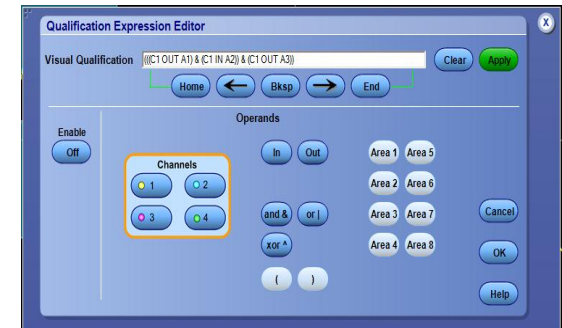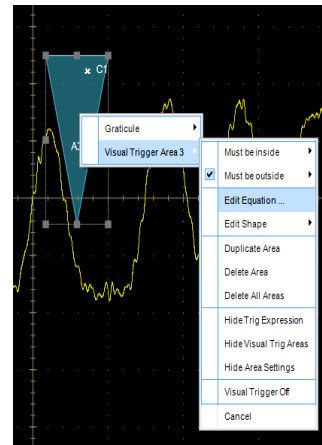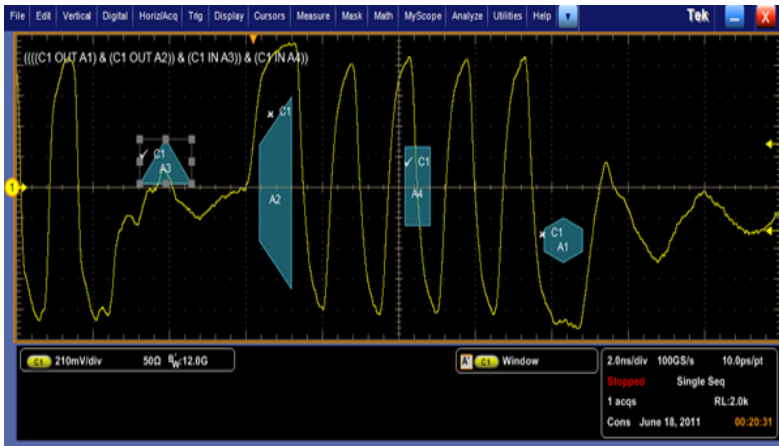
Visual Trigger Feature – DDR Eye Example

- "Before VT" eye - Visual trigger turned off. All ranks are shown. PinPoint window HW trigger to detect start of Write burst.
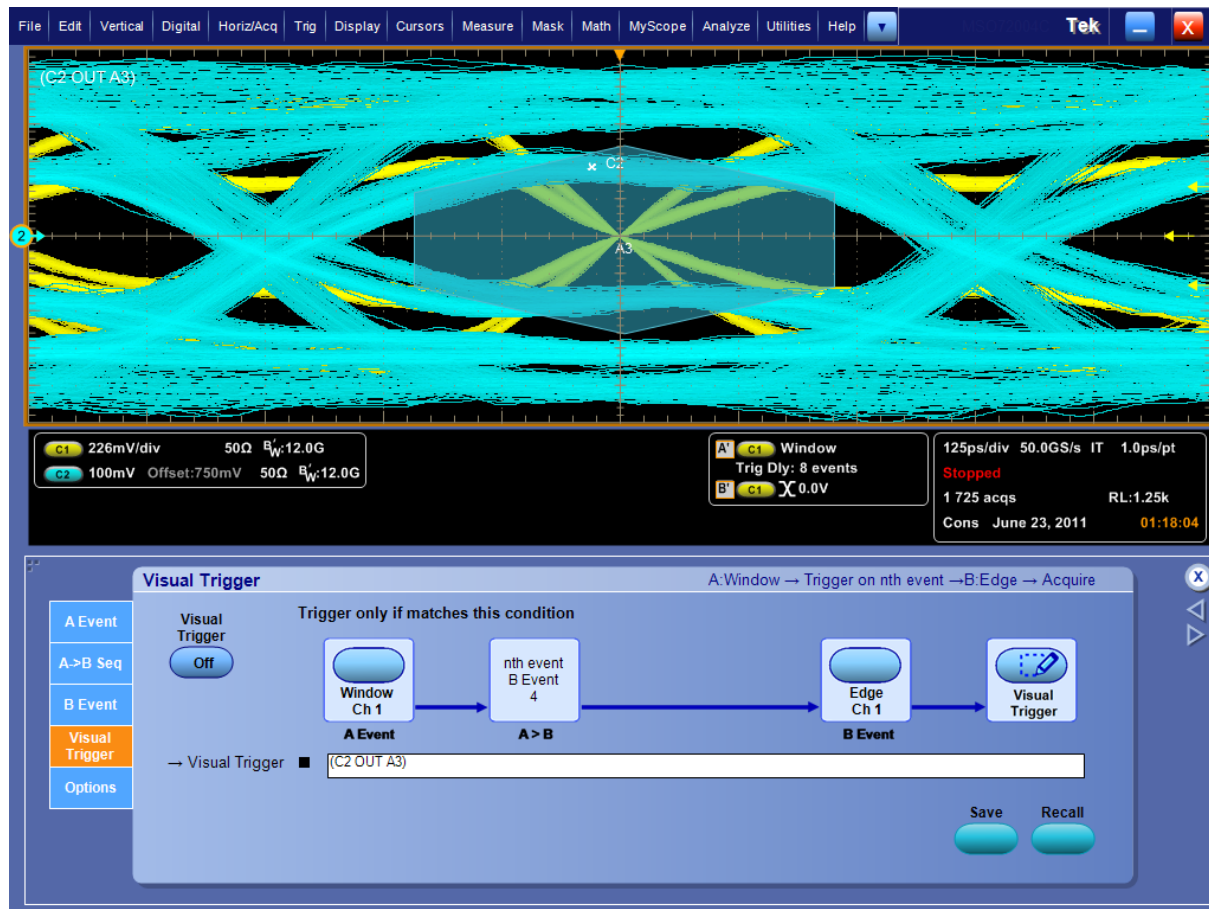
Visual Trigger Feature – DDR Eye Example

- "After VT" eye - Visual trigger enabled. DQ has to stay outside the hexagon. 2 keep out areas on the strobe (Ch1). Now, only the target rank is shown.
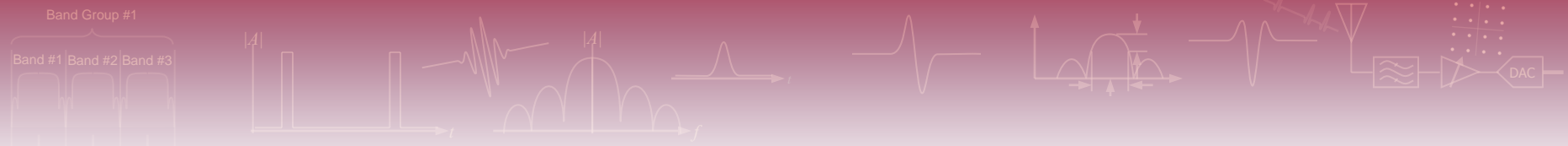
Customized DDR Measurement Software

(DDRA Analysis Software)
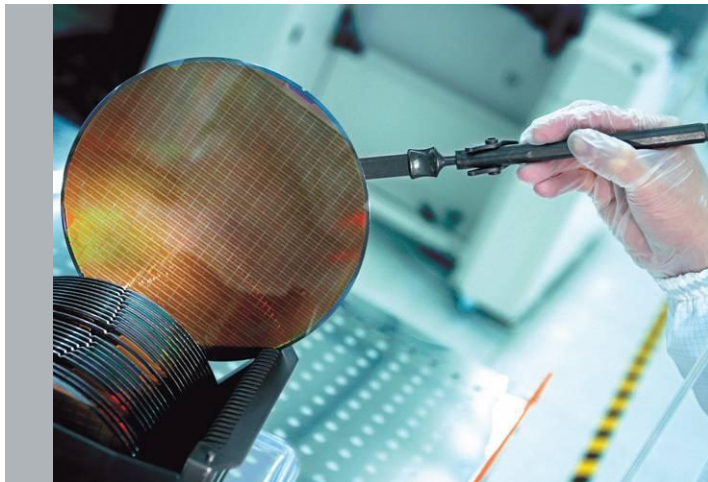
DDR Analysis

Option DDRA: Oscilloscope-based DDR tool that accelerates the validation of high-speed DDR memory bus interfaces

- Auto-configuration Wizard Guides Easy Setup and Test
- Analyze All Read/Write Bursts in the Entire Acquisition
- Plot DQS and DQ Eye Diagrams for Reads and Writes
- Perform JEDEC Conformance Tests with Pass/Fail Limits
- Use Chip Select to Qualify Multirank Measurements
- Easily Move Between Conformance-test and Analysis/Debug Tools
- Automatically Produce Consolidated Reports with Pass/Fail Information, Statistical Measurement Results, and Test-setup Information

Validation of DDR, DDR2, DDR3, LP-DDR and GDDR in one tool

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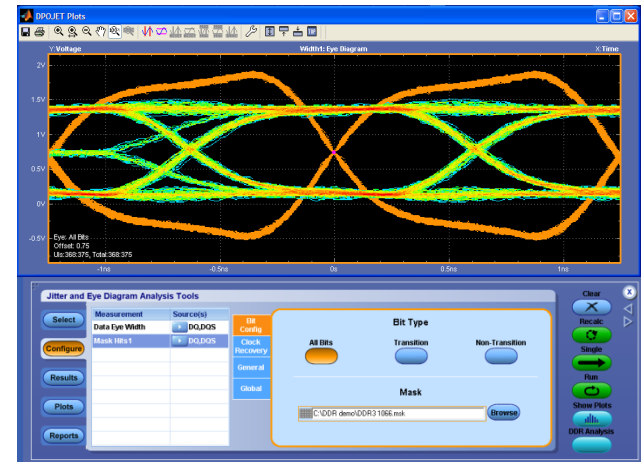
MSO / DDRA Integration Approach to Burst Detection

- Use MSO's Logic Pattern or Logic State triggering on the DDR control bus signals (CS, RAS, CAS, WE, etc.) to capture the desired burst type.

- Availability of the DDR-specific bus definitions with DDRA are made available using the (configurable) symbol table.

- The existing ASM wave shape filters (Analog DQS/DQ method) are then used to delimit the exact burst edges.

- Using command bus state, specific transactions can be isolated by MSO
  - For example, locate only Reads from a specific memory rank
  - Advanced Search & Mark on analog signals is then used for fine burst positioning to gate measurements
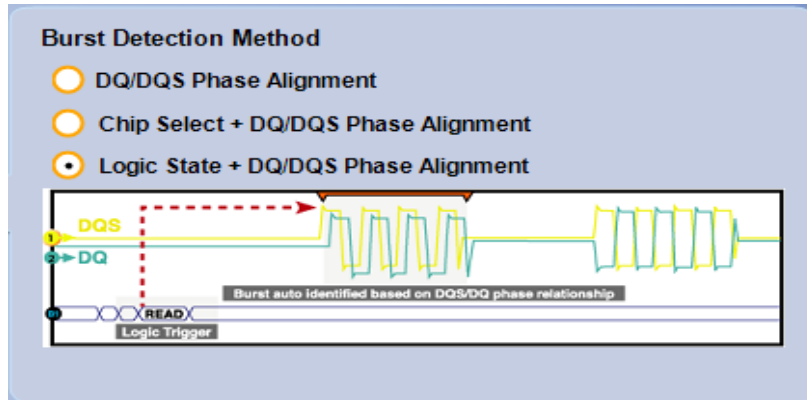
Support for Multiple DDR Generations

- JEDEC Standards specify unique measurements & methods

- DDRA = One Application SW Package
  - DDR
  - DDR2
  - DDR3
  - LPDDR
  - LPDDR2
  - GDDR3
  - GDDR5

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Automated Test Setup

- The setup process guides you through a step-by-step ("wizard") interface

Step #1
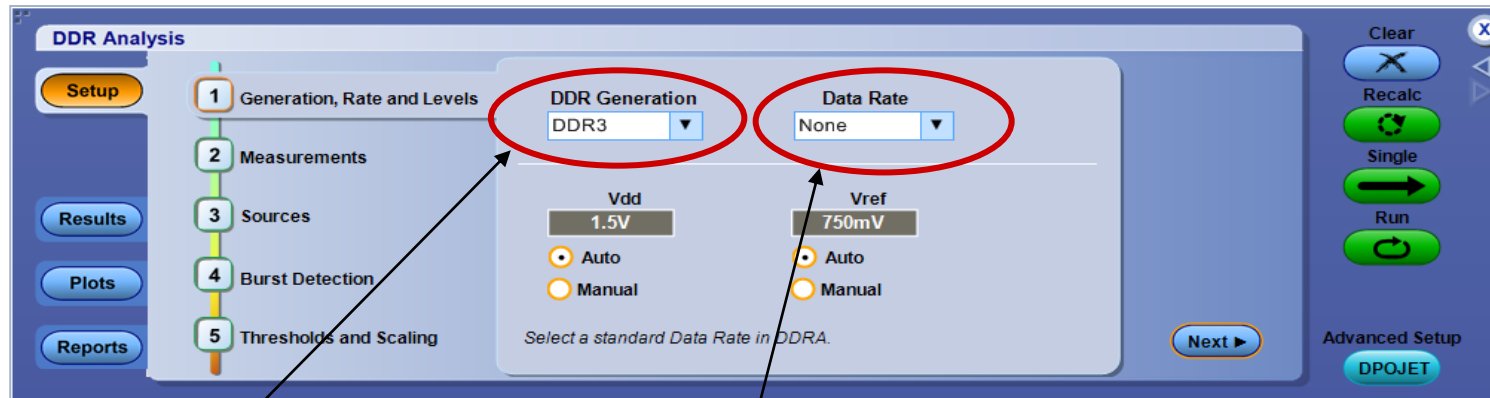
Select DDR Generation

Select DDR Rate

Step #2
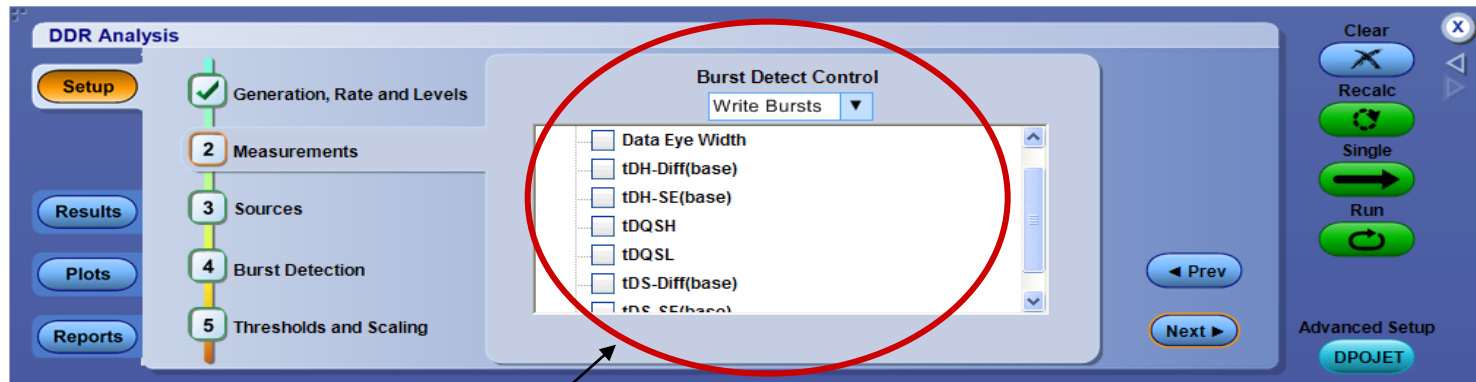
Choose measurements (Read / Write / Clock)

Source and Level Selection

Step #3

Identify scope input channels for DQS, DQ, CLK

Optional **Chip Select** qualifier

Step #4

Let DDRA set Read/Write Burst Detect Levels automatically, or customize if needed

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Threshold and Auto Scaling
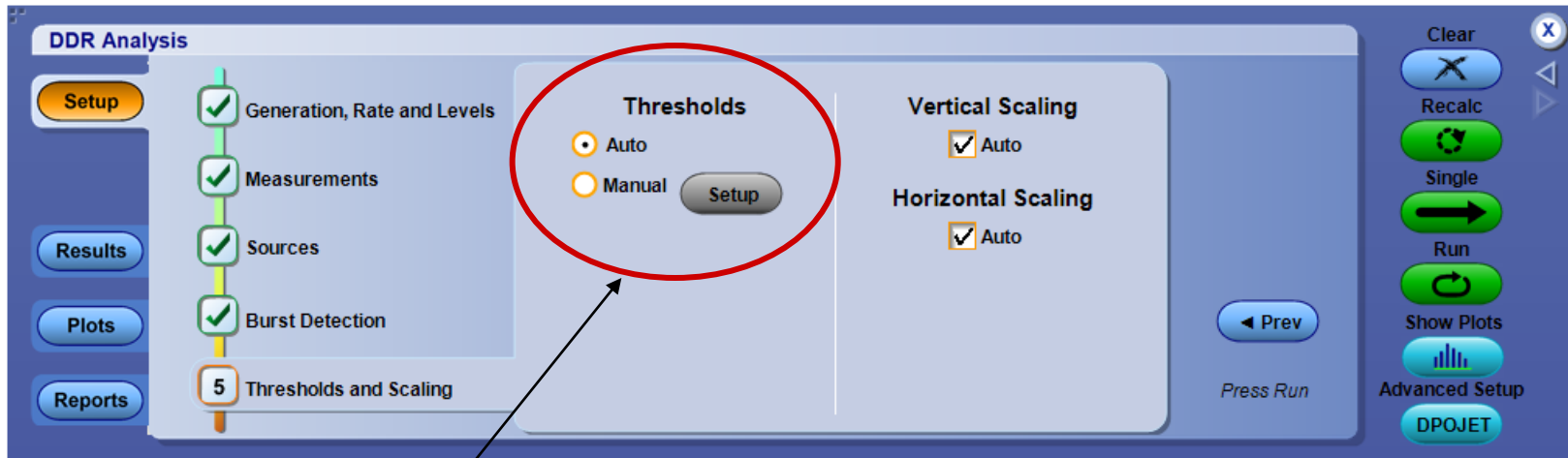
Let DDRA set Measurement Ref Levels automatically (per JEDEC), or customize if needed

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Signal Acquisition
Identify all Read/Write bursts

- Use Search & Mark to identify all Read/Write bursts in acquisition

- Marks qualify bursts for measurement by DPOJET

- Easily Identify, mark & measure all Read / Write bursts
  - Scroll through marked reads / writes across the entire waveform record
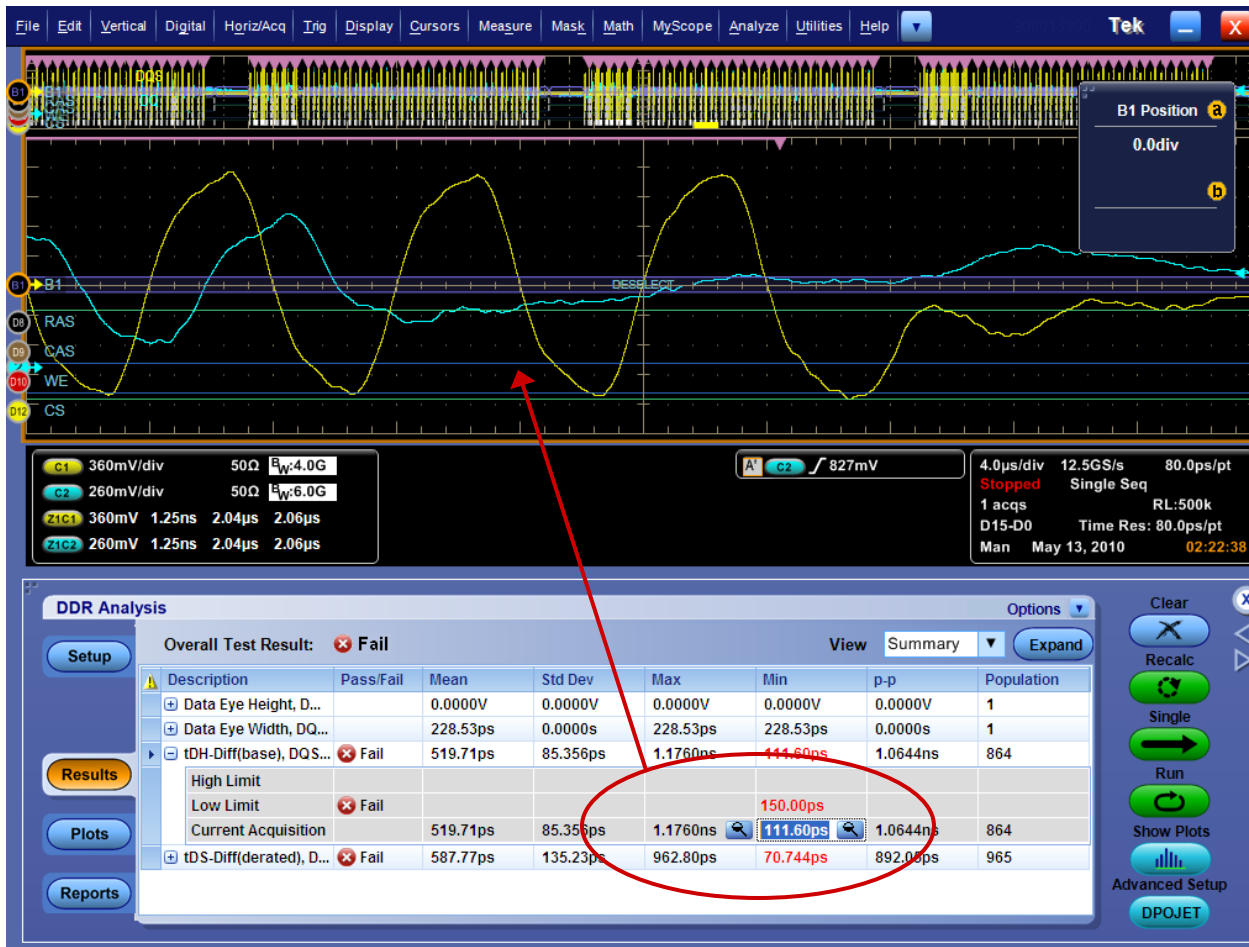 - Measurements performed on ALL reads/writes
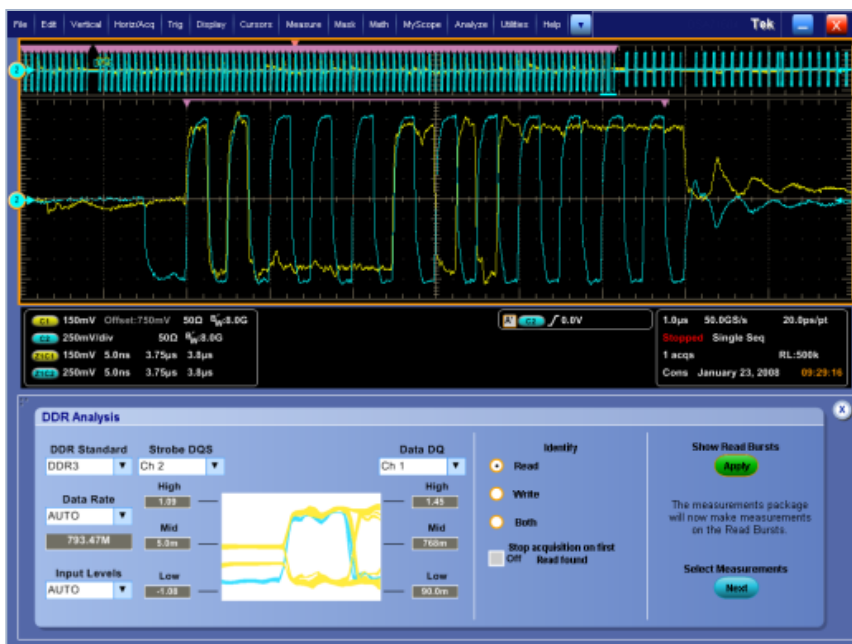
Qualify measurements for Read bursts


Qualify measurements for Write bursts

DPOJET Debug Tools

- **"Find Worst Case Events" feature**
  - Zoom to waveform from Min / Max for <u>every</u> measurement result

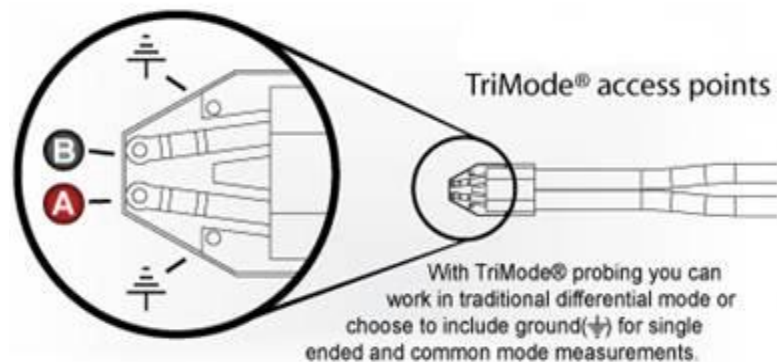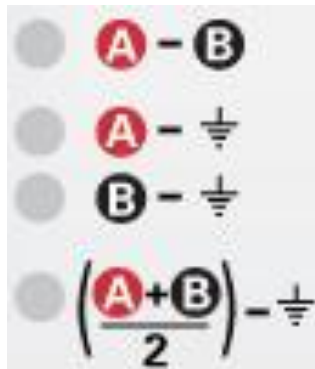**Tektronix®**

Results and Statistical Validity

- DDRA has access to all plotting & debug tools in DPOJET

- To have confidence in your test results, you need 100's, 1000's or even more observations of each measurement

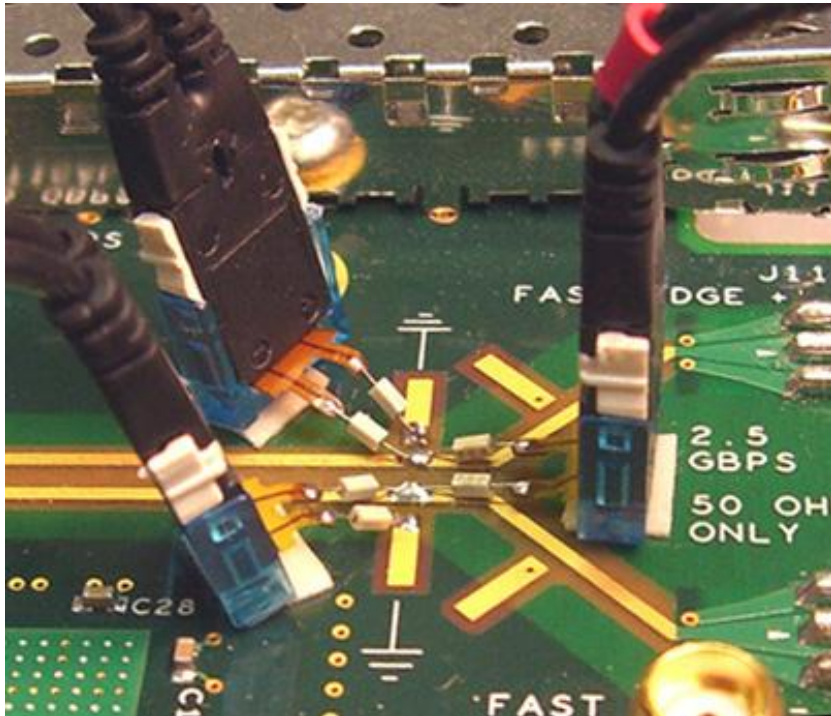- As a practical matter, measurement throughput is essential
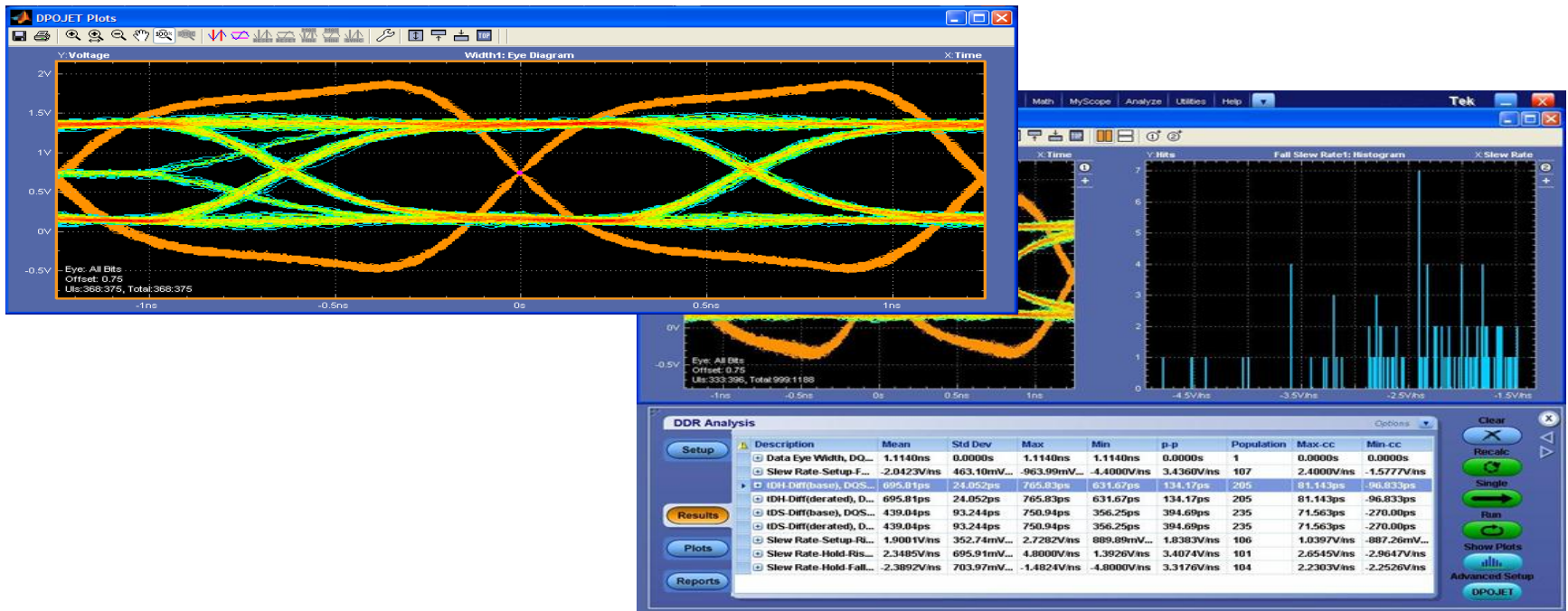
PASS/FAIL Measurements & DDR2 Eye Diagram – showing both DQ and DQS eyes

TriMode Probing

- TriMode, with a single probe-DUT connection, allows:
  - Traditional differential measurements: V+ to V-
  - Independent single ended measurements on either input
    - V+ with respect to ground
    - V- with respect to ground
  - Direct common mode measurements: ((V+) + (V-))/2 with respect to ground
- Many standards require both differential and single-ended voltage limit measurements. Requires two separate probes – Until Now!
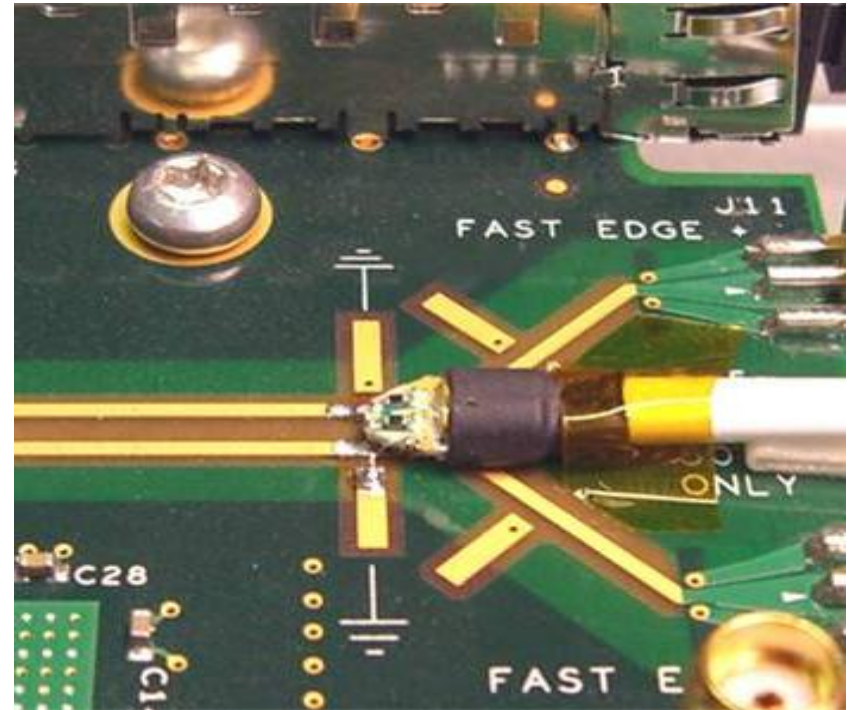

TriMode® access points

With TriMode® probing you can work in traditional differential mode or choose to include ground(⏚) for single ended and common mode measurements.

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Before and After

Before TriMode Probing
1 Probe for Differential
2 Probes for SE and Common Mode
or
1 Probe Soldered and Re-soldered 3 times
2 Probes for Common Mode

After TriMode Probing
1 Probe and 1 setup for
Differential, SE and Common Mode

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New P7500 Series Probe Tips

**TriMode Micro-Coax Tip
020-2955-xx
1.7" (43mm)**

**Socket Cable
020-2954-xx
4.1" (104mm)**

**High Temp Tip
020-2958-xx
0.48" (12mm)**

**Damped Wire Tip
020-2959-xx
1.7" (43mm)**

Summary – World's Best DDR Test Solution

COMPLETE SOULTIONS

- **DPO/DSA/MSO70000C Series Oscilloscopes**

- **P7500 Series TriMode Probes**

- **DDRA** - DDR1/2/3, LP-DDR and GDDR3,GDDR5 support in one tool

- **Visual Trigger** – EASY function of Trigger!!

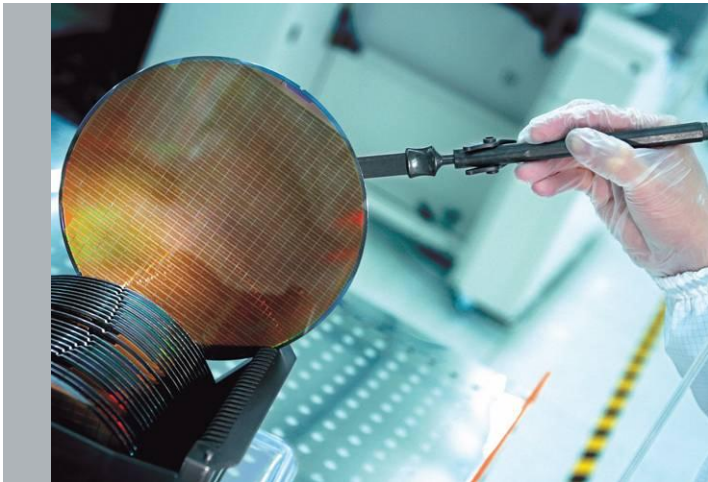- Provides JEDEC validation, characterization and full measurement support

Performance

- Based upon highest performing oscilloscopes and software analysis tools

- TriMode probing enables three measurements with a single probe connection

- Read/Write burst identification on <u>all</u> bursts

- Automated setup with JEDEC pass/fail limits

Comprehensive Analog Verification & Debug Tools for All DDR Versions

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Thank You

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