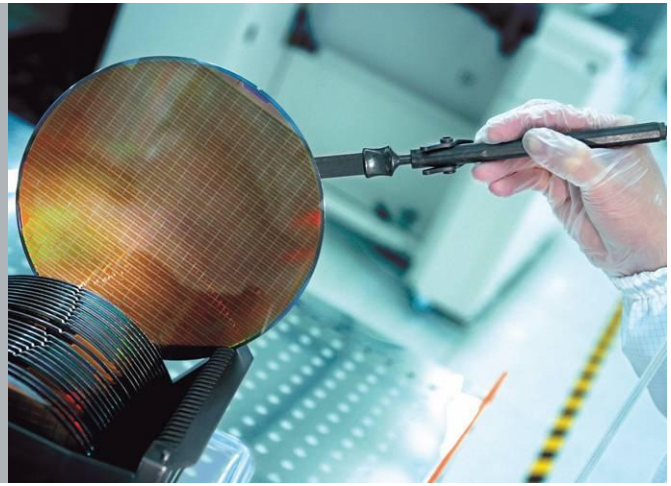
MIPI Physical Layer Test Solutions

D-PHY and M-PHY



KE Lee
Application Engineer Manager

Tektronix®

Agenda

- MIPI® Technologies
- D-Phy testing
  - Tx
  - Scopes-Decode: CSI, &DSI
  - Rx
- M-Phy testing
  - Tx (New update Mar'12)
  - Scopes-Decodes:, 8b-10b, DigRF, LLI (New), &UniPro (New)
  - Rx
- Summary, Q&A

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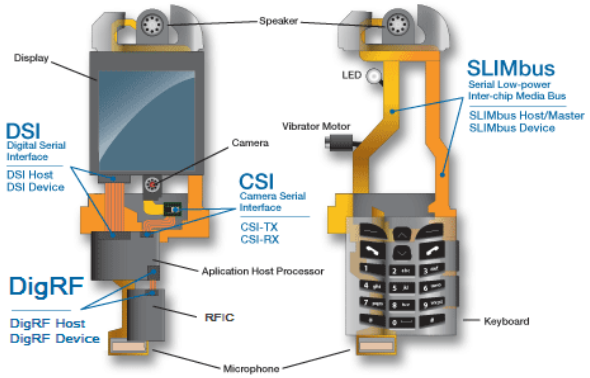
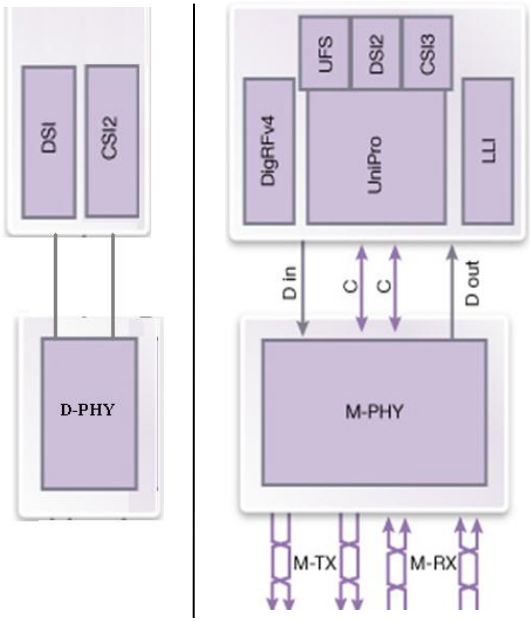
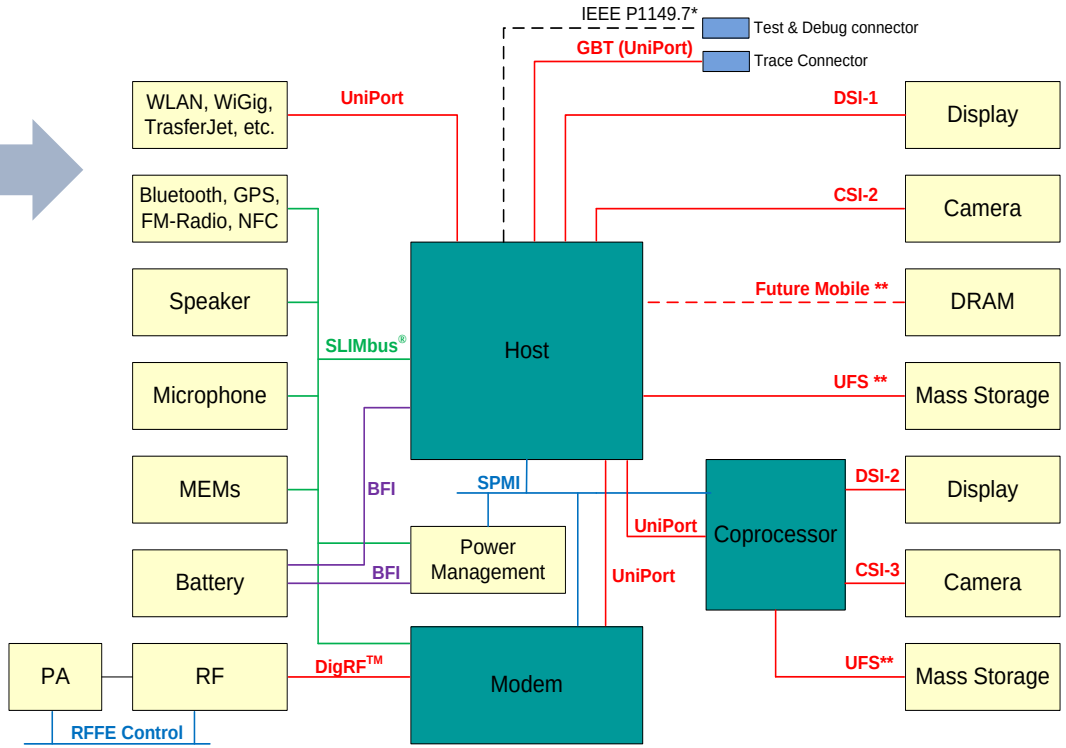
MIPI Technologies Overview
Example of a Mobile Platform







D-PHY/M-PHY based
SLIMbus
SPMI/RFFE

UniPort : UniPro + D-PHY or M-PHY

(*) Transferred to IEEE
(**) Liaison with JEDEC

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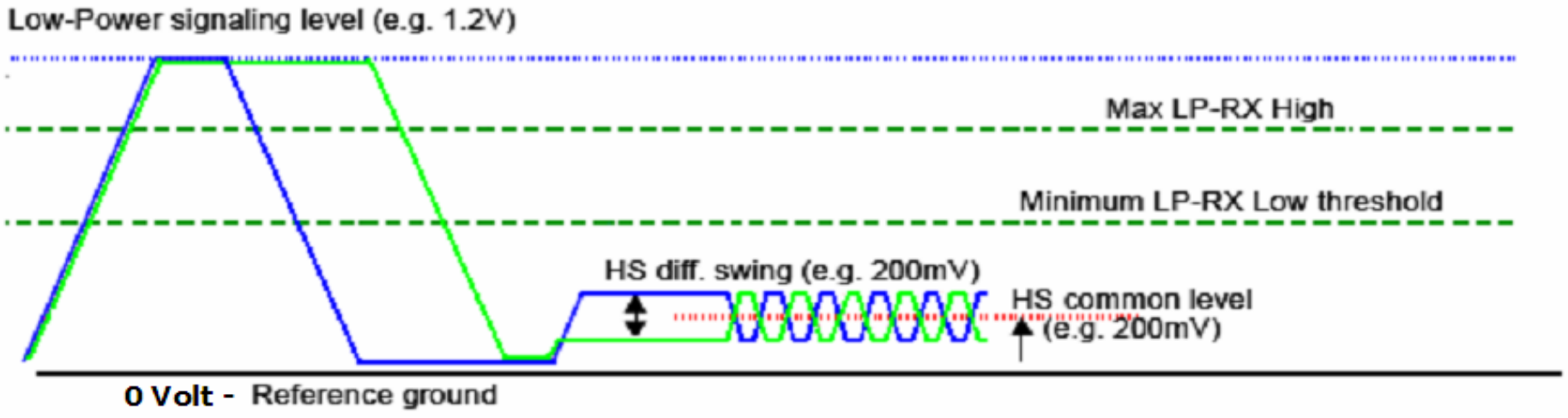
What is D-PHY ?

- It's a PHY standard for interfacing Camera (CSI) & Display (DSI)
- Two modes of transmission
  - High Speed (HS) and Low Power (LP)
- Modes are mixed during the operation
  - Transitions from LP to HS and back to LP on the fly
- Maximum Data Rate
  - High Speed mode: 80 Mbps – 1 Gbps, Typically at ~500 Mbps.
  - Low Power mode: Up to 10 Mbps
- Bus termination
  - 50 ohms in HS
  - Hi-Z in LP



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D-PHY Testing Challenges

- Logo testing is not required, but Optional.
  - MIPI is Chip-to-Chip/ Chip-to-Peripheral interface, similar to a DDR bus.
  - Mobile Phones do not need compliance logo, unlike USB/SATA devices
- No two MIPI devices are the same
  - Variable Data Rates
  - Up to 4 lanes of Data traffic,
  - Multiple different data formats
  - Specification enables custom limits.
- Characterization is significantly important
  - Mobile OEMs select the suppliers based on characterization reports.

- **Many measurements – 49**
  - **Clock Lane**
  - **Data Lane**
  - **Clock data Timing**
- **Test Equipment &Setups need to be Very Flexible**

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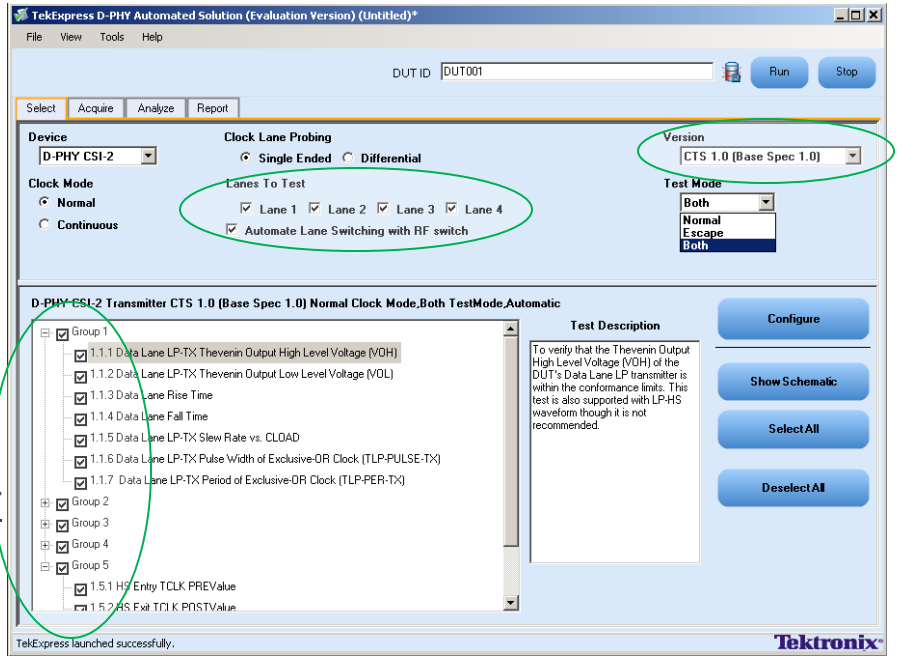
D-PHY Tx : Opt.D-PHYTX Conformance Test Solution

- Opt.D-PHYTX : D-PHY Automated Solution
  - TekExpress option for Fully-Automated testing
  - Provides Conformance and Characterization Testing
  - Based on Latest D-PHY Base Spec v1.0 and UNH's Conformance Test Suite v1.0.
  - Runs on 7K/C and 70K/B/C scopes
  - Opt.TEKEXP is Pre-Requisite
- Differentiation
  - **Un-parallel** Automation (Auto-Cursors)
  - **100%** Widest Test Coverage
  - Conformance to Latest CTS (v1.0)
  - Based on Latest Base spec (v1.0)
  - Fully-Automated for Multi-lane DUTs
  - Fully-Automated Temperature Chamber
- Value proposition
  - Custom-limits/ Limits-Editing
  - Test Reports with Pass/Fail summary, margins, & "Zoom-in" Waveform Captures
  - Tek 3.5GHz scope is the minimal configuration for accurate testing
  - D-PHY extension spec (1.5G) ready



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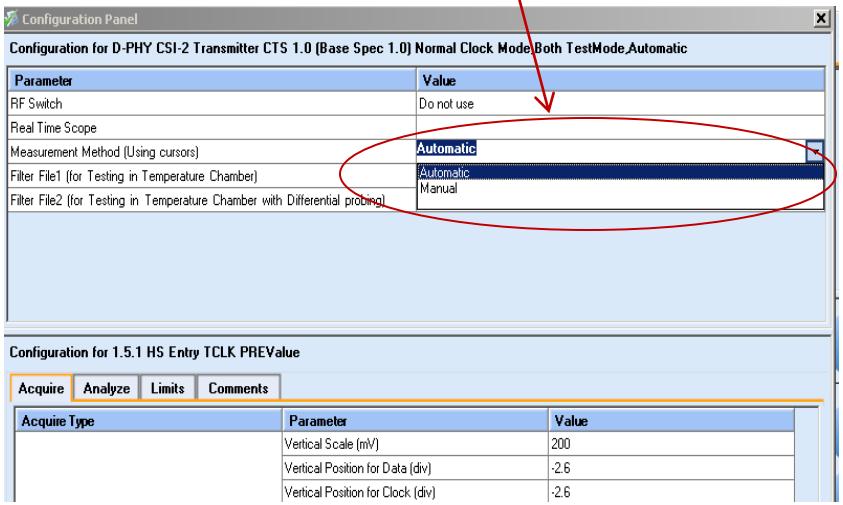
D-PHY Tx : Opt.D-PHYTX Features

Test Reports with “ZOOM-IN” screenshots of the cursors placement for each test.

Switch between Automatic and Manual cursor palcement. In Automatic mode, software can find the LP/HS regions automatically. Switch to Manual for debug or if your signal is too noisy.



D-PHY Tx : New 1.5G Data Rate Extension Spec v1.01

Spec Draft is Ready. Expected to be released for adaption in late-CY11

- Both Opt.D-PHYTX and Opt.D-PHY are **Fully-Supported**.
  - All Measurement Algorithms remain same
  - Only “Limits” vary for following Five parameters for 1.5G datarate.
    1. HS rise/fall time (tr, tf),
    2. VOD mismatch (dVOD),
    3. TX data to clock skew (TSKEW[TX]),
    4. RX setup and hold times (TSETUP[RX], THOLD[RX]),
    5. TX/RX return loss (SddTX, SddRX).
  - Both Opt.D-PHYTX and Opt.D–PHY support Limits Editing today.

- Tektronix is involved in the D-PHY 1.5G Extension discussions.

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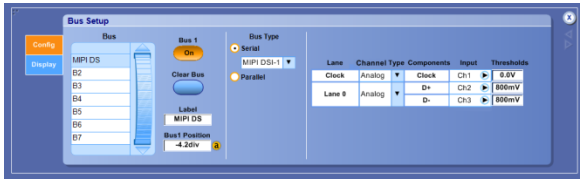
D-PHY Decode: Opt.SR-DPHY for DSI/ CSI-2 Decode

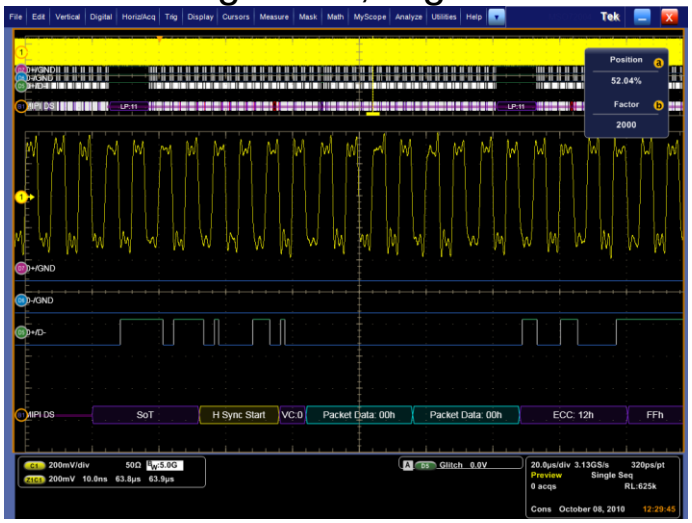
Simultaneous Acquisition

- Probe using Analog, Digital or Mixed Channels
- Simultaneous probing of DSI &CSI using MSO channels
- Working on multi-lane support, using high performance MSO digital channels
- Supported on all 7KC, 70KC and MSO70K scopes. (**Win7-OS only**)
  - Option key bit #25
- Software installed as part of TekScope firmware v6.1.2.4 or later.
  - Browse to TekScope Menu --> Vertical --> Bus Setup --> Select Bus Type as Serial-- > Select MIPI DSI or CSI from the drop down list.



Probe using Mixed Channels

Analog Clock, Digital Data



Digital Clock, Analog Data

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D-PHY Tx &Decode: Recommended Test Setup

www.tek.com/MIPI

- Scope
  - DPO7354 or DPO/DSA/MSO70404/B/C or higher for rise time accuracies
- Probes
  - For 7Ks: 4x TAPxx/ P6245/ P6249, or 4x TDP3500 (clock is non-continuous), or 3x TDP3500 (clock is continuous).
  - For 70Ks: 4xP7240, or 4xP73xx (clock is non-continuous), or 3xP73xx (clock is continuous).
- Scope Software
  - Opt.D-PHYTX on TEKEXP for Conformance Test
  - Opt.D-PHY on DPOJET for Debug, Analysis &Characterization
  - Opt.SR-DPHY for Decode of CSI &DSI traffic
- Fixtures
  - As MIPI is a chip-to-chip interface, most DUT setups are LIVE with Master-Slave/ Receiver-end connected.
  - For live-setups: No Fixtures required.
  - For non-live setups:
    - No standard fixture is defined.
    - We recommend following UNH-IOL Termination boards: www.iol.unh.edu/services/testing/mipi/MIPI_Test_Fixture_Order_Form.doc

P7380 probe used with a probe-tip

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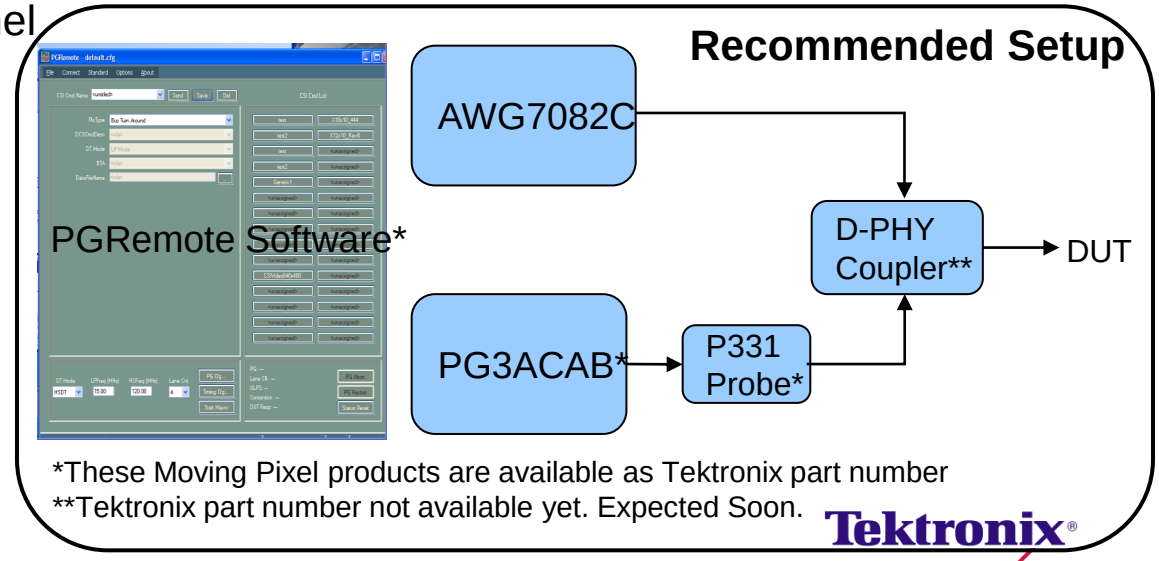
D-PHY Rx : Test Solution Overview

Simple, Quick, Easy and Re-usable

- 100% Coverage to Rx CTS
  - Meets all the requirements in UNH-IOL CTS document (v0.98)
- Quick and Easy setup
  - No complex VXI system, just stand alone instruments, and a probe.
- Cost effective solution
  - 70% Lower list price vs Competition
- Re-usable for Protocol tests
  - PG3A is the Only 4 channel solution for CSI &DSI test
- PG3A Pattern Generator
  - Controls clock and signaling to establish link with DUT
  - Adjusts voltage levels, packet type, etc to stress test receiver
- AWG7082C Generator
  - Adds jitter and interference to the D-PHY signals



D-PHY Rx : Test Solution Overview

100% Test Coverage

Group 1 LP - RX voltage and timing requirements			
Test	**Title**	**Page**	**Equipment**
2.1.1	LP - RX Logic 1 Input Voltage (V_{IH})	108	PG
2.1.2	LP - RX Logic 0 Input Voltage, non-ULP State (V_{IL})	110	PG
2.1.3	LP - RX Logic 0 Input Voltage, ULP State ($V_{IL-ULPS}$)	112	PG
2.1.4	LP - RX Minimum Pulse Width Response (T_{MIN-RX})	113	PG
2.1.5	LP - RX Input Hysteresis (T_{HYST})	114	PG
2.1.6	LP - RX Input Pulse Rejection (e_{SPIKE})	116	PG + AWG + DC Power Supply
2.1.7	LP - RX Interference Tolerance (V_{INT} and f_{INT})	120	PG + AWG
2.1.8	LP - CD Logic Contention Thresholds (V_{ILCD} ans V_{IHCD})	122	PG + AWG

Group 2 LP - RX Behavioral Requirements			
Test	**Title**	**Page**	**Equip**
2.2.1	LP - RX Initialization Period (T_{INIT})	125	PG
2.2.2	ULPS Exit: LP - RX $T_{CLKULPS}$ Timer Value	126	PG
2.2.3	Clock Lane LP - RX Invalid/Aborted ULPS Entry	127	PG
2.2.4	Data Lane LP - RX Invalid/Aborted Escape Mode Entry	128	PG
2.2.5	Data Lane LP - RX Invalid/Aborted Escape Mode Command	130	PG
2.2.6	Data Lane LP - RX Escape Mode Invalid Exit (Informative)	132	PG
2.2.7	Data Lane LP - RX Escape Mode, Ignoring Post Trigger-Command Extra Bits	134	PG
2.2.8	Data Lane LP - RX Escape Mode Unsupported/Unassigned Commands	136	PG

Group 3: HS - RX Voltage and Setup/Hold Requirements			
Test	**Title**	**Page**	**Equipment**
2.3.1	HS - RX Common Mode Voltage Tolerance ($V_{CMRX(DC)}$)	139	PG
2.3.2	HS-DX Differential Input High Threshold (V_{DTH})	141	PG
2.3.3	HS-DX Differential Input Low Threshold (V_{DTL})	143	PG
2.3.4	HS - RX Single-Ended Input High Voltage (V_{SHA})	144	PG
2.3.5	HS - RX Single-Ended Input Low Voltage (V_{SLA})	146	PG
2.3.6	HS - RX Common Mode Interference 50MHz - 450MHz (delta VCMRX(LF))	148	PG + AWG
2.3.7	HS - RX Common Mode Interference Beyond 450MHz (delta VCMRX(HF))	150	PG + AWG
2.3.8	HS - RX Setup/Hold and Jitter Tolerance	151	PG + AWG

Group 4: HS - RX Timer Requirements			
Test No.	**Title**	**Page**	**Equipment**
2.4.1	Data Lane HS - RX $T_{D-TERM-EN}$ Value	156	PG
2.4.2	Data Lane HS - RX $T_{HS-SETTLE}$ + $T_{HS-SKIP}$ Tolerance	158	PG
2.4.3	Data Lane HS - RX $T_{HS-SETTLE}$ Value	160	PG
2.4.4	Data Lane HS - RX $T_{HS-SETTLE}$ Tolerance	162	PG
2.4.5	Data Lane HS - RX $T_{HS-TERM}$ Value	164	PG
2.4.6	Clock Lane HS - RX $T_{CLK-TERM-EN}$ Value	166	PG
2.4.7	Clock Lane HS - RX $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ Tolerance	167	PG
2.4.8	Clock Lane HS - RX $T_{CLK-SETTLE}$ Value	169	PG
2.4.9	Clock Lane HS - RX $T_{CLK-SETTLE}$ Tolerance	171	PG
2.4.10	Clock Lane HS - RX $T_{CLK-MISS}$ Value	173	PG
2.4.11	Clock Lane HS - RX $T_{CLK-PRE}$ + $T_{CLK-POST}$ Tolerance	175	PG

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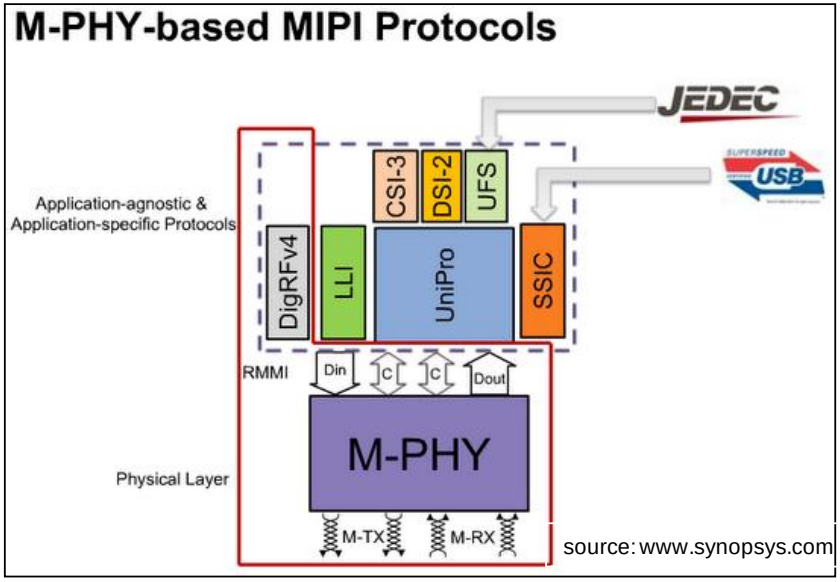
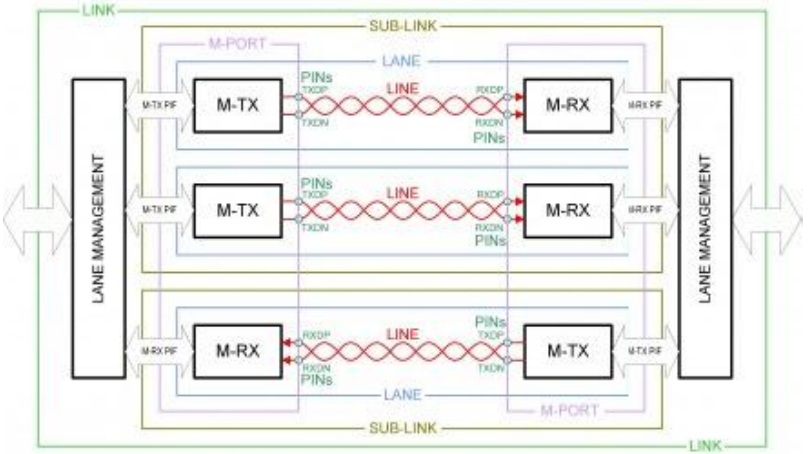
What is M-PHY ?

- M-PHY is a high-speed serial interface to the DigRFv4, UniPro, LLI, CSI-3 and DSI-2 interconnect standards of the MIPI Alliance, and the UFS and SSIC protocol standards of JEDEC and USB-IF respectively.
- M-PHY is a flexible architecture that allows the implementer to support high data rates at minimal power, cost & I/O redesign, for applications such as High Definition Video
- A Fast, Scalable, Serial Communications Architecture
  - Link – Connects M-PHY Transmitter to an M-PHY Receiver
  - Sub-link – Manage one or more lanes
  - Lane – Operation defined in the protocol (DSI, CSI, UniPro, DigRF)





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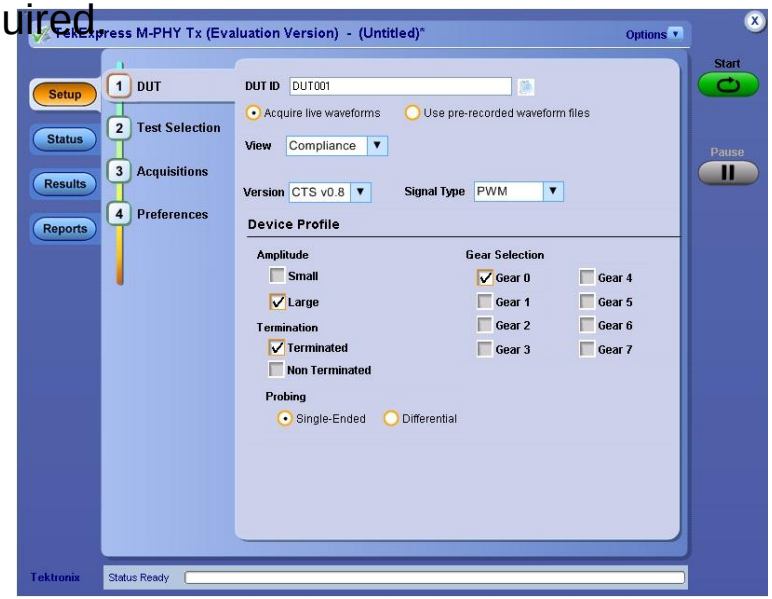
M-PHY Testing Challenges

M-PHY Signal Characteristics							
Signaling mode	**Datarates**			**Amplitudes**		**Impedance**	
	Gears	A (Gbps)	B (Gbps)	Large	Small	Resistive Terminated	Non Terminated
High Speed (HS)	G1	1.25	1.45	Terminated: 160-240mV, Non-Terminated: 320-480mV	Terminated: 100-130mV, Non-Terminated: 200-260mV	50 ohms	-
	G2	2.5	2.91				
	G3	5	5.83				
PWM (ie. TYPE-I)	Gears	Min (Mb/s)	Max (Mb/s)			50 ohms	10k ohms
	G0	0.01	3				
	G1	3	9				
	G2	6	18				
	G3	12	36				
	G4	24	72				
	G5	48	144				
	G6	96	288				
	G7	192	576				
SYS (ie. TYPE-II)			576 (Mb/s)			50 ohms	10k ohms

- Higher data rate will increase importance of Signal Integrity of links
  - More emphasis on timing/jitter and noise (signal integrity)
  - Receiver testing will be needed to stress-test resulting BER
- Number of Measurements
- Termination – Restive or not Terminated.
  - LS mode can operate either of them
  - HS mode it is always terminated, so swings are halved.
- Type-I and Type-II are Low speed modes, and are NOT interoperable
  - Type-I operates on independent local clocks. Type-II requires a shared Ref-clock.
  - DUTs may support both

M-PHY Tx : New Opt.M-PHYTX Automated Solution

- Opt.M-PHYTX
  - TekExpress (2.0) option for Single-button Automated transmitter testing
  - Provides Conformance &Debug Testing to the latest M-PHY Base Spec v1.0 &UNH's Conformance Test Suite.
  - Runs on DPO/DSA70KB/C/D or MSO70K/C scopes (6GHz and above)
  - TekExpress framework &license is included.
  - Opt.DJA is pre-requisite. Opt.M-PHY not required
- Differentiation
  - Most Complete Test coverage
    - (95% HS, 74% PWM).
  - Seamless Debug on failures.
  - Scope-based Power-Spectral Density tests



- Value proposition
  - For Gear2 M-PHY Tx testing, Tek 8GHz oscilloscope is sufficient. Where as, competition recommends a 12GHz or 13GHz oscilloscope.
  - For Gear3 M-PHY Tx testing, Tek 20G oscilloscope is sufficient. Where as, competition recommends a 25GHz oscilloscope.

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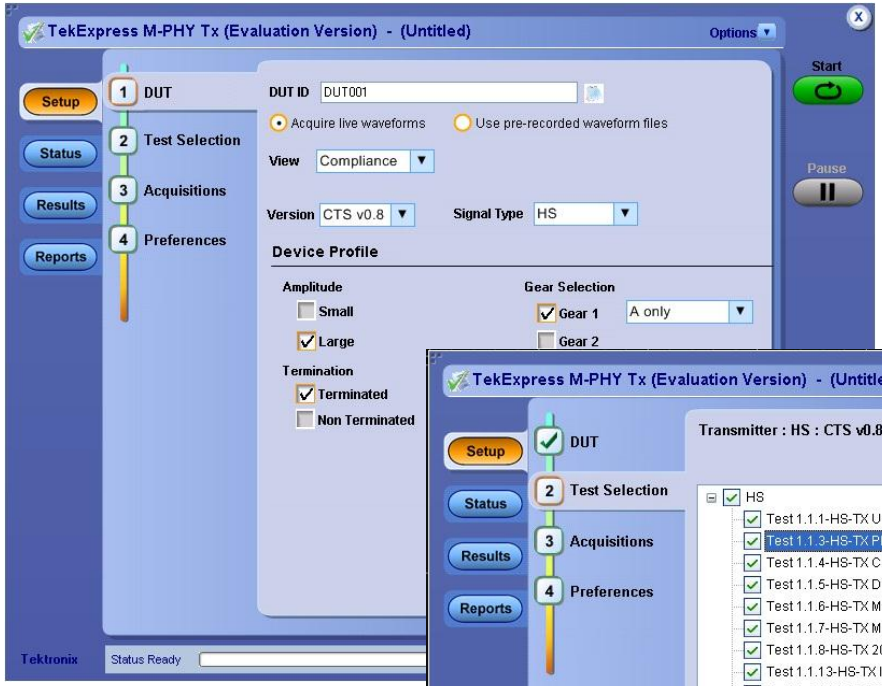
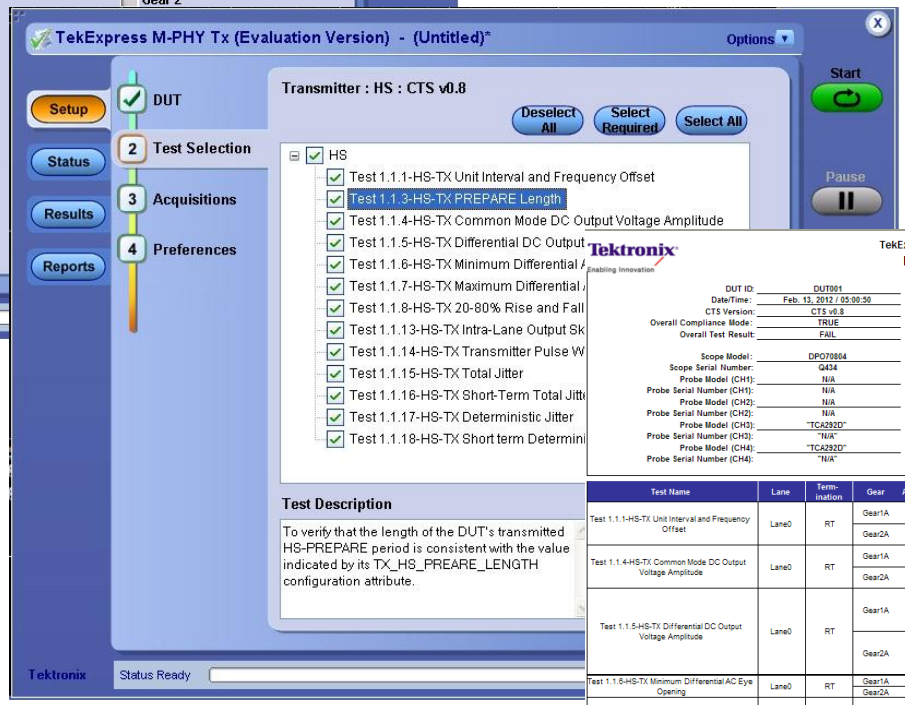
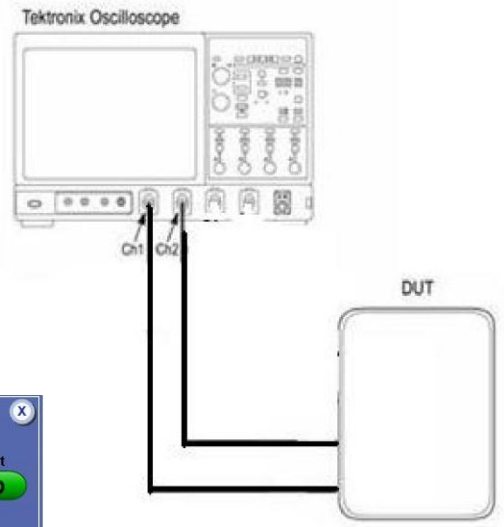
M-PHY Tx : New Opt.M-PHYTX Automation Features

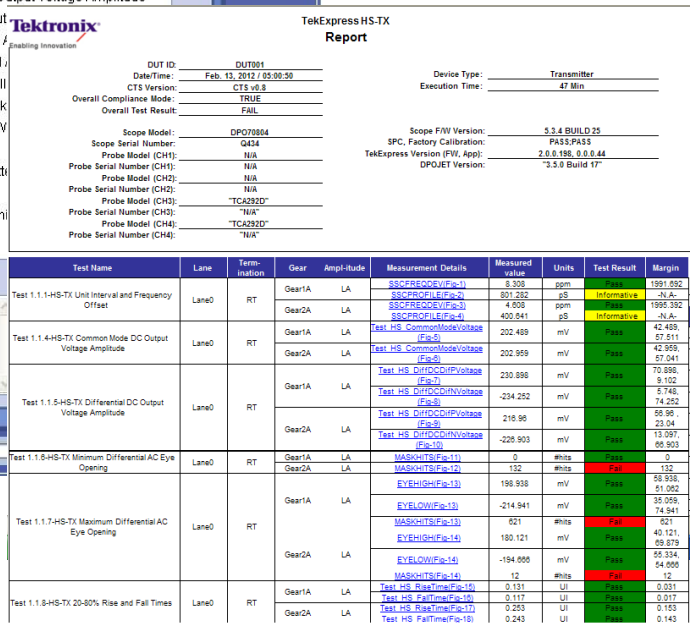
Key Feature	Benefit
Automated Testing	• Reduces the complexity of testing transmitter tests • Reduces testing time, and enables you to test devices faster • Automates apprx 700 tests in regression, in different combinations of Gears, Sub-Gears, Terminations, Amplitudes, etc
Most Complete Tests coverage	• Automates 95% of High Speed, and 75% of PWM tests
Highly Optimized Setup	• Performs Power Spectral Density (PSD) Tests using Oscilloscope-integrated Algorithms Uniquely, • Does not require an External Spectral Analyzer or Extra Hardware to Perform PSD Measurements
Seamless Debug	• Allows Pause on a Test while in Automation, and Switch to DPOJET Analysis Tool for Detailed Debug of failures
Setup Configuration	• Allows Selecting Different Gears and Sub-gears of HS and PWM Signals, Large/Small Amplitudes, Impedance Termination/Un-termination
Test reports	• Provides Single Printable Report, across Different Combinations • Provides Pass/Fail Summary Table, along with Margin Details, Optional Waveform Captures, and Eye Diagrams

M-PHY Tx : New Opt.M-PHYTX Automation Features









Test Name	Lane	Term-ination	Gear	Ampl-itude	Measurement Details	Measured value	Units	Test Result	Margin
Test 1.1.1-HS-TX Unit Interval and Frequency Offset	Lane0	RT	Gear1A	LA	SSCFREQDEV(Fig-1)	8.308	ppm	Pass	1991.692
					SSCPROFILE(Fig-2)	801.282	pS	Informative	-N.A-
			Gear2A	LA	SSCFREQDEV(Fig-3)	4.608	ppm	Pass	1995.392
					SSCPROFILE(Fig-4)	400.641	pS	Informative	-N.A-
Test 1.1.4-HS-TX Common Mode DC Output Voltage Amplitude	Lane0	RT	Gear1A	LA	Test_HS_CommonModeVoltage (Fig-5)	202.489	mV	Pass	42.489, 57.511
			Gear2A	LA	Test_HS_CommonModeVoltage (Fig-6)	202.959	mV	Pass	42.959, 57.041
Test 1.1.5-HS-TX Differential DC Output Voltage Amplitude	Lane0	RT	Gear1A	LA	Test_HS_DiffDCDiffVoltage (Fig-7)	230.898	mV	Pass	70.898, 9.102
					Test_HS_DiffDCDiffVoltage (Fig-8)	-234.252	mV	Pass	5.748, 74.252
			Gear2A	LA	Test_HS_DiffDCDiffVoltage (Fig-9)	216.96	mV	Pass	56.96 , 23.04
					Test_HS_DiffDCDiffVoltage (Fig-10)	-226.903	mV	Pass	13.097, 66.903
Test 1.1.6-HS-TX Minimum Differential AC Eye Opening	Lane0	RT	Gear1A	LA	MASKHITS(Fig-11)	0	#hits	Pass	0
			Gear2A	LA	MASKHITS(Fig-12)	132	#hits	Fail	132
Test 1.1.7-HS-TX Maximum Differential AC Eye Opening	Lane0	RT	Gear1A	LA	EYEHIGH(Fig-13)	196.938	mV	Pass	58.938, 51.062
					EYELOW(Fig-13)	-214.941	mV	Pass	35.059, 74.941
					MASKHITS(Fig-13)	621	#hits	Fail	621
			Gear2A	LA	EYEHIGH(Fig-14)	180.121	mV	Pass	40.121, 69.879
					EYELOW(Fig-14)	-194.666	mV	Pass	55.334, 54.666
					MASKHITS(Fig-14)	12	#hits	Fail	12
Test 1.1.8-HS-TX 20-80% Rise and Fall Times	Lane0	RT	Gear1A	LA	Test_HS_RiseTime(Fig-15)	0.131	UI	Pass	0.031
					Test_HS_FallTime(Fig-16)	0.117	UI	Pass	0.017
			Gear2A	LA	Test_HS_RiseTime(Fig-17)	0.253	UI	Pass	0.153
					Test_HS_FallTime(Fig-18)	0.243	UI	Pass	0.143

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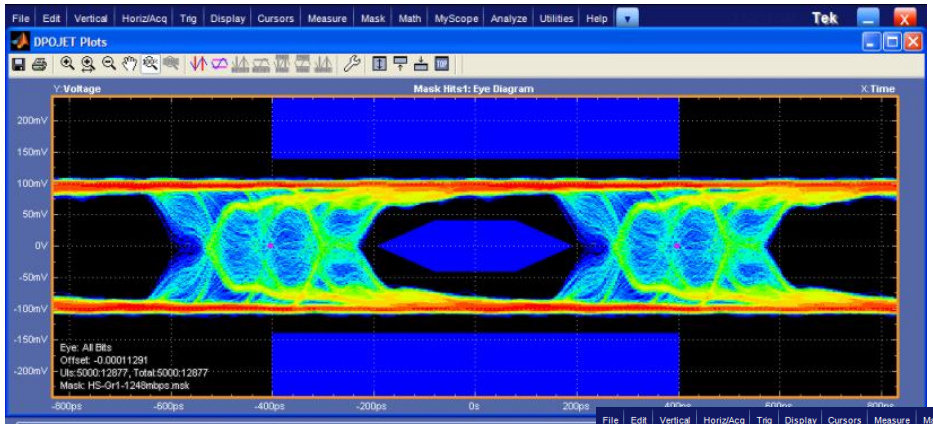
M-PHY Tx: Opt.M-PHYTX/ Opt.M-PHY Testing Solution

Eye Diagram, Power Spectral Density &Common Mode Meas. Examples



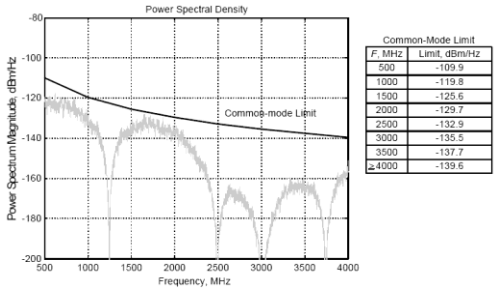


Figure 34 Common-mode Power Spectral Magnitude Limit

Test 1.1.16 – HS-TX Common-Mode Power Spectral Magnitude Limit (PSDCM-TX)

Figure 9: LA Common Mode Output Voltage

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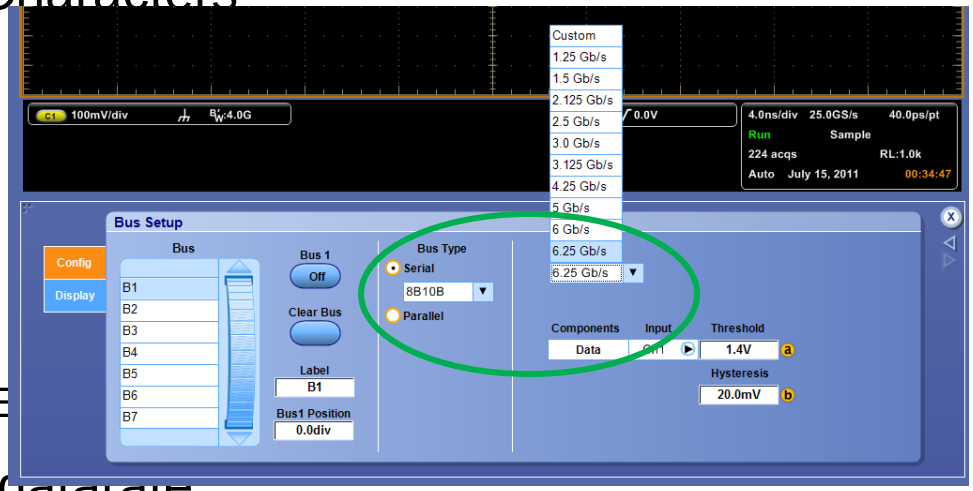
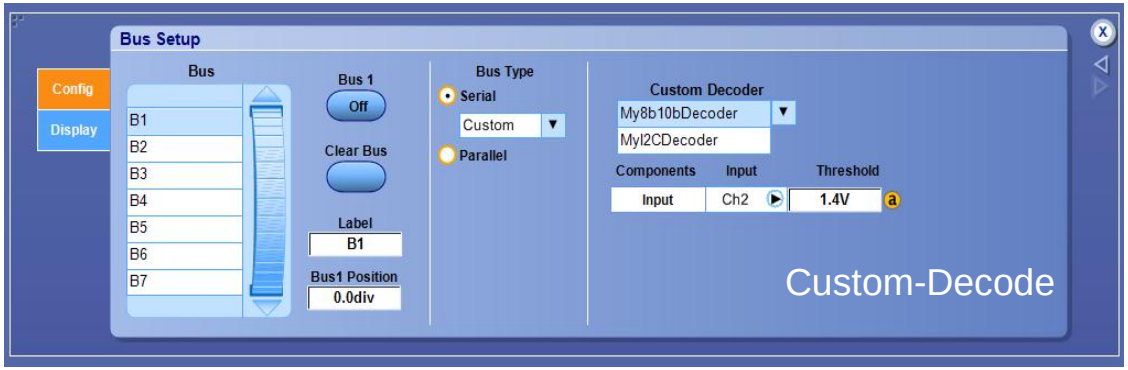
M-PHY Decode: Opt.SR-810B for 8b-10b Decode

- Decode into Symbols or 10-bit Characters
- Decode upto 6.25Gb/s Datarate
- Trigger & Search on
  - Any Control Character
  - Character/ Symbol
  - Pattern
  - Error (Character Error & Disparity E
- Custom-Decode upto 6.25Gb/s datarate
- Supported on all 70KC and MSO70K scopes.
- Software installed as part of TekScope firmware





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M-PHY Decode: Opt.MPHYVIEW for DigRFv4 Decode

- Automated Decoding:
  - Automatically recognizes data speeds, disassembles, and displays the decoded data in different readable-data formats
- 4 Lanes Decoding:
  - Acquires up to 4 lanes of data traffic at a time.
- On-line, Offline and Remote Analysis:
  - Uses TekVisa to connect to a scope.
  - Remote execution through LAN network.
- Filter Tab, Search and Options Tab:
  - Fillter the records in the listing based on user criteria.
  - Searching &highlight records that satisfy given criteria
  - Set display, disassembly, and configuration options.

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M-PHY Decodes: New PGY-UPRO and PGY-LLI

UniPro and LLI Scope-Decodes

- PGY-UPRO and PGY-LLI are Decode Software re-sell from Prodigy Technovations.
  - Provides M-PHY UniPro and M-PHY LLI Protocol Decode and Analysis.
  - Runs on DPO/DSA/MSO70000/B/C/D models (6GHz and above)
  - License mechanism is same as scope options TEK-PGY-HDMI-PA-SW, or PDI-R.
  - Opt. ST6G Serial trigger is optionally required. No other pre-requisites.
- Differentiation
  - SW Leverages ST6G serial trigger features
  - SW is First-to-Market
- Value proposition
  - SW Seamless Integration with all 70K scopes.
  - SW enables system level protocol debugging.
  - 4-Lane Automated Decoding, and Verifies CRC

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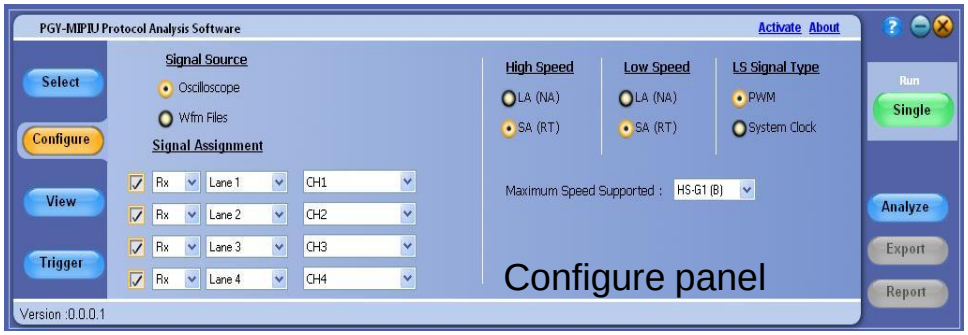
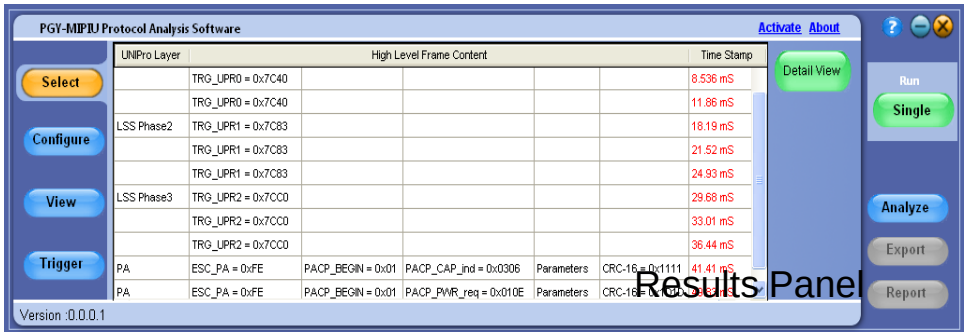
M-PHY Decodes: New PGY-UPRO and PGY-LLI

- Decode Table with Messages &Time stamp
- Overlay of decoded messages on waveform
- Packet content details, with description
- Error packets
- State diagram shows Sequence of messages
  - → ACK frame/NACK frame with time stamp.
- Trigger on UniPRO message contents (Optional)
  - Trigger PA layer message
  - Trigger on Data link layer packet message



Configure panel

Trigger Panel



Results Panel

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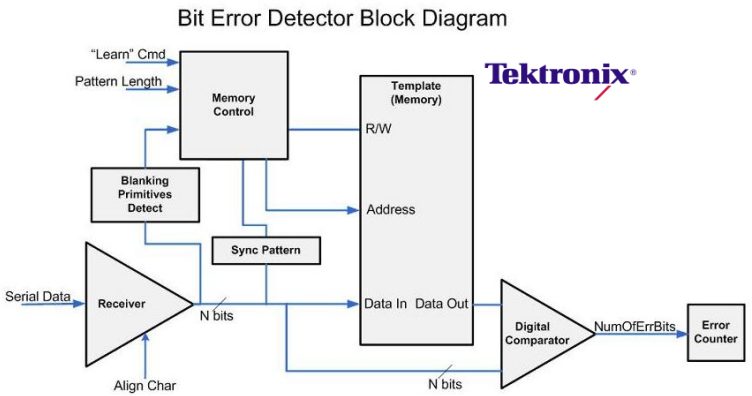
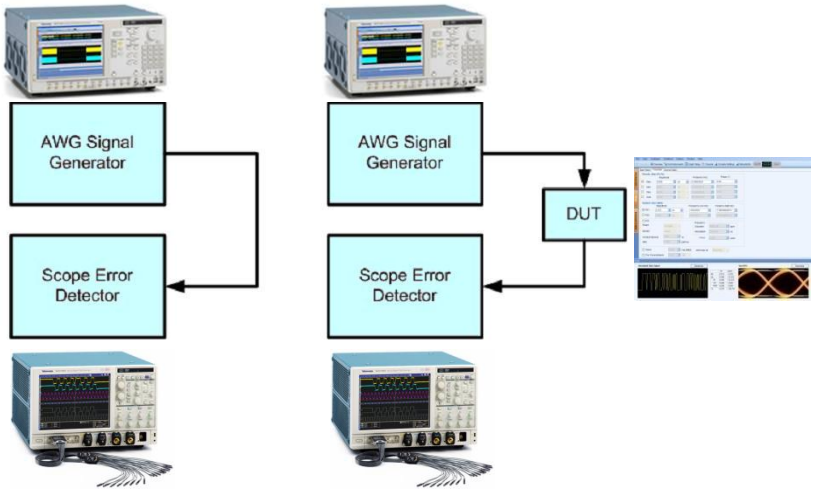
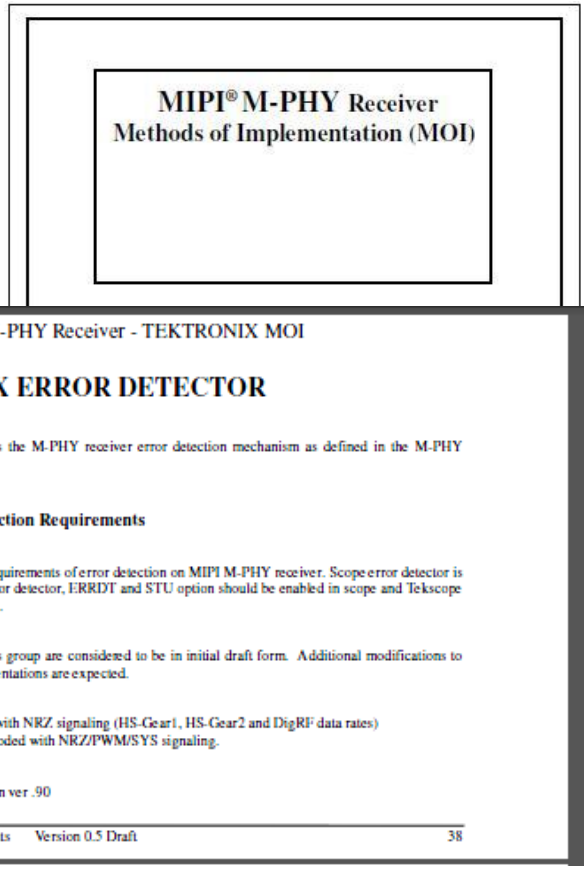
M-PHY Rx : Based on Scope built-in Error Detector

Scope-Integrated M-PHY BER using Opt.ERRDT Shipping Today



- 8B/10B Data:
  - Hardware Serial trigger: 1.25 Gb/s to 6.25 Gb/s
  - BER covers PRBS 312Mbs and above data rates.




MIPI® M-PHY Receiver
Methods of Implementation (MOI)

MIPI M-PHY Receiver - TEKTRONIX MOI

RX ERROR DETECTOR

Overview:
This section of tests verifies the M-PHY receiver error detection mechanism as defined in the M-PHY Specification.

GROUP 1: M-RX Error Detection Requirements

Overview:
This group of tests verifies various requirements of error detection on MIPI M-PHY receiver. Scope error detector is used for this purpose. For M-PHY error detector, ERRDT and STU option should be enabled in scope and Tekscope firmware v6.1.1.32 or later is required.

Status:
The test descriptions contained in this group are considered to be in initial draft form. Additional modifications to both the test descriptions and implementations are expected.

Pay Load:
Continuous PRBS 7/PRBS 9 Pattern with NRZ signaling (HS-Gear1, HS-Gear2 and DigRF data rates)
Custom burst pattern with 8b/10b encoded with NRZ/PWM/SYS signaling.

Note:
Please refer to the MPHY specification ver .90

MIPI M-PHY Rx MOI Measurements Version 0.5 Draft 38

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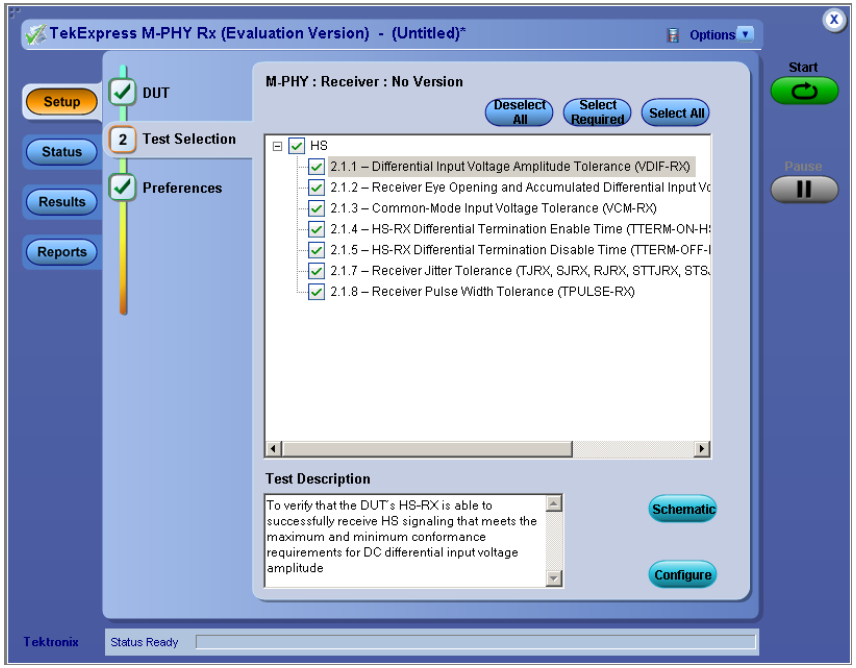
M-PHY Rx : Opt.M-PHYRX Automated Solution

- Opt.M-PHYRX
  - TekExpress (2.0) option for Fully-Automated receiver testing
  - Provides Conformance and Characterization Testing
  - Based on Latest M-PHY Base Spec v1.0 &UNH's Conformance Test Suite
  - Runs on DPO/DSA70KB/C or MSO70K/C scopes
  - TekExpress framework is included.
- Differentiation
  - Simply 2-box setup.
  - Built upon Scope ErrorDetecror ERRDT.
  - Wide HS test coverage



- Value proposition
  - Test Reports with Pass/Fail summary, with Bit-Error counts

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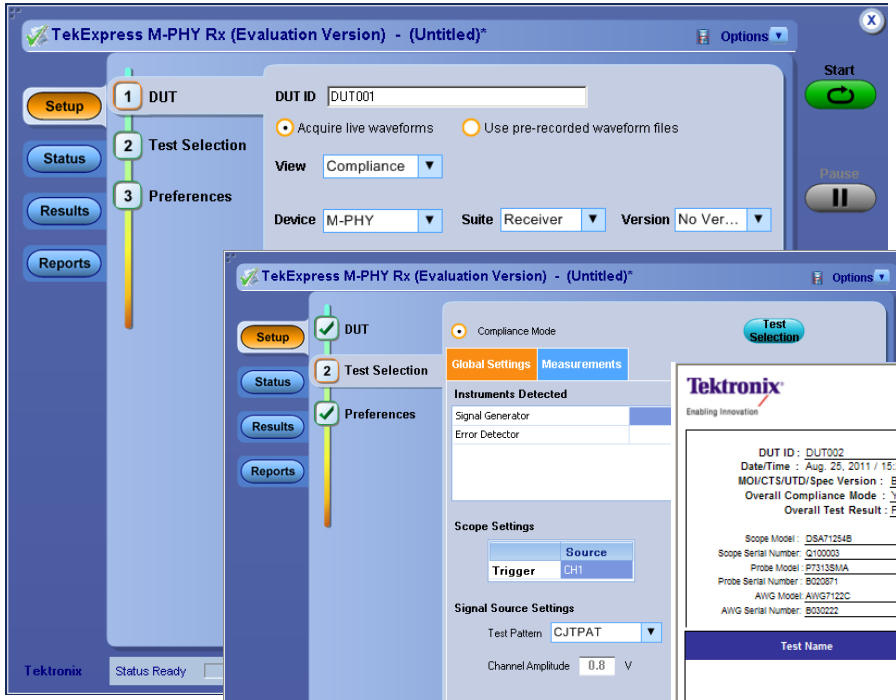
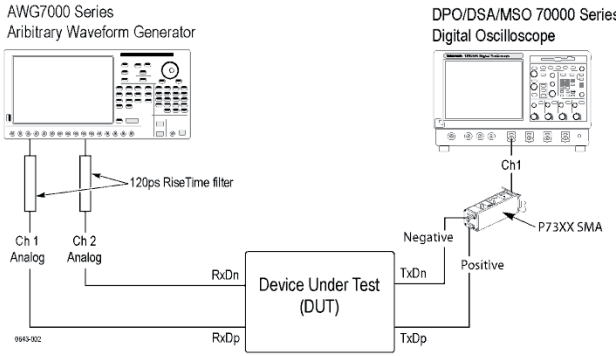
M-PHY Rx : Opt.M-PHYRX Features

Feature	Benefit
Automated Testing	• Reduces the complexity of executing receiver tests • Reduces testing time • Enables you to test devices faster
Tests coverage	• Automated test setup has comprehensive coverage of high speed Rx tests
Simple setup	• Simple Scope+AWG setup for a complete Receiver as well as Transmitter testing of M-PHY. • No other instrument is needed.
Integrated BER	• Leverages Bit-Error-Rate or Error-Count testing using Scope-Integrated ERRDT software in the background. • Scope Integrated ERRDT enables easy and quick setup, saves resource time and costs. • Scope ERRDT testing supports PRBS 312Mbps &above for all Gears. • No external/ extra hardware is required to perform BER testing
Setup Customization	• Modify the test setup as per the DUT configurations such as the high speed Gear, test time or loop-back duration, etc
Test reports	• Provides a Pass/Fail summary for all tests. •-Provides additional information such as test setup hardware and software details, Signal type selected, Bit Error, Execution time and User-comments.

M-PHY Rx : Opt.M-PHYRX Features





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Enabling Innovation

TekExpress MPHY-RX

Receiver Test Report

DUT ID : DUT002
Date/Time : Aug. 25, 2011 / 15:28:26
MOI/CTS/UTD/Spec Version : Base Spec 1.0
Overall Compliance Mode : Yes
Overall Test Result : Fail

Device Type : M-PHY
Execution Time : 31 Min

Scope Model : DSA71254B
Scope Serial Number : Q100003
Probe Model : P7313SMA
Probe Serial Number : B020871
AWG Model: AWG7122C
AWG Serial Number: B030222

Scope F/W Version : 5.3.4 DEVBUILD
SPC, Factory Calibration : PASS:PASS
TekExpress Version: 1.0.0.19
DPOJET Version: NA
AWG Firmware Version: 4.1.1.5

Test Name	Measurement Details	Pattern	Bit Error	Test Result	Limit	Execution Time
2.1.1 – Differential Input Voltage Amplitude Tolerance (VDIF-RX)	Gear 1 A Low Amplitude	CJTPAT	0	Pass	=0	
	Gear 1 A Average Amplitude - Informative	CJTPAT	0	N.A	=0	
	Gear 1 A High Amplitude	CJTPAT	0	Pass	=0	3 Min
2.1.2 – Receiver Eye Opening and Accumulated Differential Input Voltage (TEYE-RX. VDIF-ACC-RX)	Gear 1 A Average Amplitude	CJTPAT	0	Pass	=0	<1 Min
	Gear 1 A Low Amplitude - Differential Low	CJTPAT	0	Pass	=0	
	Gear 1 A Average Amplitude - Differential Low - Informative	CJTPAT	0	N.A	=0	
	Gear 1 A High Amplitude - Differential Low	CJTPAT	0	Pass	=0	
	Gear 1 A Low Amplitude - Differential High	CJTPAT	0	Pass	=0	
	Gear 1 A Average Amplitude - Differential High - Informative	CJTPAT	0	N.A	=0	
2.1.3 – Common-Mode Input Voltage Tolerance (VCM-RX)	Gear 1 A High Amplitude - Differential High	CJTPAT	0	Pass	=0	4 Min
	Gear 1 A Minimum Prepare	CJTPAT	0	Pass	=0	
2.1.4 – HS-RX Differential Termination Enable Time (TTERM-ON-HS-RX)	Gear 1 A Maximum Prepare	CJTPAT	0	Pass	=0	1 Min
	Gear 1 A Minimum Stall	CJTPAT	0	Pass	=0	
2.1.5 – HS-RX Differential Termination Disable Time (TTERM-OFF-HS-RX)	Gear 1 A Maximum Stall	CJTPAT	0	Pass	=0	1 Min
	Gear 1 A LTJ - Frequency 1	CJTPAT	206	Fail	=0	
2.1.7 – Receiver Jitter Tolerance (TJRX, SJRX, RJRX, STTJRX, STSJRX)	Gear 1 A LTJ - Frequency 2	CJTPAT	224507	Fail	=0	
	Gear 1 A LTJ - Frequency 3	CJTPAT	0	Pass	=0	2 Min
2.1.8 – Receiver Pulse Width Tolerance (TPULSE-RX)	Gear 1 A Minimum Pulse Width	CJTPAT	0	Pass	=0	1 Min
	Gear 1 B Low Amplitude	CJTPAT	0	Pass	=0	
2.1.1 – Differential Input Voltage Amplitude Tolerance (VDIF-RX)	Gear 1 B Average Amplitude - Informative	CJTPAT	0	N.A	=0	
	Gear 1 B High Amplitude	CJTPAT	0	Pass	=0	2 Min
2.1.2 – Receiver Eye Opening and Accumulated Differential Input Voltage (TEYE-RX. VDIF-ACC-RX)	Gear 1 B Average Amplitude	CJTPAT	0	Pass	=0	2 Min
	Gear 1 B Low Amplitude - Differential					

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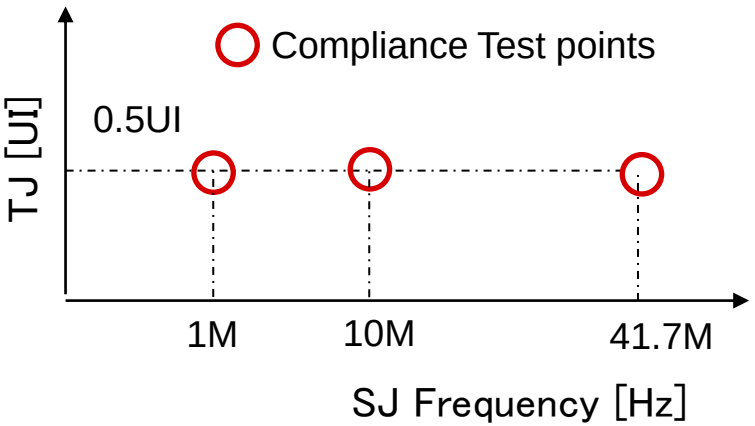
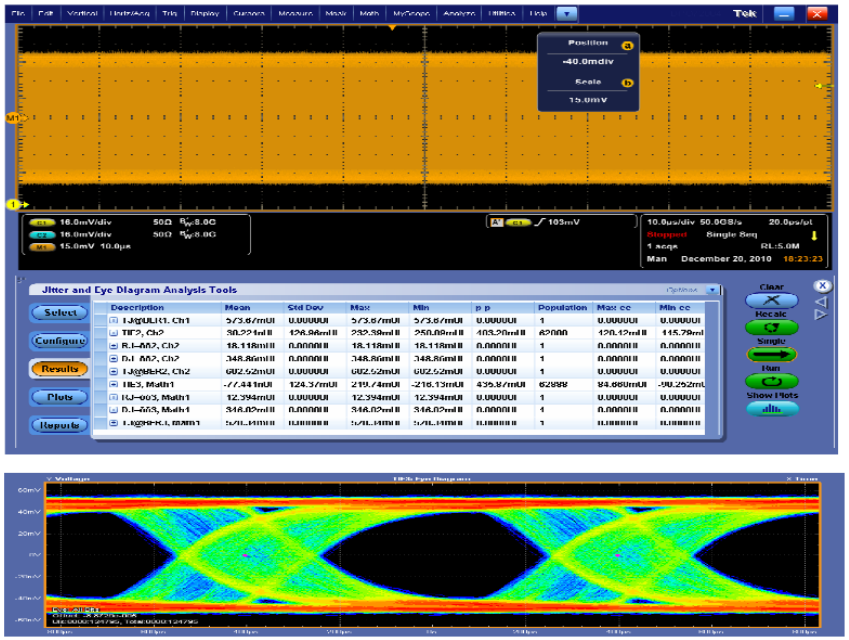
M-PHY Rx Test Setup: Test Impairments using AWG

Manual Setup/ Capabilities

- Supports Flexible signal impairments using Serial Express (optionally) for Characterization.
- Supports Jitter insertion and Pulse Width Modulation (PWM) as per the base specification v1.0.
- Supports testing the DUT in both loopback and non-loopback mode.



1. Long Term Jitter based pattern for PRBS7 continuous Pattern
   - Sinusoidal Jitter Frequency (SJ1) =1 MHz



Example Jitter generation using AWG &Cable impairments, as per the specs.

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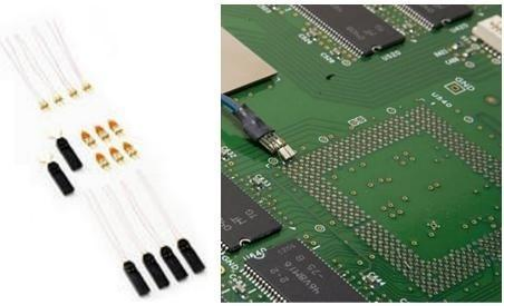
M-PHY Tx &Rx Recommended Test Setup www.tek.com/MIPI

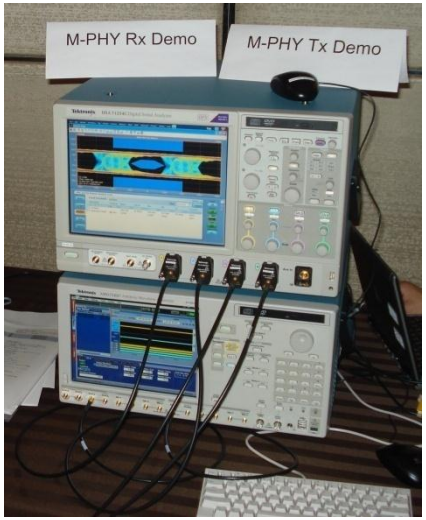
- Scopes
  - DPO70604/B/C or above, for HS-Gear1 Only (Tx &Rx).
  - DPO70804/B/C or above, for HS-Gear1&2 Only (Tx &Rx)
  - DPO71254/B/C or above, for All HS-Gears (Rx Only)
  - DPO72004/B/C or above, for All HS-Gears (Tx &Rx).
- Probes
  - 2x P73xxSMA/P73xx, for Tx HS upto Gears2, or 2x P75xx with P75LRST for Tx HS upto Gear3.
  - 2x P73xxSMA/P73xx, for Tx PWM All Gears.
  - 1x P73xxSMA, for Rx.
- Signal Generators for Rx
  - AWG7082C, AWG7102 or above, for HS-Gear1 Only.
  - AWG7122C without Interleave, for HS-Gear1&2 Only.
  - AWG7122C with Interleave (option 06), for All HS-Gears.
- Software
  - New Opt.M-PHYTX Transmitter Automated Solution (Opt.DJA is pre-requisite).
  - New PGY-UPRO Protocol Decode (Opt.ST6G optionally required).
  - New PGY-LLI Protocol Decode (Opt.ST6G optionally required).
  - Opt.M-PHYRX Receiver Automation (Opt.ERRDT is pre-requisite).
  - Opt.SR-810B, for 8b-10b Decode
  - MPHYVIEW, for DigRFv4 Protocol Decode
  - Optional: Opt.M-PHY Essentials based on DPOJET
  - Optional: SerialXpress for custom-patterns using AWG
- Fixtures
  - As MIPI is chip-to-chip interface, most DUT setups are LIVE with Master-Slave/ Receiver-end connected. For live-setups: No Fixtures required. For non-live setups UNH-IOL Termination boards expected to be available soon



P7380 probe used with a probe-tip

Tektronix M-PHY Testing Solution

- Industry **1st** tools
  - Tektronix announced M-PHY Measurements &Decode tools, in September 2010, during MIPI Alliance Athens F2F.
- Simply **"2-Box"** Solution : Just a Scope + AWG needed for Tx &Rx.
- PSD (Power Spectral Density) measurements on Scope are IP-Patented



Industry 1st M-PHY Tools Demonstrated
at MIPI-Alliance F2F, Athens, Sept'10 and Osaka, March'11

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Press Release Source: Tektronix

Tektronix Introduces Industry's First Test Tools for MIPI M-PHY Debug and Validation

Monday September 27, 9:00 am ET

Support for New High-Speed M-PHY Specification Includes DPOJET toolset, and M-PHY DigRFv4 Decode for Tektronix Oscilloscopes

BEAVERTON, OR--(Marketwire - 09/27/10) - Tektronix, Inc., the world's leading manufacturer of oscilloscopes, today introduced the industry's first testing tools for the MIPI® Alliance M-PHY standard, allowing customers to immediately get started with performance verification and debug for this important new specification using Tektronix DPO/DSA/MSO70000B Series oscilloscopes.

The announcement was made in conjunction with the MIPI Alliance All-Members meeting taking place this week in Athens, Greece. The M-PHY specification is an essential part of the MIPI Alliance's vision for more efficient high-speed interfaces on mobile devices. Compared to the current D-PHY specification, M-PHY supports faster chip-to-chip

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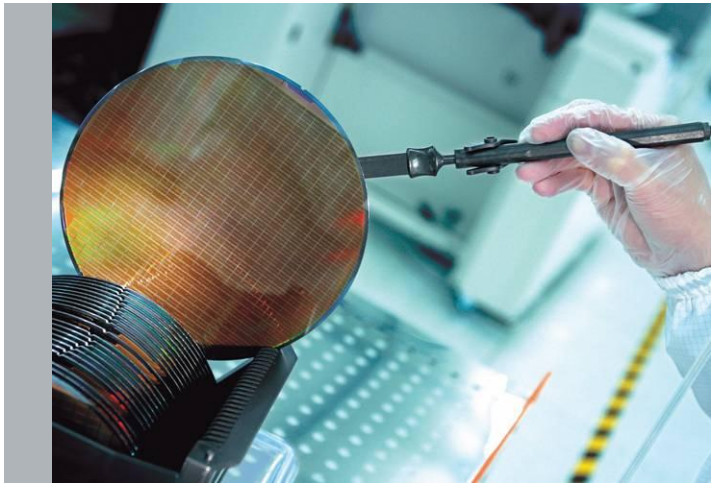
MIPI DSI/CSI2 Protocol solution



Woo,Jun Hyung
Application Engineer

Tektronix®

Agenda

- Introducing MIPI® Protocol Layer
  - What is MIPI DSI ?
  - What is MIPI CSI ?
- MIPI Protocol Validation Solution
- MIPI Stimulus Test using Pattern Generator
- MIPI Protocol decode solution using TLA
- Summary, Q&A

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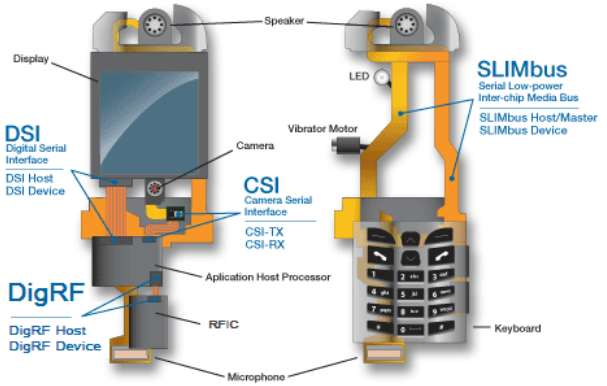
Example Mobile Terminal Block Diagram



Display
DSI
Display Driver IC
DSI
GPS
CMOS Image Senor
CSI
Camera Driver IC
CSI
Baseband IC
Apps Processor
Tx/Rx Processor
DigRF
RF
Air Interface (ex. W-CDMA, WiMax)
SLIMbus
Loudspeaker
Ear Piece
FM Radio
Microphone
Audio Driver IC
SLIMbus
Memory Interfaces (ex. Mobile DDR, Mobile SDRAM, Flash, etc)
Memory (Internal)
Memory (SD Card)

Definitions
CSI = Camera Serial Interface
DSI = Display Serial Interface
SLIMbus = Serial Low-power Inter-chip Media Bus

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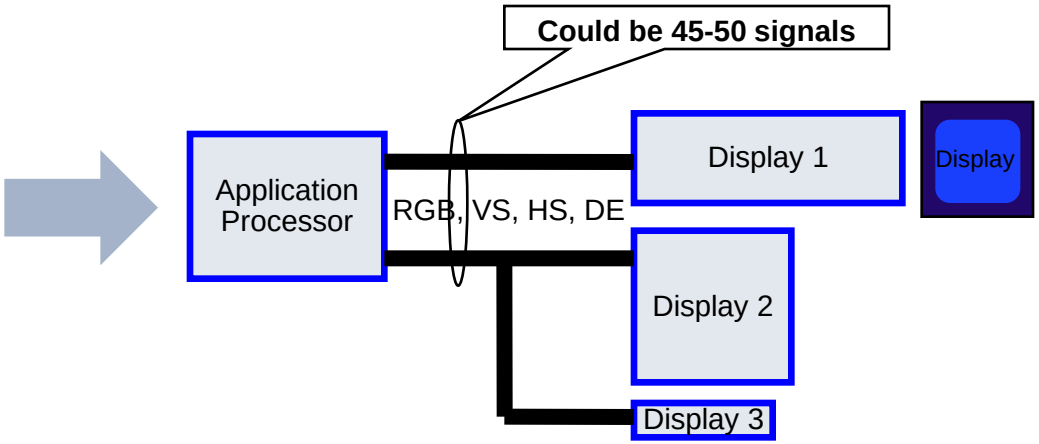
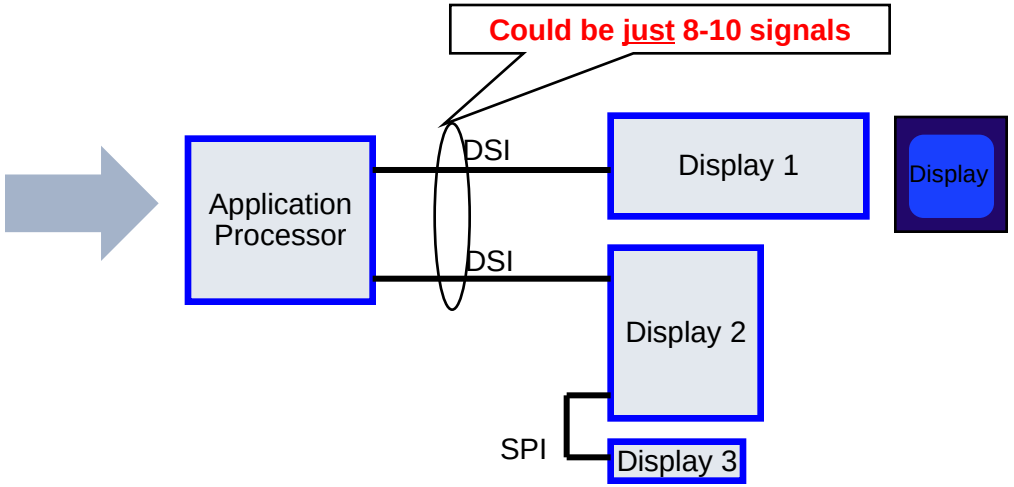
What is MIPI DSI ?

DSI is the specification for processor-to-display interconnect in handheld platforms

- The Legacy Standards in a Mobile Device
  - Exposed wide standards
    - RGB, VS, HS or DE
  - All are parallel busses
    - Each 45-50 signals



- **MIPI DSI-1**
  - Only Single standard: DSI-1
  - Multiple Displays – One Interface
  - Supports all Common Display technologies
  - A Serial bus
    - Just 8-10 signals
      - 5:1 ratio savings in signals
    - Lower EMI
  - **Physical layer is D-PHY**
  - **Protocol layer is DSI-1**



- **MIPI DSI-2**
  - Higher Data rate
    - Backward Compatible to DSI
  - **Physical layer is M-PHY**
  - **Protocol layer is DSI-2**

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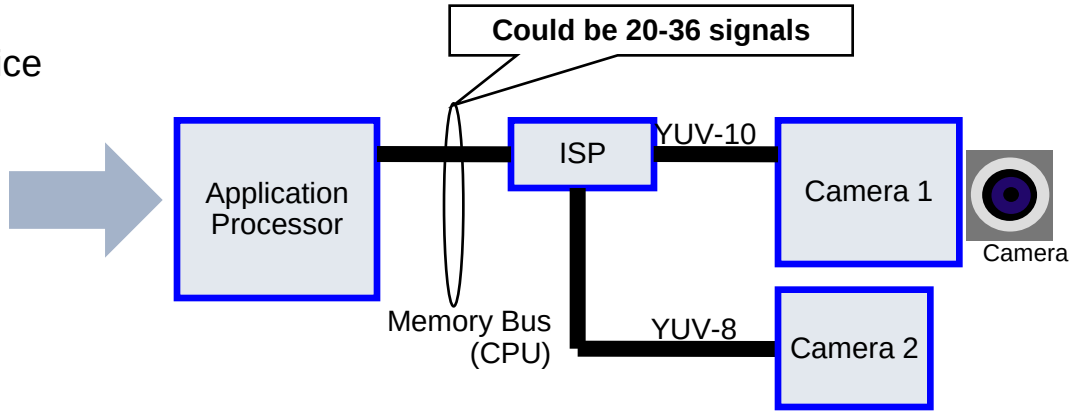
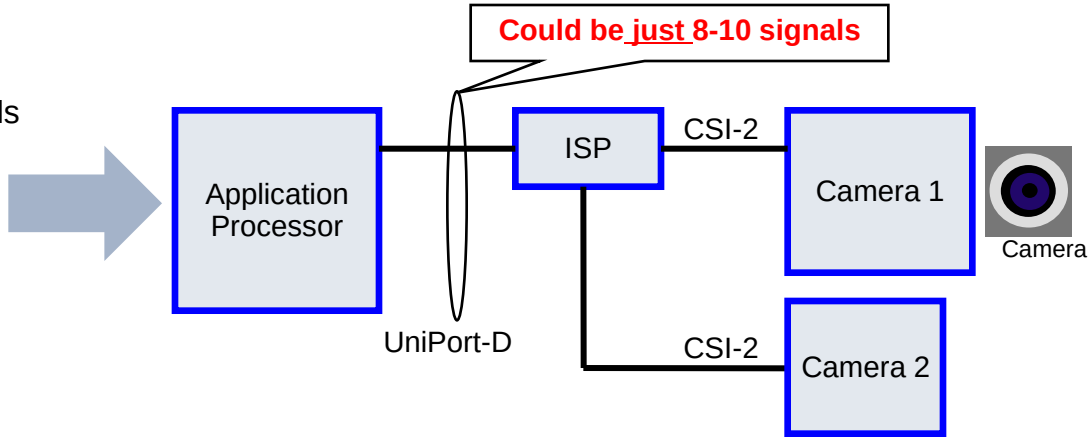
What is MIPI CSI ?

CSI is the serial interface specification
for Camera/ imaging peripherals and host processors

- The Legacy Standards in a Mobile Device
  - Exposed wide standards
    - YUV-10, YUV-8, etc
  - All are parallel busses
    - Each 20-36 signals



- **MIPI CSI-2**
  - Only Single standard
    - Multiple Cameras – One Interface
    - Physical layer is D-Phy
  - A Serial bus
    - Just 8-10 signals
      - 3:1 ratio savings in signals
    - Lower EMI
  - **Physical layer is D-PHY**
  - **Protocol layer is CSI-2**



- **MIPI CSI-3**
  - Higher Data rate
  - Backward Compatible to CSI-2
  - **Physical layer is M-PHY**
  - **Protocol layer is CSI-3**

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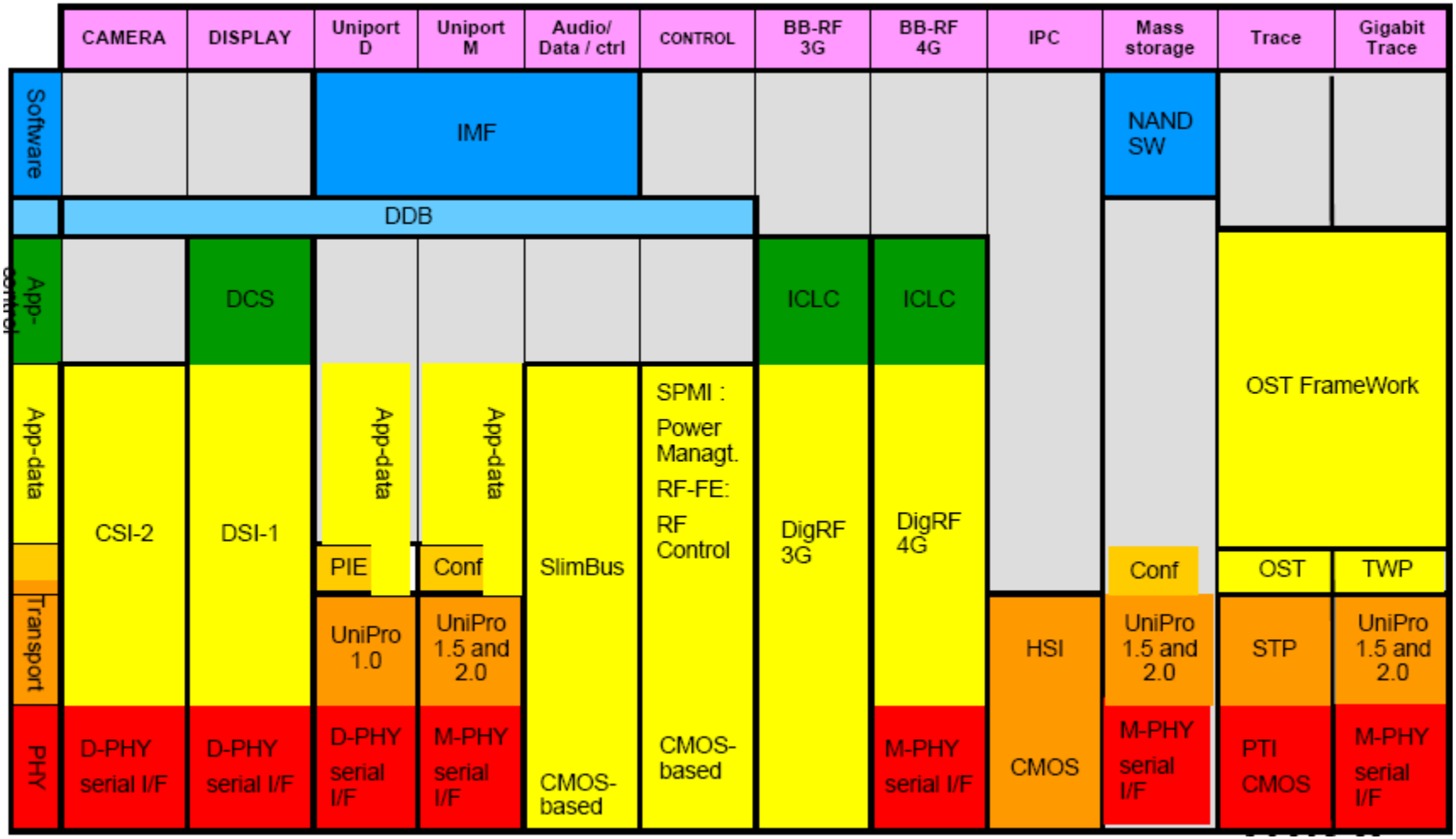
MIPI Protocol Stacks

(source: mipi.org)



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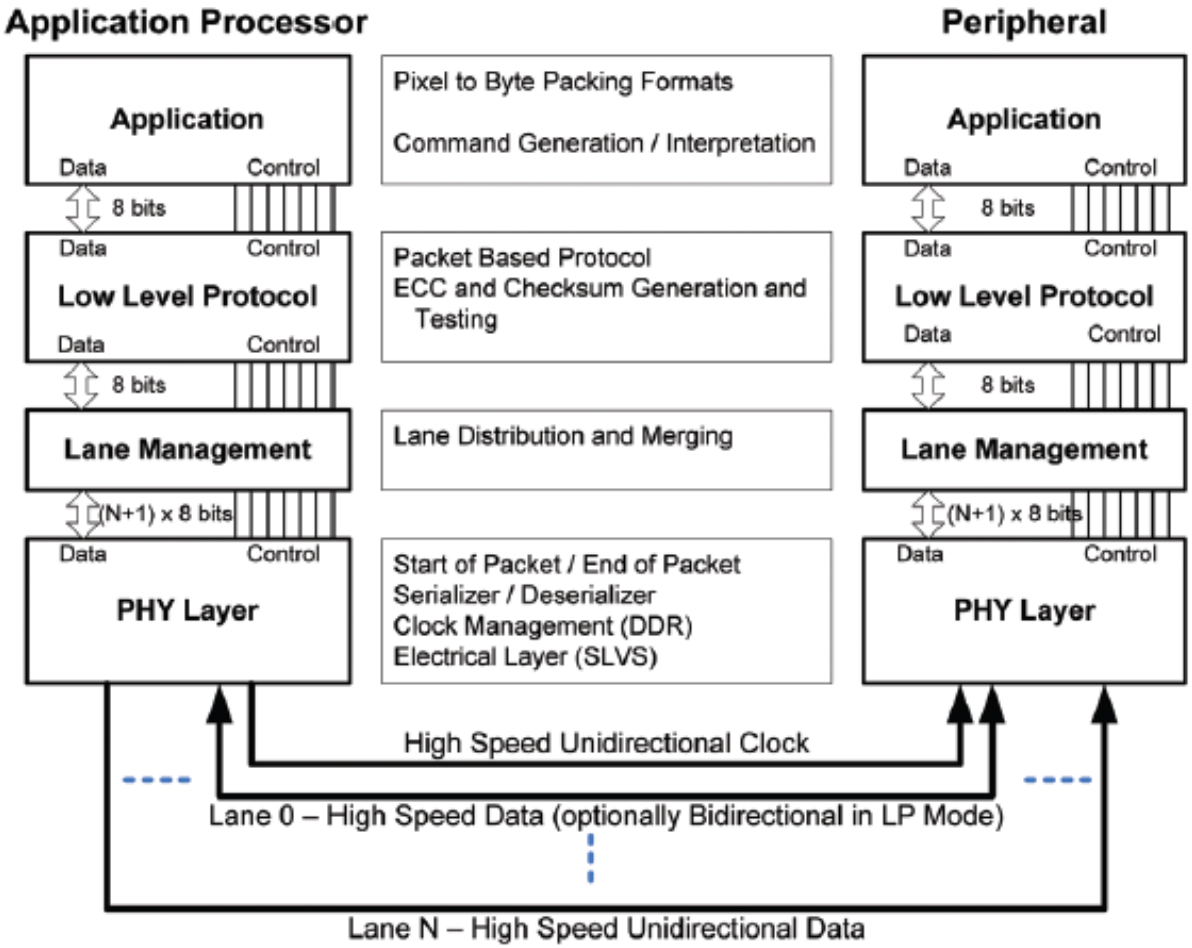
MIPI DSI Layered Architecture



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MIPI D-PHY

Test Solutions

Analog

Protocol

Stimulus

Component Level Testing
System Level Debug
HW/SW Integration
Characterization
Compliance

Tools to cover all your test needs for today and in future

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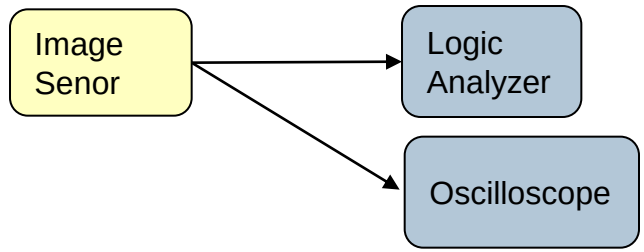
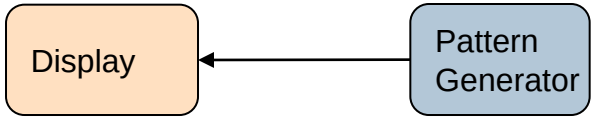
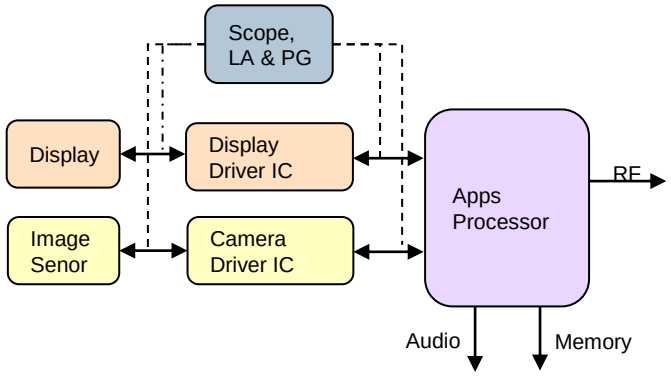
MIPI Solutions and Techniques

- Oscilloscope
  - Signal Integrity
  - D-PHY Physical Layer Test
- Logic Analyzer
  - Validation and debug of the MIPI protocol
- Pattern Generator
  - MIPI Signal Generation
  - Stimulating Driver ICs, Devices, and Processors
- Oscilloscope, Logic Analyzer and Pattern Generator
  - System level Validation & Debug
  - Testing fully integrated mobile handset platforms







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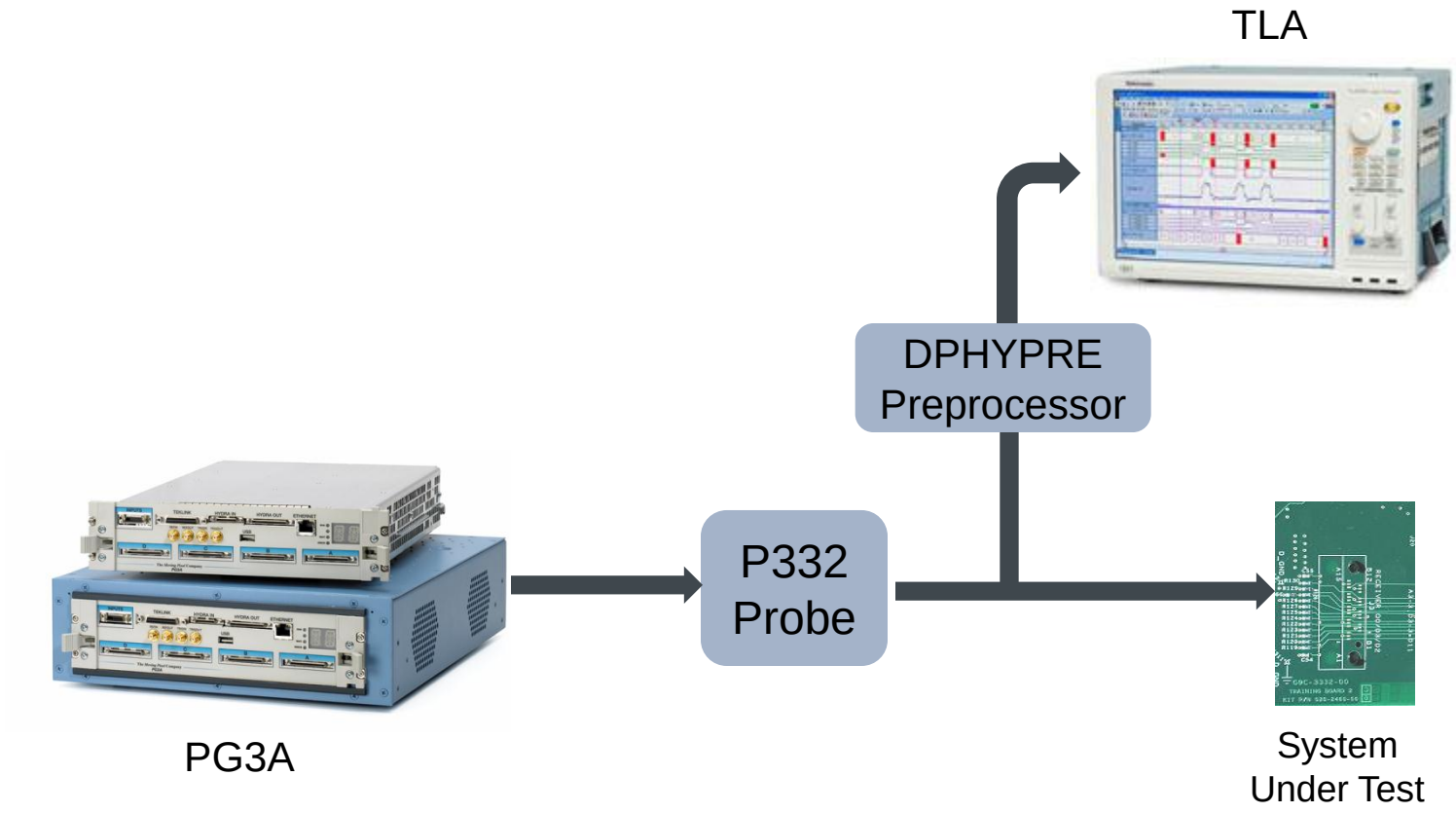
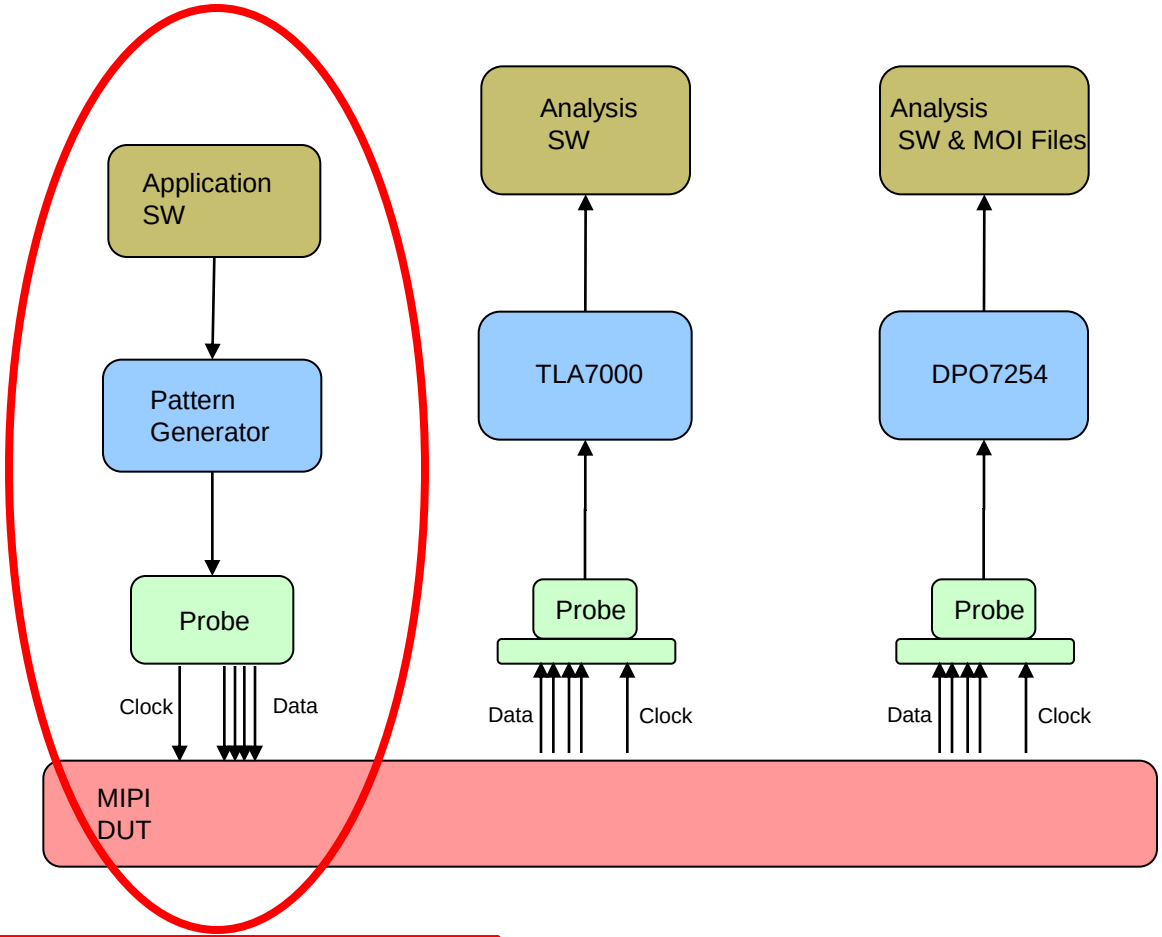
Typical Protocol Validation Test Setup



Stimulus

Test Environment



Signal Generation

Using Pattern Generator

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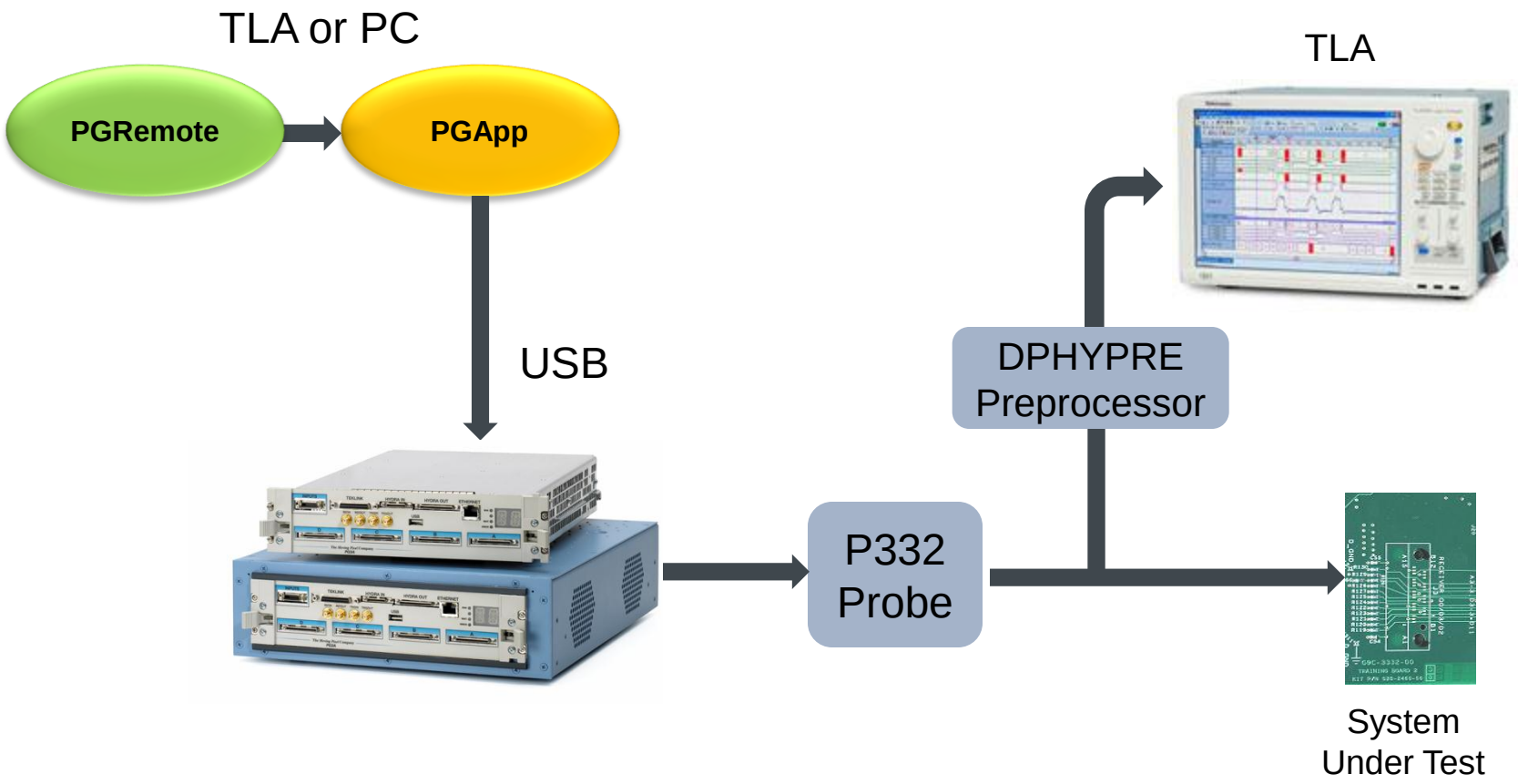
Stimulus Setup



Stimulus

- **Protocol Testing** – Stimulating buses with known good data packets or packets with intentional errors tests the system's adherence to a specified protocol
- **Infrequent Events** - System bugs that only appear when infrequent events occur can be quickly reproduced with a pattern generator by repeatedly stimulating the system with the key external event
- **Automated Test** – Production line test setups can utilize the PG3A as a general purpose digital I/O source with a large number of channels

Digital Pattern Generators

	PG3AMOD	PG3ACAB	PG3L
			
Max clock rate	300MHz		
# of Channels	64		32
Memory	32M Vectors		
Data models	Flat or block based		
Output levels	External Probes determine voltage		
Form factor	Plug-in module for TLA7K	External cabinet for stand-alone use or with the TLA	
PGApp (Win XP, WIN7)	Convenient pattern entry with multiple pattern fills, import and export		
Ref In/Out, Ext Trig In/Out	Yes	Yes	No
External events	9	9	8
Width Expandable	To 256 bits	To 256 bits	No
P300 Inputs Probe	Yes	Yes	No
Probe Cables	4	4	1
Delay Line Range on a Group of 8 Bits	500ns	500ns	7.5ns

MIPI Applications are not supported on PG3L

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P332 MIPI D-PHY Probe for PG3A

Key Features

- MIPI D-PHY Probe for use with PG3AMOD and PG3ACAB
- Generate CSI2 and DSI data over D-PHY
- 4-Data Lanes and 1-Clock lane
- 1.5Gbps / Lane data rate
- SMA outputs for each lane
- LP and HS Voltage and Timing adjustable on a each lane separately

PG3A

P332

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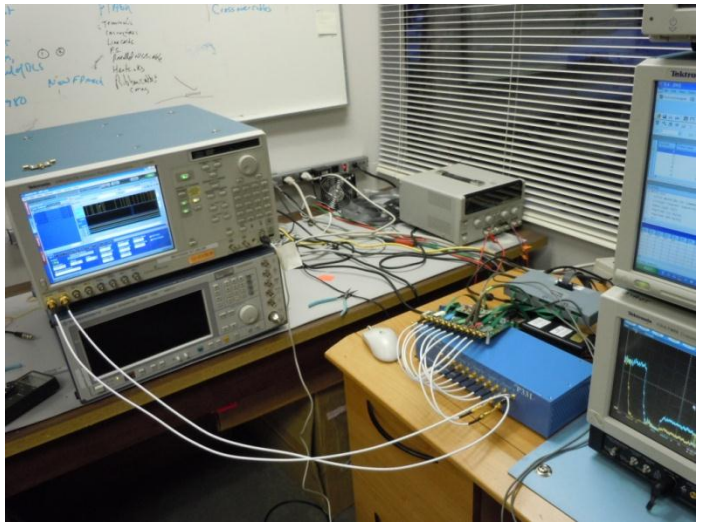
P332 MIPI D-PHY Probe

Key Features

- Optional external clock input port suitable for impaired clock testing (e.g. jitter, noise, etc)
- Ability to insert simple commands into vertical blanking while in continuous video mode
- Proper BTA response handshaking when DUT returns control back to PG
- LP contention detection



Noise injection setup for D-PHY Rx Testing

Preserve your investment with the ONLY 4 lane, 1.5Gbps stimulus solution in the market.

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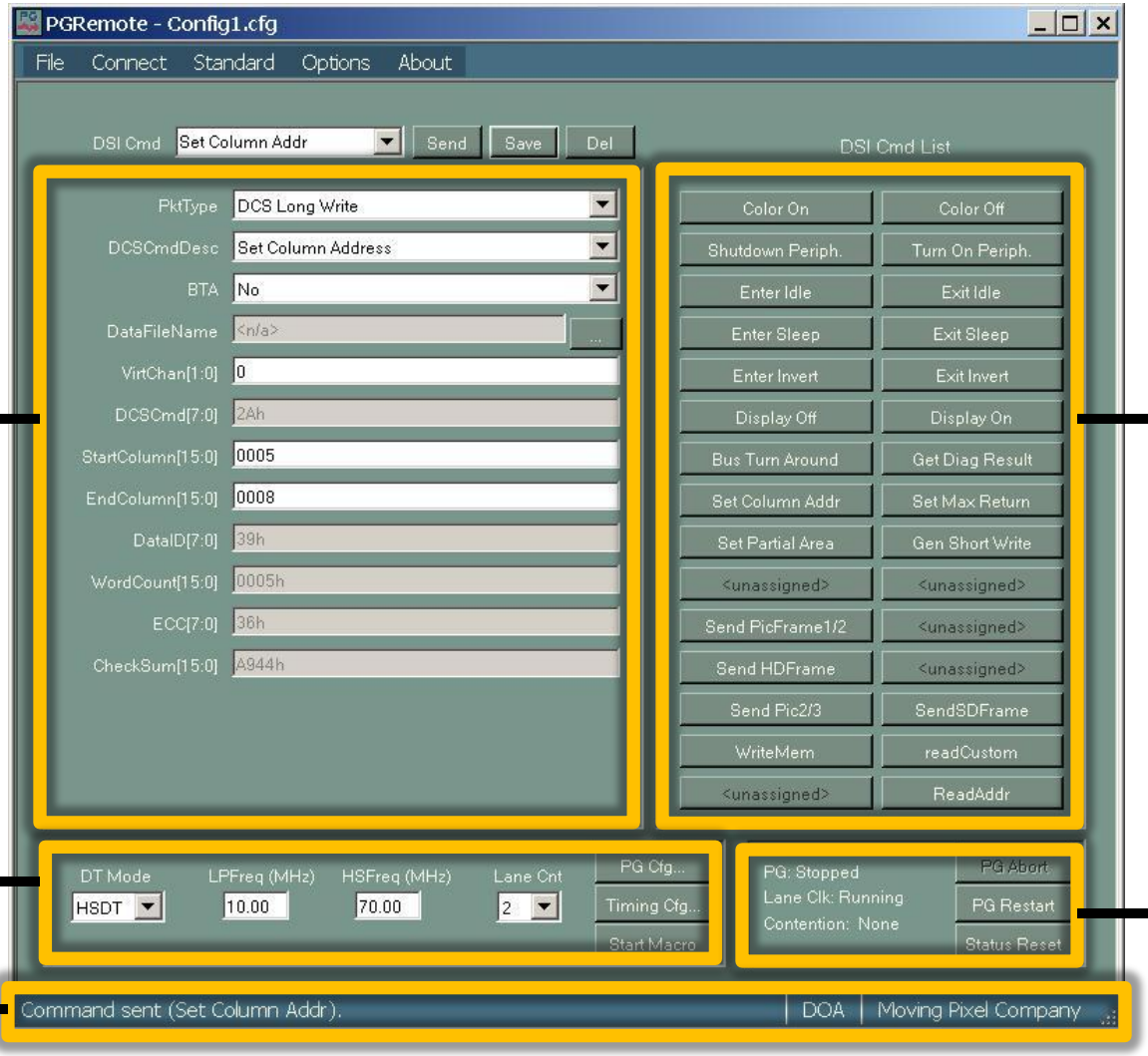
PGRemote

Push Button Interface to generate CSI2 / DSI Vectors



Define CSI/DSI commands and arguments

Configuration Parameters for PG playback, and D-PHY

Status Bar

Command Buttons

PG, probe status and operational controls

PGRemote Main Window

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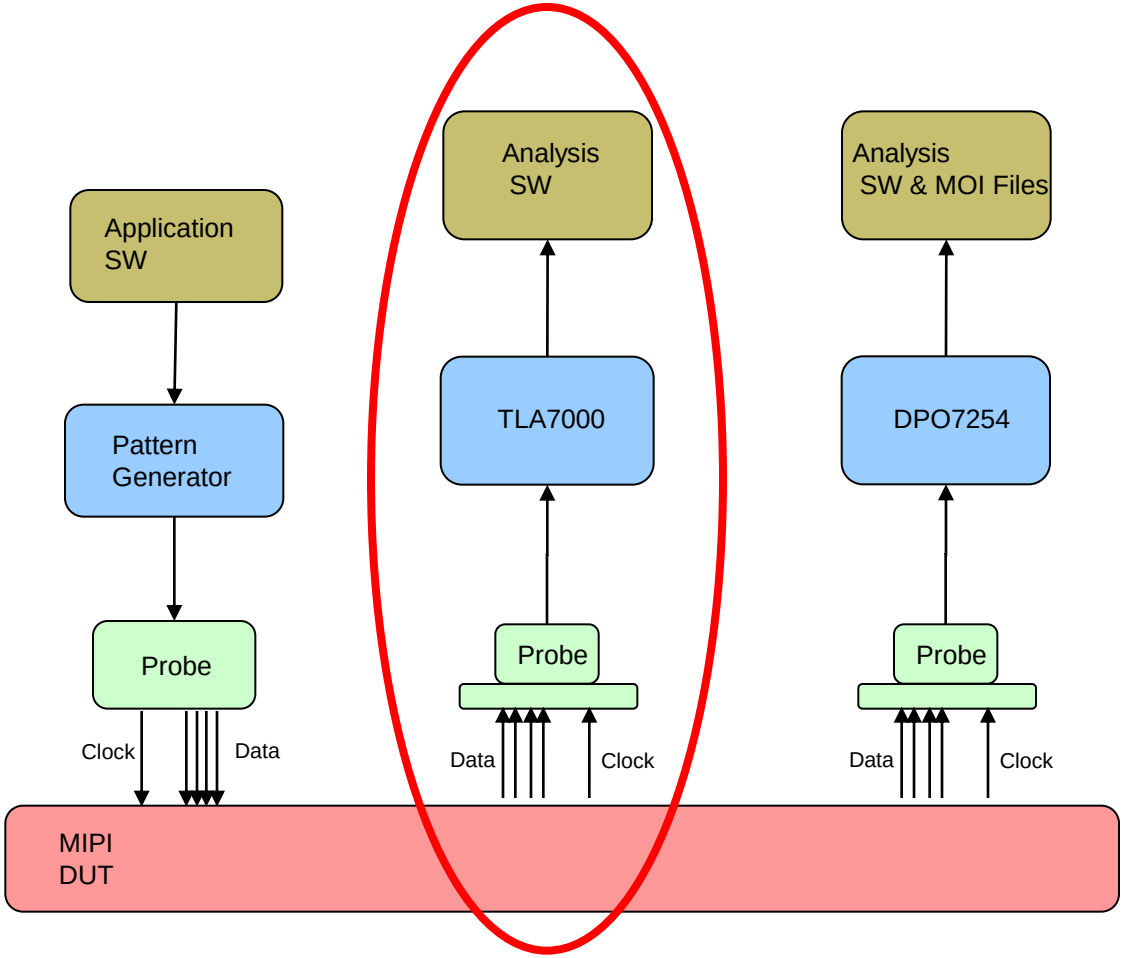
PGRemote

- Push Button User interface to generate CSI2 or DSI vectors and probe control
- Adjust frequency, voltage and delay in HS and LP modes
- Adjust D-PHY state timing parameters
- Adjust frame timing and generate looping video
- Enter and exit Low power states
- Create custom commands, Macros and assign them to buttons
- Save restore a configuration
- Ability to use P332 as a generic high-speed serial probe
- The PG can be operated in several modes
  - Pushbutton Mode using the PGRemote software
  - Macro Mode using the PGRemote software
  - Scripting
  - Full remote control mode

Protocol Validation

Test Environment



Signal Acquisition
- Using Logic Analyzer

CSI2/DSI Protocol validation

Solution Overview

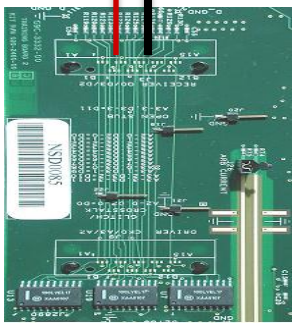
P6982 or
P6980 Probe

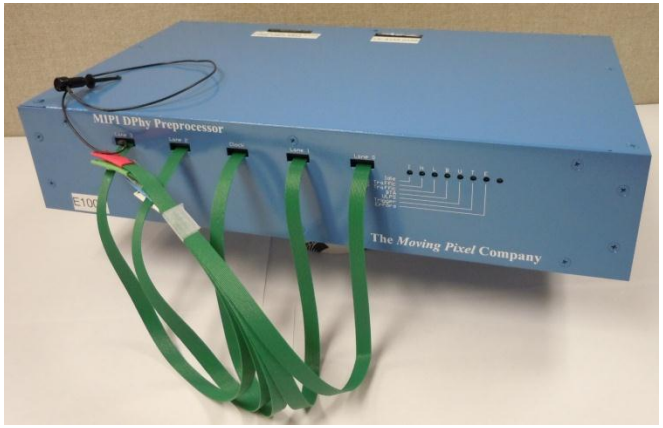
D-PHY
Preprocessor

USB Cable
For Control

Clk

Data
(up to 4 Lanes)





D-PHY Preprocessor

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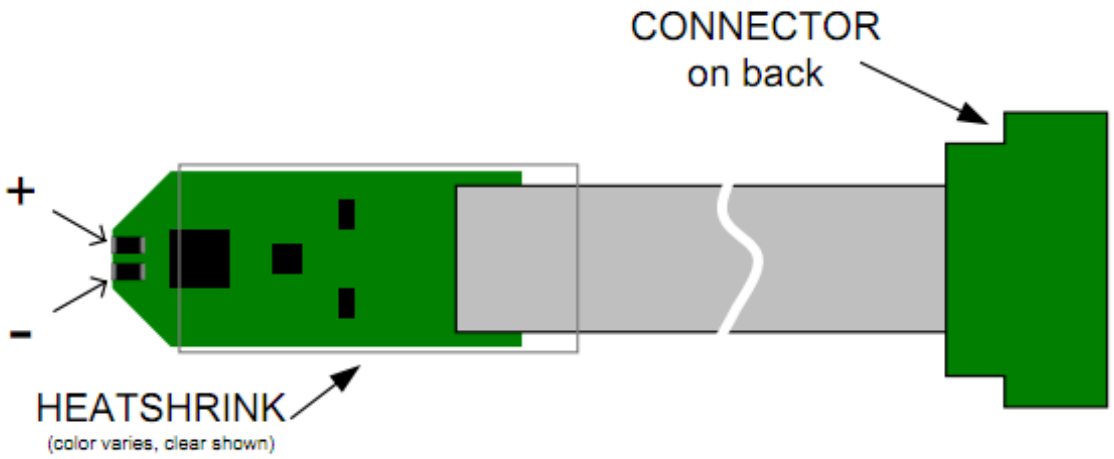
Probing

- D-PhyPreprocessor has Solder-Down Probes
- Each Data Lane and the Clock Lane has a separate probe
- Probes are color coded for easy identification
- Can support Data Rates of up to 1.5Gb/s on each lane



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D-PHY Preprocessor

- Support 1.5Gbps per lane
- Support for up to 4 Lanes of D-PHY data
- Color coded solder down probes for easy identification
- Support CSI2/DSI Protocols
- Advanced Packet Level Triggering
- Real Time Filtering
- Lane activity and Error Status
- Simultaneous Low Power and High Speed Data Acquisition
- 8x improvement in TLA Memory usage
- Image Export
- Compatible with both TLA6k and TLA7k

Preserve your investment with the ONLY 4 lane,
1.5Gbps protocol solution in the market.

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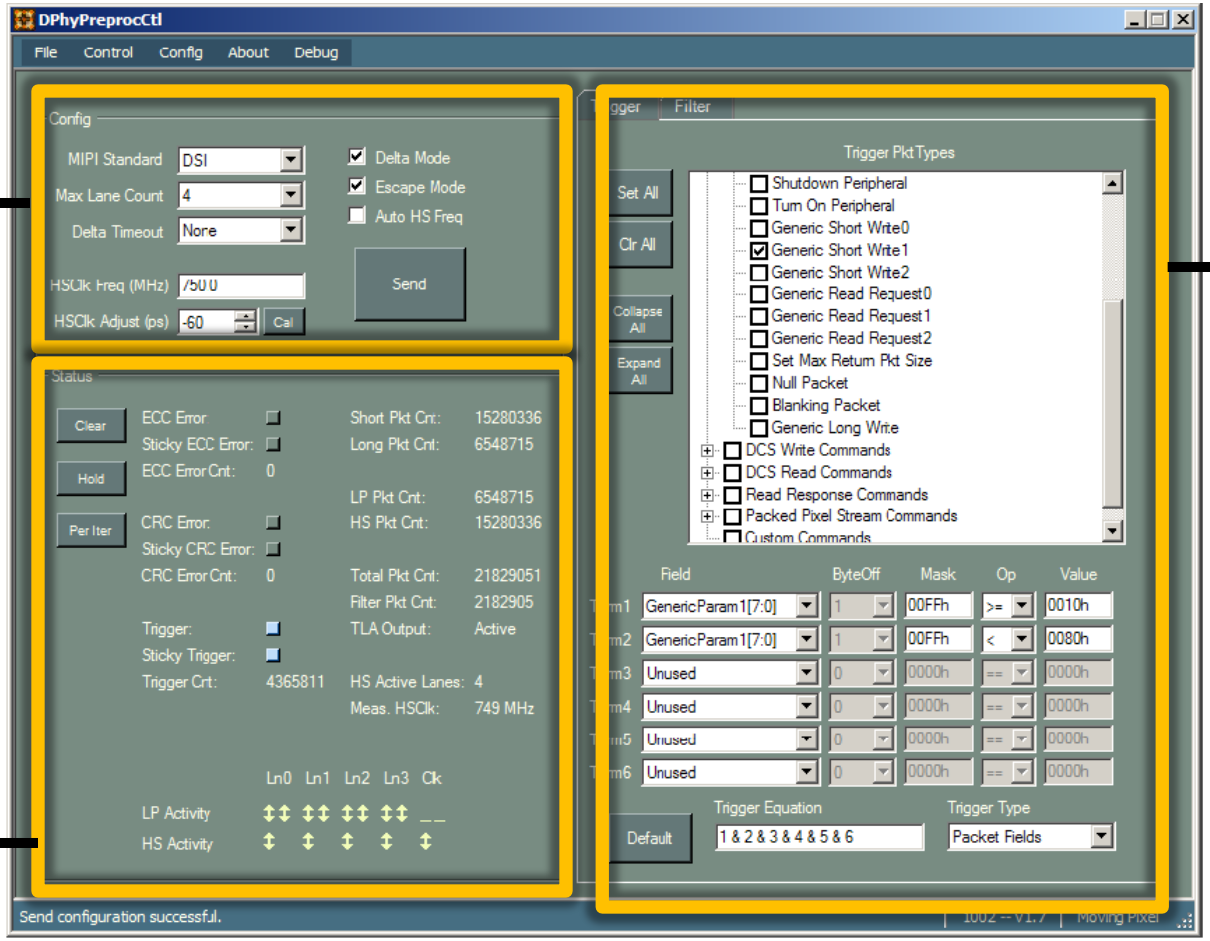
D-PHY Preprocessor control UI

Preprocessor Configuration



Trigger & Filter Definitions

Status Area
- Lane Activity
- Trigger Status
- Error Status

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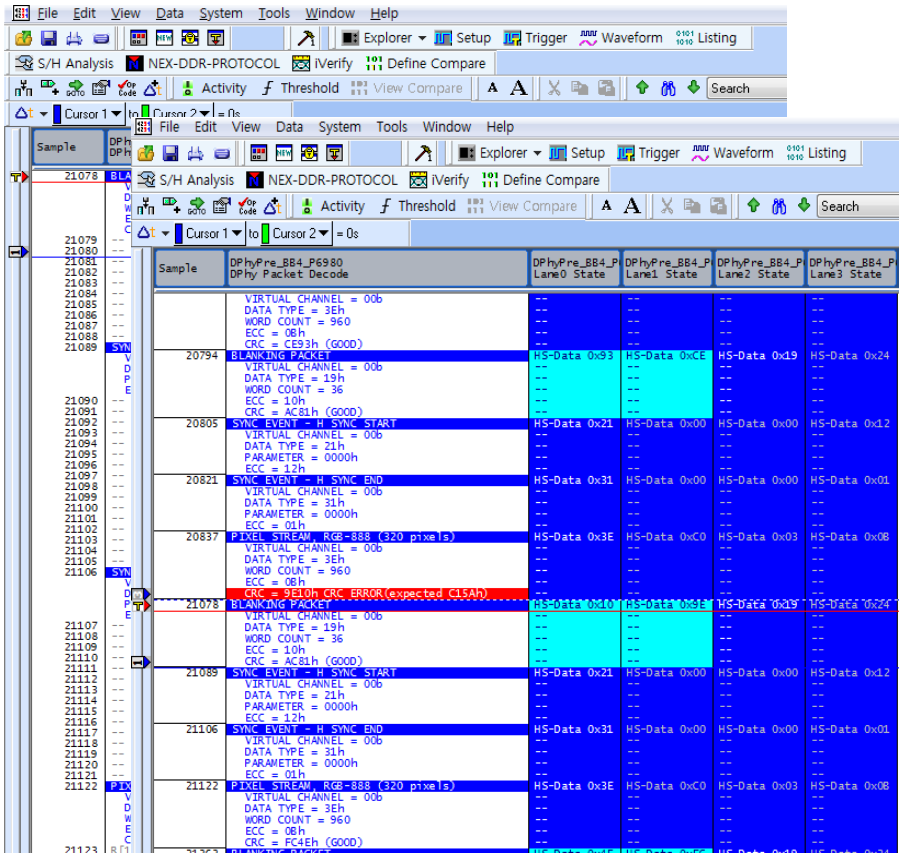
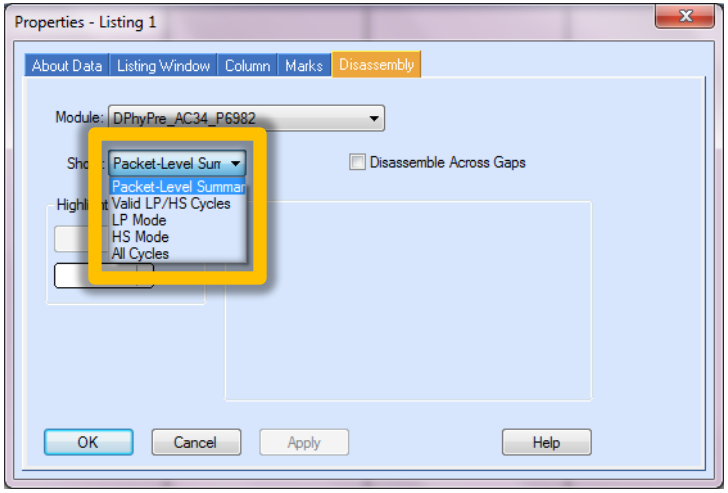
D-PHY Decode

- Supports from 1 to 4 lanes of D-PHY data
- Decode and Display
  - All LP and HS state transitions
  - LP commands and data
  - LP and HS Data in Byte Format
  - All types of Short and Long packets
  - DCS Command decode
- Supports different RGB and YUV Schemes
- Supports ECC and Checksum verification.
- selectively view the decoded information at different levels of hierarchy





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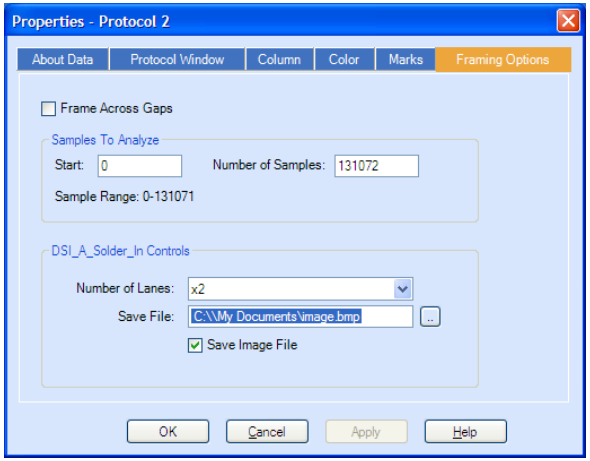
Protocol Support

- Packets extracted & stored for further analysis
- Image rendering
  - Rendering with Partial Data supported
- Different RGB export options



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Data Formats supported

CSI Formats

- YUV420 8-bit (legacy)
- YUV420 8-Bit
- YUV420 10-bit
- YUV422 8-bit
- YUV422 10-Bit
- RGB888
- RGB666
- RGB565
- RGB555
- RGB444

DSI Formats

- RGB888
- RGB666 Packed
- RGB666 Loosely Packed
- RGB 565

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System Configuration

Protocol Decode

- Option - 1
  - DPHYPRE (1ea)
  - P6982 (2ea)
  - TLA6K or TLA7ACx (1ea)
  - TLA7012/TLA7016 (1ea)
    - For use with TLA7ACx
- Option - 2
  - DPHYPRE (1ea)
  - P6980 (1ea)
  - TLA7BBx (1ea)
  - TLA7012/TLA7016 (1ea)
    - For use with TLA7BBx

Stimulus

- Option - 1
  - PG3AMOD (1ea)
  - P332 (1ea)
  - PGRemoteSW (1ea)
  - TLA7012/TLA7016 (1ea)
    - For use with PG3AMOD
- Option - 2
  - PG3ACAB (1ea)
  - P332 (1ea)
  - PGRemoteSW (1ea)

Summary

- Stimulus
  - Only 4 Lane stimulus solution that can support 1.5Gbps Data rate / lane.
  - Provides the flexibility to control link level timing parameters as well as PHY level timing and voltage parameters
  - Supports both the DSI and CSI2 protocols
- Protocol
  - Only 4 Lane Protocol validation solution that can support 1.5Gbps Data Rate / Lane
  - Provides sophisticated Packet level Triggering, real time filtering, Status Monitoring and LED indicators
  - Supports both the DSI and CSI2 protocols


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