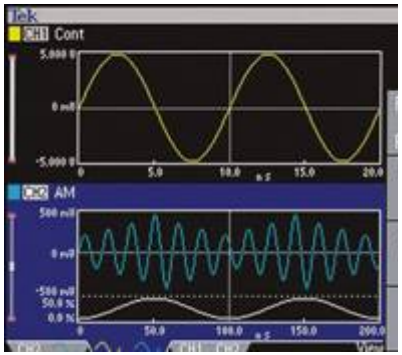
Receiver Testing Methodologies



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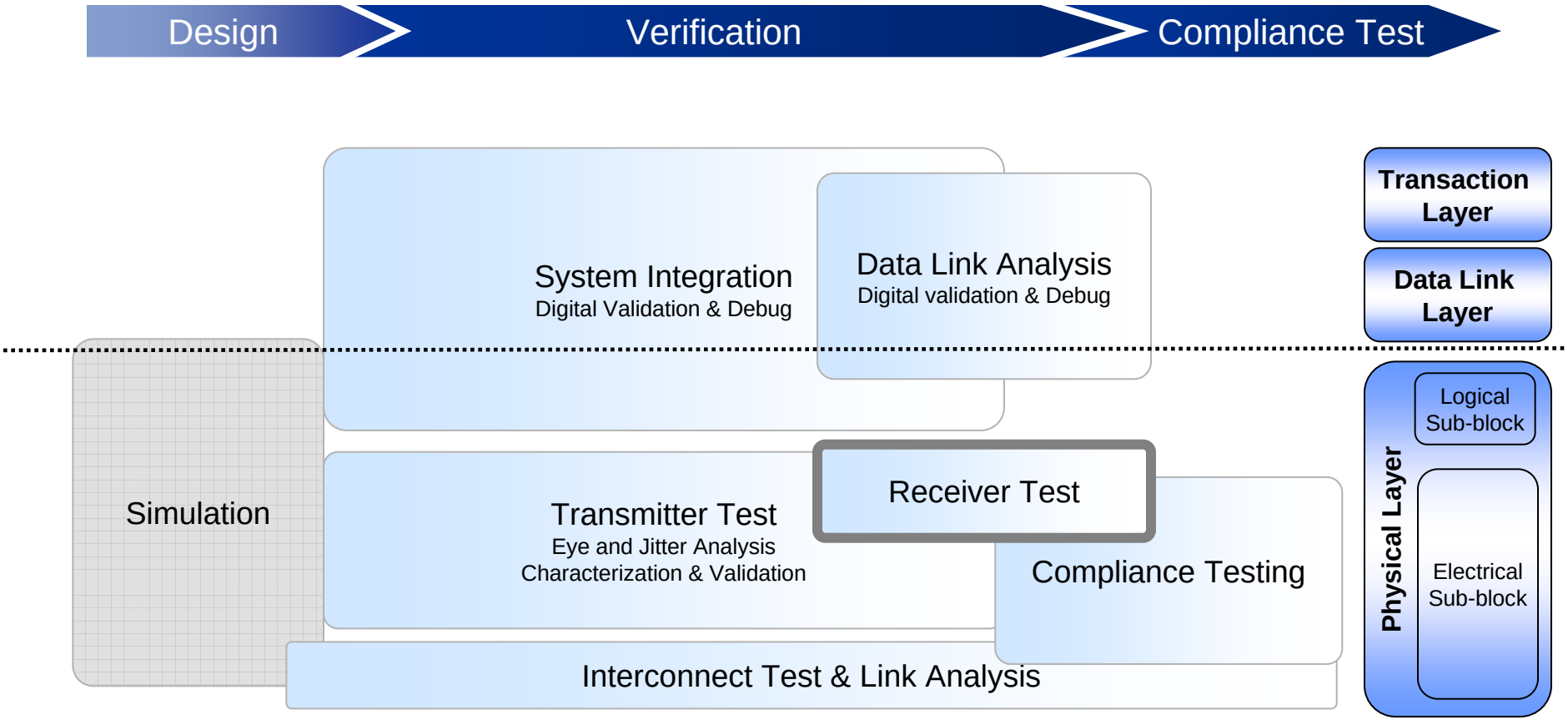
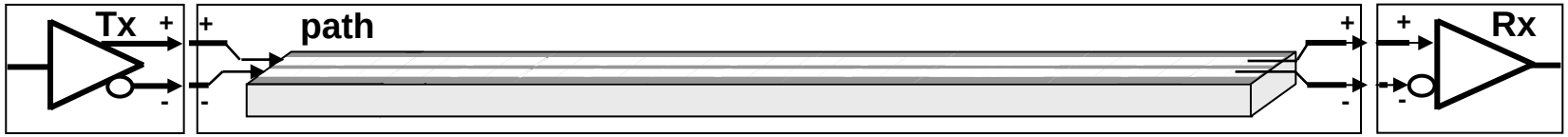
Agenda

- High Speed Serial Test Challenges
  - Overview
  - Error Rate as an indicator of performance
  - Focus on Receiver Testing
  - Loopback
- Receiver Tolerance Testing
  - Stress Pattern Library
  - Pattern Generation and Calibration
  - Frame Error Rate Detection
- Compliance Testing
  - MOIs, CTS
  - Toolset
- Summary

High Speed Serial Test Challenges





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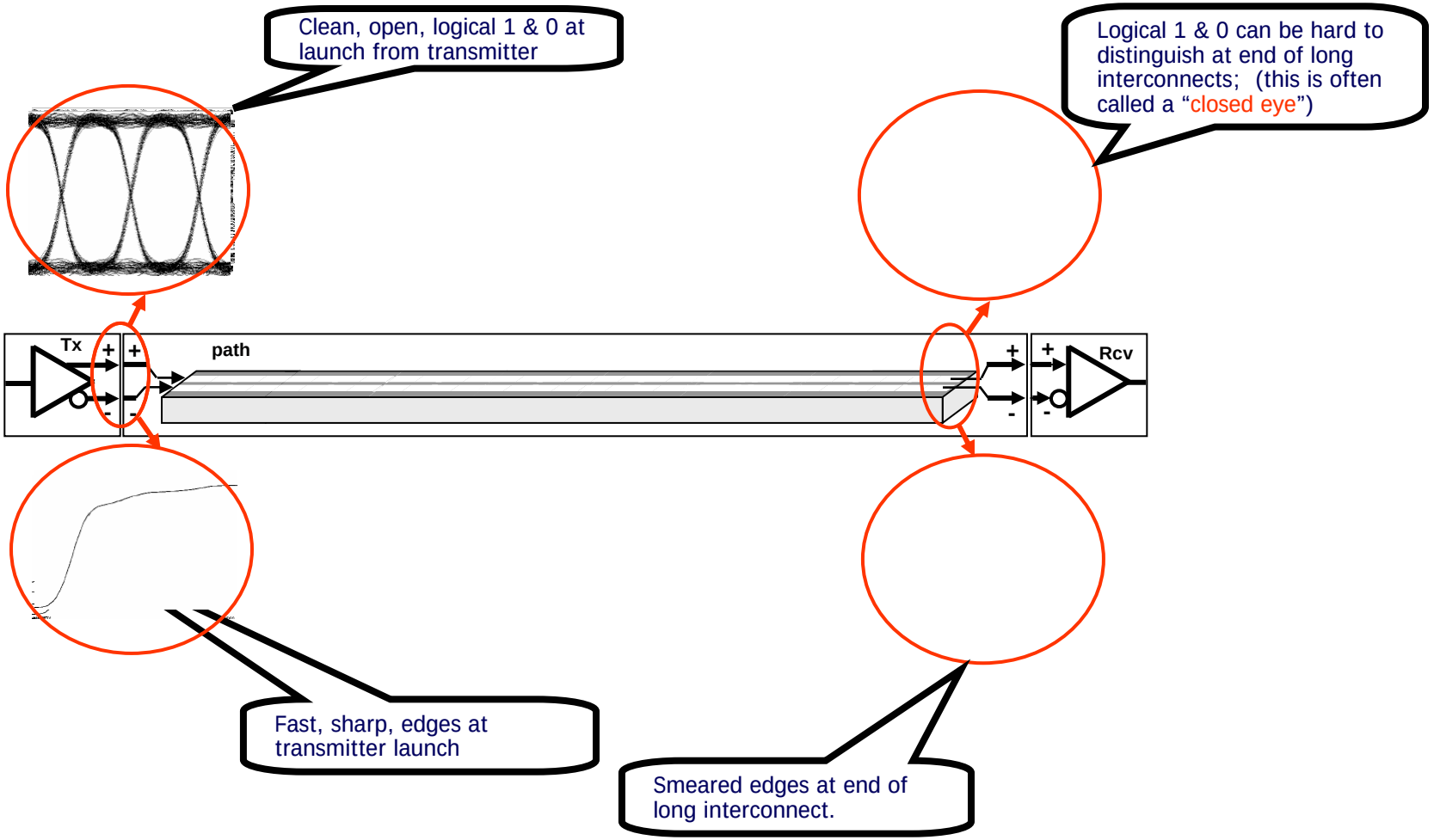
High Speed Serial Interconnect: Loss

The faster the data rate and the longer the Interconnect, then the more loss in the signal



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Receiver Performance measured with error rate

- Will the receiver work in real world conditions?
- What is the worst-case behavior?
- Send $1x10^{12}$ bits and measure 1 bit error
  - BER = 1 error / $1x\ 10^{12}$ bits = **1×10^{-12}**
- Mean time between errors
  - Needs to be meaningful (acceptable target BER)
  - Measured vs. Estimated
- Direct measurement test time example (5Gb/s)
  - Target BER of $1x10^{-6}$ = **200 useconds**
  - Target BER of $1x10^{-12}$ = **3.33 minutes**
  - Target BER of $1x10^{-15}$ = **2.31 days**

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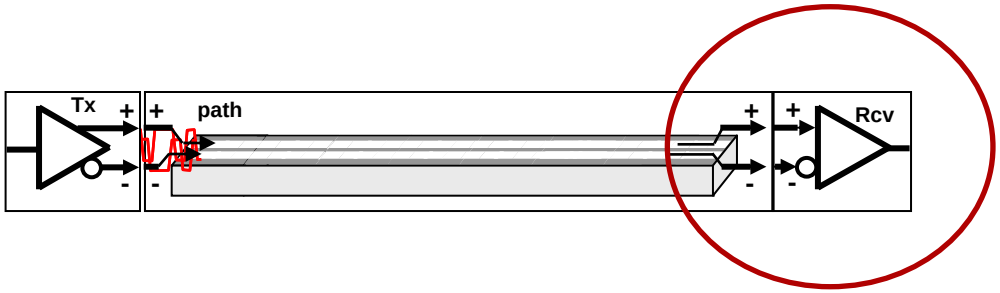
Receiver Testing

- Limit, stress and compliance test your receiver design
- Stress your Receiver in absence of the transmitter and transmission lines
- Stress your receiver with a variety of limit stress and compliance test signals

- Signal Generation
  - Increasing data-rates for high speed serial data
  - Increasing bandwidth in RF
- Replication of “Real-World” signals
  - Replicate transmission effects
  - Generate signals including all noise, jitter and other imperfections
    “known-good” and “known-bad” signals

High Speed Serial Data



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Standards define the requirements

In both design and manufacturing, requirements for receiver tests are standards-driven

All standards require Jitter Tolerance measurements for compliance

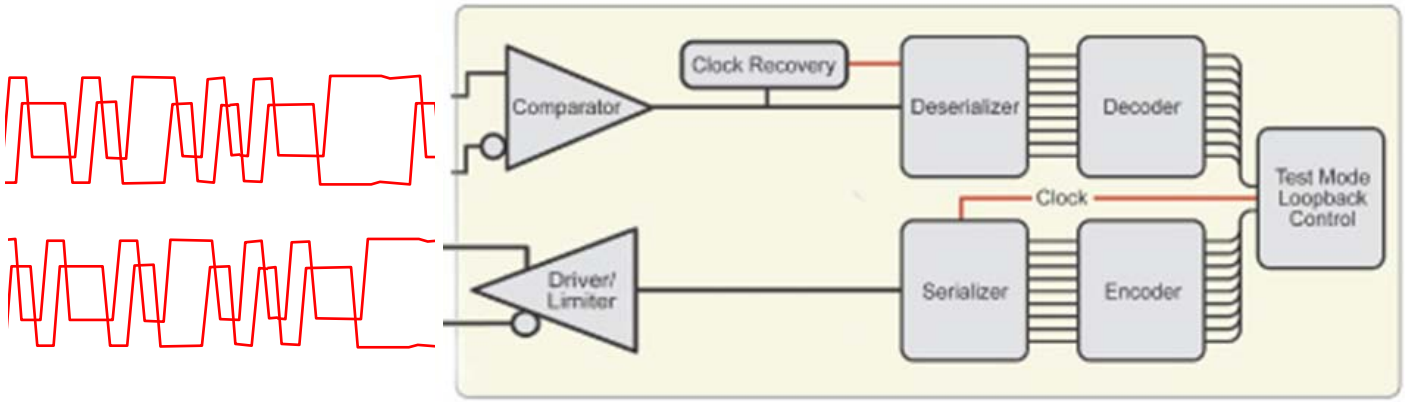
Types of devices tested:

- SerDes
- Transceivers
- Multi Media Sink devices
- Rx devices

Standard	Data Rate	Jitter Tolerance	Timing Skew	Amplitude Sensitivity	Emphasis
SATA Gen 2	3 Gb/s	★	-	★	-
PCI Express 1.0	2.5 Gb/s	★	★	★	★
PCI Express 2.0	5 Gb/s	★	★	★	★
HDMI 1.3	0.75 Gb/s to 3.4 Gb/s	★	★	★	-
FC 4, 8 G	4.25 Gb/s to 8.5 Gb/s	★	★	★	★
DisplayPort	2.7 Gb/s	★	★	★	★
USB 3.0	5 Gb/s	★	-	★	★

Loopback

- External verification of compliance pattern used with Loopback technique
- Internal operation
  - Rx signal detected at decision circuit
  - Retimed (SKPs consumed/inserted) for compensation of clock differences
  - No error correction
- Internal error counter implementation becoming more common
  - DisplayPort
  - USB 3.0



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  - Test configuration
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  - Toolset
- Summary

DisplayPort Example (from Compliance Test Specification 1.1)

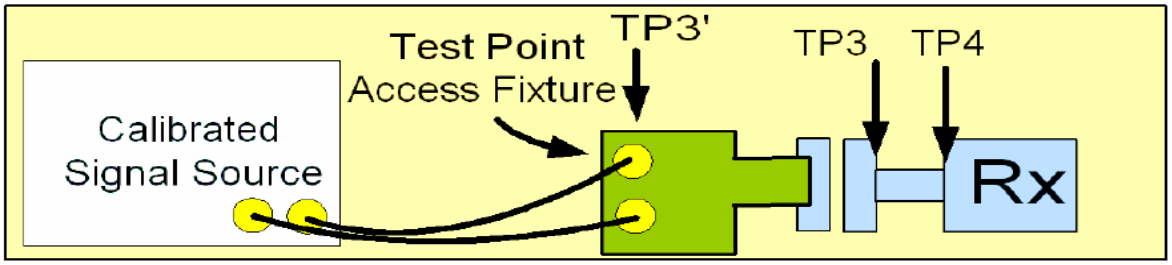
4.1 Sink Jitter Tolerance Test (Normative)

4.1.1 Test Objective

The VESA DisplayPort Standard outlines a **minimum** Receiver Eye diagram which is measured at the receiver silicon component junction. This test is designed to provide an **impaired** stimulus which has been calibrated to the minimum TP3 connector electrical properties.

4.1.2 Interoperability Statement

This test will test the receiver ability to sustain a 10E-9 BER under **most severe** signaling conditions permitted by the specification.



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Stressed Pattern Library: Putting it all together

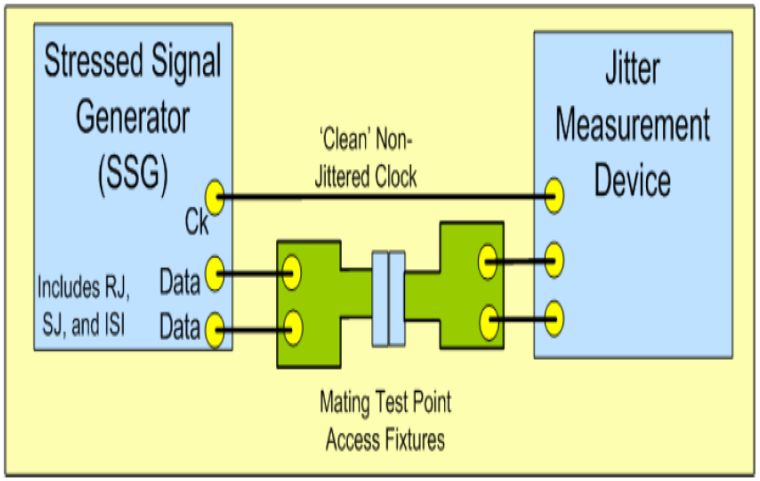

Figure 4-4: Jitter Tolerance Testing Calibration Setup

Table 4-2: Jitter Component Settings for Reduced Rate

f(Sj)	Tj(JTRBRrx)	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1648	570	7.9	981
10	~~778~~	~~570~~	~~7.9~~	~~111~~
20	747	570	7.9	80

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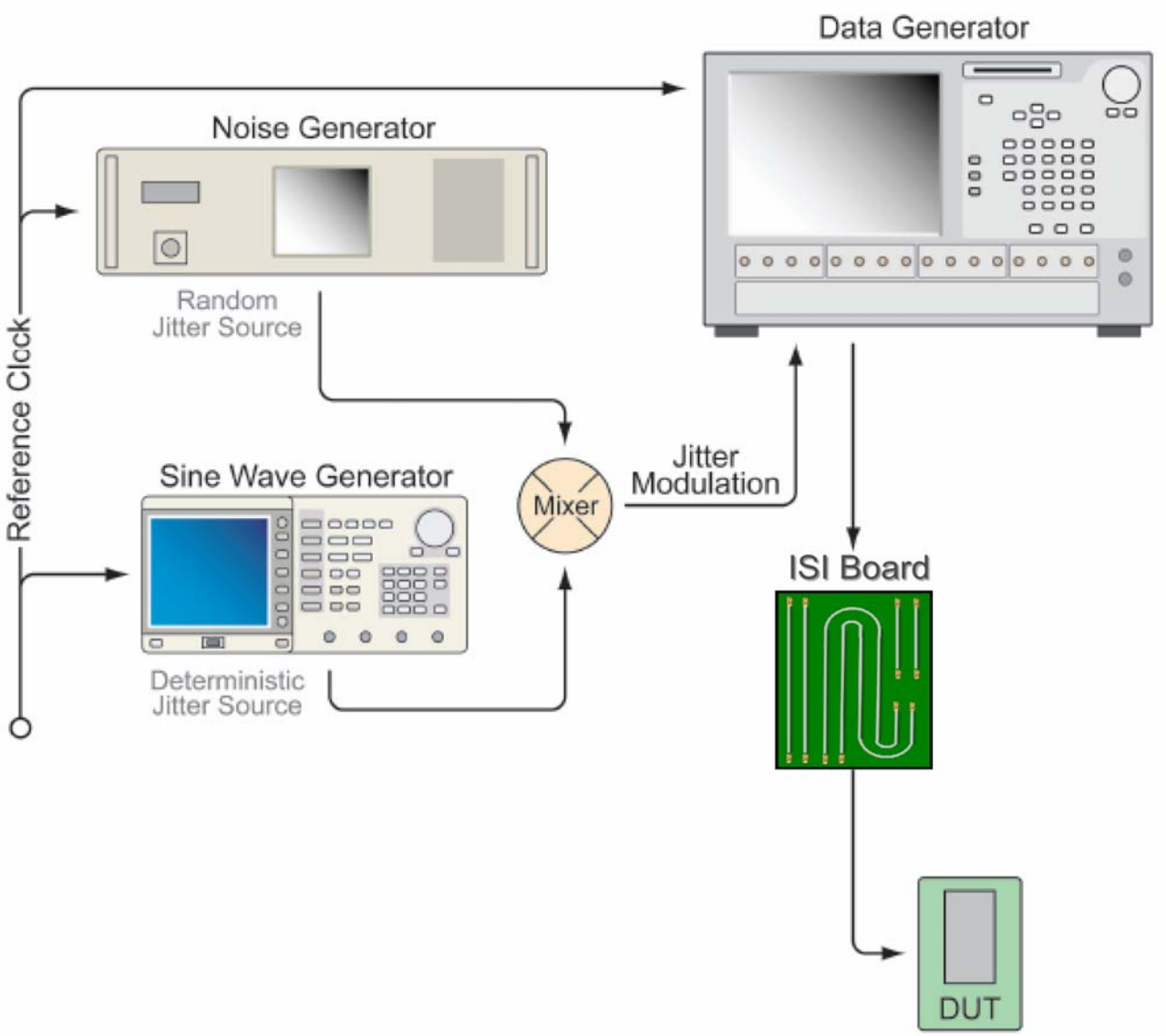
Traditional Receiver Test Configuration



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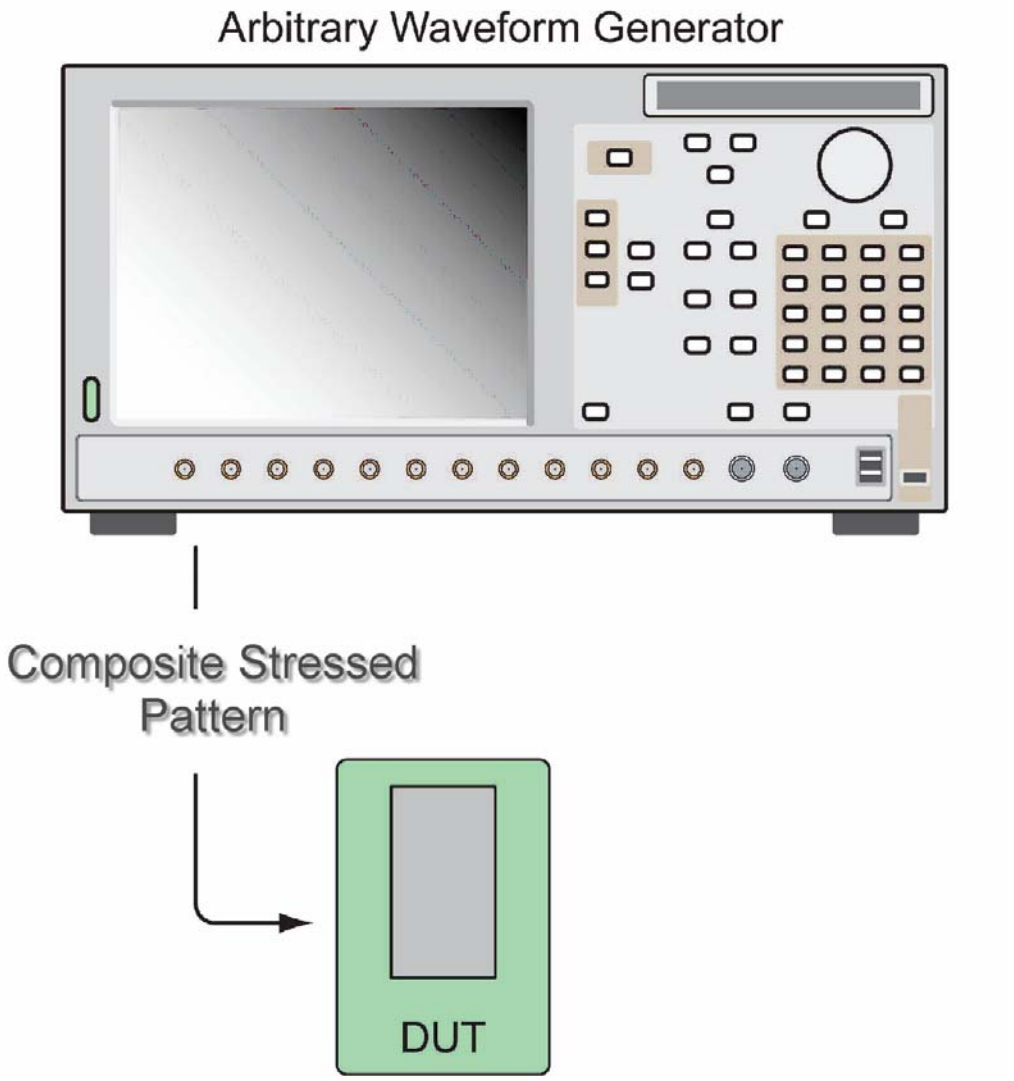
Direct Synthesis for thorough Receiver Testing



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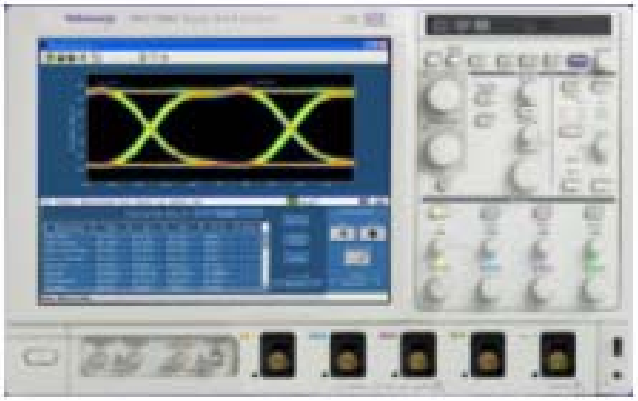
Pattern generation and calibration

AWG7122B (24GS/s)

DSA70804 (>8GHz, jitter calibration)



Lane 2 Half clock pattern on adjacent lanes

Lane 1 Stressed Pattern applied on Lane under test

Lane 0 Half clock pattern on adjacent lanes

Device Under Test

ET-DP-TPA-P (Plug fixture)

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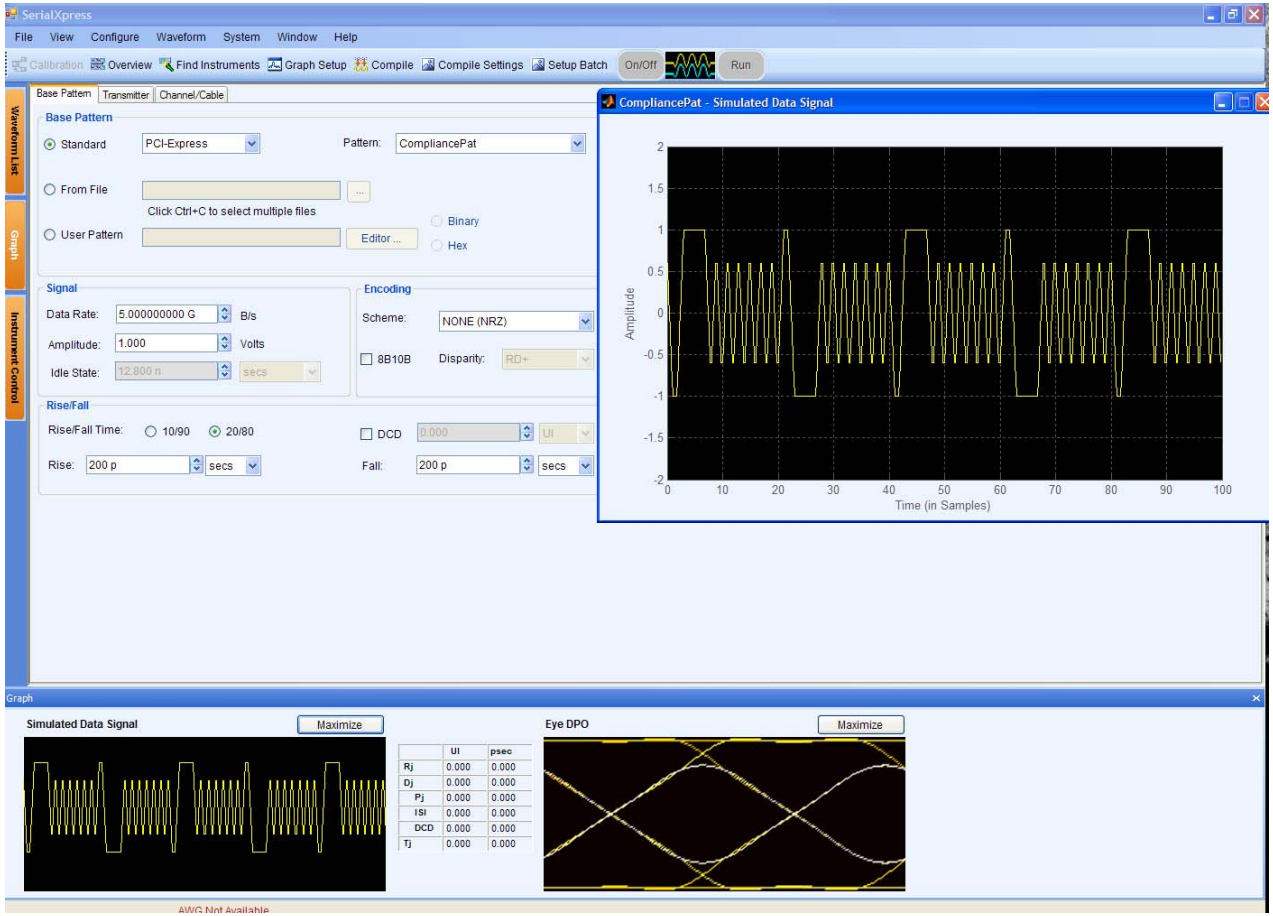
Serial Data Waveform Synthesis using SerialXpress®

Standard Base Patterns Selections

- SATA
- SAS
- HDMI
- DisplayPort
- PCIe
- Fiber Channel

Rise time setting

Graphic simulations of Compiled Data



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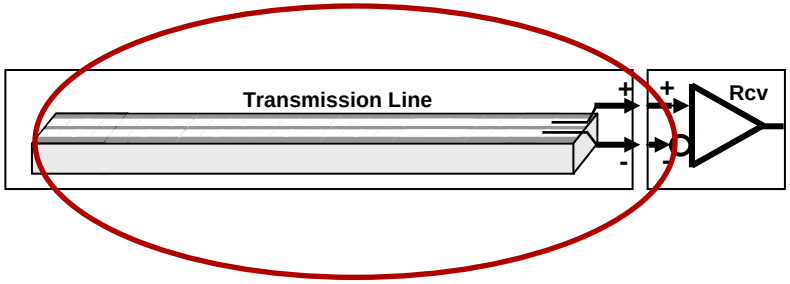
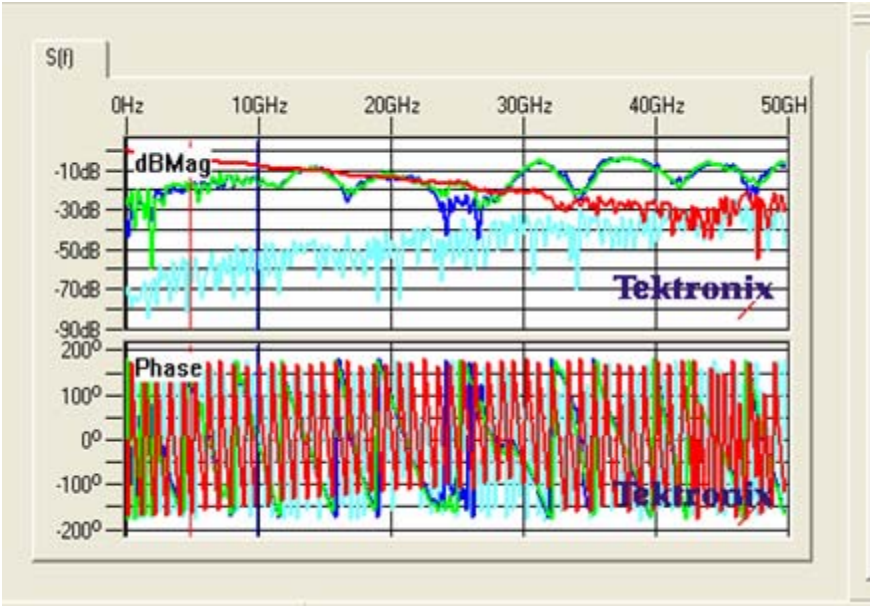
Direct Synthesis - SerialXpress®

- Direct Synthesis of ISI



High Speed Serial Data



- Extract Mixed Mode S-Parameters from a reference impairment or model them mathematically.
- Feed the s4p file into SerialXpress® , and get an exact numerical model of that response in a full digital form.
- ISI Direct settable input feature.
- ISI Scaling feature that allows for virtual cable length adjustment (what-if scenarios)

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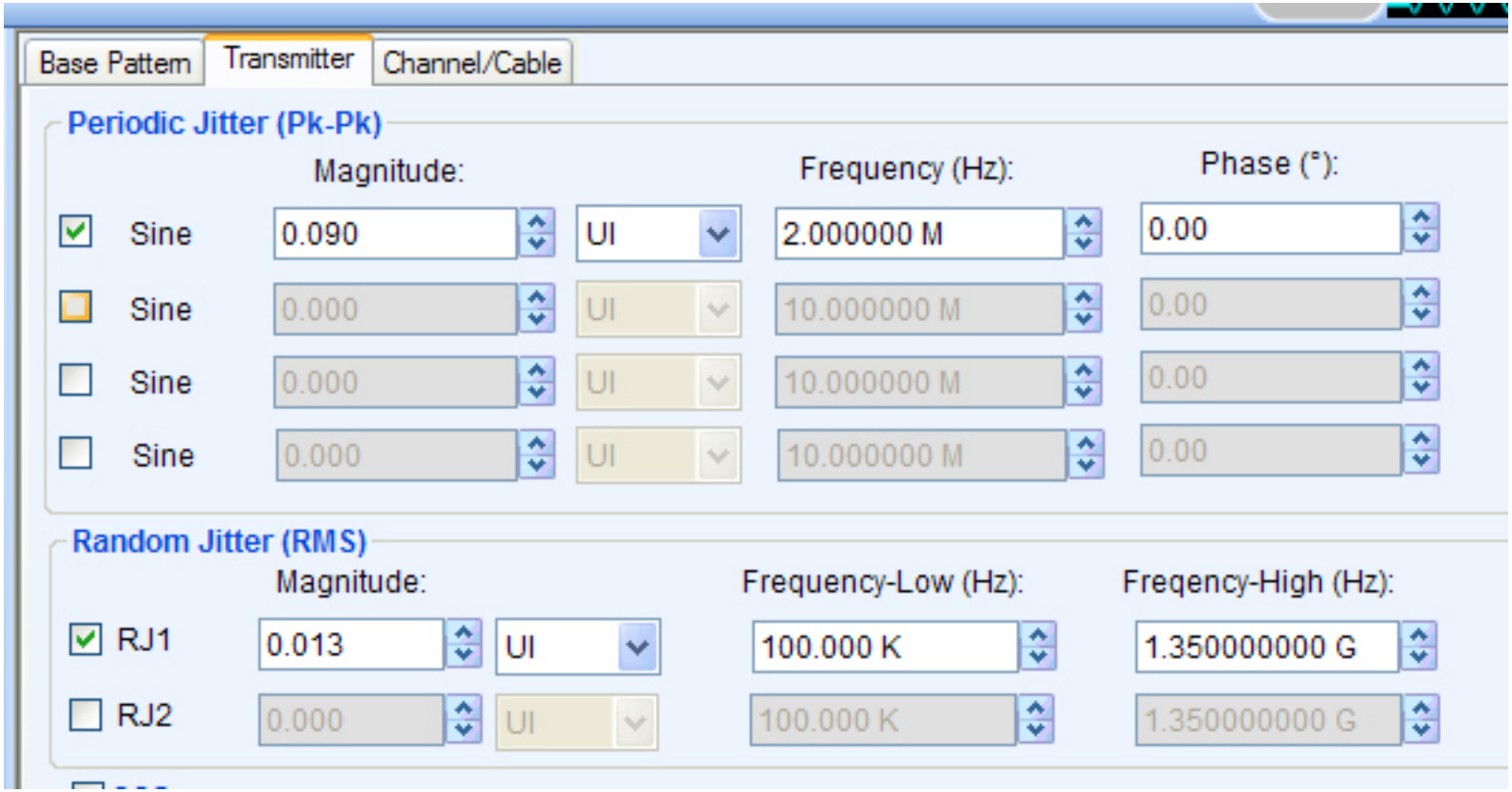
Serial Data Jitter Generation using SerialXpress®

- Up to four SJ components with freq and phase settings
- Two Random jitter components with specific bandpass settings



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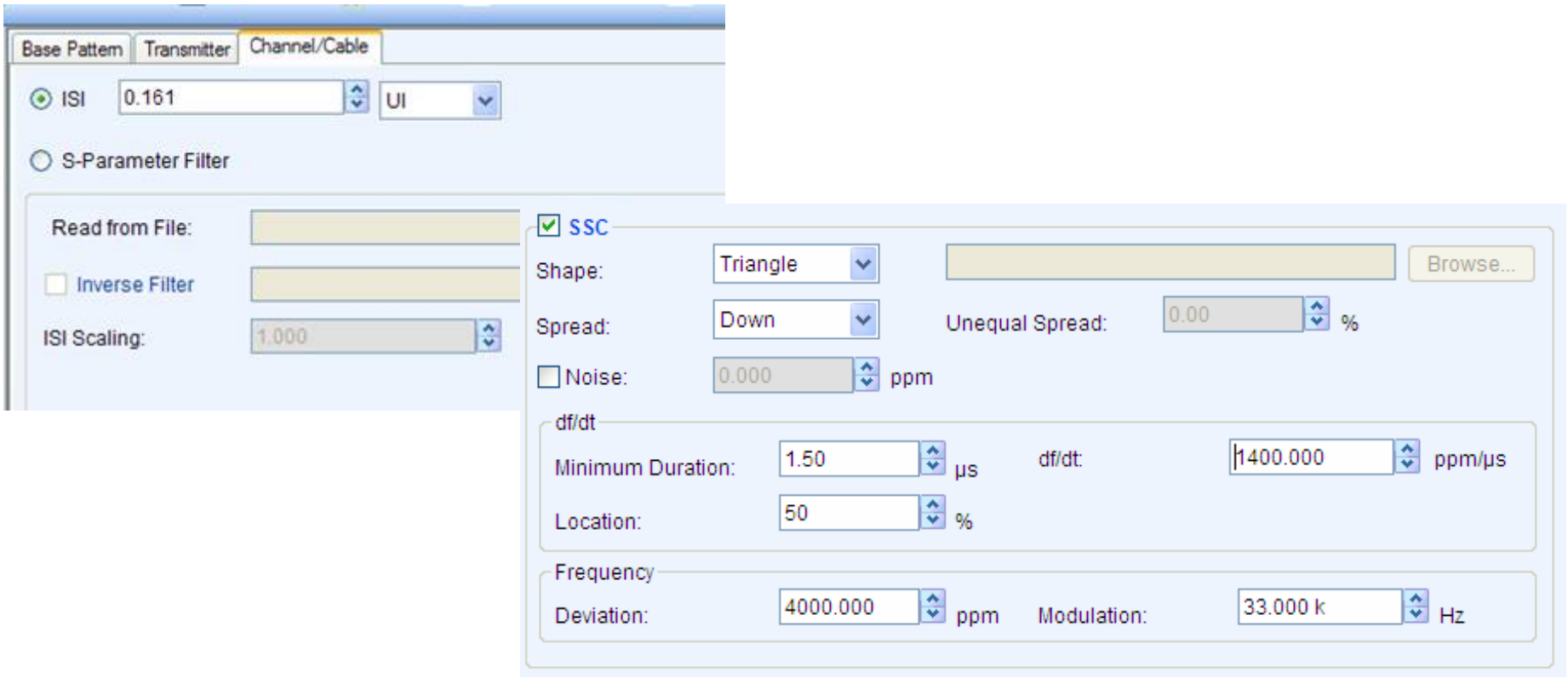
SerialXpress® makes it easy

- Dial in specific amounts of ISI or import S-Parameter TouchStone files with patented ISI scaling capability
- SSC, Pre-emphasis and Noise can also be synthesized



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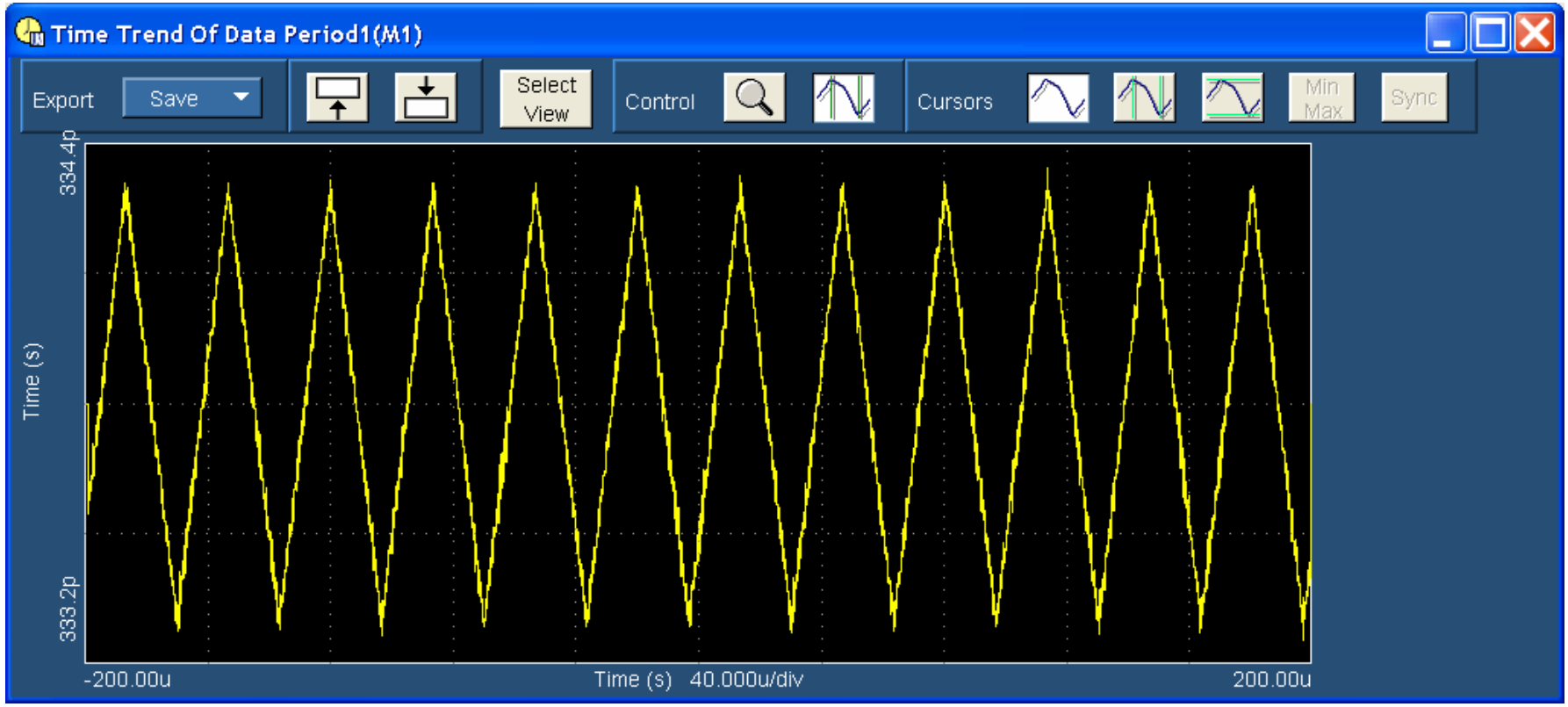
SSC Modulation Deviation Requirements:

Started simple and rapidly became a dissertation problem

Typical “good” SSC profile acquired from a SATA device



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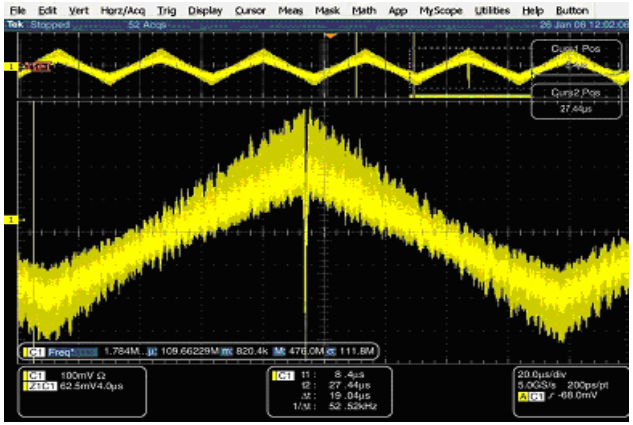
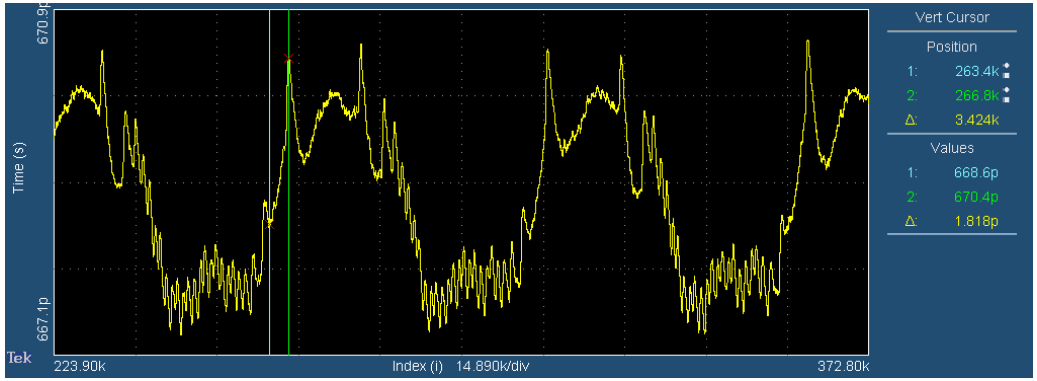
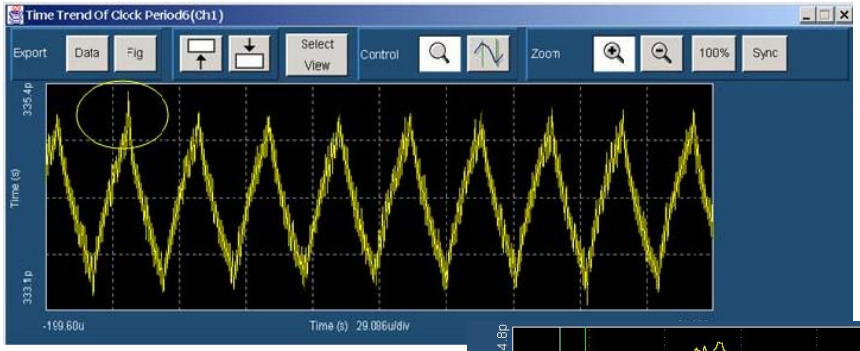
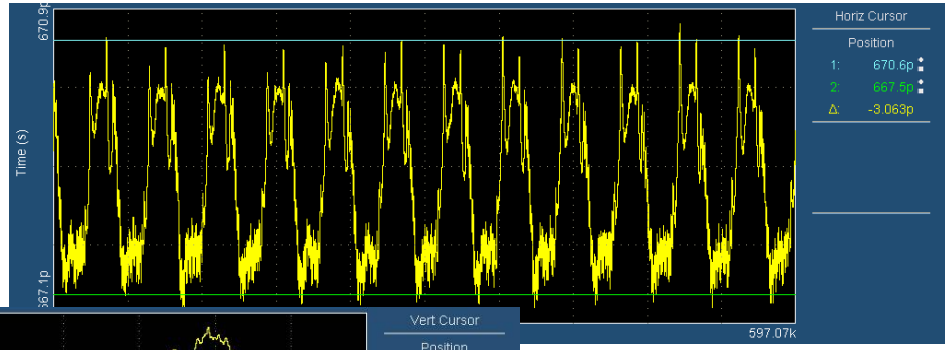
SSC Modulation Deviation Requirements:

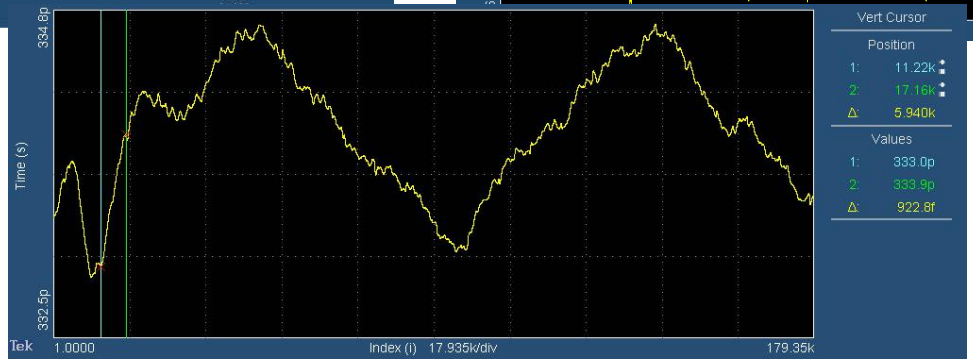
Of what value is a perfect SSC modulation in the area of stress testing?











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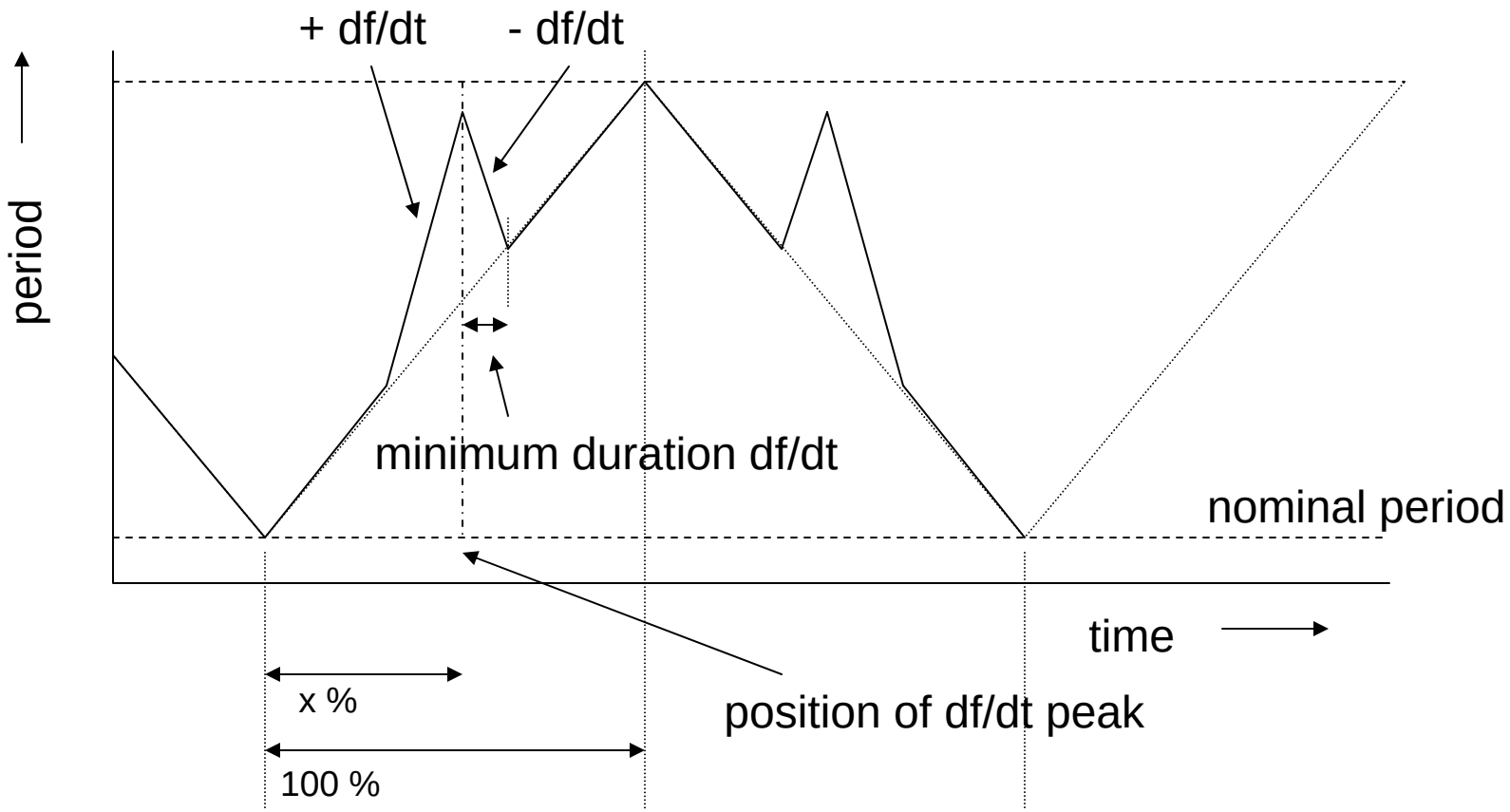
Future test requirements

Parameterized SSC df/dt impairments, along with precision jitter impairments



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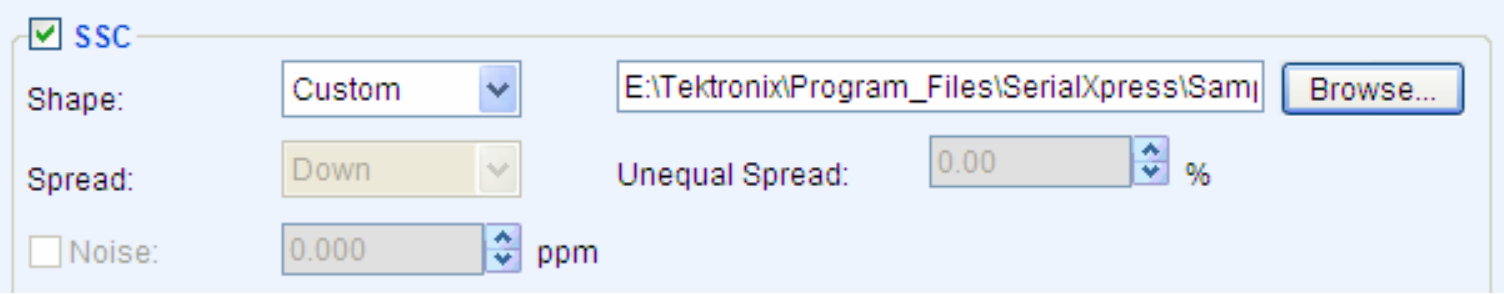
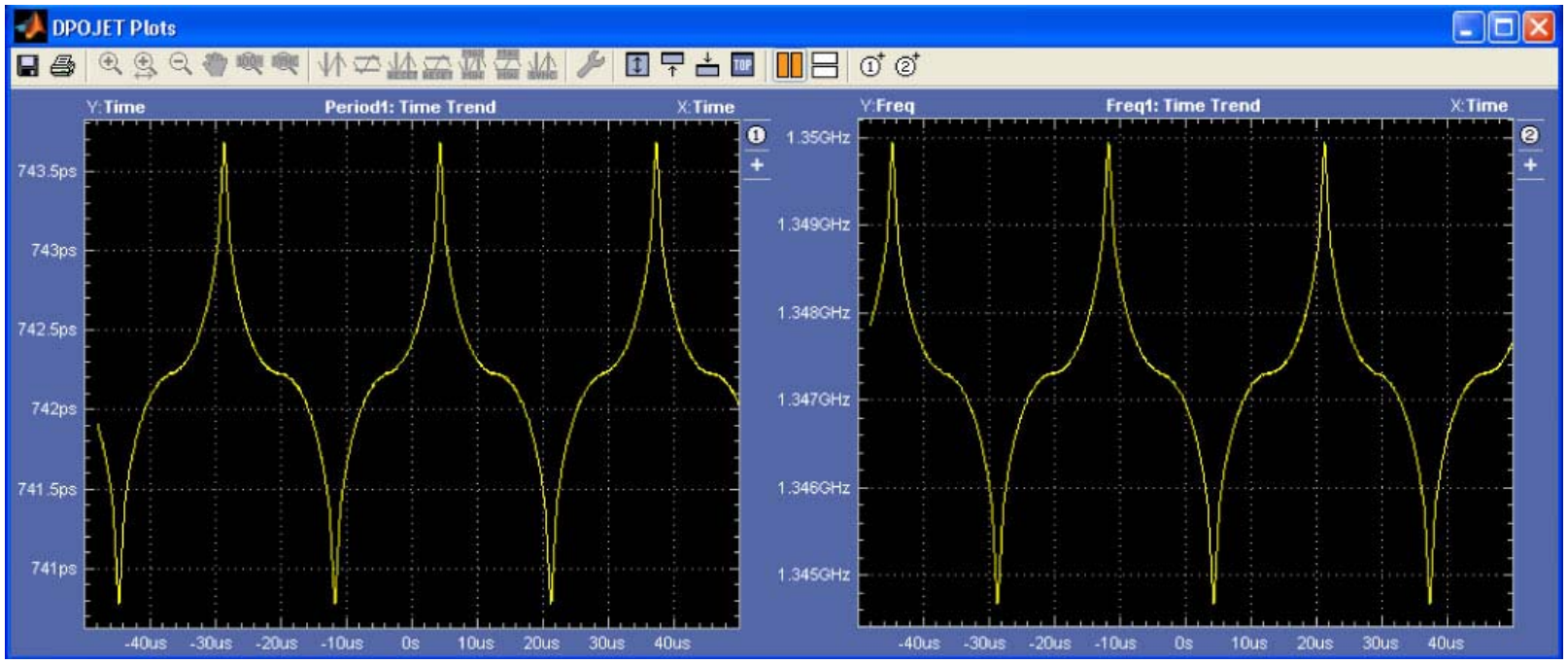
Custom SSC





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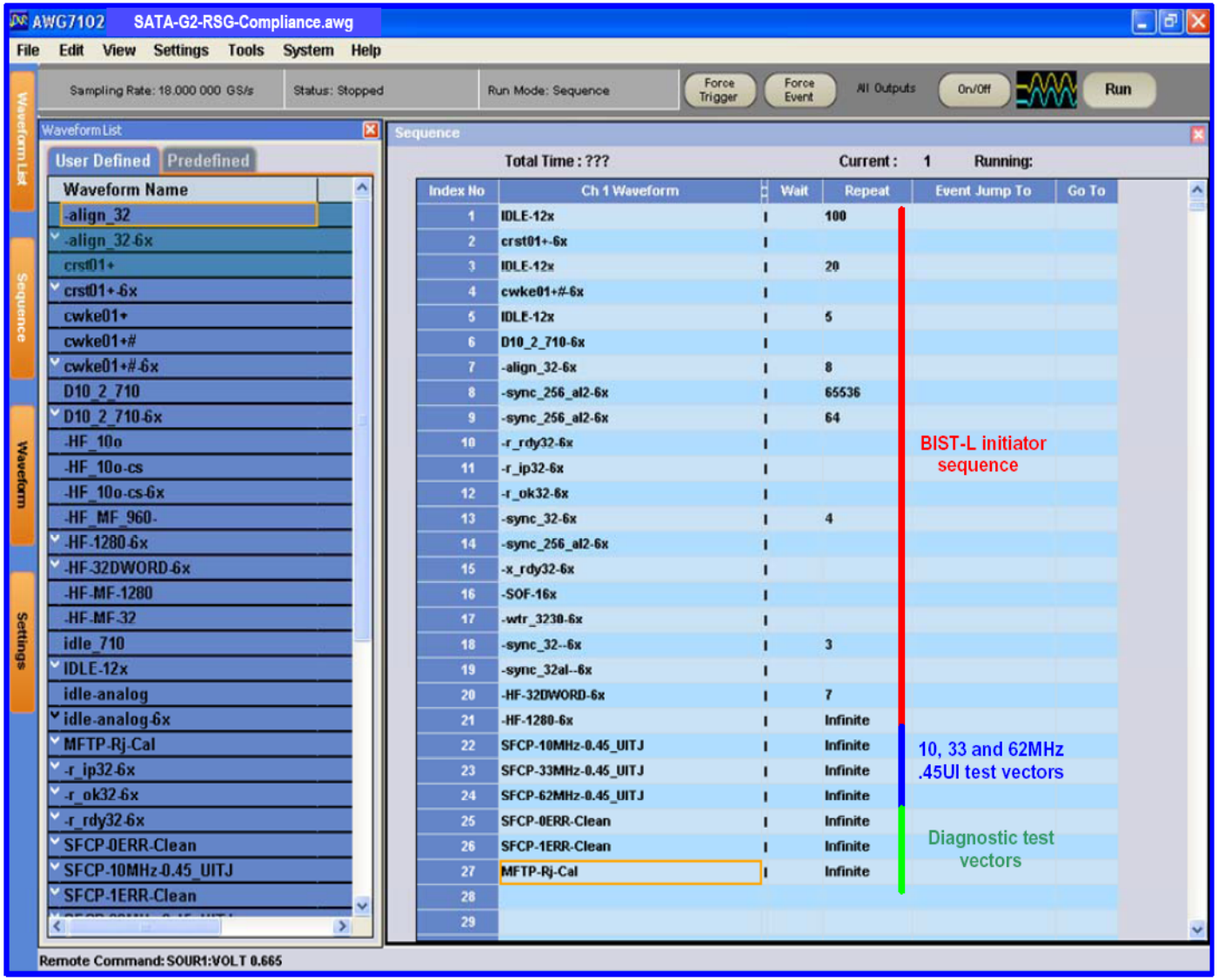
Built-In Self Test - Loopback Negotiation



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Frame Error Detection

- Clock skew management between host and device
- Requires Align primitives to not trigger error

Serial Bus	Bit Error Detector	Internal Error Detector	Frame Error Detector
PCI Express 2.0	X		
PCI Express 3.0	X[1]		
SATA Gen 2			X
SATA Gen 3			X
DisplayPort		X	
USB 3.0		X	X
HDMI 1.3			

[1] Estimate

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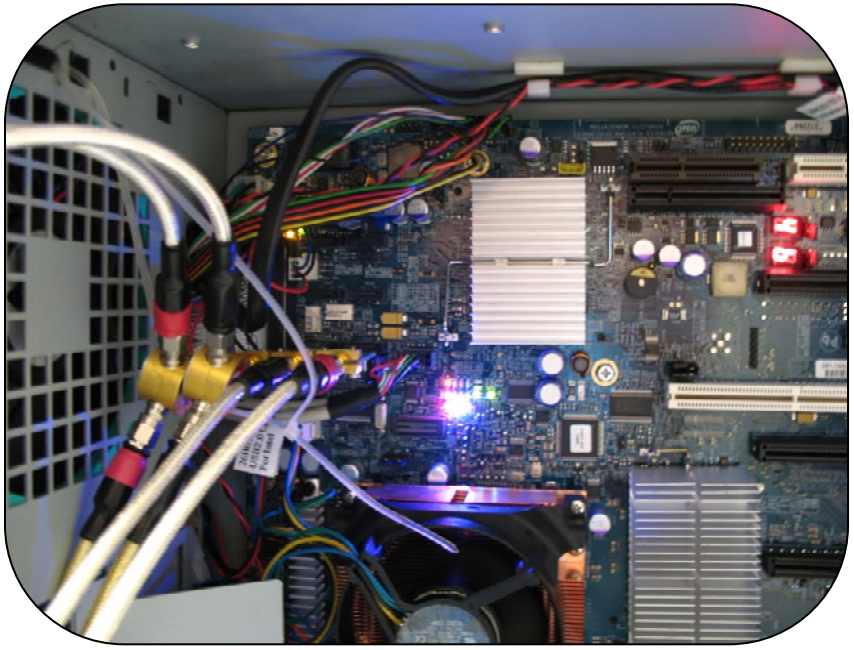
- High Speed Serial Test Challenges
  - Overview
  - Focus on Receiver Testing
  - Error Rate as an indicator
  - Loopback
- Receiver Tolerance Testing
  - Stress Pattern Library
  - Pattern Generation and Calibration
  - Frame Error Rate Detection (Protocol aware method)
- Compliance Testing
  - Methods of Implementation
  - Toolset
- Summary

SATA: Receiver Signaling Group of tests or RSG Testing.

- The Serial ATA Consortium is the first standards body to mandate silicon level support features to facilitate Receiver Testing into it's Gen-2 base specification.
- OEM's such as Dell and HP require integrators list certification to enter their supply chain.
- **RSG testing is not optional.**
- Tektronix has been at the forefront of the receiver test initiatives, and has consistently been the first to review and first to gain certification of it's test methods or MOI's.



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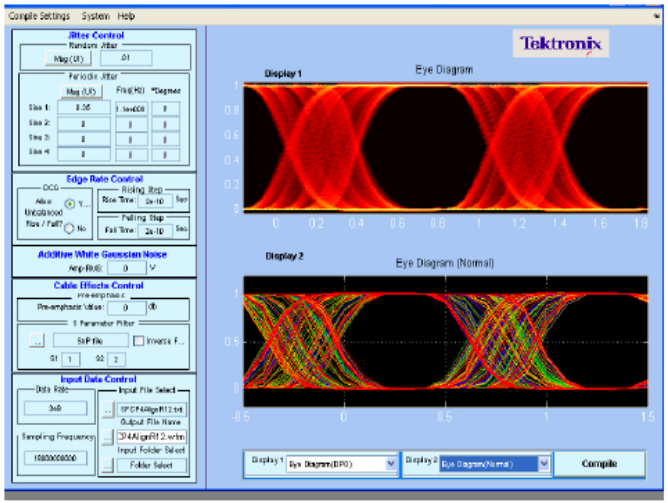
Tek RSG Method of Implementation

Tektronix, Inc.

Serial ATA
International Organization

Version 1.0RC
January 17, 2008

Serial ATA Interoperability Program Revision 1.3
Tektronix MOI for RSG Tests
(Using AWG7102 and CHS Frame Error Analyzer)



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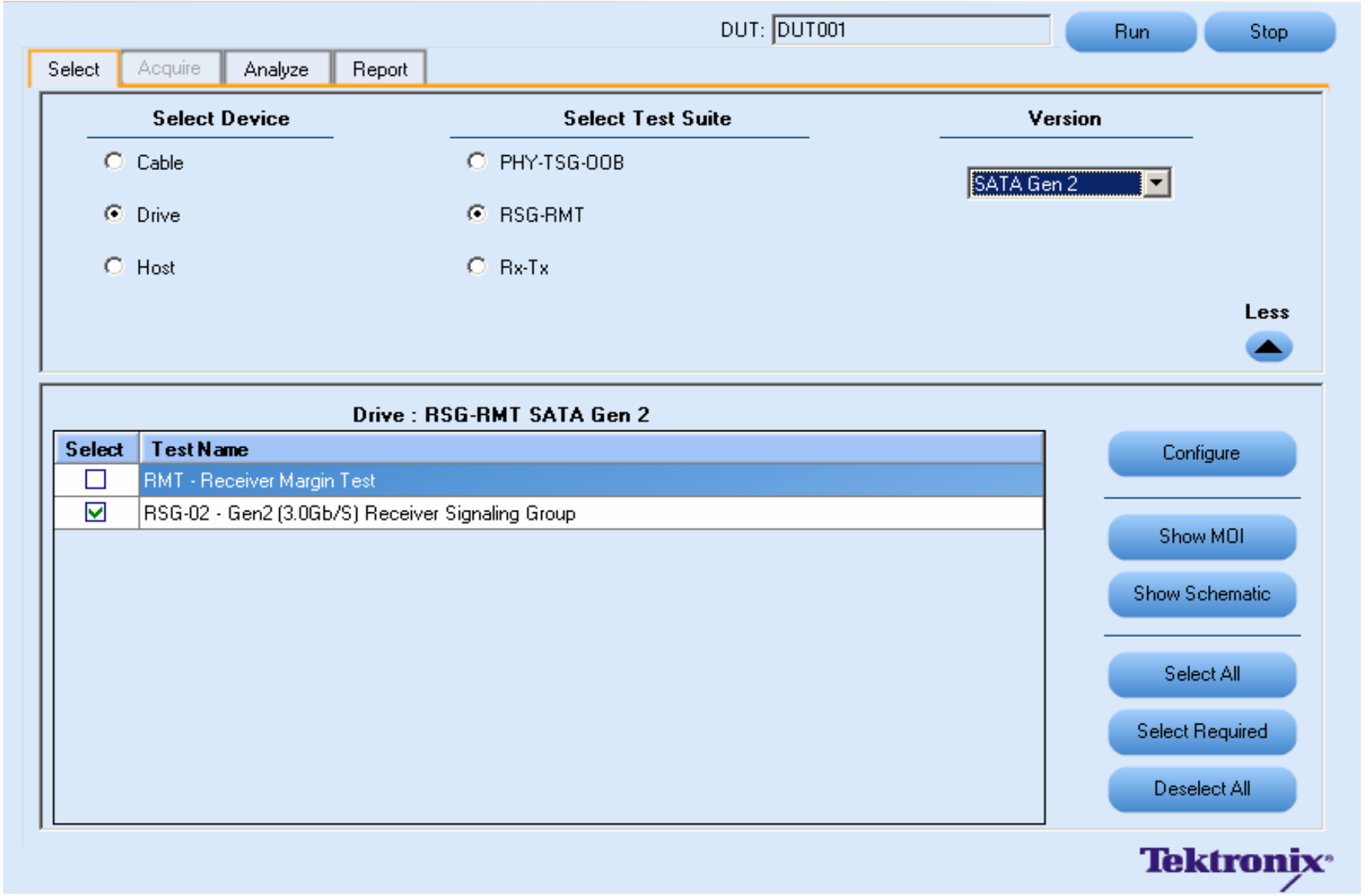
Receiver Signal Group/Receiver Margin Testing



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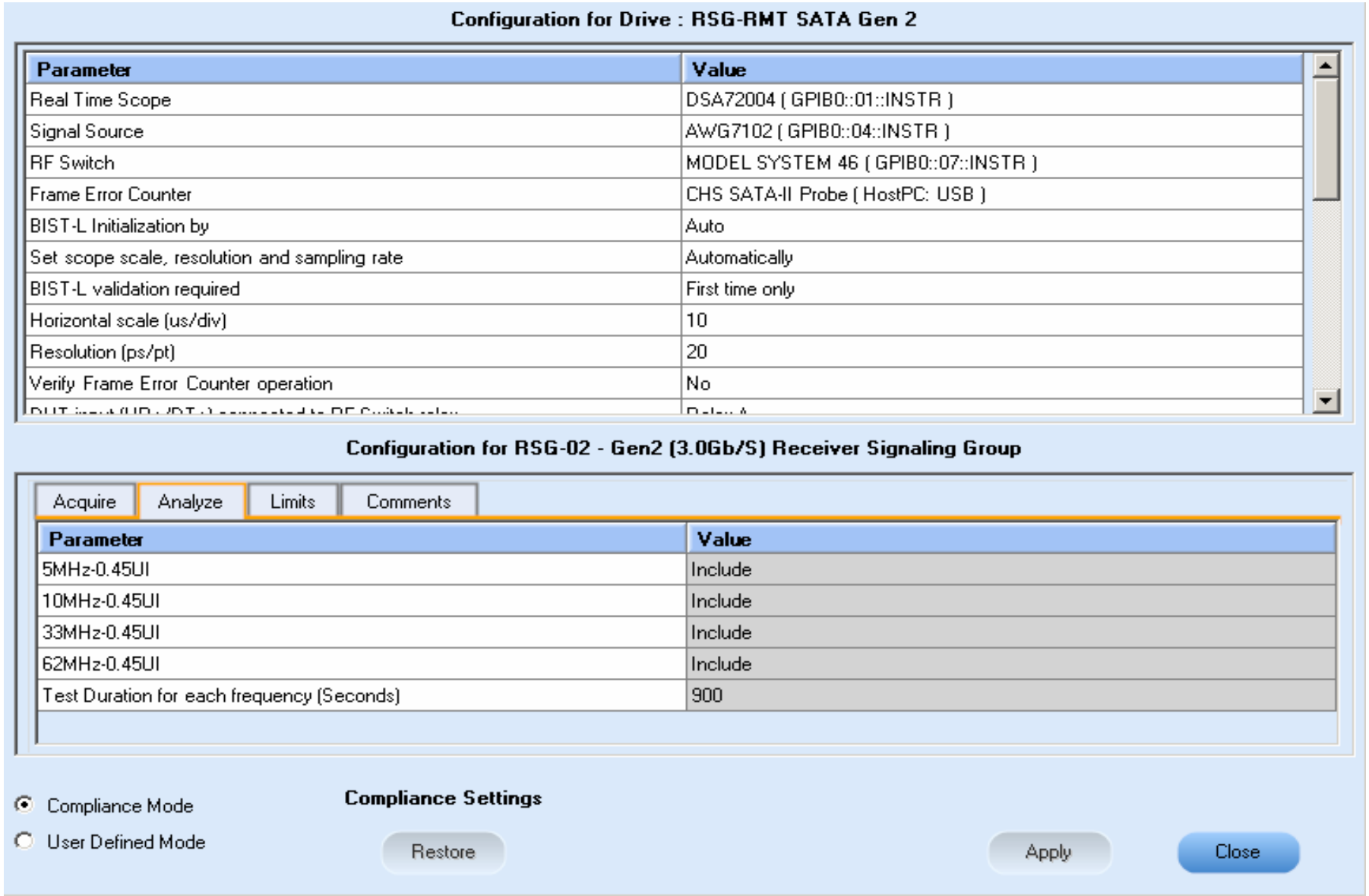
Receiver Signal Group/Receiver Margin Testing

The RSG/RMT product is broken into two different capabilities

1. RSG tracks the SATA MOI Receiver Signaling Group MOI
   - This configuration injects a SATA UTD 1.3 conformant set of four stressed signals into the device and monitors the error counter for an interval of 20 minutes. It automatically cycles through the four stressed signals (5, 10, 33 and 62 MHz), at the 20 minute points for an elapsed test time of roughly 1.5 Hours.
2. RMT Receiver Margin Test.
   - Successively apply a monotonically increasing impaired jitter profile from lower to increasing jitter magnitude and detect the point when the DUT starts to pass framing errors.
   - When Errors are detected, terminate the test at that frequency, and step to the next frequency in the test list.

Receiver Signal Group/Receiver Margin Testing



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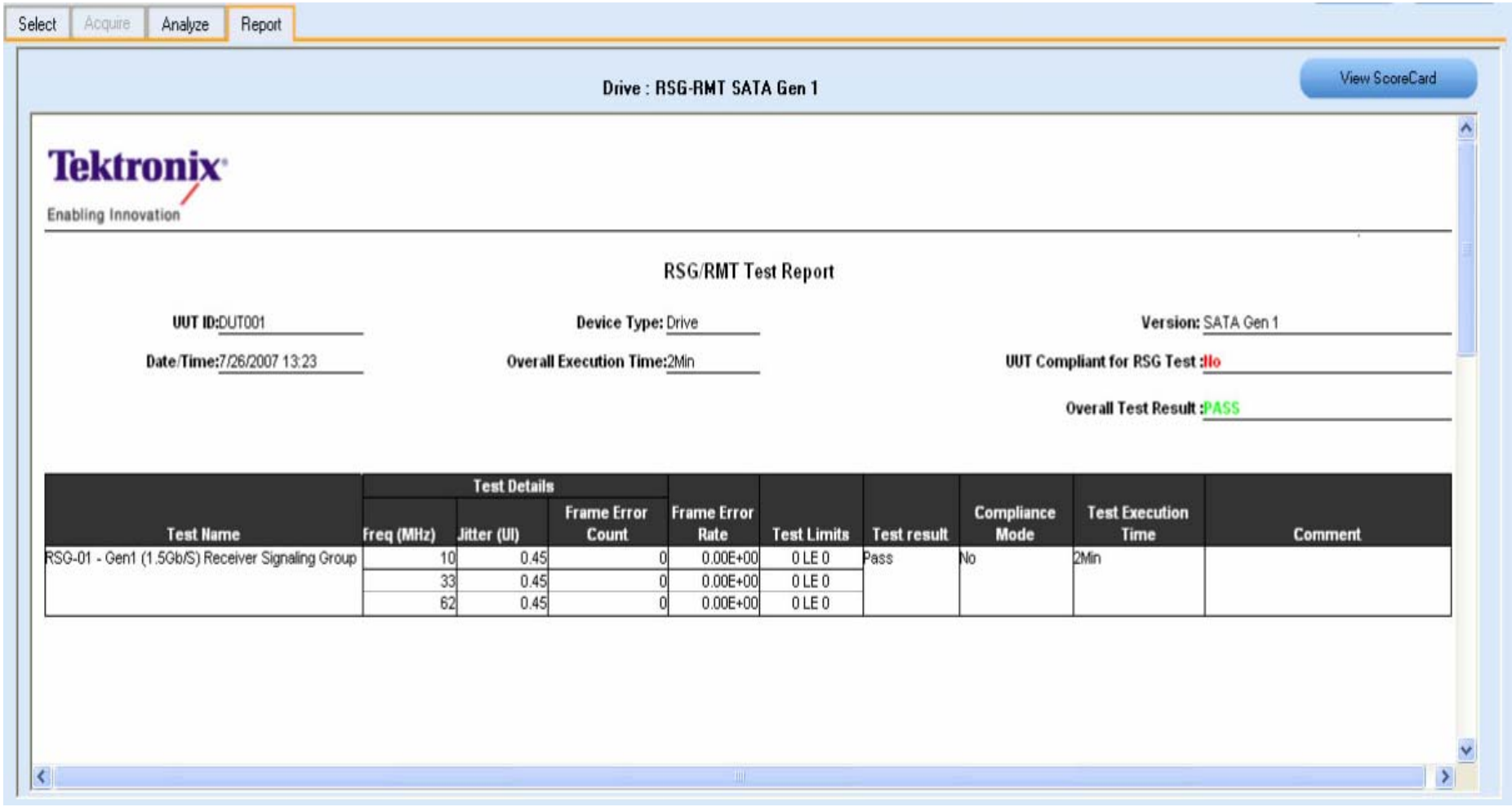

Test Name	Test Details			Frame Error Rate	Test Limits	Test result	Compliance Mode	Test Execution Time	Comment
	Freq (MHz)	Jitter (UI)	Frame Error Count						
RSG-01 - Gen1 (1.5Gb/S) Receiver Signaling Group	10	0.45	0	0.00E+00	0 LE 0	Pass	No	2Min	
	33	0.45	0	0.00E+00	0 LE 0				
	62	0.45	0	0.00E+00	0 LE 0				

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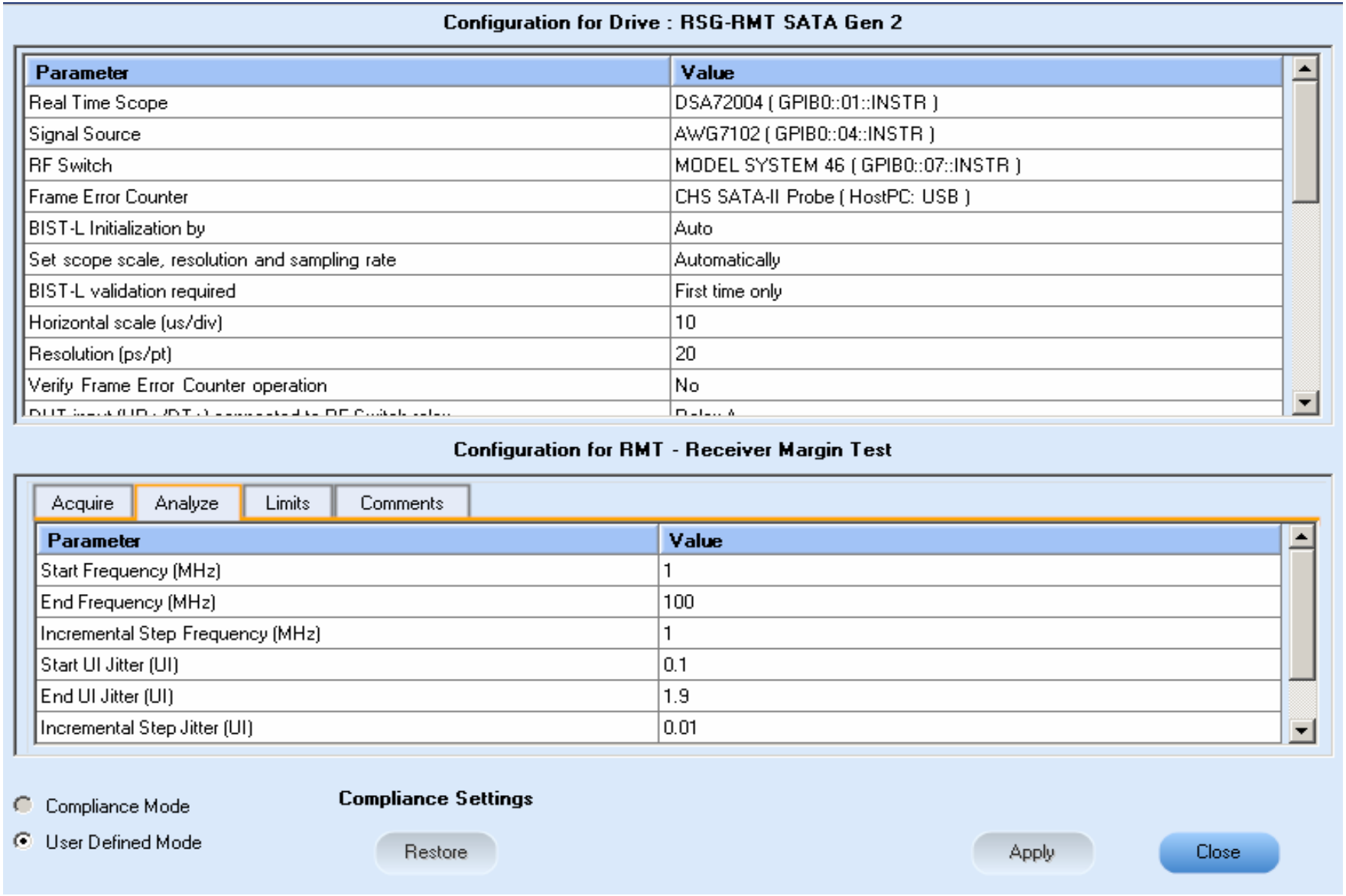

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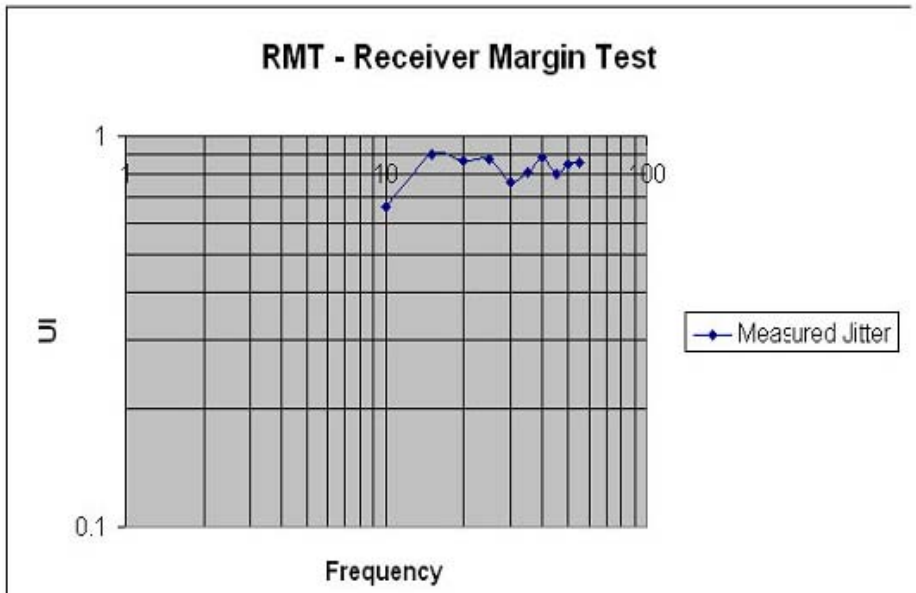
Receiver Margin Testing Jitter Tolerance Curve

Select | Acquire | Analyze | Report

Drive : RSG-RMT SATA Gen 1

View ScoreCard

Test Name	Test Details				Test Limits	Test result	Compliance Mode	Ana Executi
	Freq (MHz)	Jitter (UI)	Measured Jitter	Frame Error Rate				
RMT - Receiver Margin Test	10	0.7	0.661105345	1.51E+00	0 LE 0	Fal	Yes	1 Days 16 I
	15	1.1	0.898606564	3.34E+01	0 LE 0			
	20	1	0.862758612	2.32E+00	0 LE 0			
	25	1.1	0.871977738	1.15E+00	0 LE 0			
	30	0.9	0.765123514	1.31E+00	0 LE 0			
	35	1	0.811301178	1.23E+00	0 LE 0			
	40	1.1	0.878377846	1.20E+03	0 LE 0			
	45	1	0.797549112	1.25E+00	0 LE 0			
	50	1.1	0.845262332	3.55E+00	0 LE 0			
	55	1.1	0.858960335	2.33E+00	0 LE 0			



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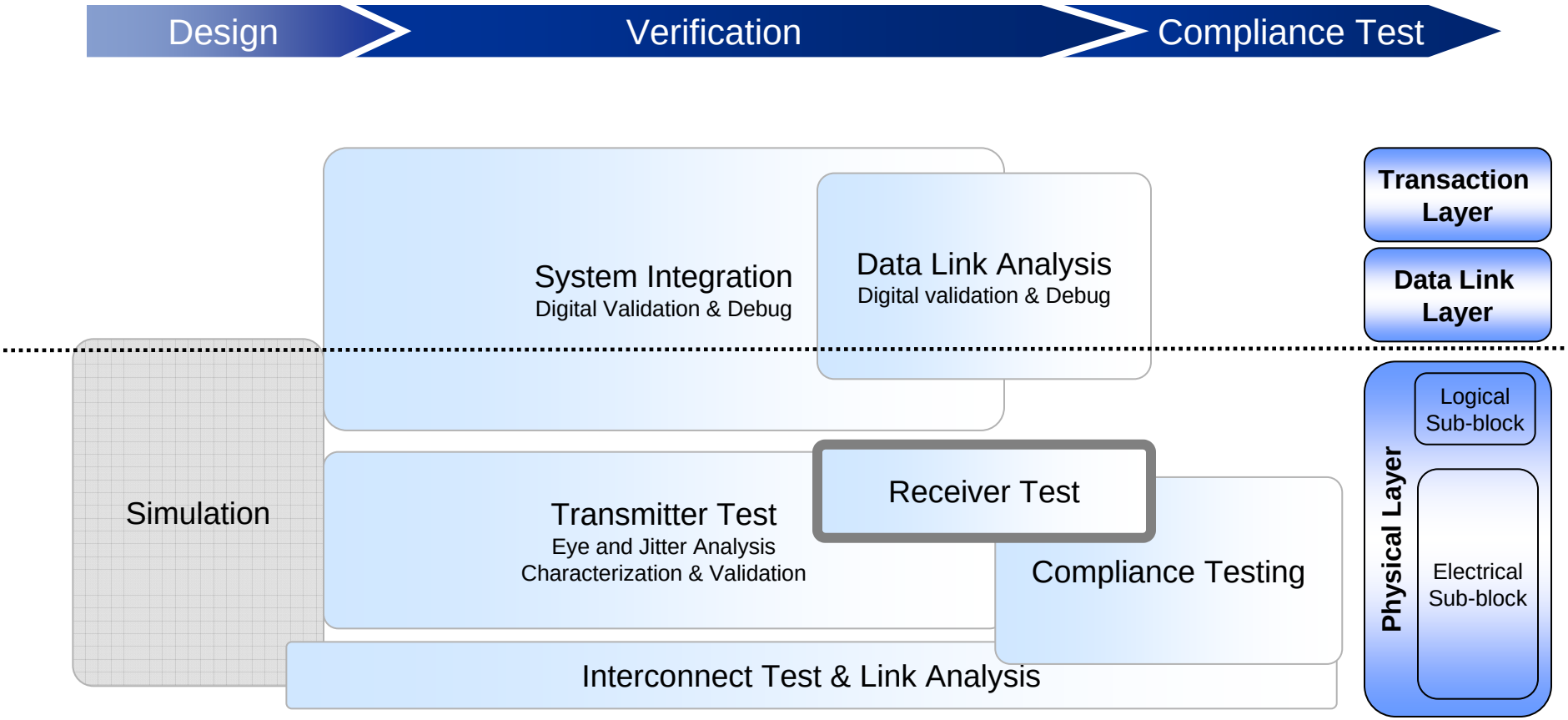
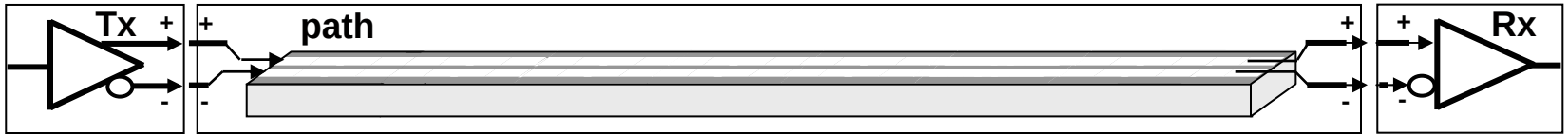
High Speed Serial Test Challenges





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Summary

- AWG7000B is a one box solution for high performance complex jitter generation
- SerialXpress® advanced jitter generation software is a powerful, easy to use to synthesize high speed serial patterns for Rx testing
- TekExpress® RSG/RMT provides a comprehensive automation system to greatly simply the receiver test's required by the SATA –IO.
  - Automatic Frame Error detector and instrument interaction.
  - AWG Digital setups fully encapsulate the Jitter profile with no external SSC, ISI, SJ generators.
- Provisions to share and propagate setups electronically is a revolutionary step forward in the receiver test industry.