Receiver Testing Methodologies





Agenda

- High Speed Serial Test Challenges
 - Overview
 - Error Rate as an indicator of performance
 - Focus on Receiver Testing
 - Loopback
- Receiver Tolerance Testing
 - Stress Pattern Library
 - Pattern Generation and Calibration
 - Frame Error Rate Detection
- Compliance Testing
 - MOIs, CTS
 - Toolset
- Summary



High Speed Serial Test Challenges







High Speed Serial Interconnect: Loss

The faster the data rate and the longer the Interconnect, then the more loss in the signal





Receiver Performance measured with error rate

- Will the receiver work in real world conditions?
- What is the worst-case behavior?
- Send 1x10¹² bits and measure 1 bit error
 - BER = 1 error / 1x 10^{12} bits = 1×10^{-12}
- Mean time between errors
 - Needs to be meaningful (acceptable target BER)
 - Measured vs. Estimated
- Direct measurement test time example (5Gb/s)
 - Target BER of 1x10⁻⁶ = <u>200 useconds</u>
 - Target BER of 1x10⁻¹² = <u>3.33 minutes</u>
 - Target BER of 1x10⁻¹⁵ = <u>2.31 days</u>







Receiver Testing

- Limit, stress and compliance test your receiver design
- Stress your Receiver in absence of the transmitter and transmission lines
- Stress your receiver with a variety of limit stress and compliance test signals
- Signal Generation
 - Increasing data-rates for high speed serial data
 - Increasing bandwidth in RF

- Replication of "Real-World" signals
 - Replicate transmission effects
 - Generate signals including all noise, jitter and other imperfections *"known-good" and "known-bad" signals*



High Speed Serial Data



Standards define the requirements

In both design and manufacturing, requirements for receiver tests are standards-driven

All standards require Jitter Tolerance measurements for compliance

Types of devices tested:

- SerDes
- Transceivers
- Multi Media Sink devices
- Rx devices

Standard	Data Rate	Jitter Tolerance	Timing Skew	Amplitude Sensitivity	Emphasis
SATA Gen 2	3 Gb/s	*	-	*	-
PCI Express 1.0	2.5 Gb/s	*	*	*	*
PCI Express 2.0	5 Gb/s	*	*	*	*
HDMI 1.3	0.75 Gb/s to 3.4 Gb/s	*	*	*	-
FC 4, 8 G	4.25 Gb/s to 8.5 Gb/s	*	*	*	*
DisplayPort	2.7 Gb/s	*	*	*	*
USB 3.0	5 Gb/s	*	-	*	*



Loopback

- External verification of compliance pattern used with Loopback technique
- Internal operation
 - Rx signal detected at decision circuit
 - Retimed (SKPs consumed/inserted) for compensation of clock differences
 - No error correction
- Internal error counter implementation becoming more common
 - DisplayPort
 - USB 3.0





Agenda

- High Speed Serial Test Challenges
 - Overview
 - Focus on receiver testing
 - Error rate as an indicator
 - Loopback
- Receiver Tolerance Testing
 - Stress pattern library
 - Test configuration
 - Pattern generation and calibration
 - Frame error rate detection (Protocol aware method)
- Compliance Testing
 - MOIs, CTS,
 - Toolset
- Summary



| 10/17/2008

DisplayPort Example (from Compliance Test Specification 1.1)

4.1 Sink Jitter Tolerance Test (Normative)

4.1.1 Test Objective

The VESA DisplayPort Standard outlines a <u>minimum</u> Receiver Eye diagram which is measured at the receiver silicon component junction. This test is designed to provide an <u>impaired</u> stimulus which has been calibrated to the minimum TP3 connector electrical properties.

4.1.2 Interoperability Statement

This test will test the receiver ability to sustain a 10E-9 BER under <u>most</u> <u>severe</u> signaling conditions permitted by the specification.





Stressed Pattern Library: Putting it all together



Figure 4-4: Jitter Tolerance Testing Calibration Setup

	Table +2. Sitter Component Settings for Reduced Rate									
f(Sj)	Tj(JTRBRrx)	ISI	RJ(RMS)	SJ						
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]						
2		570	7.9	981						
10	778	570	7.9							
20	747	570	7.9	80						

Table 4-2: Jitter Component Settings for Reduced Rate



Traditional Receiver Test Configuration



Tektronix

Direct Synthesis for thorough Receiver Testing





Pattern generation and calibration

AWG7122B (24GS/s)



ET-DP-TPA-P (Plug fixture)

DSA70804 (>8GHz, jitter calibration)



Serial Data Waveform Synthesis using SerialXpress®

Standard Base Patterns Selections

- SATA
- SAS
- HDMI
- DisplayPort
- PCIe
- Fiber Channel

Rise time setting

Graphic simulations of Compiled Data

 O Standard PCI-Express ♥ Pattern: CompliancePat O From File Click CH+C to select multiple files Binary User Pattern: Editor Hex Signal Data Rate: 5.00000000 G ♥ Bis Amplitude: 1.000 ♥ Voits Bi10B Dispanty: RbseFall Rise Fall Rise Fall Time: O 1090 ● 2080 D CD D DD D D D	ase Pattern Transmitter Channel/Cable Base Pattern		CompliancePat - Simulated Data Signal
Signal Encoding Scheme: NONE (NR2) Ide State: 0.5 Amplitude: 1.000 0 voits 0 B10B Disparity: Pt Idle State: 12800 n 0 secs 0 0.5 RiseFall RiseFall 0.000 0 U -1.5 RiseFall 0.5 -1.5 -2.0 10 20 30 40 50 60 70 80 90 11	Standard PCI-Express Circh Ctri+C to select multiple User Pattern	Pattern: CompliancePat v files Binary Editor Hex	
Rise: 200 p © secs ✓ 200 p © secs ✓ -2 0 10 20 30 40 50 60 70 80 90 1 Time (in Samples)	Signal Data Rate: 5.00000000 G ♀ B/s Amplitude: 1.000 ♀ Volts Idle State: 12.800 n ♀ secs Rise/Fall Rise/Fall Time: ○ 10/90 20/80	Cheme: NONE (NR2)	0.5 -0.5 -1 -1.5
	Rise: 200 p 🕥 secs 💌	Fail: Zuu p 👿 Secs M	-20 10 20 30 40 50 60 70 80 90 11 Time (in Samples)



Direct Synthesis - SerialXpress®





- Extract Mixed Mode S-Parameters from a reference impairment or model them mathematically.
- Feed the s4p file into SerialXpress[®], and get an exact numerical model of that response in a full digital form.
- ISI Direct settable input feature.
- ISI Scaling feature that allows for virtual cable length adjustment (what-if scenarios)



Serial Data Jitter Generation using SerialXpress®

- Up to four SJ components with freq and phase settings
- Two Random jitter components with specific bandpass settings

Base Pattern	Transmitter	Channel/Cable					
- Periodic J	litter (Pk-Pk Mag) nitude:		Frequency (Hz):		Phase (°):	
Sine	0.090	*	UI	✓ 2.000000 M	*	0.00	
Sine	0.000	*	UI	✓ 10.000000 M	*	0.00	
Sine	0.000	*	UI	✓ 10.000000 M	*	0.00	
Sine	0.000	*	UI	✓ 10.000000 M	*	0.00	
Random Jitter (RMS) Frequency-Low (Hz): Freqency-High (Hz):							
✓ RJ1	0.013	Ç UI	*	100.000 K		1.35000000 G	
🔲 RJ2	0.000	tu 🗘	~	100.000 K		1.35000000 G	



SerialXpress® makes it easy

- Dial in specific amounts of ISI or import S-Parameter TouchStone files with patented ISI scaling capability
- SSC, Pre-emphasis and Noise can also be synthesized

Base Pattern Transmitter ISI 0.161 S-Parameter Filter	Channel/Cable		
Read from File: Inverse Filter ISI Scaling:	1.000	Spread:	Triangle ♥ Browse Down ♥ Unequal Spread: 0.00 ♥ % 0.000 ♥ ppm
		df/dt Minimum Duration Location: Frequency Deviation:	n: 1.50 🔹 µs df/dt: [1400.000 🔹 ppm/µs 50 🔹 % 4000.000 🗣 ppm Modulation: 33.000 k 🗘 Hz



SSC Modulation Deviation Requirements:

Started simple and rapidly became a dissertation problem

Typical "good" SSC profile acquired from a SATA device





SSC Modulation Deviation Requirements: Of what value is a perfect SSC modulation in the area of stress testing?





Future test requirements

Parameterized SSC df/dt impairments, along with precision jitter impairments



Custom SSC







Built-In Self Test - Loopback Negotiation

ĮVC į	WG7102 SATA-G2-RSG-Com	pliance.awg						- 7 🛛
File	Edit View Settings Tools	System Help						I
Wav	Sampling Rate: 18.000 000 GS/s	Status: Stopped	F	Run Mode: Sequence	Force Trigger Event	All Output	s On/Off	Run
	WaveformList	🔀 S	equence					X
2	User Defined Predefined			Total Time : ???		Current :	1 Running:	
2	Waveform Name	^	Index No	Ch 1 Waveform	Wait	Repeat	Event Jump To Go 1	0
-	-align_32		1	IDLE-12x	i	100		-
	≚ -align_32-6x		2	crst01+-6x	1			
	crst01+		3	IDLE-12x	1	20		
th ag	≚ crst01+-6x		4	cwke01+#-6x	1			
Jen.	cwke01+		5	IDLE-12x	1	5		
8	cwke01+#		6	D10_2_710-6x	1			
	cwke01+#-6x		1	-align_32-6x	1	8		
	D10_2_710		8	-sync_256_al2-6x	1	65536		
	D10_2_710-6x		9	-sync_256_al2-6x	1	64		
\$	_HF_10o		10	-r_rdy32-6x	1		BIST-L initiator	
avef	-HF_10o-cs		11	-r_ip32-6x	1		sequence	
Ĩ	-HF_10o-cs-6x		12	-r_ok32-6x	1			
	_HF_MF_960-		13	-sync_32-6x	1	4		
	≚ -HF-1280-6×		14	-sync_256_al2-6x	1			
	-HF-32DWORD-6x		15	-x_rdy32-6x	1			
	-HF-MF-1280		16	-SOF-16x	1			
Set	-HF-MF-32		17	-wtr_3230-6x				
tting	idle_710		18	-sync_326x	1	3		
8	TIDLE-12x		19	-sync_32al6x	1			
	idle-analog		20	-HF-32DWORD-6x		7		
	≚idle-analog-6x		21	-HF-1280-6x		Infinite		
	MFTP-Rj-Cal		22	SFCP-10MHz-0.45_UITJ		Infinite	10, 33 and 62MHz	
	∑_r_ip32.6x		23	SFCP-33MHz-0.45_UITJ		Infinite	.45UI test vectors	
	∑ -r_ok32-6x		24	SFCP-62MHz-0.45_UITJ	1	Infinite		
	∑-r_rdy32-6x		25	SFCP-0ERR-Clean	1	Infinite	Discussedia dast	
	SFCP-0ERR-Clean		26	SFCP-1ERR-Clean	1	Infinite	Diagnostic test	
	SFCP-10MHz-0.45_UITJ		27	MFTP-Rj-Cal	1	Infinite	vectors	
	SFCP-1ERR-Clean	× 1	28			•		
	<	X	29					~
	Remote Command: SOUR1:VOLT 0.66	\$5						



Frame Error Detection

- Clock skew management between host and device
- Requires Align primitives to not trigger error

Serial Bus	Bit Error Detector	Internal Error Detector	Frame Error Detector
PCI Express 2.0	X		
PCI Express 3.0	X ¹		
SATA Gen 2			X
SATA Gen 3			Х
DisplayPort		X	
USB 3.0		X	Х
HDMI 1.3			

¹ Estimate

1

10/17/2008



Agenda

- High Speed Serial Test Challenges
 - Overview
 - Focus on Receiver Testing
 - Error Rate as an indicator
 - Loopback
- Receiver Tolerance Testing
 - Stress Pattern Library
 - Pattern Generation and Calibration
 - Frame Error Rate Detection (Protocol aware method)
- Compliance Testing
 - Methods of Implementation
 - Toolset
- Summary



SATA: Receiver Signaling Group of tests or RSG Testing.

- The Serial ATA Consortium is the first standards body to mandate silicon level support features to facilitate Receiver Testing into it's Gen-2 base specification.
- OEM's such as Dell and HP require integrators list certification to enter their supply chain.
- RSG testing is not optional.
- Tektronix has been at the forefront of the receiver test initiatives, and has consistently been the first to review and first to gain certification of it's test methods or MOI's.





Tek RSG Method of Implementation





				DUT: [DUT001	Run Stop
elect	Acquire	Analyze	Report		
	Select	Device		Select Test Suite	Version
C	Cable			O PHY-TSG-00B	CATA Con 2
œ	Drive			RSG-RMT	SATA den 2
C	Host			O Bx-Tx	
					Less
			Drive : I	RSG-RMT SATA Gen 2	
5 elect	t TestNa	ame			Configure
	BMT - Be	eceiver Margir	n Tiest		
	RSG-02	· Gen2 (3.0Gb	/S) Receive	r Signaling Group	Show MOI
					Show Schematic
					Select All
					Select Required
					Deselect All
					Tektronix
	_				Taktro

The RSG/RMT product is broken into two different capabilities

- 1. RSG tracks the SATA MOI Receiver Signaling Group MOI
 - This configuration injects a SATA UTD 1.3 conformant set of four stressed signals into the device and monitors the error counter for an interval of 20 minutes. It automatically cycles through the four stressed signals (5, 10, 33 and 62 MHz), at the 20 minute points for an elapsed test time of roughly 1.5 Hours.
- 2. RMT Receiver Margin Test.
 - Successively apply a monotonically increasing impaired jitter profile from lower to increasing jitter magnitude and detect the point when the DUT starts to pass framing errors.
 - When Errors are detected, terminate the test at that frequency, and step to the next frequency in the test list.



Configuration for Drive : RSG-RMT SATA Gen 2

Parameter	Value
Real Time Scope	DSA72004 (GPIB0::01::INSTR)
Signal Source	AWG7102 (GPIB0::04::INSTR)
RF Switch	MODEL SYSTEM 46 (GPIB0::07::INSTR)
Frame Error Counter	CHS SATA-II Probe (HostPC: USB)
BIST-L Initialization by	Auto
Set scope scale, resolution and sampling rate	Automatically
BIST-L validation required	First time only
Horizontal scale (us/div)	10
Resolution (ps/pt)	20
Verify Frame Error Counter operation	No
	Delen A

Configuration for RSG-02 - Gen2 (3.0Gb/S) Receiver Signaling Group

Acquire Analyze Limits Comments					
Parameter	Value				
5MHz-0.45UI	Include				
10MHz-0.45UI	Include				
33MHz-0.45UI	Include Include				
62MHz-0.45UI					
Test Duration for each frequency (Seconds)	900				
Compliance Mode Compliance Settings					

C User Defined Mode Restore Apply Close



10/17/2008

elect Acquire Analyze Report					
	Drive : F	ISG-RMT SATA Gen 1			View ScoreCard
Tektronix					<u>^</u>
Enabling Innovation					
		RSG/RMT Test Report			
UUT ID:DUT001	Device Type:	Drive		Version: SATA	en 1
Date/Time:7/26/2007 13:23	Overall Execution Time	::2Min	UUT Con	npliant for RSG Test : <mark>Ilo</mark>	
				Overall Test Result : <mark>PASS</mark>	
	Test Details				
Test Name	Frame Error Freq (MHz) Jitter (UI) Count	Frame Error Rate Test Limit	Compliance Test result Mode	Test Execution Time	Comment
RSG-01 - Gen1 (1.5Gb/S) Receiver Signaling Group	10 0.45 0 33 0.45 0	0 0.00E+00 0 LE 0 0 0.00E+00 0 LE 0	Pass No	2Min	
×	62 0.45 0	0 0.00E+00 0 LE 0			
					~



The RSG/RMT product is broken into two different capabilities

- 1. RSG tracks the SATA MOI Receiver Signaling Group MOI
 - This configuration injects a SATA UTD 1.3 conformant set of four stressed signals into the device and monitors the error counter for an interval of 20 minutes. It automatically cycles through the four stressed signals (5, 10, 33 and 62 MHz), at the 20 minute points for an elapsed test time of roughly 1.5 Hours.

2. RMT Receiver Margin Test.

- Successively apply a monotonically increasing impaired jitter profile from lower to increasing jitter magnitude and detect the point when the DUT starts to pass framing errors.
- When Errors are detected, terminate the test at that frequency, and step to the next frequency in the test list.



Configuration for Drive : RSG-RMT SATA Gen 2

Parameter	Value	
Real Time Scope	DSA72004 (GPIB0::01::INSTR)	
Signal Source	AWG7102 (GPIB0::04::INSTR)	
RF Switch	MODEL SYSTEM 46 (GPIB0::07::INSTR)	
Frame Error Counter	CHS SATA-II Probe (HostPC: USB)	
BIST-L Initialization by	Auto	
Set scope scale, resolution and sampling rate	Automatically	
BIST-L validation required	First time only	
Horizontal scale (us/div)	10	
Resolution (ps/pt)	20	
Verify Frame Error Counter operation	No	
	Delau à	

Configuration for RMT - Receiver Margin Test

Acquire Analyze Limits Comments	
Parameter	Value
Start Frequency (MHz)	1
End Frequency (MHz)	100
Incremental Step Frequency (MHz)	1
Start UI Jitter (UI)	0.1
End UI Jitter (UI)	1.9
Incremental Step Jitter (UI)	0.01

🧧 Compliance Mode

Compliance Settings

💿 User Defined Mode

Restore





Close

Apply

Receiver Margin Testing Jitter Tolerance Curve



10/17/2008



Agenda

- High Speed Serial Test Challenges
 - Overview
 - Focus on Receiver Testing
 - Error Rate as an indicator
 - Loopback
- Receiver Tolerance Testing
 - Stress Pattern Library
 - Pattern Generation and Calibration
 - Frame Error Rate Detection (Protocol aware method)
- Compliance Testing
 - MOIs, CTS,
 - Toolset
- Summary



High Speed Serial Test Challenges







Summary

- AWG7000B is a one box solution for high performance complex jitter generation
- SerialXpress® advanced jitter generation software is a powerful, easy to use to synthesize high speed serial patterns for Rx testing
- TekExpress® RSG/RMT provides a comprehensive automation system to greatly simply the receiver test's required by the SATA –IO.
 - Automatic Frame Error detector and instrument interaction.
 - AWG Digital setups fully encapsulate the Jitter profile with no external SSC, ISI, SJ generators.
- Provisions to share and propagate setups electronically is a revolutionary step forward in the receiver test industry.

