Receiver Testing Methodologies
Agenda

- High Speed Serial Test Challenges
  - Overview
  - Error Rate as an indicator of performance
  - Focus on Receiver Testing
  - Loopback

- Receiver Tolerance Testing
  - Stress Pattern Library
  - Pattern Generation and Calibration
  - Frame Error Rate Detection

- Compliance Testing
  - MOIs, CTS
  - Toolset

- Summary
High Speed Serial Test Challenges

- Design
  - Verification
  - Compliance Test

- Simulation
  - System Integration
    - Digital Validation & Debug
  - Transmitter Test
    - Eye and Jitter Analysis
      - Characterization & Validation
  - Interconnect Test & Link Analysis

- Physical Layer
  - Logical Sub-block
    - Electrical Sub-block
  - Data Link Layer
    - Digital Validation & Debug
  - Receiver Test
    - Compliance Testing

- Transaction Layer
High Speed Serial Interconnect: Loss
The faster the data rate and the longer the Interconnect, then the more loss in the signal.

- Clean, open, logical 1 & 0 at launch from transmitter
- Logical 1 & 0 can be hard to distinguish at end of long interconnects; (this is often called a "closed eye")
- Fast, sharp, edges at transmitter launch
- Smeared edges at end of long interconnect.
Receiver Performance measured with error rate

- Will the receiver work in real world conditions?
- What is the worst-case behavior?
- Send $1 \times 10^{12}$ bits and measure 1 bit error
  - $BER = \frac{1 \text{ error}}{1 \times 10^{12} \text{ bits}} = 1 \times 10^{-12}$
- Mean time between errors
  - Needs to be meaningful (acceptable target BER)
  - Measured vs. Estimated
- Direct measurement test time example (5Gb/s)
  - Target BER of $1 \times 10^{-6} = 200 \text{ useconds}$
  - Target BER of $1 \times 10^{-12} = 3.33 \text{ minutes}$
  - Target BER of $1 \times 10^{-15} = 2.31 \text{ days}$
Receiver Testing

- Limit, stress and compliance test your receiver design
- Stress your Receiver in absence of the transmitter and transmission lines
- Stress your receiver with a variety of limit stress and compliance test signals

- **Signal Generation**
  - Increasing data-rates for high speed serial data
  - Increasing bandwidth in RF

- **Replication of “Real-World” signals**
  - Replicate transmission effects
  - Generate signals including all noise, jitter and other imperfections
    - “known-good” and “known-bad” signals

*High Speed Serial Data*
In both design and manufacturing, requirements for receiver tests are standards-driven. All standards require Jitter Tolerance measurements for compliance.

### Types of devices tested:
- SerDes
- Transceivers
- Multi Media Sink devices
- Rx devices

#### Standards define the requirements

<table>
<thead>
<tr>
<th>Standard</th>
<th>Data Rate</th>
<th>Jitter Tolerance</th>
<th>Timing Skew</th>
<th>Amplitude Sensitivity</th>
<th>Emphasis</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA Gen 2</td>
<td>3 Gb/s</td>
<td>★</td>
<td>-</td>
<td>★</td>
<td>-</td>
</tr>
<tr>
<td>PCI Express 1.0</td>
<td>2.5 Gb/s</td>
<td>★</td>
<td>★</td>
<td>★</td>
<td>★</td>
</tr>
<tr>
<td>PCI Express 2.0</td>
<td>5 Gb/s</td>
<td>★</td>
<td>★</td>
<td>★</td>
<td>★</td>
</tr>
<tr>
<td>HDMI 1.3</td>
<td>0.75 Gb/s to 3.4 Gb/s</td>
<td>★</td>
<td>★</td>
<td>★</td>
<td>-</td>
</tr>
<tr>
<td>FC 4, 8 G</td>
<td>4.25 Gb/s to 8.5 Gb/s</td>
<td>★</td>
<td>★</td>
<td>★</td>
<td>★</td>
</tr>
<tr>
<td>DisplayPort</td>
<td>2.7 Gb/s</td>
<td>★</td>
<td>★</td>
<td>★</td>
<td>★</td>
</tr>
<tr>
<td>USB 3.0</td>
<td>5 Gb/s</td>
<td>★</td>
<td>-</td>
<td>★</td>
<td>★</td>
</tr>
</tbody>
</table>
Loopback

- External verification of compliance pattern used with Loopback technique
- Internal operation
  - Rx signal detected at decision circuit
  - Retimed (SKPs consumed/inserted) for compensation of clock differences
  - No error correction
- Internal error counter implementation becoming more common
  - DisplayPort
  - USB 3.0
Agenda

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  - Loopback

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  - Stress pattern library
  - Test configuration
  - Pattern generation and calibration
  - Frame error rate detection (Protocol aware method)

- Compliance Testing
  - MOIs, CTS,
  - Toolset

- Summary
4.1 Sink Jitter Tolerance Test (Normative)

4.1.1 Test Objective

The VESA DisplayPort Standard outlines a minimum Receiver Eye diagram which is measured at the receiver silicon component junction. This test is designed to provide an impaired stimulus which has been calibrated to the minimum TP3 connector electrical properties.

4.1.2 Interoperability Statement

This test will test the receiver ability to sustain a 10E-9 BER under most severe signaling conditions permitted by the specification.
Stressed Pattern Library: Putting it all together

Figure 4-4: Jitter Tolerance Testing Calibration Setup

Table 4-2: Jitter Component Settings for Reduced Rate

<table>
<thead>
<tr>
<th>f(Sj) [MHz]</th>
<th>Tj(JTRBRrx) [mUI]</th>
<th>ISI [mUI]</th>
<th>RJ(RMS) [mUI]</th>
<th>SJ [mUI]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1648</td>
<td>570</td>
<td>7.9</td>
<td>981</td>
</tr>
<tr>
<td>10</td>
<td>778</td>
<td>570</td>
<td>7.9</td>
<td>111</td>
</tr>
<tr>
<td>20</td>
<td>747</td>
<td>570</td>
<td>7.9</td>
<td>80</td>
</tr>
</tbody>
</table>
Traditional Receiver Test Configuration
Direct Synthesis for thorough Receiver Testing

Arbitrary Waveform Generator

Composite Stressed Pattern

DUT
Pattern generation and calibration

**AWG7122B (24GS/s)**

**DSA70804 (>8GHz, jitter calibration)**

Lane 2 Half clock pattern on adjacent lanes

Lane 1 Stressed Pattern applied on Lane under test

Lane 0 Half clock pattern on adjacent lanes

**ET-DP-TPA-P (Plug fixture)**
Serial Data Waveform Synthesis using SerialXpress®

Standard Base Patterns Selections
- SATA
- SAS
- HDMI
- DisplayPort
- PCIe
- Fiber Channel

Rise time setting

Graphic simulations of Compiled Data
Direct Synthesis - SerialXpress®

- Direct Synthesis of ISI

- Extract Mixed Mode S-Parameters from a reference impairment or model them mathematically.
- Feed the s4p file into SerialXpress®, and get an exact numerical model of that response in a full digital form.
- ISI Direct settable input feature.
- ISI Scaling feature that allows for virtual cable length adjustment (what-if scenarios)
Serial Data Jitter Generation using SerialXpress®

- Up to four SJ components with freq and phase settings
- Two Random jitter components with specific bandpass settings
SerialXpress® makes it easy

- Dial in specific amounts of ISI or import S-Parameter TouchStone files with patented ISI scaling capability
- SSC, Pre-emphasis and Noise can also be synthesized
SSC Modulation Deviation Requirements:
Started simple and rapidly became a dissertation problem

Typical “good” SSC profile acquired from a SATA device
SSC Modulation Deviation Requirements:
Of what value is a perfect SSC modulation in the area of stress testing?
Future test requirements

Parameterized SSC df/dt impairments, along with precision jitter impairments
Custom SSC
Built-In Self Test - Loopback Negotiation

BIST-L initiator sequence
10, 33 and 62MHz .45UI test vectors
Diagnostic test vectors
Frame Error Detection

- Clock skew management between host and device
- Requires Align primitives to not trigger error

<table>
<thead>
<tr>
<th>Serial Bus</th>
<th>Bit Error Detector</th>
<th>Internal Error Detector</th>
<th>Frame Error Detector</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express 2.0</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCI Express 3.0</td>
<td>X¹</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SATA Gen 2</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>SATA Gen 3</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>DisplayPort</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>USB 3.0</td>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>HDMI 1.3</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹ Estimate
Agenda

- High Speed Serial Test Challenges
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  - Focus on Receiver Testing
  - Error Rate as an indicator
  - Loopback

- Receiver Tolerance Testing
  - Stress Pattern Library
  - Pattern Generation and Calibration
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- Compliance Testing
  - Methods of Implementation
  - Toolset

- Summary
SATA: Receiver Signaling Group of tests or RSG Testing.

- The Serial ATA Consortium is the first standards body to mandate silicon level support features to facilitate Receiver Testing into it’s Gen-2 base specification.
- OEM’s such as Dell and HP require integrators list certification to enter their supply chain.
- **RSG testing is not optional.**
- Tektronix has been at the forefront of the receiver test initiatives, and has consistently been the first to review and first to gain certification of it’s test methods or MOI’s.
Tek RSG Method of Implementation

Serial ATA
International Organization

Version 1.0RC
January 17, 2008

Serial ATA Interoperability Program Revision 1.3
Tektronix MOI for RSG Tests
(Using AWG7102 and CHS Frame Error Analyzer)

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This material is provided for reference only. The Serial ATA International Organization does not endorse the vendor equipment outlined in this document.
Receiver Signal Group/Receiver Margin Testing

Select Device
- Cable
- Drive
- Host

Select Test Suite
- PHY-TSG-008
- RSG-RMT
- Rx-Tx

Version
- SATA Gen 2

Drive: RSG-RMT SATA Gen 2

Select
- RMT - Receiver Margin Test
- RSG-02 - Gen2 (3.0Gb/S) Receiver Signaling Group

Configure
- Show MDI
- Show Schematic
- Select All
- Select Required
- Deselect All
Receiver Signal Group/Receiver Margin Testing

The RSG/RMT product is broken into two different capabilities

1. **RSG tracks the SATA MOI Receiver Signaling Group MOI**
   - This configuration injects a SATA UTD 1.3 conformant set of four stressed signals into the device and monitors the error counter for an interval of 20 minutes. It automatically cycles through the four stressed signals (5, 10, 33 and 62 MHz), at the 20 minute points for an elapsed test time of roughly 1.5 Hours.

2. **RMT Receiver Margin Test.**
   - Successively apply a monotonically increasing impaired jitter profile from lower to increasing jitter magnitude and detect the point when the DUT starts to pass framing errors.
   - When Errors are detected, terminate the test at that frequency, and step to the next frequency in the test list.
### Receiver Signal Group/Receiver Margin Testing

#### Configuration for Drive: RSG-RMT SATA Gen 2

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Time Scope</td>
<td>DSA72004 ( GPIB0::01::INSTR )</td>
</tr>
<tr>
<td>Signal Source</td>
<td>AWG7102 ( GPIB0::04::INSTR )</td>
</tr>
<tr>
<td>RF Switch</td>
<td>MODEL SYSTEM 46 ( GPIB0::07::INSTR )</td>
</tr>
<tr>
<td>Frame Error Counter</td>
<td>CHS SATA-II Probe ( HostPC: USB )</td>
</tr>
<tr>
<td>BIST-L Initialization by</td>
<td>Auto</td>
</tr>
<tr>
<td>Set scope scale, resolution and sampling rate</td>
<td>Automatically</td>
</tr>
<tr>
<td>BIST-L validation required</td>
<td>First time only</td>
</tr>
<tr>
<td>Horizontal scale [us/div]</td>
<td>10</td>
</tr>
<tr>
<td>Resolution [ps/pt]</td>
<td>20</td>
</tr>
<tr>
<td>Verify Frame Error Counter operation</td>
<td>No</td>
</tr>
</tbody>
</table>

#### Configuration for RSG-02 - Gen2 (3.0Gb/S) Receiver Signaling Group

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>5MHz-0.45UI</td>
<td>Include</td>
</tr>
<tr>
<td>10MHz-0.45UI</td>
<td>Include</td>
</tr>
<tr>
<td>33MHz-0.45UI</td>
<td>Include</td>
</tr>
<tr>
<td>62MHz-0.45UI</td>
<td>Include</td>
</tr>
<tr>
<td>Test Duration for each frequency (Seconds)</td>
<td>900</td>
</tr>
</tbody>
</table>

#### Compliance Settings

- Compliance Mode
- User Defined Mode

[Buttons: Restore, Apply, Close]
## Receiver Signal Group/Receiver Margin Testing

### RSG/RMT Test Report

**UUT ID:** UUT001  
**Device Type:** Drive  
**Version:** SATA Gen 1  
**Overall Test Result:** PASS

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Freq (MHz)</th>
<th>Jitter (UI)</th>
<th>Frame Error Count</th>
<th>Frame Error Rate</th>
<th>Test Limits</th>
<th>Test Result</th>
<th>Compliance Mode</th>
<th>Test Execution Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSG-01 - Gen1 (1.5Gb/s) Receiver Signaling Group</td>
<td>16</td>
<td>0.43</td>
<td>0</td>
<td>0.00E+00</td>
<td>0 LE 0</td>
<td>Pass</td>
<td>No</td>
<td>2 Min</td>
</tr>
</tbody>
</table>
Receiver Signal Group/Receiver Margin Testing

The RSG/RMT product is broken into two different capabilities

1. **RSG tracks the SATA MOI Receiver Signaling Group MOI**
   - This configuration injects a SATA UTD 1.3 conformant set of four stressed signals into the device and monitors the error counter for an interval of 20 minutes. It automatically cycles through the four stressed signals (5, 10, 33 and 62 MHz), at the 20 minute points for an elapsed test time of roughly 1.5 Hours.

2. **RMT Receiver Margin Test.**
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   - When Errors are detected, terminate the test at that frequency, and step to the next frequency in the test list.
## Receiver Signal Group/Receiver Margin Testing

### Configuration for Drive: RSG-RMT SATA Gen 2

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Time Scope</td>
<td>DSA72004 (GPIB0::01::INSTR)</td>
</tr>
<tr>
<td>Signal Source</td>
<td>AWG7102 (GPIB0::04::INSTR)</td>
</tr>
<tr>
<td>RF Switch</td>
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<tr>
<td>Frame Error Counter</td>
<td>CHS SATA-2I Probe (HostPC: USB)</td>
</tr>
<tr>
<td>BIST-L Initialization by</td>
<td>Auto</td>
</tr>
<tr>
<td>Set scope scale, resolution and sampling rate</td>
<td>Automatically</td>
</tr>
<tr>
<td>BIST-L validation required</td>
<td>First time only</td>
</tr>
<tr>
<td>Horizontal scale (us/div)</td>
<td>10</td>
</tr>
<tr>
<td>Resolution (ps/pt)</td>
<td>20</td>
</tr>
<tr>
<td>Verify Frame Error Counter operation</td>
<td>No</td>
</tr>
<tr>
<td>RMT input (IDC1) connected to RF Switch</td>
<td>Rethread</td>
</tr>
</tbody>
</table>

### Configuration for RMT - Receiver Margin Test

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start Frequency (MHz)</td>
<td>1</td>
</tr>
<tr>
<td>End Frequency (MHz)</td>
<td>100</td>
</tr>
<tr>
<td>Incremental Step Frequency (MHz)</td>
<td>1</td>
</tr>
<tr>
<td>Start UI Jitter (UI)</td>
<td>0.1</td>
</tr>
<tr>
<td>End UI Jitter (UI)</td>
<td>1.9</td>
</tr>
<tr>
<td>Incremental Step Jitter (UI)</td>
<td>0.01</td>
</tr>
</tbody>
</table>

**Compliance Settings**

- [ ] Compliance Mode
- [ ] User Defined Mode

[Restore] [Apply] [Close]
Receiver Margin Testing Jitter Tolerance Curve

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Test Details</th>
<th>Frame Error Rate</th>
<th>Test Limits</th>
<th>Test result</th>
<th>Compliance Mode</th>
<th>Ana Execute</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMT - Receiver Margin Test</td>
<td>Freq (MHz) 10 Jitter (UI) 0.7 Measured Jitter 0.6811056245 Frame Error Rate 1.51E-03 Test Limits OLE 0</td>
<td></td>
<td></td>
<td>Fail</td>
<td>Yes</td>
<td>Days 16</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>1.1</td>
<td>0.898668584</td>
<td>3.36E-03</td>
<td>OLE 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>1</td>
<td>0.892778842</td>
<td>2.26E-03</td>
<td>OLE 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>1.1</td>
<td>0.871977738</td>
<td>1.19E-03</td>
<td>OLE 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>0.8</td>
<td>0.795123014</td>
<td>1.31E-03</td>
<td>OLE 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>35</td>
<td>1</td>
<td>0.811201117</td>
<td>1.23E-03</td>
<td>OLE 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>1.1</td>
<td>0.793772344</td>
<td>1.32E-03</td>
<td>OLE 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>45</td>
<td>1</td>
<td>0.792910261</td>
<td>1.32E-03</td>
<td>OLE 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>1.1</td>
<td>0.846523323</td>
<td>3.89E-03</td>
<td>OLE 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>55</td>
<td>1.1</td>
<td>0.8536600335</td>
<td>2.39E-03</td>
<td>OLE 0</td>
<td></td>
</tr>
</tbody>
</table>

RMT - Receiver Margin Test

![Graph showing measured jitter over frequency](image-url)
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  - System Integration
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  - transmitter Test
    - Eye and Jitter Analysis
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- Verification
  - Data Link Analysis
    - Digital validation & Debug
  - Receiver Test
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- Compliance Test
  - Interconnect Test & Link Analysis

Diagram:
- Tx + path + Rx
- Physical Sub-block: Logical Sub-block
- Simulation
  - Logical Sub-block: Electrical Sub-block

10/17/2008
Summary

- AWG7000B is a one box solution for high performance complex jitter generation

- SerialXpress® advanced jitter generation software is a powerful, easy to use to synthesize high speed serial patterns for Rx testing

- TekExpress® RSG/RMT provides a comprehensive automation system to greatly simplify the receiver test’s required by the SATA –IO.
  - Automatic Frame Error detector and instrument interaction.
  - AWG Digital setups fully encapsulate the Jitter profile with no external SSC, ISI, SJ generators.

- Provisions to share and propagate setups electronically is a revolutionary step forward in the receiver test industry.