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Establishing a PCIe® Reference Mask Using a TMT4 Margin Tester

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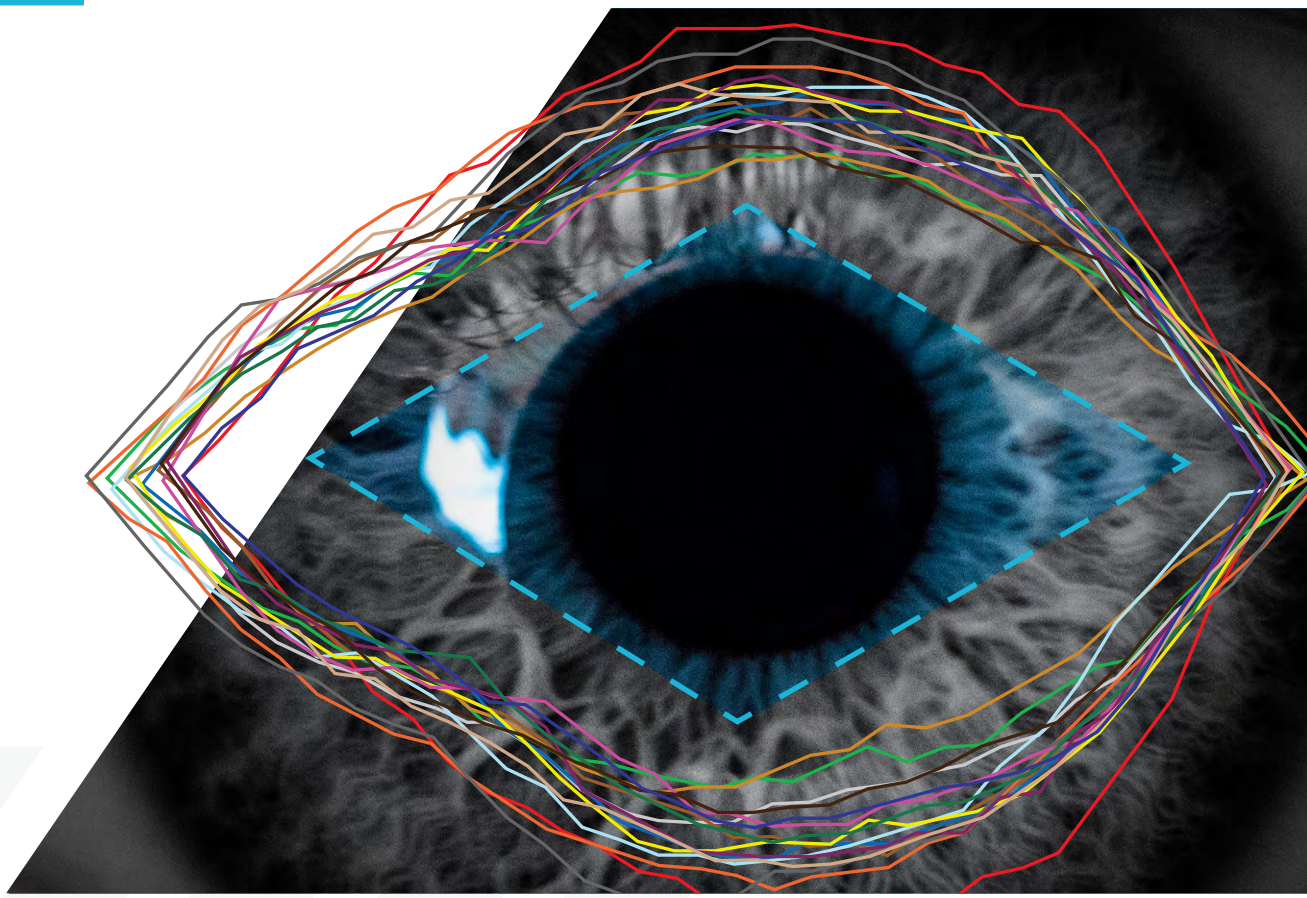
WHITE PAPER



Introduction

With the introduction of the TMT4 Margin Tester for PCIe® link health testing, the question arises as to what the "best mask" is to determine pass or fail of a device under test (DUT). Should the standard PCIe compliance mask be used? Is there a consistent mask that can be used across all types of PCIe DUTs? And if not, how should one assess whether the results from their testing qualify their DUT as "good"? The aim of this whitepaper is to help address how to think about the pass/fail mask feature available in the TMT4 Margin Tester's custom scan, and what to consider when determining which pass/fail limits are best for a given DUT.

Evaluation of Link Health with Tx and Rx Testing

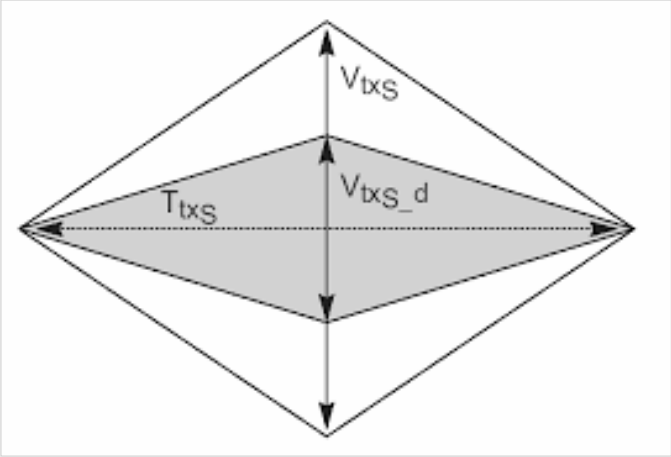
After link training, a PCIe device under test may go through additional link equalization processes to establish stable connection among the devices. Link equalization is a link optimization process that modifies the characteristics of the transmitted data waveform so that it results in the most stable PCIe link at a higher data rate. Link equalization is achieved by using the preset values defined in PCIe specification. Preset values are configurations that can modify the characteristics of the transmitted data wave form.

The Tektronix TMT4 allows users to quickly assess the link health of their PCIe generation 3 and 4 designs in minutes. The instrument acts as an active link partner with the device under test (DUT) and enables users to control presets via protocol and quickly display eye diagrams with their associated link training parameters, providing insights into potential design flaws on a lane-by-lane or preset-by-preset basis.

TMT4 testing includes both the Tx and the Rx of a given DUT and may be conducted by either using all the available lanes and presets detected during link training, or by selecting specific lanes or presets of interest. There are two test modes available in the TMT4: Quick Scan and Custom Scan. In Quick Scan mode, the TMT4 will evaluate the DUT link health by automatically selecting the best preset per each available lane with the purpose of optimizing test time and lane performance, whereas Custom Scan evaluates specifically chosen lanes and presets.

What Considerations Are There with TMT4 Custom Scan Masks?

There are several considerations when determining a pass/fail mask for TMT4 Custom Scans. The most notable is that the method of test using TMT4 is quite different than traditional compliance testing. While compliance testing uses mathematically modeled reference receivers and test signals, the TMT4 Margin Tester uses real receivers and real link traffic. This means that the mask specified for use in the PCIe spec for compliance testing is not necessarily a good mask to use when evaluating DUT health using TMT4.



Generalized PCI Express® (PCIe) Compliance Receiver Mask

Additionally, since the TMT4 is a part of the link with the DUT, the contribution to the overall eye is a combination of the DUT *and* the TMT4 as they form a link together. This means that while one mask may be a good fit for one DUT when paired with a TMT4, it may not be the best mask for a different DUT, which has trained differently with a different transceiver.

Since one mask cannot necessarily be used for all possible DUTs, the best reference point then is to assess a distribution of commercially available DUTs who have all passed compliance testing and see where any given DUT falls on the distribution. From there, the team or organization can determine whether they want their pass/fail mask to be the 10th percentile of commercially available DUTs, the 50th percentile, or even the 95th percentile. Using a reference mask from a large data set gives organizations a jump off point in determining their pass/fail mask, as opposed to a strict mask that every DUT should be compared to as is done in the PCIe specification for compliance testing.

Reference Mask Data Collection and Analysis

To create distributions across presets and assess the percentile of a given DUT's performance, a significant data collection effort was undertaken. Tektronix purchased a large sample size of commercially available DUTs, even using some TMT4 units as DUTs, to gather a data set consisting of >50 total combinations of commercially available PCIe Gen 3 and Gen 4 devices[1].

Each combination was tested using the TMT4's custom scan feature. Custom scans enable users to force specific test parameters for a more thorough evaluation of their Tx signal paths. Both the Tx eye diagram and the link training parameter table results can be configured to view the results by lanes tested or by presets tested.

Here, the devices varied from 4 lanes wide (40 eyes/device) up to 16 lanes wide (160 eyes/device), including both Root Complex and Endpoint devices.

This pool consisted of SSDs of varying connector types, motherboards with varying chipsets, graphics cards from varying vendors, network cards, and other PCIe devices to ensure a wide distribution of connector, device type, and chipset.

This data collection effort resulted in roughly 100,000 eye diagrams to be used in developing reference distributions for establishing pass/fail eye masks. A tabular view of the percentile by preset for Gen 3 and Gen 4 eye height and eye width follows, while the group distribution charts and individual distribution charts can be found in the appendix.

Establishing a PCIe® Reference Mask Using a TMT4 Margin Tester – All Devices

Gen 4 EH (mV)	5%	10%	25%	50%	75%	90%	95%
P0	55	65	75	90	100	110	115
P1	65	75	85	95	105	115	125
P2	60	70	85	95	105	115	125
P3	65	75	85	100	110	125	130
P4	60	70	85	100	110	125	130
P5	80	90	105	120	135	145	155
P6	85	95	110	125	140	150	160
P7	80	95	105	115	130	140	150
P8	90	100	115	125	140	150	160
P9	90	100	110	125	140	150	160

Gen 4 EW (ps)	5%	10%	25%	50%	75%	90%	95%
P0	15	17	20	23	26	28	29
P1	18	20	23	25	27	29	31
P2	18	20	22	24	26	28	30
P3	19	22	24	26	28	30	32
P4	21	24	27	29	32	33	34
P5	24	27	29	31	33	34	35
P6	23	26	28	30	32	33	34
P7	20	22	24	26	28	29	31
P8	22	23	25	27	29	31	32
P9	22	24	26	28	30	31	32

Gen 3 EH (mV)	5%	10%	25%	50%	75%	90%	95%
P0	150	155	165	180	190	205	210
P1	150	155	165	180	190	200	210
P2	150	155	165	180	190	200	210
P3	150	155	165	180	190	205	210
P4	150	160	170	180	190	205	215
P5	150	155	165	180	195	205	210
P6	145	150	160	175	185	200	210
P7	150	155	165	175	190	200	210
P8	140	145	155	170	180	190	200
P9	130	135	145	160	170	180	190

Gen 3 EW (ps)	5%	10%	25%	50%	75%	90%	95%
P0	77	79	81	83	86	88	89
P1	81	82	84	86	88	90	92
P2	80	81	83	85	87	90	91
P3	81	83	85	87	89	92	93
P4	84	86	88	91	94	96	97
P5	82	83	85	87	89	92	93
P6	80	81	83	85	87	89	90
P7	76	77	79	81	83	85	86
P8	76	77	79	82	83	85	86
P9	75	77	79	81	84	86	87

[1] **PCIe Gen3 vs Gen4.** With Gen4 the data rate increased by 2x from 8 GT/s for Gen3 to 16 GT/s for Gen4. The Gen4 16 GT/s data rate uses scrambling, the same as Gen3's 8 GT/s, with no encoding change from Gen3 (128b/130b). The minimum eye height for Gen4 was reduced to 15 mVpp.

PCIe Gen 3 and Gen 4 Percentile of Eye Height and Eye Width Measurements – AICs[2] Only

Gen 4 EH (mV)	5%	10%	25%	50%	75%	90%	95%
P0	70	75	80	90	105	115	125
P1	80	85	90	100	115	125	130
P2	75	80	85	100	110	120	130
P3	80	85	95	105	115	125	130
P4	85	90	95	105	115	125	130
P5	100	105	115	125	135	145	150
P6	105	110	120	130	140	155	160
P7	100	105	115	125	140	150	155
P8	105	115	125	140	150	160	165
P9	110	115	125	135	145	155	160

Gen 4 EW (ps)	5%	10%	25%	50%	75%	90%	95%
P0	17	18	20	22	25	27	28
P1	21	22	25	25	28	31	32
P2	19	20	22	24	27	30	31
P3	23	24	25	27	30	32	34
P4	28	29	31	32	34	35	36
P5	30	31	32	33	35	36	37
P6	28	29	30	32	33	35	36
P7	22	23	24	26	28	31	33
P8	24	25	26	28	30	33	34
P9	27	28	29	30	32	33	34

Gen 3 EH (mV)	5%	10%	25%	50%	75%	90%	95%
P0	150	155	165	175	190	200	205
P1	150	155	165	175	190	200	210
P2	150	155	165	175	190	200	205
P3	145	155	165	175	190	200	210
P4	150	155	165	175	190	200	210
P5	150	155	165	180	195	205	210
P6	145	150	160	175	185	200	205
P7	145	150	160	175	190	200	210
P8	135	140	155	165	175	185	195
P9	140	145	155	165	180	190	195

Gen 3 EW (ps)	5%	10%	25%	50%	75%	90%	95%
P0	77	79	81	84	87	89	90
P1	81	82	84	86	88	90	91
P2	79	81	82	84	86	88	89
P3	82	83	85	87	89	91	93
P4	86	88	89	92	95	97	98
P5	83	84	86	88	90	92	94
P6	81	82	84	86	88	90	91
P7	75	77	78	80	82	84	85
P8	76	77	79	82	84	85	86
P9	78	79	81	83	85	87	88

PCIe Gen 3 and Gen 4 Percentile of Eye Height and Eye Width Measurements – MBs[3] Only

Gen 4 EH (mV)	5%	10%	25%	50%	75%	90%	95%
P0	50	55	80	95	105	115	120
P1	55	65	85	100	110	120	125
P2	55	65	85	95	105	120	125
P3	55	65	90	100	110	125	130
P4	60	70	90	105	120	130	135
P5	80	90	110	125	140	155	160
P6	85	95	115	130	145	160	165
P7	70	80	105	120	130	140	145
P8	80	90	115	130	140	155	160
P9	85	100	120	130	145	155	165

Gen 4 EW (ps)	5%	10%	25%	50%	75%	90%	95%
P0	13	15	22	25	27	29	30
P1	17	19	21	23	25	27	28
P2	16	18	21	23	25	28	29
P3	15	18	22	25	26	28	29
P4	17	21	26	28	31	32	34
P5	22	24	27	29	31	33	34
P6	22	23	27	28	30	32	33
P7	19	20	23	26	28	29	30
P8	21	22	23	25	26	27	28
P9	20	22	25	27	29	30	31

Gen 3 EH (mV)	5%	10%	25%	50%	75%	90%	95%
P0	155	160	170	185	200	210	220
P1	155	160	170	180	195	205	215
P2	155	160	170	185	195	205	215
P3	155	165	170	185	195	210	215
P4	150	155	165	175	190	200	210
P5	150	155	165	175	190	200	210
P6	140	145	155	165	180	190	200
P7	150	160	165	180	190	205	215
P8	135	140	150	165	180	190	200
P9	125	130	140	150	165	180	185

Gen 3 EW (ps)	5%	10%	25%	50%	75%	90%	95%
P0	78	79	81	84	86	88	89
P1	80	82	84	86	89	91	93
P2	80	82	84	86	89	91	92
P3	80	82	84	86	89	91	92
P4	83	85	87	90	93	95	96
P5	81	82	85	87	90	92	93
P6	79	80	83	85	87	89	90
P7	76	77	79	82	84	85	86
P8	75	76	79	81	83	85	86
P9	75	77	79	82	84	86	87

Using the data collected above, users of TMT4 can evaluate how their device performs relative to a large data set of commercially available DUTs, and organizations can establish a rough percentile threshold as a pass/fail limit based on how they want their DUT to perform relative to other commercially available PCIe devices. While TMT4 does not offer a different mask setting by preset, a single mask could be used considering the strictest eye height or eye width by percentile. For example, if Company A wanted to establish the 50th percentile of all devices as their pass/fail for Gen 3 and Gen 4, their masks could be as follows:

Gen 4	Min Eye Height	125 mV
	Min Eye Width	31 ps
Gen 3	Min Eye Height	180 mV
	Min Eye Width	91 ps

While these thresholds may see failures at certain presets since the strictest limits were used, it still establishes a consistent pass/fail mask for the company to use based on reference distributions from commercially available devices.

[2] Add In Card/Endpoint.

[3] Motherboard or System Board/Root Complex.

Likewise, if instead a company is curious to plot where their device sits relative to these reference distributions, that could be done as well. Exported test data from a TMT4 could be used to see where a given device falls relative to a large population of devices today as simply a pulse on performance, as opposed to a true pass/fail limit. Here is an example using random data:

Gen 4 Eye Height	Smallest Eye Height Across Lanes	Estimated Percentile
P0	98	75th
P1	102	75th
P2	96	50th
P3	105	60th
P4	111	75th
P5	115	40th
P6	138	75th
P7	141	90th
P8	137	75th
P9	130	60th

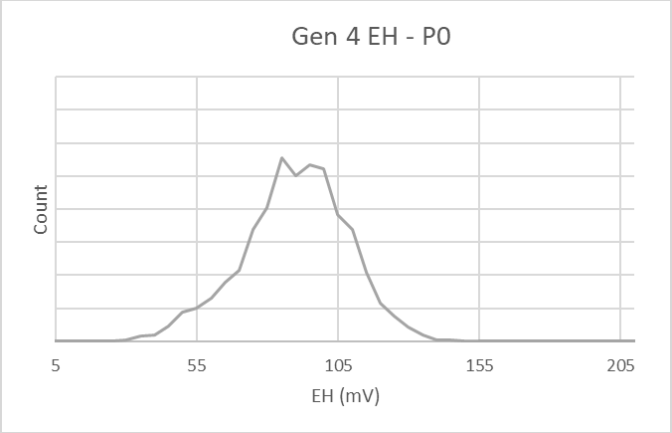
Conclusion

While a single universal mask does not align with the test methodology of TMT4, using reference masks based on a distribution of commercially available PCIe DUTs is a method of establishing a reasonable pass/fail mask for a given DUT. Using the distribution charts available in this paper, users of TMT4 can develop reference masks that are meaningful in assessing the health of their device relative to what is commercially available today.

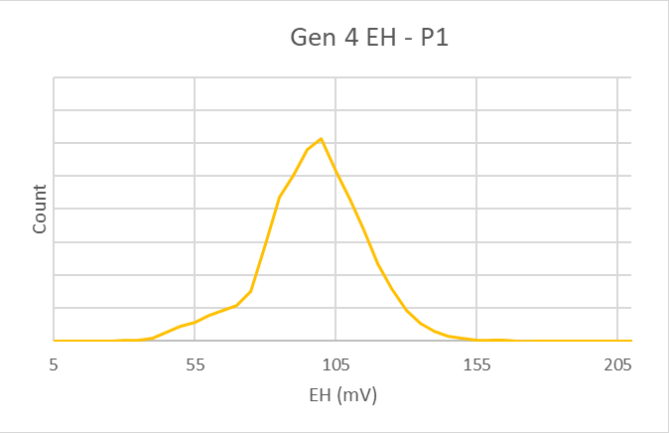
To further validate your PCIe design or to test for compliance using the standard compliance mask, be sure to visit us online and learn more about our entire portfolio of PCIe test solutions.

APPENDIX

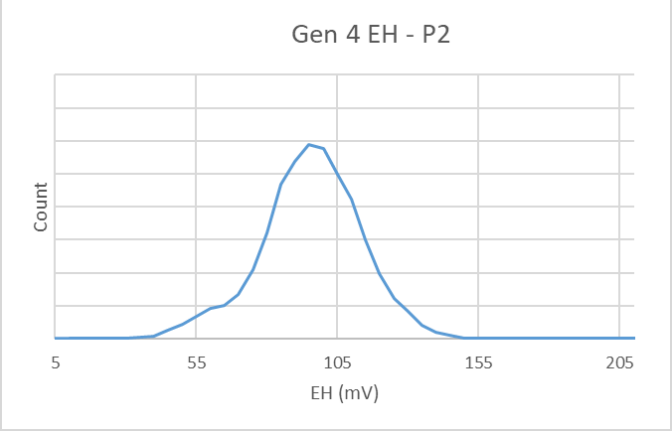
PCIe Gen 4 DUT Eye Height Distribution by Preset with TMT4 – All Devices



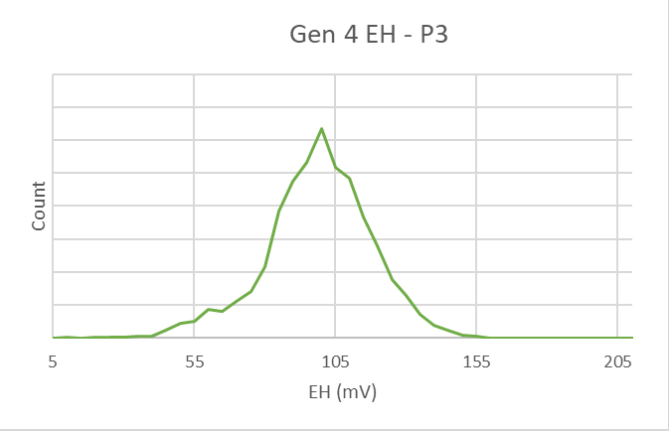
Distribution by PCIe Preset 0 for Gen 4 Eye Height across all devices tested.



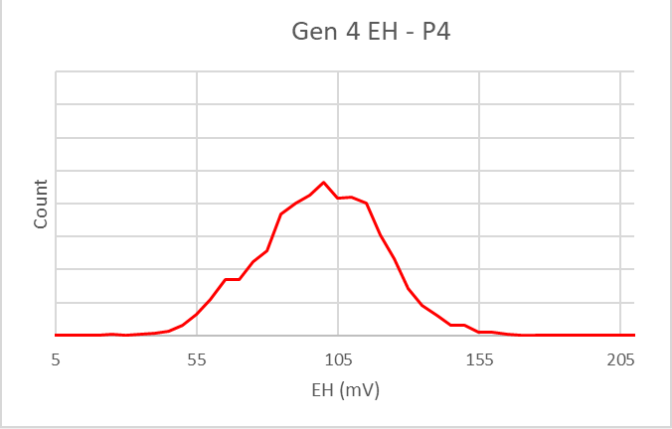
Distribution by PCIe Preset 1 for Gen 4 Eye Height across all devices tested.



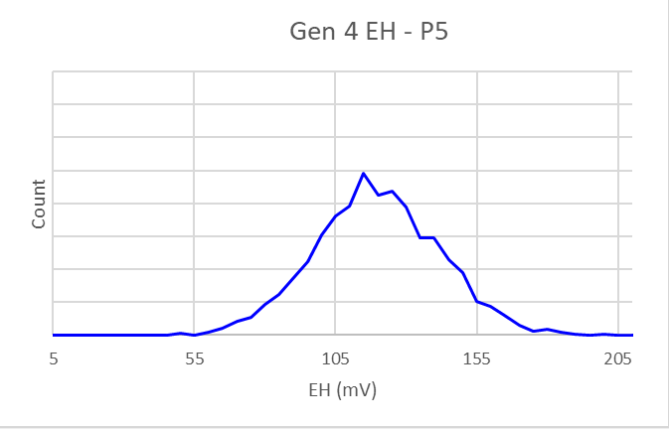
Distribution by PCIe Preset 2 for Gen 4 Eye Height across all devices tested.



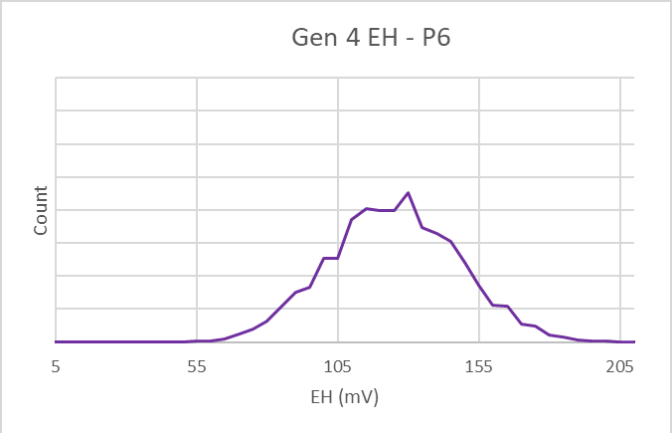
Distribution by PCIe Preset 3 for Gen 4 Eye Height across all devices tested.



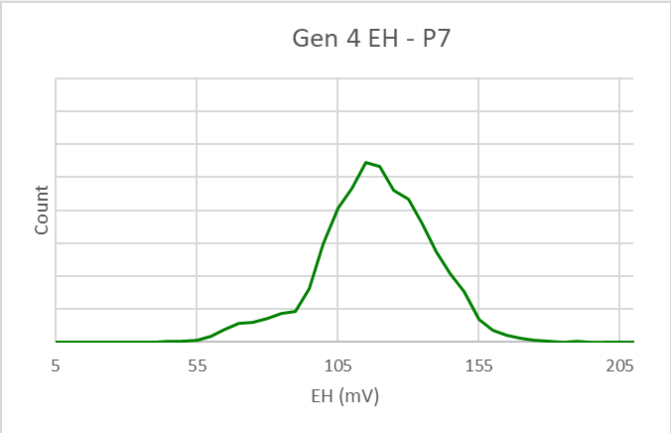
Distribution by PCIe Preset 4 for Gen 4 Eye Height across all devices tested.



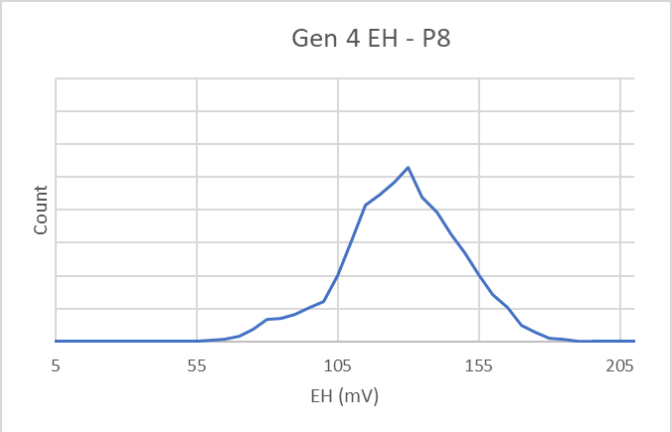
Distribution by PCIe Preset 5 for Gen 4 Eye Height across all devices tested.



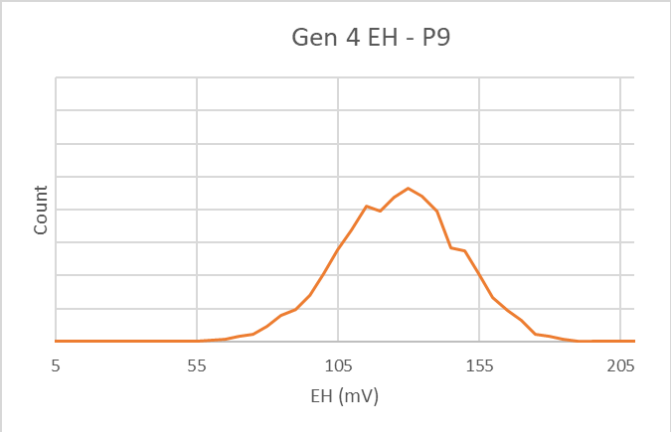
Distribution by PCIe Preset 6 for Gen 4 Eye Height across all devices tested.



Distribution by PCIe Preset 7 for Gen 4 Eye Height across all devices tested.

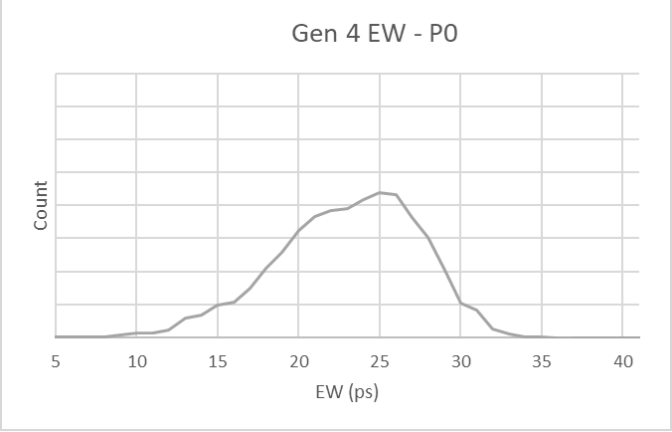


Distribution by PCIe Preset 8 for Gen 4 Eye Height across all devices tested.

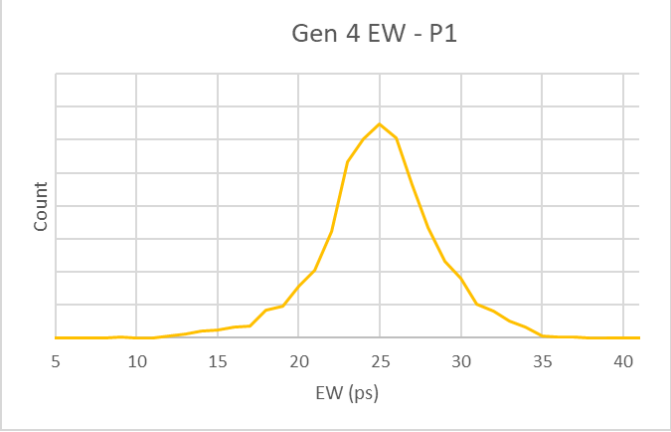


Distribution by PCIe Preset 9 for Gen 4 Eye Height across all devices tested.

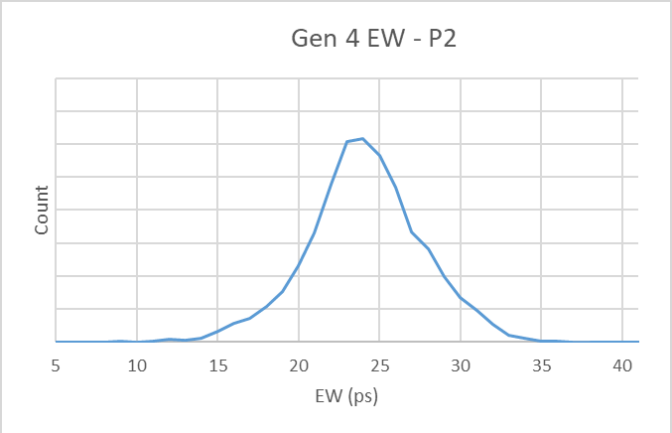
PCIe Gen 4 DUT Eye Width Distribution by Preset with TMT4 – All Devices



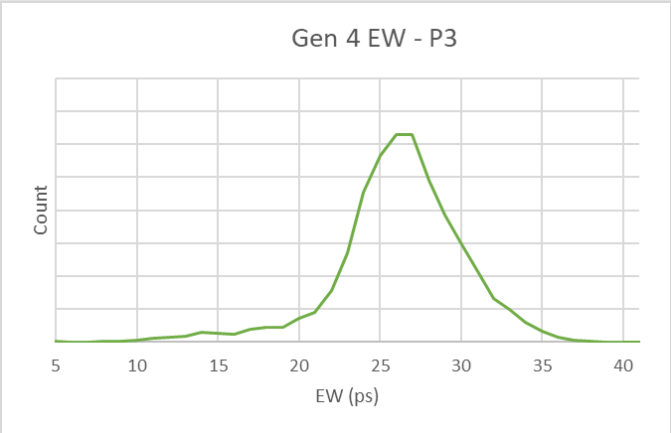
Distribution by PCIe Preset 0 for Gen 4 Eye Width across all devices tested.



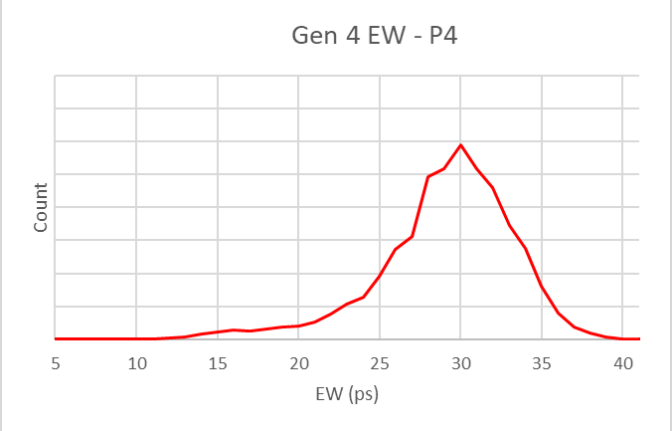
Distribution by PCIe Preset 1 for Gen 4 Eye Width across all devices tested.



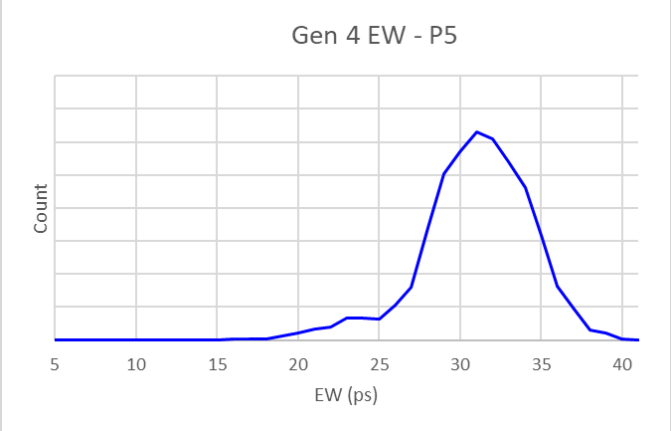
Distribution by PCIe Preset 2 for Gen 4 Eye Width across all devices tested.



Distribution by PCIe Preset 3 for Gen 4 Eye Width across all devices tested.

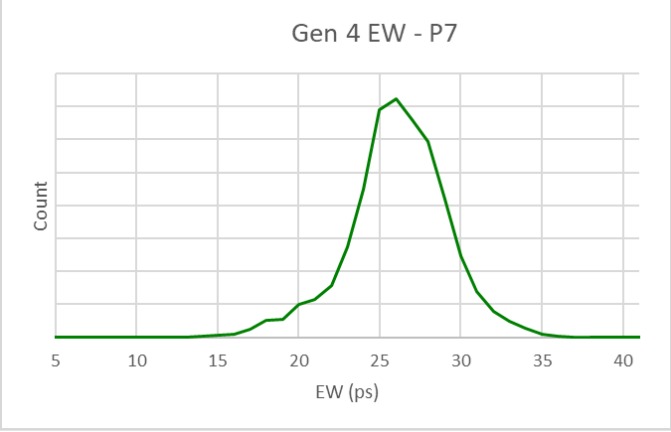


Distribution by PCIe Preset 4 for Gen 4 Eye Width across all devices tested.

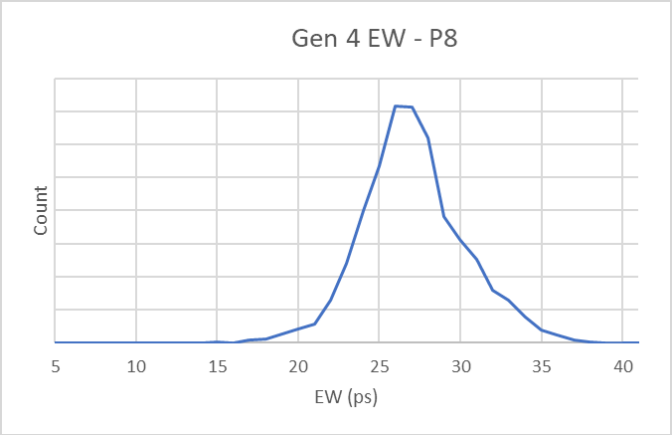


Distribution by PCIe Preset 5 for Gen 4 Eye Width across all devices tested.

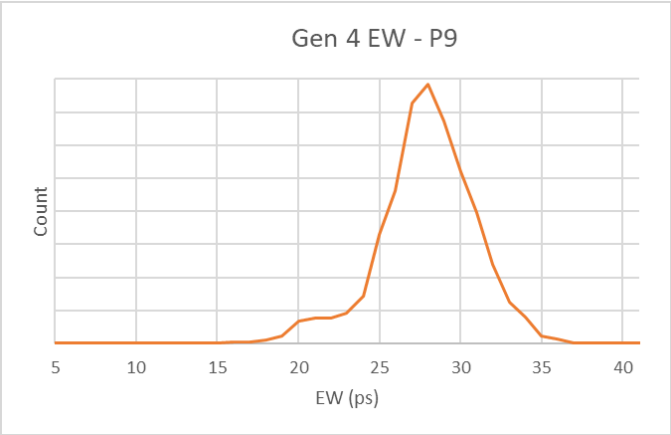
Distribution by PCIe Preset 6 for Gen 4 Eye Width across all devices tested.



Distribution by PCIe Preset 7 for Gen 4 Eye Width across all devices tested.

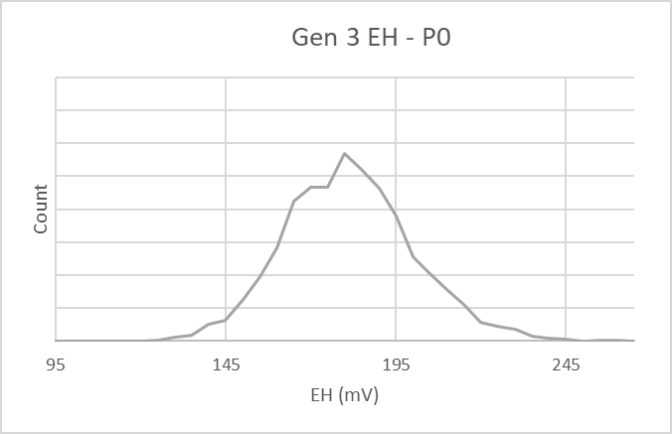


Distribution by PCIe Preset 8 for Gen 4 Eye Width across all devices tested.

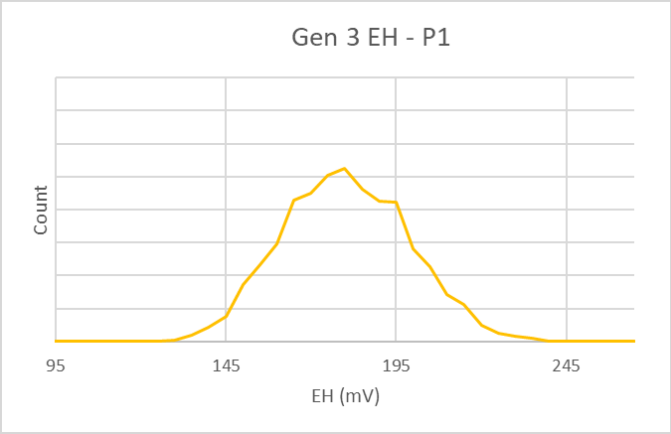


Distribution by PCIe Preset 9 for Gen 4 Eye Width across all devices tested.

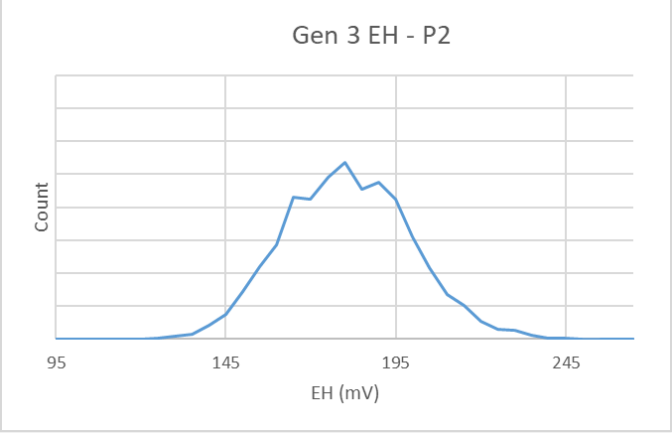
PCIe Gen 3 DUT Eye Height Distribution by Preset with TMT4 – All Devices



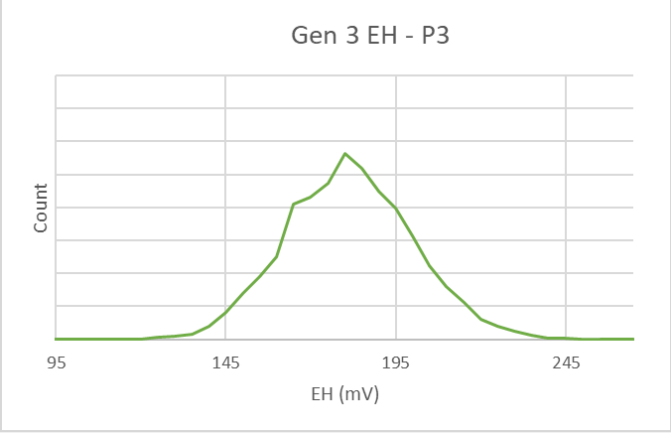
Distribution by PCIe Preset 0 for Gen 3 Eye Height across all devices tested.



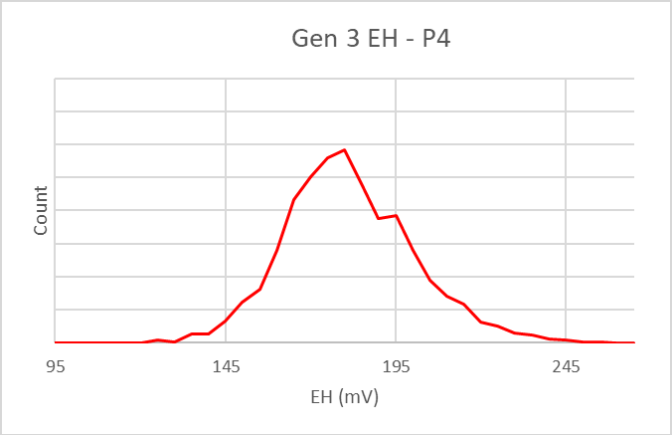
Distribution by PCIe Preset 1 for Gen 3 Eye Height across all devices tested.



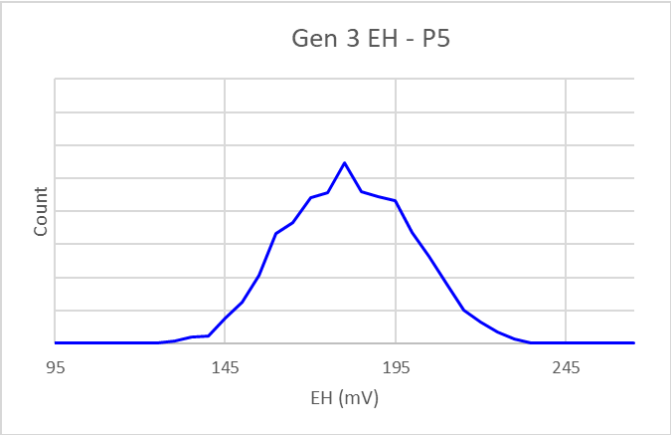
Distribution by PCIe Preset 2 for Gen 3 Eye Height across all devices tested.



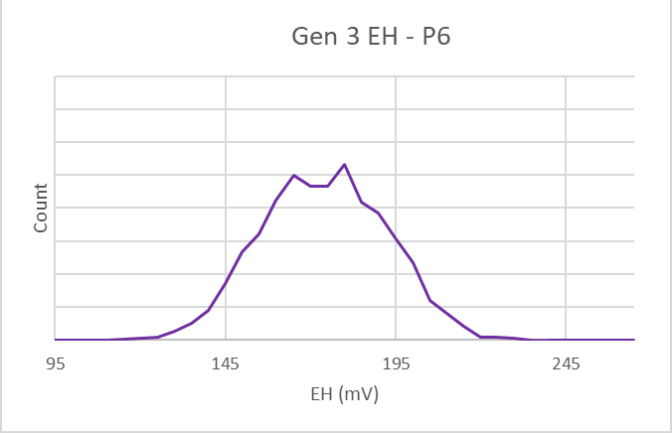
Distribution by PCIe Preset 3 for Gen 3 Eye Height across all devices tested.



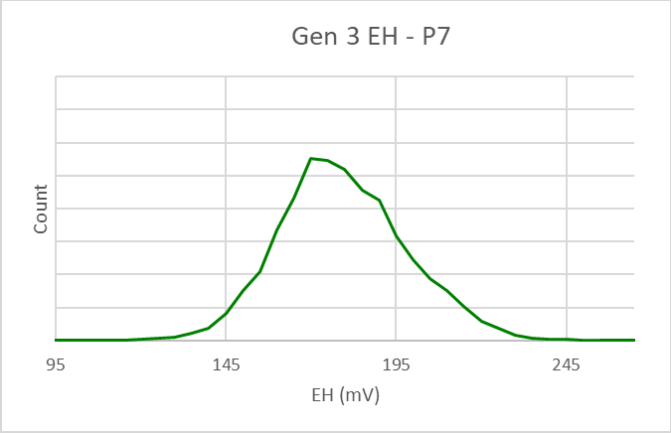
Distribution by PCIe Preset 4 for Gen 3 Eye Height across all devices tested.



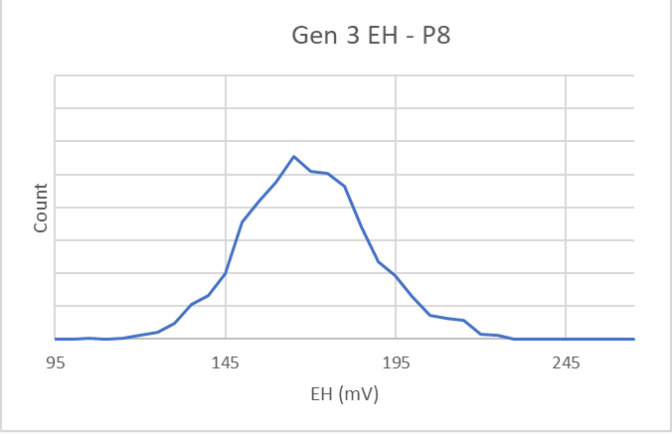
Distribution by PCIe Preset 5 for Gen 3 Eye Height across all devices tested.



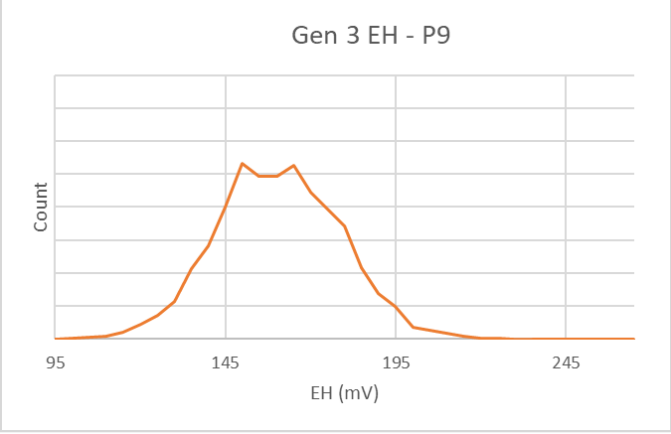
Distribution by PCIe Preset 6 for Gen 3 Eye Height across all devices tested.



Distribution by PCIe Preset 7 for Gen 3 Eye Height across all devices tested.

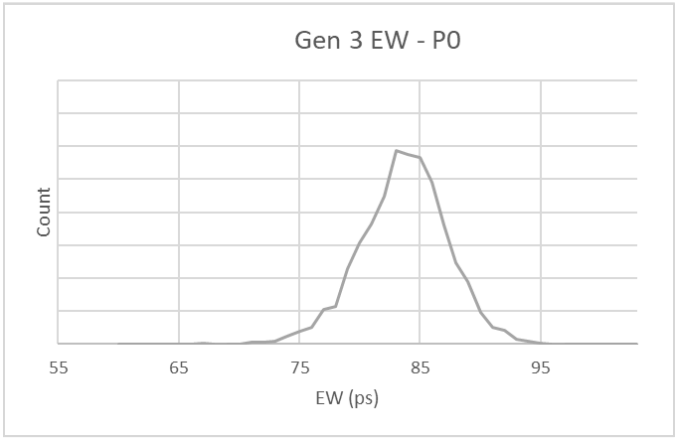


Distribution by PCIe Preset 8 for Gen 3 Eye Height across all devices tested.

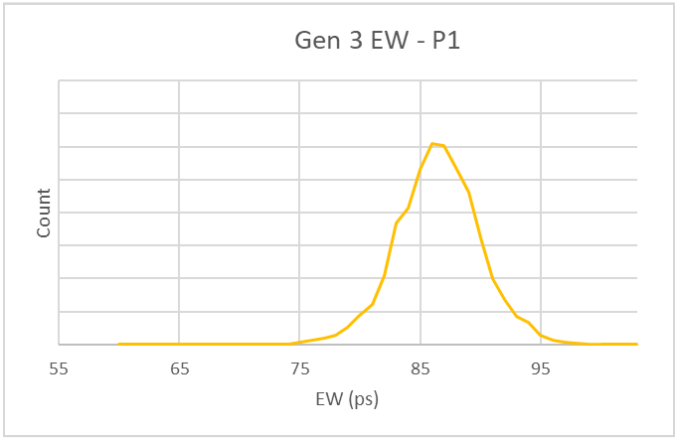


Distribution by PCIe Preset 9 for Gen 3 Eye Height across all devices tested.

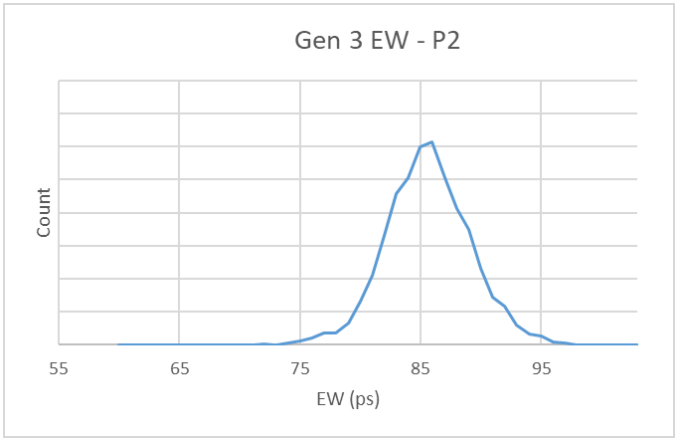
PCIe Gen 3 DUT Eye Width Distribution by Preset with TMT4 – All Devices



Distribution by PCIe Preset 0 for Gen 3 Eye Width across all devices tested.

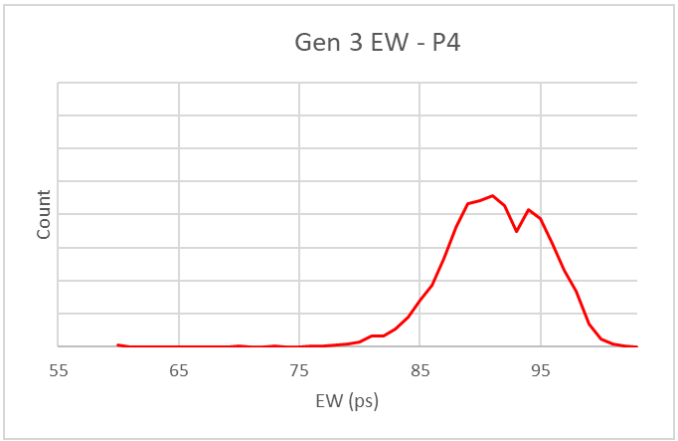


Distribution by PCIe Preset 1 for Gen 3 Eye Width across all devices tested.

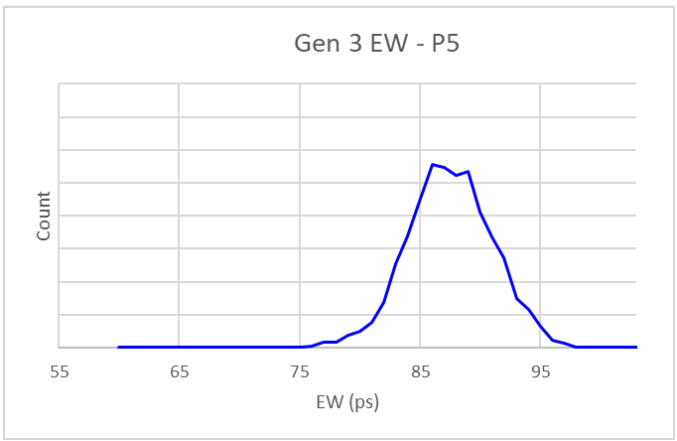


Distribution by PCIe Preset 2 for Gen 3 Eye Width across all devices tested.

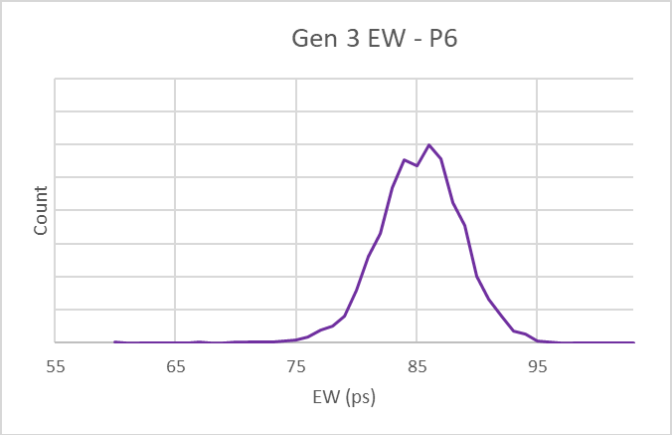
Distribution by PCIe Preset 3 for Gen 3 Eye Width across all devices tested.



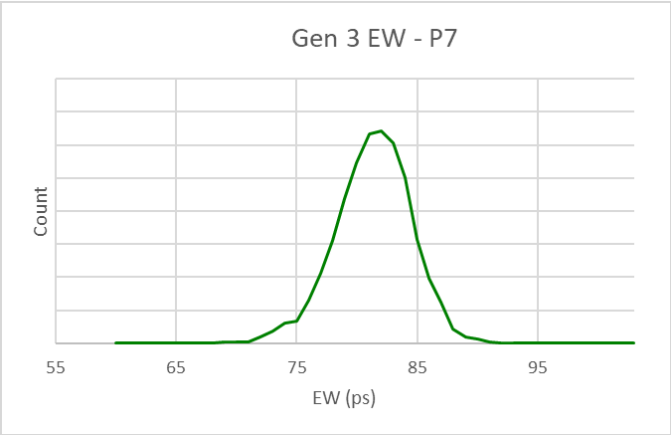
Distribution by PCIe Preset 4 for Gen 3 Eye Width across all devices tested.



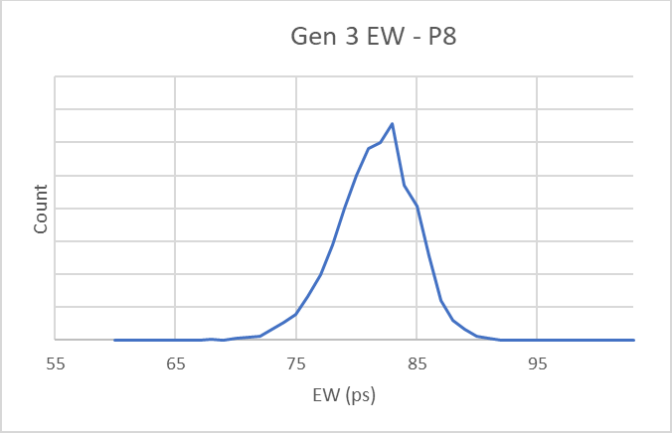
Distribution by PCIe Preset 5 for Gen 3 Eye Width across all devices tested.



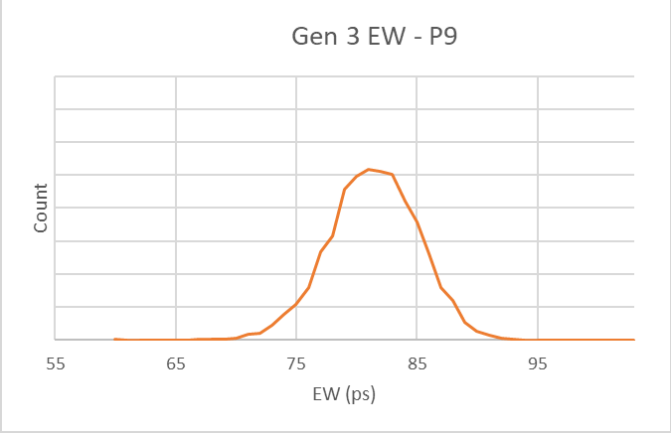
Distribution by PCIe Preset 6 for Gen 3 Eye Width across all devices tested.



Distribution by PCIe Preset 7 for Gen 3 Eye Width across all devices tested.

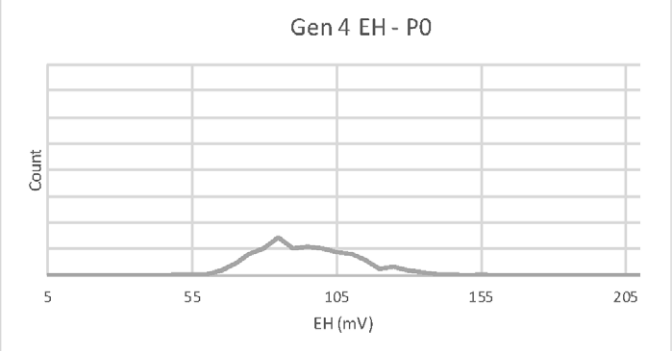


Distribution by PCIe Preset 8 for Gen 3 Eye Width across all devices tested.

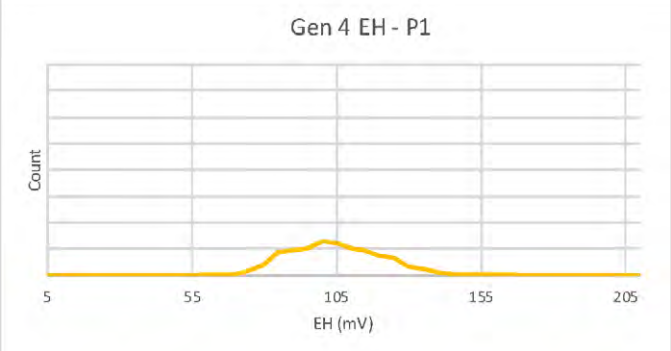


Distribution by PCIe Preset 9 for Gen 3 Eye Width across all devices tested.

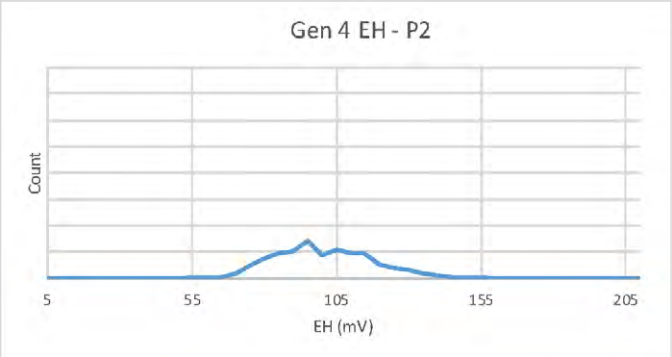
PCIe Gen 4 DUT Eye Height Distribution by Preset with TMT4 – AICs Only



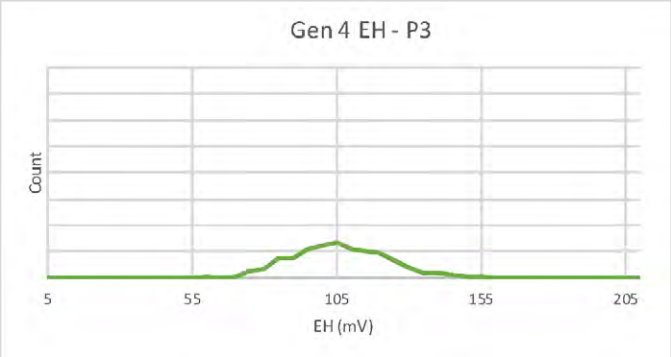
Distribution by PCIe Preset 0 for Gen 4 Eye Height – AICs Only.



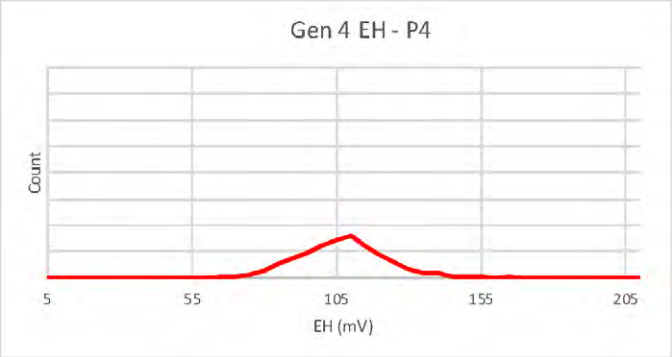
Distribution by PCIe Preset 1 for Gen 4 Eye Height – AICs Only.



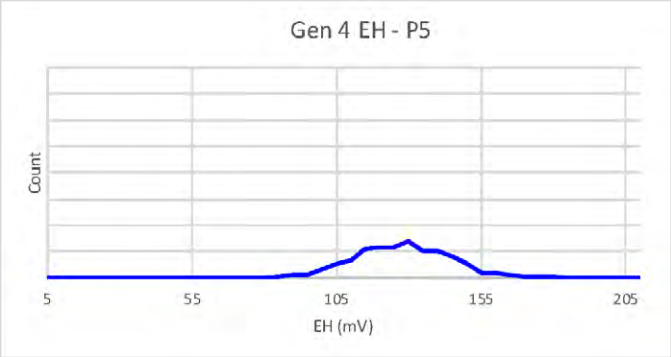
Distribution by PCIe Preset 2 for Gen 4 Eye Height – AICs Only.



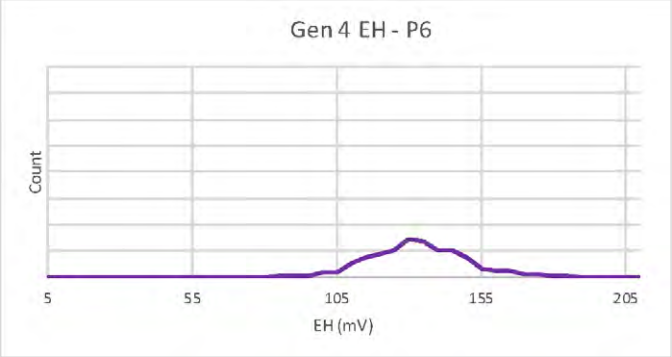
Distribution by PCIe Preset 3 for Gen 4 Eye Height – AICs Only.



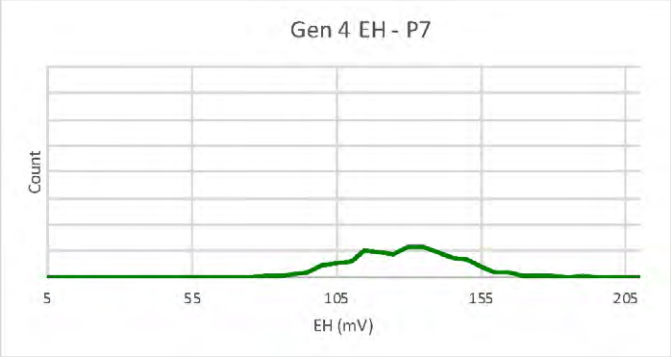
Distribution by PCIe Preset 4 for Gen 4 Eye Height – AICs Only.



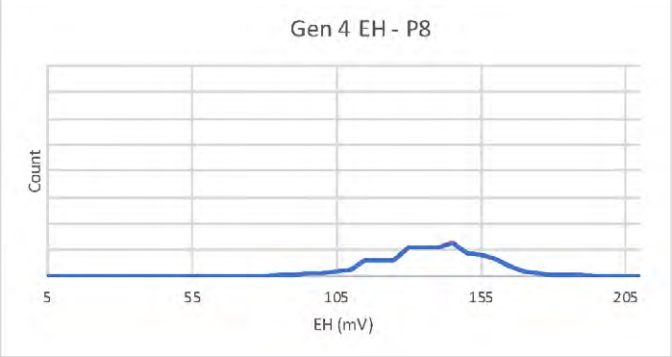
Distribution by PCIe Preset 5 for Gen 4 Eye Height – AICs Only.



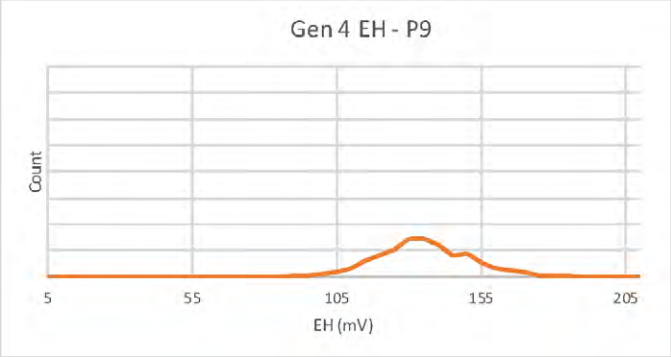
Distribution by PCIe Preset 6 for Gen 4 Eye Height – AICs Only.



Distribution by PCIe Preset 7 for Gen 4 Eye Height – AICs Only.

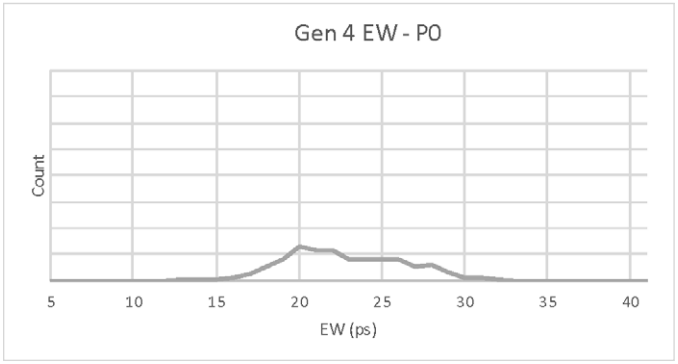


Distribution by PCIe Preset 8 for Gen 4 Eye Height – AICs Only.

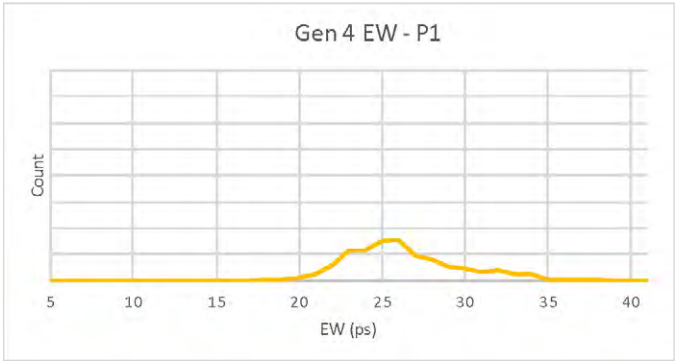


Distribution by PCIe Preset 9 for Gen 4 Eye Height – AICs Only.

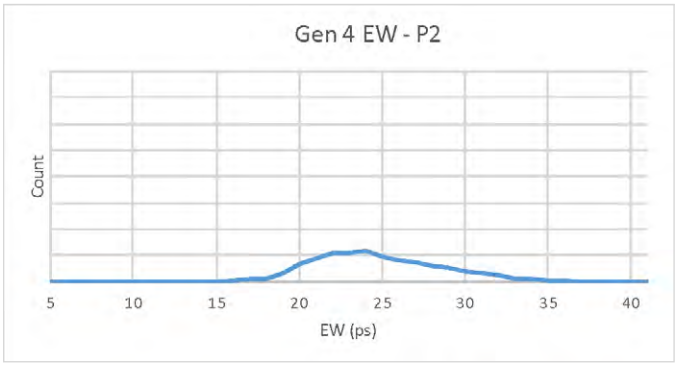
PCIe Gen 4 DUT Eye Width Distribution by Preset with TMT4 – AICs Only



Distribution by PCIe Preset 0 for Gen 4 Eye Width – AICs Only.



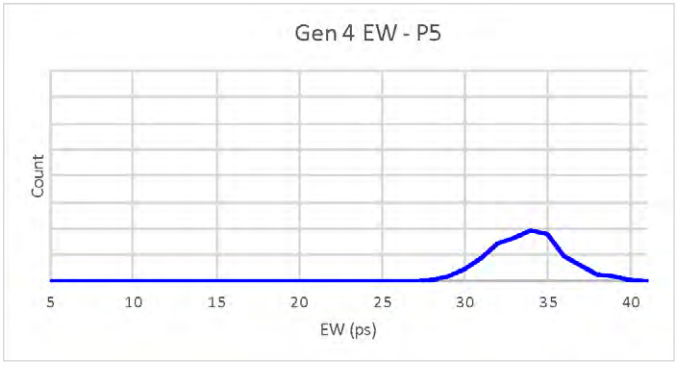
Distribution by PCIe Preset 1 for Gen 4 Eye Width – AICs Only.



Distribution by PCIe Preset 2 for Gen 4 Eye Width – AICs Only.

Distribution by PCIe Preset 3 for Gen 4 Eye Width – AICs Only.

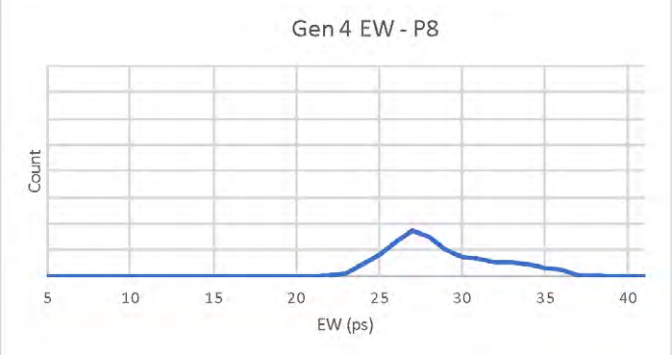
Distribution by PCIe Preset 4 for Gen 4 Eye Width – AICs Only.



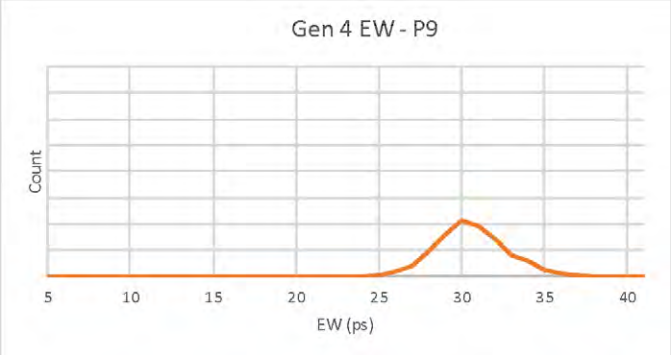
Distribution by PCIe Preset 5 for Gen 4 Eye Width – AICs Only.

Distribution by PCIe Preset 6 for Gen 4 Eye Width – AICs Only.

Distribution by PCIe Preset 7 for Gen 4 Eye Width – AICs Only.

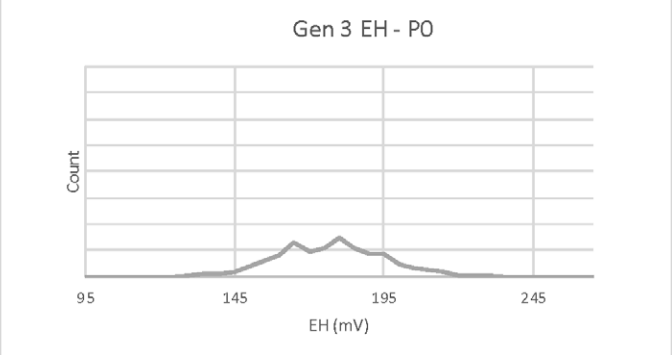


Distribution by PCIe Preset 8 for Gen 4 Eye Width – AICs Only.

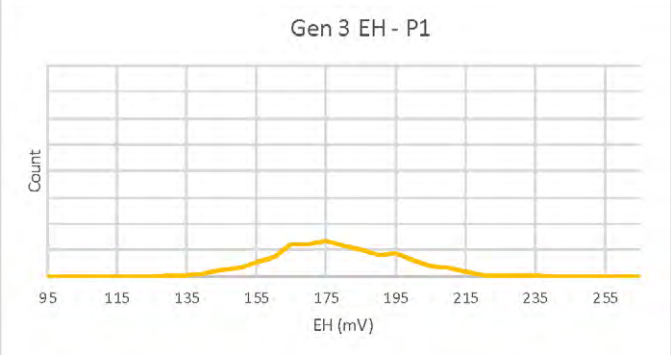


Distribution by PCIe Preset 9 for Gen 4 Eye Width – AICs Only.

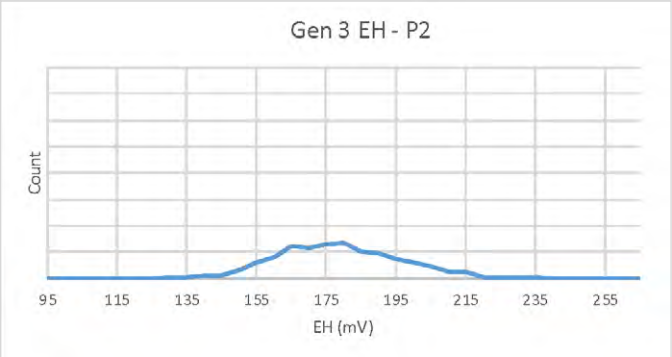
PCIe Gen 3 DUT Eye Height Distribution by Preset with TMT4 – AICs Only



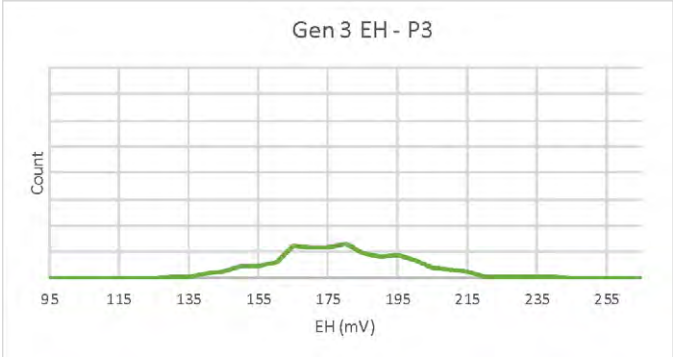
Distribution by PCIe Preset 0 for Gen 3 Eye Height – AICs Only.



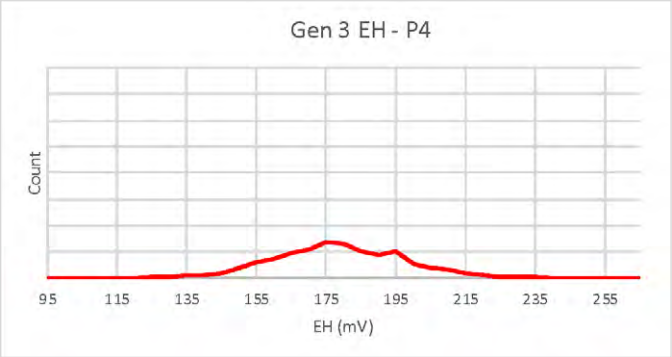
Distribution by PCIe Preset 1 for Gen 3 Eye Height – AICs Only.



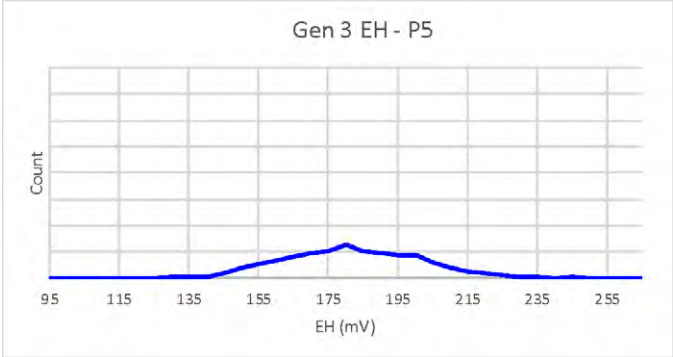
Distribution by PCIe Preset 2 for Gen 3 Eye Height – AICs Only.



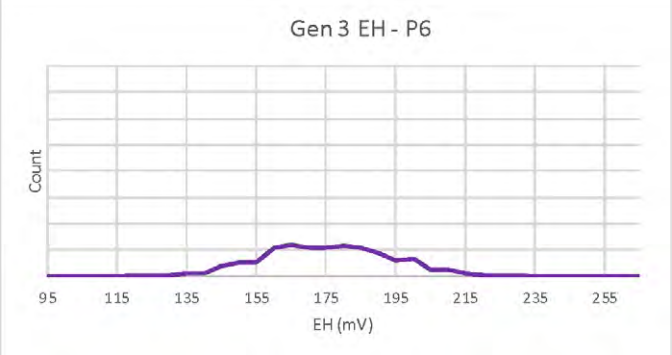
Distribution by PCIe Preset 3 for Gen 3 Eye Height – AICs Only.



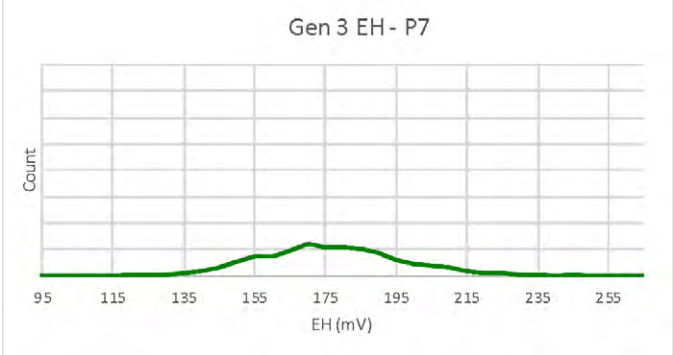
Distribution by PCIe Preset 4 for Gen 3 Eye Height – AICs Only.



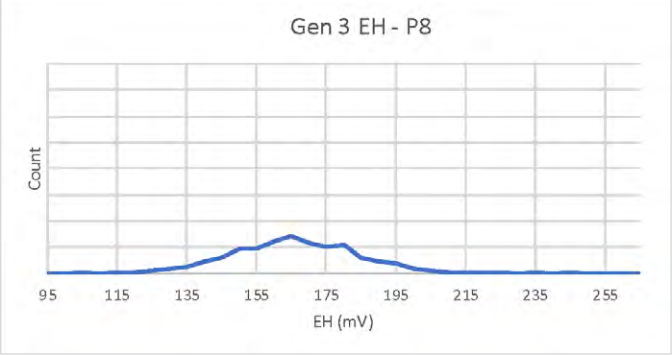
Distribution by PCIe Preset 5 for Gen 3 Eye Height – AICs Only.



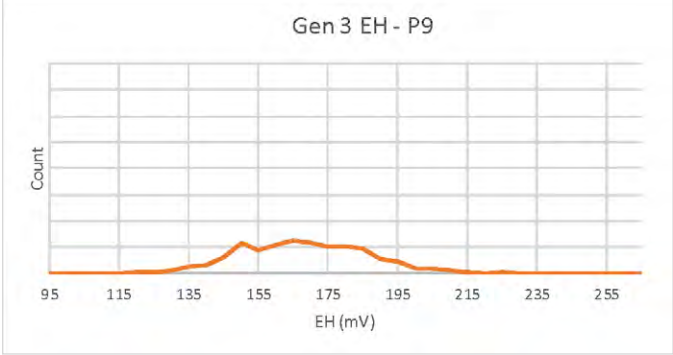
Distribution by PCIe Preset 6 for Gen 3 Eye Height – AICs Only.



Distribution by PCIe Preset 7 for Gen 3 Eye Height – AICs Only.

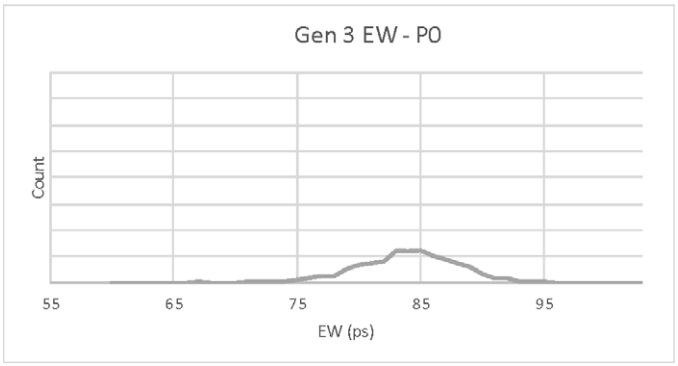


Distribution by PCIe Preset 8 for Gen 3 Eye Height – AICs Only.



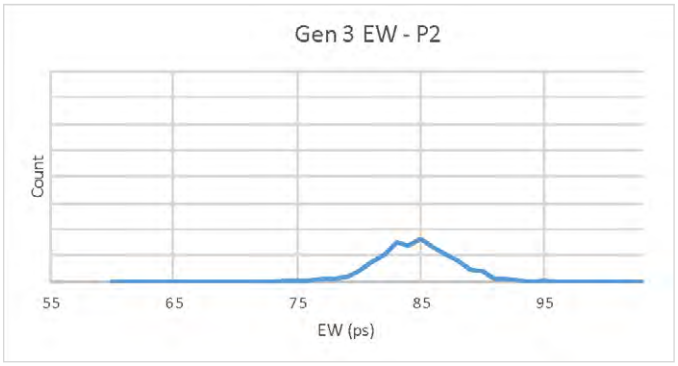
Distribution by PCIe Preset 9 for Gen 3 Eye Height – AICs Only.

PCIe Gen 3 DUT Eye Width Distribution by Preset with TMT4 – AICs Only



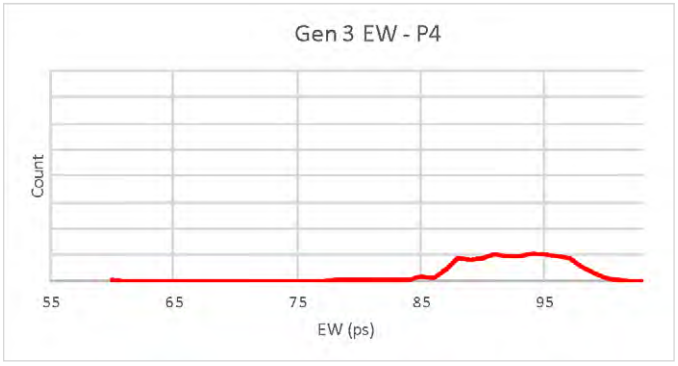
Distribution by PCIe Preset 0 for Gen 3 Eye Width – AICs Only.

Distribution by PCIe Preset 1 for Gen 3 Eye Width – AICs Only.

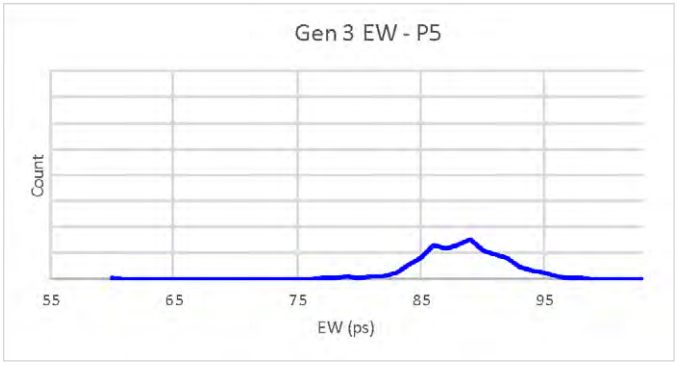


Distribution by PCIe Preset 2 for Gen 3 Eye Width – AICs Only.

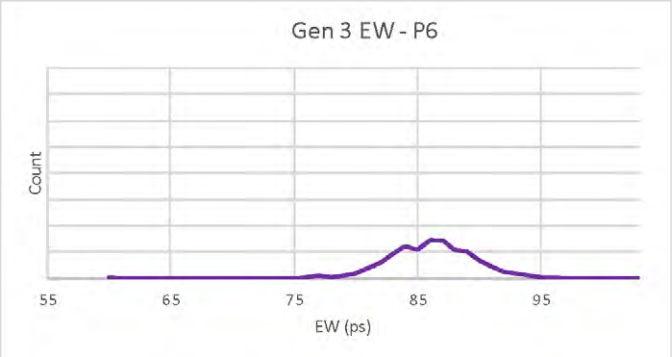
Distribution by PCIe Preset 3 for Gen 3 Eye Width – AICs Only.



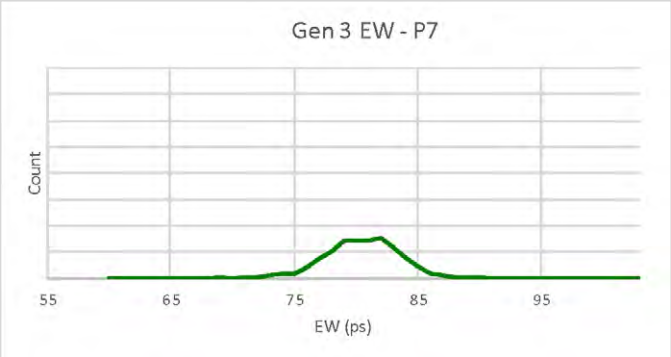
Distribution by PCIe Preset 4 for Gen 3 Eye Width – AICs Only.



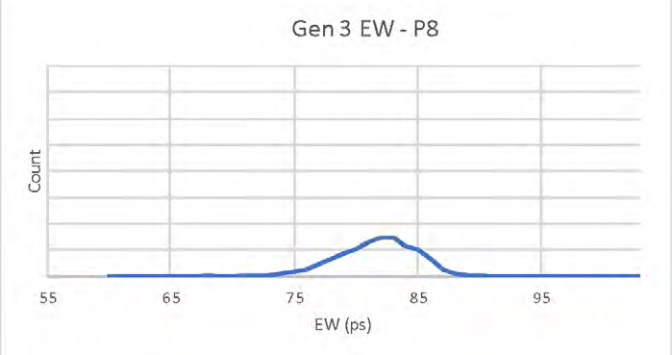
Distribution by PCIe Preset 5 for Gen 3 Eye Width – AICs Only.



Distribution by PCIe Preset 6 for Gen 3 Eye Width – AICs Only.



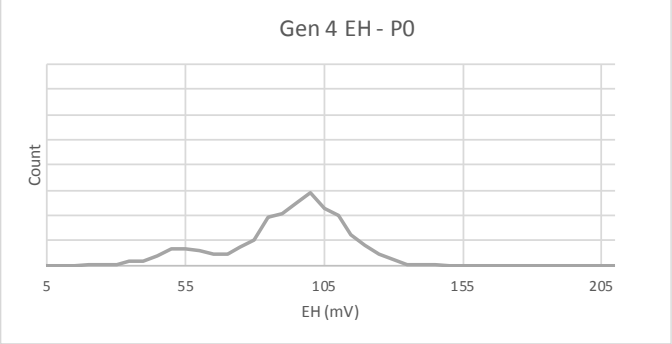
Distribution by PCIe Preset 7 for Gen 3 Eye Width – AICs Only.



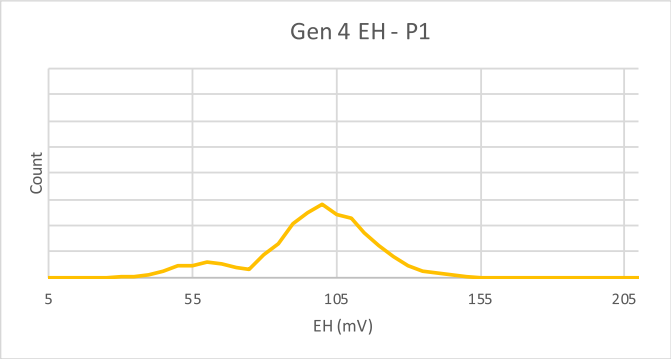
Distribution by PCIe Preset 8 for Gen 3 Eye Width – AICs Only.

Distribution by PCIe Preset 9 for Gen 3 Eye Width – AICs Only.

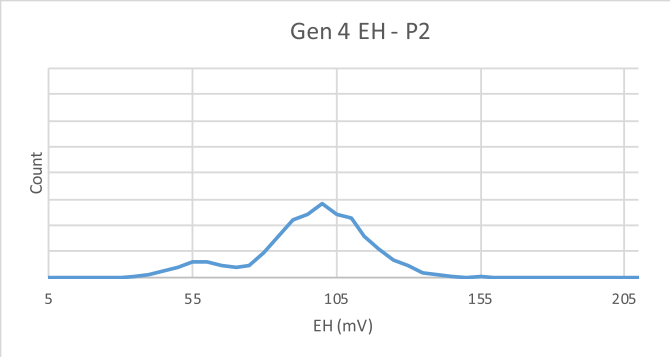
PCIe Gen 4 DUT Eye Height Distribution by Preset with TMT4 – MBs Only



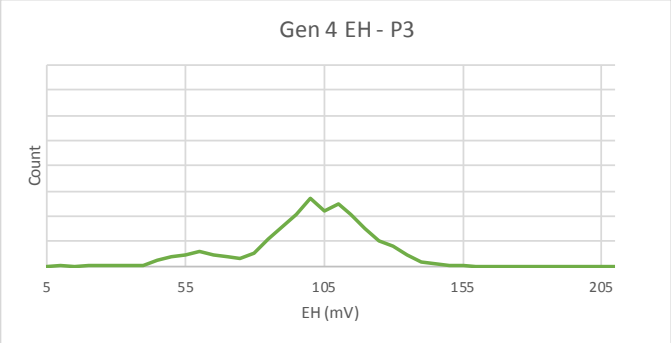
Distribution by PCIe Preset 0 for Gen 4 Eye Height – MBs Only.



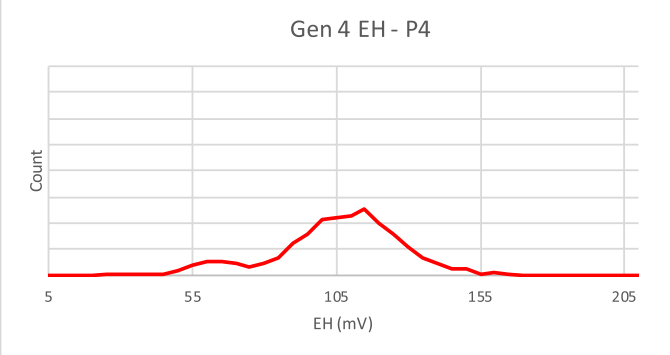
Distribution by PCIe Preset 1 for Gen 4 Eye Height – MBs Only.



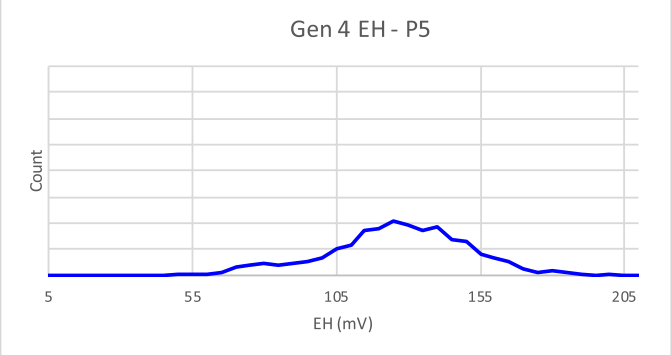
Distribution by PCIe Preset 2 for Gen 4 Eye Height – MBs Only.



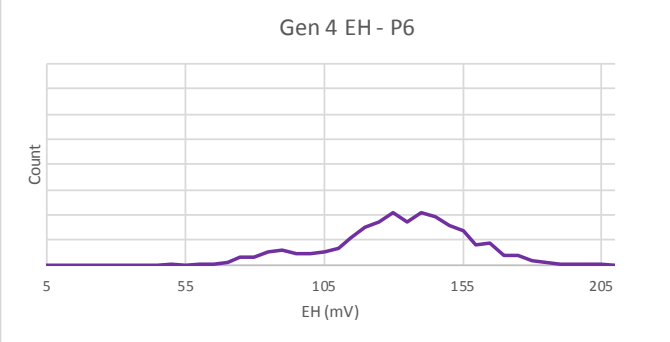
Distribution by PCIe Preset 3 for Gen 4 Eye Height – MBs Only.



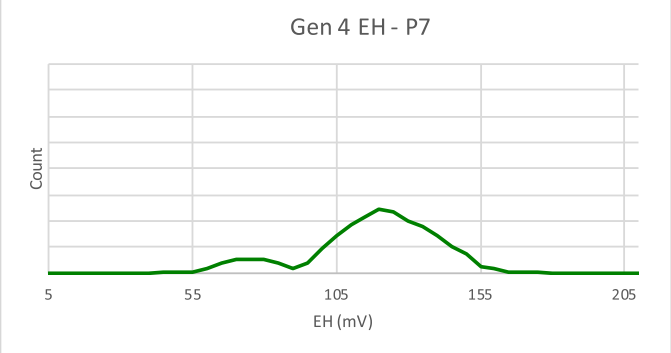
Distribution by PCIe Preset 4 for Gen 4 Eye Height – MBs Only.



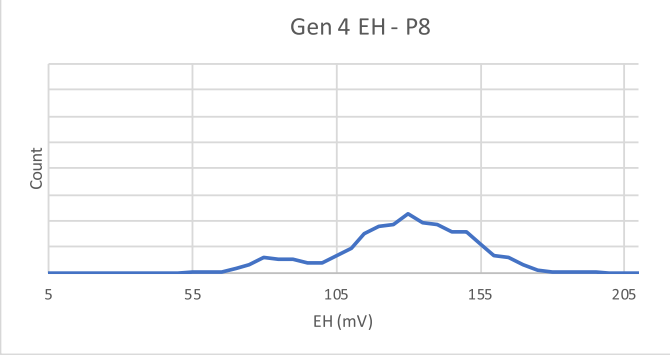
Distribution by PCIe Preset 5 for Gen 4 Eye Height – MBs Only.



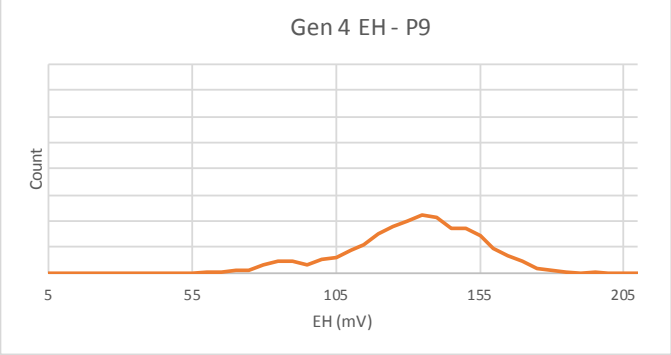
Distribution by PCIe Preset 6 for Gen 4 Eye Height – MBs Only.



Distribution by PCIe Preset 7 for Gen 4 Eye Height – MBs Only.

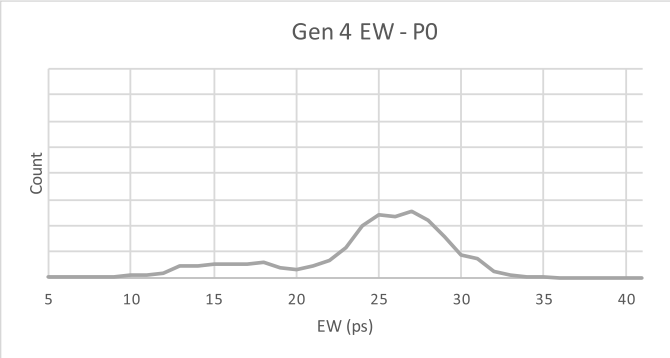


Distribution by PCIe Preset 8 for Gen 4 Eye Height – MBs Only.

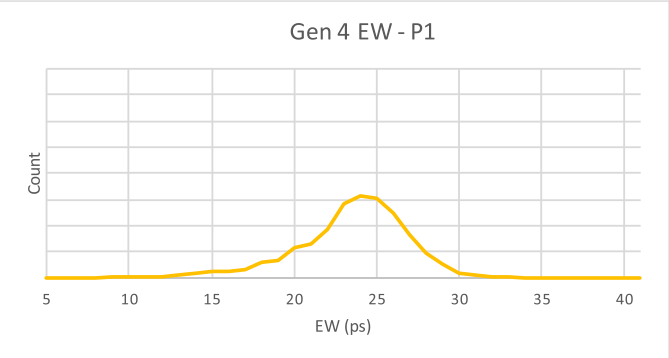


Distribution by PCIe Preset 9 for Gen 4 Eye Height – MBs Only.

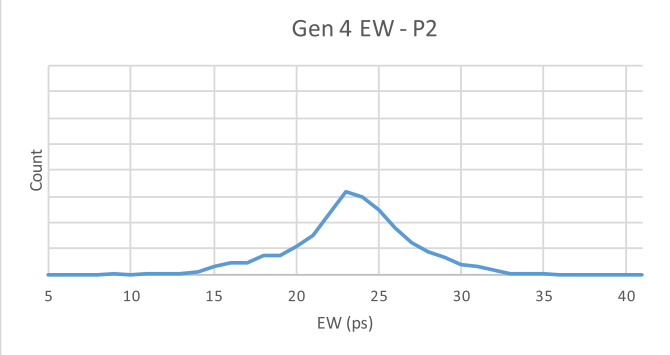
PCIe Gen 4 DUT Eye Width Distribution by Preset with TMT4 – MBs Only



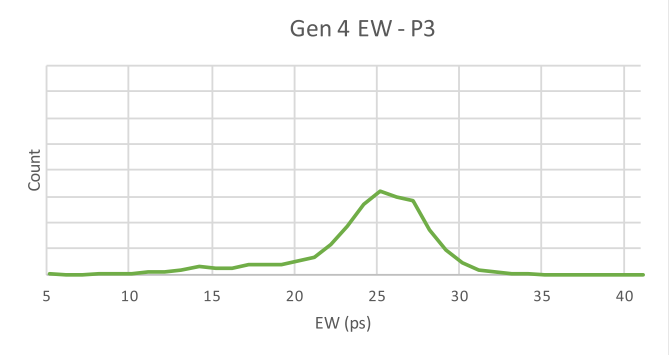
Distribution by PCIe Preset 0 for Gen 4 Eye Width – MBs Only.



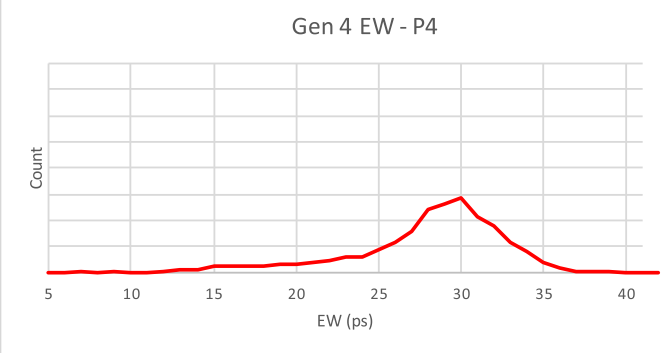
Distribution by PCIe Preset 1 for Gen 4 Eye Width – MBs Only.



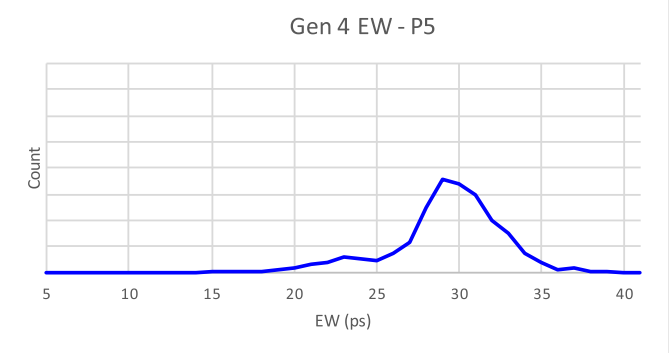
Distribution by PCIe Preset 2 for Gen 4 Eye Width – MBs Only.



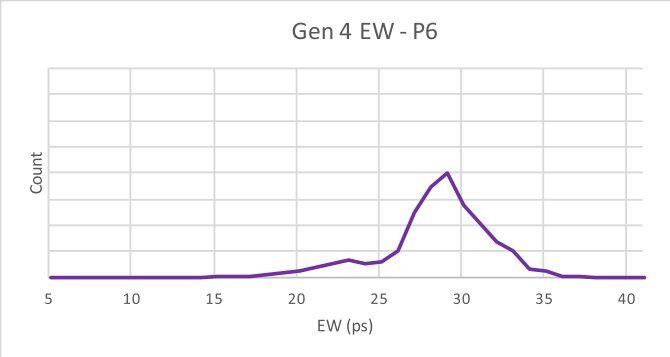
Distribution by PCIe Preset 3 for Gen 4 Eye Width – MBs Only.



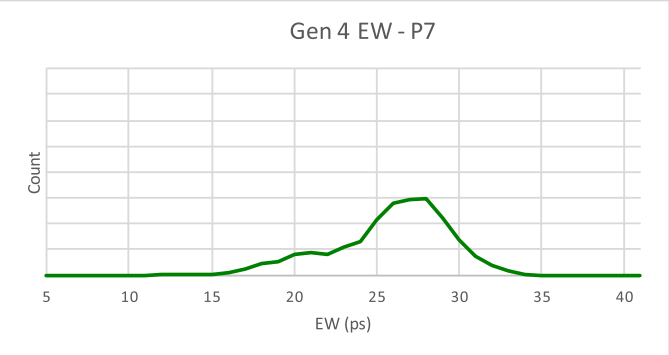
Distribution by PCIe Preset 4 for Gen 4 Eye Width – MBs Only.



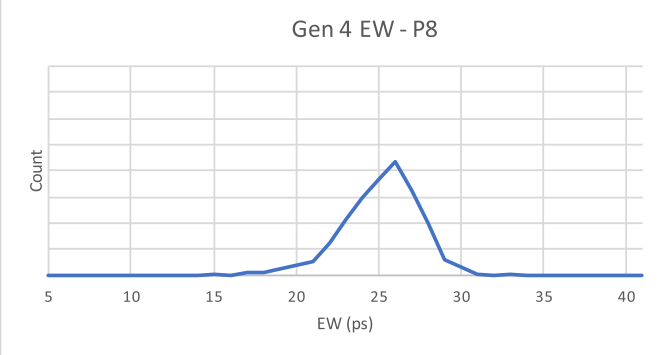
Distribution by PCIe Preset 5 for Gen 4 Eye Width – MBs Only.



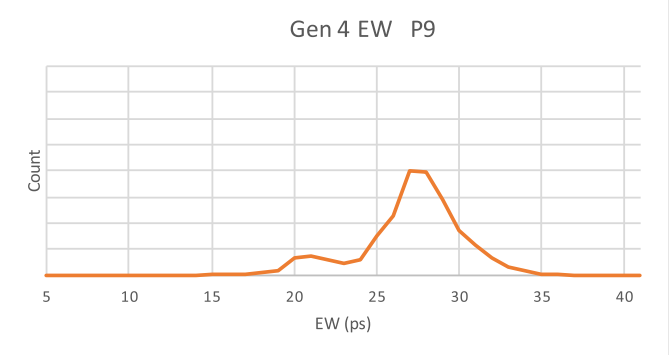
Distribution by PCIe Preset 6 for Gen 4 Eye Width – MBs Only.



Distribution by PCIe Preset 7 for Gen 4 Eye Width – MBs Only.

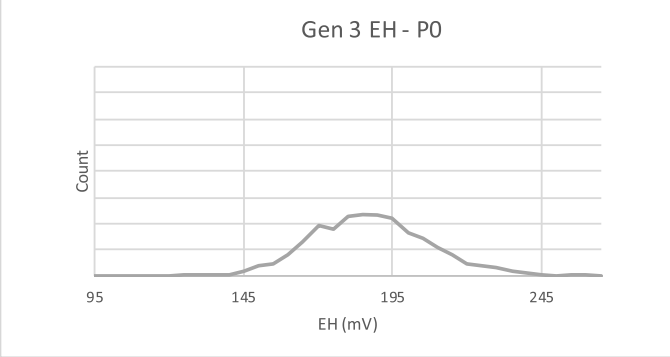


Distribution by PCIe Preset 8 for Gen 4 Eye Width – MBs Only.

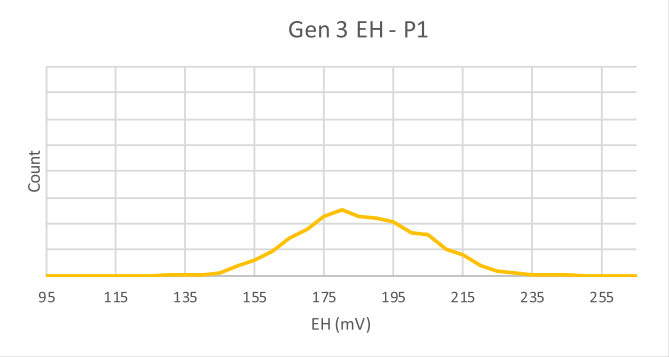


Distribution by PCIe Preset 9 for Gen 4 Eye Width – MBs Only.

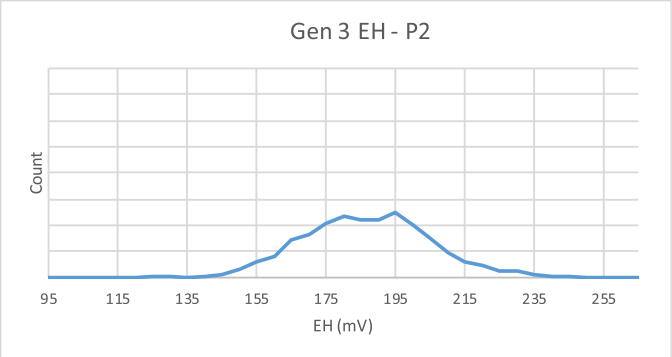
PCIe Gen 3 DUT Eye Height Distribution by Preset with TMT4 – MBs Only



Distribution by PCIe Preset 0 for Gen 3 Eye Height – MBs Only.

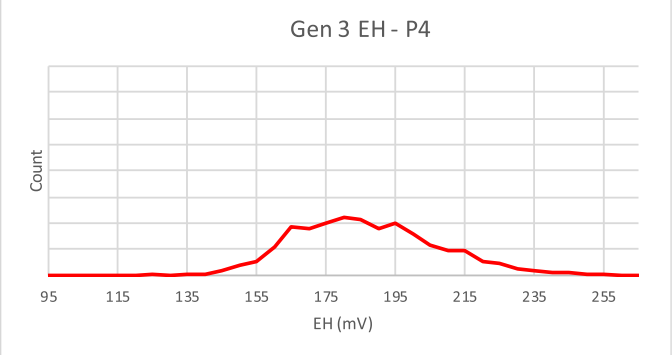


Distribution by PCIe Preset 1 for Gen 3 Eye Height – MBs Only.

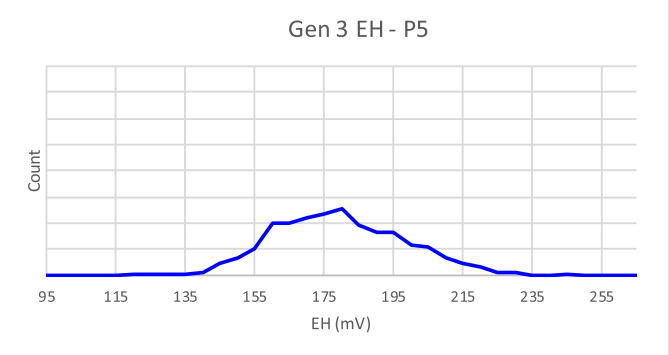


Distribution by PCIe Preset 2 for Gen 3 Eye Height – MBs Only.

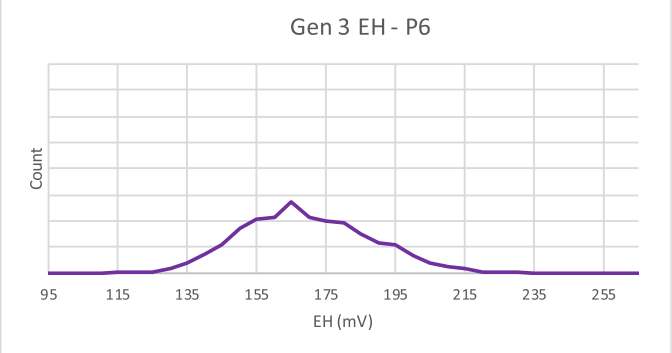
Distribution by PCIe Preset 3 for Gen 3 Eye Height – MBs Only.



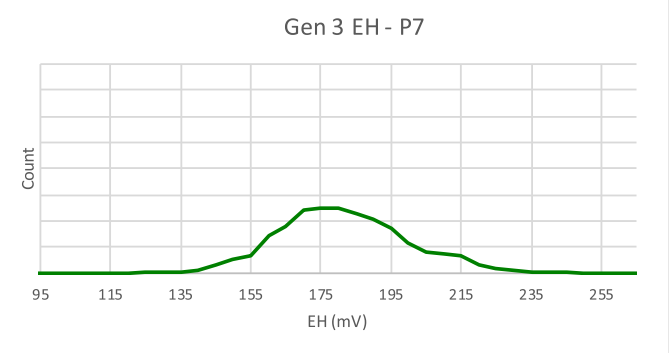
Distribution by PCIe Preset 4 for Gen 3 Eye Height – MBs Only.



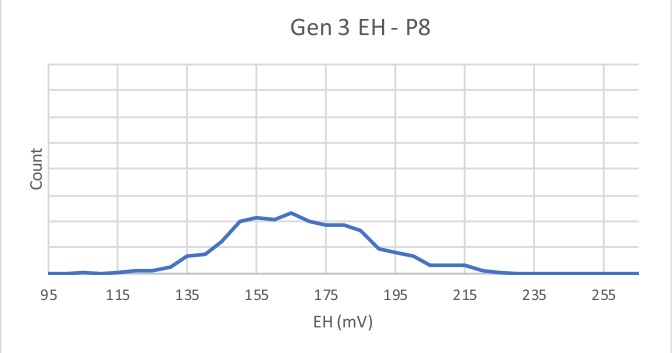
Distribution by PCIe Preset 5 for Gen 3 Eye Height – MBs Only.



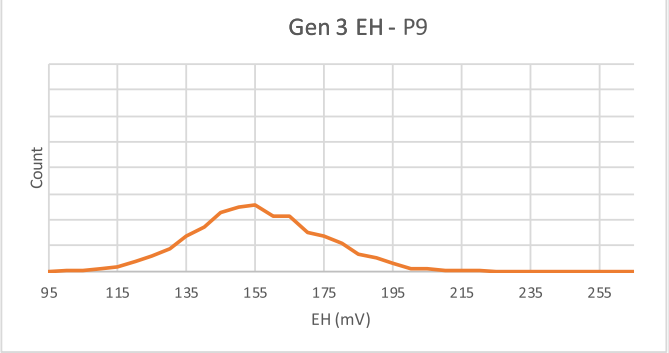
Distribution by PCIe Preset 6 for Gen 3 Eye Height – MBs Only.



Distribution by PCIe Preset 7 for Gen 3 Eye Height – MBs Only.

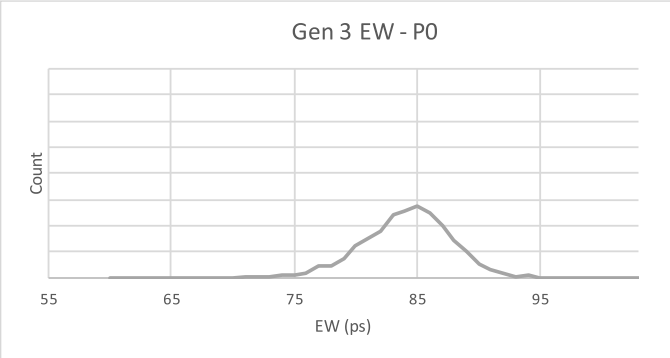


Distribution by PCIe Preset 8 for Gen 3 Eye Height – MBs Only.

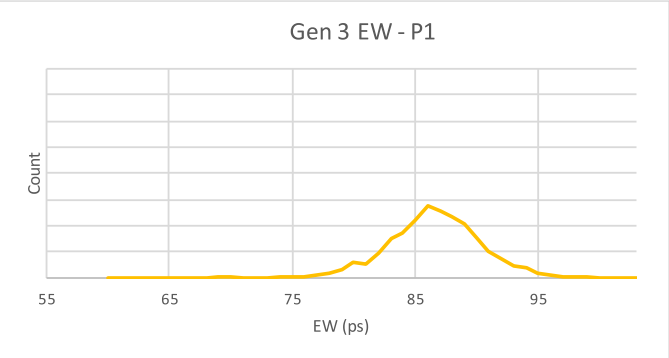


Distribution by PCIe Preset 9 for Gen 3 Eye Height – MBs Only.

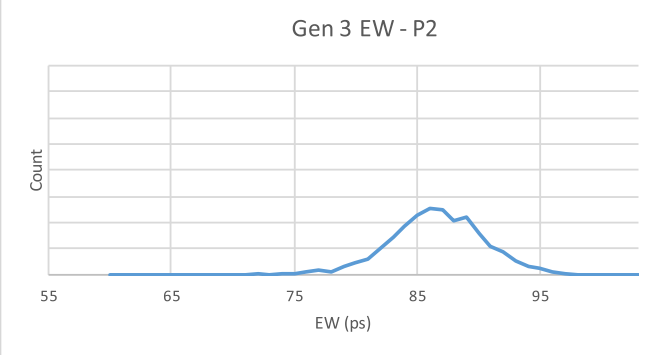
PCIe Gen 3 DUT Eye Width Distribution by Preset with TMT4 – MBs Only



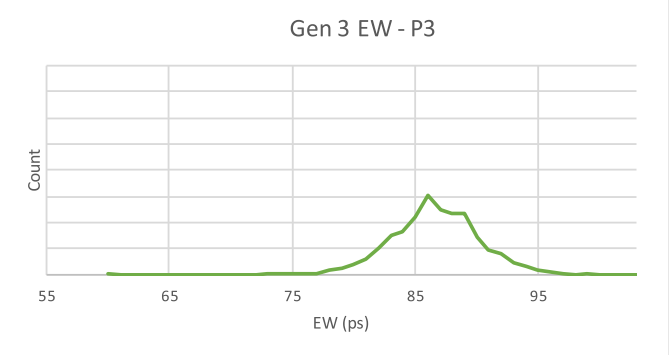
Distribution by PCIe Preset 0 for Gen 3 Eye Width – MBs Only.



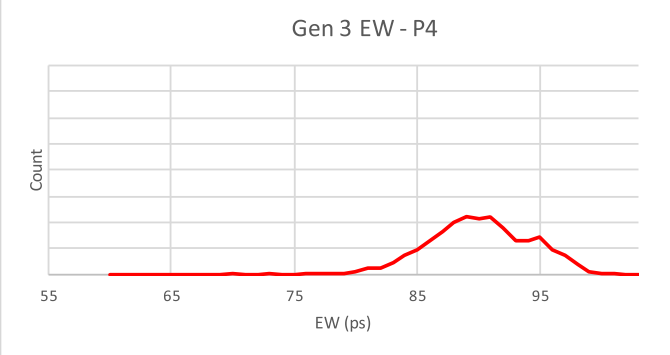
Distribution by PCIe Preset 1 for Gen 3 Eye Width – MBs Only.



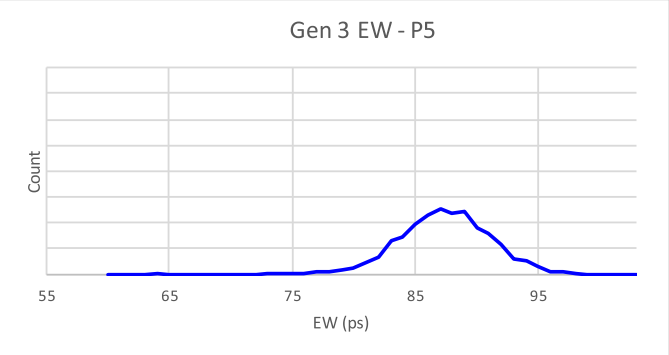
Distribution by PCIe Preset 2 for Gen 3 Eye Width – MBs Only.



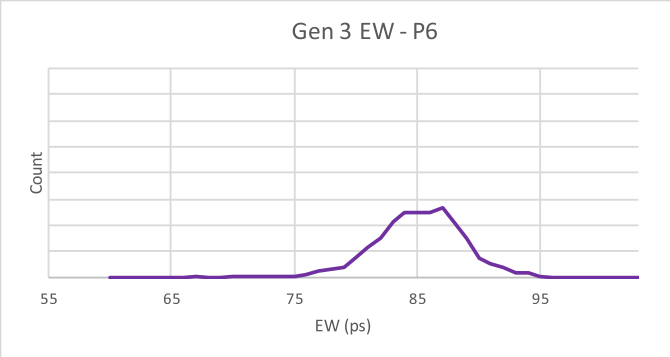
Distribution by PCIe Preset 3 for Gen 3 Eye Width – MBs Only.



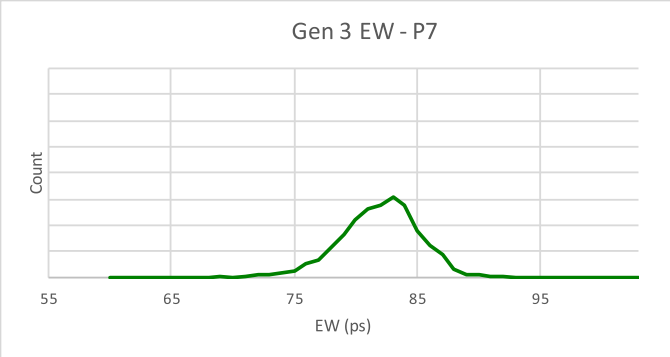
Distribution by PCIe Preset 4 for Gen 3 Eye Width – MBs Only.



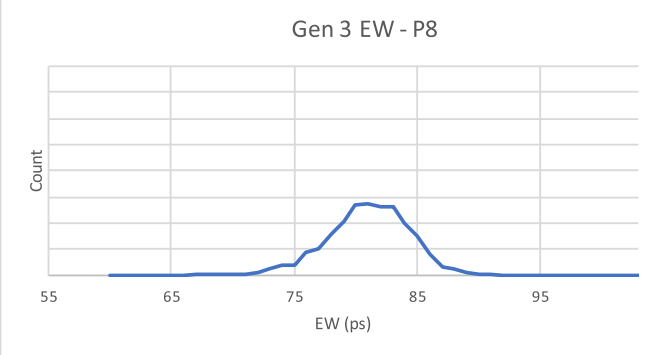
Distribution by PCIe Preset 5 for Gen 3 Eye Width – MBs Only.



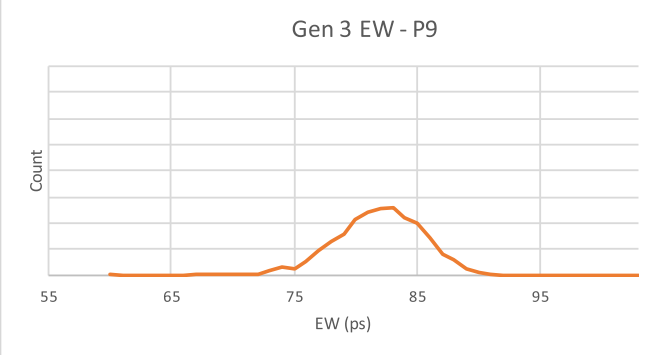
Distribution by PCIe Preset 6 for Gen 3 Eye Width – MBs Only.



Distribution by PCIe Preset 7 for Gen 3 Eye Width – MBs Only.



Distribution by PCIe Preset 8 for Gen 3 Eye Width – MBs Only.



Distribution by PCIe Preset 9 for Gen 3 Eye Width – MBs Only.

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