
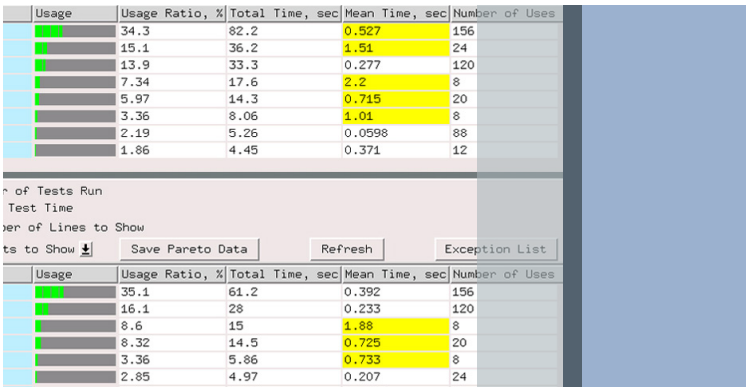


# Achieving Maximum Throughput with Keithley S530 Parametric Test Systems

## Application Note

Keithley Instruments is a world leader in the development of precision DC electrical instruments and integrated parametric test systems. Its expertise in parametric test technology goes back to the early days of the semiconductor industry and continues today with the development of new systems and measurement techniques. This application note addresses recent developments in system test speed optimization and offers general guidelines for test speed optimization at both the system and specific test algorithm level. Although it was developed for existing and new users of Keithley S530 Parametric Test Systems, it can be also useful to any parametric test engineer.

On a system level, Keithley recently implemented enhancements to the S530 Parametric Test System that can improve test time by 20 percent or more. This requires updating the system to Version 5.6 of the Keithley Test Environment (KTE). The actual improvement that S530 users can see will depend on the actual parametric test code and the distribution of various test types (e.g., the number of low current tests versus high current tests and sweeps).

Test engineers are well aware that overall parametric system speed and performance are only partially dependent on the performance of the system hardware. Using optimized test algorithms is just as important to achieving adequate accuracy at a reasonable throughput. This application note discusses some considerations and measurement methods that can help to optimize test code while minimizing the required accuracy vs. speed trade-offs.

When optimizing a parametric test system's test speed, it is important to understand the general trade-off between test speed (system throughput) and measurement accuracy (repeatability and data correlation). This trade-off applies to the system hardware's overall measurement capability, as well as the test algorithm or test code. The curve in **Figure 1** illustrates one of the causes for this trade-off: low current measurements take longer to complete, with higher accuracy requiring longer measurement times. At higher current levels, this trade-off is less significant.

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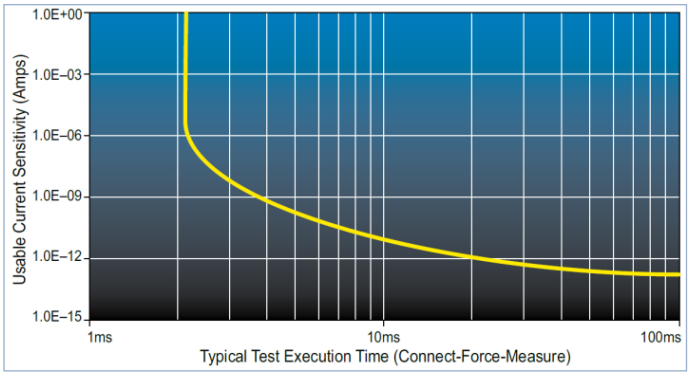


**Figure 1: Sensitivity vs.** typical execution time for connect-force-measure for different current levels.

## Test time optimization strategies and approaches

Overall system test speed is a function of the total time of all the individual test programs and is always determined by two factors: overall system performance and the design of the user test programs. Although both are equally important, let's first address optimizing the user test programs.

Optimizing large production testing at the cassette or wafer level is no trivial task, as opposed to focusing on optimization of specific individual test programs. Many Keithley systems customers have employed the following approach, often in cooperation with Keithley applications engineers.

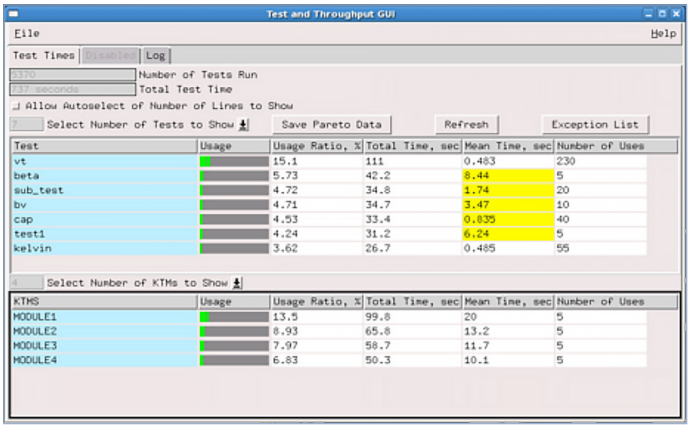


**Figure 2: Test time distribution in Pareto analysis.**

The first step in this approach is to create a time log file for a full wafer lot test by enabling software flags. Each individual test is logged. Then all tests are grouped by type, for example, "vt" test, "beta" test, "breakdown" test, etc. As shown in Figure 2, a Pareto report is created using one of the Keithley system software tools, *ptlog*. The first column shows the name of the test or test macros (in KTMS section). The second and third columns show relative usage of the test in terms of its percent contribution; the fifth column displays the average test time per test/macros. Analysis is performed for individual tests and those same measurements made within test macros (typically subsite-level test programs). Improvements in the test times for only a few top test time contributors provides predictable test time improvement for a full wafer lot test. For example, by reviewing the individual tests shown in **Figure 2** and reducing the test times for "vt" to 0.24 seconds and for "beta" to 1 second, overall test time can be improved by approximately 10 percent. Only two test types must be changed to realize this improvement. Pareto data makes it easy to identify the few tests that need speed optimization. Prioritizing the effort will produce the greatest benefit for the time invested in adjusting the test code.

Optimization and test time improvement must be performed in conjunction with correlation analysis that compares the new measurement data with historical data. Because test time improvement always has the potential to cause data shift, which is unacceptable in semiconductor process control monitoring (PCM), it is preferable to minimize the number of changes needed to achieve the maximum possible benefit. This application note doesn't address the complications associated with correlation issues because there are too many options to consider and experience with device physics and device design knowledge are usually required. However, to ensure successful and effective correlation issue resolution, cooperation between the test engineer and the device engineer is essential.

## Best practices and standard test scenarios

By considering some specific test scenarios, it's possible to identify considerations and approaches that should help to minimize test times with little or no data quality trade-off.

### Low current/leakage measurement optimization

Leakage or $I_{off}$ measurement is the measurement of currents ranging from 1nA to 0.1pA. The dynamic range of a source measure unit (SMU) instrument depends on the power line cycle (PLC) integration time and is typically within four to five digits of the measurement range. For example, to measure 1pA-level leakage, the SMU current range must be set to 10nA or lower. As mentioned previously, current measurement test time increases dramatically on low current ranges.

Real device leakage is usually much smaller than what is actually measured for PCM. Leakage tests rarely measure actual device leakage. Usually, this test returns a value that is a function of the lowest allowed current range, device capacitance,

SMU settling, and user delay. Therefore, to some degree, leakage measurements can be "dialed in." There's no point to waiting a long time to measure a small leakage value that doesn't represent any physical property. From a PCM perspective, it's important to establish some reasonable leakage floor for the leakage measurements (for example, 2–10pA) to optimize test time.

Therefore, to optimize leakage tests, the minimum required current value for each device must be established first. Based on this value, choose the minimum allowed current range. If the minimum required current is 10pA, then limit the lowest allowable measurement range to (1e-11 * 1e4 = 1e-7) 100nA using these commands:

***lorangei(SMU1, 1e-7);*** *//limits the lowest allowed range*

***setmode(SMU1, KI_INTGPLC, PLC);*** *//sets integration time to PLC*

***measi(SMU1, &dummy);*** *//dummy measurement, used here to bring the range to the appropriate setting*

***intgi(SMU1, &Ioff);*** *//measurement with integration over PLC*

In the calculation above, *1e4* represents four digits of SMU dynamic range. Keithley recommends using a PLC integration setting of 0.1PLC (1.6ms of test time at 60Hz,) or possibly up to 1PLC (16ms) for low current measurements. Of course, these settings are simply recommendations and ultimately must be revised after the test engineer and PCM data specialist consider them. With KTEv5.6, 1pA to 5pA measurements now settle in the range of 0.2 to 0.3 seconds, depending on the bias level.

## Voltage breakdown measurements

The voltage breakdown test, which is widely used to characterize the electrical strength of various structures, can be performed in two ways. The most common technique sweeps voltage, stopping at some level of the current. The second technique forces current and directly measures breakdown voltage. Both techniques have limitations that must be understood to allow accurate evaluation of the breakdown voltage at a minimum time.

Voltage sweep is the slowest technique because it usually measures a large number of points. Decreasing the number of points and speeding up the slew rate may lead to false measurements, given that there is capacitive displacement current ( ) that can be comparable to the requested current trigger level and cause a trigger at a smaller, premature voltage levels.

The main disadvantage of the second technique is the dependency of voltage on the test time in poorly designed tests. Two undesirable things usually happen in the tests. For large capacitors, it takes a long and unknown time to charge the capacitor fully to reach breakdown voltage. This time can be characterized in the lab. But in the production environment, when a large number of tests must be done quickly, this test becomes difficult to run. Also, some breakdown structures may show degradation of the hold voltage with time.

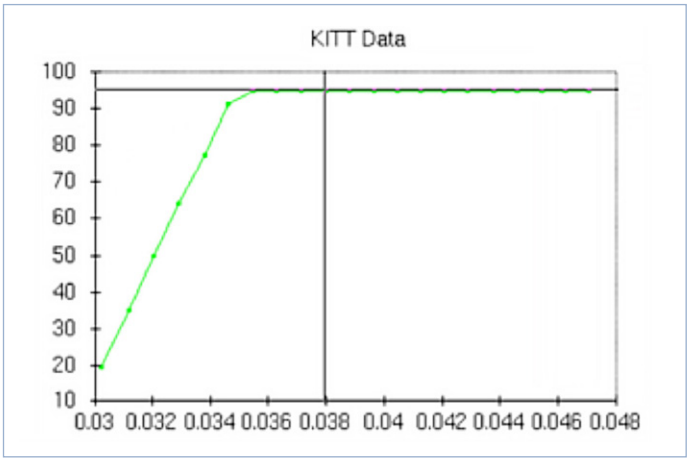


**Figure 3: Example of breakdown voltage test (voltage vs.** time)

For breakdown voltage tests, Keithley recommends using a properly designed "force current" technique using the following sequence:

1. Force test current.
2. Monitor voltage vs. time.
3. Stop the test when the latest measured voltage is less than the previous one or if the voltage slope decreases significantly. The test should timeout if it exceeds the time limit.

Implementing this sequence allows measuring breakdown voltages as fast as possible, with no dependency on the test time. **Figure 3** illustrates an example of a non-destructive breakdown test. This test should stop when the V(t) slope becomes horizontal. Keithley applications engineers can provide S530 system users with further examples of a properly designed breakdown test.

## Transistor threshold voltage ($V_{th}$) tests

Transistor characterization or, more specifically, threshold voltage measurement is an example of a very common test that usually represents a significant portion of the overall PCM test time. Extrapolated Vth at maximum $g_m$ is an industry-standard technique that provides a very stable threshold voltage measurement. In this technique, gate voltage is swept over a range of voltages. From the $I_dV_g$ array, the threshold voltage is

calculated from intercept of the $I_dV_g$ tangent curve at maximum transconductance (**Figure 4**).

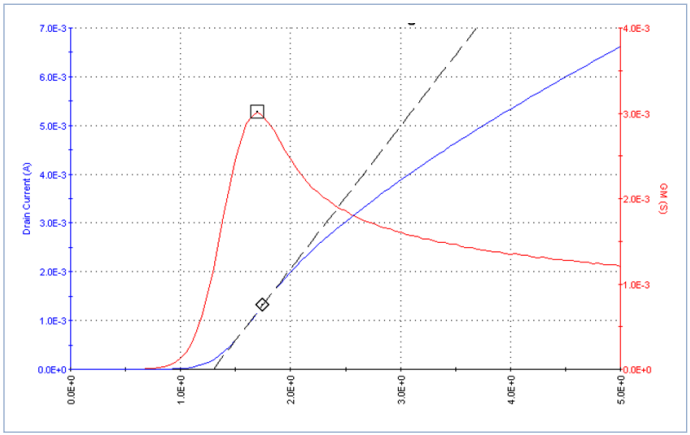


**Figure 4: $I_d/V_g$ data for threshold voltage measurement.**

One common mistake in the implementation of the test is the measurement of drain current in auto-range mode. In these tests, most of the test time is taken up by the measurement of the $I_{off}$ current; the $V_{th}$ value is calculated from only two or three points at the intercept line. Therefore, once again, the simplest fix for bloated test times is to control the lowest allowed current measurement range using this command:
***lorangei(DRAIN_SMU, 1-e4);***

This allows the measurement to be done in auto-range mode but fixes the lowest allowed range to 1e4, which provides adequate current resolution at the 1.0A–0.1µA level of drain current. Limit the number of sweep points used to about 30. Increasing the number of points does not improve accuracy of the extracted $V_{th}$; instead, it can actually degrade the accuracy due to smaller voltage steps, which will increase data noise in the digital differentiation.

## "Learn-Range" optimization techniques

Keithley has developed several implementations of adaptive testing, in which test program content changes based on test results. The data-driven design of the Keithley Test Environment (KTE) facilitates this capability. Test data can be easily stored and retrieved in the test program. However, given that data manipulation is a capability that can be used in any environment, test program engineers might find the following suggestion useful when using any hardware.

Previous test results, such as threshold voltage or drain current measurements, can be used to accelerate an executing test program, by storing and retrieving data from a previous site and adjusting the current test according to the expected value of the result. Usage and optimization of the test in accordance with the expected value can provide significant test speed benefits. Many Keithley systems users have used this learn-range capability successfully in test programs.

## Capacitance measurement optimization, "smart" offset measurements

Offset or "chuck down" measurements are required for capacitance tests. In poorly designed tests, this offset measurement is performed for each test instance. Some system users perform offset measurement once per wafer or per lot and do not have a time penalty for this redundant measurement. They still have to organize the data flow and use multiple naming conventions to use previously measured values reliably.

In general, Keithley recommends making test code adaptable and intelligent. Capacitance tests should handle data manipulation internally by defining a unique keyword that includes used pins and test conditions. The test code then should use this keyword to measure, store, and retrieve the offset value if needed. This allows for one offset value measurement per wafer lot, does not require management of off-values in the test program, and scales to test programs of any size. Actual test code implementation can be provided to Keithley system users upon request or training.

## Test time optimization recommendations

Several general considerations and recommendations are useful in optimizing test times.

One of most common ways to handle correlation issues is the use of the delay function. Although it does help "fix" some of the tests quickly, it is typically used when there is insufficient time on the production floor to understand the root cause of the correlation problem and resolve it properly. The need to charge capacitive devices fully makes a longer delay necessary. It's important to note that the most recent generation of Keithley system SMUs do not exhibit "range compliance." In earlier generations of DC instruments, the current from the SMU was limited to the set current measurement range, which made it necessary to wait for full charge. This need was especially pronounced on lower current ranges, such as 0.1µA and lower. Newer Keithley system SMUs eliminate the need to wait for full charge and allow faster "force V/measure I" operation. "Force I" mode is unaffected by this consideration. The best way to handle capacitive load situations and eliminate the need for any delay is live monitoring of current in the test and proper specification of exit criteria. This would allow eliminating artificial delays and making tests independent of arbitrary delay settings.

Another suggestion that is obvious but often overlooked in many optimization efforts is the use of fixed ranges when-

ever possible. Although the advantage of auto-range tests is self-evident because auto-ranging allows the use of the same test for a wide range of measurements, the use of a fixed range provides some extra time improvement in many scenarios. A breakdown test is a good example: the trigger current is known and a fixed current range could be set to 10*TriggerCurrentValue to enhance accuracy and speed with no trade-off.

At lower current values, it is advantageous to use the integration function *(intgi(SMU, &I);)* instead of any delay. For example, for currents measured in the range of 1µA to 1nA, the proper PLC setting should be about 0.1, which is 1.7ms (1 PLC being equal to 1/60th of a second or 16.7ms). This time is small relative to the total time of a standard test, but it provides better accuracy than the standard measure current *(measi(SMU, &I);)* function. For lower currents, 1.0 PLC will provide a better trade-off between test time and accuracy.

## S530 recent system improvements

As mentioned previously, Keithley has enhanced both the S530 system hardware and software (KTEv5.6) to focus primarily on speed improvement. Overall improvement of system test speed will be approximately 20 percent without any test code changes and little or no impact on data correlation. The overall throughput improvement possible will depend on the specific use-case or mix of devices and measurements.

S530 system and KTEv5.6 software speed improvements come from several areas:

- Low current test speed: Settling times on the lower SMU current measurement ranges have been improved to speed up measurement. Although sub-picoamp measurements previously took approximately two seconds to settle, settling time for the same measurement now takes approximately 0.2 seconds.
- Improvement in sweeps: KTEv5.6 leverages the sweep capabilities inherent in the S530's system SMUs. Each range used in a multi-range sweep has unique built-in delays (i.e., lower current measurement ranges with longer delays than higher measurement ranges). By using the new setmode command *KI_DELAY_FACTOR*, this delay factor value is multiplied by the built-in delay associated with each range. With sweep functions often representing a large portion of overall wafer test time, significant time savings can be realized with this new approach to managing delay settings within KTE.
- Device initialization [*devint() speed-up*]: This command is used to (re)initialize the system and is used at the end of most tests. This function was streamlined in KTEv5.6, and because it is used so frequently, the cumulative time savings is substantial.
- New Keithley DMM: The previous generation DMM used in S530 systems was designed more for bench applications and was controlled via GPIB. Keithley's latest DMM is designed for high-speed system applications and is controlled via Ethernet. As a result, S530 measurements such as differential voltage and low resistance can now be made at substantially higher speeds.
- New System Speed Mode: Users can change overall system speed easily by modifying the system configuration file. As discussed previously, there is always a performance trade-off between speed and accuracy. The system speed mode options are FAST, LEGACY and CUSTOM. The fast mode is now the default setting and provides a speed improvement of approximately 20 percent over previous versions of S530 KTE software. The legacy mode setting provides performance compatible with previous KTE versions. Several system speed improvements are tied to System Speed Mode, including the new *DELAY_FACTOR* setting described previously. This feature can also be used with individual tests or test macros with the *setmode()* command.

```
[SYSTEM SPEED MODE]
MODE = FAST

[INSTRUMENTATION]
VERSION_ID=1
LIST=GNDU,MTRX1,SMU1,SMU2,SMU3,SMU4,KIB,KIP,CMTR1,VMTR1
```

**Figure 5: Modifying *icconfig_QMO.ini* for changing system speed mode (FAST, LEGACY)**

```
[SYSTEM SPEED MODE]
MODE = CUSTOM

NPLC=0.01
INTG_NPLC=1
ANALOG_FILTER=1
DELAY_FACTOR=1

[INSTRUMENTATION]
VERSION_ID=1
LIST=GNDU,MTRX1,SMU1,SMU2,SMU3,SMU4,KIB,KIP,CMTR1,VMTR1
```

**Figure 6: Modifying *icconfig_QMO.ini* for change system speed mode (CUSTOM)**

## Optimization cases

As stated previously, enhancements to the S530 and its system software (KTEv5.6) can improve overall measurement time (at the wafer or lot level) by approximately 20 percent without requiring any user test code changes. It is possible that correlation for a few of the measurements will drift outside the acceptable PCM window and may require adjustment. But even in this case, that improvement of approximately 20 percent should still be achievable.

Now, consider various cases in which S530 users not only get the benefits of the latest S530 system and software enhancements but also apply some of the optimization techniques discussed here. Keithley has examined three different use-cases to assess the total test time improvement from the system and software enhancements in conjunction with optimization efforts. The first case is for general semiconductor wafer test, which includes common tests for semiconductor wafer PCM structures. The second case is wafer test that includes a higher percentage of sweep measurements. The last case includes a higher percentage of low current measurements. With both system and software enhancements plus optimization efforts, improvements ranging from 25 to 40 percent were realized across this range of use cases. The actual timing improvement data will depend on the type of test program, the amount of built-in hardcoded delay, and the contributions of various tests, such as leakage tests vs. high current tests, amount of voltage sweeps, and capacitance measurements.

The actual level of test speed improvement depends on the use case; for example, a case with a large fraction of leakage or low current tests will differ from a case with a significant fraction of the voltage sweeps. Some test code contains a large number of built-in delays. These delays can be removed; however, this will require correlation effort and time. And different tests provide different levels of potential speed gain vs. time invested.

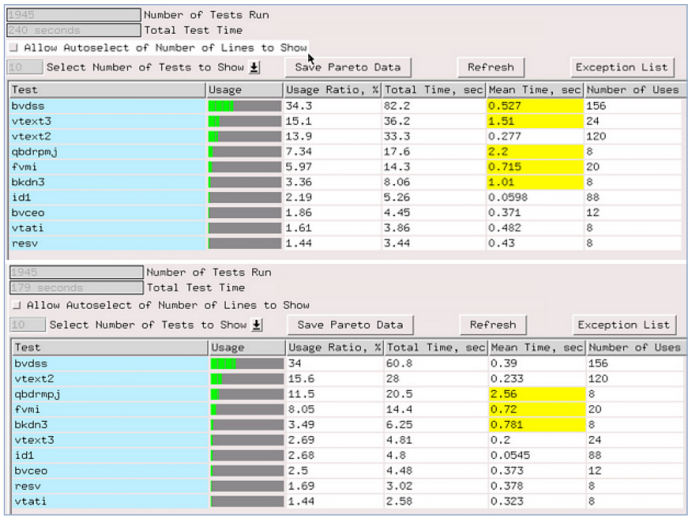


**Figure 7: Test time, Pareto distribution, before (above) and after (below) installing most recent KTE update.**

**Figure 7** shows a before-and-after example of the recent S530 system and software enhancement benefits. Sample data was collected on an actual wafer in which the total test time decreased from 240 to 179 seconds for 4 sites, amounting to a 25 percent test speed improvement. The test program contains about 250 tested parameters and includes well-known or standard tests. In this case, the test type distribution tilts slightly towards a higher number of breakdown tests and voltage sweeps.

This example does not include any further improvement that can be achieved using optimization techniques of user test code as described earlier in this application note. The test speed improvement represents only that associated with the system and software enhancements. On average, additional optimization of user tests usually brings another 5 to 20 percent improvement, depending on the initial optimization level of the original code.

The most important columns in the analysis are Usage Ratio and Mean Time. Usage Ratio determines the priority for further test code improvement, and Mean Time determines the feasibility of the improvement. The yellow highlighting is identifies tests longer than 0.6 seconds, which have a higher chance of optimization success.

## Summary and suggestions for action

To summarize, Keithley continues to explore and develop ways in which the S530 Parametric Test System can make PCM-acceptable measurements faster than previously possible. This application note outlines the combination of system hardware, software, and applications knowledge necessary to achieve continuous improvement. The most recent enhancements are associated with KTEv5.6 system software, which can provide test time improvements of 20 percent or higher, depending on the wafer test case. This is obviously good news for existing S530 system users who can upgrade their systems and for those considering new systems.

To optimize test speed vs. accuracy or repeatability still further, a new software tool (time breakdown with ptlog that generates Pareto data) allows for a quick test speed analysis of the whole wafer-level test, and identifies areas for potential improvement. Specific optimization techniques and trade-off considerations for the most common tests, such as leakage tests, threshold voltage measurements, and breakdown tests, were also discussed. Keithley applications engineers are available for consultation with S530 users and their test program needs.

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