

Gearing Up for Parametric Test's High Voltage Future

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Introduction

Many parametric test engineers are learning to cope with new high voltage process requirements. Not surprisingly, high voltage processes require high voltage parametric testing for process control and reliability monitoring. Part of the challenge lies in the fact that these new high voltage requirements *add* to the list of parametric tests rather than *replacing* some portion of it. In many if not most cases, the high voltage transistors are controlled by complex logic that requires low voltage/low current parametric test. Consequently, both high voltage and logic tests have to be addressed within the same test plan while minimizing impact on throughput.

How Did This Happen?

The IC industry has been delivering on Gordon Moore's prediction of doubling transistor density every 18 months and has done so for nearly half a century. As computing power soared, the need to integrate more of the product functionality into a single chip has led to concepts like "More than Moore." Whereas Moore referred to transistor density scaling, "More than Moore" speaks to scaling the circuit board down to a single chip. The power devices that once lived on the circuit board are increasingly integral to the IC itself.

One of the first areas to benefit from the "More than Moore" philosophy is power management. Power management comes in several flavors, including *smart* power management, *green* power management, and *integrated* power management. In every case, the combination of computational power, programmability, and high power driver circuits provide a platform to control and manage power and, consequently, to exercise control over the real world.

For example, let's consider Bipolar-CMOS-DMOS (BCD) technology. The term *BCD* is often used to describe a number of variants, including combinations such as

CMOS-LDMOS, NMOS-LDMOS, etc. The general case can be described as a single-chip IC that includes CMOS logic, as well as bipolar and DMOS driver circuits that support high current, high voltage, and high power control.

Most of yesterday's BCD technologies were limited to less than 100V. Although providing impressive performance, these devices are easily characterized with existing parametric test systems. Today, a class of BCD technologies have emerged that use LDMOS to support voltages as high as 700V or 800V, clearly showing an upward trend. These devices require special consideration when developing a parametric test strategy. It's expected that BCD technologies will exceed 1000V by about 2012. Such high voltage devices are currently used for applications such as High Intensity Discharge (HID) illumination, where a combination of high voltage and high power is needed.

There are a variety of applications for high voltage BCDs:

- Industrial controls (motor and actuator control)
- Automotive controls (lighting, engine control, drive train control, etc.)
- Advanced lighting (LED, HID, etc.)
- Power conversion and storage
- Display (backlight)

What Are the New Test Challenges?

Comprehensive CMOS process control monitoring (PCM) using parametric test (sometimes called e-test) involves measuring a suite of 50 or more parameters. This test suite is performed on a special test element group or TEG. A TEG includes representative devices and structures, such as transistors, diodes, capacitors, resistors, etc. These TEGs are most often located in the kerf or alley between ICs and are destroyed when the wafer is diced prior to packaging. When a technology or process is immature, a high percentage of the TEGs are measured. A mature process may require measuring as few as 15 of the TEGs per wafer cassette.

The first challenge associated with testing BCD technologies is that each device type (bipolar, CMOS, and LDMOS) requires a unique suite of tests. This nearly triples the number of tests needed and significantly increases the complexity of the TEG. The second challenge is that the LDMOS device or the power device must be tested at high voltage and sometimes using high current. This includes breakdown and leakage tests for devices that can withstand hundreds of volts. These tests require voltage levels well beyond the range of standard parametric test systems. Finally, the LDMOS device may require testing at up to 1A or 10 times the capability of the standard parametric tester.

Breakdown tests are not just a simple matter of testing a two-terminal dielectric structure. The off-state channel-breakdown and leakage must also be characterized. To perform this test, the gate has to be in a controlled state. This requires the use of a source-measure unit (SMU) on both the gate and the drain, with the drain attached to a high voltage SMU. As it turns out, the most likely failure mode during this test effectively shorts the drain to the gate. As a result, the SMU on the gate may be subjected to the full potential of the high voltage SMU connected to the drain, in which case, it will likely be damaged.

The final challenge is monitoring the reliability of the process. This means that both dielectric and device reliability information must be captured as early as possible to ensure timely process adjustments. This is typically done with wafer level reliability (WLR) test techniques. The goal of these tests is not to predict absolute product lifetimes but rather to detect trends in failure mechanisms related to process control. More often than not, fast tests like J-ramp and V-ramp breakdown tests are performed. These tests require voltages high enough to ensure failures, so they must exceed design targets by 20 percent or more. As a result, testing a 200V device is beyond the scope of a standard parametric test system.

High Voltage Test System Considerations

Standard parametric test systems are typically designed to support single-ended signals up to 100V and differential signals up to 200V. Consequently, these systems use signal paths that support up to 300V to 500V to ensure long-term performance and reliability. But what about 1000V applications? What is the consequence of using an under-rated probe card and interconnect in a high voltage application? Most often, the failure will be far from subtle and several instruments could be damaged in a single unfortunate incident. Certain probe card adapters (PCAs) and probe cards can support higher voltages if a pin wiring configuration that skips every other probe pin is used. This simple technique may double the effective voltage rating of the probe card and PCA. However, this technique cannot be universally applied to all probe cards and an engineering analysis is required to verify safe performance.

BCD and similar technologies require testing the CMOS logic at a few volts and few nano-amps while also supporting high voltage tests at up to 1000V or so. There are several ways to support this requirement:

- The least attractive strategy is to use dedicated high voltage testers and a standard parametric test system in a two-pass fashion. This two-pass strategy may also require using separate probe stations or physically reconfiguring the probe station between standard and high voltage operations. However, there are further complications to this approach. After the two-pass process is complete, the resulting test data must be merged to build a complete picture of the test results.
- The second strategy is to use dedicated pins with directional connections to the high voltage instruments. This limits flexibility and may force changes in TEG design or increase complexity by forcing additional prober moves, which would reduce throughput.
- The most attractive strategy to support this dynamic range is for the parametric test system to switch either standard or high voltage SMUs to *any pin*, as Keithley's Series S530 High Voltage Parametric Test System allows. This is done using a switch matrix that includes both high voltage and general-purpose signal paths. This allows for greater speed and flexibility and a single-pass scenario that reduces system complexity and the opportunity for human error.

As with all production tools, the high voltage parametric test system must be robust in terms of operator safety and system reliability. These goals are achieved with rigorous system engineering practices. System interlocks must prevent operators and instruments from being exposed to dangerous voltages. In addition, the system's low voltage instrumentation must be protected from damaging high voltages without compromising its low-level performance.

Test Plan Development

Given the special high voltage system considerations described already, it's unsurprising that high voltage testing also has an impact on test plan development. Even the most sophisticated system design can't protect the test structure or the system from poor test programming. To take a simple example, it is well-known that hot switching a relay reduces the lifetimes of the relay contacts. (*Hot switching* refers to opening or closing contacts with a potential applied.) At low voltages, hot switching might reduce contact life from 10^8 to 10^5 cycles. In an automated environment, this is problematic enough. However, in a high voltage regime, hot switching could reduce the relay contact lifetimes to 10^0 cycles—a *single closure*. Consequently, great care must be taken when creating a test plan to ensure the SMUs are sourcing zero volts prior to opening or closing any crosspoints in the switch matrix.

High Voltage Parametric System Roadmap

The roadmap for BCD technologies and related processes over the next two to five years clearly indicates the need to move beyond 1000V in parametric test. This will pose a number of challenges for high voltage parametric test systems. Instrumentation is likely the least significant of the challenges; however, probing at more than 1500V will almost certainly be much more challenging. High voltage switch matrix technology will also need to evolve to maintain the high flexibility and speed that modern production parametric test systems must provide.

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