Link Analysis and Interconnect/Cable Testing for High Speed Serial Standards

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Agenda

- ☞ Serial Data Network and Link Analysis Applications
- Serial Data Network Analysis and Cable Testing
- Serial Data Link Analysis and Jitter, Noise and BER Measurements
- Summary

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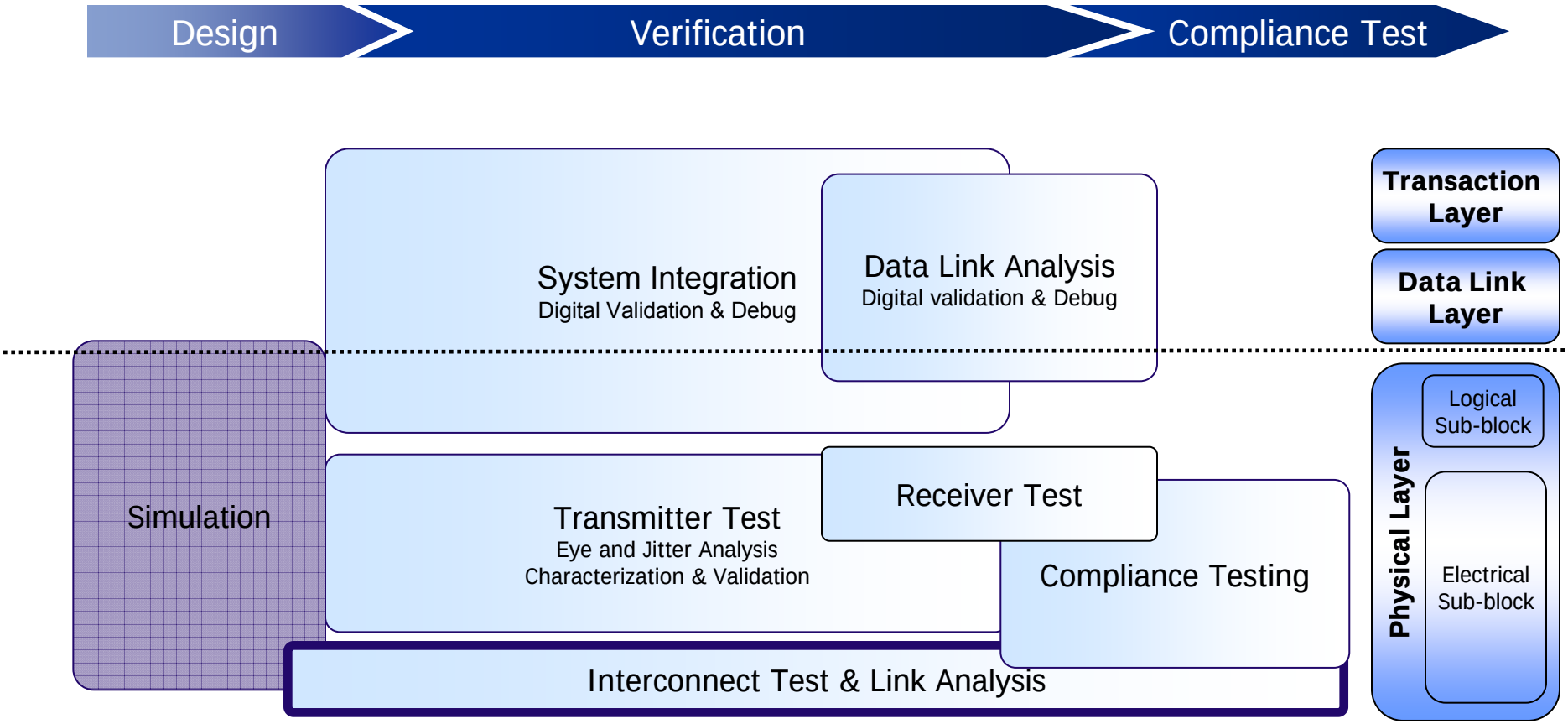
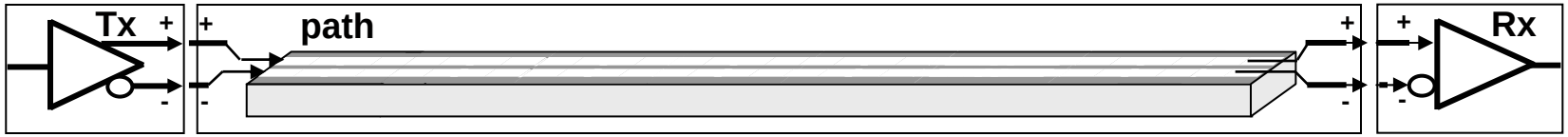
High Speed Serial Test Challenges





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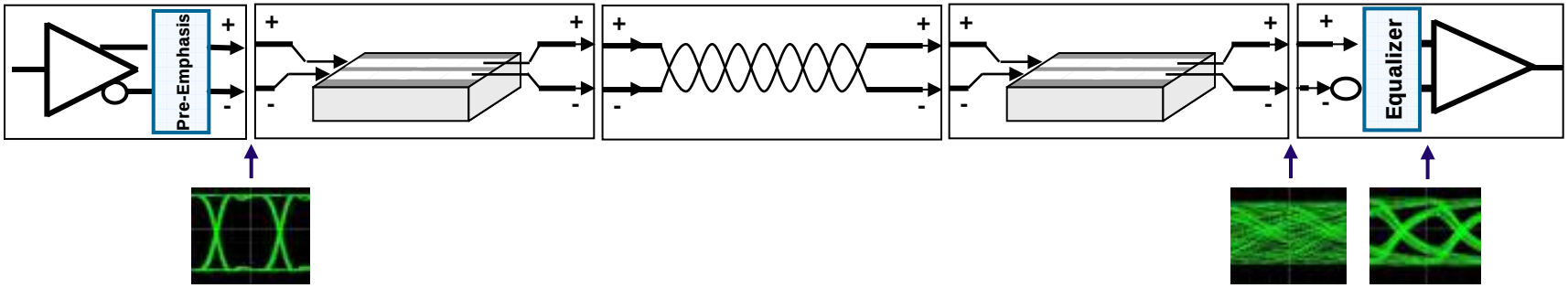
Market Dynamics

- 2nd & 3rd Gen HSS standards deploying
- Faster data rates and low level signals
- Understanding HF losses is critical

Standard	Data Rate
SATA Gen III	6 Gb/s
SATA Gen II	3 Gb/s
PCI Express 1.0	2.5 Gb/s
PCI Express 2.0	5 Gb/s
DisplayPort	2.7 Gb/s
HDMI 1.3	0.75 Gb/s to 2.25 Gb/s
FC 1, 2, 4 Gb/s	1 Gb/s to 4.25 Gb/s
FB-DIMM II	4.8-9.6 Gb/s
FibreChannel	4.25-8.5 Gb/s
10GE Ethernet	10.3125 Gb/s



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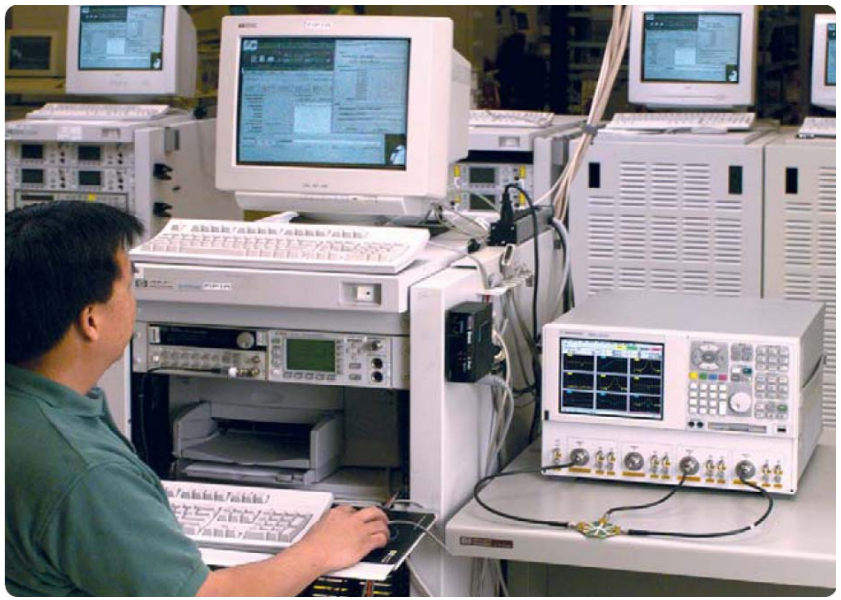
Serial Data Network Analysis Application

- Time and frequency domain analysis, compliance testing of differential interconnects for data rates from 1 Gb/s to 10 Gb/s, and beyond
- Needs:
  - Accurate and repeatable impedance and S-parameter measurement results
  - Validate design performance
  - Verify standards compliance
  - Minimize test cost
  - Minimize test time
- Traditional S-parameter measurement methods – Vector Network Analyzers
- Modern S-parameter measurements – using TDR



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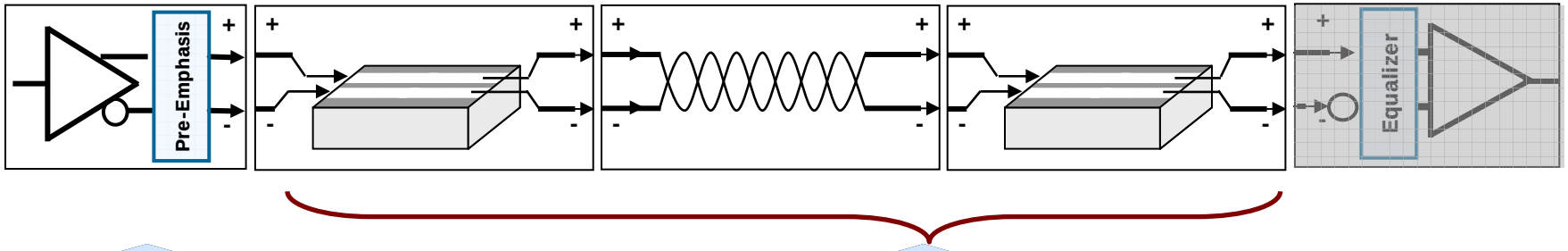
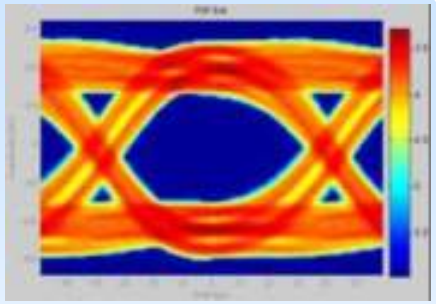
Design Dynamics: Interactions Between Tx and Channel



Transmitter Analysis

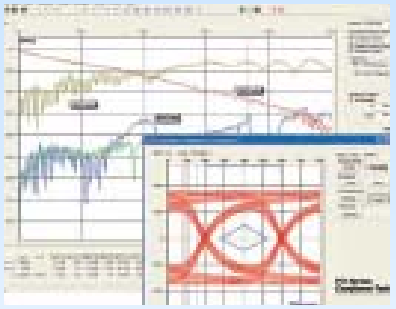
Jitter separation
Noise separation
Eye Contour and
BER Eye



- Characterization of the transmitter…

Network Analysis

Impedance measurements
Insertion & Return Loss
Cross Talk characterization



- Characterization of the network (channel) through TDR and S-Parameters

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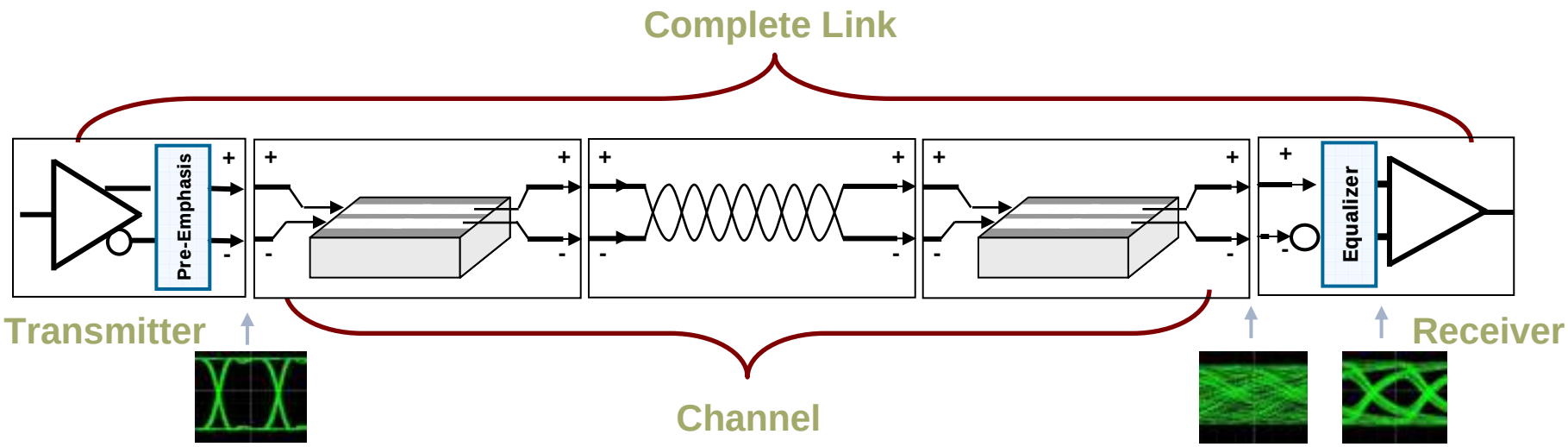
Emerging Serial Data Link Analysis Application



- Traditional measurement techniques are inadequate – e.g., measuring transmitter or receiver alone is insufficient
- Must understand interactions between transmitter, channel and receiver
- Equalization employed to compensate for signal loss at speeds >2.5 Gbs
- Must understand pre-emphasis effects at the transmitter output
- Need to understand effects of measurement systems (e.g., probing)
- Channel performance does not easily scale with transmitter/receiver performance
- Spread Spectrum Clocking (SSC) is emerging in low-cost standards

Complete Link Needs to be Considered – Need for Serial Data Link Analysis

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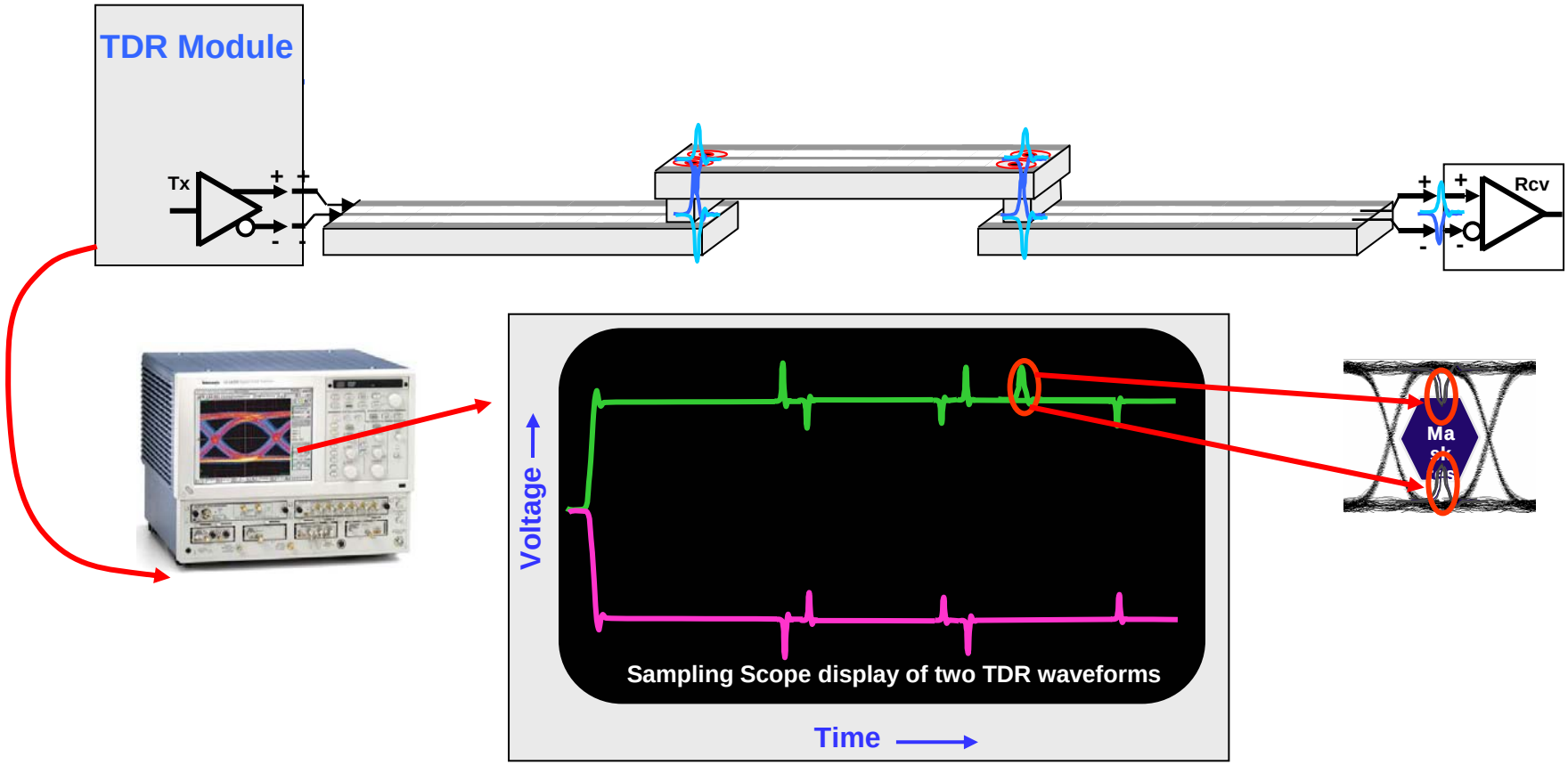
Network Characterization: Time-Domain Reflectometry (TDR)



Common TDR Measurements:

- Impedance
- Delay
- Intra-pair skew
- Inter-pair skew

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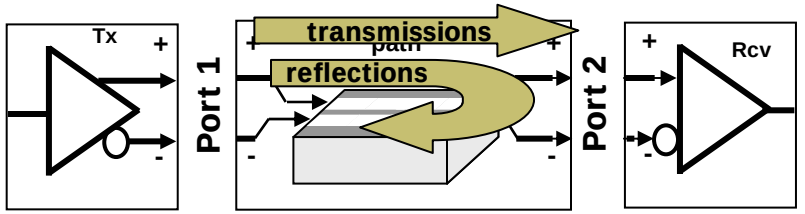
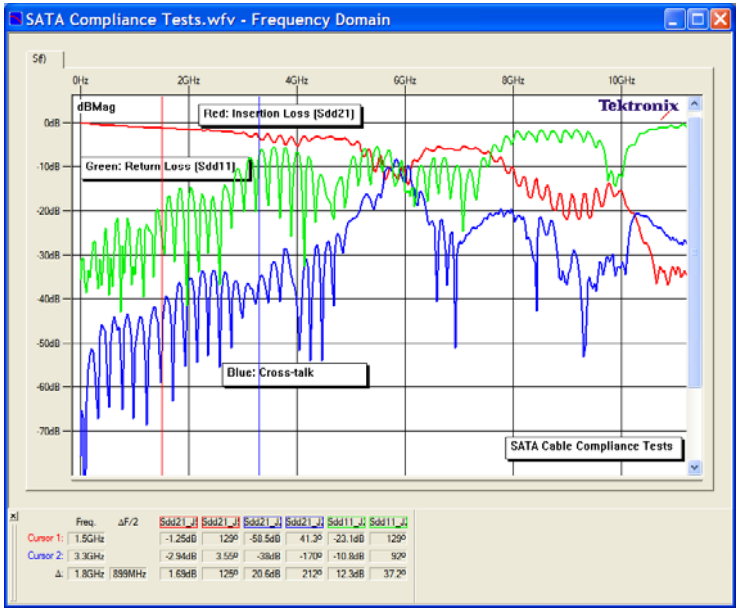
Network Characterization: S-Parameters

Frequency-domain characterization of reflections and loss in a network



Quantitative insight into the causes of signal integrity problems



Common S-parameter Measurements:

- Differential return loss
- Differential insertion loss
- Frequency domain crosstalk

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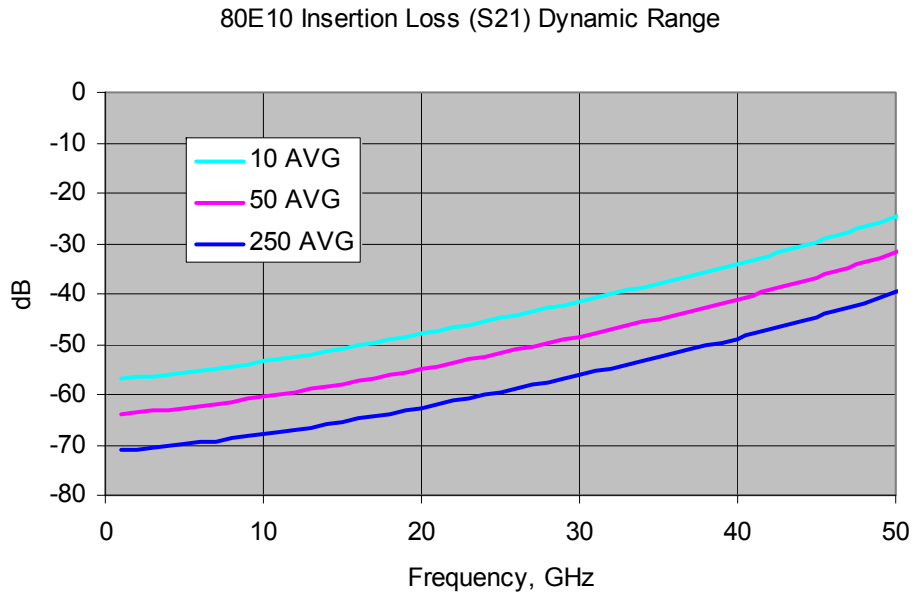
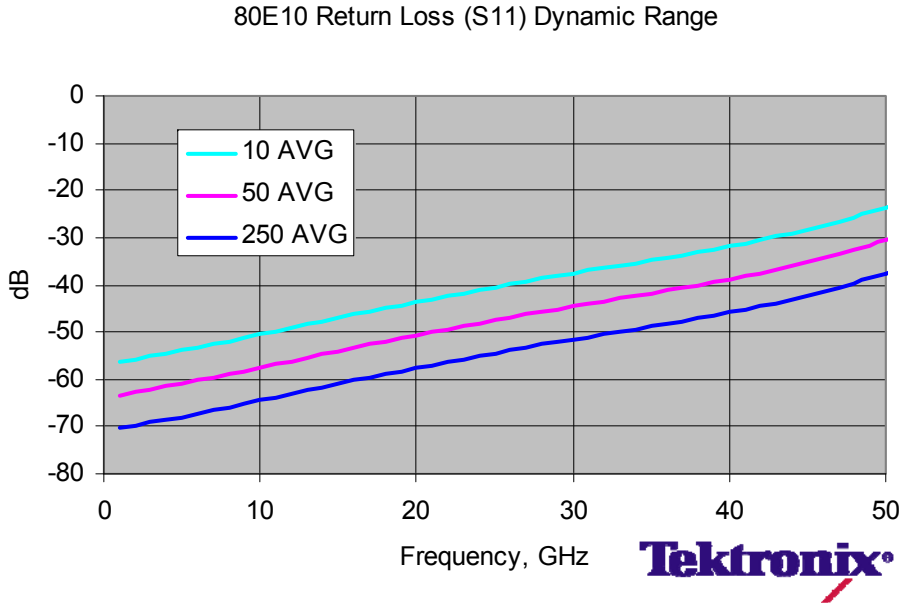
Dynamic Range for Insertion Loss and Return Loss

- -70 dB at DC, -40 dB at 50 GHz
- Best dynamic range with:
  - More points
  - More averages
  - Shorter acquisition window
- Dynamic range for insertion loss (S_{21}) is a thru measurement without connection between ports
- Dynamic range for return loss (S_{11}) is a reflection measurement of a precision 50 Ohm termination





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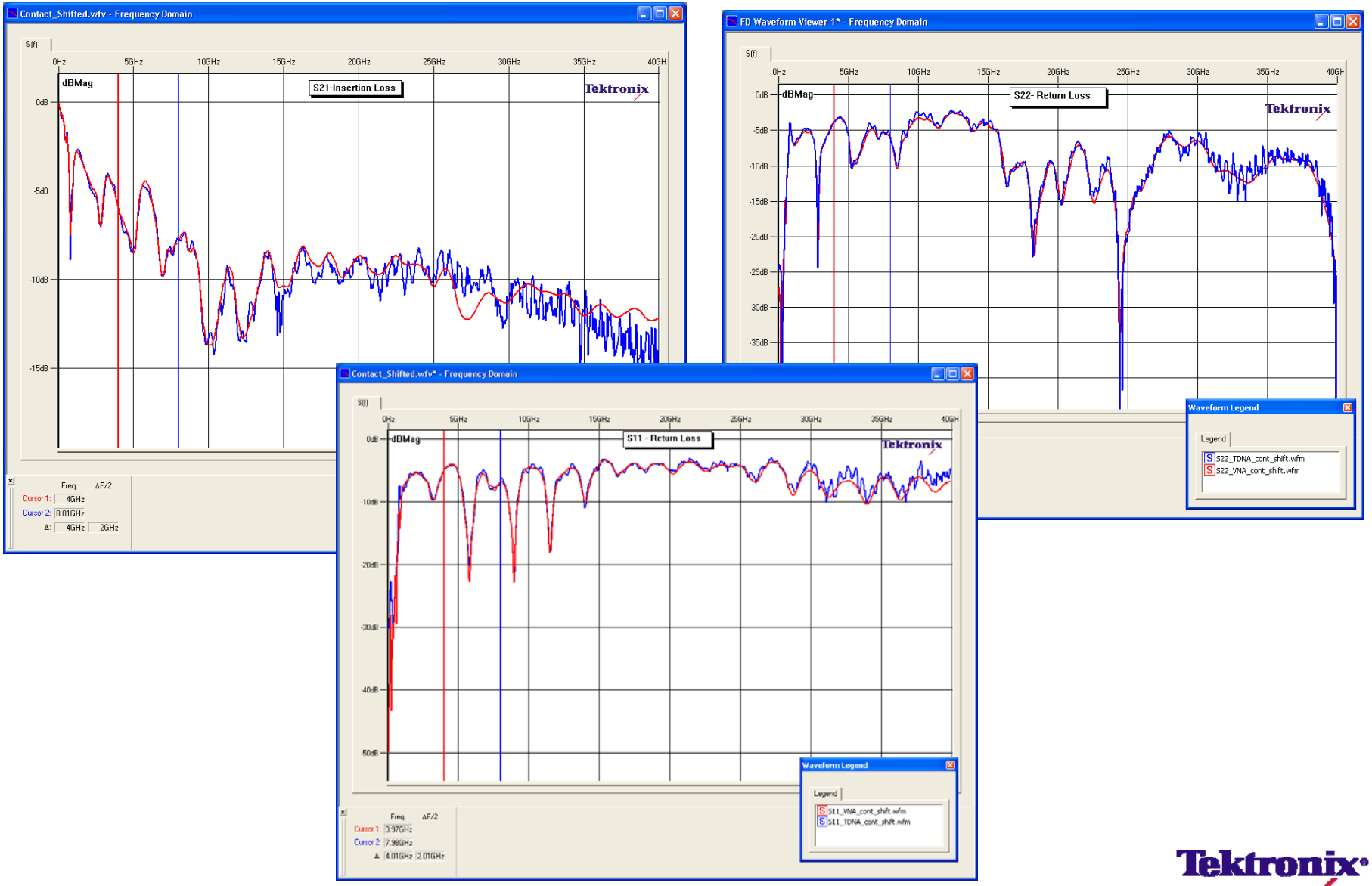
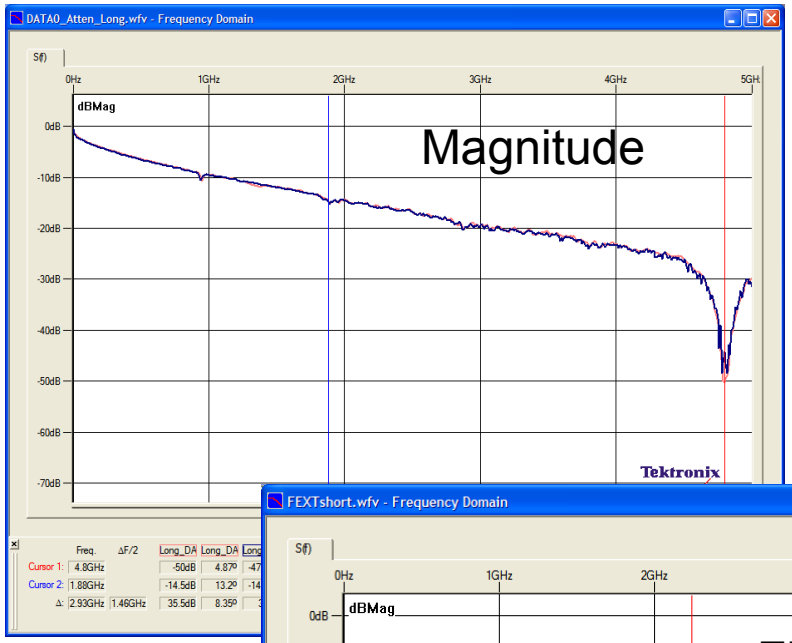
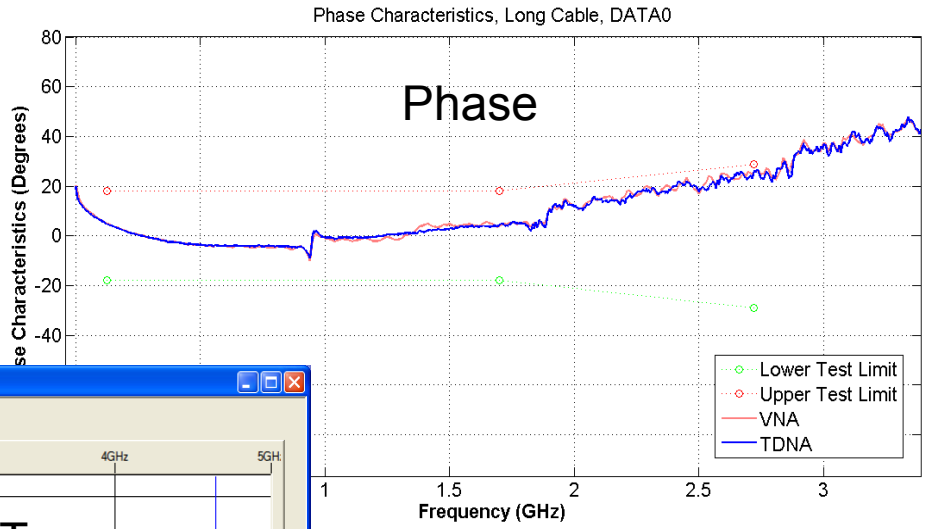
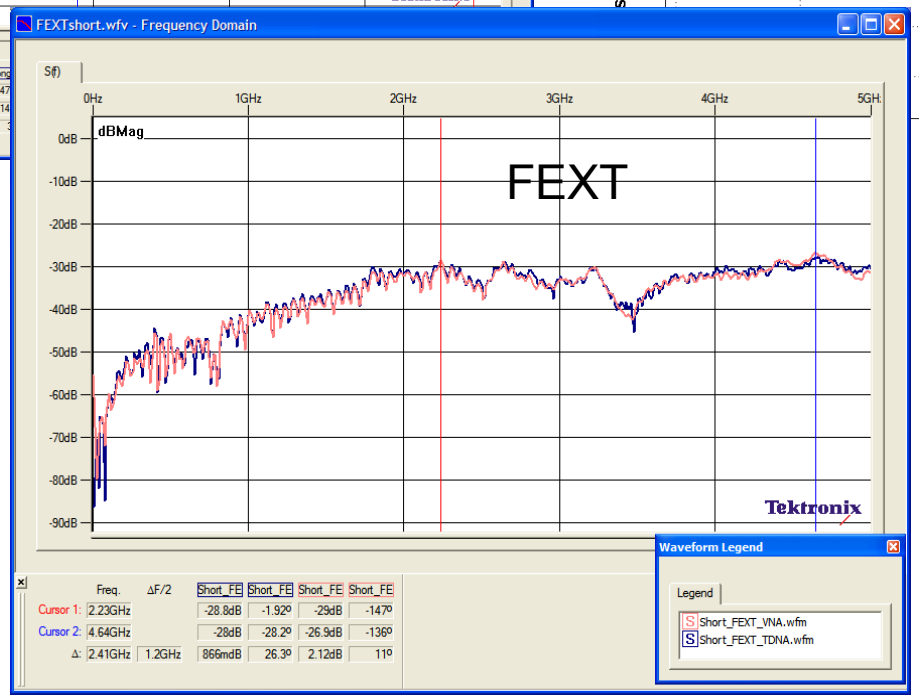
TDR-VNA S-parameter Correlation (40GHz)



HDMI Cable Example (with VNA correlation, 5 GHz)







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Compliance Test: Fit To Customer Needs

Standard	Data Rate	TDR	Required Frequency Domain Measurements			Lowest Measurement Level	Measurement Bandwidth Range
			Differential Return Loss	Different. Insertion Loss	Differential Crosstalk		
✓SATA Gen 2	3 Gb/s	★	★	★	★	-26 dB	100 MHz to 5 GHz
✓PCI Express	2.5 Gb/s	★	★	★	-	-10 dB	500 MHz to 3.75 GHz
✓HDMI	3.4 Gb/s	★	★	★	★	- 54 dB[1]	100 MHz to 2.5 GHz
✓FC 1, 2, 4 Gb/s	0.75 Gb/s to 4.25 Gb/s	★	-	★	★	-30 dB	300 kHz to 4.125 GHz
✓FB-DIMM II	1 Gb/s to 4.25 Gb/s	★	★	★	-	-20 dB	100 MHz to 8 GHz
✓Infiniband	5 Gb/s	★	★	-	-	-8 dB	100 MHz to 3.2 GHz
✓XAUI	2.5 Gb/s	★	★	★	-	-10 dB	Up to 1.25 GHz
✓10 GigE	3.125 Gb/s	★	★	★	★	-32 dB	100 MHz to 2 GHz

[1] -54 dB at low frequency only, well within the performance range of 80E10

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Real Advantages vs Perceived Issues

TDR-Based Solution vs. VNA

- TDR-Based Solution Advantages:
  - Ease of calibration, and consequently…
    - Fast throughput
    - Ease of use
    - Easy fixture de-embedding – critical for compliance testing
  - 25%-35% lower cost for differential serial data application requirements
- Perceived Issues w/TDR-Based Solution
  - Lower dynamic range
    - Up to 70dB for TDR-based vs. up to 100 dB for traditional VNA
    - 70dB is perfectly suitable for serial data applications
      - typical measurement is in -10 to -40dB range

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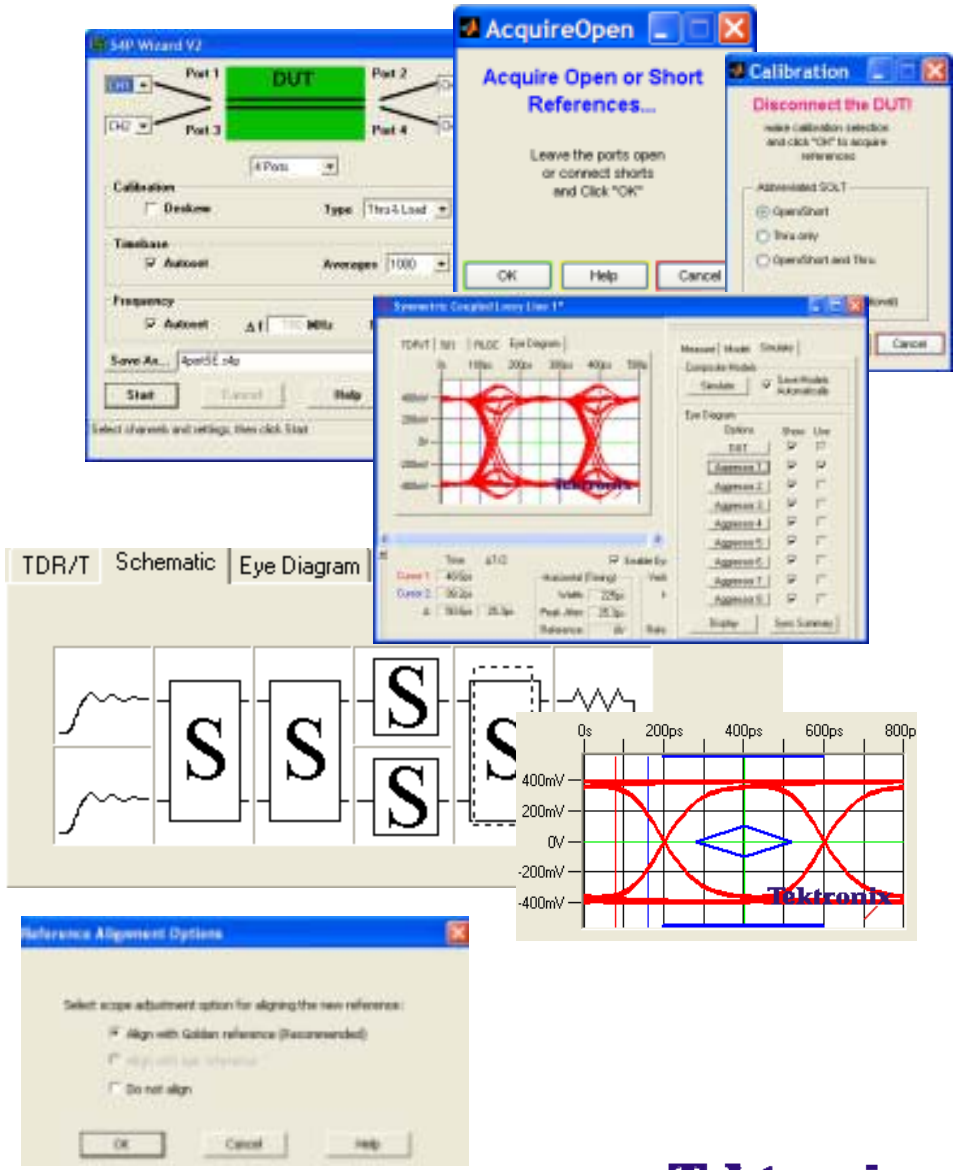
IConnect® Software Unique Capabilities

- Automated data collection using scripts for SDNA
  - For serial data standards – or Touchstone output
- Eye diagram – including crosstalk effects and equalization
  - Standard-defined compliance testing and channel analysis
- Complete channel simulation using Link Simulator
  - *Measurement based, no Spice models required*
  - Combine 5 backplanes and 5 cables and choose the best performing combination in minutes instead of hours or days
  - Not for Tx/Rx simulation
- EZ Z-line UI for efficient fault isolation



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- ✓ Serial Data Network and Link Analysis Applications
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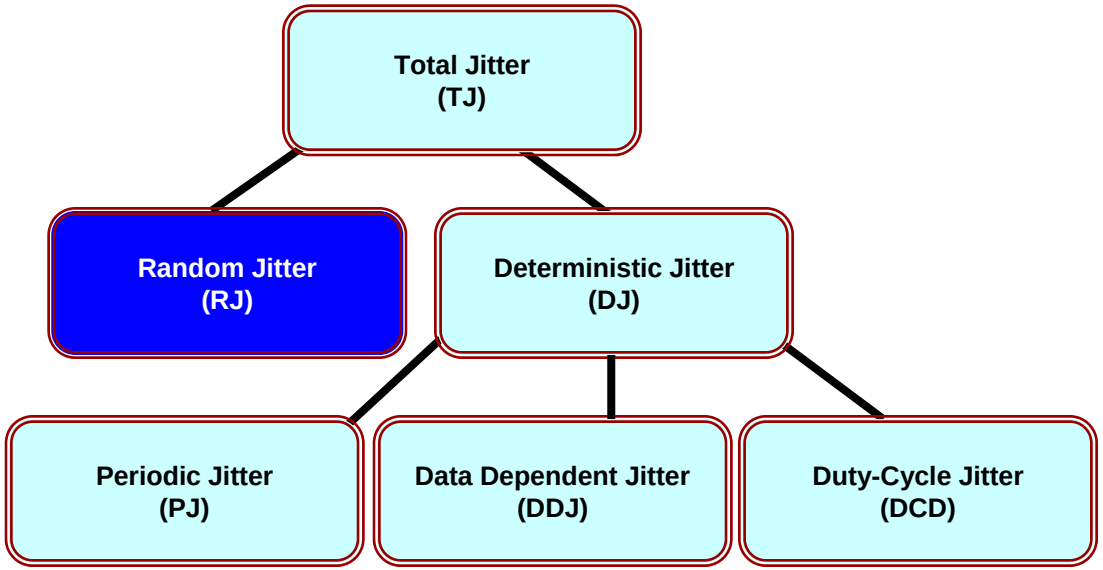
The Case for Jitter Analysis

- The case for Jitter analysis has been accepted industry wide
  - Separating jitter into its constituent components provides increased precision and insight into root cause of BER performance



Constituent Components of Jitter

= Unbounded

= Bounded

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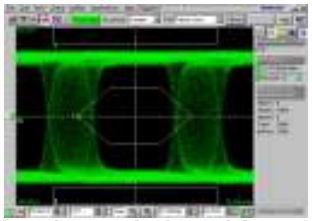
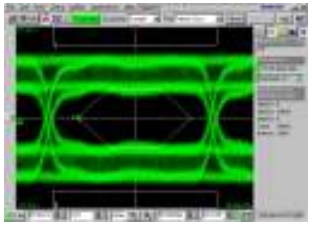
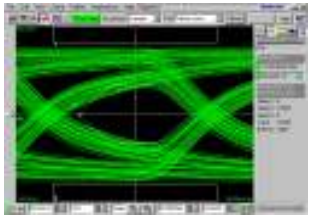
The Cause for Jitter and Noise and BER Analysis



Jitter dominated signal impairment



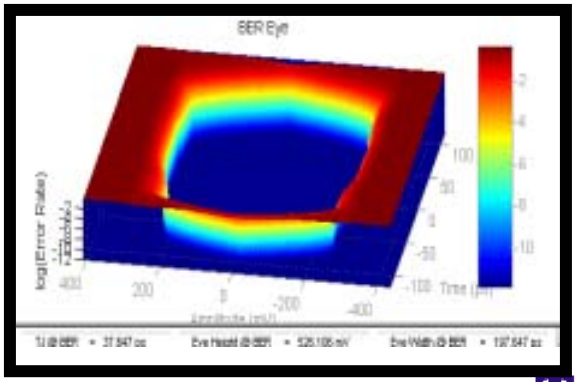
Noise dominated signal impairment



Jitter & Noise signal impairment

- BER of a link is limited by just Jitter
  - Jitter separation leads to insight into root cause
  - BER extrapolations and bathtub curves are accurate
- Sometimes it is **noise** that dominates the BER
  - Jitter separation provides very little insight into root cause of BER performance
- Often it is limited by both Jitter and Noise
  - Jitter separation provides only a limited answer

- 80SJNB: Jitter and Noise Separation and Accurate BER Extrapolation



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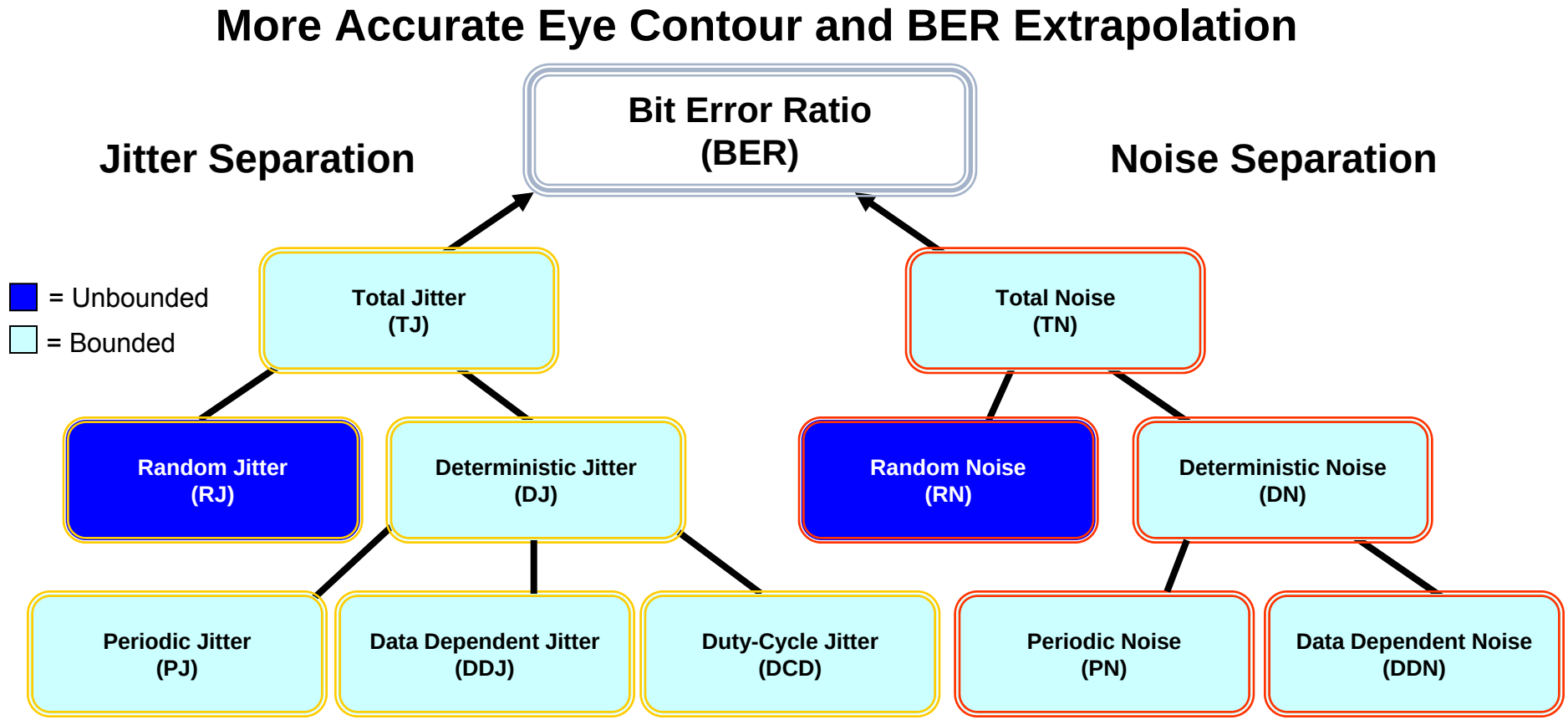
More Accurate BER Analysis



80SJNB the FIRST oscilloscope solution to TOTAL BER analysis!

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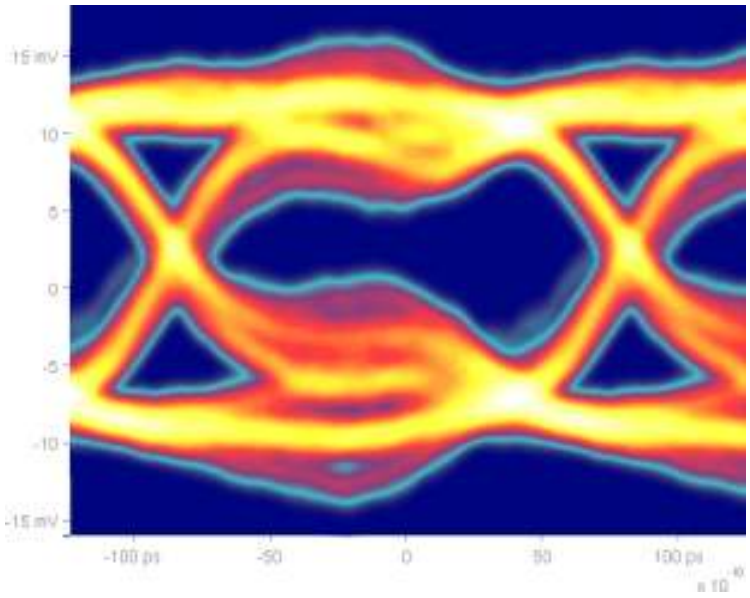
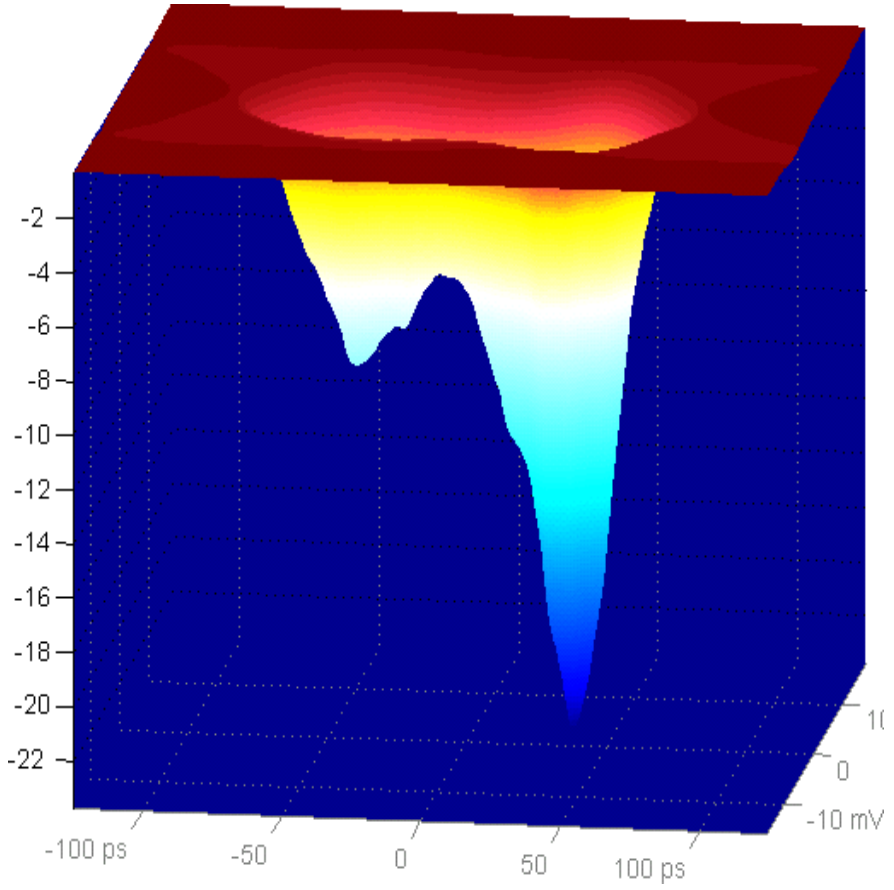
The Breakthrough in Serial Data: PDF Eye, BER Eye

- Jitter and Noise separation provides crucial new understanding of a data link's BER
  - Statistical Eye diagrams describing the probability of the signal across the eye
  - Jitter-only solution do not give accurate BER predictions





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80SJNB Advanced Jitter, Noise and BER Analysis Software

Jitter and Noise Results

Measurement	Description
TJ @ BER	Total jitter @ BER
RJ	Random jitter
RJ (h)	Horizontal component of random jitter
RJ (v)	Vertical component of random jitter
RJ (δ-δ)	Random jitter computed in the dual Dirac model
DJ	Deterministic jitter
DDJ	Data dependent jitter
DDPWS	Data Dependent Pulse Width Shrinkage
DCD	Duty cycle distortion
DJ (δ-δ)	Deterministic jitter computed in the dual Dirac model
PJ	Periodic jitter
PJ (h)	Horizontal component of periodic jitter
PJ (v)	Vertical component of periodic jitter
EOH @ BER	Horizontal eye opening @ specified BER

Measurement	Description
RN	Random noise
RN (v)	Vertical component of random noise
RN (h)	Horizontal component of random noise
DN	Deterministic noise
DDN1	Data dependent noise on logical level 1
DDN0	Data dependent noise on logical level 0
PN	Periodic noise
PN (v)	Vertical component of periodic noise
PN (h)	Horizontal component of periodic noise
EOV @ BER	Vertical eye opening @ specified BER

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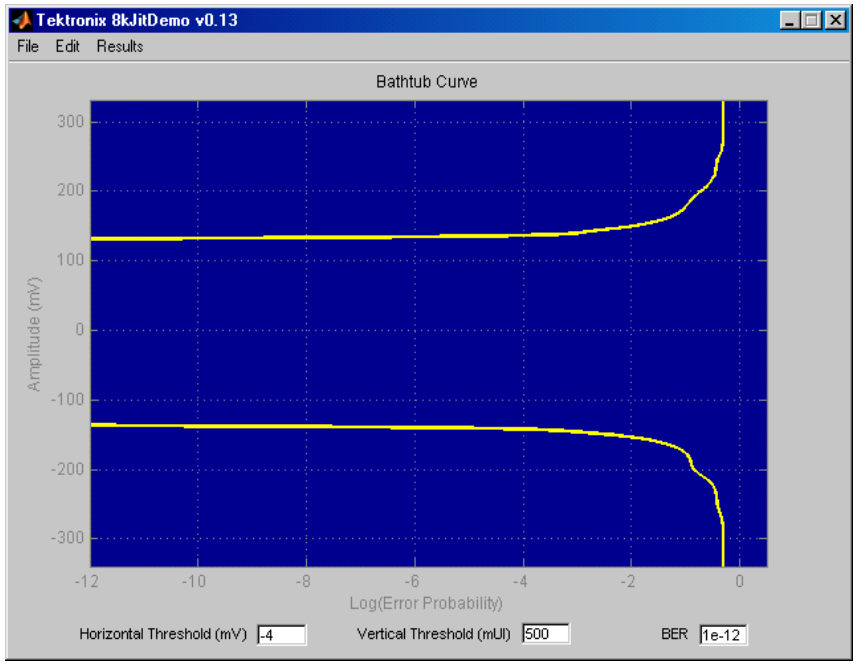
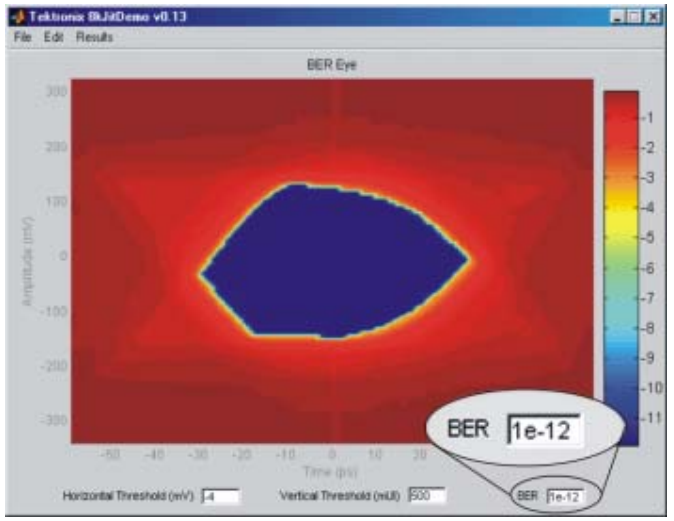
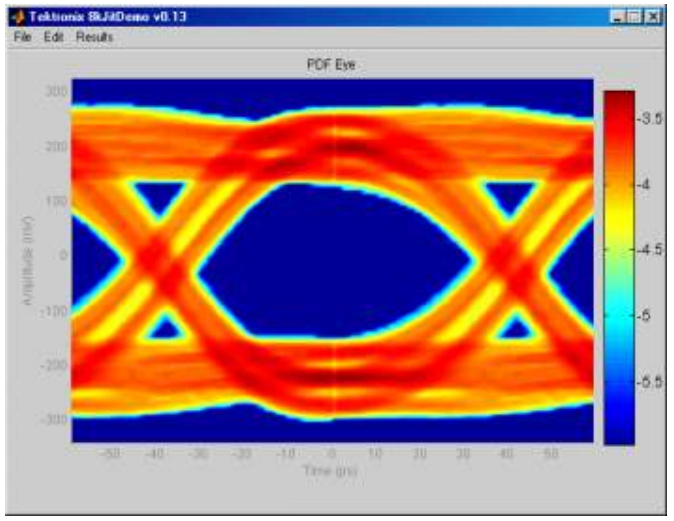
80SJNB Results Overview

Computed Horizontal and *Vertical* Bathtub, BER-Eye view, Contours view, and others.







Whatever should be measured, plot or calculated – if its serial data 80SJNB has the answer.

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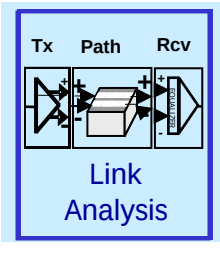
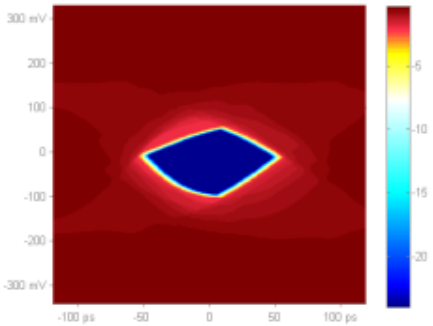
The Foundation for Serial Data Link Analysis

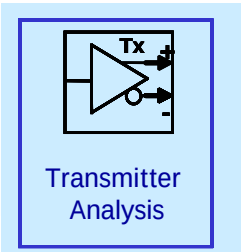
- Serial Data Link Analysis
  - Combined transmitter & channel analysis for virtual view at the receiver
  - Impairment compensation with Equalization and Emphasis

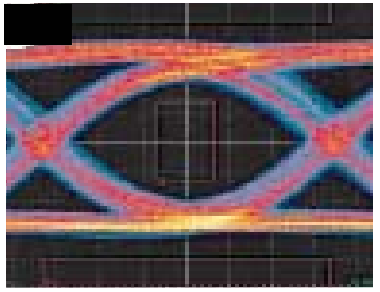




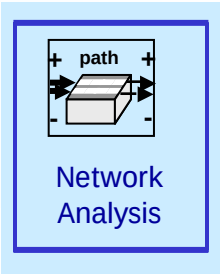
Builds on and incorporates:

- Transmitter Characterization
  - Jitter separation
  - Noise separation
  - Eye Contour and BER Eye





- SDNA For Channel Characterization
  - Impedance measurements
  - Insertion & Return Loss
  - Cross Talk characterization



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Pre-/De-Emphasis, Equalization, & SSC in High Speed Standards

	Data rate [Gbps]	Pre- / De-emphasis in Tx	Equalization: FFE only:☆ FFE/DFE:★	Spread Spectrum Clocking (SSC)
SATA Gen 2	3	-	-	-
SATA Gen 3	6	★	★ Opt.	★
PCI Express 1.0	2.5	-	-	★
PCI Express 2.0	5	★	★ Opt.	Opt.
USB 3.0	5	★	-	★
FibreChannel	<4.25	-	-	-
FibreChannel	8.5	★	★	-
XAUI	3.125	★	-	-
10GE Ethernet LRM (Multi-mode fiber)	10.3125	-	★	-
10GE Ethernet KR (backplane)	10.3125	★	★	-
SFP+ Interconnect	8G, 10G	★	★	-

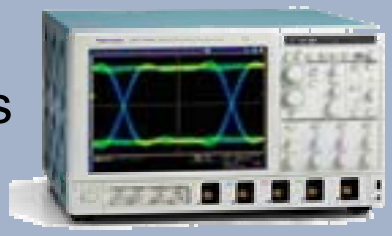
One High Performance Oscilloscope Does not Fit All High-End Applications

System

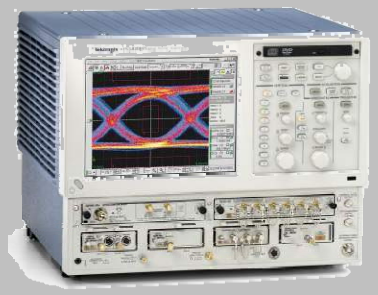
Add-In Cards

Chip

Real-time Scopes



The most versatile tool for all areas of high-speed digital and analog applications



Sampling Scopes

For applications that place top priority on waveform precision

R&D

Verification/Compliance

Manufacturing

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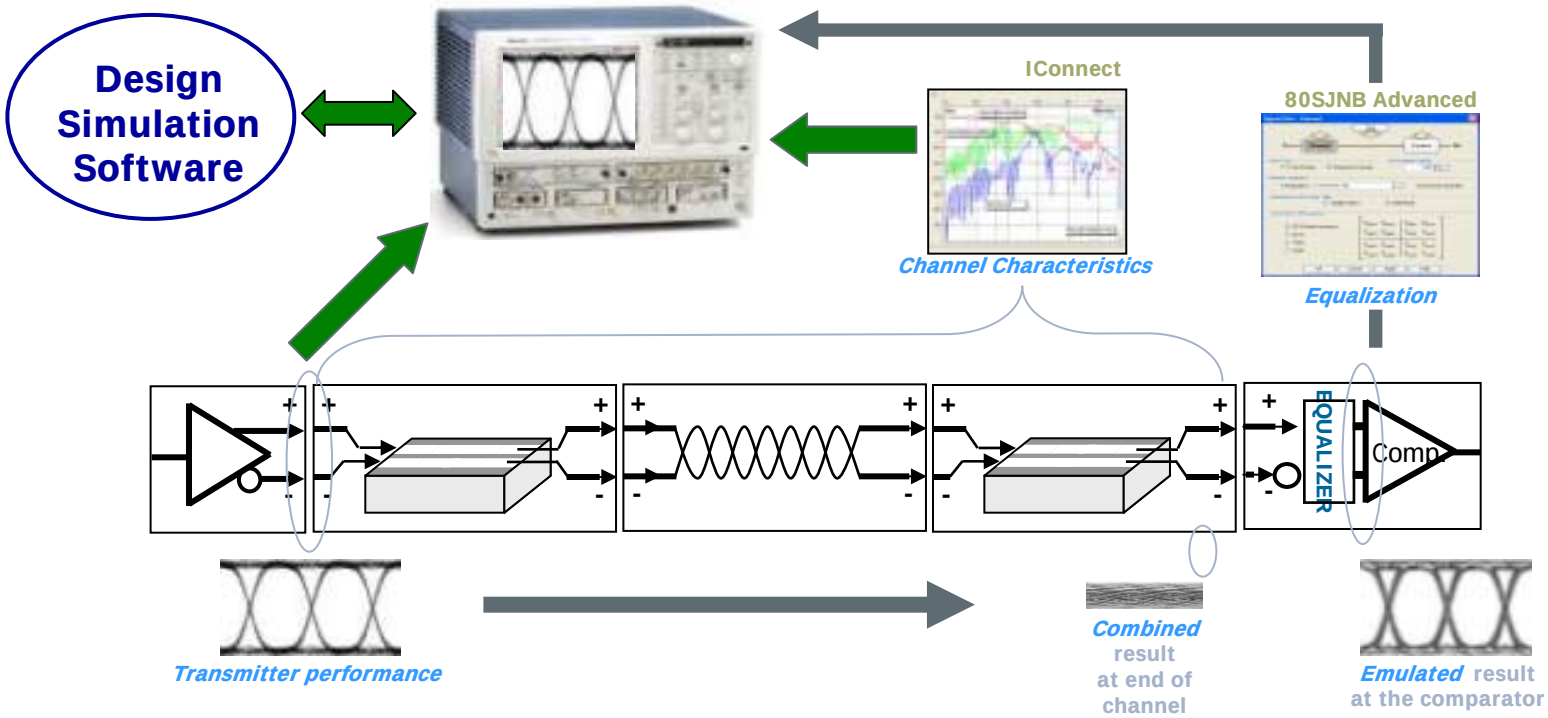
Serial Data Link Analysis Tool for DSA8200



- Characterization of the channel (network)
- Characterization of the transmitter
- Emulation of the waveform at the receiver; output to simulation software
- Closed loop analysis and correction, from transmitter to receiver

Most Complete SDLA Solution In the Industry

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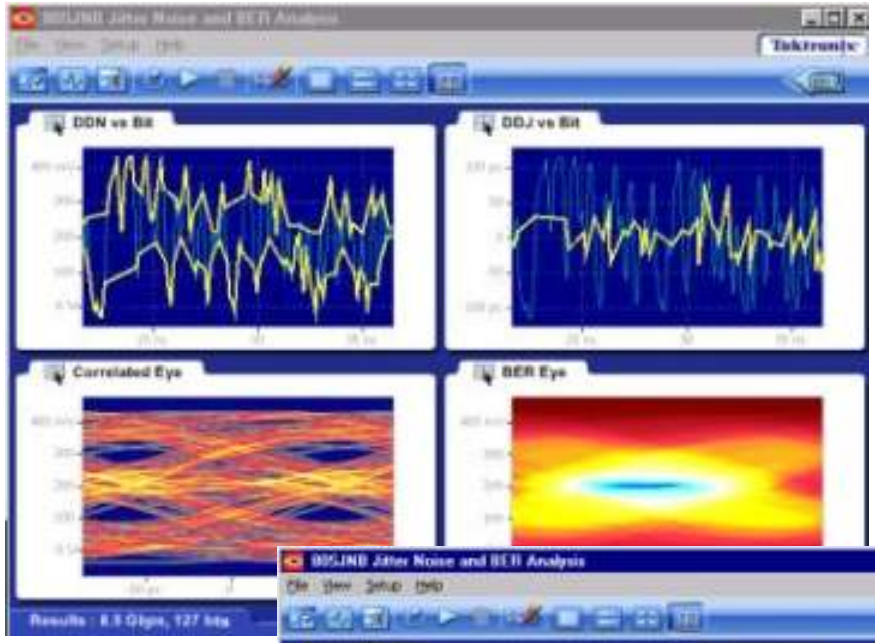
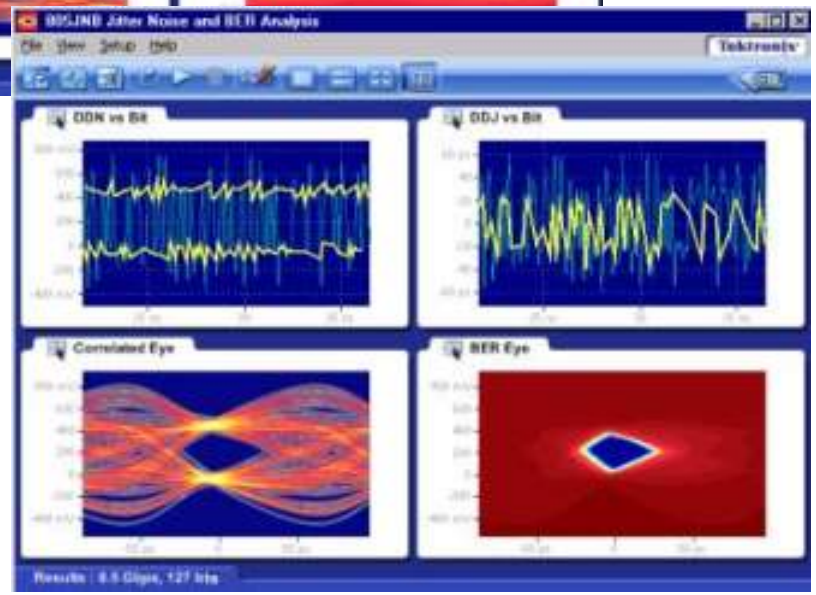
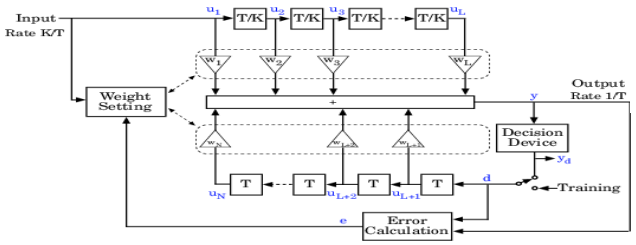
80SJNB Advanced: Equalization Effect

- 8.5 Gb/s Signal Without Equalization….



- … and with FFE/DFE Equalization





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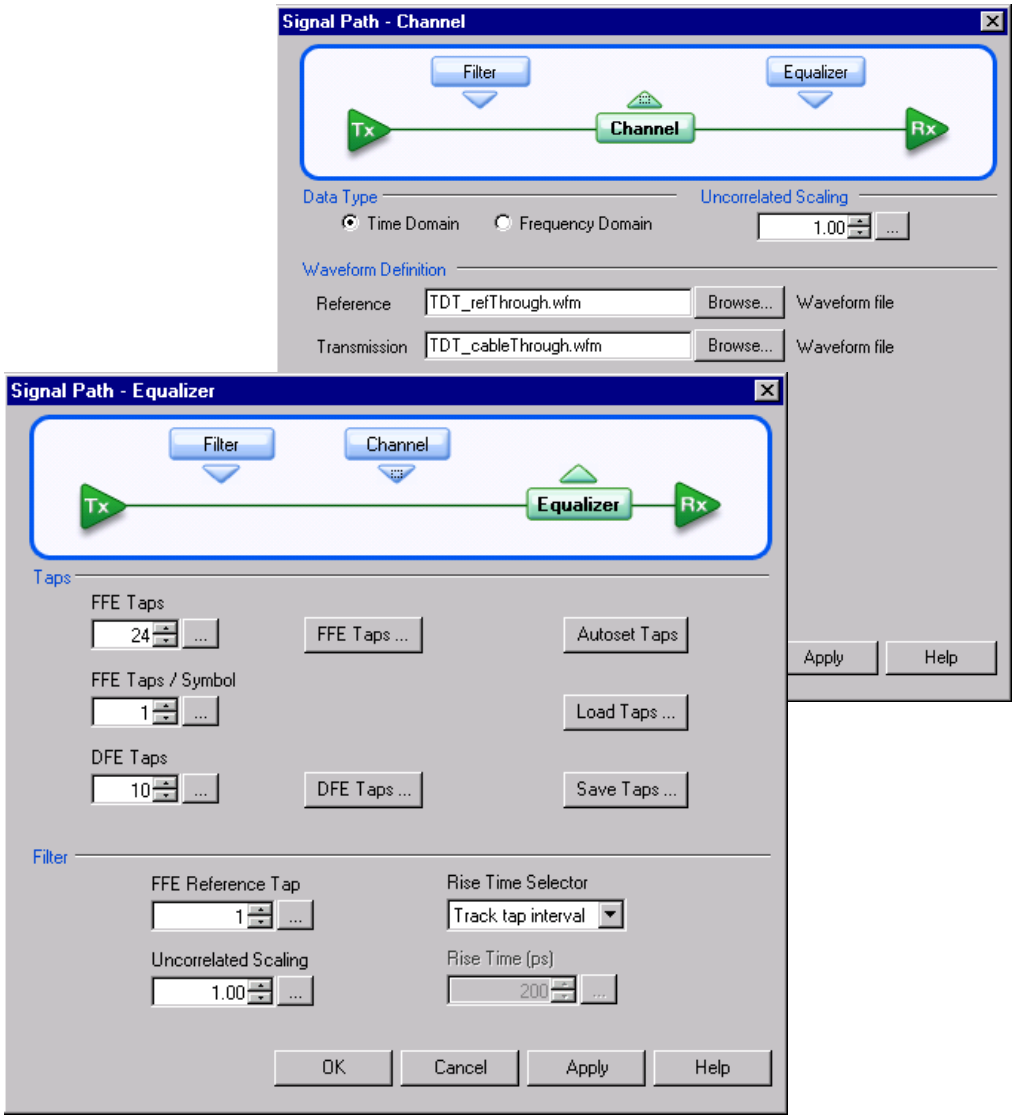
80SJNB Equalization, Channel Emulation

- Emulate channel effects using Touchstone S-parameter or TDR/T data
- Max FFE taps – 100
  - FFE taps per UI – 1, 2, 5, 10
- Max DFE taps – 40
- Ability to “Autoset Taps” to minimize noise
- Delay FFE filter using “FFE Reference Tap”
- “Rise Time Selector” to emulate effects of DFE path
  - Defines a Gaussian filter
  - T_{rise} defaults to 20% of UI



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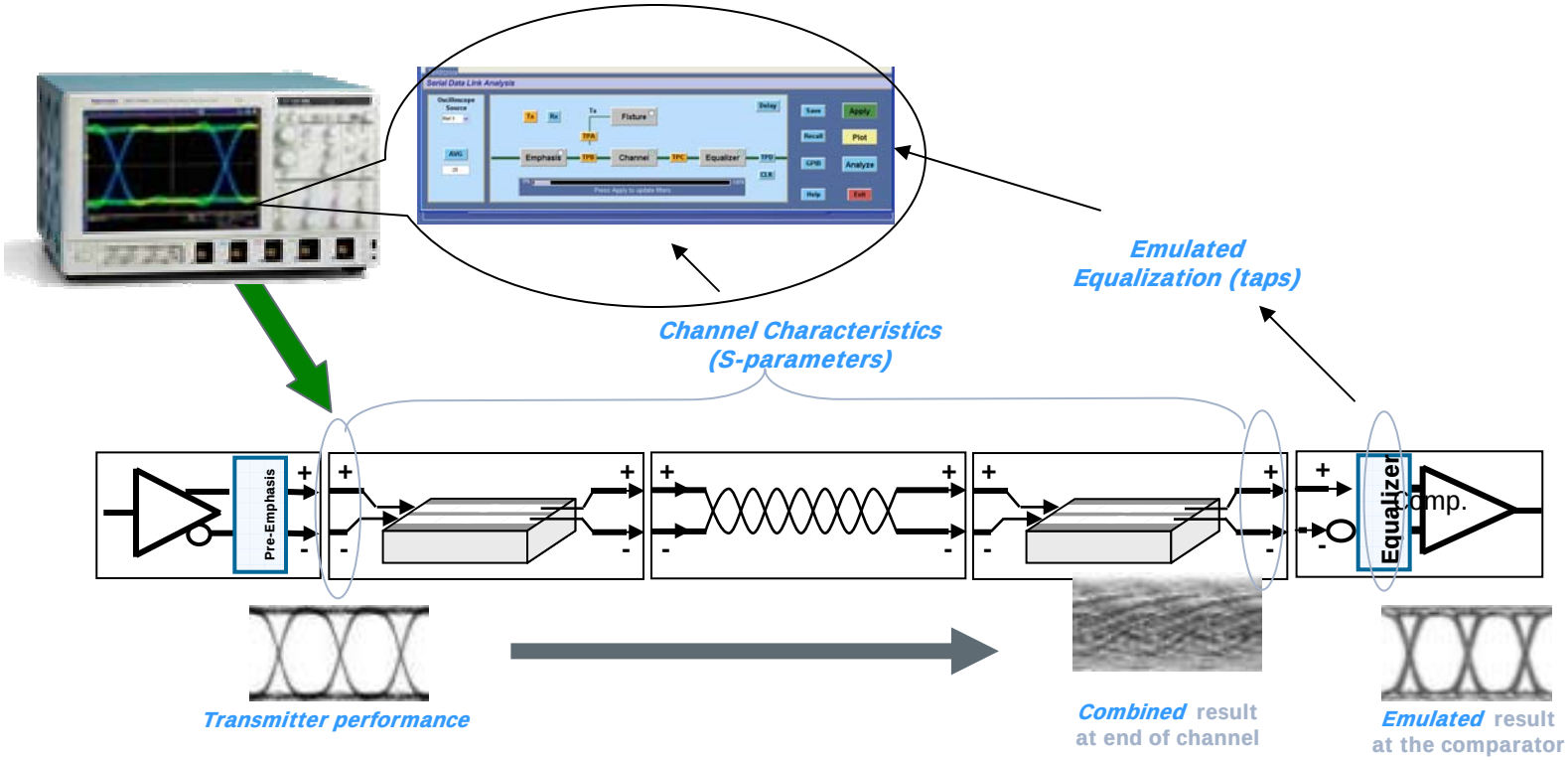
Introducing Serial Data Link Analysis for DSA/DPO70000



- Characterization of the transmitter
- Emulation of the waveform at the receiver; including effects of the channel and equalization
- Remove the effects of the test fixture

Complete SDLA Solution for Real Time

Precise – Insightful - Flexible

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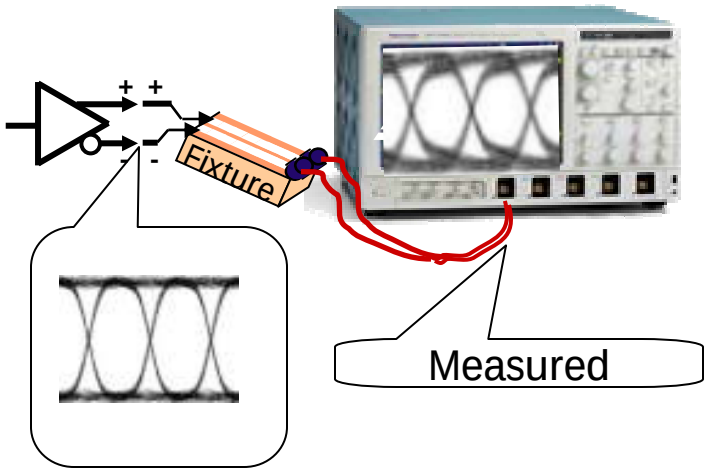
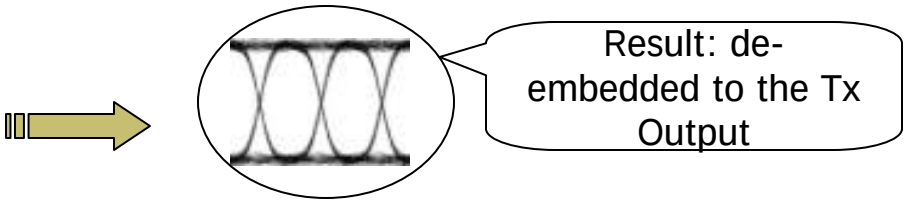
De-embed test fixture (probing) on DSA/DPO70000

- When measuring the signal, the fixture impacts the result
- What does the signal look like at the Tx, without fixture?





- Measure the Fixture (with TDR, VNA, etc and generate the S parameters: *.S1p (S21),*.S2p or *.S4p (SE or Diff)
- In SDLA: Select “Fixture”. Import the S parameter file. Select a reasonable filter bandwidth (for the inversion)
- Debug the results created in frequency and time domain

Note: Model does not support return loss

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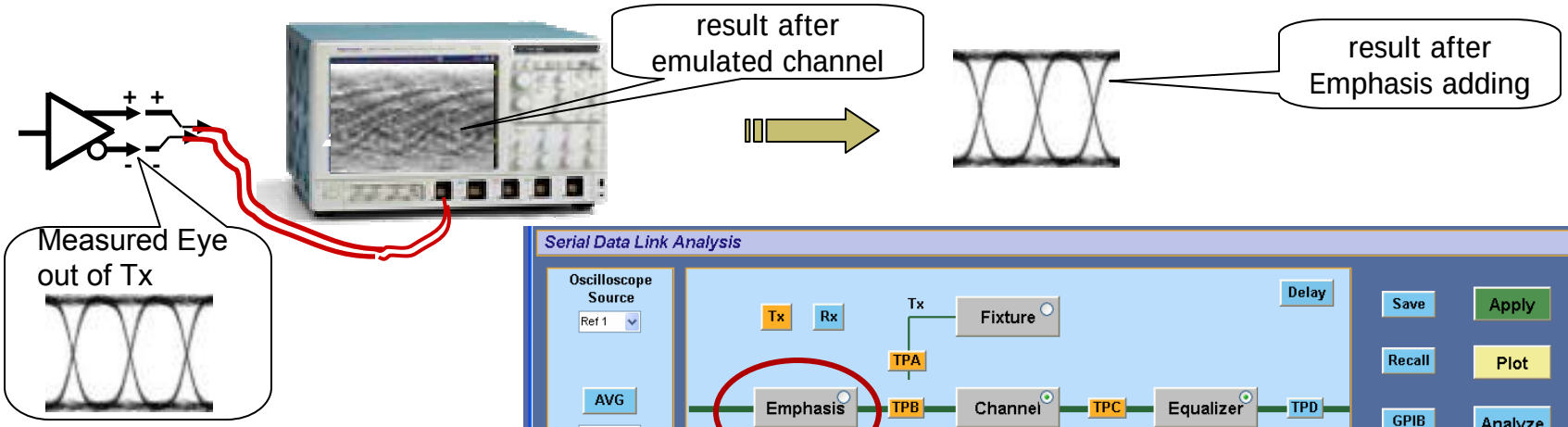
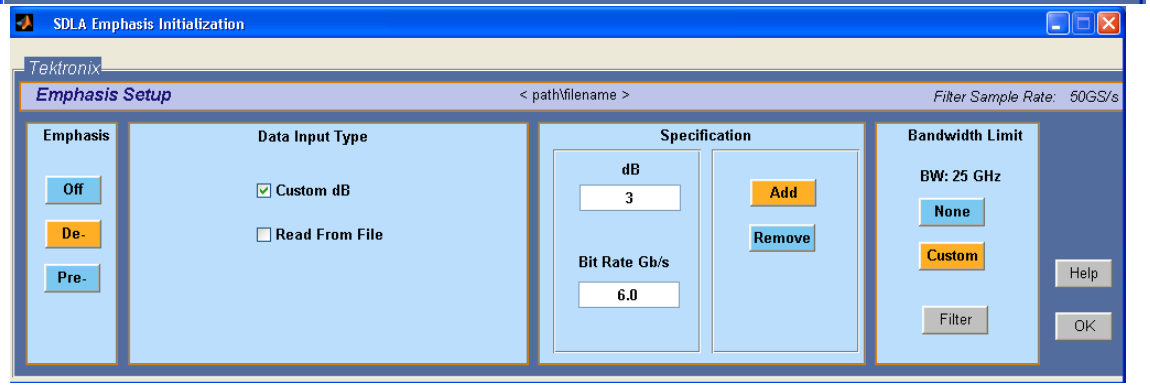
De/Pre-emphasis – add/ remove emulation

- When measuring the signal after the emulated channel
- What would the signal look like at the Rx, with Emphasis?

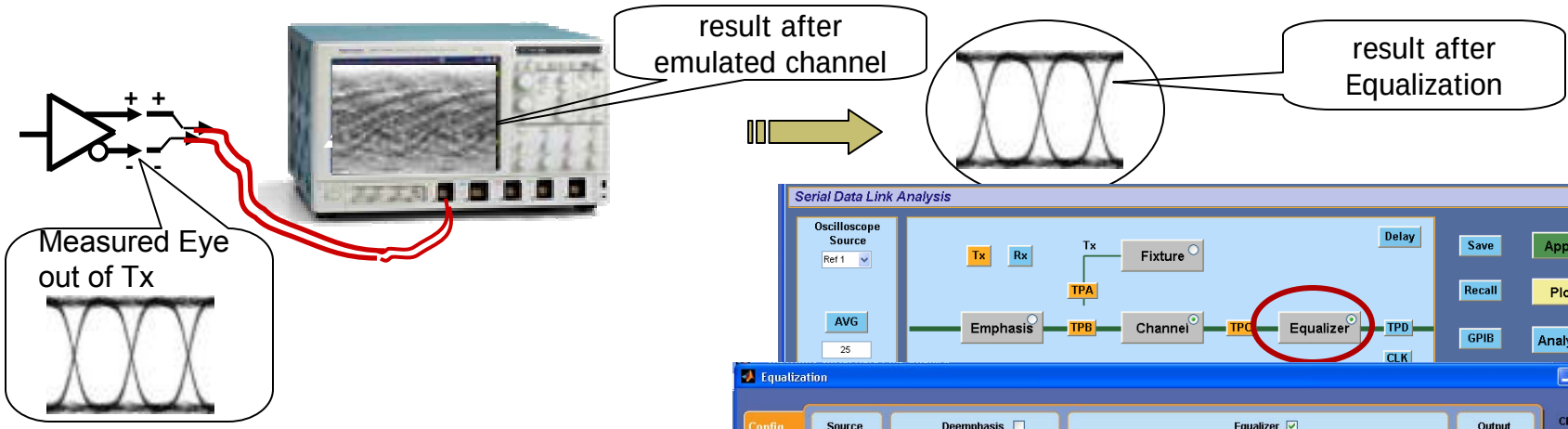


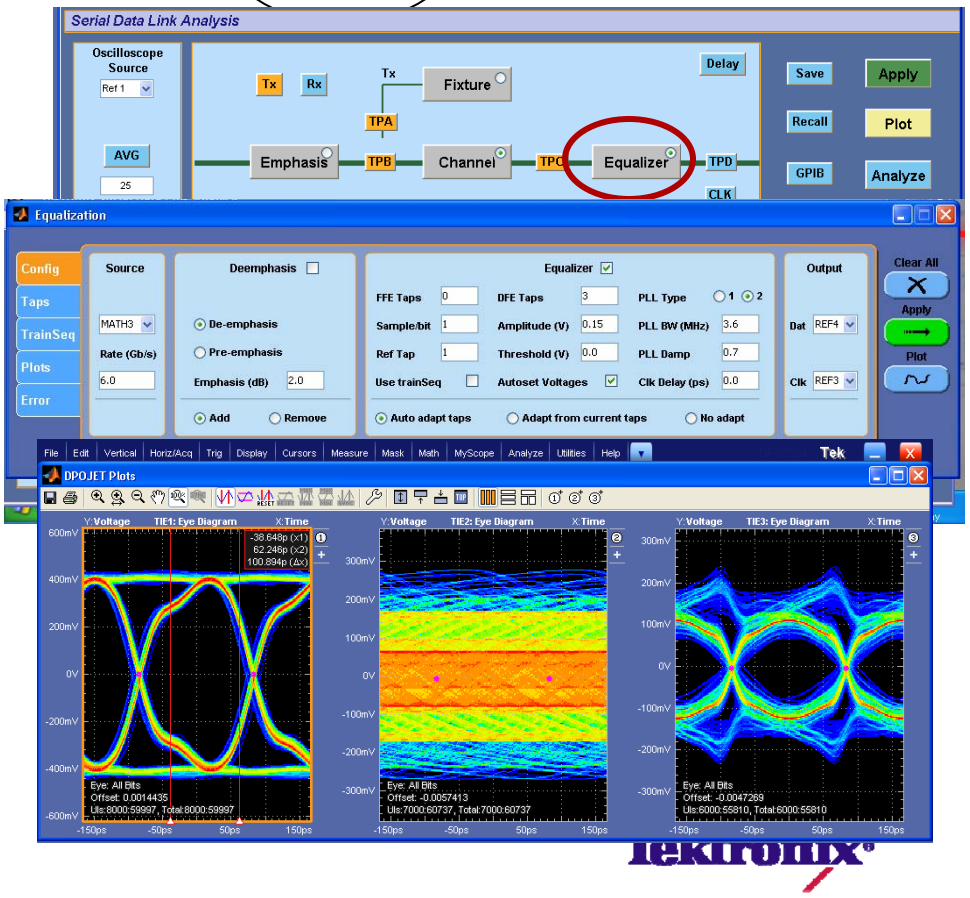
- Transmitter equalization
  - Pre/De-emphasis.
  - Enter the dB
- See the results in frequency and time domain for debug



Rx Equalization Emulation with FFE and DFE

- What would the signal look like at the Rx, with Equalization?
- When measuring the signal after the emulated channel





- Supports FFE and DFE.
- DFE has 3 modes of operation: Adapt from provided taps, Adapt from automatically generated taps, do not adapt.
- Same Clock recovery as DPOJET
- Slicer controls
- Support training sequence
- Create Ref waveforms to plot into Eye diagrams in DPOJET

Agenda

- ✓ Serial Data Network and Link Analysis Applications
- ✓ Serial Data Network Analysis and Cable Testing
- ✓ Serial Data Link Analysis and Jitter, Noise and BER Measurements
- ☞ Summary

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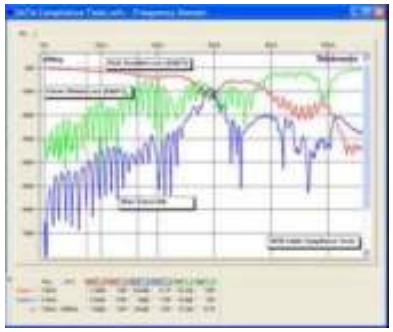
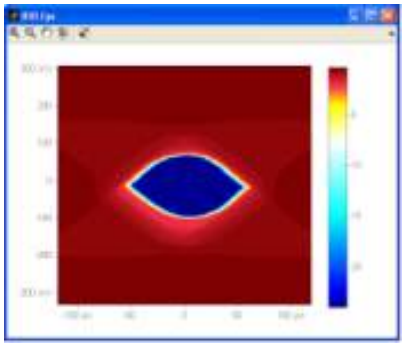
Serial Data Network and Link Analysis Toolset



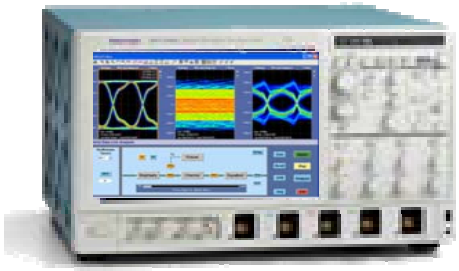
TDR/TDT/IConnect for Serial Data Network Analysis

- 50 GHz TDR/TDT system and S-Parameter measurements, highly accurate impedance and loss measurements
- Up to 1M record length



80SJNB – Jitter Noise, BER and Link Analysis

- Advanced Transmitter Analysis with SSC support
- "Complete Link" – channel embedding/de-embedding, equalization (FFE/DFE)
- Separation of Jitter & Noise into deterministic & random components at the comparator
- Eye contour and BER eye calculations at the comparator



Serial Data Link Analysis for DSA/DPO70000

- DFE/FFE Equalization algorithms correlated to industry references
- Time and Frequency plots to verify S-parameters translation
- Equalization with 3 modes of adaptation that can learn from a known pattern, a random pattern or traffic or can be pre-configured

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