泰克2014年春季创新论坛 数据中心外部互联接口测试综合解决方案







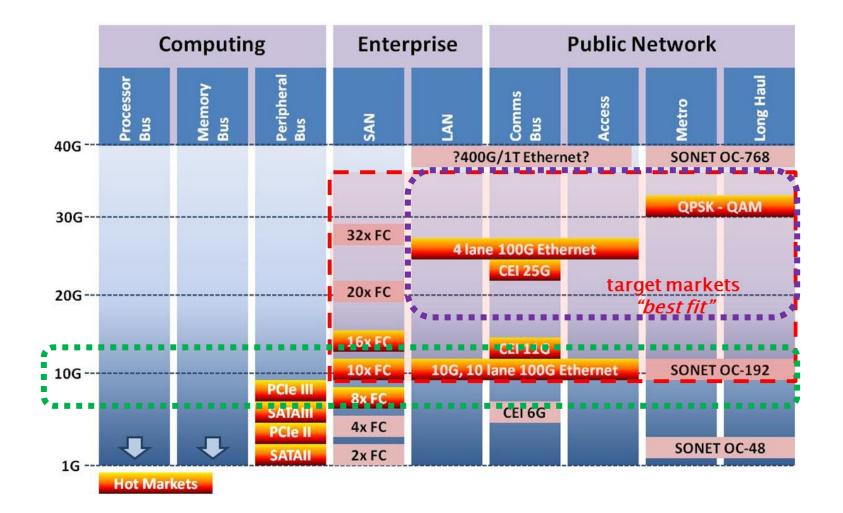
What's Data Center

- A data center is a facility used to house computer systems and associated components/modules, such as telecommunications and storage systems.
 - Servers and high performance storage w/ associated interfaces (SAS, SATA, PCIe, FC, IB, SFP+, CEI etc.)
 - Local Area Network such as switches and routers(1000Base-T, 10GBase-T, etc.)
 - Edge Networks such as line cards, legacy serdes/transceivers(XFP /SFP+/QSFP+) and fiber optic transceivers(NRZ&MM)
 - Backbone Networks such as Fiber optic transceivers(CXP/CFP/CFP2 /QSFP28, SM or Coherent optic) and high speed routers/switches(CEI, 40GBase-CR4/100GBase-CR10, PAM4, QAM16 etc.)





Segment and Data Rate







Agenda

- Tektronix 10Gbps Solution Portfolio
 - Transmitter
 - SFF-8431 SFP+ / SFF-8635 QSFP+
 - 10GBASE-T Automation Solution
 - 40GBASE-CR4 Debug and Automated Compliance Solution
 - Receiver
 - SFP+
 - 40&100G Ethernet XLAUI/CAUI, XLPPI/CPPI, & OIF-CEI
- Tektronix 25Gbps/40Gbps/100Gbps Solution Portfolio
 - Transmitter
 - OIF-CEI-VSR Compliance and Debug Testing
 - Receiver
 - Bertscope+DSA8300
 - Picosecond Pulse Labs PatternPro BERT Instruments
 - Optical
 - 155Mbps~100Gbps DSA8300 All-IN-ONE solution
 - 80C15 25Gbps MM optical
 - Coherent Optical Comms





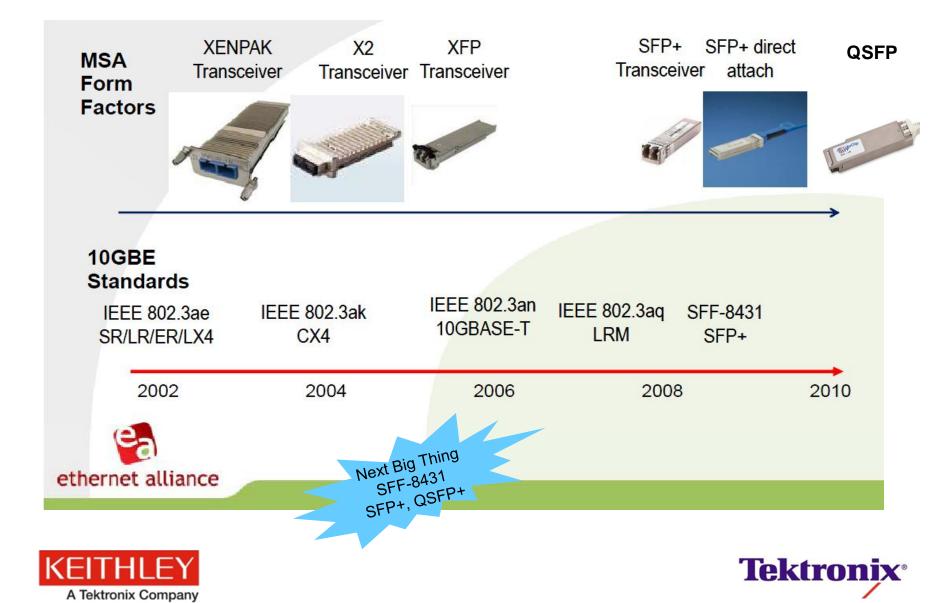
SFF-8431 SFP+ / SFF-8635 QSFP+ Compliance and Debug Testing







10Gigabit Ethernet Interface Evolution



SFF-8431 SFP+/SFF-8635 QSFP+ Technology overview

- SFP+ is a next-generation hot-pluggable, small footprint, serial-toserial multi-rate optical transceiver for 8.5GbE to 11.1GbE Datacom and Storage Area Networks (SAN) applications.
- SFF-8635 QSFP+ 10 Gb/s 4X Pluggable Transceiver Solution (QSFP10)
- SFP+ technology moved the clock and data recovery units out of the module and onto the line card – Reducing size drastically
- As a result, the modules are smaller, consume less power, allow increased port density, and are less expensive compared to XFP.
- High density capable Up to 48 ports in a rack
- Low power per port Host Port power < 1 W and Low Latency</p>





SFP+ Test Challenges

- Test Time
 - 48 Port Devices
 - Multiple test points and repetition in setup
- Debug vs. Compliance
 - When and how to make the shift with port replication in the process
 - Difficult to detect low amplitude impact on eye pattern performance
- Connectivity
 - Smaller package with difficulty to access test points
- Ambiguous Test Specification
 - Primary instrument defined for eye pattern measurements is equivalenttime oscilloscope so redefinition needed for real-time oscilloscope
- Test Pattern Setup
 - PRBS31 pattern is treated as an arbitrary waveform





SFP-TX Host Transmitter Measurements

• 15 Defined Measurements for Host Tx Compliance

SL		Signal Type	Limit			
No.	Measuremnts	Recommended	Min	Target	Max	Units
Hos	t Transmitter output electrical Specifications:	-				
1	Single Ended Output Voltage Range	PRBS31	-0.3		4	V
2	Output AC Common Mode voltage (RMS)	PRBS31			15	mV(RMS)
Hos	t Transmitter Jitter and Eye Mask specifications	-				
3	Crosstalk source rise/fall time (20%-80%) (Tr, Tf)	8180		34		ps
4	Crosstalk source amplitude (p-p differential)	8180		1000		mV
5	Signal rise/fall time (20%-80%) (Tr, Tf)	8180	34			ps
6	Total Jitter (p-p) (Tj)	PRBS31			0.28	UI(p-p)
7	Data Dependent Jitter (p-p) (DDJ)	PRBS9			0.1	UI(p-p)
8	Data Dependent Pulse Width Shrinkage (p-p) (DDPWS)	PRBS9			0.055	UI(p-p)
9	Uncorrelated Jitter (RMS) (UJ)	PRBS9			0.023	UI(p-p)
10	Transmitter Qsq	8180	50			
11	Eye mask hit ratio(Mask hit ratio of 5×10-5)	PRBS31	X1=0.12UI,	X2=0.33UI,	Y1=95m\	/, Y2=350mV
Hos	t Transmitter output specifications for Cu (SFP+ host supp	orting direct				
12	Voltage Modulation Amplitude (p-p)	8180	300			mV
13	Transmitter Qsq Output AC Common Mode voltage	8180	63.1			
14	Output AC Common Mode Voltage	PRBS31			12	mV(RMS)
15	Host Output TWDPc *	PRBS9			10.7	dBe





Tektronix SFP-TX – Automation Part

Tekronic Destrated Managera Destrate Destrate Destrate Destrate <td< th=""><th></th></td<>	

- Operates on Tektronix DPO/DSA70000C/DX Series Oscilloscopes
- Automate setup & quickly generate reports
- Meets Compliance needs of SFF-8431/SFF-8635
- User defined mode supports PRBS7, PRBS11, PRBS15, PRBS20 & PRBS23 in addition to patterns supported in Compliance mode including PRBS9, PRBS31 and 8180.





Tektronix SFP-TX – Debug Part



- Operates on Tektronix DPO/DSA70000C/DX Series Oscilloscopes
- DPOJET(DJA) Standard Specific Drop down menu item
- Meets Compliance needs of SFF-8431/SFF-8635
- Signal patterns supported include 8180, PRBS9 & PRBS31

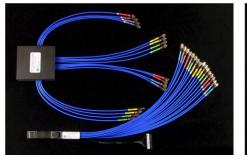




Ethernet SFP+ QSFP+ Compliance and Debug Solution– SFP-TX,SFP-WDP

Complete Solutions for Physical Layer Test

Models	Channels	Bandwidth	Required Options
DPO/DSA/ MSO70K	4	≥16GHz	SFP-TX, SFP-WDP, DJA (DJA included with DSA)





QSFP+ HCB & MCB

SFP+ HCB & MCB

Transmitter Test Recommended Accessories – Probes & Fixtures			
Probing			
SMA Cables Matched-pair SMA cables (TCA-SMA connector)			
	Fixturing		
TF-SFP-TPA-HCB-P	SFP+ Host Compliance Board Plug		
TF-SFP-TPA-MCB-R	SFP+ Module Compliance Board Receptacle		
TF-SFP-TPA-PR	SFP+ Host Compliance Board Plug and Module		
IT-SEP-IPA-PK	Compliance Board Receptacle		
TF-SFP-TPA-HCB-PK	SFP+ Host Compliance Board Plug Kit with DC		
TF-SFP-TPA-HCB-PK	Blocks		
TF-SFP-TPA-MCB-RK	SFP+ Module Compliance Board Receptacle Kit		
TI-SIF-TFA-WICD-INK	with DC Blocks and Termination		
TF-SFP-TPA-PRK	SFP+ Host Module Compliance Board and Module		
IF-SFP-IPA-PKK	Compliance Board with DC Blocks and Termination		
TF-QSFP-TPA-HCB-P	QSFP+ Host Compliance Board Plug		
TF-QSFP-TPA-MCB-R	QSFP+ Module Compliance Board Receptacle		
	QSFP+ Host Compliance Board Plug and Module		
TF-QSFP-TPA-PR	Compliance Board Receptacle		
TF-DC-BLOCK-KIT	DC Block Kit (Quantity 4)		
	Iektronix		

Transmitter Test Recommended		
Accessories - Sof	DPOJET jitter and eye	
Opt. DJA	diagram analysis – Advanced	
Opt. SFP-TX	Ethernet SFP+ QSFP+ Compliance and Debug Solution	
DPOFL-SFP-TX	Ethernet SFP+ QSFP+ Compliance and Debug Solution – Floating	
Opt. SFP-WDP	Ethernet SFP+ QSFP+ Compliance and Debug	
DPOFL-SFP-WDP	Ethernet SFP+ QSFP+ Compliance and Debug Solution – Floating	



10GBASE-T Automation Solution

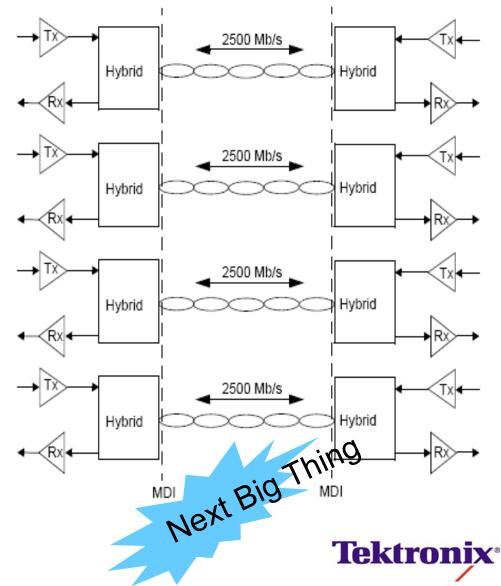






10GBASE-T - Overview

- 10GBASE-T provides 10 gigabit/second connections over unshielded or shielded twisted pair cables, over distances up to 100 m. 2.5Gbps per lane (A, B, C & D)
- Baseband 16-level PAM signaling with a modulation rate of 800M symbols per second is used on each of the wire pairs.
- Supports full duplex operation only
- Compatibility of Auto Negotiation enabled to also operate 10/100/1000 BASE-T
- Supports a BER of less than or equal to 10E-12 on all supported distances and Classes
- Provides a cost advantage over fiber





XGbT – 10GBASE-T Automation Solution

- Comprehensive Automated Solution for 10GBASE-T PHY Compliance
- XGbT performs spectral-based measurements, such as PSD, Power Level, and Linearity, all with a simplified instrument configuration.
- One-button Selection of Multiple Tests and Four-channel Support
- Detailed Test Reports with Margin and Statistical Information Aid Analysis
- Efficient Test Execution on Oscilloscope or PC with Instrument Remote Control
- Call XGbT application programmatically through NI LabVIEW or NI TestStand[™] for controlling XGbT test instrumentation along with thermal chambers, power supplies etc.





XGbT–10GBASE-T Transmitter Measurements

10GBASE-T Measurements covered in XGbT Solution

	Measurement	Test Mode	XGbT Features / Notes
1	Maximum output droop	Sub clause 55.5.3.1, Test Mode 6	Flexibility to test beyond compliance – XGbT provides the flexibility to perform testing beyond what is specified in IEEE standard 802.3an-2006. It helps users to analyze their PHY in addition to compliance tests.
2	Transmitter timing jitter – Master	Sub clause 55.5.3.3, Test Mode 2	Measure Jitter down to just few picoseconds. Software Filters are designed and applied on the acquired data automatically while performing measurements.
3	Transmit clock frequency	Sub clause 55.5.3.5, Test Mode 2	Exact PPM value for measured clock frequency is shown
4.	Transmitter timing jitter – Slave	Sub clause 55.5.3.3, Test Mode 1 and Mode 3	Measure Jitter down to just few picoseconds. Software filters are designed and applied on the acquired data automatically while performing measurements.
5	Transmitter linearity	Sub clause 55.5.3.2, Test Mode 4. Tones 1-5	Spectral Features of the scope are used to perform the measurement, a methodology that is unique to Tektronix and approved by UNH-IOL
6	Transmitter power spectral density (PSD) and power level	Sub clause 55.5.3.4, Test Mode 5	Spectral Features of the scope are used to perform the measurement, a methodology that is unique to Tektronix and approved by UNH-IOL
7.	Return Loss	Sub clause 55.8.2.1, Test Mode 5	Return Loss is performed using AWG, this method is unique to Tektronix.





TF-XGbT Test Fixture

The XGbT test fixture provides easy access to the 10GBASE-T Electrical signals to perform conformance testing and device characterization as described in of IEEE 802.3an-2006 sub-clause 55.5.3 & 55.8.2.1. This fixture is used with the Tektronix's XGbT- 10GBASE-T Automation Solution to provide fast and accurate design debugging and validation. XGbT fixture covers all seven measurements including Jitter Slave and MDI Return Loss



Fig 1: XGbT Test Fixture main board

Fig 2: Calibration Board



Figure 3: RJ45 Shielded Patch cord





10GBASE-T Automated Compliance Solution - XGbT

Complete Solutions for Physical Layer Test



Features

realures	Denents
One Box Solution	"One Box solution" XGbT uses scope for performing all measurements. When performing 10GBASE-T PHY layer testing customers can use scope rather than using multiple instruments. XGbT provides simplified and cost effective solution.
Multiple lane support	XGbT can perform all four lane testing simultaneously. User can make the connections, hit the run button and get a report. XGbT users don't require to make any new connection as is the case with Agilent U7236A solution.
DUT Automation	User can make connections and software will automatically put the DUT in different test modes. Test time is reduced and user experience is improved many folds. Test time can reduce by 30- 50%.
Diverse Probing solution support	Design Engineers have options to choose between Cost effective SMA cables and or Probes which can support complete automation of four lanes
XGbT can be run on a general purpose	XGbT can be run remotely and user need not be in front of the scope in the lab.

A Tektronix Company

comprehensive device validation

	DUTID BUILDE	Run Stop	
Select Acquire Analy	ce Report		
Source	Test Lanes	DUT Automation	
Oilferential	O All Lanes	O Using MDIO	
Single Ended	Select Lane Lane A Lane B Lane C Lane D	⊙ Manual	
Test Measurements		Test Description	
Consop Power Spectral Density Constrainty Constrainty Constrainty Constrainty Constrainty		Droop -> (IEEE Std 802.3an-2006 isoction 55.5.3.1; Set the DUT to operate in text mode 6. Droop Positive is performed by measuring voltage law at 10 ns and 50 ns after the zero crossing on the sing edge. Similarly, Droop Negative is performed by	
Tone-3		Click to view image of the waveform	
⊘ Tone-4 ⊘ Tone-5		Configure	
Tone-5		ShowSchematic SelectAll	
Clock Frequency			
		SelectAll	

A versatile, analysis solutions to span compliance and characterization

Featuring:

- One-button Selection of Multiple Tests and Fourchannel Support
- Simplified Instrument Setup Save Time and Resources
- Detailed Test Reports with Margin and Statistical Information Aid Analysis
- User-defined Mode enables Flexible Parameter Control for
 - Characterization and Margin Analysis
- Efficient Test Execution on Oscilloscope or PC with
 Instrument Remote Control
- Single Instrument Analysis of Time- and Frequencydomain Measurements
- Signal Acquisition and Analysis Support for Differential Probes or Direct SMA Cabling
- Uses MDIO Interface to put the DUT in Test Mode which Helps End-users to Automate their Test Bench
- Four-channel Support
- Fine Grain Programment for the state nix

10GBASE-T Automated Compliance Solution - XGbT

Complete Solutions for Physical Layer Test

Models	Channels	Bandwidth	Required Options
DPO/DSA/ MSO70K	4	≥4GHz	XGbT

Transmitter Test	Transmitter Test Required Accessories			
XGbT	10GBASE-T Automation Compliance Solution			
Fixture				
TF-XGbT	XGbT Test Fixture			

XGbT Supported Probes

Scope	All Measurements (Except Return Loss)	Return Loss
DPO/DSA/MSO70000	P6300*1	P6300*1
	P7330, P7350	P7330, P7350
	TriMode Probes – P7520, P7516, P7513A, P7508, P7506, P7504	TriMode Probes – P7520, P7516, P7513A, P7508, P7506, P7504
	SMA Cables	P7340A, P7360A, P7380A
	P7350SMA, P7380SMA, P7313SMA	



Key Applications	Benefits
 10GBASE-T Silicon Validation 	 Comprehensive coverage of physical layer measurements
 XGbT Compliance Test 	 Complete automation of all Compliance Measurements
 XGbT Device Production Testing 	 Product companies manufacturing 48port 10GBASE-T switches would like to use XGbT for production testing of their devices





40GBASE-CR4 Debug and Automated Compliance Solution

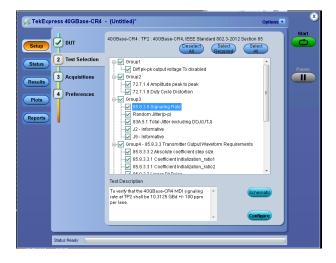






40GBASE-CR4 technology overview

- The clause 85 of IEEE 802.3 specification details out 40GBASE-CR4 PMD. The 40GBASE-CR4 is a lowswing AC coupled differential interface. AC coupling at the receiver allows for interoperability between components operating from different supply voltages. Low-swing differential signaling provides noise immunity and improved electromagnetic interference (EMI).
- The 40GBASE-CR4 signal paths are point-to-point connections. For 40GBASE-CR4, there are four differential paths in each direction for a total of eight pairs, or sixteen connections. 40GBASE-CR4 is a 40 Gigabit Ethernet technology. It uses 4 lanes to achieve the required data rate(4 *10.3125 Gbps). The channel between transmitter and receiver is four lanes of shielded balanced copper cabling. Length of the signal path in 40GBASE-CR4 can range from 0.5 m to 7 m.









Transmitter characteristics for 40GBASE-CR4

Parameter	Sub clause ref	Value	Units	TP0	TP2
Signaling Rate, per lane	85.8.3.9	10.3125 ± 100 ppm	GBd	1	1
Unit interval nominal	85.8.3.9	96.969697	ps	1	1
Differential peak-to-peak output voltage (max) with Tx disabled		30	mV	1	1
Common Mode Voltage Limits	72.7.1.4	0 to 1.9	V	1	1
Differential Output Return Loss		See Equation (85–1)	dB	1	1
Common Mode Output Return Loss		See Equation (72–6) & (72–7)	dB	1	
Amplitude peak to peak(max)	72.7.1.4	1200	mV		1
Random Jitter (p-p)	72.7.1.9	0.15	UI	1	1
Duty Cycle Distortion	72.7.1.9	0.35	UI	1	1
Total Jitter excluding DDJ	83A.5.1	0.25	UI		1
Total Jitter	72.7.1.9	Informative	UI	1	
Deterministic Jitter	72.7.1.9	Informative	UI	1	
J2 (Informative)	-	Informative	UI		1
J9 (Informative)	-	Informative	UI		1
Transititon Time (20% - 80%)	72.7.1.7	Thformative test for TP2 Normative test for TP2	UI	1	1
Transmitted waveform					
- max normalized error(linear fit), "e"	85.8.3.3	0.037			
- abs coefficient step size	85.8.3.3.2	0.0083 min, 0.05 max	-		1
- minimum precursor fullscale range	85.8.3.3.3	1.54			
- minimum post cursor fullscale range	85.8.3.3.3	4			
Transmitter DC amplitude	85.8.3.3	0.34 min, 0.6 max	V	1	1
Linear fit pulse (min)	85.8.3.3	0.63 × Transmitter DC amplitude	v	1	1



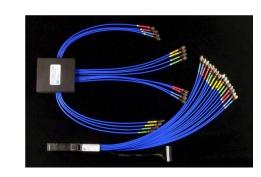


40G-CR4 Compliance and Debug Solution

Recommended Equipment	:			
Oscilloscope	Software	Accesscories	Test Fixture	
Required	Required			
DPO/DSA/MSO71604C	40G-CR4 & DJA*1	TF-DC-BLOCK-K	TF-QSFP-TPA-HCB-P	
DPO/DSA/MSO72004C			QSFP+ Host Compliance	
DPO/DSA72504D			Board Plug	
DPO/DSA73304D				
*1 - Prerequisite for 40G-CR4				

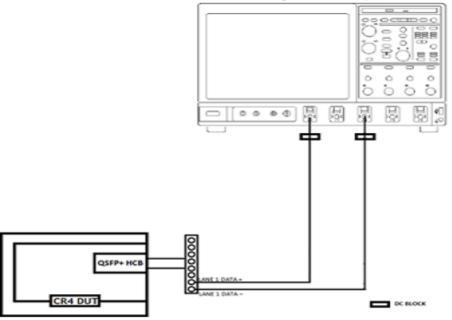


SFP+ HCB & MCB



QSFP+ HCB & MCB









Tektronix 40G-CR4 - Features & Benefit

Features

Benefits

Developed on Platform of choice for Debug and Compliance	Tektronix 40G-CR4 is developed on a Real Time Oscilloscope platform, which is the platform of choice for engineers working on designing their products around 40GBASE-CR4 technology.
Seamless movement from Compliance to Debug Environment	Customers can seamlessly move from compliance to debug environment and use world-class debug tool from Tektronix i.e. DPOJET.
Return Loss Measurement Support	The 40G-CR4 solution does provide the ability to take an .s16p file as an input to map the results against limits. This feature provides design engineers an option to use common reporting and plotting mechanism available on one instrument.
Informative measurements	Additional informative measurements have been added to compliance suit which provide design engineers with greater insight into their designs. Additional measurements include Total Jitter, Deterministic Jitter, J2, J9 and Transition Time.
"One Stop Shop" - Test Fixture Availability	Engineers working on QSFP+/SFP+ can turn to Tektronix for their complete PHY testing solution needs including fixtures and don't have to design their own fixtures
DPOJET Setup files provided	DPOJET setup files for N1N0, PRBS9 patterns are provided with the 40G-CR4 which help set scope and load measurements in DPOJET. This helps reduce debug time and set the scope for debug environment.





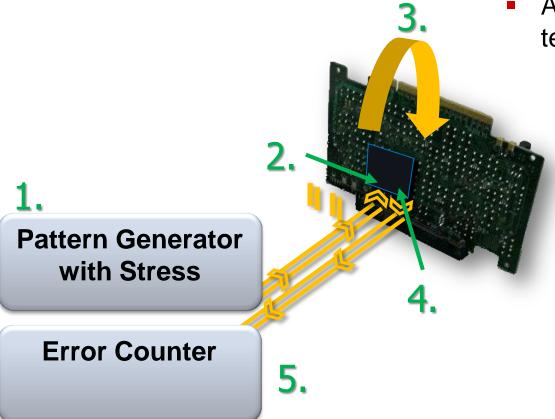
SFP+, 40&100G Ethernet XLAUI/CAUI, XLPPI/CPPI, & OIF-CEI Receiver Testing







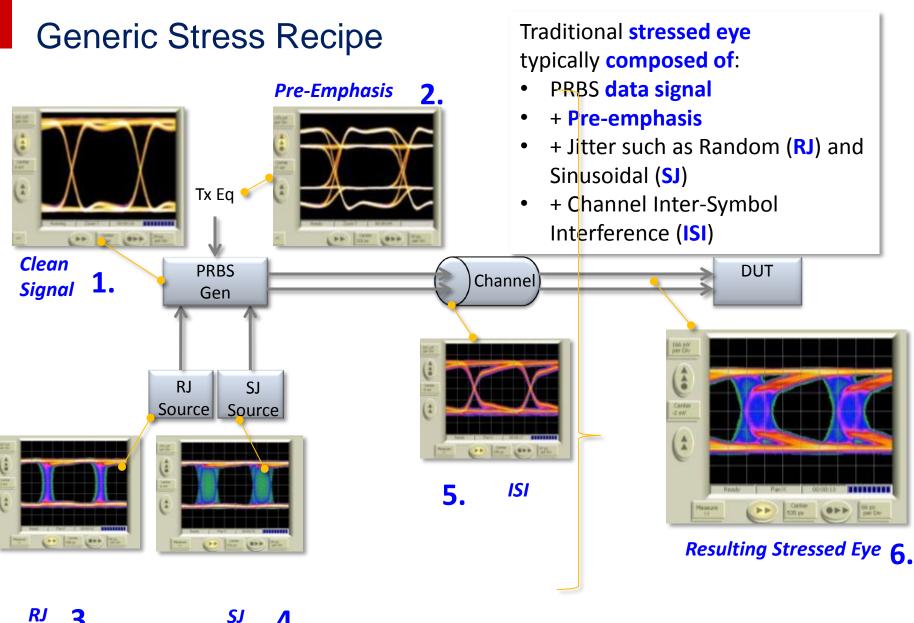
Basic Receiver Testing



- At the simplest level, receiver testing is composed of:
 - Send impaired signal to the receiver under test
 - 2. The receiver decides whether the incoming bits are a one or a zero
 - 3. The chip loops back the bit stream to the transmitter
 - 4. The transmitter sends out exactly the bits it received
 - An error counter compares the bits to the expected signal and looks for mistakes (errors)

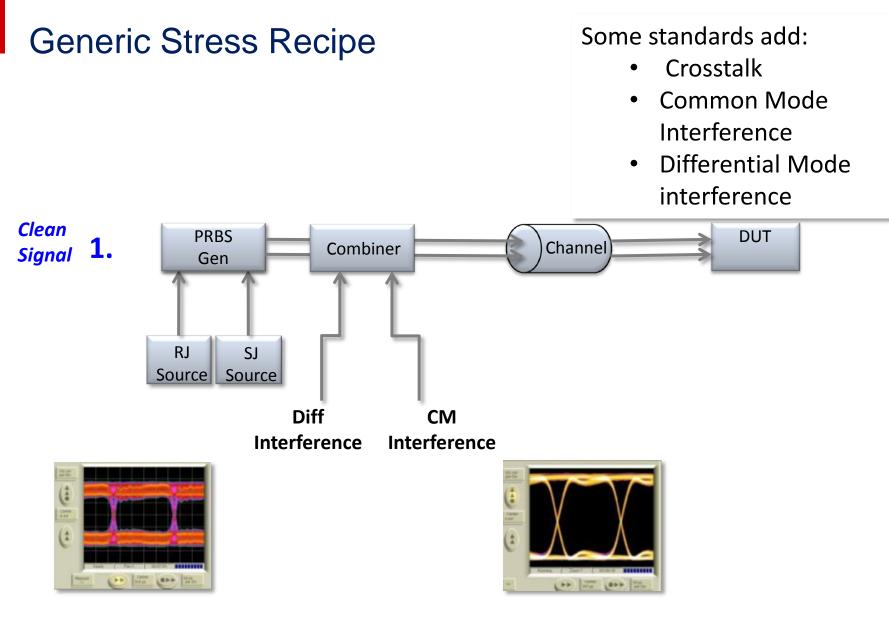
















SFP+ Host Rx Calibration Example

- Test the intrinsic jitter of the test source. The J2 shall be <0.15UI and TJ<0.25UI
- Add SJ@20MHz until the J2 increase by 0.05UI
- Add ISI with ISI board until the 0.3UI DDPWS and at least 80% J2(0.8*0.42=0.336UI) are reached.
- If J2 don't reach 0.42UI target value, then add Sine Interface&2GHz&In-phase until 0.42UI J2 target is achieved.
- Add Rj@100MHz~1GHz until 0.7UI Tj target is achieved.
- Decrease the output signal amplitude to meet the Eye Mask@1E-12 requirement with Bert contour.(I don't demo the step).

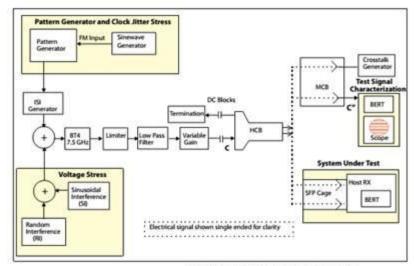


Figure 50 Jitter Tolerance Test Configuration

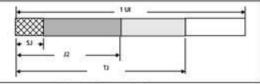


Figure 51 Stressed eye jitter components

Tektronix[®]

Table 14 Host receiver supporting limiting module input compliance test signal calibrated at C"

Parameters - C"	Symbol	Conditions	Target Value	Max	Units
Crosstalk Source Rise/Fall time (20% to 80%)	Tr, Tf	Sec <u>D.6</u>	34		ps
Crosstalk Source Amplitude (p-p differential)		See 1	700		mV
AC Common Mode Voltage		See 2 and <u>D.15</u>		7.5	mV (RMS)
99% Jäter	12	See 3, D.5, D.11	0.42		UI (p-p)
Pulse Width Shrinkage Jitter	DDPWS	See 4, D.3	0.3		UI (p+p)
Total Jitter	TJ	BER 1×10 ⁻¹² see D.5. D.11	0.70		UI (p-p)
Eye Mask	X1	Mask hit ratio of 1×10 ⁻¹² ,			UI
Eye Mask Amplitude Sensitivity 5.8	Y1	See D.2. D.11.	150		mV
Eye Mask Amplitude Overload 6.7.8	¥2		425		mV



Stressed Receiver Block Diagram Examples 40 & 100 G Ethernet XLAUI/CAUI, XLPPI/CPPI, & OIF-CEI

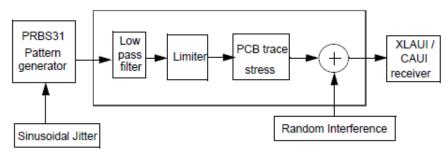


Figure 83A–15—Stressed-eye and jitter tolerance test setup

Different standards use different stresses. Most use SJ, many require RJ and BUJ and ISI as well. Some require vertical eye closure – some use SI, some use RI, some use both.

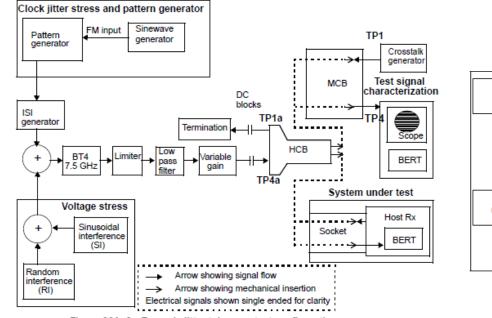


Figure 86A-8—Example jitter tolerance test configuration



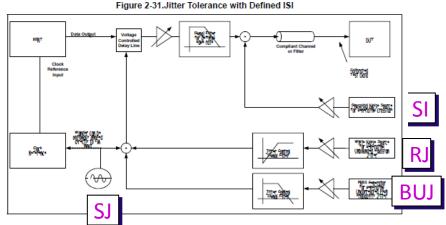


Figure from OIF-CEI-2.0



25Gbps/40Gbps/100Gbps Solution Portfolio







The top-to-bottom of 100G standards

Dista	nce	Standard	Modulation/signaling	Tel: solution
X,000) km	OIF, OTN, ITU	Complex optical	OM4000, TDS73304D
10 to	40 km	Ethernet 100GBASE- LR4, -ER4	NRZ Single-Mode	DSA8300+80C10C; BSA286CL, CRU286A
100 m	n to 2km	Ethernet	NRZ MM and SM	DSA8300+ 80C15C; BSA286CL, CR286A
10 m		Ethernet	NRZ over cable or el.<->opt. cable	DSA8300+ 80E09B/10B+80A08
Backp 1m	olane <	Ethernet, OIF CEI	NRZ, PAM4	BSA286CL, CR286A PSPL PatternPro
	onnect e to chip, o chip	OIF CEI Ethernet	NRZ	As above, + CEIVSR Sol. SW





Tektronix Performance Solutions By Application and Customer End Product

End Product	Interface PHY	Transmission Test	Receiver Test
SerDes	Electrical	DSA8300 w/80E10B & 82A04B (Golden Eye) MSO70000DX (Debug)	BSA286C PSPL PatternPro (full line of Picosecond Products, OEM+new)
Transceiver/Cable	Electrical	DSA8300 w/80E10B (Compliance & TDR) MSO70000DX (Debug)	BSA286C PSPL PatternPro
Transceiver/Cable	Optical	DSA8300 w/80C10C, 80C14 (NRZ-Serial) OM4000 w/DPO73304DX (Modulation Check)	BSA286C (NRZ-Serial Signaling) PSPL PatternPro AWG70000 or PPG320X w/OM5510 (QPSK, PAM-based Modulation)
Line Card/System	Electrical	DSA8300 w/80E10B (Compliance & TDR) MSO70000DX (Debug)	BSA286C PSPL PatternPro
Line Card/System	Optical	DSA8300 w/80C10C, 80C14 (NRZ-Serial) OM4000 w/DPO73304DX (Modulation)	BSA286C (NRZ-Serial) PSPL PatternPro AWG70000 or PPG320X w/OM5510 (QPSK, PAM-based Modulation)





CEI-VSR Compliance and Debug Testing

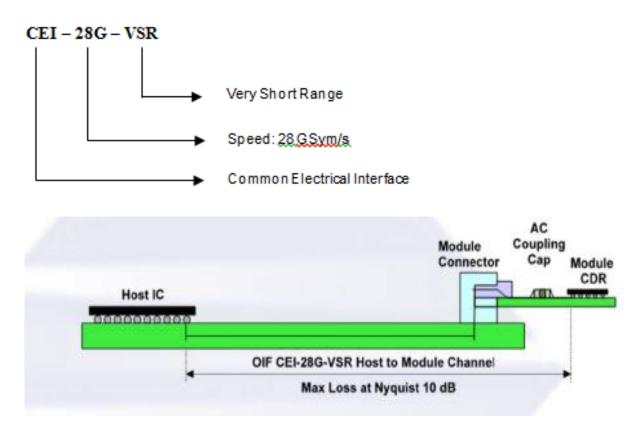






CEI-28G-VSR Technology Evolution

OIF-CEI-VSR - Optical Internetworking Forum - Common Electrical Interface -28G-VSR (CEI-28G-VSR)







CEI-28G-VSR Technology Evolution

- CEI-28G-VSR This clause details the requirements for the CEI-28G-VSR very short reach high speed chip-module electrical I/O of nominal baud rates of 19.60 Gsym/s to 28.05 Gsym/s.
- The industry is transitioning from 10x10G to a more efficient 4x25 electrical interconnect.
- The first standard body in the move to 25 Gb/s signaling is the OIF CEI, with the VSR, SR, and LR (very short reach, short reach, long reach) standards
- Under development is the Ethernet's 802.3bm 100GBASE-KR4 backplane standard, as well as the Ethernet interconnect standard, 802.bj CAUI4.
- The electrical I/O is based on high speed, low voltage logic, and connections are point-to-point balanced differential pairs.





CEI-VSR Transmitter Measurements

Parameters	CEI-28G-VSRH2M	CEI-28G-VSR M2H	Components used for performing Measurements
Baudrate	1.1	1.1	Clock Recovery
Rise times / fall times	1.3.2	1.3.3	AL - Algorithm Library
Differential output voltage	1.3.2	1.3.3	Base Scope
			Customer need to enter value, if we do this
Output Common mode voltage	1.3.2	1.3.3	measurement on scope it will demage the scope
TX Common Mode Noise RMS	1,3.2	1.3.3	Base Scope
UUGJ-Uncorrelated Unbounded Gaussian Jitter			RJ in 80SJNB
UBHPJ-Uncorrelated Bounded High Probability Jitter			PJ in 80SJNB
Eye width (EW15)	1.3.2	1.3.3	80SJNB
Eye height (EH15)	1.3.2	1.3.3	80SJNB
Vertical eye closure		1.3.3	80SJNB





Option CEI-VSR - Compliance and Debug Solution

- Automated Tests
 - One-button selection of critical H2M & M2H Tests reduces testing time
- Integrated Debugging
 - Popular 80SJNB-based interface enables deeper debug of timing root cause analysis without moving to a different instrument/measurement setup
- CTLE Filters
 - Option CEI-VSR determining the optimal value of CTLE peaking, which is required by the CEI 28G Very Short Reach for the Host-to-Module interface. The best CTLE filter is chosen from the given set of filters and used for performing the measurement.
- J2 & J9 Measurements
 - Rely on off-the-shelf products to perform this complex measurement rather than developing custom lab setup reducing testing time and complexity
- Documentation/Reporting
- Signal Validation

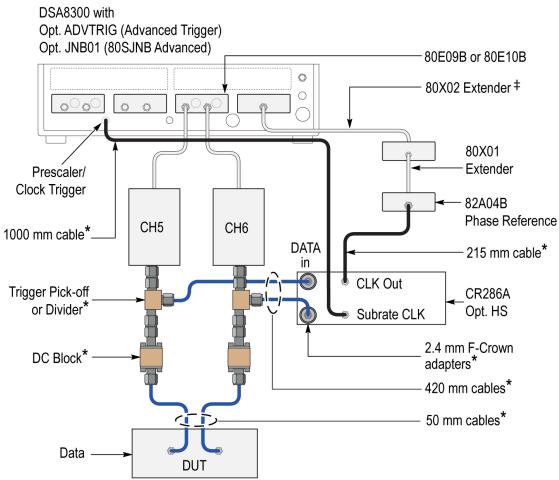




805JNB Jitter Noise an	nd BER Analysis						mix x	Setups				
File View Setup He	lp.		Tektroni			PSync. III	Арр	Phase Re	Ma	sk T	DR	Disp
	mart			0 40	VI IV	NN	M	Wfm Data		1	Cursor	Meas
			E			Internal Concession		Vert	Horz	Acq		1
DJ PDF		DDJ vs Bit								Acq	MO	de/Trigge
a urror		CA DOSAS DA						Wavefor	11			
· · · · · · · · · · · · · · · · · · ·								M1		2 On	Defi	ne
10		AV AND A HIS	4月1日 日本の一日本日の									
10-0	·····	2m-11-11-11-11-11-11-11-11-11-11-11-11-11						C5-C6				
Apr 1	135	-11.51	4 64					Setup				
BER Bathtub		BER Eye						10.002				1.1
	F	10 m						Scale		243.0mV/	div 📗	1÷
8.0				TOWN HOLD	W. Marther			Positio		-100.0md		(·)
3.4.				in white	9 ·			Positio	n	-100.0mg	V III	
-20		-525.411	and the second se		- Walt			Chann	e e			
		-27 m	21.00		Window		- 1			0.0V		1.1
din 1	- 27.28											
Results : 25.781 Gbps, 511 bits	2.0					Maria	- 1	Offse	1.			1
Results : 25.781 Gbps, 511 bits Data Source: NATH1	Dat	Rate: 25.781 Gbps	Filter: False			Mass	-"	Offse	e		٦Ĵ	
Data Source: NATH1 SSC: Off	Patt	ern: 511 bits	Channel: False	Acquisition		Marris	1	Ottse	e		Ì	
Data Source: NATH1 SSC: Off Phase Reference: 12.8905 GH	z San	ern: 511 bits sple Court: 151.10 k	Charnel: False Equalizer: None			Mass	1	Offsi	e			
Data Source: MATH1 SSC: Off Phase Reference: 12.8905 GH Jitter (Decision Threshold: 24	z San	em: 511 bits tple Court: 151.10 k Noise (Sampling Phase:	Charnel: False Equalizer: None	Acquisition AutoSync to Sele		Mana			e			1
Data Source: MATH1 SSC: Off Phase Reference: 12.8905 GH Jitter (Decision Threshold: 24 Random Jitter	z San (40 mV)	ern: 511 bits hple Count: 151.10 k Noise (Sempling Phase: Random Noise	Channel: False Equalizer: None 0 UI)	Acquisition		Mana	Signal Condit		<u>r</u>			
Deta Source: MATH1 SSC: Off Phase Reference: 12.8905 GH Jitter (Decision Threshold: 24 Random Jitter RJ (RMS)	z San (40 mV) = 251.36 fs	ern: 511 bits nple Count: 151.10 k Noise (Sempling Phase: Random Noise RN (RMS)	Channel: False Equalizer: None 0.UE) = 5.07 mV	Acquisition AutoSync to Sele Signal	icted Source	Page			<u>t</u>			
Data Source: NATH1 SSC: Off Phase Reference: 12.8905 GH Jitter (Decision Threshold: 24 Random Jitter RJ (RMS) RJ(h) (RMS)	z San (40 mV) = 251.36 fs = 227.62 fs	ern: 511 bits nple Count: 151.10 k Noise (Sampling Phase: Random Noise RN (RMS) RN(V) (RMS)	Charnel: False Equalizer: None 0 UE) = \$.07 mV = \$.07 mV	Acquisition AutoSync to Sele Signal	icted Source	• DH	Wavelength		<u>t</u>			
Data Source: NATH1 SSC: Off Phase Reference: 12.8905 GH Jitter (Decision Threshold: 24 Random Jitter RJ (RMS) RJ(h) (RMS) RJ(h) (RMS)	z San (40 mV) = 251.36 fs	em: 511 bits sple Count: 151.10 k Noise (Sampling Phase: Random Noise RN (RMS) RN(v) (RMS) RN(v) (RMS)	Channel: False Equalizer: None 0.UE) = 5.07 mV	Acquisition AutoSync to Sele Signal Source	icted Source	Page			a			
Data Source: NATH1 SSC: Off Phase Reference: 12,8905 GH Jitter (Decision Threshold: 24 Random Jitter RJ (RMS) RJ(N) (RMS) RJ(V) (RMS) RJ(V) (RMS) Deterministi; Jitter	z San (40 mV) = 251.36 fs = 227.62 fs = 106.64 fs	em: 511 bits pple Count: 151.10 k Noise (Sempling Phase: Random Noise RN (RMS) RN(h) (RMS) Deterministic Noise	Channel: False Equalizer: None 0 UE) = 5.07 mV = 5.07 mV = 641.99 mV	Acquisition Accosync to Sele Signal Source	icted Source	Page	Vavelength Filter		α			
Data Source: MATH1 SSC: Off Phase Reference: 12.8905 GH Jitter (Docision Threshold: 24 Random Jitter RJ (NS) RJ(N) (RMS) RJ(V) (RMS) Deterministic Jitter 03	z Patt 2 San 20 mV) = 251.36 fs = 227.62 fs = 105.64 fs = 3.13 ps	em: 511 bits pie Court: 151.10 k Noise (Sergling Phase: Ro (RMS) RN(v) (RMS) RN(v) (RMS) RN(v) (RMS) Deterministic Noise DN	Channel: False Equalizer: None 0.01:) = 5.07 mV = 5.07 mV = 641.99 mV = 177.27 mV	Acquisition Accosync to Sele Signal Source	icted Source	Page	Wavelength		a.			
Data Source: MATH1 SSC: Off Phase Reference: 12.8905 GH Jitter (Decision Threshold: 24 Random Jitter RJ (BMS) RJ(b) (RMS) RJ(b) (RMS) Deterministic Jitter 0 DD0	z Patt z San 40 mV) = 251.36 fs = 227.42 fs = 105.64 fs = 3.13 ps = 2.56 ps	em: 511 bits sple Count: 151.10 k Noise (Samping Phase: Random Noise RN (SMS) RN(V) (RMS) RN(V) (RMS) Deterministic Noise DN DDN	Channel: Palse Equalizer: None 0 UE) = \$.07 mV = \$.07 mV = 641.99 mV = 176.25 mV = 176.55 mV	Acquisition Accosync to Sele Signal Source	icted Source	Page	Vlavelength Filter Bandwidth		e			
Data Source: MATH1 SSC: Off Phase Reference: 12.8905 GH Jitter (Decision Threshold: 24 Random Jitter RJ(fn)(RMS) RJ(h)(RMS) RJ(h)(RMS) Deterministic Jitter OJ DDD DCD	z Patt z San (40 mV) = 251.36 fs = 227.62 fs = 105.64 fs = 3.13 ps = 2.56 ps = 123.72 fs	em: S11 bits nple Court: 151.10 k Noise (Sampling Phase: Random Noise RN (V) (RMS) RN(V) (RMS) RN(V) (RMS) Deterministic Noise DN DON DDN(evel 1)	Channel: Palse Equalizer: None 0 UE) = 5.07 mV = 5.07 mV = 641.99 mV = 177.27 mV = 176.55 mV = 181.21 mV	Acquisition Accosync to Sele Signal Source	icted Source	Page	Vavelength Filter		a			
Data Source: MATH1 SSC: Off Phase Reference: 12.8905 GH Jitter (Decision Threshold: 24 Random Jitter RJ (BMS) RJ(b) (RMS) RJ(b) (RMS) Deterministic Jitter 0 DD0	z Patt z San (40 mV) = 251.36 fs = 227.42 fs = 105.64 fs = 3.13 ps = 2.56 ps = 123.72 fs	em: 511 bits sple Count: 151.10 k Noise (Samping Phase: Random Noise RN (SMS) RN(V) (RMS) RN(V) (RMS) Deterministic Noise DN DDN	Channel: Palse Equalizer: None 0 UE) = \$.07 mV = \$.07 mV = 641.99 mV = 176.25 mV = 176.35 mV	Acquisition ActoSync to Sele Sgral Source Source Source Recommended Data Pattern	INTH: CSC6	• D#	Vlavelength Filter Bandwidth Pattern Clock		A			
Data Source: MATH1 SSC: Off Phase Reference: 12.895 GH Phase Reference: 12.895 GH Phase Reference: 12.895 GH BATCH (MMS) R(M) (MMS) R(M) (MMS) Deterministic Miter D1 DCD DCP D00 DCP D00 DCP MS	2 Patt 2 San 40 mV) = 251.36 fs = 227.62 fs = 105.64 fs = 3.13 ps = 2.56 ps = 123.72 fs = 1.23 ps	em: 511 bits pipe Count: 151.10 k Noise (Samping Phase: Random Noise RN (RMS) RN(v) (RMS) RN(v) (RMS) Deterministic Noise DN DDN(level 1) DDN(level 0)	Channel: False Equalizer: None 0 UL) = 5.07 mV = 5.07 mV = 641.99 nV = 177.27 mV = 176.55 mV = 181.21 mV = 192.44 mV	Acquisition ActoSync to Sele Sgral Source Source Source Recommended Data Pattern	icted Source	Page	Vlavelength Filter Bandwidth		A			
Data Source: NATH1 SSC: OF Pasa: Reference: 12.5905 GH Jitter (Decision Threshold: 24 Random Inter R0 (RH5) R(r) (RH5) R(r) (RH5) R(r) (RH5) Deterministic Jitter D1 DCD DCD DCD DCD DU/4-0)	Z San 40 mV) = 251.36 fs = 227.42 fs = 105.64 fs = 123.72 fs = 123.72 fs = 123.72 fs = 123.72 fs = 255.57 fs	earn 511 bis pic Court: 55.00 k Noise (Semping Phase: Random Noise RN (NS) RN(v) (RNS) Deterministic Noise DN DDN DDN(evel 1) DDN(evel 1) DDN(evel 1) PN(v)	Channel: False Equalizer: None 0.U5)	Acquisition ActoSync to Sele Source Source Source SSC is present Recommended Outs Pattern Rate 2	Intel Source	· D#	Vlavelength Filter Bandwidth Pattern Clock Scorce	Contraction Contraction	A			
Data Source: MATH1 SBC: OF Phase Reference: 12.8905 GH Phase Reference: 12.8905 GH Riffer (Decasion Threshold: 24 Random Attree Rij(N) (INIS) Rij(N) (INIS) Rij(N) (INIS) Rij(N) (INIS) Rij(N) (INIS) DCD DCD DCD DCD DDPWS BUIJ(6-4) P	z San 40 mV) 251.36 fs 227.42 fs 205.64 fs 237.74 fs 237.75 fs 237.57	erm 511 bis pipe Court: 151.10 k Nolee (Senging Phase: Random Noise Ex (INS) RN(b) (RHS) Deterministic Noise DN DDN(evel 1) DDN(evel 1) DDN(evel 0) BUN(6-d) PN PN(b)	Channel: False Equalizer: None 0.01	Acquisition ActoSync to Sele Sgral Source Source Source Recommended Data Pattern	Intel Source	• D#	Vlavelength Filter Bandwidth Pattern Clock	Contraction Contraction	4			
Data Source: MATri1 SSC: Off Phase Reference: 12.8905 GH Phase Reference: 12.8905 GH Phase Reference: 12.8905 GH Rith() (RMS) Rith() (R	Z San 40 mV) = 251.36 fs = 227.42 fs = 105.64 fs = 123.72 fs = 123.72 fs = 123.72 fs = 123.72 fs = 255.57 fs	earn 511 bis pic Court: 55.00 k Noise (Semping Phase: Random Noise RN (NS) RN(v) (RNS) Deterministic Noise DN DDN DDN(evel 1) DDN(evel 1) DDN(evel 1) PN(v)	Channel: False Equalizer: None 0.U5)	Acquisition ActoSync to Sele Source Source Source SSC is present Recommended Outs Pattern Rate 2	Intel Source	· D#	Vlavelength Filter Bandwidth Pattern Clock Scorce Recovery R	Cock/Presc	4			
Data Source: MATH1 SBC: OF Phase Reference: 12.8905 GH Phase Reference: 12.8905 GH Rifter (Decason Threshold: 25 Random: Atter R(h) (INIS) R(h) (INIS) R(h) (INIS) DD DDD DDPWS BUJ(d-d) P) P(h) P(h)	z San 40 mV) 251.36 fs 227.42 fs 205.64 fs 237.74 fs 237.75 fs 237.57	erm 511 bis pipe Court: 151.10 k Nolee (Senging Phase: Random Noise Ex (INS) RN(b) (RHS) Deterministic Noise DN DDN(evel 1) DDN(evel 1) DDN(evel 0) BUN(6-d) PN PN(b)	Channel: False Equalizer: None 0 UE	Acquisition ActoSync to Sele Source Source Source SSC is present Recommended Outs Pattern Rate 2	Intel Source	· D#	Vlavelength Filter Bandwidth Pattern Clock Scorce	Cock/Presc	4		- J	
Data Source: MATRI SSC: Of Phase Reference: 12.5995 Or Bandro Methods 20 Sandron Atter 20 (SMS) R(N) (SMS) R(N) (SMS) Determinisht: Atter O D D D D D D D D D D D D D D D D D D	Patt z San 4.40 mV) = 251.06 fs = 227.42 fs = 105.64 fs = 1.13 ps = 123.72 fs = 123.72 fs = 2.56 ps = 123.72 fs = 273.57 fs = 0 s = 50.00 fs = 50.00 fs = 50.00 fs = 50.00 fs = 50.00 fs	amn 511 bia pic Court: 51.0 k Note: CSantolico Phase: Random Neck (Shripiloo Phase: Randov Neck) Rit(v) (SHS) Rit(v) (SHS) Rit(v) (SHS) DDN(evel 1) DDN(evel 1) Rit(v)	Chandl: Faile Boaliter: None 50//5 50/mW 50/mW 641,99 m/ 176,55 m/ 176,55 m/ 176,55 m/ 199,44 m/ 9,98 m/ 9,98 m/ 9,98 m/ 2,98,46 m/	Acquisition ActoSync to Sele Source Source Source SSC is present Recommended Outs Pattern Rate 2	Intel Source	· D#	Wavelength Filter Bandwidth Pattern Clock Scorce Recovery R Phase Refere	Cock/Prec	4		- J	
Data Source: MATRI: SSC: GT Phase Reference: 12.595 GH Jitter (Decesion Threshold s2 Random Jitter Readom Jitter RAMON JINES DO DO DCC DO/D DO DCC DO/D P(Y) [1955] P(Y) [205] P(Y) P(Y) <	2 San .40 mV) = 251.36 fs = 227.42 fs = 106.54 fs = 3.13 ps = 2.35 ps = 123.72 fs = 123.72 fs = 123.72 fs = 50.00 fs = 275.57 fs = 0 s = 50.00 fs	arm 511 bia pic Court: 15:1.0 k Note: [Stratplay Desci Random Rese Random Rese	Chandl: Fable Bealter: None 5.02 million 5.02 million 6.01 Million 6.01 Million 6.01 Million 1.17,23 million 1.17,23 million 1.17,24 million 9.98 million 7.77,21 million 9.98 million 9.99 million 9.99 million 9.99 million 9.99 million 9.99 million 9.99 million 9.90	Acquisition ActoSync to Sele Source Source Source SSC is present Recommended Outs Pattern Rate 2	Intel Source	· D#	Vlavelength Filter Bandwicth Pattern Clock Source Plase Patere Source	Cock/Prec	4	+ + +	- III	
Data Source #MR1 Soc; Off Phase Reference: 12,2495 GH Bitted Education Threeholds & Bitted Education Threeholds & Ref (1) (845) Ref (1) (845) CO OC OCO OCO Bitted (1) (845) Ref (1) (84	Patt z San 4.40 mV) = 251.06 fs = 227.42 fs = 105.64 fs = 1.13 ps = 123.72 fs = 123.72 fs = 2.56 ps = 123.72 fs = 273.57 fs = 0 s = 50.00 fs = 50.00 fs = 50.00 fs = 50.00 fs = 50.00 fs	em: S11 bit epic Contr. 151.0 k Kons (Standbog Phases Endom Netrice RN(v) (RNS) RN(v) (RNS) RN(v) (RNS) Endom Netrice Deterministic Noise DA DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) RN(v)	Chandl: Faile Boaliter: None 50//5 50/mW 50/mW 641,99 m/ 176,55 m/ 176,55 m/ 176,55 m/ 199,44 m/ 9,98 m/ 9,98 m/ 9,98 m/ 2,98,46 m/	Acquisition ActoSync to Sele Source Source Source SSC is present Recommended Outs Pattern Rate 2	Intel Source	· D#	Wavelength Filter Bandwidth Pattern Clock Scorce Recovery R Phase Refere	Cock/Prec	4		- III	
Date Source #M2H1 SSC: OF Phase Reference: 12.8995 GP Minister Dousses Human Source Staff Datases Human Source SQL (SHS)	2 San 40 mV) 2 251.36 fs 2 227.42 fs 2 105.46 fs 2 105.46 fs 2 105.46 fs 2 105.46 fs 2 103.72 fs 2 103.72 fs 2 103.75 fs 2 75.57 fs 0 8 5 0.00 fs 5 0.05 fs 5 0.36 fs 5 0.	em S1 bit get Contr. 153.10 k Nose (Strandy) Phases Rendom Neise RN(v) (NSS) RN(v) (NSS) RN(v) (NSS) RN(v) (NSS) Colt Colt Colt Colt Colt Colt RN(v)	Channel: Fable Boalsberr, Nore Boalsberr, Nore	Acquisition ActoSync to Sele Source Source Source SSC is present Recommended Outs Pattern Rate 2	Intel Source	· D#	Vlavelength Filter Bandwicth Pattern Clock Source Plase Patere Source	Cock/Prec	4	+ + +	- III	
Data Source #MR1 Soc; Off Phase Reference: 12,2495 GH Bitted Education Threeholds & Bitted Education Threeholds & Ref (1) (845) Ref (1) (845) CO OC OCO OCO Bitted (1) (845) Ref (1) (84	Patt z San 4.40 mV) = 251.06 fs = 227.42 fs = 105.64 fs = 1.13 ps = 123.72 fs = 123.72 fs = 2.56 ps = 123.72 fs = 273.57 fs = 0 s = 50.00 fs = 50.00 fs = 50.00 fs = 50.00 fs = 50.00 fs	em: S11 bit epic Contr. 151.0 k Kons (Standbog Phases Endom Netrice RN(v) (RNS) RN(v) (RNS) RN(v) (RNS) Endom Netrice Deterministic Noise DA DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) DON(evel 1) RN(v)	Chandl: Fable Bealter: None 5.02 million 5.02 million 6.01 Million 6.01 Million 6.01 Million 1.17,23 million 1.17,23 million 1.17,24 million 9.98 million 7.77,21 million 9.98 million 9.99 million 9.99 million 9.99 million 9.99 million 9.99 million 9.99 million 9.90	Acquisition ActoSync to Sele Source Source Source SSC is present Recommended Outs Pattern Rate 2	Intel Source	· D#	Vlavelength Filter Bandwicth Pattern Clock Source Plase Patere Source	Cock/Prec	4	+ + +	- III	



Host Transmitter Test Setup



* See application note 071-3207-XX for information about the cables and interconnect accessories required for this setup.

[‡] Or 80N01 Extender





Option CEI-VSR Recommended Test Equipment

Platform	DSA8300
Software Options	 Option CEI-VSR - OIF CEI 3.0 Compliance Solution for DSA8300 Option JNB01 - 80SJNB ADVANCED Option ADVTRIG - Advanced triggers with pattern sync
BERTScope [®] Clock Recovery	CR286A
Remote Sampling Scope Module	80E10B - 8000 Series, Dual Channel, 50 GHz, Remote Electrical Sampling Module w/ TDR (includes D1) OR 80E09B - 8000 Series, Dual Channel, 60 GHz, Remote Electrical Sampling Module (includes D1)80E10/B** ** Will not support TDR based measurement
Phase reference module	82A04B - 8000 Series, Phase Reference Module (includes D1)
Module Extender Cable	Module Extender Cable : 1 # 80X01 & 1 # 80X02(Status : Please contact Product Marketing for availability and Status)
Other Accescories	 2 # Trigger Pick-off T 2.4 mm M-F-F 5361-237-14DB(PSPLabs) 6 # 50mm Cable, 2.4 mm M-M SF1611-60003(SV Microwave) 2 # DC Block 2.4 mm M-F 5509-205-224(PSPLabs) 2 # 2.4 mm F-Crown PN 7005A-12(Aeroflex) 2 # 420 mm Cable 2.4 mm M-M, SF1611-60003(SV Microwave)





Tektronix 80B28G Bundle Elements



CR286A



82A04B Phase Reference Module and Std. Accessory 80X02 2 Meter Extender Cable



80A08 Accessory Kit







Practices for Measurements on 25 Gb/s Signaling **Application Note** 86W-29118-x



80E09B 60 GHz, Dual Channel **Remote Sampling Module**



80X01 1 Meter Extender Cable



Tektronix LE320/LE160 32 & 16Gbps Linear Equalizer Product Introduction

- Compact two channel 32Gbps 9 Fixed Tap linear equalizer design in a "remote module" configuration
- +/-20dB tap controls offer flexible preemphais or channel de-embed capabilities.
- User (and PI) configurable filter properties allows flexible parametric equalization
- Electronically switchable frequency dependent filter capability permits DDJ tolerance testing and testing against known reference channel models
- Front-end signal path (CTLE) for Sampling or BERT Instruments







Rx/Tx testing for Industrial HSSD at 100G Key Value Propositions

- BSA286C:
 - Support for rates through 29G offer 3% margin over standard base spec's.

		100GBase-	32G	
Key Comms	100GBase-	XR4	Fibre-	
Rates	XR4	(FEC)	Channel	CEI
Rate	25.7813	27.7390	28.0500	28.0500
I UI (period)	38.7879	36.0500	35.6500	35.6500
Allocated Rj (UI)	0.13	0.13	0.14	0.13
Rj in Psec RMS	0.3602	0.3348	0.3565	0.3310

- <300pSec RMS Rj allows following the J2 and J9 jitter intercepts with margin.
- DSA8300: ~100fSec Jitter measurements.

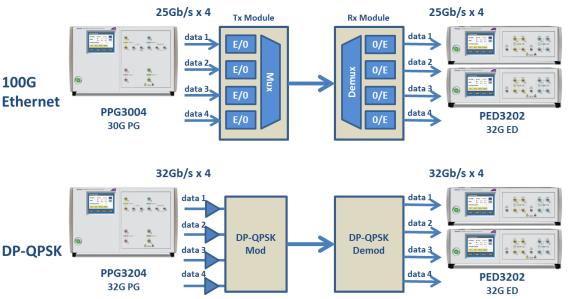
Data Source: CH1		Data Rate: 2	28 Gbps	Filter: False	e	Total Jitter @ BER			Total Noise @ BER		
SSC: Off		Pattern: 127	' bits	Channel: F	alse	TJ (1E-12)	=	5.92 ps	TN (1E-12)	=	220.38 m
Phase Reference: 7 GHz		Sample Cou	nt: 52.70 k	Equalizer:	None	Eye Opening (1E-12)		29.79 ps	Eye Opening (1E-12)	=	60 4 60 V
Jitter (Decision Threshold: -)	7.73 mV)		Noise (Sampling Phase:	0 UI)		, , , , ,			Eye Amplitude	=	905.27 m
Random Jitter			Random Noise			Dual Dirac			SSC Modulation		
RJ (RMS)	=	199.01 fs	RN (RMS)	=	4.98 mV	RJ(d-d)	=	223.73 fs	Magnitude	=	0 ppm
RJ(h) (RMS)	=	160.06 fs	RN(v) (RMS)	=	4.98 mV	DJ(d-d)	=	2.77 ps	Frequency	=	0 Hz
RJ(v) (RMS)	=	118.26 fs	RN(h) (RMS)	=	108.30 u\	DJ PDF			DDJ vs Bit		
Deterministic Jitter			Deterministic Noise			0.05			A JA MALE A A MALE O	-ihm.	6 8 16 . 16
DJ	=	3.59 ps	DN	=	161.33 m	0.04-			2 ps - 10 - 10 - 10 - 10 - 10 - 10 - 10 - 1	1	
DDJ	=	3.17 ps	DDN	=	155.62 m	0.02 -			°-∿-JMML V MML	\mathcal{M}	∽ ₩
DCD	=	198.77 fs	DDN(level 1)	=	144.05 m				-2 ps - 41 (1 - 1 - 1 - 4 - 4) (1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	1.1.1	111
DDPWS	=	1.13 ps	DDN(level 0)	=	171.04 m	BER Batht	ub	5 ps	^{30 ns 31} BER ² Eye	33	34 ns
P]	=	144.94 fs	PN	=	4.53 mV			······	600 mV - 400 -		
PJ(h)	=	97.27 fs	PN(v)	=	4.53 mV	윤 표 -10			200 -	-	
PJ(v)	=	107.46 fs	PN(h)	=	65.82 uV	ي ۲۰۱۶	······ <mark>/</mark> ·		-200 -		
		/				-20 -	••••••		-600 mV		
KEITH	LΕλ					-20 ps 0		20 ps		20	202

A Tektronix Company

What is PatternPro?

- PatternPro is a line of serial data instruments targeted at high-speed BERT testing. Designed to specifically address:
 - Multi-channel testing (4 lane BERT for 100GE and coherent)
 - High-speed NRZ testing (roadmap to 56 Gb/s)
 - Multi-level testing (PAM4 and DP-QPSK QAM16)
- Product line emphasis is on highperformance, value, and ease of use
- Separate instruments for PPG and PED
- PC GUI software to control instruments and perform analysis



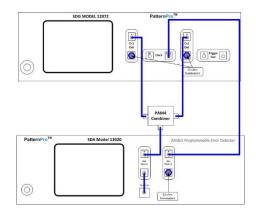


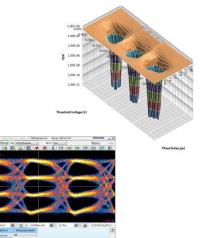
Typical Multi-lane Test Configurations



32G PAM4 BERT System

- Industry's first high-speed PAM4 BERT!
- PSPL products assembled into bundled system
 - Programmable pattern generator
 - Programmable error detector
 - Analysis software
 - PAM-4 accessory kit
- PAM4 Signal Generator
 - Aligned channels simplify multi-level signal generation
 - User-programmable data patterns allow test of PAM4 custom data
- PAM4 Analyzer
 - BER measurements analyzes every bit of each pattern
 - Contour plots, bathtub curves, total jitter analysis via software tools









NRZ Optical Test Solutions



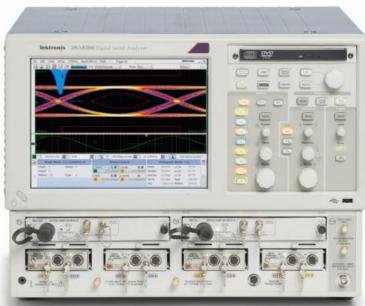




Introducing the DSA8300 Digital Serial Analyzer More Performance and Versatility

- Industry's best native time-base jitter performance, 425 fs _{RMS} typical (on up to 8 simultaneously acquired channels)
- 100 fs RMS time-base jitter when equipped with the 82A04B
- 16,000 point native record length
- 16 bits of vertical resolution
- Optional fully integrated pattern synchronization (replaces 80A06)
- 4X Pattern Sync throughput improvement
- Clock Pre-scalar maximum input frequency 20 GHz typical
- 3 GHz Intel Core 2[™] Duo CPU
- New user interface look and feel leveraging MS Windows 7 Ultimate Operating System
- XVGA (1024 X 768) 10.4 inch display







DSA8300 Digital Serial Analyzer DSA8300 Optical Module Portfolio

Single and Multi-mo	ode, Broad Wavelength (750 - 1650 nm) Modules
80C07B	Supports standard rates to 2.7 Gb/s, high sensitivity, optional integrated clock recovery
80C08D	Supports all of the 8/10 Gb/s applications, high sensitivity, optional integrated clock recovery, optional Integrated CR
80C12B	Supports standard rates from 155 Mb/s – 11.3 Gb/s, high sensitivity - data pick-off for external CRU e.g. CR125A
80C14	Supports rates from 8.5 Gb/s – 14.063 Gb/s, high sensitivity – data pick-off for external CRU e.g. CR175A
80C15	Supports standard rates from 25.73 Gb/s – 28.05 Gb/s (maximum optical bandwidth > 32 GHz)

Single-mode, Long	g Wavelength (1100 - 1650nm) Modules
80C11B	Optical bandwidth to 30GHz, supports 10Gbit/s up to14G+ standards, optional Integrated CR
80C10C	Optical bandwidth to 80GHz, supports all 40 and 100 Gb/s (4 x 25 Gb/s) standards, optional CR trigger pickoff for e.g. CR286A CRU, optional high sensitivity photo-receiver for use with external equipment (e.g. for optical BER testing with BERTScope)
KEITHLEY	Tektronix

A Tektronix Company

155 Mb/s to100 Gb/s Optical Compliance Testing DSA8300 ALL-IN-ONE Solution

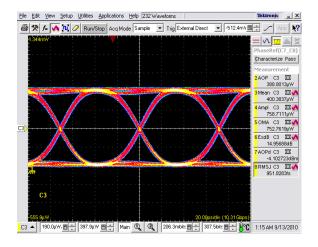
Tektronix DSA8300 All-In-One System

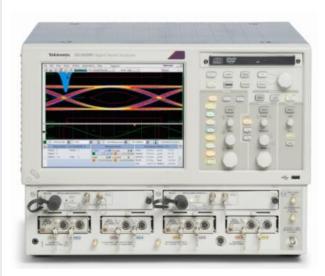
+ 80C12B Optical Module (155 Mb/s to 11.3 Gb/s)
+ 80C10C-F1 Optical Module (25.7 Gb/s to 44.5 Gb/s)

+ 2 slots available to acquire 4 electrical signals

The Only ALL-IN-ONE Solution with:

- All major ORRs from 155 Mb/s thru 44.5Gb/s
- Highest repeatability & best sensitivity
- SMF and MMF support to 12G
- Up to 3x throughput advantage vs. alternative
- 425 fs _{RMS} native jitter
- 100 fs _{RMS} jitter when equipped with 82A04B
- Integrated clock recovery trigger pickoff
- Clock recovery available via Tektronix CR286 (to 28.6 Gb/s), or third party (to 44.5 Gb/s)









All-in-One Optical Test Feature Summary

The 80C12B Optical Modules provides:

- Support for all major rates from 15 Mb/s to 11.3 Gb/s
- Low-noise, wide dynamic range
- Excellent optical sensitivity

80C10C Optical module

- Support both 25 Gb/s and 40 Gb/s in a single module
- Superior noise performance

The DSA8300 ALL-IN-ONE Solution Provides

 Support for all major rates from 155 Mb/s to 44.5 Gb/s

Integrated and Calibrated Clock Recovery

- Tektronix CR286A up to 28.6 Gb/s
- Third party CRU to 44.5 Gb/s

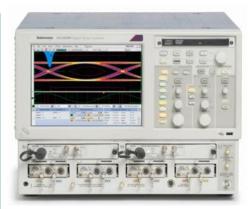


Standard	Line Rate	80C12B	80C10C Opt F1
OC-3/STM-1	155 Mb/s		
OC-12/STM-4	622 Mb/s		
FC1063	1.0625 Gb/s		
ENET1250	1.250 Gb/s		
FC2125	2.125 Gb/s		
OC48//STM48, GBE, INF2500	2.488 Gb/s 2.500 Gb/s		
FEC2.666	2.666 Gb/s		
!0GBASE-X4, FC3188	3.125 Gb/s 3.188 Gb/s		
FC4250	4.250 Gb/s		
INF5000	5.000 Gb/s		
OBSAI6144	6.144 Gb/s		
CPRI7373	7.373 Gb/s		
FC8500*8, OC-192/STM-64, 8GFC, 10GBASE- W, 10GBASE-R, 40GBASE-R4, 100GBASE-R10, 10GFC, FEC10.66, FEC10.71, FEC11.10, FC11317	8.500, 9.95,10.31, 10.51,10.66,10.71,11.1, 11.3 Gb/s ORR Filters plus Unfiltered bandwidth path (typically 12 GHz)		
100GBase-LR4, 100GBase-ER4 Infiniband EDR (LW)	4 x 25.781 Gb/s		
SONET/SDH OTU4	4 x 27.95 Gb/s		
40GBase-FR	41.25 Gb/s		
OC-768 / STM-256, VSR-2000	39.813 Gb/s		
OTU3 (OC-768 + G.709 FEC), VSR-2000 , 4x10G LAN-PHY (OTU3)	43.018 Gb/s 44.50 Gb/s		

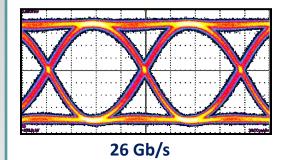
Tektronix 80C15 Optical Sampling Module

<mark>v = 80C15</mark>

- Single-Channel Optical Plug-in Module for DSA8300
- Unfiltered Optical Bandwidth >32 GHz
- 9/62.5/125 µm Single-/Multi-Mode Fiber Input
- Short- and Long-Wavelength Support 780-1650 nm
- 200 kS/s Acquisition Rate
- Jitter Floor <150 fs_{RMS} (with 82A04B)
- Reference Receiver Filters:
 - ✓ 32G FibreChannel (28.05 Gb/s)
 - ✓ OTU4 (27.95 Gb/s)
 - 100Gbase-LR4/ER4/SR4 (25.78 Gb/s)
 - 26G EDR Infiniband (25.78 Gb/s)











Coherent Optical Comms







Coherent Optical Modulation Why/What/How is it Tested?

Why coherent modulation?

Demand for long-haul network bandwidth is growing at an exponential rate due to the increased consumption of video content on mobile devices, streaming media to the home, and the transformation of the internet. Coherent technology allows 40G and even 100G transmission over existing 10G infrastructure. This allows network operators to increase their network capacity with a relatively small capital investment.

What is coherent modulation?

Traditional 10G transmissions modulate the amplitude of the light, a.k.a. or on-off keying (OOK). Direct detection is used in the receiver.



Coherent transmissions modulate the phase of the light, the simplest case is phase shift keying.



By doubling the number of phase states, the bit/symbol rate is also doubled.



QPSK

Quadrature Phase Shift Keying 2 bits/symbol

Rotating the polarization of one QPSK signal, and combining it with a second QPSK signal, doubles the bit/symbol rate again.



4 bits/symbol

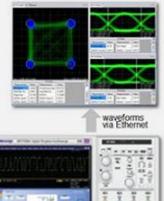
Other formats are also used such as Differential QPSK (DQPSK), 8-PSK, and Quadrature Amplitude Modulation (QAM).

What are the **benefits** of coherent modulation?

- · The channel bit-rate can be quadrupled (when using DP-QPSK), without increasing bandwidth, through existing fiber infrastructure.
- · Linear digital filtering can now compensate for major sources of degradation such as Chromatic Dispersion (CD) and Polarization Mode Dispersion (PMD).
- 4.3dB improvement in noise tolerance compared to direct detection.

How is coherent modulation tested?

The OM4106D software transforms the digitized electric field and displays the original tributary waveforms. The SW provides specialized visualization tools and measurements.



.....

.

A scope (RT or ET¹) digitizes the electric field.

coherent optical input (fiber) An Optical Modulation Analyzer (OMA), such as the OM4106D converts the optical signal into a dual-polarization electric field.

*For more information on how to choose an RT or ET scope, see the Choosing an Oscilloscope for Coherent Modulation Analysis technical brief.

Tektronix[•]

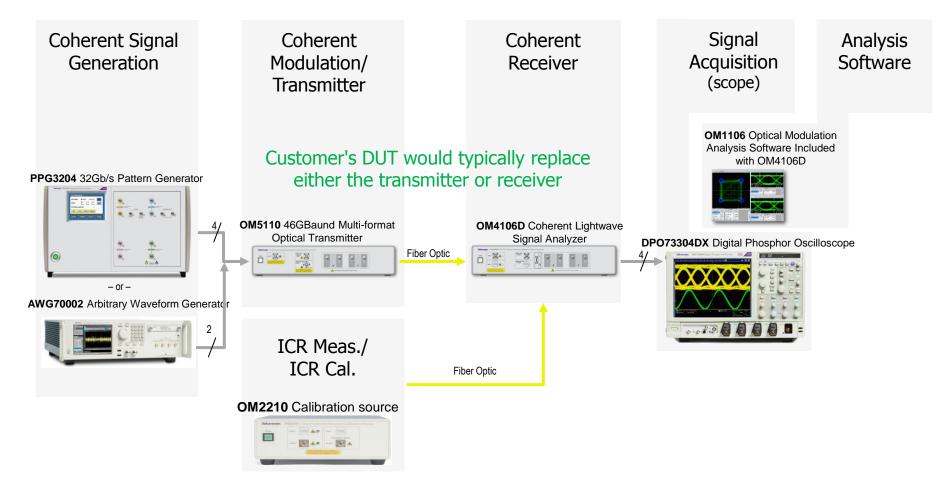
electric field

to scope





Coherent Optical System



Tektronix offers complete end-to-end testing of coherent modulation formats.





Tektronix 100G Comprehensive Testing Solutions



- DSA8300 Sampling Oscilloscope >70GHz Bandwidth

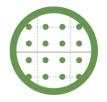
 - <100 fsec jitter noise</p>
 - Pass/Fail at high throughput
 - BUJ-Based Jitter Analysis



- BSA286C Bit Error Rate Tester
 - 28.6 Gb/sec Data Rate
 - Low intrinsic jitter
 - Stressed, calibrated PRBS31 patterns
 - Error location & Jitter Analysis



- PatternPro BERT Instruments
 - 40 Gb/sec Data Rate
 - Up to 4 synchronized channels (PG + ED)
 - Low intrinsic jitter
 - Stressed, calibrated PRBS31 patterns



- OM4000 Coherent Lightwave Analyzer
 - DP-QPSK Analysis
 - Constellation Mapping to BER
 - Works with RT or ET Scopes













Tektronix®



