# 泰克2014年春季创新论坛

数字高清接口HDMI2.0/DP1.2的测试挑战以及解决方案







# Agenda

- HDMI Overview and updates
- HDMI 2.0 Solution
  - HDMI2.0 Source Testing
  - HDMI2.0 Sink Testing
- DisplayPort 1.2 Overview
  - DisplayPort Transmitter Testing
  - DisplayPort Sink/Receiver Testing
- eDP testing for eDP 1.4 specification





# HDMI – High Definition Multimedia Interface Overview







#### Overview of HDMI

- From 2003 till date and looking ahead...
  - Tek only solution provide for HDMI from 2003 to 2007
  - Contributor of SoftCRU method to the Specification
  - Innovative Sink solution leveraging Direct Synthesis method of AWG
- HDMI 1.0 ----- 1.65GBps
- HDMI 1.4 ---- 3.4GBps
- HDMI 2.0......6GBps

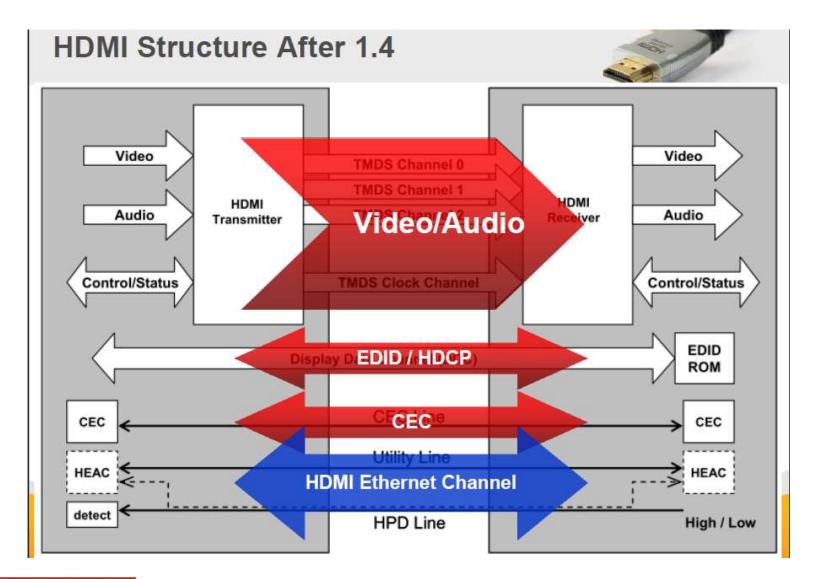








### **HDMI** Basics





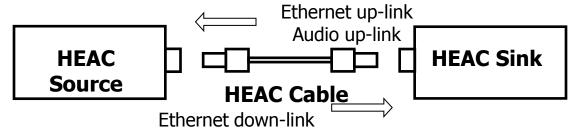


# **HDMI Technology and Solution Status**

Over 1000+ adopters till date

Source: HDMI LLC

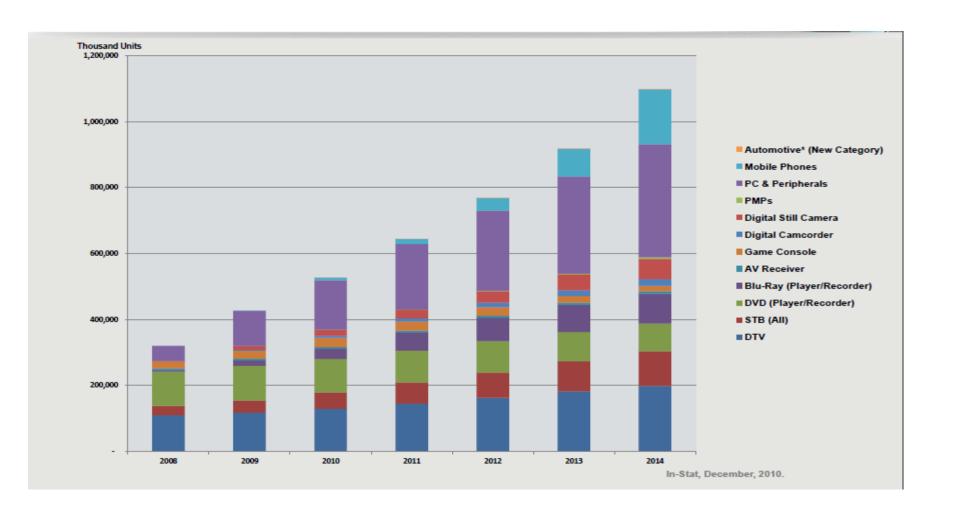
- HDMI Expands Footprint
  - HDMI has made inroads into PC industry
    - New computer platforms have HDMI interfaces
  - Hand held devices with miniature HDMI devices
    - New connectors Type C and Type D introduced
  - HDMI Forays into Automotive Type E
  - Year 2011 3D Year
  - Still camera
  - Advertising billboards
- HDMI NOW Truly Single Digital Interconnect for uncompressed Audio/Video
  - HEAC (ARC)







### **HDMI Market Overview**







# Tektronix HDMI 1.4b Solution- Approved in CTS 1.4b

#### DPO/DSA/MSO Real Time Oscilloscopes



# AWG5K/B or AWG7K/B Arbitrary Waveform Generators



# DSA8300 Sampling Scope with i-connect software



Common Set of test equipment for HDMI and HEAC

#### **HDMI Fixtures:**

- 1. Type A( TF-HDMI-TPA-S/-STX)
- 2. Type C(TF-HDMIC-TPA-S/-STX)
- 3. Type D( TF-HDMID-TPA-P/-R)
- 4. Type E(TF-HDMIE-TPA-KIT)
- 5. HEAC Fixtures(TF-HEAC-TPA-KIT)

#### **Probes and Accessories**

HDMI Probes HEAC Probes HDMI Accessory Kit





#### Tektronix and HDMI Forum

- Due to the HDMI Specifications' overwhelming success, the HDMI Founders created an organization where interested companies can participate in the future development of the HDMI Specification.
- On October 25, 2011, the HDMI Founders announced the launch of the HDMI Forum, 89 companies in the HDMI forum as of date.
- Tektronix is member of this HDMI Forum. Actively participating in weekly/monthly calls and face-face meetings
- Tektronix's U.N.Vasudev is chairman of HDMI forum test subgroup
- HDMI Forum has released the HDMI specifications 2.0 version 1.0 on 4<sup>th</sup> Sept 2013 and Compliance Test specifications 2.0 version on 11<sup>th</sup> Apr. 2014.

High-Definition Multimedia Interface Version 2.0 Compliance Test Specification

April 11, 2014

DM: Newson

Page 3.4

HDMI2.0 CTS

tigh-Definition Multimedia Interface

Specification Version 2.0

September 4, 201

CONFIDENTIAL

60Millores :

Deliberty

CAPT DESIGN

HDMI2.0 spec.





#### HDMI 2.0 Features

- Uses same Cat 2 Cable and HDMI 1.4b connector
- Support 4K 2K 4:4:4 60/50 Hz 594MCSC(Mega Characters per Second per Channel)
- Support 4K 2K 4:2:0 297Mcsc
- 3D; 21: 9; Audio
- Low level Bit error rate testing
- Scrambling is introduced and mandatory for rates >340Mcsc.





# **HDMI2.0 Source Testing**







## **HDMI 2.0 Source Testing Equipment Needs**

Table 4-24 Source AC Characteristics at TP1

Item	Value
Rise time / fall time (20%-80%)	if attached Sink supports < 340MHz
	75psec ≤ Rise time / fall time
	if attached Sink supports ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz
	42.5osec ≤ Data Rise time / Data fall time
	75psec ≤ Clock Rise time / Clock fall time

<u>Item</u>	<u>Value</u>
Rise time / fall time (20%-80%)	if attached Sink supports ≥ 340MHz and transmitted TMDS Character Rate ≥ 340MHz
	42.5psec ≤ Data Rise time / Data fall time
	75psec ≤ Clock Rise time / Clock fall time

HDMI 1.4 RT/FT (20%-80%) data signals is 75ps

- HDMI 2.0 RT/FT (20%-80%) data signals is 42.5ps
- 16GHz BW scope will give 1% error and hence is recommended for HDMI 2.0 testing.
- P7313SMA probes (same used in HDMI 1.4b)
- Option HDM and HDM-DS
- HDMI 2.0 Fixture set

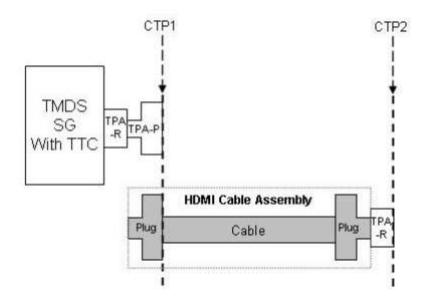
<sup>\*\*\*</sup>Note- We shall also support a 12.5GHz BW scope which would result in appx. 10% inaccuracy in RT/FT results .





## Source Testing 1.4b Vs 2.0

- Eye Diagram and Clock Jitter test is now performed at TP2
- Rest of the tests is same as HDMI 1.4b.
- 1.4b CTS test is a pre-requisite for HDMI 2.0
- Min 8GHz scope to 16GHz scope
- New Fixtures
- Same Probes
- HDM and HDM-DS Software

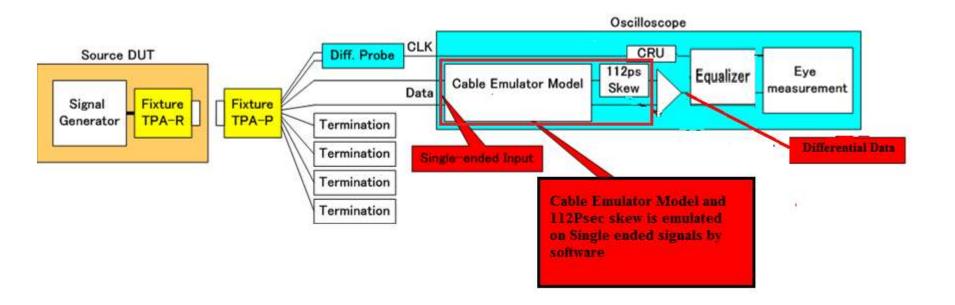






## Source Testing

- Source Eye Diagram test is measured at TP2\_EQ.
- TP2 is the signal after passing along a worst cable.
  - Worst cable has worst attenuation and skew of 112ps.







#### Source Electrical Test Items

- Test ID HF1-1: Source TMDS Electrical 340-600Mcsc V<sub>L</sub>
- Test ID HF1-2: Source TMDS Electrical 340-600Mcsc T<sub>RISE</sub>, T<sub>FALL</sub>
- Test ID HF1-3: Source TMDS Electrical 340-600Mcsc Inter-Pair Skew
- Test ID HF1-4: Source TMDS Electrical 340-600Mcsc Intra-Pair Skew
- Test ID HF1-5: Source TMDS Electrical 340-600Mcsc Differential Voltage
- Test ID HF1-6: Source TMDS Electrical 340-600Mcsc Clock Duty Cycle
- Test ID HF1-7: Source TMDS Electrical 340-600Mcsc Clock Jitter
- Test ID HF1-8: Source TMDS Electrical 340-600Mcsc Data Eye Diagram
- Test ID HF1-9: Source TMDS Electrical 340-600Mcsc Differential Impedance





# Source Eye Diagram Test

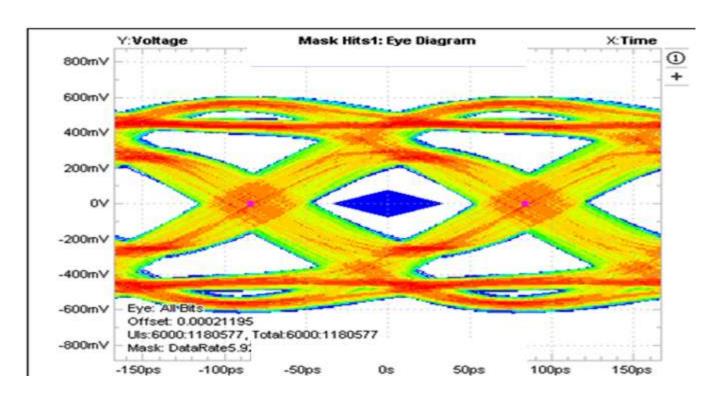
DPO/DSA/MSO70000 Series ≥ 16GHz Include Reference Cable Emulator (s4p) and Reference Cable Equalizer Diff Clk SE Data Clk + Clk -Data + **Data SMA Pair Cable HDMI Source** HDMI Plug Fixture with EDID Emulator





Tektronix Oscilloscope

# TP2 Source Eye for HDMI 2.0 6G Signal



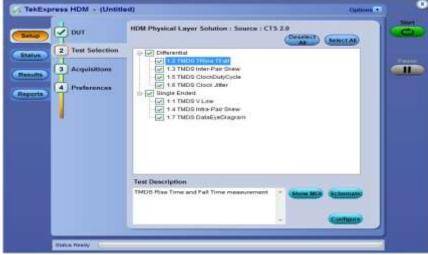
Single End Input eye rendered at Tek lab





# HDMI 2.0 Tx Compliance Software(Option:HDM)











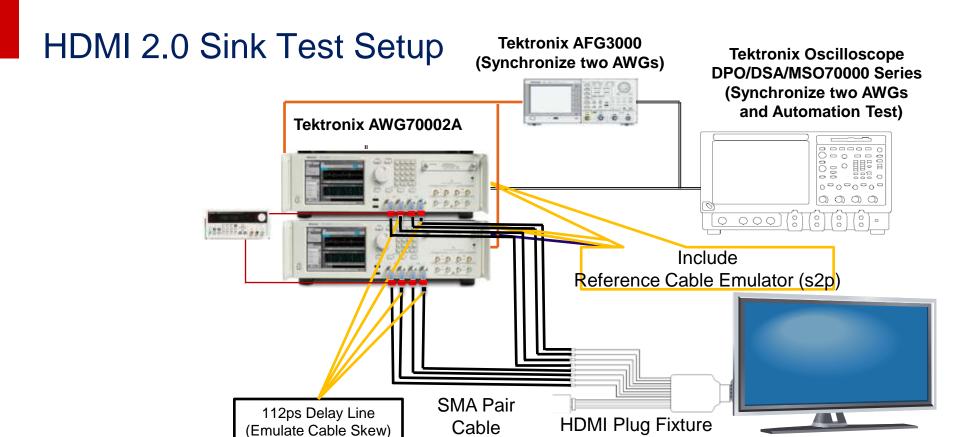


# HDMI2.0 Sink Testing













**HDMI Sink** 



#### Sink Electrical Test Items

- Test ID HF2-1: Sink TMDS Electrical 340-600Mcsc Min/Max Differential Swing Tolerance
- Test ID HF2-2: Sink TMDS Electrical 340-600Mcsc Intra-Pair Skew
- Test ID HF2-3: Sink TMDS Electrical 340-600Mcsc Jitter Tolerance
- Test ID HF2-4: Sink TMDS Electrical 340-600Mcsc Differential Impedance (performed using sampling scope)





# Sink Testing 1.4b Vs 2.0

- Jitter Tolerance test needs +ve and –ve lanes tested with 112ps delay line
- Rest of the tests is similar to HDMI 1.4b tests
- 1.4b CTS test is a pre-requisite for HDMI 2.0
- Need AWG 70002A for HDMI 2.0 Compliance and Margin needs while AWG7122C is suitable for HDMI 2.0 Compliance testing only..
- Min 8GHz scope to 16GHz scope
- Fixtures and Probes
- HDM and HDM-DS Software





## HDMI 2.0 Sink testing Equipment needs

- 16GHz BW scope will give 1% error and hence is recommended for HDMI 2.0 Sink testing for Jitter Verification/Calibration/Controller.
- P7313SMA probes
- Option HDM and HDM-DS
- HDMI 2.0 Fixture set
- 2# AWG7122C with Opt 01,02 or 06, 08 for HDMI 2.0 Compliance only setup.

OR

 2# AWG70002A with Opt 01,03 and 225 for HDMI 2.0 Compliance and Margin Test setup.(Margin test feature will be available later and is part of roadmap)

\*\*\*Note- We shall also support a 12.5GHz BW scope which would result in appx. 10% inaccuracy in RT/FT results.





# HDMI 2.0 Rx solution positioning statement

- Tektronix will support HDMI 2.0 Sink <u>Electrical and protocol</u> tests using either AWG7122C (w/ Opt 01,02/06,08) AND AWG70002A (W/ Opt 01,03,225)
- Solution Positioning:
  - Compliance solution for HDMI 2.0 Rx
    - 2# AWG7122C with opt 01, 02/06 and 08
    - 1# AFG3102/C

Customers can use common test setup for HDMI 1.4b and HDMI 2.0 giving value for their investment in Tektronix HDMI 1.4b Rx solution.

- Compliance and Margin solution for HDMI 2.0 Rx
  - 2# AWG70002A with Opt 01,03 and 225.
  - 1# AFG3102/C

Customers can <u>use common test setup</u> for HDMI 1.4b and HDMI 2.0 giving value for their investment in Tektronix HDMI 1.4b Rx solution





#### Tektronix HDMI 2.0 Solution

- DPO/DSA/MSO 70004B/C/D/DX Series Real Time Oscilloscope with BW ≥ 16GHz (we also support 12.5GHz BW scope for HDMI 2.0) with Opt 10XL, Opt DJA, Opt SR-EMBD and SR-CUST.
- HDMI 2.0 Advanced Analysis and Compliance Software for Source Option HDM (will need Opt HT3 as HDMI 1.4b testing is a pre-requisite for HDMI 2.0)
- HDMI 2.0 Advanced Analysis and Compliance Software for Sink Option HDM-DS (this needs Opt HDM and will need Opt HT3-DS as HDMI 1.4b testing is a pre-requisite for HDMI 2.0).
- Probes P7313SMA (Four)
- HDMI 2.0 Test Fixture Available from Third Party.
- AWG70002A with Opt 01,03 and 225 (Qty.2) OR AWG7122C with Opt 01,02 or 06 and 08 for the innovative direct Synthesis based HDMI 2.0 Sink Testing.
- DSA8300 or Equivalent with 80E03/80E04 and I-Connect Software for HDMI cable testing (performed manually using MOIs)

Please contact local Tektronix account managers for further details.





# DisplayPort 1.2 Overview







# DisplayPort – Technology Overview

#### DisplayPort is expanding its foot print

- Standard DisplayPort
  - Specification Version 1.2
  - CTS Version 1.2b
  - Data Rates 1.62GBps, 2.7Gbps and 5.4Gbps
  - Box to Box (1, 2, 4 lanes)
- eDP
  - Specification Version 1.4
  - CTG in progress
  - Data Rates 1.62Gbps to 5.4Gbps
  - Embedded(single box Laptops) (1,2,4 lanes)
- MyDP
  - Specification Version 1.0
  - CTS Version 1.0 (in approval)
  - Data Rates 1.62GBps, 2.7Gbps and 5.4Gbps
  - Mobiles (1 lane)
- iDP
  - Specification Version 1.1
  - CTG
  - Data Rates 3.24 , 3.78
  - LVDS replacement







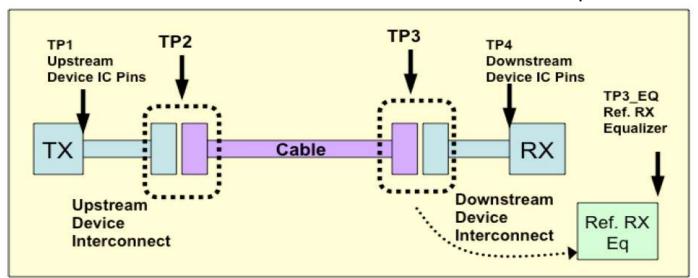




## DisplayPort 1.2 Overview

- The DisplayPort PHY Compliance
   Test Specification establishes a test
   regimen to determine compliance of
   DisplayPort devices segmented into:
  - Source
  - Receiver
  - Copper Cable
  - Hybrid devices
  - Tethered devices

- Test Point Definitions
  - TP1: at the pins of the transmitter device.
  - TP2: at the test interface on a test access fixture
  - TP3: at the test interface on a test access
  - TP3\_EQ: TP3 with equalizer applied.
  - TP4: at the pins of a receiving device







# DisplayPort Transmitter Testing







# DisplayPort CTS1.2b

#### **Source Test Suite**

- 1. EYE Diagram
- 2. Non Pre-Emphasis Level Verification
- Pre-Emphasis Level Verification and Maximum Differential Pk-Pk Output Voltage
- 4. Inter-pair Skew
- Intra-Pair Skew
- Differential Transition Time
- 7. Single Ended Rise and Fall Time Mismatch
- Overshoot and Undershoot Test
- 9. Frequency Accuracy
- 10. AC Common Mode Noise
- 11. Non ISI Jitter Measurement
- 12. Total Jitter and Random Jitter Measurement
- 13. Unit Interval
- 14. Main Link Frequency Compliance Stability
- 15. 1Spread Spectrum Modulation Frequency
- 16. Spread Spectrum Deviation
- 17. dF/dt Spread Spectrum Deviation HF Variation
- 18. Dual-mode TMDS Clock (NOW supported)
- 19. Dual-mode EYE Diagram Testing (NOW supported)
- 20. AUX lane Eye Diagram(NOW supported)
- 21. Aux lane Rx sensitivity(NOW supported)

#### **DUT Configuration**

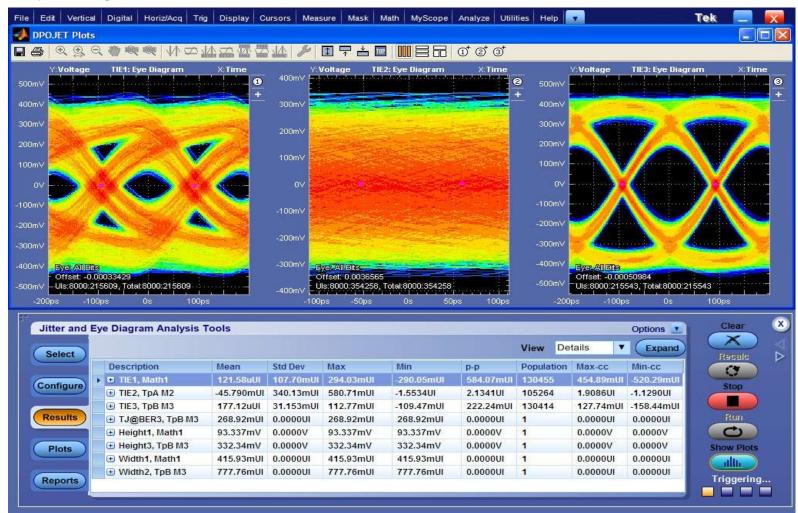
- 1. Bit Rates: RBR, HBR or **HBR2**
- 2. Patterns: D10.2,PRBS7, COMP,
- PLTPAT,PCTPAT
- 3. FFE (Pre-Emphasis): 0dB, 3.5dB,
- 6dB, 9.5dB
- 4. Output Levels: 400mV, 600mV,
- 800mV, 1200mV
- 5. SSC (Spread Spectrum): On/Off
- 6. Post-Curser2: Level 0,1,2,3
- 7. Lane Width, 1,2,4





# Eye Diagram Test using Eye Compliance Pattern

An Eye diagram test for 800mV, 0dB pre-emphasis at TP2,TP3, TP3-EQ.

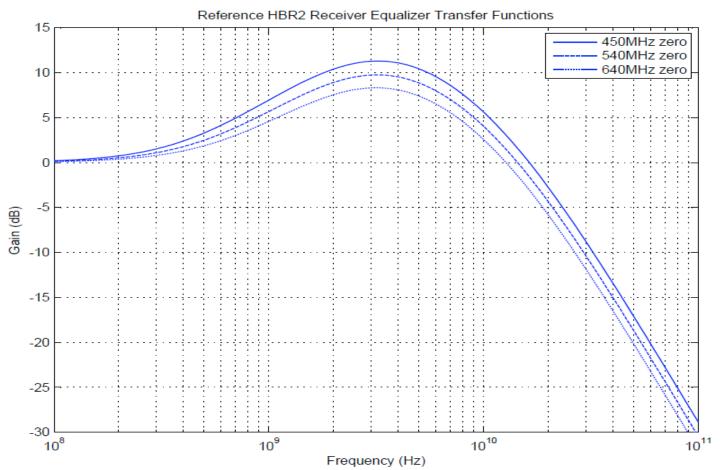






# DisplayPort 1.2 CTLE Properties

1.2 CTS requires adaptive application of one of three reference equalizers to the far end signal, to find a passing condition.







# Key Elements of DisplayPort 1.2 Transition: Eye Diagram/Mask

1.2 CTS Requires Adaptive Eye Diagram

A Tektronix Company

- Find the highest vertical eye point between .375 -- .625 UI at 10E-9BER
- Analytical tools which examine the vertical noise components project the Rn components to 10E9 BER. These tools have been proven in the field in SATA where they have been deployed for over two years.

Table 3-19: DisplayPort Main Link Transmitter (Main TX) TP3 EQ Parameters

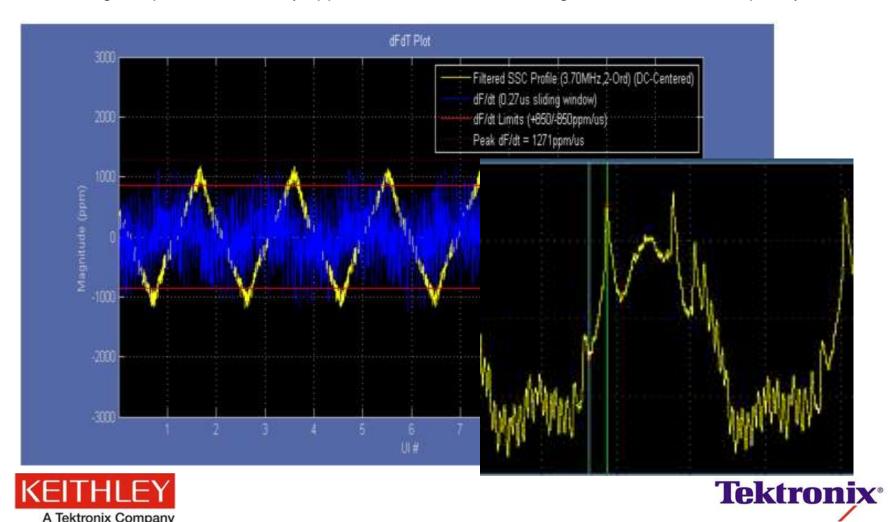
TX TP3 EQ (Compliance Cable Model with HBR2 Reference Receiver Equalization - Normative) Parameter Min Nom Max Units Comments Symbol FyeDiagram & Bathtub after CIC Maximum TX Total Jitter 0.62 TTX-TJ 86106 HBR2 For HBR2. Measured at 1E-9 BER using the HBR2 Maximum TX 0.49 TTX-DJ 86106 HBR2 Compliance EYE pattern. Deterministic Jitter Maximum TX Total Jitter 0.40 TTX-TJ D10.2 HBR2 Maximum TX For HBR2. Measured at 1E-9 0.25 TTX-DJ D10.2 HBR2 BER using the D10.2 Deterministic Jitter compliance pattern. Maximum TX Random 0.23 UI TTX-RJ\_D10.2\_HBR2 For HBR2. Measured at 1E-9 TX Differential Peak-to-BER using the HBR2 110 TTX-DIFFp-p\_HBR2 Peak EYE Voltage Compliance EYE pattern. For HBR2. Uses 0.5 CDF of the jitter distribution as the OUI TX Differential Peak-toreference point. TX TTX-DIFFP-0.375 0.625 Peak EYE Voltage Differential Peak-to-Peak EYE BER (O-Scale) p RANGE HBR2 Measurement Range Voltage requirement can be met anywhere within this UI 6 to 12 BER = 59.57 tps/0.36U

Min Diff Valtage Amplitude & BER = 647.29mVM



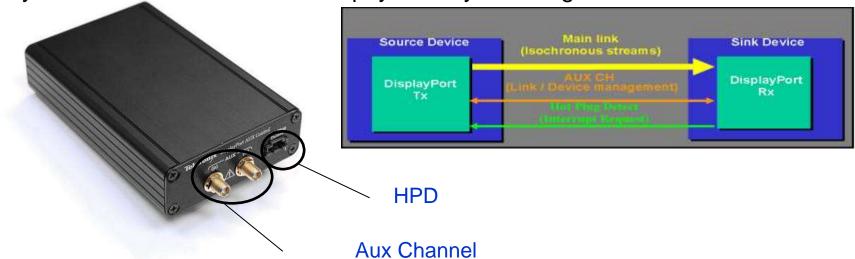
# Key Elements of DisplayPort 1.2 Transition: dFdT

While dFdT measurements have a unique origin emerging from the SATA and SAS specifications where the history of examining SATA dFdT has led this to become a highly recommend analysis. The dFdT contributing components will rarely appear in the normal Jitter budget due to their low frequency nature.



# DisplayPort Auxiliary Channel Controller (DP-AUX)

Why use Aux channel controller in physical layer testing?



- Speeds Up Test Time No User Interaction is Required to Change Source Output Signal or Validate Sink Silicon State or Error Count
- No Need to Learn Vendor-specific Software A Single GUI Supports All Vendors
- •View & Log Decoded AUX Traffic and Hot Plug Detect (HPD) Events from the Device under Test to the DP-AUX DisplayPort AUX Controller
- Ability to Read and Write DPCD Registers Supports Debug Activities
- •Tektronix DP-AUX can serves as a DP1.2 Sink Enables source to transmit the required patterns for testing.





# Automation: DisplayPort testing is a large task!

#### Combination Parameters For DP1.2 Testing

Combination of Tests

Data Rate - 3

1. Differential Tests

Lanes - 4

2. Single Ended Tests

Pre-Emphasis - 4 Levels

Voltage Swing - 4 Levels

Post Cursor2 - 4 Levels

SSC - 2 Levels(SSC On and Off)

Patterns - 5 Supported Patterns

Test	Waveforms (SSC, 4 Lanes Possible Combinations)
Eye Diagram Test	80
Pre-Emphasis Test	240
Non-Pre-Emphasis	32
Total Jitter	80

~432 Acquired signals for DP1.2 Normative Measurements per lane. X4 lanes results in <u>1728 Automated</u> Acquisitions per DUT.



## TekExpress DisplayPort 1.2 Automation

- Comprehensive Display Port Version 1.2 Physical Layer Conformance and Compliance Verification Tool
  - All Core DP1.2 measurements
  - Keithley RF Switch and DP-AUX fully automated solution.
  - Selected measurements can be applied across all test permutations (SSC,CTLE's, swing, rates, pre- emphasis, etc.) translates to 1728

    measurements.

    DP12 will provide full user intervention free, automated testing. This is the killer value proposition.

    Device Profile
  - Factory Automation API for full product control in silicon automation systems.
  - Complimentary Fixtures and Compliance Interconnect Channel HW defined by VESA make this package a full customer solution with no compromises.





V Level 0 V Level 2

Prompt me if signal chec....

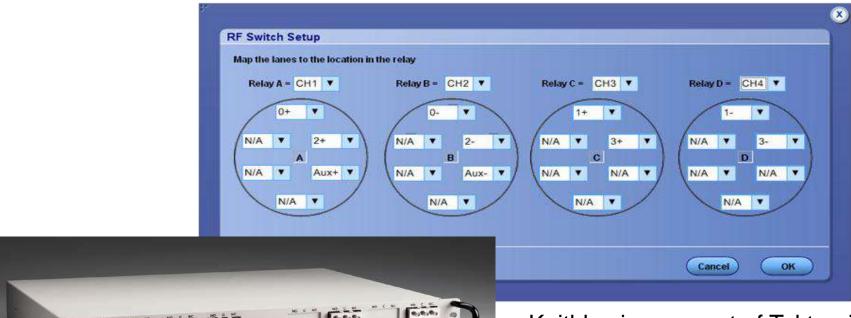
√ 1 (600m/V) 
√ 3 (1200m/V)

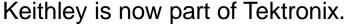
Link Width

11

# Keithley RF Switch Integration and Automation

DisplayPort transmitter has both Differential tests and Single ended tests and with the integration of RF switch we have complete automated solution without any user intervention for switching between lanes with both single ended and differential tests in sequential automated passes.



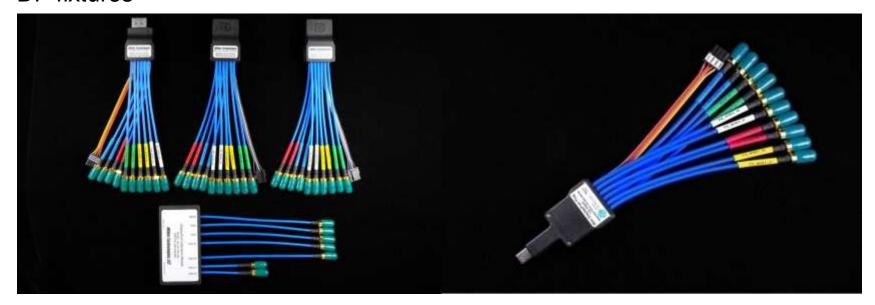






# Conventional Display Port Fixtures + CIC

Partnership with Wilder Technologies to design and channel high performance DP fixtures



Wilder TF-DP-TPA-PRC fixtures and BSA12500ISI available directly from Tektronix



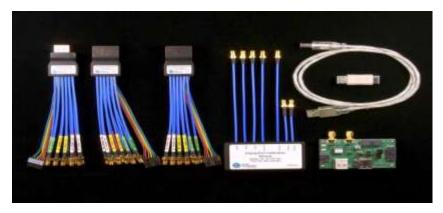




### DP++ fixtures



**TF-DPI-TPA-PA** 



**TF-DPI-TPA-PRRCA** 



TF-MDPI-TPA-PA



**TF-MDPI-TPA-PRRCA** 





# DisplayPort Receiver Testing







# DisplayPort 1.2 Sink (Rx) Test Overview

Receiver testing is performed with a Tektronix BSA125C BertScope and BERTScope ISI Board(or Wilder HBR2 ISI Channel).BER observation times range from 37 seconds to 10.5 minutes depending on the data rate and jitter frequency being tested.

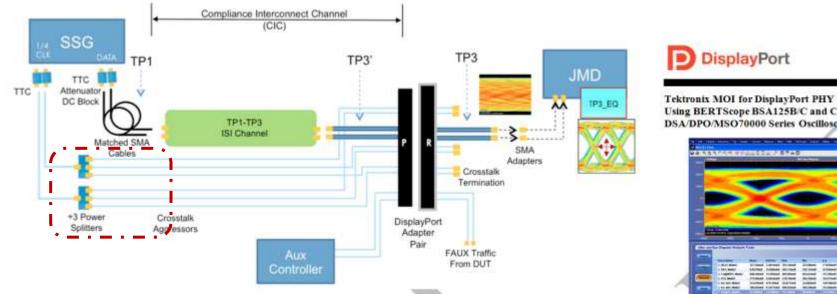
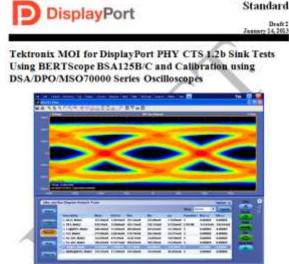


Figure 2: DP1.2b CTS HBR/HBR2 Conceptual Setup (Figure 4-3 in PHY 1.2b CTS)

f(SJ)	TJ(JTHBR2rx)	ISI	RJ(RMS)	Approximate SJ <sub>SWEEP</sub>	SJ <sub>FIXED</sub> @ 200MHz
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]	[mUI]
2	1026	220	16.7	505	100
10	636	220	16.7	116	100
20	624	220	16.7	104	100
100	620	220	16.7	100	100



DisplayPort<sup>TM</sup>



# DisplayPort 1.2Sink (Rx) Test Observation Time

Four Principal Test Frequencies at 2, 10, 20 and 100 MHz SJ

Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable	Observation Time <sup>1</sup> (seconds)	Data Rate Offset
HBR2				HBR2 =185s	
HBR	2 MHz	1012	1000	HBR=370s	0
RBR				RBR=620s	
HBR2				HBR2=19s	+350ppm
HBR	10 MHz	1011	100	HBR=37s	+350ppm
RBR				RBR=62s	+350ppm
HBR2				HBR2=19s	
HBR	20 MHz	1011	100	HBR=37s	0
RBR				RBR=62s	
HBR2	100 MHz	1011	100	HBR2=19s	0
HBR	100 M112	10	100	HBR=37s	U

To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR:  $10^{11}$  bits at HBR = 370ps/UI \* 10<sup>11</sup> UI = 37 seconds

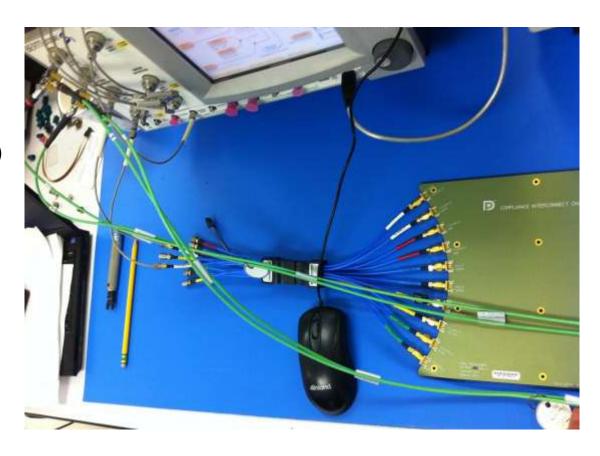




## BertScope Receiver Test Solution

#### **Typical Configuration**

- BertScope BSA85C
  - Option STR
- DPP125A (no 4T needed)
- BSA12500ISI
- DP-AUX
- TF-DP-CIC-C1
  - Wilder DP 1.2 ISI Board

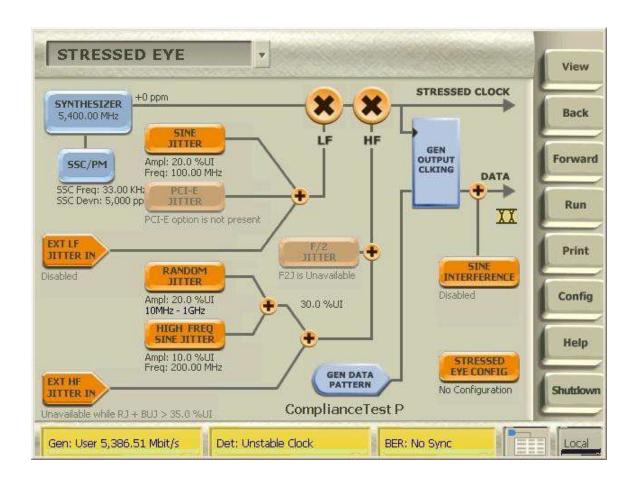






# Two Tone SJ, with Stationary HFSJ Parked at 200 MHz

New HFSJ source for fixed 200 MHz SJ as required by DP1.2.

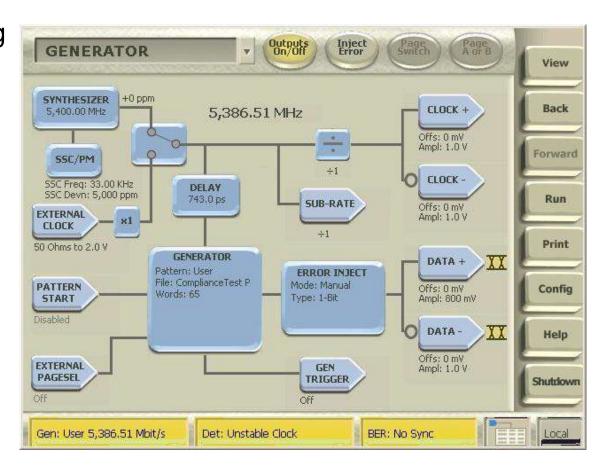






# DisplayPort 1.2 Crosstalk (BUJ) Configuration

Generator page showing Patterns and capability of generation large amount Crosstalk with differential sub-rate Clock Outputs.

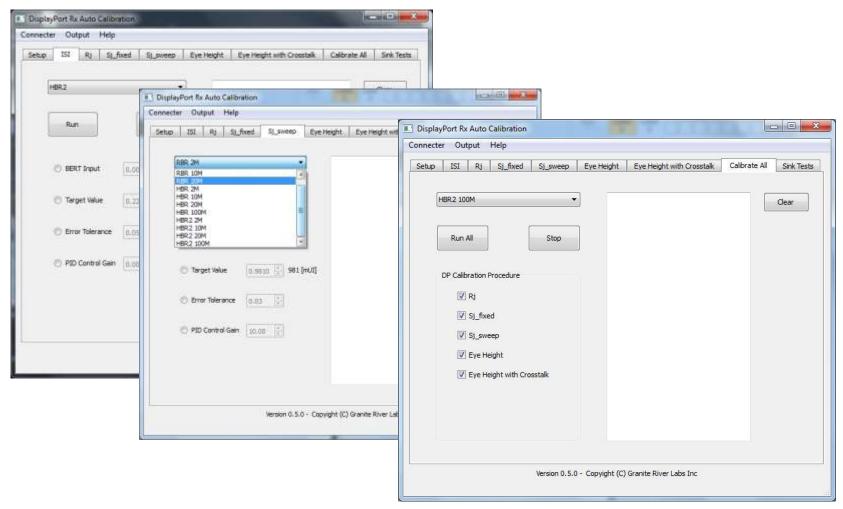






# DisplayPort 1.2b Sink automation SW

New TEK-GRL-DP-SINKSW







# eDP testing for eDP 1.4 specification



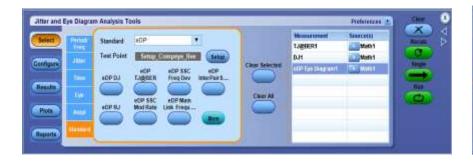


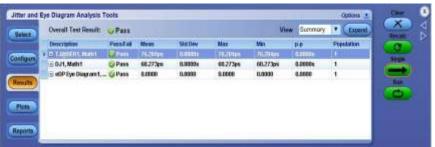


# **Embedded Display Port-eDP**

Option EDP is designed to provide component and system designers with a comprehensive verification and debug solution the latest Embedded DisplayPort Specification 1.4.

Using the familiar DPOJET look and feel the user can select the setup based on their specific measurements requirements. In addition, as the 1.4 specification allows the data rate to be anywhere within a range of speeds from RBR to HBR2 rates opt EDP will provide the dynamic mask generation required to ensure proper testing





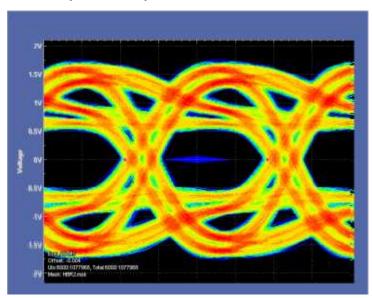


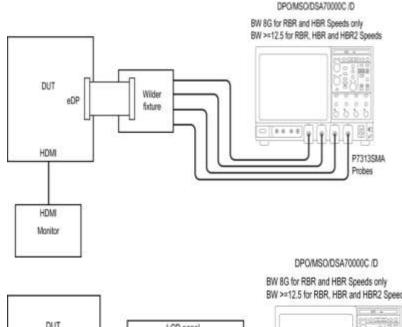


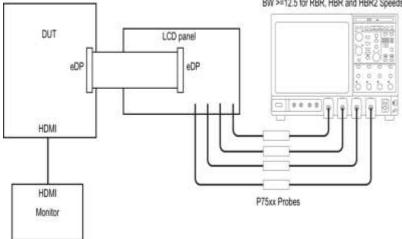
# Embedded Display Port-eDP Typical connection

#### eDP source measurements:

- Test 3.1 Eye Diagram Test
- Test 3.2 Inter Pair Skew test
- Test 3.3 Non-ISI Jitter Measurements
- Test 3.4 Total Jitter
- Test 3.5 Deterministic jitter
- Test 3.6 Random Jitter
- Test 3.7 Main Link Frequency Stability
- Test 3.8 Spread Spectrum Modulation Frequency
- Test 3.9 Spread Spectrum Modulation Deviation











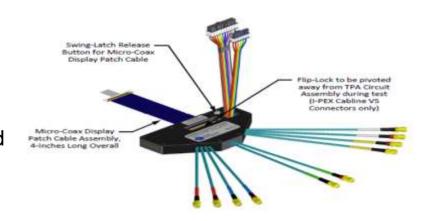
## **Embedded Display Port-eDP**

#### **Oscilloscope Requirements**

- Option EDP requires a DPO/DSA/MSO 70K scope running firmware version
- •6.4.0 or higher and DPOJet version 6.0 or higher.
- •For customers testing RBR (1.62 Gb/sec) and HBR (2.7 Gb/sec) a minimum bandwidth of 8Ghz is required.
- •For customers testing HBR2 (5.4 Gb/sec) a minimum 12.5GHz BW is required.

#### **Probing**

- ■For customers testing RBR (1.62 Gb/sec) or HBR (2.7 Gb/sec) Qty 4 P7380 or P7380SMA are required if testing more then two lanes at one time.
- •For customers testing HBR2 (5.4 Gb/sec) and HBR (2.7 Gb/sec) and RBR
- •(1.62 Gb/sec) Qty 4 P7313 or P7313MA are required if testing more then two lanes at one time.
- •An optional eDP fixture is available on the Tektronix PAI :TF-FDP-TPA-PRC







# Complete Tektronix DisplayPort Instrument Portfolio

Receiver/Sink Tests (Characterization) Receiver Silicon characterization and compliance testing capability to 26Gbps	<b>BSA125C</b> with JMAP and SSC and HW Options DPP 125A and CR125A provide support for future bit-rates (12-26G) with a unique portfolio of Scope and Bert combined features.	THE RESERVE OF THE PARTY OF THE
DP Channel Tests Source and Sink electrical channel performance, Crosstalk, Impedance and return loss. High Dynamic Range instrument	DSA8300 80E10 TDR Sampling Module for DSA8200 Sampling Scope S-Parameter Analysis Software 80SICON Software	
Cable Tests Cable crosstalk, skew and frequency domain measurements, sdd21, sdd11.	DSA8300 4X 80E08 TDR Sampling Module for DSA8300 Sampling Scope	
Transmitter/Source Tests Signal timing stability and SSC analysis, Transmitter AC parametric, Jitter, Amplitude.	DSA71254C DPOJET Jitter Analysis software SMA Adapters TCA-SMA 2 per scope Differential SMA Probe P7313SMA (optional) + DP-AUX controller + DP12 (Sw Option)+Option eDP	





# Tektronix Displayport Solution Equipment Configuration

- 1# DPO/DSA/MSO70000 C/D/DX series Real time Oscilloscope with BW >/= 12.5GHz
- Option DPTX12 SW or Opt eDP essentials or TEK-GRL-DP-SINKSW
- 4# P7313SMA probes OR Direct SMA or Using RF Switch
- Display port Fixtures Based on specific customer needs for normal/mini/DP++/eDP
- BertScope BSA85C with Opt STR
- DPP125A (no 4T needed)
- BSA12500ISI
- DP-AUX





# Tektronix®



