Tektronix Innovation Forum

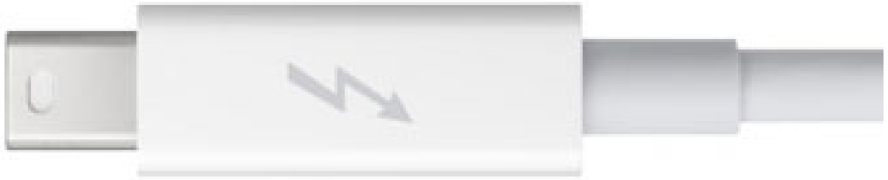
Enabling Innovation in the Digital Age

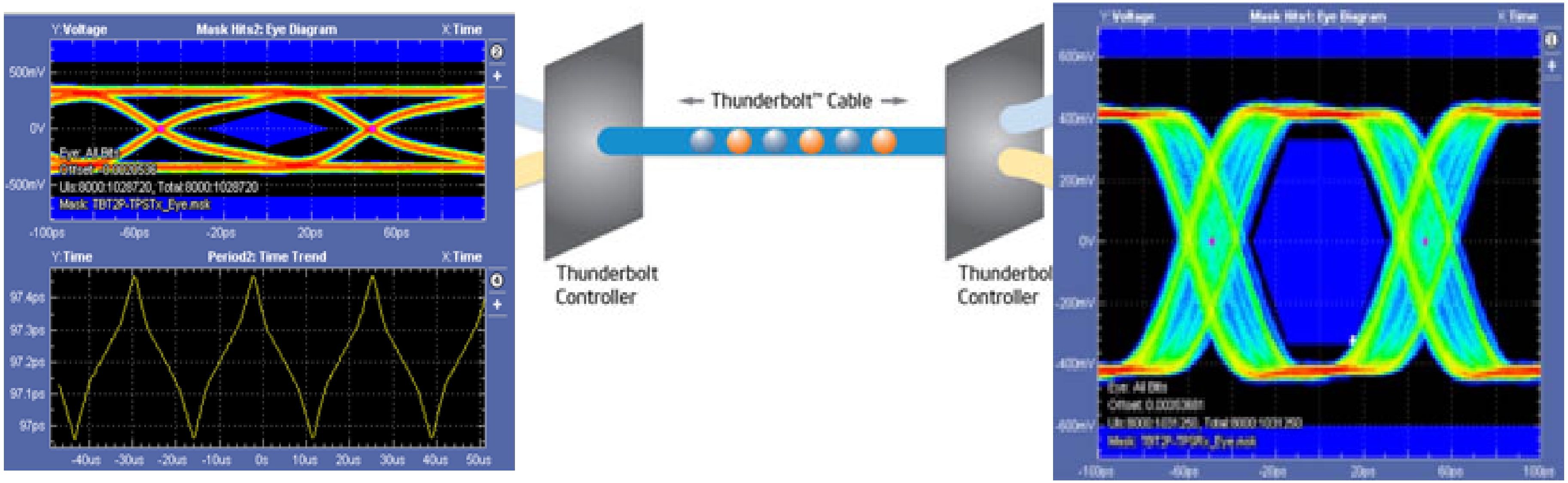
Thunderbolt Physical Layer testing and technology overview

Presenter: John Calvin

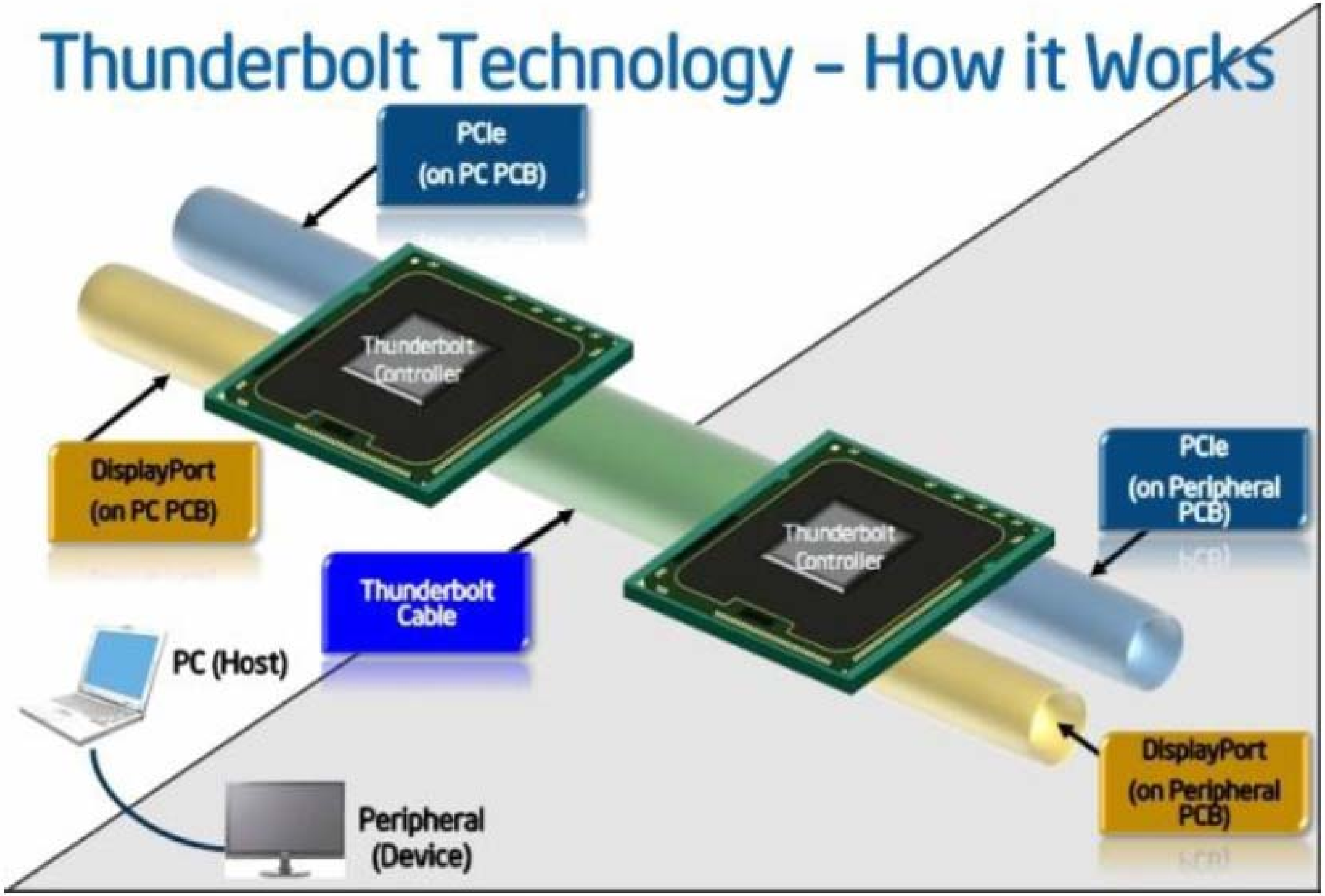
Tektronix®

THUNDERBOLT™



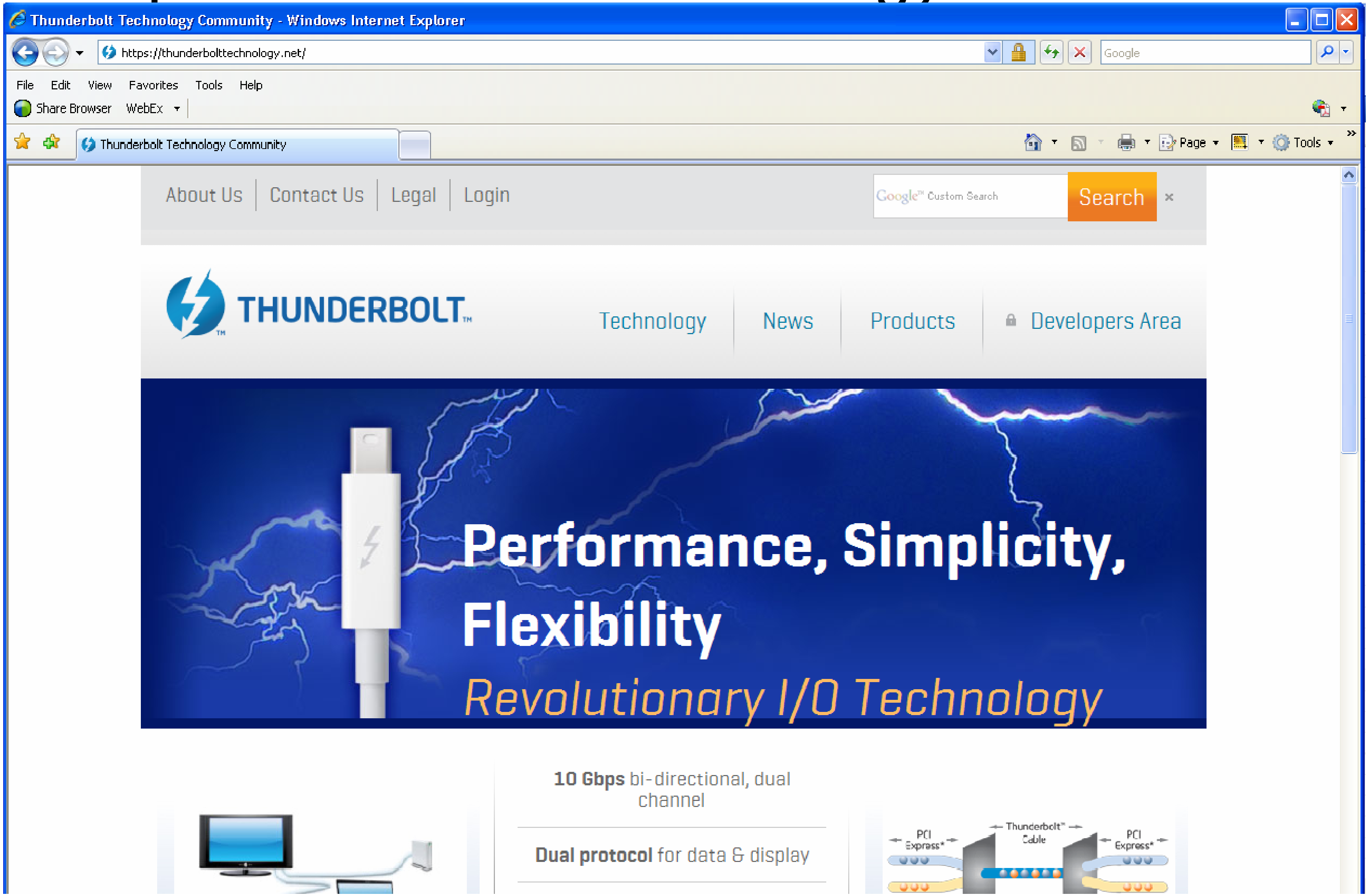


Thunderbolt Overview



Thunderbolt technology have new chip system and wiring, which allow transfer of video display and information at 10Gigabit per second (Gbps) in both directions, all in one cable, Thunderbolt control component does not require an Intel processor, but runs on its own as a router switches between channels, the Thunderbolt channels to the PCI Express.

Thunderbolt Developers Network https://thunderbolttechnology.net/



https://thunderbolttechnology.net/

10 Gbps bi-directional, dual channel

Dual protocol for data & display

Thunderbolt Overview

- Thunderbolt signaling is a dual NRZ (64/66b Encoded) 10.3125Gb/sec (Same as SFP+) differential Tx pairs and two differential Rx pairs.
- Instrument BW has been recommended at 16GHz by Intel. The connectors do not pass significant energy beyond 16GHz, and the noise content beyond 16G is regarded as a significant measurement liability.
- Tektronix recommends Instrument bandwidth to 20GHz to properly align De-Embed filters stop band performance into the 4'th signaling harmonic's null.
- Tektronix and GRL have partnered on test development and efforts towards enabling the Thunderbolt ecosystem with an test MOI which illustrates sanctioned methods of test for Transmitter, Receiver and Channel characterization.
- Intel Thunderbolt Overview with Intel's Jason Ziller: http://www.youtube.com/watch?v=gk69pCcVSSQ

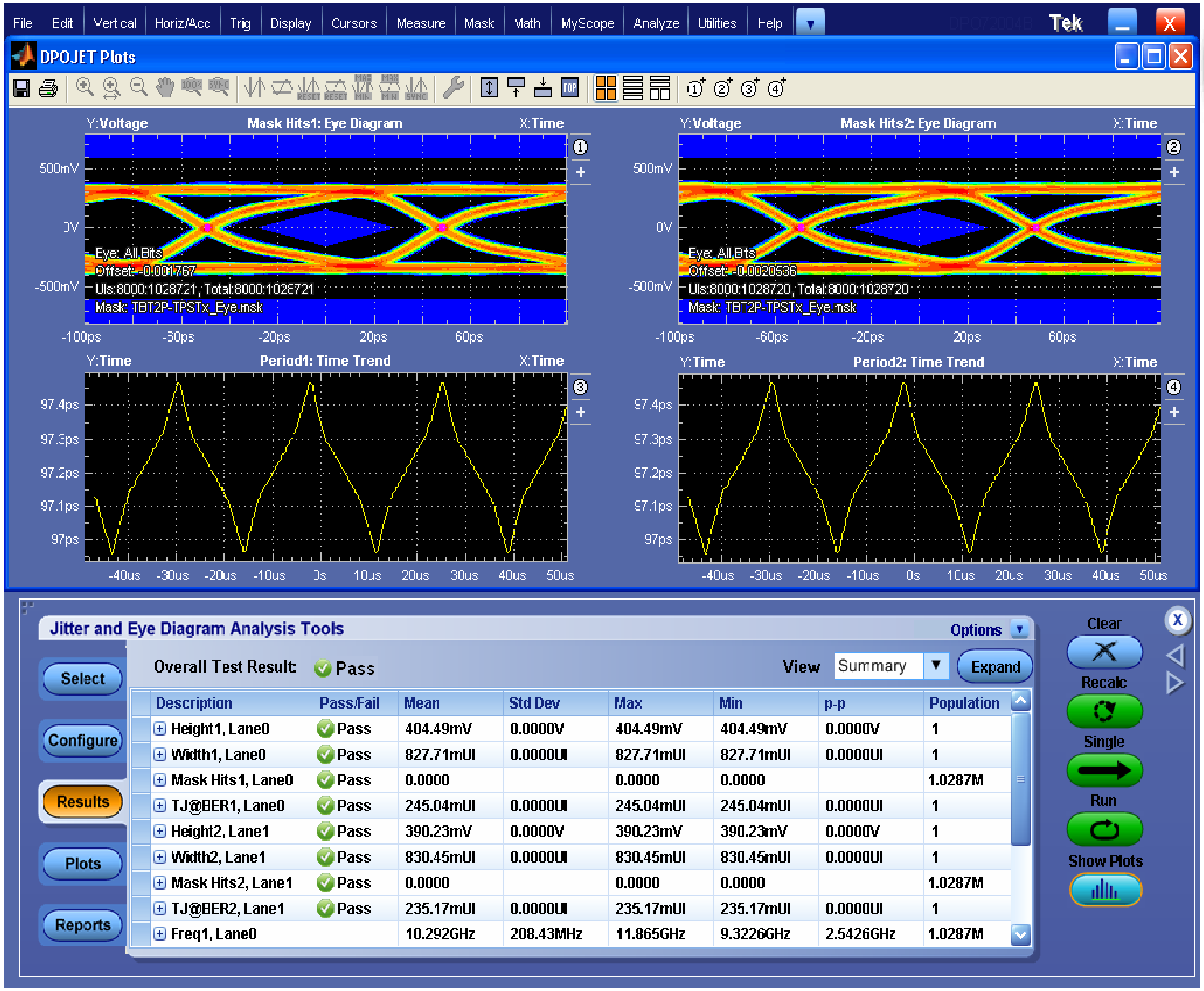
Thunderbolt Transmitter Test Overview

- Thunderbolt from a physical layer validation has a very straight forward test configuration. All measurements are near end with Fixtures fully de-embedd. Thunderbolt conformance requires Displayport 1.2 conformance which is where things become more complex.

- Source Test Suite
  - PHY1.1 – Transition Timing
  - PHY1.2 – Intra-Pair Skew
  - PHY1.3 – AC Common Mode RMS
  - PHY1.4 – AC Common Mode Peak
  - PHY1.5 – Eye Height
  - PHY1.6 – Eye Width
  - PHY1.7 – Max Differential Voltage
  - PHY1.8 – Total Jitter at 10-13 BER
  - PHY1.9 – Unit Interval
  - PHY1.10 – SSC Modulation Frequency

- DUT Configuration
  - 1. Bit Rates: (DP1.2) + 10.3125Gb/sec
  - 2. Patterns: 81’s80’s, PRBS-9, PRBS-31
  - 3. SSC (Spread Spectrum): On/Off

Thunderbolt Transmitter Testing
Fully supported in Tektronix's current solutions



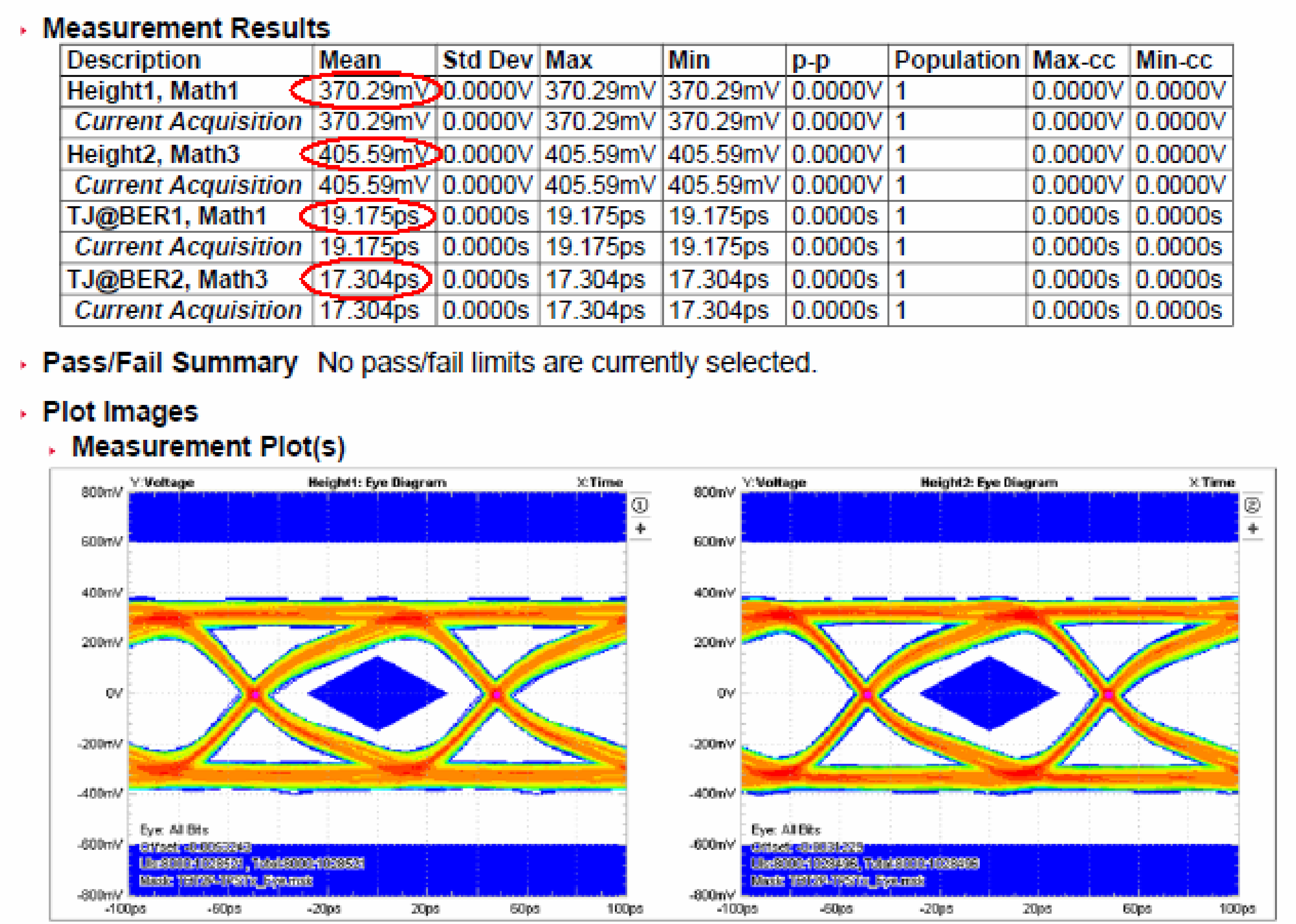
Overall Test Result: Pass

View: Summary

Description	Pass/Fail	Mean	Std Dev	Max	Min	p-p	Population
Height1, Lane0	Pass	404.49mV	0.0000V	404.49mV	404.49mV	0.0000V	1
Width1, Lane0	Pass	827.71mUI	0.0000UI	827.71mUI	827.71mUI	0.0000UI	1
Mask Hits1, Lane0	Pass	0.0000		0.0000	0.0000		1.0287M
TJ@BER1, Lane0	Pass	245.04mUI	0.0000UI	245.04mUI	245.04mUI	0.0000UI	1
Height2, Lane1	Pass	390.23mV	0.0000V	390.23mV	390.23mV	0.0000V	1
Width2, Lane1	Pass	830.45mUI	0.0000UI	830.45mUI	830.45mUI	0.0000UI	1
Mask Hits2, Lane1	Pass	0.0000		0.0000	0.0000		1.0287M
TJ@BER2, Lane1	Pass	235.17mUI	0.0000UI	235.17mUI	235.17mUI	0.0000UI	1
Freq1, Lane0		10.292GHz	208.43MHz	11.865GHz	9.3226GHz	2.5426GHz	1.0287M

Thunderbolt

De-Embedded test results
Thunderbolt Fixture De-Embed results



- **Measurement Results**

Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Height1, Math1	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Height2, Math3	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
TJ@BER1, Math1	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
TJ@BER2, Math3	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s

- **Pass/Fail Summary** No pass/fail limits are currently selected.
- **Plot Images**
  - **Measurement Plot(s)**

Thunderbolt Jitter Analysis
BUJ

- Interconnect and board layout technology is advancing and the greatest area of focus is in reducing the insertion loss and Signal-to-Crosstalk ratio. Packaging parasitics cannot be ignored here either and important from both a modeling and measurement needs.
- The implications of complex channel interaction as well as SERDES multiplexing method, can be observed and identified in an output signal by examining the type and amount of Bounded Uncorrelated Jitter or BUJ.
- There is a strong Cause–and-Effect relationship between Crosstalk (NEXT) and BUJ which in most systems get's classified as Random if special steps are not observed.

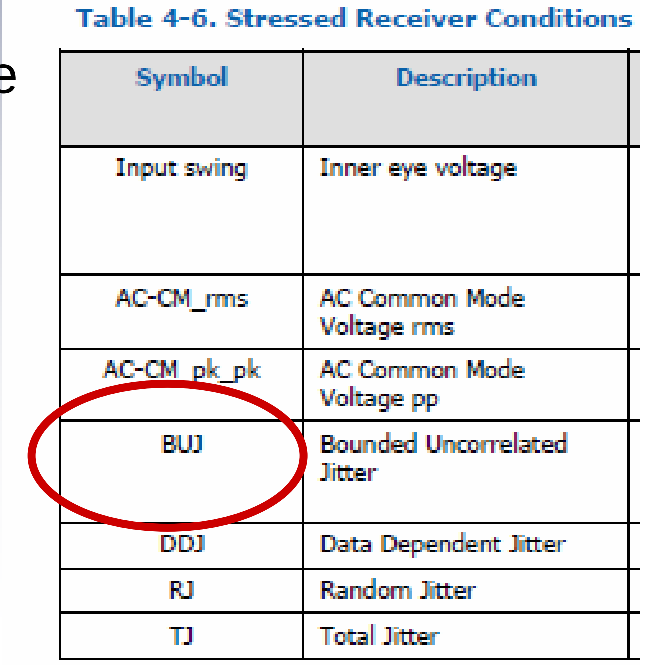


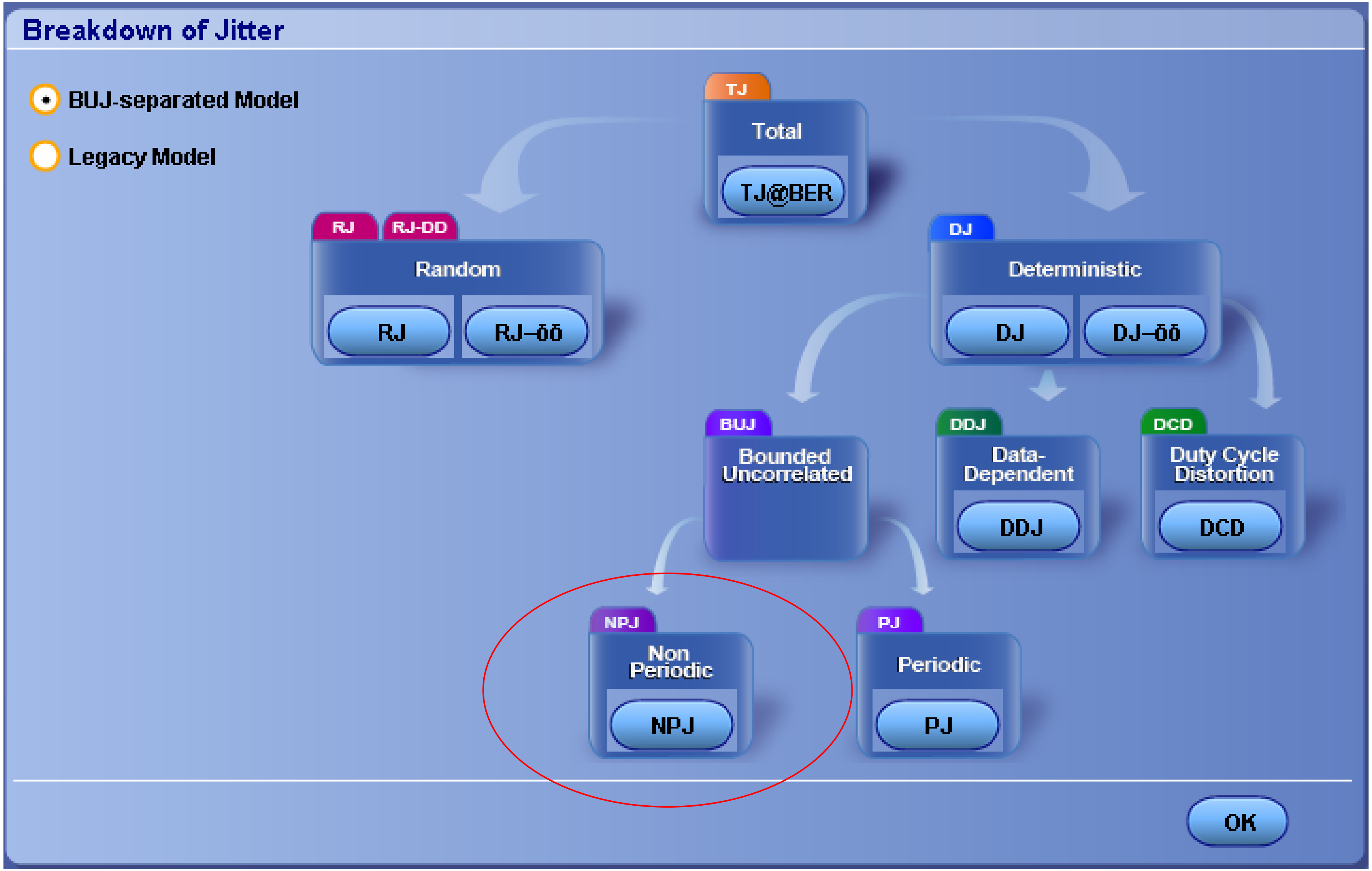
Table 4-6. Stressed Receiver Conditions

Symbol	Description
Input swing	Inner eye voltage
AC-CM_rms	AC Common Mode Voltage rms
AC-CM_pk_pk	AC Common Mode Voltage pp
BUJ	Bounded Uncorrelated Jitter
DDJ	Data Dependent Jitter
RJ	Random Jitter
TJ	Total Jitter

Tektronix

Jitter Analysis Advances

BUJ is now core to DPOJET real time jitter analysis

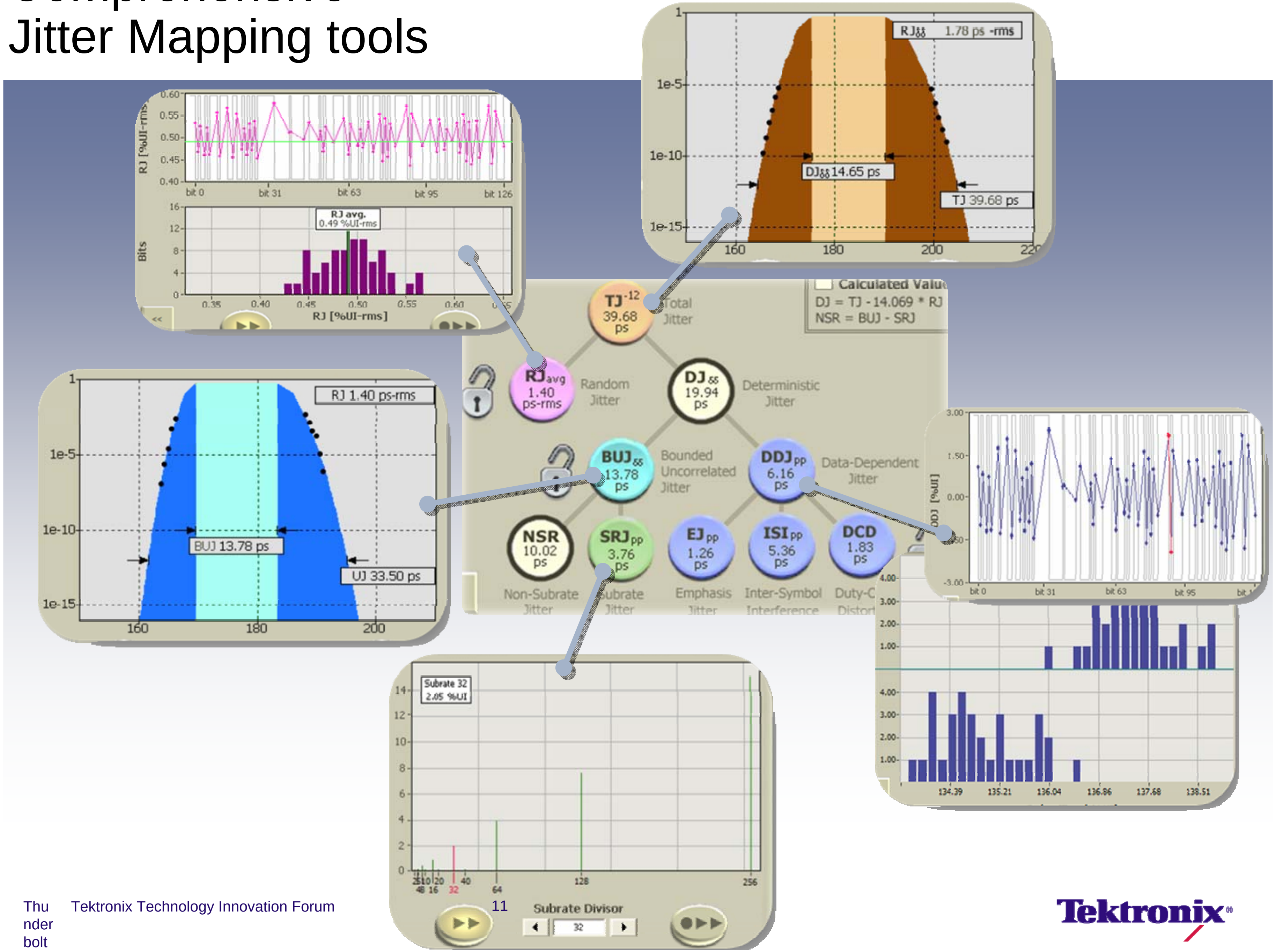


Breakdown of Jitter

● BUJ-separated Model

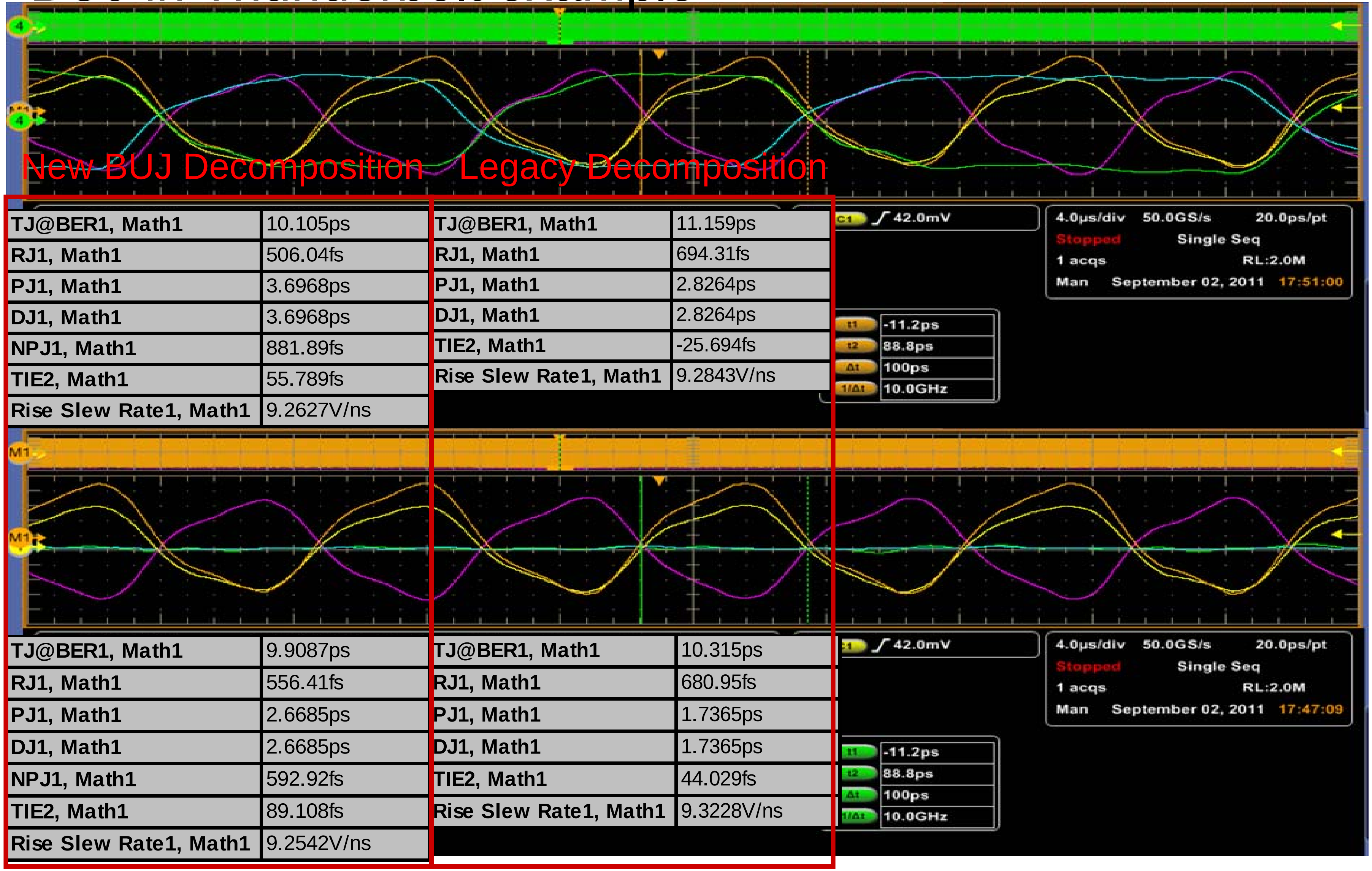
○ Legacy Model

Comprehensive Jitter Mapping tools



Jitter Analysis Advances

BUJ in Thunderbolt example



New BUJ Decomposition

TJ@BER1, Math1	10.105ps
RJ1, Math1	506.04fs
PJ1, Math1	3.6968ps
DJ1, Math1	3.6968ps
NPJ1, Math1	881.89fs
TIE2, Math1	55.789fs
Rise Slew Rate1, Math1	9.2627V/ns

Legacy Decomposition

TJ@BER1, Math1	11.159ps
RJ1, Math1	694.31fs
PJ1, Math1	2.8264ps
DJ1, Math1	2.8264ps
TIE2, Math1	-25.694fs
Rise Slew Rate1, Math1	9.2843V/ns

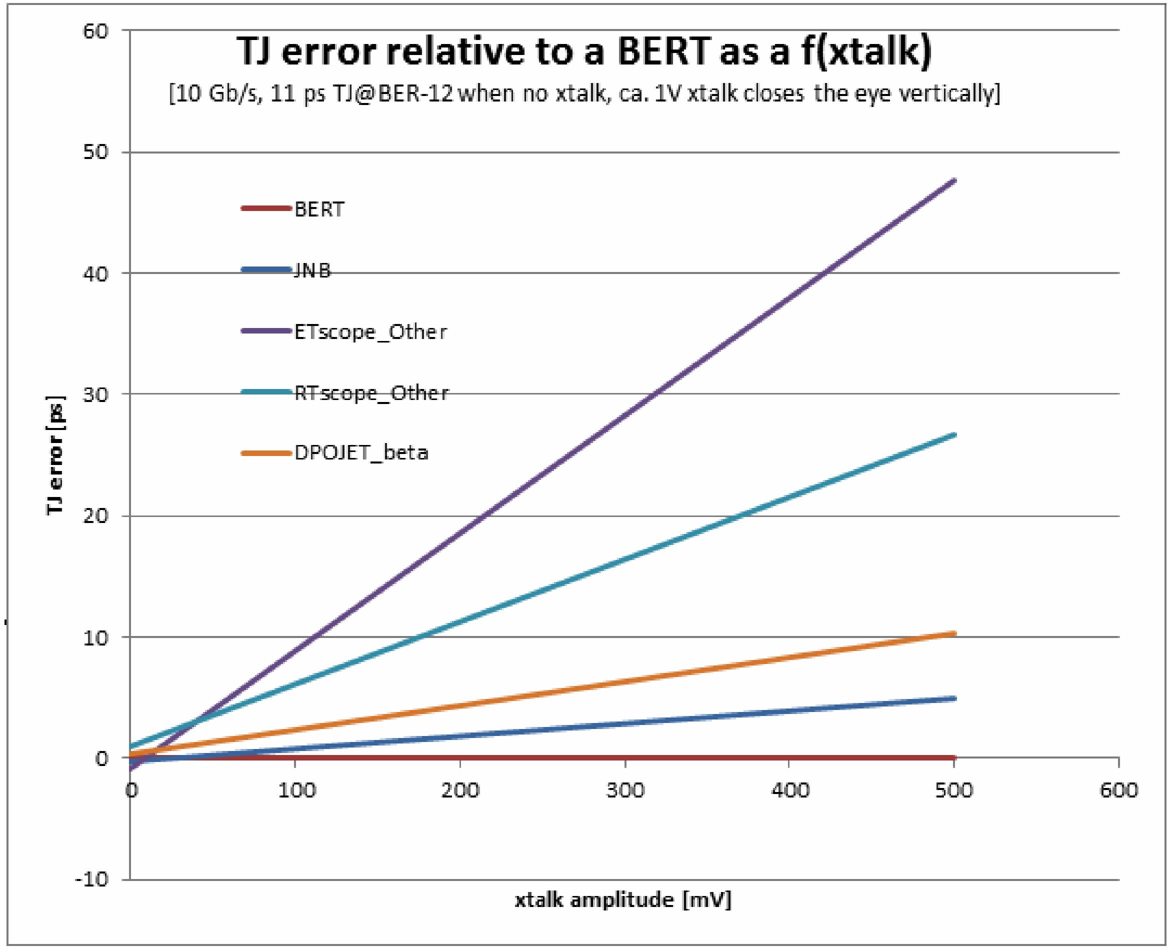
TJ@BER1, Math1	9.9087ps
RJ1, Math1	556.41fs
PJ1, Math1	2.6685ps
DJ1, Math1	2.6685ps
NPJ1, Math1	592.92fs
TIE2, Math1	89.108fs
Rise Slew Rate1, Math1	9.2542V/ns

TJ@BER1, Math1	10.315ps
RJ1, Math1	680.95fs
PJ1, Math1	1.7365ps
DJ1, Math1	1.7365ps
TIE2, Math1	44.029fs
Rise Slew Rate1, Math1	9.3228V/ns

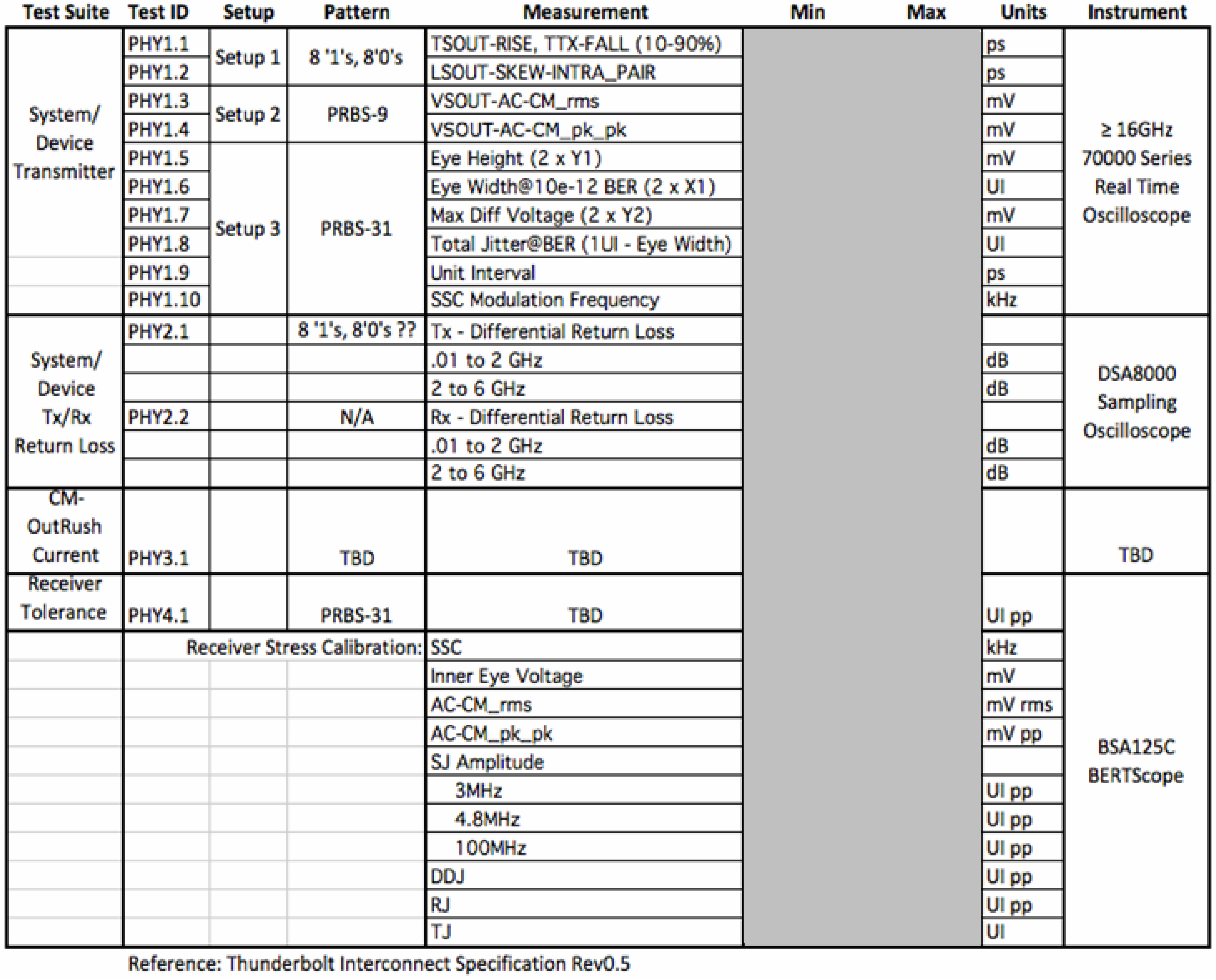
Jitter Analysis Advances

Results of the BUJ-aware jitter analysis algorithm

- Setup: DUT: victim pattern: 0011, aggressor pattern PRBS7, amplitude of both aggressor and victim 500 mV
  Oscilloscopes:
  RL of 2MS (RTOs),
  BW>=18GHz
  BERT RX: 12 hrs
  All plots are linear interp. from several points
- Both ET and RT Tek scopes run the new, BUJ-able analysis
- Note: longer RL improves, longer aggres. worsens, the results given here.



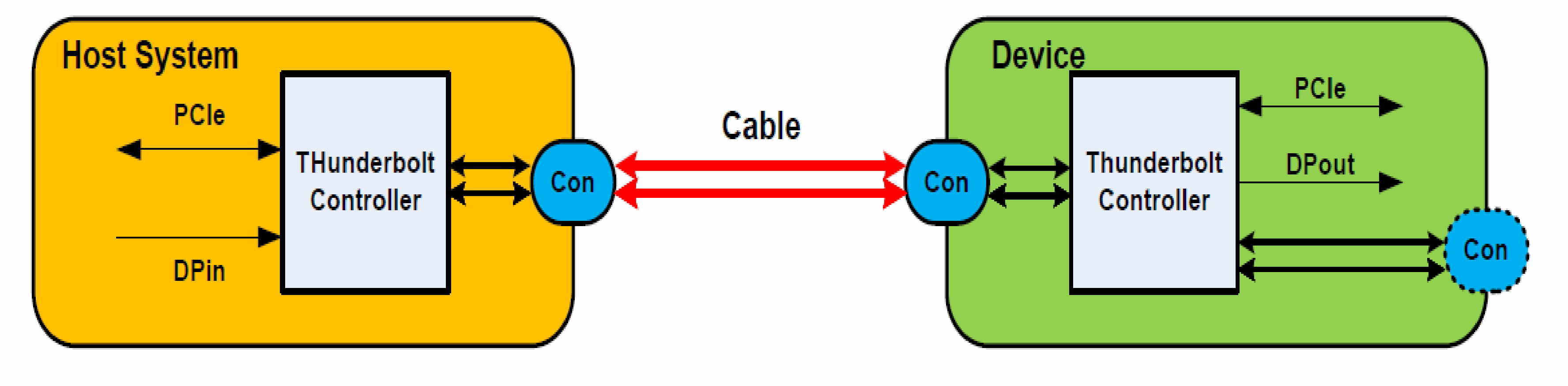
Current (.5 TBT Spec Version) Measurement Summary



Test Suite	Test ID	Setup	Pattern	Measurement	Min	Max	Units	Instrument
System/ Device Transmitter	PHY1.1	Setup 1	8 '1's, 8'0's	TSOUT-RISE, TTX-FALL (10-90%)			ps	≥ 16GHz 70000 Series Real Time Oscilloscope
	PHY1.2			LSOUT-SKEW-INTRA_PAIR			ps	
	PHY1.3	Setup 2	PRBS-9	VSOUT-AC-CM_rms			mV	
	PHY1.4			VSOUT-AC-CM_pk_pk			mV	
	PHY1.5	Setup 3	PRBS-31	Eye Height (2 x Y1)			mV	
	PHY1.6			Eye Width@10e-12 BER (2 x X1)			UI	
	PHY1.7			Max Diff Voltage (2 x Y2)			mV	
	PHY1.8			Total Jitter@BER (1UI - Eye Width)			UI	
	PHY1.9			Unit Interval			ps	
	PHY1.10			SSC Modulation Frequency			kHz	
System/ Device Tx/Rx Return Loss	PHY2.1		8 '1's, 8'0's ??	Tx - Differential Return Loss				DSA8000 Sampling Oscilloscope
				.01 to 2 GHz			dB	
				2 to 6 GHz			dB	
	PHY2.2		N/A	Rx - Differential Return Loss				
				.01 to 2 GHz			dB	
				2 to 6 GHz			dB	
CM-OutRush Current	PHY3.1		TBD	TBD				TBD
Receiver Tolerance	PHY4.1		PRBS-31	TBD			UI pp	BSA125C BERTScope
			Receiver Stress Calibration:	SSC			kHz	
				Inner Eye Voltage			mV	
				AC-CM_rms			mV rms	
				AC-CM_pk_pk			mV pp	
				SJ Amplitude				
				3MHz			UI pp	
				4.8MHz			UI pp	
				100MHz			UI pp	
				DDJ			UI pp	
				RJ			UI pp	
				TJ			UI	

Reference: Thunderbolt Interconnect Specification Rev0.5

Thunderbolt Transmitter Testing

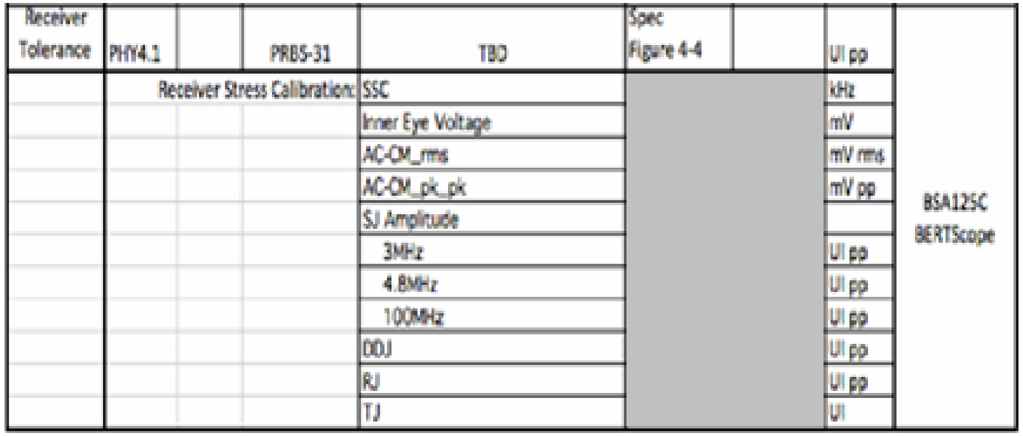


- One of the key benefits of the Thunderbolt design is an architecture which alleviates needs to perform "Far End" signal integrity analysis as found in other standards such as USB3, SAS, or PCIE.
- The absence of link negotiation and having to deal with the uncertainty of an unknown cable (Channel) and a unknown receiver (Disk Drive for instance) greatly simplifies and improves the link integrity.
    - The Tx system has to manage a fairly simple contract to deliver bits to the connector point with a 1E-12 BER certainty.
    - The Active Cable (which does it's own smart link negotiation on power up) has an independent contract to deliver bits from one end to the other with a 1E-12 BER certainty.
    - The Rx system has to manage the receipt of the signals to a certainty 1E-12 BER.
- The three independent contracts are designed to work together as a system, but complex system level link negotiation is not required.

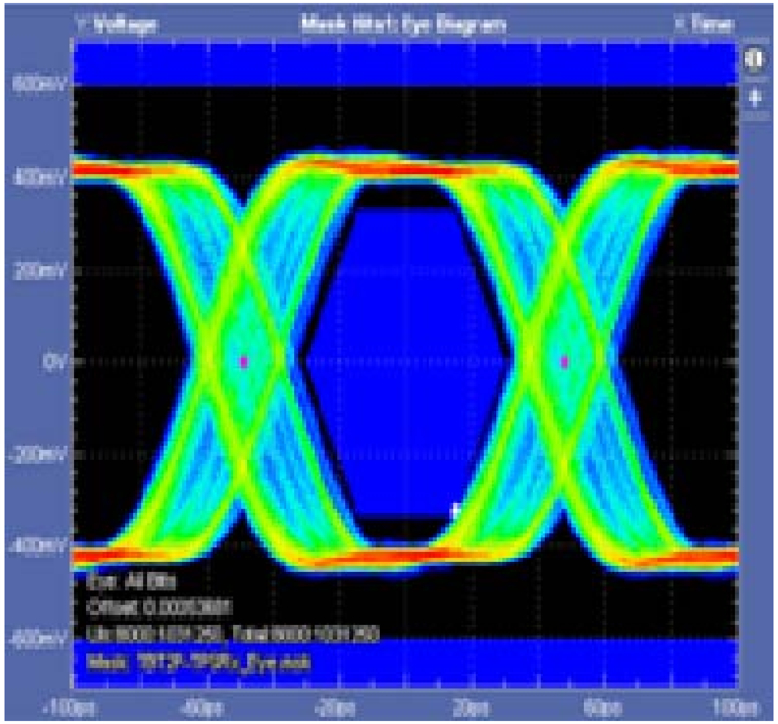
Thunderbolt Receiver: Stressed Pattern Calibration

- The Receiver test pattern used in Thunderbolt is a PRBS-31, however the calibration is performed on a PRBS-11 pattern.

Freq	*BERScopeSj*	*DPOJET Measured Pj*
3MHz	*26%*	*310mUI*
4.8MHz	*7%*	*123mUI*
100MHz	*8%*	*128mUI*

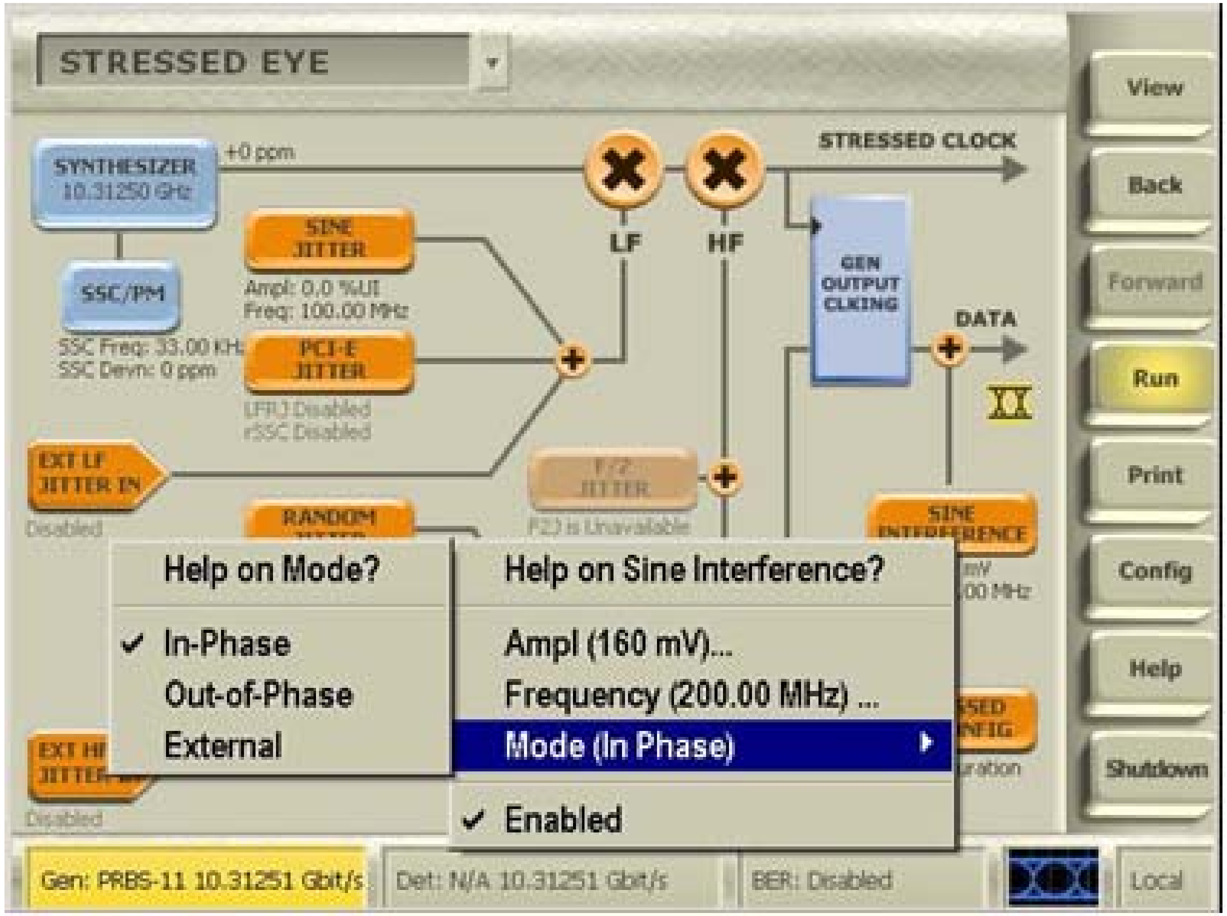


Receiver Tolerance	PHY4.1		PRBS-31	TBD	Spec Figure 4-4		UI pp	
	Receiver Stress Calibration:			SSC			kHz	BSA125C BERTScope
				Inner Eye Voltage			mV	
				AC-CM_rms			mV rms	
				AC-CM_pk_pk			mV pp	
				SJ Amplitude				
				3MHz			UI pp	
				4.8MHz			UI pp	
				100MHz			UI pp	
				DDJ			UI pp	
				RJ			UI pp	
				TJ			UI	



Thunderbolt Receiver: AC Common Calibration

- 200MHz AC Common Mode noise is part of the Thunderbolt impairment profile.



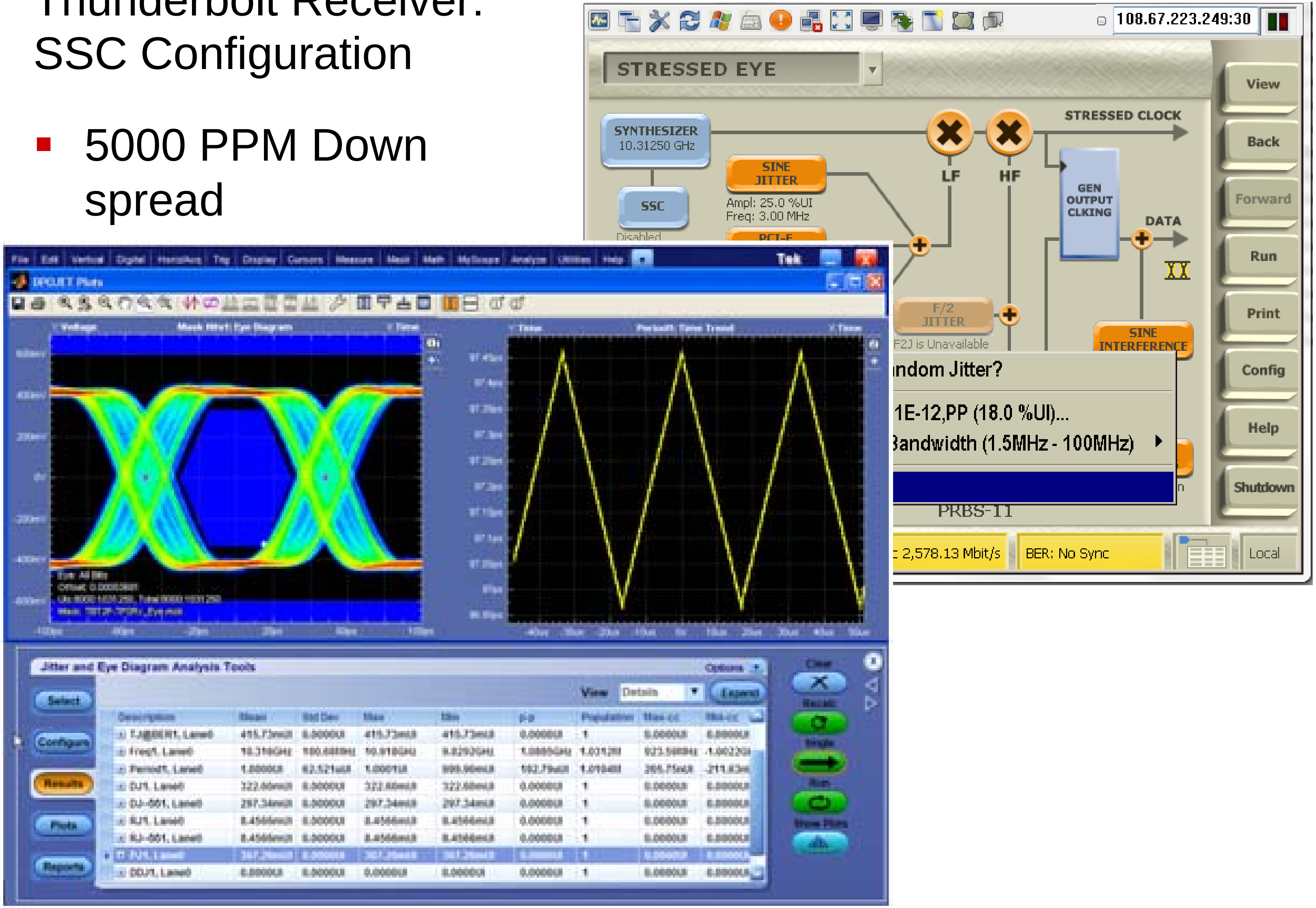
Gen: PRBS-11 10.31251 Gbit/s

Det: N/A 10.31251 Gbit/s

BER: Disabled

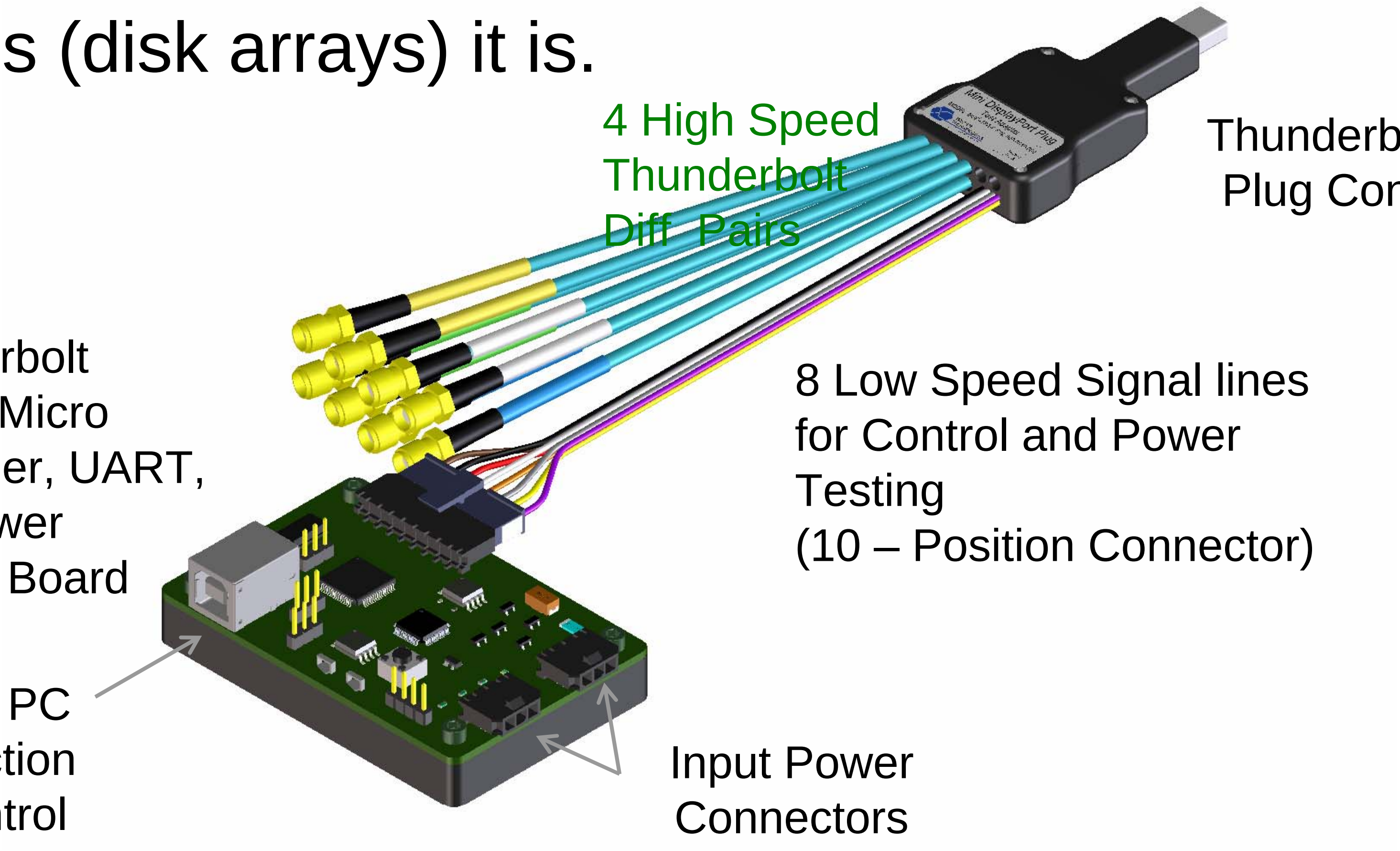
Thunderbolt Receiver: SSC Configuration

- 5000 PPM Down spread



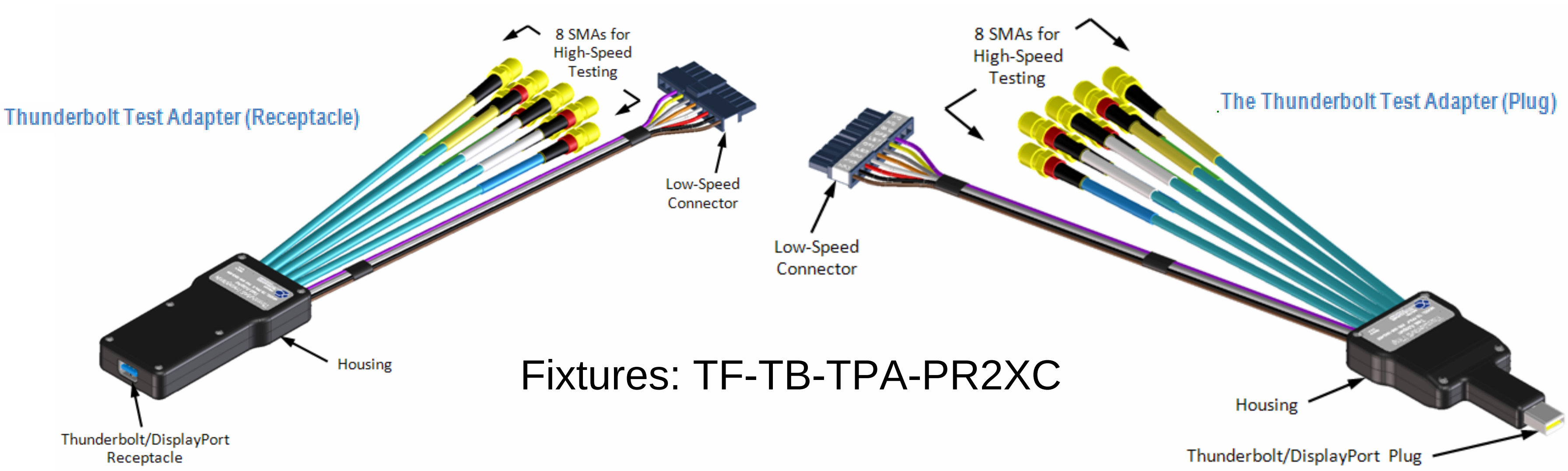
Thunderbolt Digital Port Micro Controller

- The Digital Port Micro is responsible for Test Pattern and general state control, as well as error polling in the DUT. For hosts this is not essential but for devices (disk arrays) it is.



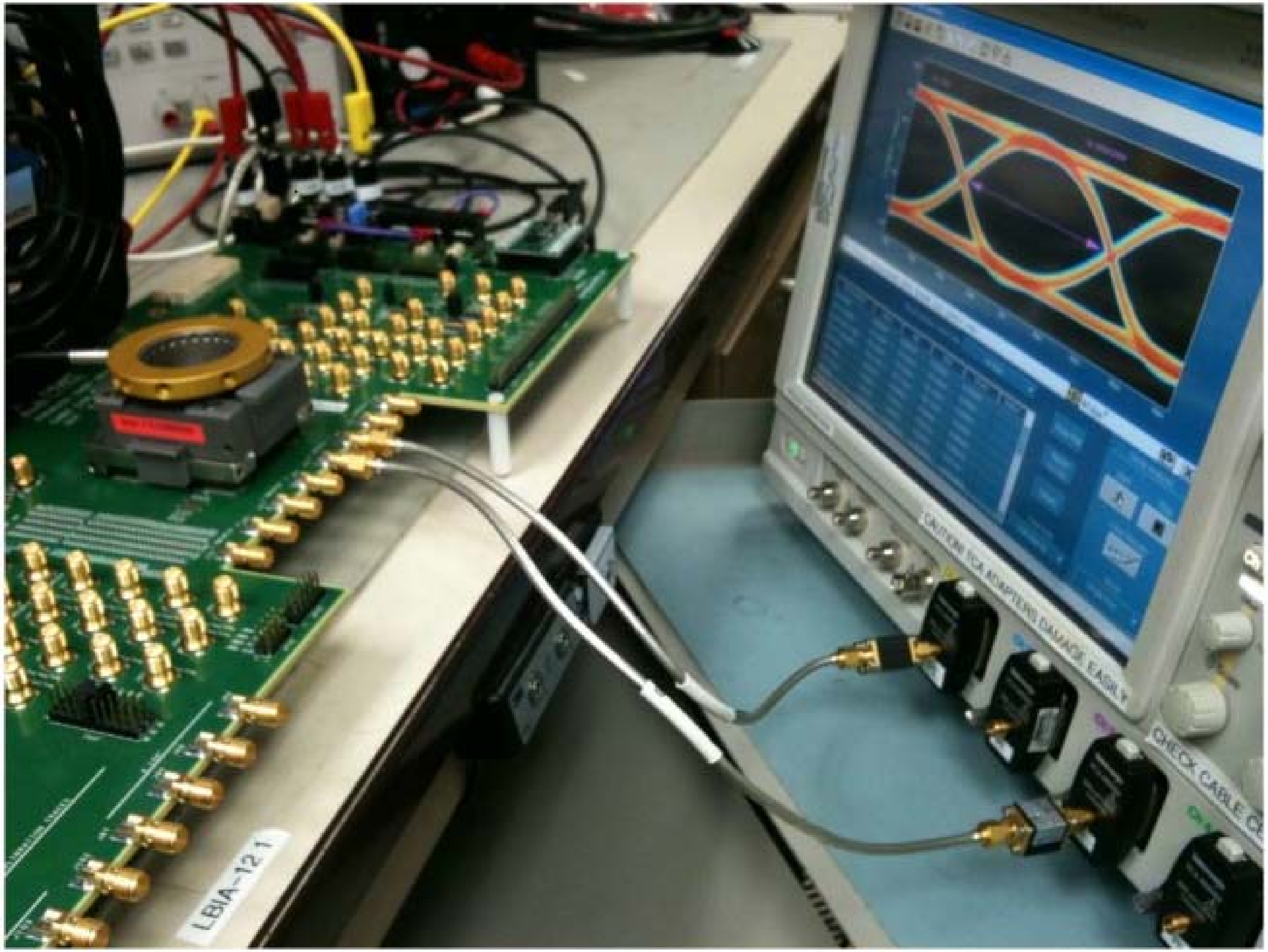
Instrument Considerations

- Phase 0 (Thunderbolt Silicon/System Designers):
  - 30+G Real Time Oscilloscope to Tx Characterization and Rx Calibration
  - BertScope: 12G stimulus and error detector for Receiver Testing/Cable Testing.
- Phase 1-2 (ODM/OEM):
  - 20 GHz Real Time Instrumentation (**De-Embed Stop Band set to 4'th harmonic**)
  - 12.5G BertScope for receiver testing.



Fixtures: TF-TB-TPA-PR2XC

Phase 0 (Silicon Designer) Configuration

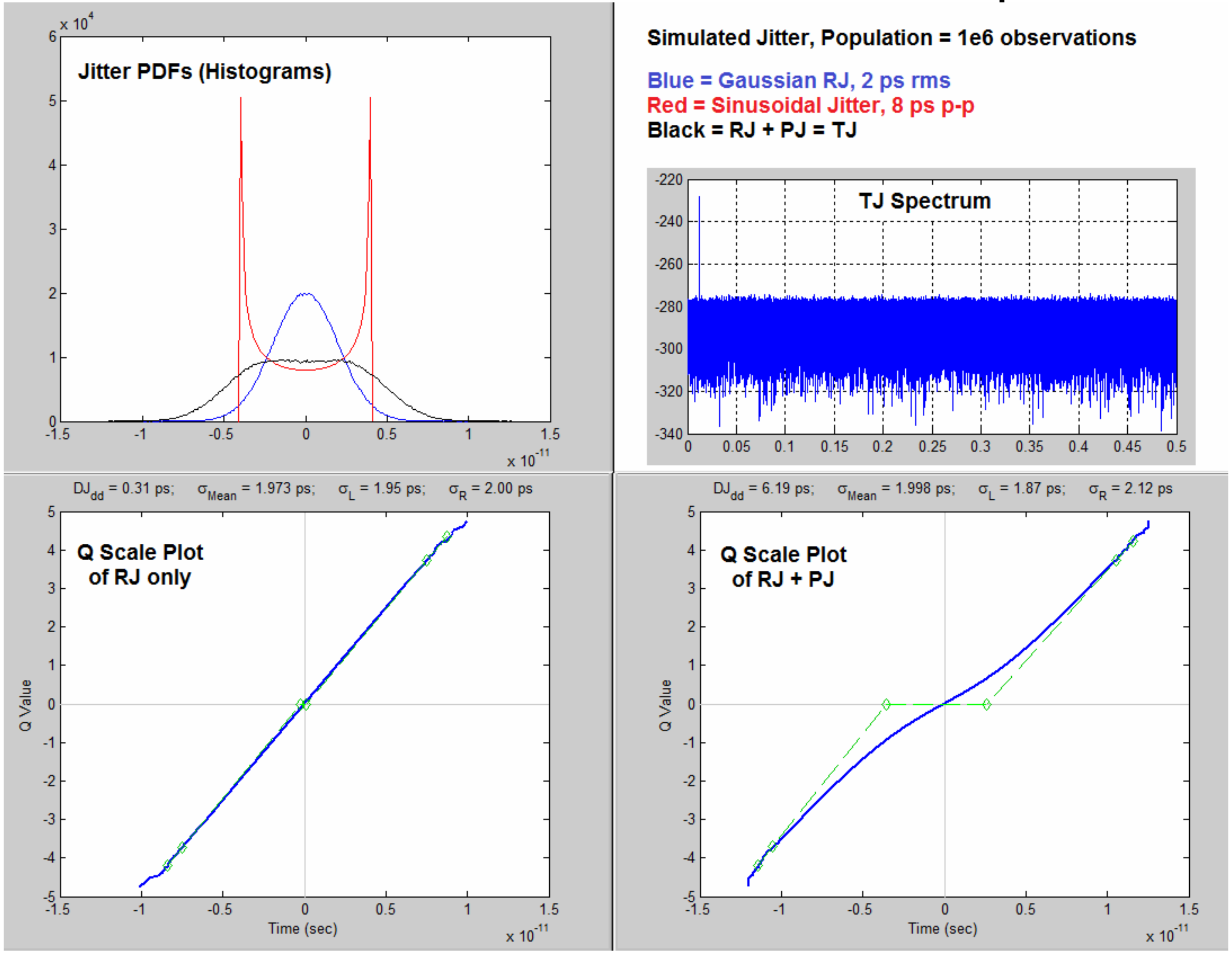


Complete Thunderbolt Instrument Portfolio

Receiver Tests/Active Cable Tests Receiver silicon and system margin testing. Tj, Rj, DDJ, BUJ, AC-CM	**BSA125C** with **JMAP** and SSC and **HW Options DPPS125** and **CR125A** provide support for future bit-rates (12-26G) with a unique portfolio of Scope and Bert combined features. Fixtures:TF-TB-TPA-PR2XC	
Channel Tests Return Loss (HF,LF) . (SDD11,SDD22) Common Mode Return Loss (SCC22) Mode Conversion (SCC12) Channel Insertion Loss (SDD21) Near End Crosstalk (NEXT)	**DSA8300** 80E10 TDR Sampling Module for DSA8300 Sampling Scope S-Parameter Analysis Software 80SICON Software for DSA8300 Fixtures: TF-TB-TPA-PR2XC	
TransmitterTests AC Parametric measurements Jitter Eye Opening AC Common Mode Data Dependant Pulse Width Shrinkage	**DSA72004D** DPOJET Jitter Analysis software TCA-292D Coax Adapters 4 per scope ThunderBolt MOI Fixtures: TF-TB-TPA-PR2XC	

Backup Material on BUJ

Jitter Analysis Advances
Tek Patented Random and Deterministic separation



Simulated Jitter, Population = 1e6 observations

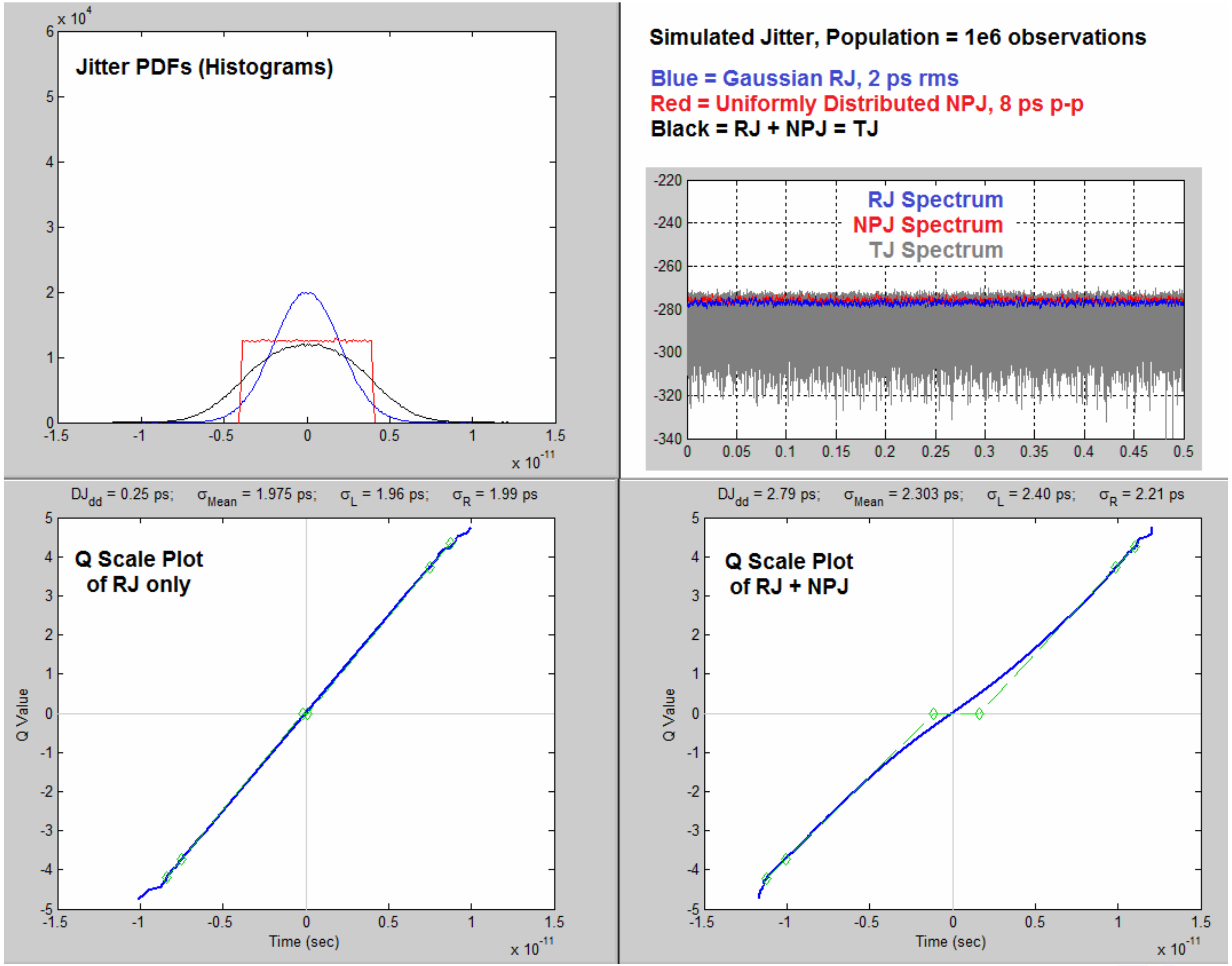
Blue = Gaussian RJ, 2 ps rms
Red = Sinusoidal Jitter, 8 ps p-p
Black = RJ + PJ = TJ

DJ_{dd} = 0.31 ps; σ_{Mean} = 1.973 ps; σ_L = 1.95 ps; σ_R = 2.00 ps

DJ_{dd} = 6.19 ps; σ_{Mean} = 1.998 ps; σ_L = 1.87 ps; σ_R = 2.12 ps

Jitter Analysis Advances

Q-Scale transformations and BUJ

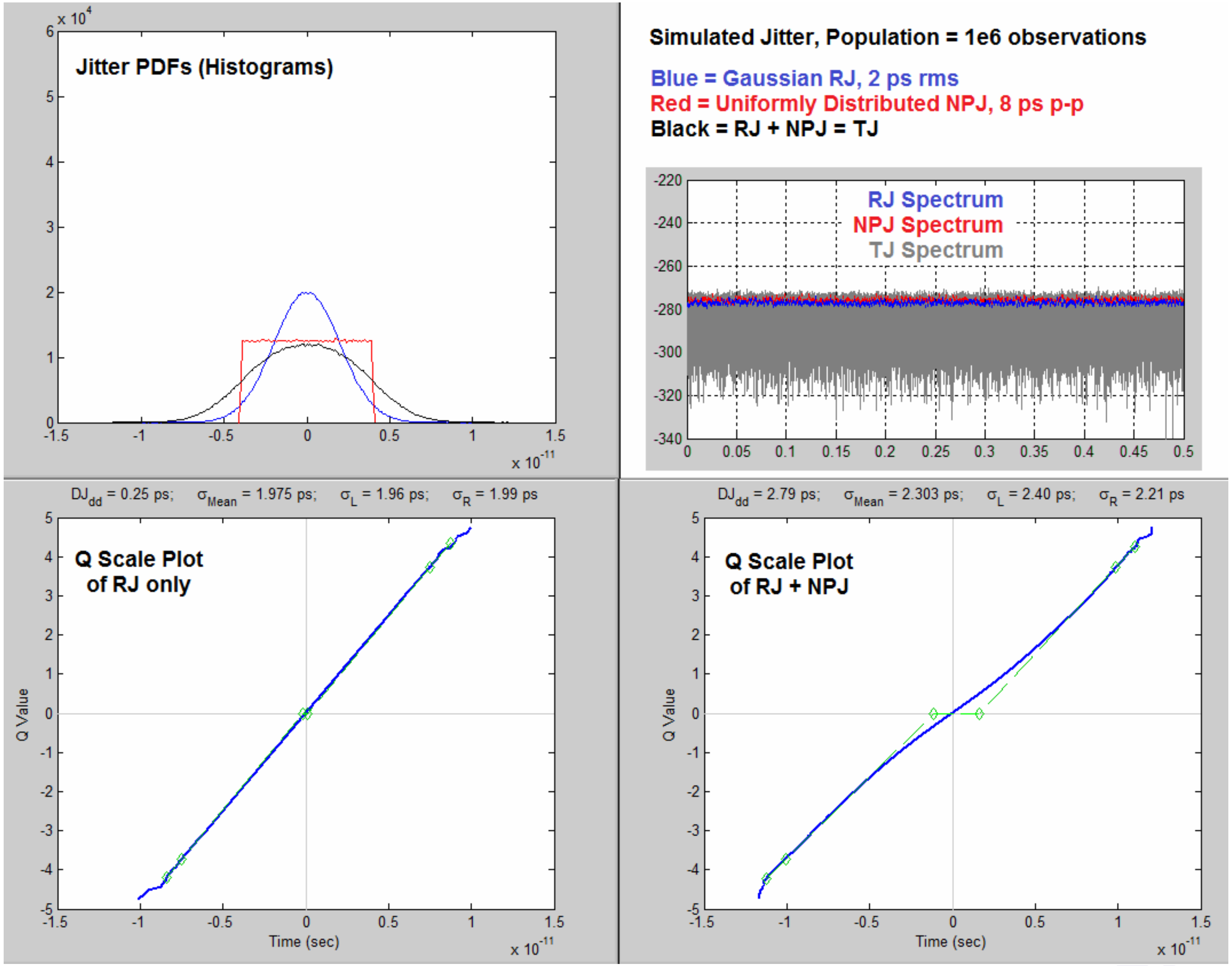


Simulated Jitter, Population = 1e6 observations

Blue = Gaussian RJ, 2 ps rms
Red = Uniformly Distributed NPJ, 8 ps p-p
Black = RJ + NPJ = TJ

Jitter Analysis Advances

Q-Scale transformations and BUJ



Simulated Jitter, Population = 1e6 observations

Blue = Gaussian RJ, 2 ps rms

Red = Uniformly Distributed NPJ, 8 ps p-p

Black = RJ + NPJ = TJ