USB 3.0 Physical Layer Testing

Sarah Boen
USB 3.0 Technology Timeline & Tektronix Involvement

2008

- Spec Development
- Silicon Phase

2009

- Test Vendor Compliance Group Participation
- PIL (Peripheral Interop Lab)
  - April 09 0.5 Test Spec (CWG Kickoff)
  - Dec 09 0.9 Spec
  - April 10 1.0 Spec

2010

- USB-IF Plugfests
  - Milpitas, CA
  - Taipei Taiwan

2011

- Deployment Phase
  - Taipei Taiwan

Integration Phase

- Product Development
- USB-IF Tool Development

Tektronix Test Solution Updates

Transmitter, Receiver, Channel
USB CTS Updates

- Draft .9 is available on the USB-IF site
- Updates not in .9 Specification
  - Tethered Devices (i.e Flash Drive) are tested with 11” Host Channel Only
    - Short cable is used for RX testing
    - Host channel is embedded for TX testing
  - Receiver Calibration Eye Height Limits: 145mV for Device and 180mV for Hosts
  - Receiver Jitter Tolerance Frequencies: 10Mhz, 20Mhz, and 33Mhz have been added
  - Updated Calibration Procedure
SuperSpeed Compliance

- PIL Lab
- USB Workshops
- Test Labs can provide pre-testing support and are currently being certified for USB testing

- Tektronix solutions are available in all locations!
USB 3.0 Key Considerations

- Receiver testing now required
  - Jitter tolerance
  - SSC, Asynchronous Ref Clocks can lead to interoperability issues

- Channel considerations
  - Need to consider transmission line effects
  - Software channel emulation for early designs

- New Challenges
  - 12” Long Host Channels
  - Closed Eye at Rx
  - Equalization
    - De-emphasis at Tx
    - Continuous Time Linear Equalizer (CTLE) at Rx

- Test strategy
  - Cost-effective tools
  - Flexible solutions
Tektronix Solutions for USB 3.0 Transmitter Testing

• Comprehensive Solution Goes Beyond Compliance
  – All measurements accessible in DPOJET for debug
  – Support for multiple test points (i.e. at the silicon pins or compliance test point)

• Complete Toolset for Characterizing USB 3.0 Designs
  – Create custom CTLE and Channel Emulation or De-Embed Filters with SDLA (Serial Data Link Analysis)

• Automated
  – No need to be a USB 3.0 Expert
  – Automatically acquire all necessary waveforms for processing (CP0, CP1, LFPS) with AWG7K or AFG

• SigTest Integration
  – SigTest is completely integrated into TekExpress
  – No need to manually configure the scope and setup SigTest for processing
  – User flexibility to process the waveforms using Tektronix algorithms and SigTest to compare the results

• Comprehensive Reporting
  – Complete Test Report in .mht format with pass / fail and margin results
  – Plots include for quick visual inspection
Transmitter Solutions

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  - User flexibility to process the waveforms using Tektronix algorithms and SigTest to compare the results

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  - Automatically acquire all necessary waveforms for processing (CP0, CP1, LFPS) with AWG7K or AFG
USB 3.0 Test Fixtures

- Two options for USB 3.0 Test Fixtures
  - Tektronix supplied fixtures
    - Enables SW channel emulation for TX and RX testing
    - Published electrical specifications
    - Supports TX, RX, and Cable testing
    - Available from Tektronix
  - USB-IF supplied fixtures and cables (shown below)
    - Used for compliance testing
    - Enables SW channel emulation for TX only
    - Supports TX and RX testing
    - Available from the USB-IF
USB 3.0 Compliance Test Configuration

- **USB 3.0 is a closed eye specification**
  - Reference channel is embedded and CTLE is applied

- **USB 3.0 Reference Channels**
  - **Host Reference Channel**
    - 11” back panel is applied for device testing
  - **Device Reference Channel**
    - 5” device channel is applied for host testing
  - **3 Meter Reference Cable**
    - Used for host and device (except captive devices) testing in addition to reference channels

- **USB 3.0 Reference Equalizer**
  - Attenuates the low frequency content of the signal to open the eye
Fixture and Channel De-Embedding

- Why de-embed - Improve Margin
  - Removes fixture effects that are not present in a real system
  - Remove the effects of the channel and connector for measurements defined at the TX pins

- De-Embedding Process
  - Characterize channel with TDR or Simulator to create S-parameters
  - Create de-embed filter with SDLA software
Channel Embedding

- Compliance Testing is done by embedding the compliance channel, but many designers want to validate other channel models
  - Understand transmitter margin given worst case channels
  - Model channel and cable combinations beyond compliance requirements
  - Create interconnect models with SDLA software to analyze channel effects
Receiver Equalization

- Tektronix USB Solutions ships with the USB Specification defined CTLE Function
- Customizing CTLE functions and creating filters for use with Tektronix’ USB Solution is easily achieved with SDLA (Serial Data Link Analysis Software)
USB 3.0 Transmitter Measurement Overview

- **Voltage and Timing**
  - Eye Height
  - Pk to Pk Differential Voltage
  - RJ
  - DJ
  - TJ
  - Slew Rate

- **Low Frequency Periodic Signaling (LFPS)**
  - Pk to Pk Differential Voltage
  - Rise / Fall Time
  - AC Common Mode
  - tBurst
  - tRepeat
  - tPeriod

- **SSC**
  - Modulation Rate
  - Deviation
Voltage and Timing

- Voltage, Eye Height, Jitter
LFPS TX Measurements

- LFPS signaling is critical for establishing link communication
- LFPS TX test verify common mode, voltage, tPeriod, tBurst, tRepeat
- Channel is not embedded for LFPS tests
SSC Measurements

- Both Maximum and Minimum Frequency Deviation must be considered
  - Assume nominal UI of 200ps
  - Limits are +0/-4000ppm and +0/-5000ppm, plus +/- 300ppm for ref clock accuracy
- Compliance Channel is not embedded for SSC measurements
**LFPS RX Test**

- Required Compliance Test to verify that the DUT RX will respond to LFPS signaling
- Test is ran across four different settings

<table>
<thead>
<tr>
<th>tPeriod</th>
<th>VTX-DIFF-PP-LFPS</th>
<th>Duty Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>50ns</td>
<td>800mV</td>
<td>50%</td>
</tr>
<tr>
<td>50ns</td>
<td>1000mV</td>
<td>40%</td>
</tr>
<tr>
<td>50ns</td>
<td>1000mV</td>
<td>60%</td>
</tr>
<tr>
<td>50ns</td>
<td>1200mV</td>
<td>50%</td>
</tr>
</tbody>
</table>
LFPS RX Test

- AWG generates spec compliant LFPS signaling
- Validate LFPS response with RT Scope
USB 3.0 Droop / Drop Test

- New Test Fixture Available from USB-IF
  - Provides 150mA / 900mA load
  - Previous fixture provides 100mA / 500mA load

- Amount of power drawn is changed from 500mA to 900mA for high power devices

- Fixture is orderable at:
USB 3.0 Compliance and Automation

• Complete Automation of USB 3.0 Measurements with TekExpress
• No need to learn technology specific software applications - TekExpress is a Common Framework from Serial Applications including SATA, USB, DisplayPort, HDMI, and Ethernet
• TekExpress utilizes DPOJET USB 3.0 Specific algorithms making it easy to move from compliance to DPOJET for debug
TekExpress USB 3.0 Automated Solution

- Supports testing for USB 3.0 Hosts and Devices
- Automatically selects the correct channel emulation filter when software is selected
- Easily select measurements of interest for test execution
- Supports all compliance and LFPS TX measurements
- User choice of algorithm execution- SigTest or DPOJET
- Automates DUT toggling to acquire CP0, CP1, and LFPS Patterns
Complete USB 3.0 Transmitter Solution

DPO/DSA70000 Series Oscilloscopes

- Go Beyond Compliance Testing
  - Debug Suite with DPOJET
  - SDLA for Channel Modeling
  - Tektronix Super Speed USB Fixtures

- Automation software for characterization and compliance
  - TekExpress with option USB-TX (includes option USB3)

- Recommended Scope
  - 12.5 GHz Real-Time Scope
    - 50GS/s Sample Rate
  - P7313SMA Differential Probe (Optional)

TF-USB3-AB-KIT
USB 3.0 Receiver Testing
USB 3.0 Receiver Testing Overview

- A jitter tolerance test is required for certification, though debug and characterization capabilities are needed to ensure that receivers will work in real world conditions
  - Send specific test data patterns to the device-under-test (DUT) through a known channel (fixtures and cables)
  - Add a specific “recipe” of stresses and de-emphasis
  - Command the DUT into loopback mode
  - Return “echoed” data to a BERT
  - Detected errors are inferred to be a result of bad DUT receiver decisions
USB 3.0 Compliance Receiver Tolerance Test Overview

- Seven Test Points
- SSC Clocking is enabled
- BER Test is performed at $10^{-10}$
- De-Emphasis Level is set to -3dB
- Amplitude at the end of the compliance channel: 180mV Hosts and 145mV Devices
- Each SJ term in the table below is tested one at a time after the device is in loopback mode

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SJ</th>
<th>RJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>500kHz</td>
<td>400ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>1MHz</td>
<td>200ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>2MHz</td>
<td>100ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>4.9MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
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<tr>
<td>10MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
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<tr>
<td>20MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>33MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
<tr>
<td>50MHz</td>
<td>40ps</td>
<td>2.42ps RMS</td>
</tr>
</tbody>
</table>
Generic USB 3.0 RX Test Configuration

Host Receiver Test

- Error Detector
- Pattern Generator
- Reference Channel
- Adapter

- SMA
- USB (type B)
- USB (type A)
- Host DUT

Device Receiver Test

- Error Detector
- Pattern Generator
- Reference Channel
- Adapter

- SMA
- USB (type A)
- USB (type B)
- Device DUT
- Short Cable
USB 3.0 Stress Recipe - Calibration

Long waveform capture by Real Time Scope

Mature standard with fully automated solutions for stress calibration and good correlation

Test Equipment

SigTest Post-processing

PCle 3
USB 3
USB 3.0 Calibration

- **Host Calibration Setup**

- **Device Calibration Setup**

- **Calibration Procedure**

  ✓ Connect signal source directly to scope
  ✓ Calibrate de-emphasis to 3.0 dB + 5/-0% dB using CP0 with SSC off and CTLE off
  ✓ Connect signal source through the compliance channel
  ✓ Measured peak to peak TJ
  ✓ Calibrate RJ(2.42 +/- 10% ps RMS/30.8 +/- 10% ps peak to peak at a BER of 10-10) with CP1 at the end of the channel applying CTLE and JTF
  ✓ Calibrate SJ using CP0 until measured peak to peak TJ increases by that amount. Apply CTLE and set JTF at 50Khz.
  ✓ Expected Tj with jitter off should be less than 100 ps. If this threshold is exceeded, replace the channel fixture(s) and/or cable(s).
USB 3 Loopback Negotiation

- **RX Detect**
  - SuperSpeed Link Partner is
  - Availability is determined

- **Polling.LFPS**
  - DUT and Generator Send LFPS and establishes LFPS Handshake

- **Polling.RxEQ**
  - DUT and Generator send TSEQ in order to establish DUT RX Equalization Settings

- **Polling.Active**
  - DUT and Generator send 8 TS1

- **Polling.Configuration**
  - Generator instructs DUT to loopback by setting the loopback bit in the TS2 training sequence

- **Polling.Idle**
  - DUT directed to Loopback
Two Solutions for USB 3.0 Receiver Testing

BERTScope BSA85C and AWG7122C

- Tektronix has the right solution to meet your needs
  - Both provide fully automated Receiver Compliance and Jitter Tolerance Testing
  - Both offer advanced impairments to debug problems caused by SSC or other anomalies
  - Both support a wide range of HSS Standards
  - Both support asynchronous clocking (SKP order set rejection)

- BERTScope
  - Performance that you need up to 26Gb/s for next generations standards including DisplayPort 1.2, SATA/SAS, 10G KR, PCI Express 3.0
  - Impairments can be changed on the fly to see the effect of increasing or reducing jitter
  - Debug and analysis tools enable quick identification of RX errors
  - True BER measurements

- Arbitrary Waveform Generator
  - Common platform for MIPI, HDMI, USB 3.0, and SATA
  - Only solution available that provides a common setup between transmitter and receiver testing without the need of RF switches and additional setup complexity
  - Easily apply sparameter models to verify designs under different channel conditions without the need of physical ISI channels
  - Generate SJ > 1Ghz to debug elusive problems caused by other system clocks
BERTScope USB 3.0 RX Test Configuration

USB Switch creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode.

DPP125B De-emphasis Processor
CR125A Clock Recovery
BSA85C BERTScope
AWG USB 3.0 RX/TX Test Configuration

- Only test equipment setup with a common configuration for Receiver and Transmitter Testing
- All Signal Impairments including channel impairments generated by the AWG
- No need for external error detectors
  - Only Oscilloscope based bit or symbol error detection solution (Ellisys Protocol Analyzers also supported)
Tektronix USB 3.0 Summary

- **Complete**
  - Solutions available today for USB3.0 Transmitter, Cable, Channel, and Receiver Testing

- **More than a Compliance Solution**
  - Solutions to meet debugging, characterization, and compliance needs
  - Receiver stresses that go beyond compliance

- **Increased Productivity**
  - Fully automated transmitter and receiver test solutions
  - Analysis tools integrated on the BERTScope enable the isolation and root cause determination of receiver errors

- **Performance**
  - 26Gb/s BERTScope provides coverage for next generation testing needs
  - Low noise floor enables measurements of small data eyes for compliance testing and receiver calibration
  - Only 6.25Gb/s hardware serial trigger to capture protocol events that are causing failures or interoperability problems

- **Expertise**
  - Actively engaged in the USB Working Groups
  - Regional support by Tektronix Application Engineering Experts
Extensive application information at:

www.tek.com
Resources

• Access to Specifications

• Tektronix USB Electrical PHY Tools and MOI’s
  – www.tektronix.com/usb
  – www.tektronix.com/software