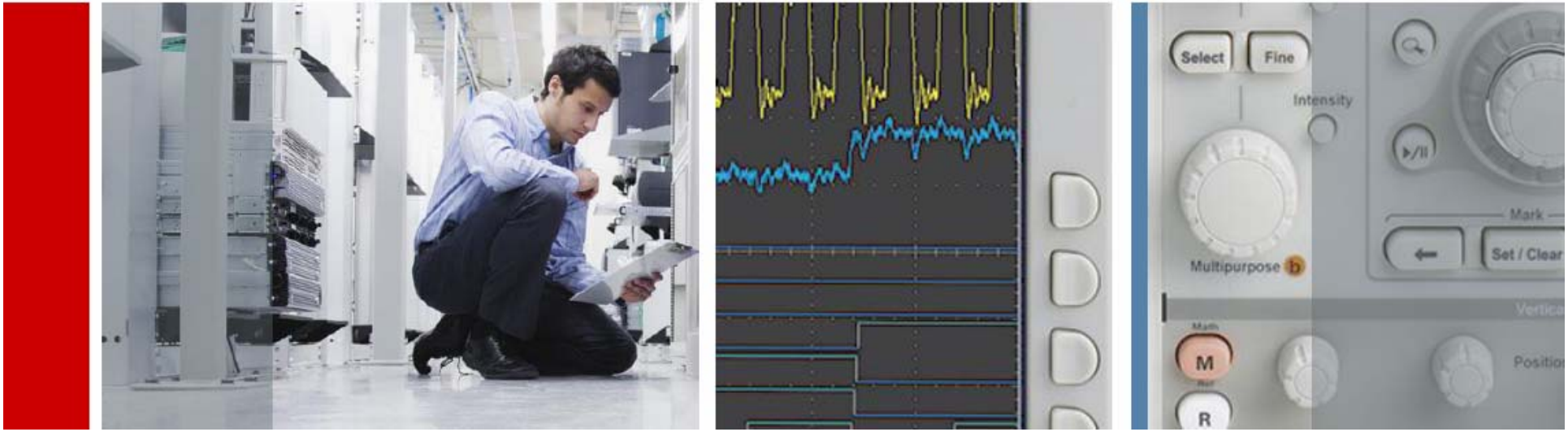
Tektronix MHL Solution- A complete Solution



MHL
Mobile High-Definition Link

Tektronix®

Tektronix is a **contributor** adopter for MHL CTS

Welcome MHL Adopters

BizLink Technologies, Inc.
www.bizlinktech.com
Cable Assemblies and Wiring Harnesses

Compal Electronics Inc.
www.compal.com
Electronics manufacturer of notebook computers and monitors

Explore Microelectronics, Inc.
http://www.epmi.com.tw
Fabless company developing high-speed interface ICs

Fairchild Semiconductor
www.fairchildsemi.com
Delivers semiconductor solutions for power and mobile designs

Hosiden Corporation
www.hosiden.com
Manufactures and sells electronic components, electromechanical parts and LCD elements

Johnson Component and Equipment Co., Ltd.
www.jcecable.com
Cable Manufacturer

Niketech Electronic Corporation
www.niketech.com.tw
Provider of connectors for the electronics industry

Parade Technologies, Inc.
www.paradetech.com
Develops and supplies advanced and cost-effective high-speed display interface solutions

Sumitomo Electric Industries, Ltd.
global-sei.com
Designs, manufactures and sells cable and components and advanced electronic devices

Sunplus Technology Co., Ltd.
www.sunplus.com
Provider of multimedia IC solutions

Sure-Fire Electrical Corporation
www.sure-fire.com.tw
Global OEM/ODM supplier of cables, connectors and devices

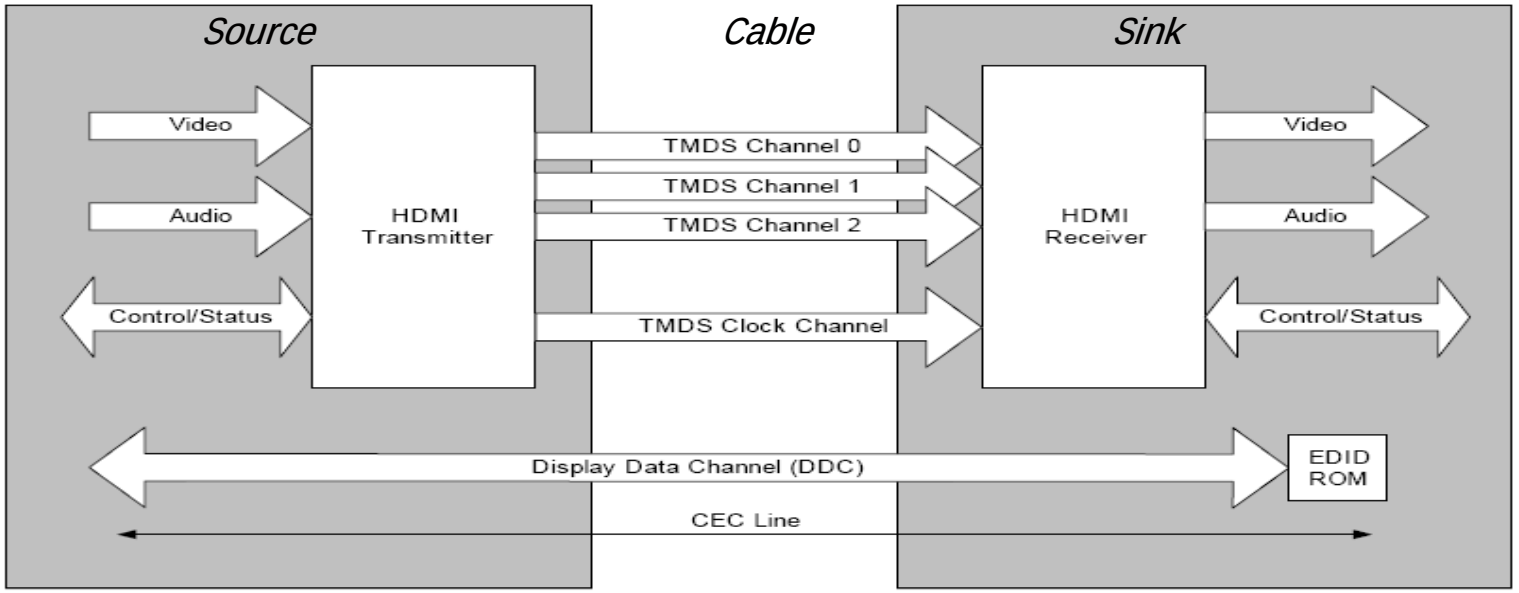
Synopsys
www.synopsys.com
Provider of electronic design automation (EDA) software, IP and services

Tektronix
www.tek.com
Test, measurement and monitoring solutions

YFC-BonEagle Electric Co., Ltd.
www.cables.com.tw
Manufactures power cord sets, LAN cable, patch cords and networking accessories

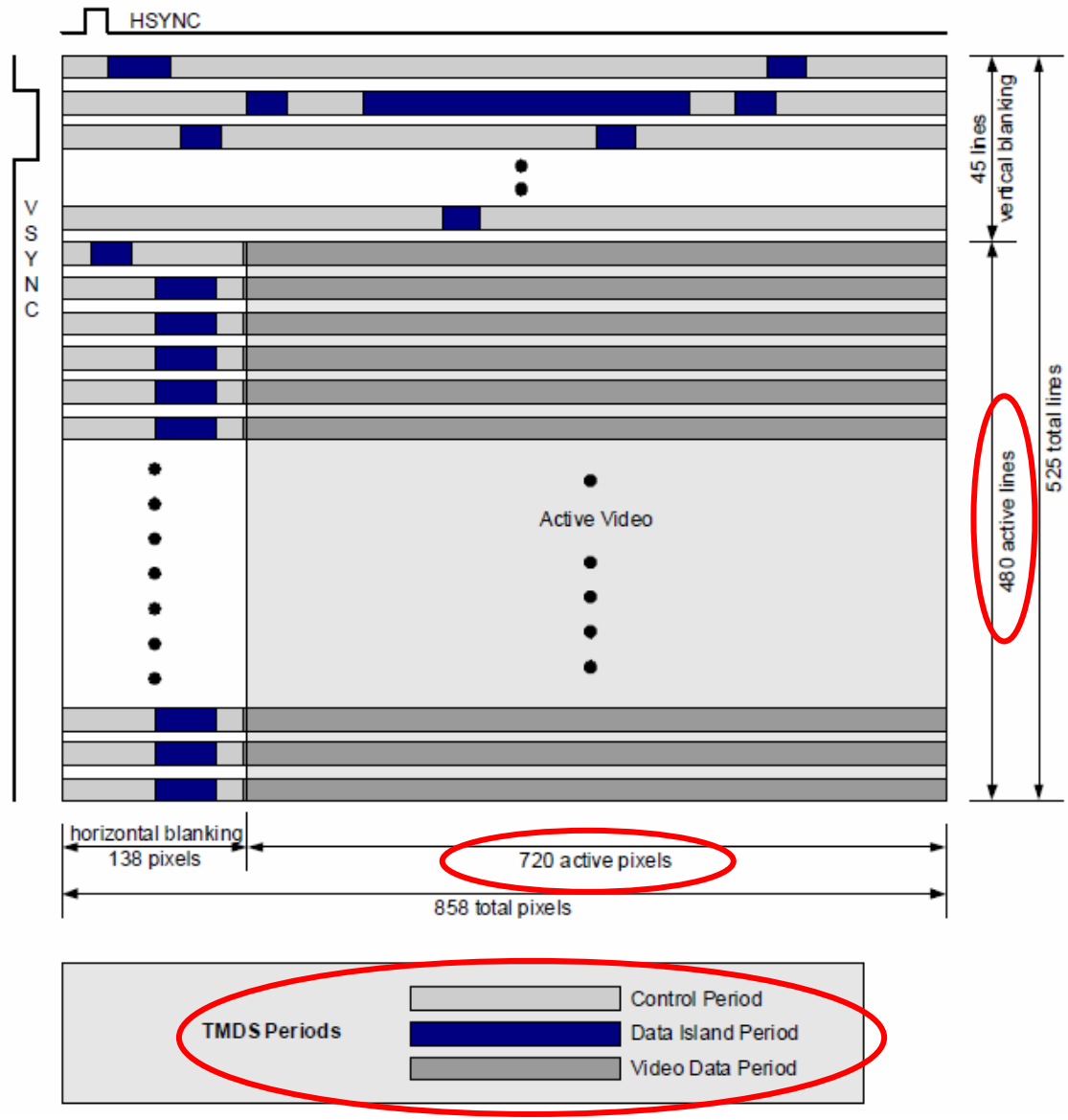
Tektronix®

HDMI briefing



- **Clock**
  - 1 lane differential clock
  - $T_{clcck} = 10 * T_{BIT}$
- **Data**
  - 3 lanes TMDS differential data
- **DDC / EDID**
  - DDC (Display Data Channel) is used by the Source to read the Sink's E-EDID (Extended Display Identification Data) in order to discover the Sink's configuration and/or capabilities.

TMDS (480p video frame)



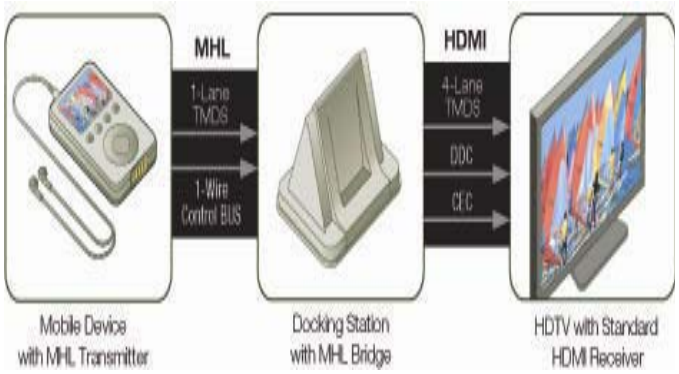
Tektronix®

MHL Introduction

Mobile HD Link (MHL) technology is a low pin count HD audio and video interface that connects portable electronics devices such as mobile phones, digital cameras, camcorders and portable media players, to HDTVs.

The technology allows mobile devices to output digital 1080 Full HD resolution via the existing mobile connector without the real estate and cost of another dedicated video connector.

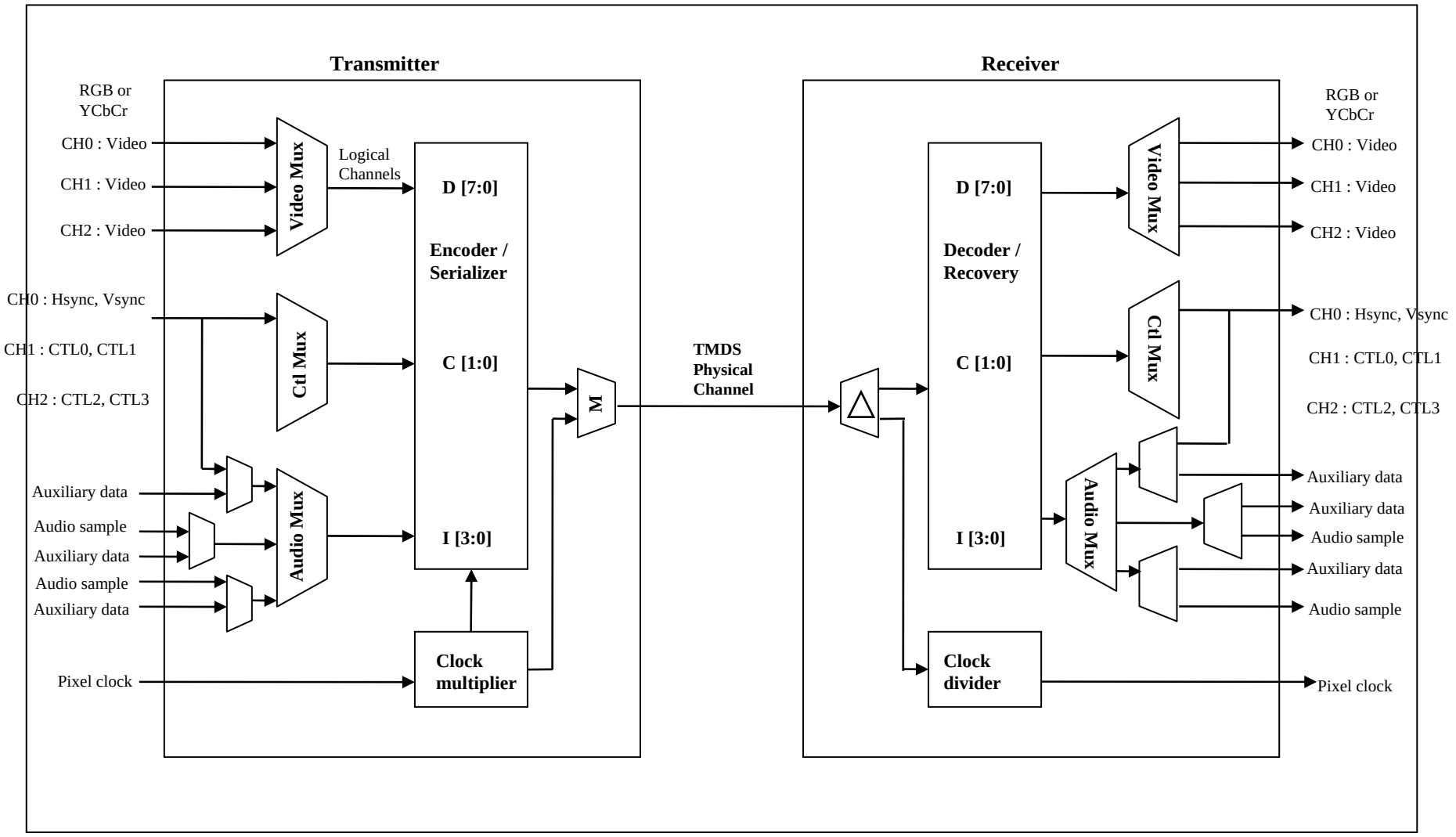
Together with an MHL-to-HDMI bridge, the MHL-enabled mobile device becomes a fully compliant HDMI source and can connect to the television's standard HDMI input port.



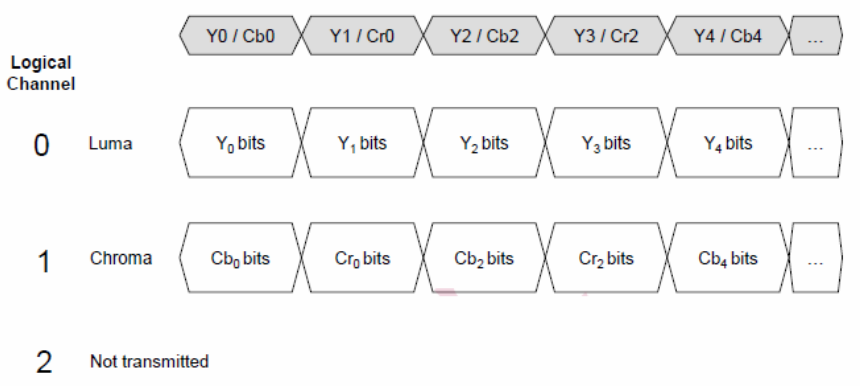
Difference between HDMI and MHL

- **HDMI**
  - Four lanes
    - One differential clock lane
    - Three differential TMDS data lanes
  - DDC
  - Max. 3.4GHz data rate/per lane @ 340MHz clock
  - HDMI connector
  - Max. resolution 4096 x 2160p24
  - Not support PackedPixel mode
  - For home multimedia
  - CTS 1.4
- **MHL**
  - Only one lane
    - One differential TMDS data lane
    - Clock is embedded
  - C-Bus
  - Max. 2.225GHz data rate @ 74.25MHz clock
  - Compatible with uUSB
  - Max. resolution 1920 x 1080i60 1080p in packedpixel mode
  - Support PackedPixel mode
  - For mobile device
  - CTS 1.1 (June 2011)

MHL Transmitter and Receiver block diagram

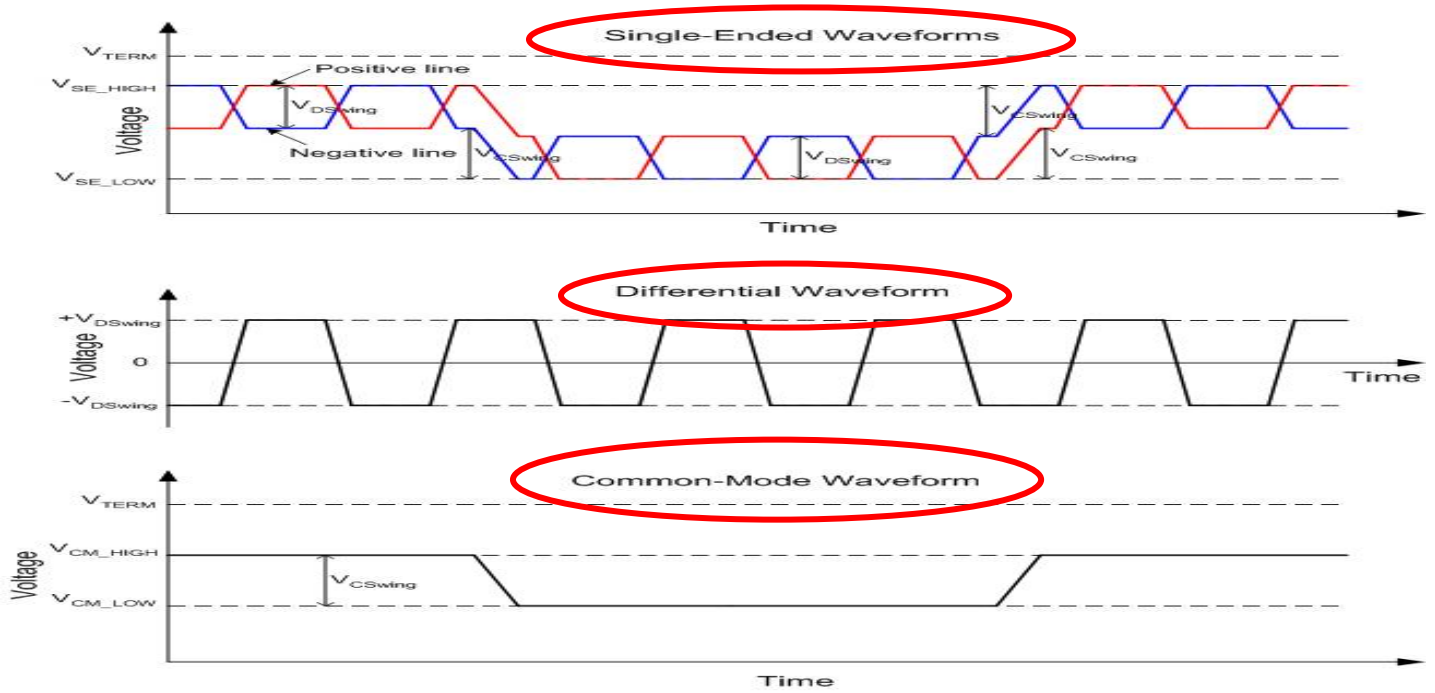


MHL overview



- **Video**
  - 24 bit mode
    - RGB 4:4:4 ; YCbCr 4:4:4 ; YCbCr 4:2:2
  - PackedPixel mode
    - It encoding maps the 8-bit YCbCr 4:2:2 data onto two Logical channels
    - It doesn't support encoding of RGB and YCbCr 4:4:4
- **Audio**
  - The behavior within Audio Sample Subpackets shall follow the corresponding rules specified in the IEC 60958 or IEC 61937 specifications.

MHL Signal Complexity – 1



- Clock rate / Date rate
  - Max. 75MHz MHL clock rate and 2.25GHz date rate (1080i/60Hz)
  - TMDS (Transition Minimized Differential Signaling) encoding in the Source converts the 8 bits of data into a 10 bit
  - Pack 3 data lanes and 1 clock lane into one lane
- Video mode minimum support requirement
  - 720x480p / 60Hz or 720x576p / 50Hz

MHL Signal Complexity – 2

MHL Consortium was formed in Sept 2009 with the following founding members:

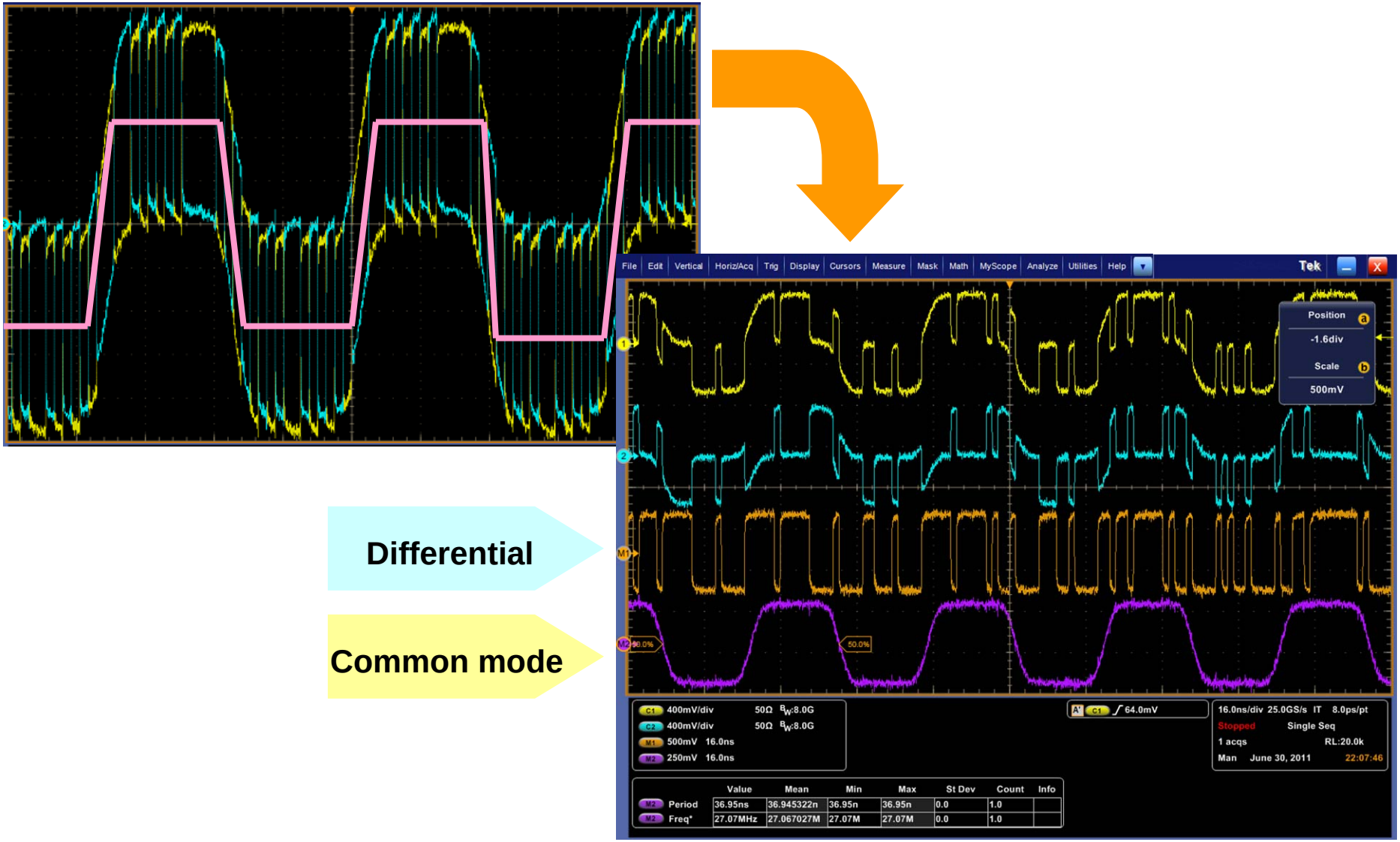
- NOKIA
- SAMSUNG
- Silicon Image
- Sony
- Toshiba

The Specification 1.1 version is announced in Q1 2011.
The MHL Consortium also released CTS 1.1 version in June 2011. Complete Tektronix solution were approved in CTS 1.1
Tektronix is a contributor adopter and actively involved in defining the CTS 1.1

9. Turn on the DUT and enable MHL mode through Device Discovery and CBus Information Exchange with the CBus Source board.
10. Examine the output of the Sink through the display image.
11. Record errors on the display if any for the given V_{TERM}, frequency and and DC voltage level.
12. If there is no error on the display in all recorded results, then PASS. Otherwise FAIL.

The above procedure is fully automated by Tektronix MHL Compliance Software (Option MHD).

MHL Signal (D+ and D-)



Tektronix®

TMDS Test Equipment -1

- **Digital Oscilloscope**
  - TMDS measurements require a High-bandwidth Digital Oscilloscope.
  - -3dB Bandwidth : DC to 8GHz or greater
  - Sampling rate > 20G sample/sec, when 2 or more channels are simultaneously sampling.
  - Sample memory : more than 20M samples per channel.

- **Differential Probe**
  - -3dB Bandwidth : DC to 8GHz or greater

- **MHL Pattern Generator *(For Sink Test)***
  - Generate MHL clock and data for all MHL defined format
  - Maximum output data bit rate > 3Gbps
  - Internal clock and data jitter generation (optional)
    - Two independent jitters
    - Jitter tolerance : 100KHz to 20MHz
    - Jitter amplitude : maximum 1 UI for 750Mbps ~ 3Gbps with 0.05 UI granulites

- **MHL Cable Emulator**
  - The MHL Cable Emulator shell represent the differential and common-mode insertion losses

- **Transition Time Converter (TTC)**
  - 120ps TTC is required

TMDS Test Equipment -2

- **Transition Time Converter (TTC)**
  - The transition time converter shall slow down the rise and fall times of output signal of MHL signal generator to 200ps (differential 20-80%) and 600ps (common-mode 20-80%)

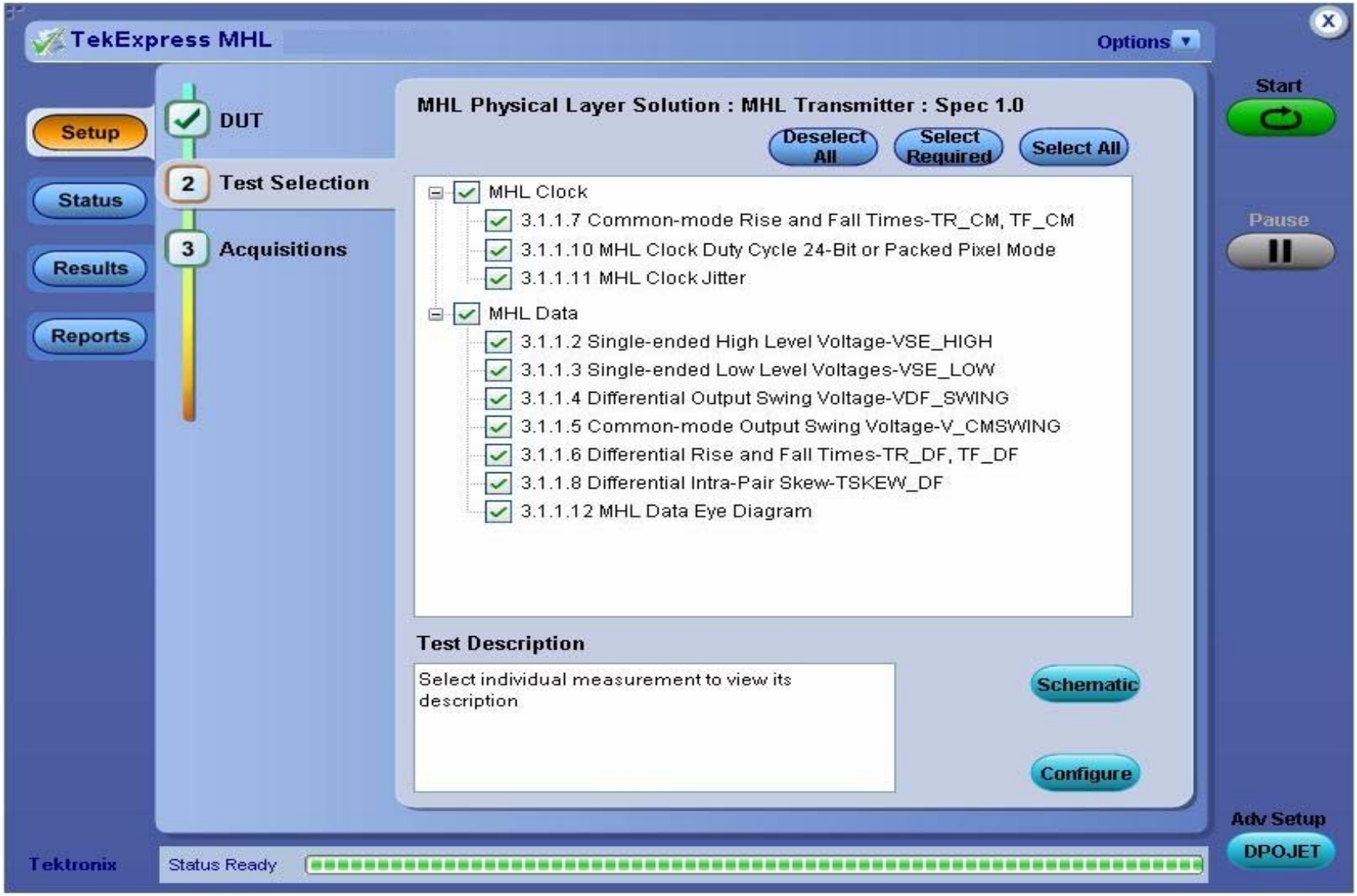
- **TDR/TDT Oscilloscope *(For Cable Test)***
  - TDR measurement
    - Bandwidth >= 18GHz
    - Pulse rise time <= 75ps (10-90%)
    - 2 port
    - Rise time adjustment capability to 200ps (20-80% differential) and 600ps (20-80% common-mode)
  - TDT measurement
    - Bandwidth >= 18GHz
    - Pulse rise time <= 75ps (10-90%)
    - 4 port

Tektronix MHL test Setup

- DPO/DSA/MSO 70804B/C – Real Time oscilloscope with BW >/= 8GHz
- MHL Compliance software –**Option MHD**
- Probes : Qty.2 - P7313SMA and Qty.1 - P7240
- MHL Protocol Analyzer Software **TEK-PGY-MHL-PA-SW**
- MHL Test fixture- Available from Wilder Technologies our fixture partner
- AWG7122C with Opt 01, 02 or 06, 08 for innovative direct synthesis based MHL Rx/Dongle testing performed manually using AWG MHL patterns and MOI
- C-Bus Sink and Source board is needed and is available from Simplaylabs
- DSA8200 or Equivalent with 80E03/80E04 and I-Connect software for MHL cable testing (performed manually using MOIs)

Tektronix MHL Tx measurement

MHL Compliance Software for Tx test - Option MHD



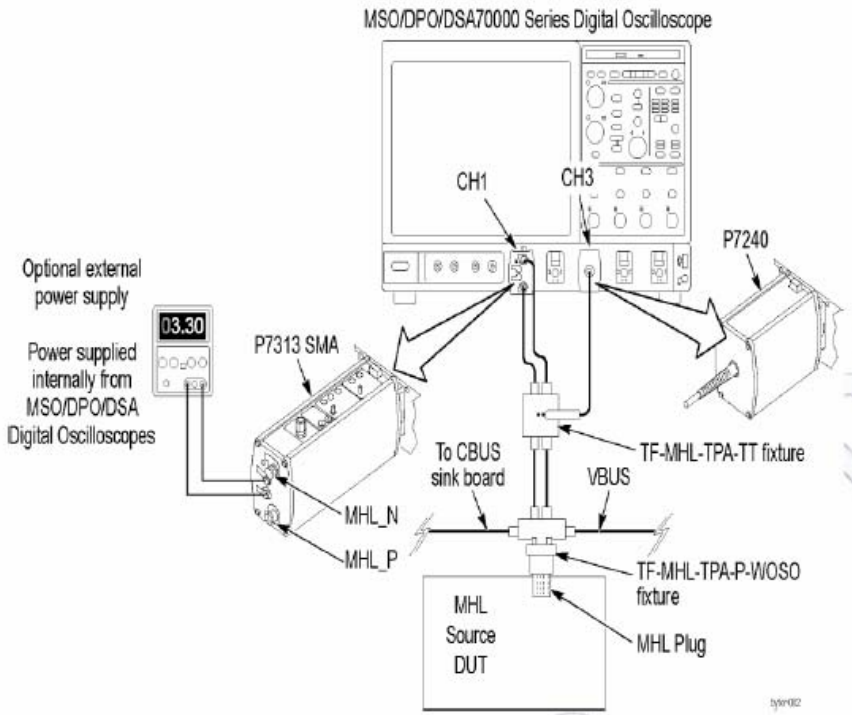
Tektronix®

MHL Tx tests supported in **Option MHD**

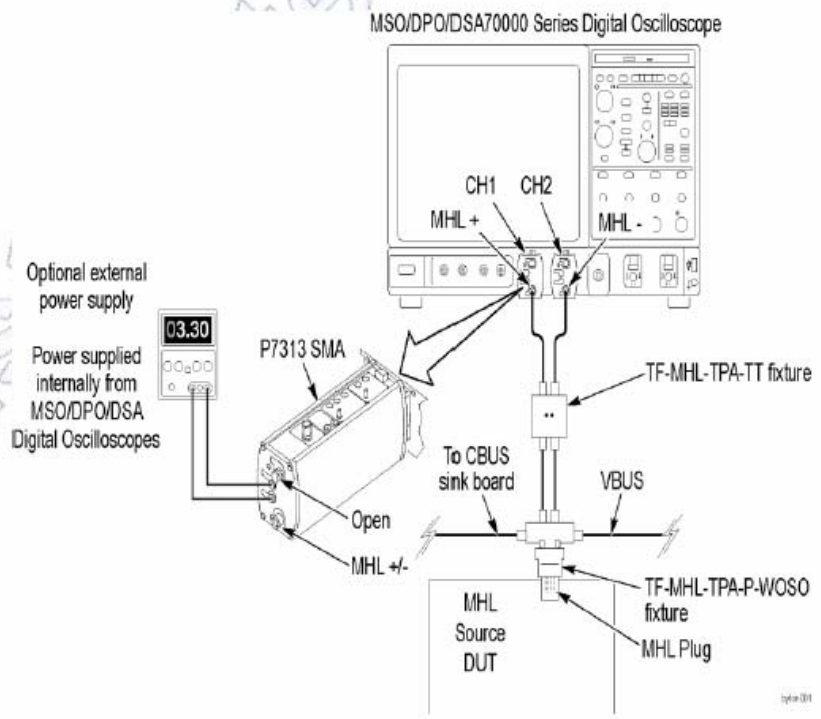
Physical Layer Tests:

- **MHL Transmitter Tests**
  - 3.1.1.2 Single-ended High Level Voltage V_{SE_HIGH}
    V_{TERM} -540mV ⩽ V_{SE_HIGH} ⩽ V_{TERM} +10mV
  - 3.1.1.3 Single-ended Low Level Voltage V_{SE_LOW}
    V_{TERM} -1760mV ⩽ V_{SE_LOW} ⩽ V_{TERM} -700mV
  - 3.1.1.4 Differential Output Swing Voltage $V_{DFSWING}$
    600mV ⩽ $V_{DFSWING}$ ⩽ 1000mV
  - 3.1.1.5 Common Mode Output Swing Voltage $V_{CMSWING}$
    360mV ⩽ $V_{CMSWING}$ ⩽ Min (720mV, 0.85 $V_{DFSWING}$)
  - 3.1.1.6 Differential Rise and Fall Times T_{R_DF}, T_{F_DF}
    T_{R_DF} ⩾ 75ps and T_{F_DF} ⩾ 75ps
  - 3.1.1.7 Common Mode Rise and Fall Times T_{R_CM}, T_{F_CM}
    600ps ⩽ T_{R_CM} ⩽ 2500ps and 600ps ⩽ T_{F_CM} ⩽ 2500ps
  - 3.1.1.8 Differential Intra Pair Skew T_{SKEW_DF}
    T_{SKEW_DF} ⩽ Min (0.12 T_{BIT}, 50ps)
  - 3.1.1.10 MHL Clock Duty Cycle (24-Bit or Packed Pixel Mode)
    35% T_{MHL} ⩽ Clock Duty Cycle ⩽ 65% T_{MHL}
  - 3.1.1.11 MHL Clock Jitter
    $T_{CLK\_JITTER\_TP1}$ ⩽ 0.25 T_{BIT} + 200ps , up to 2.25Gbps
  - 3.1.1.12 MHL Data Eye Diagram

Tektronix MHL Tx Setup



MHL Differential and CM test setup
7 tests

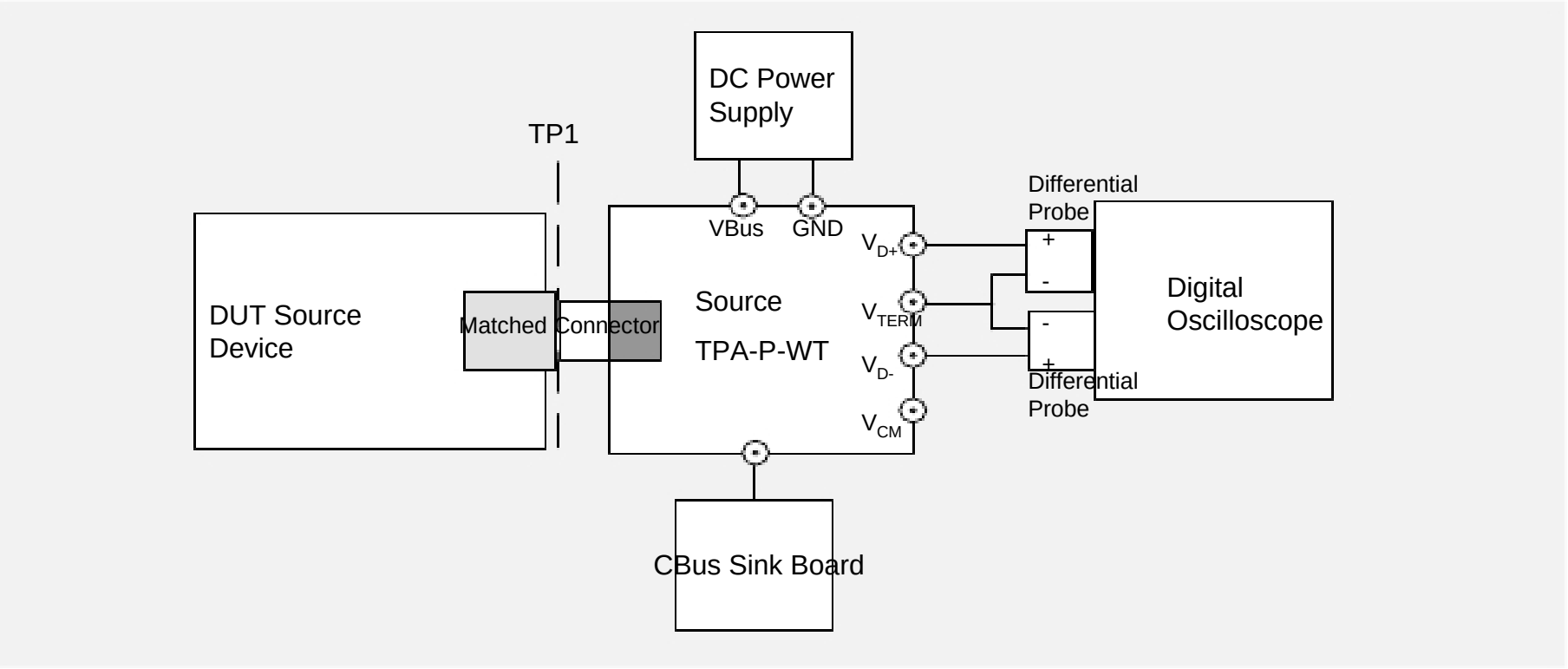


Single Ended and Intra Pair Skew test setup
3Tests

Also same setup is used for MHL Protocol Testing

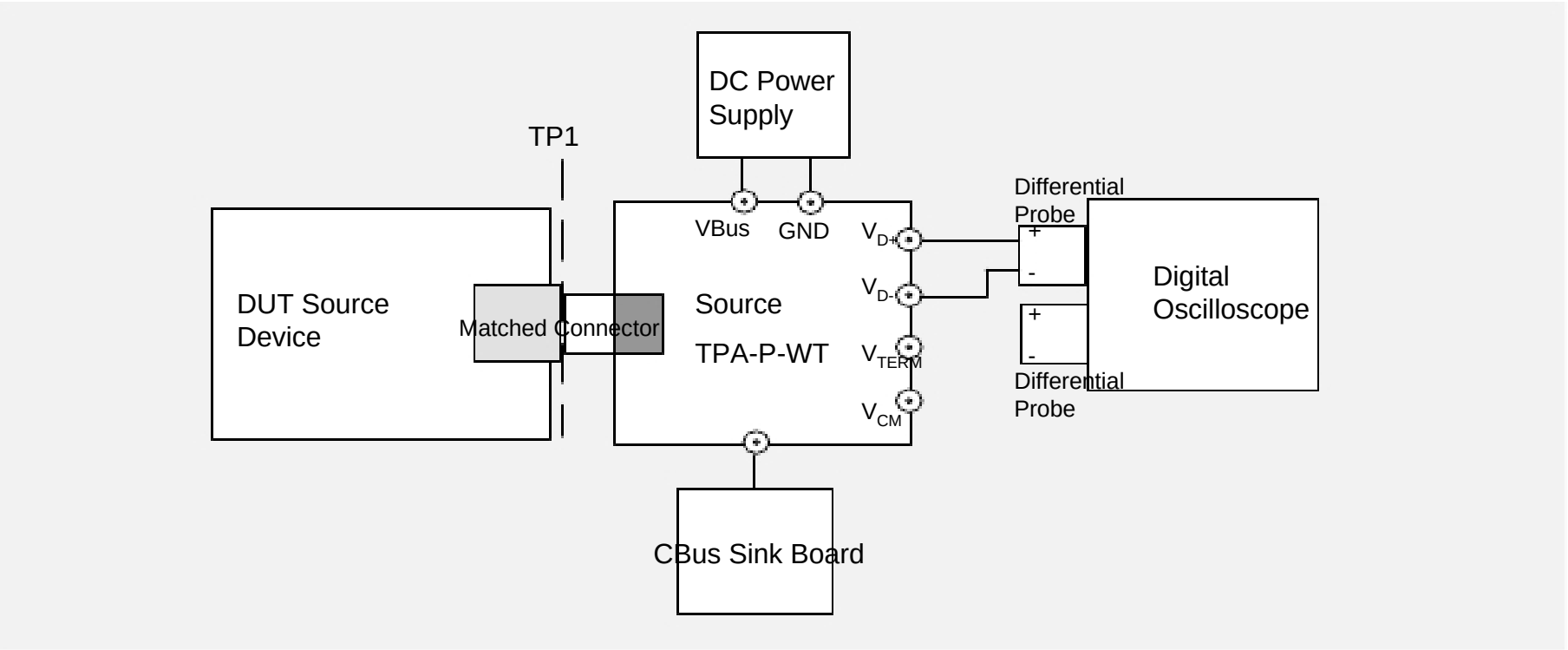
C-Bus Sink and Source Board is needed for hand shaking and is available from Simplaylabs.

MHL Source Tx – Single-ended mode



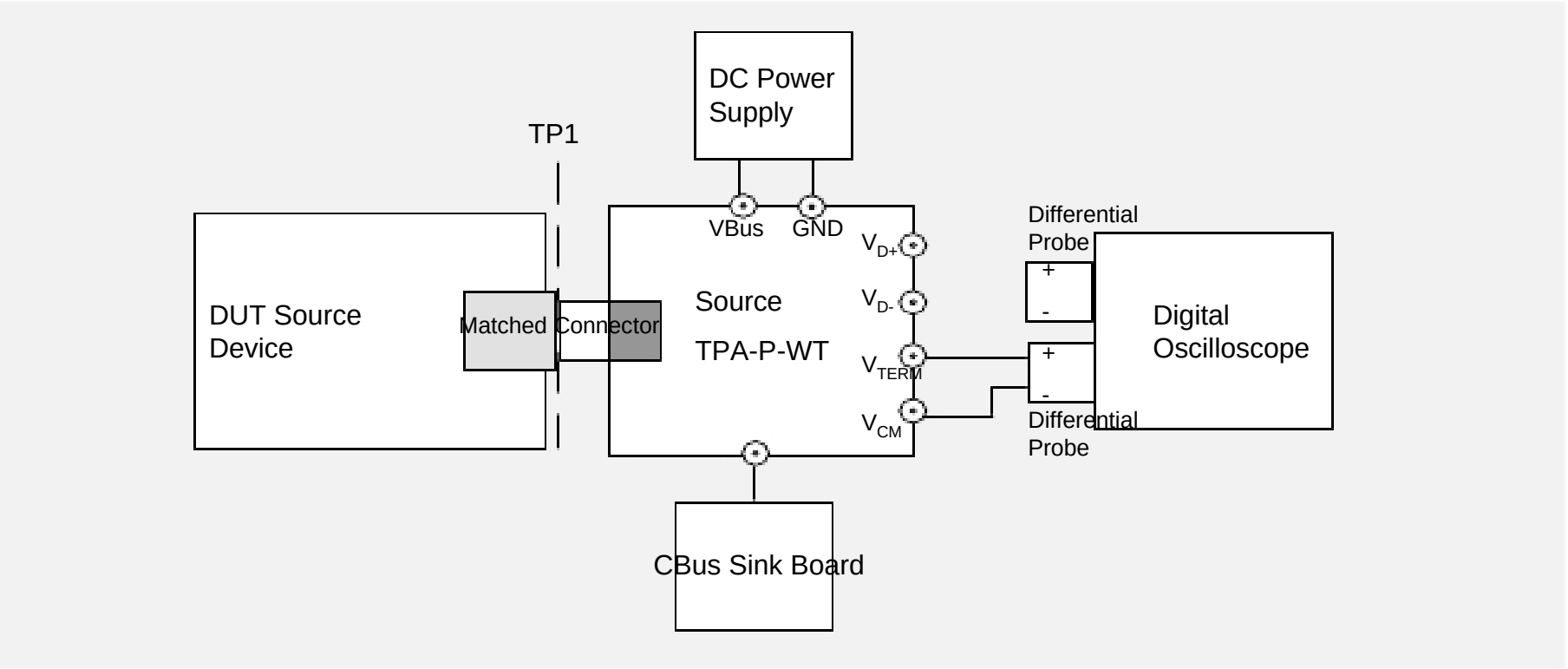
- Single-ended
  - 3.1.1.2 Single-ended High Level Voltage V_{SE_HIGH}
  - 3.1.1.3 Single-ended Low Level Voltage V_{SE_LOW}
  - Reference to V_{TERM} ; not Ground

MHL Source Tx – Differential mode



- Differential mode measurement is for DATA

MHL Source Tx – Common mode

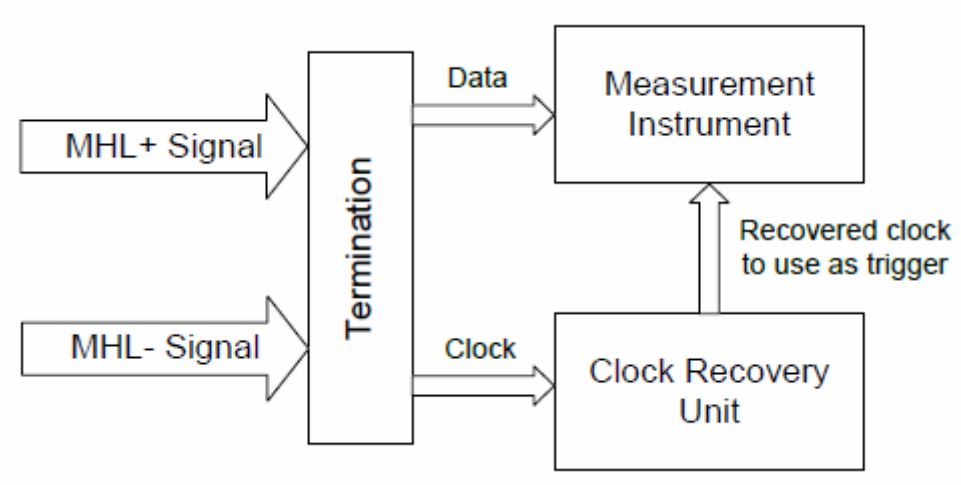


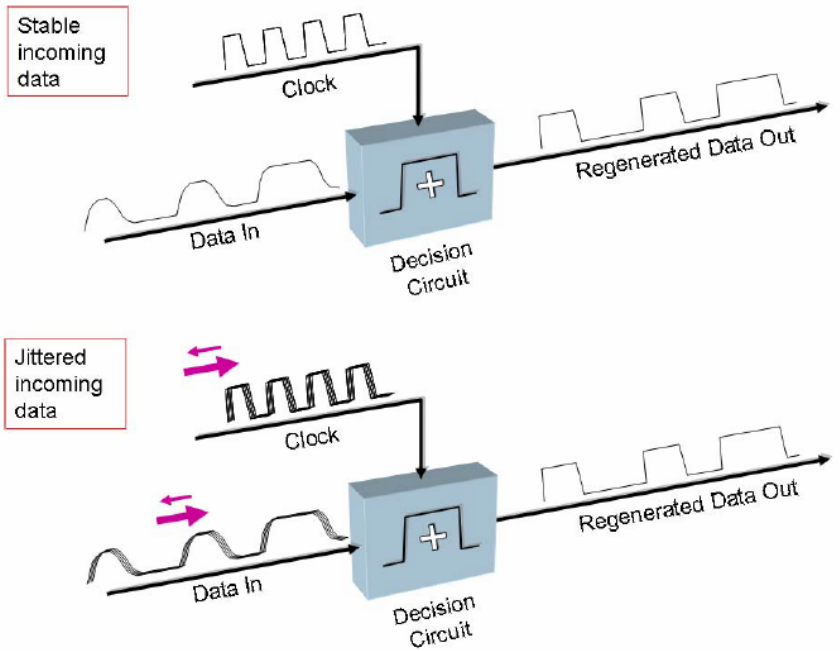
- Common mode measurement is for CLOCK

MHL Clock Recovery Unit

- **All MHL jitter and eye diagram specifications are specified relative to Recovered Clock, generated by a Clock Recovery Unit (CRU).**

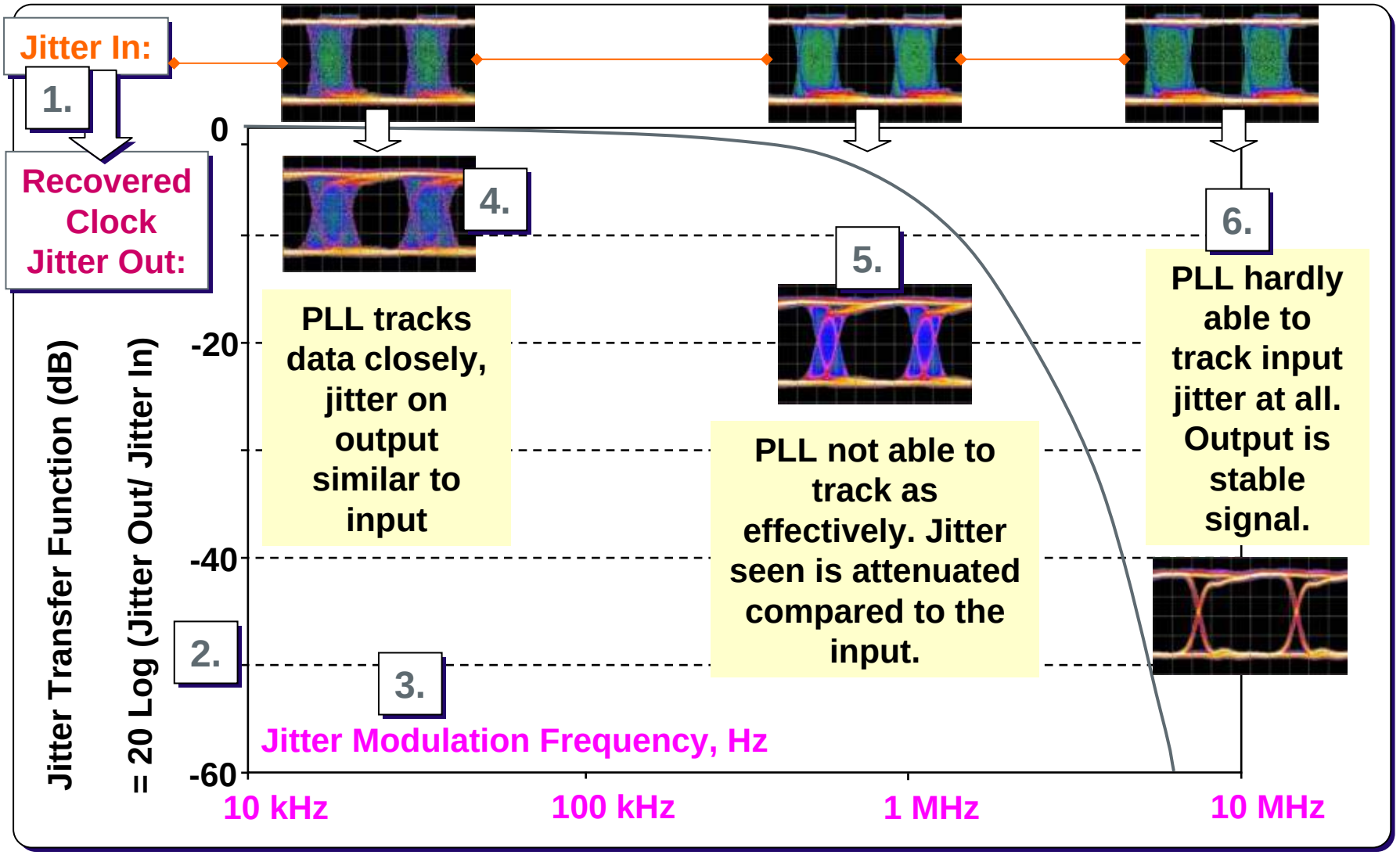
- $H(jf) = \frac{1}{\left[1 + \frac{jf}{f_0}\right]}$,where f_0 is 4MHz



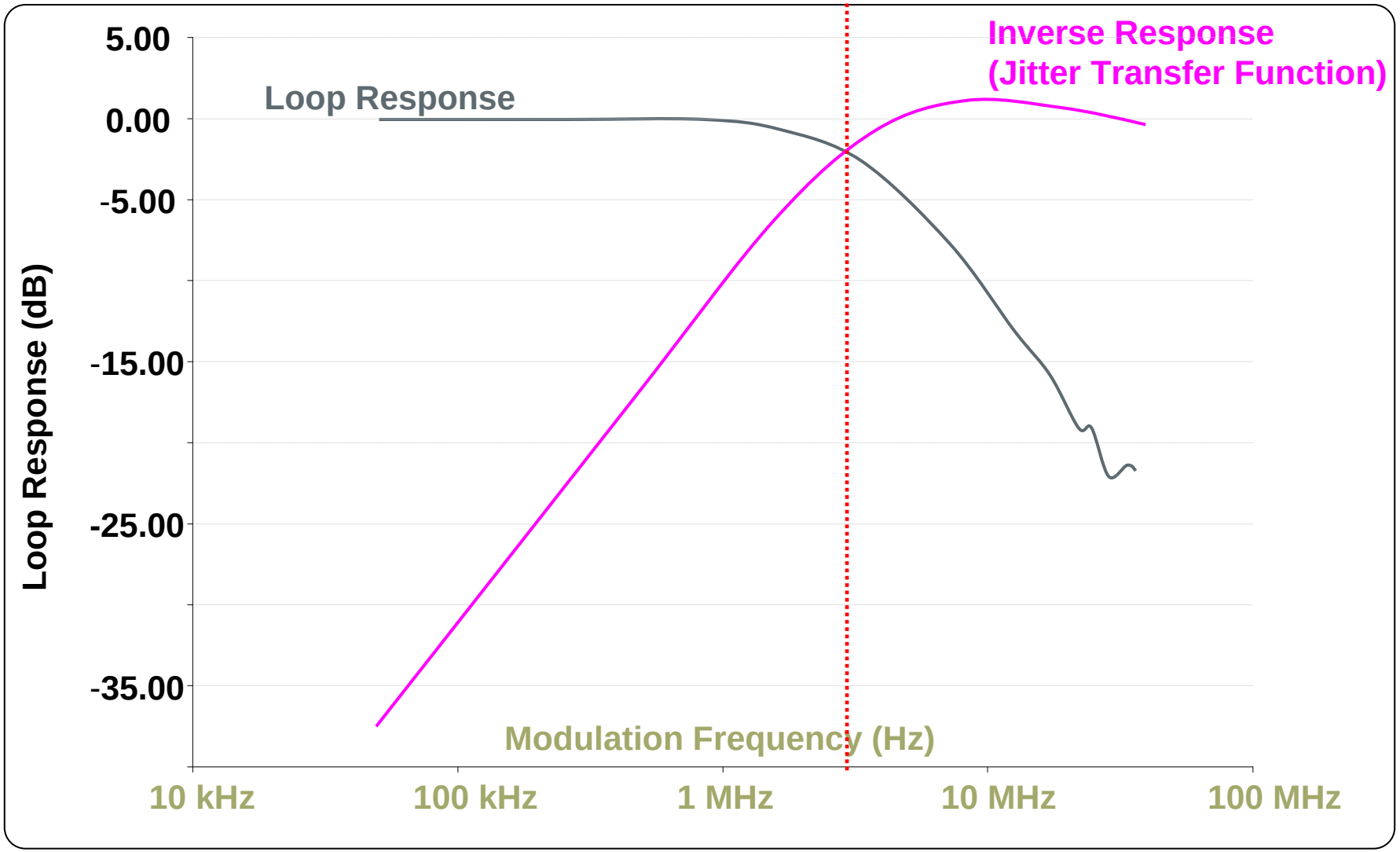


Tektronix®

The Loop Response - Illustrated



The Loop Response - Illustrated



Tektronix MHL Rx measurement

Tektronix®

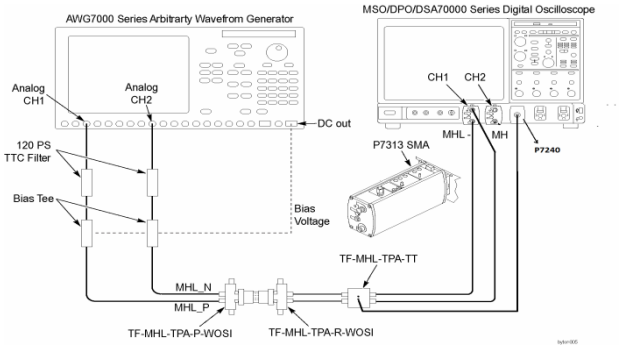
MHL Rx tests supported in MOI

Physical Layer Tests:

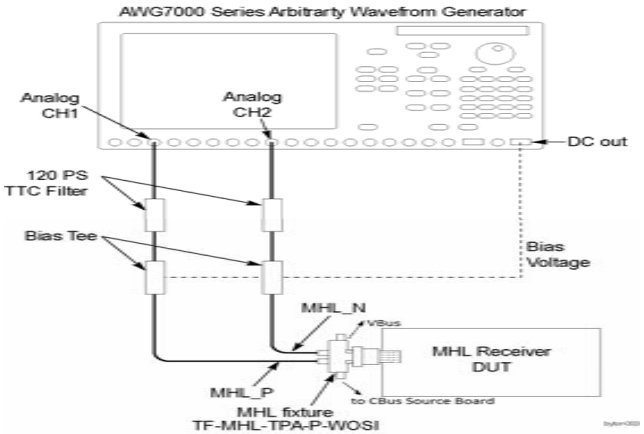
- **MHL Receiver Tests**
  - 4.1.1.2 Input Signal DC Voltage Level Tolerance
  - 4.1.1.3 Input Signal Minimum and Maximum Swings Voltages Level Tolerance
  - 4.1.1.4 Intra Pair Skew Tolerance
  - 4.1.1.5 Jitter Tolerance
- **MHL Dongle Tests**
  - 5.1.1.1 Input Signal Single-Ended Voltage Level Tolerance
  - 5.1.1.2 Input Signal Minimum and Maximum Swings Voltages Level Tolerance
  - 5.1.1.3 Intra Pair Skew Tolerance
  - 5.1.1.4 Jitter Tolerance

Tektronix MHL solution setup for Sink and Dongle Testing- MOI based

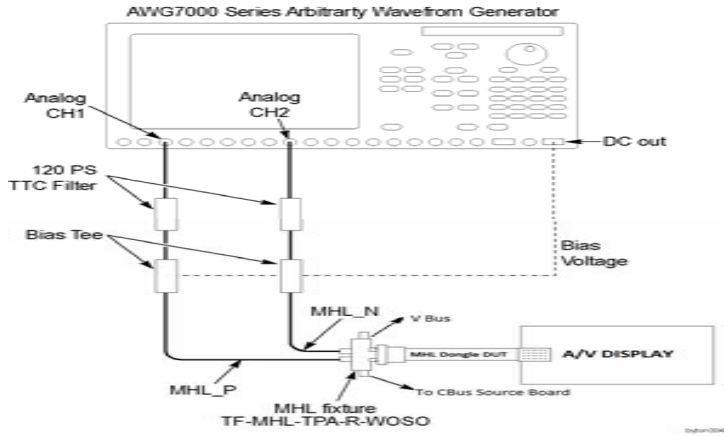
- **MHL Sink and Dongle Test setup based on Direct Synthesis capability of AWG7122C series shown below**
  - **Simple setup**
  - **Easy to use**



AWG Pattern Verification setup

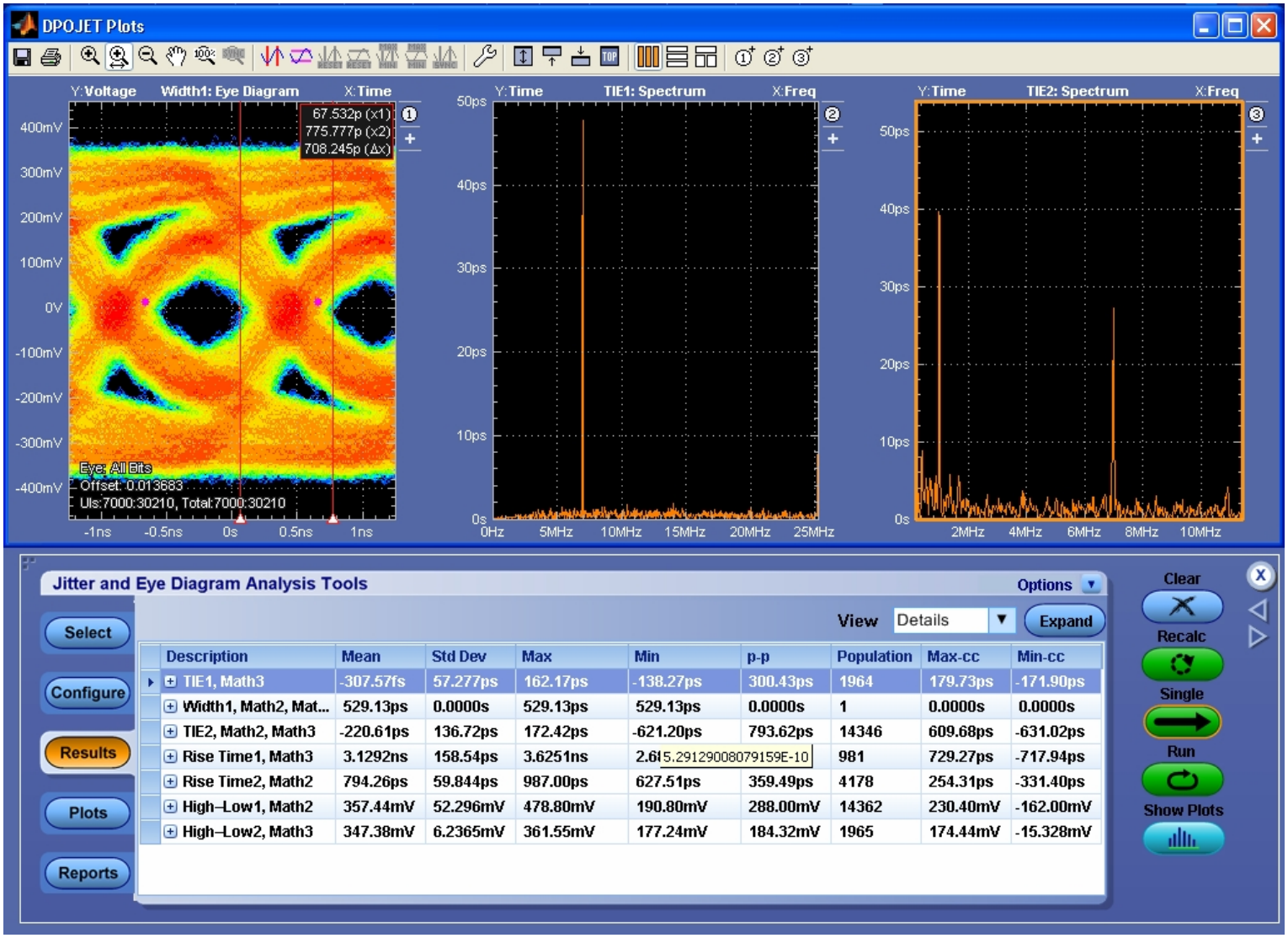


Common Test setup for all Sink Tests



Common Test setup for all Dongle Tests

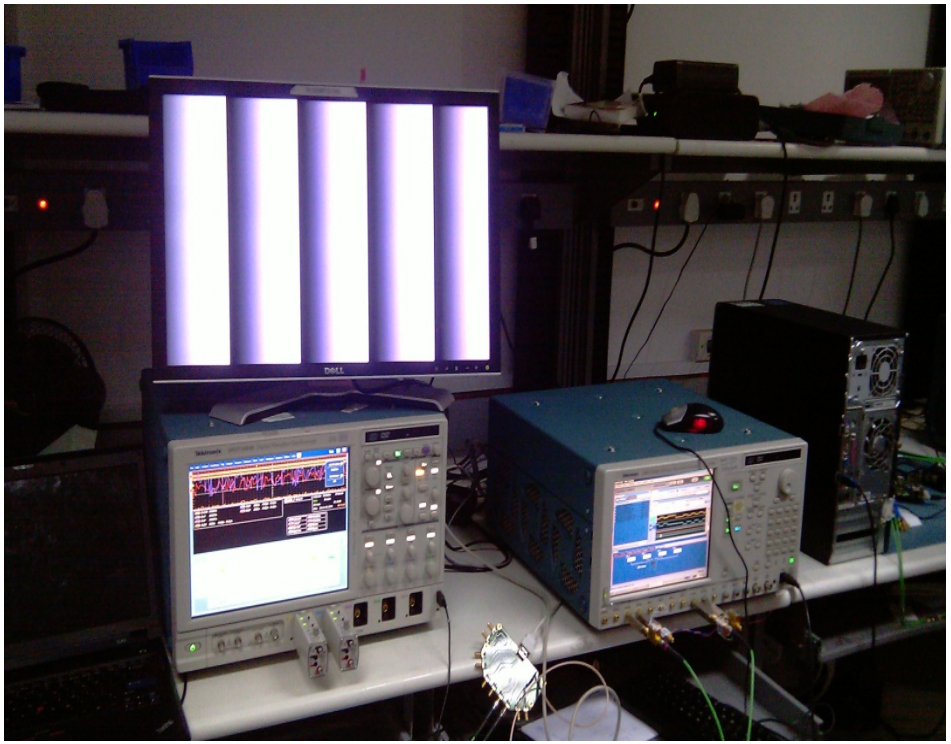
Tektronix MHL solution setup for Sink and Dongle Testing- MOI based



Tektronix®

Tektronix Actual Sink and Dongle setup – A Snapshot

- **MHL Sink and Dongle Test setup based on Direct Synthesis capability of AWG7122C series shown below**
  - **Simple setup**
  - **Easy to use**



Rx solution comparison

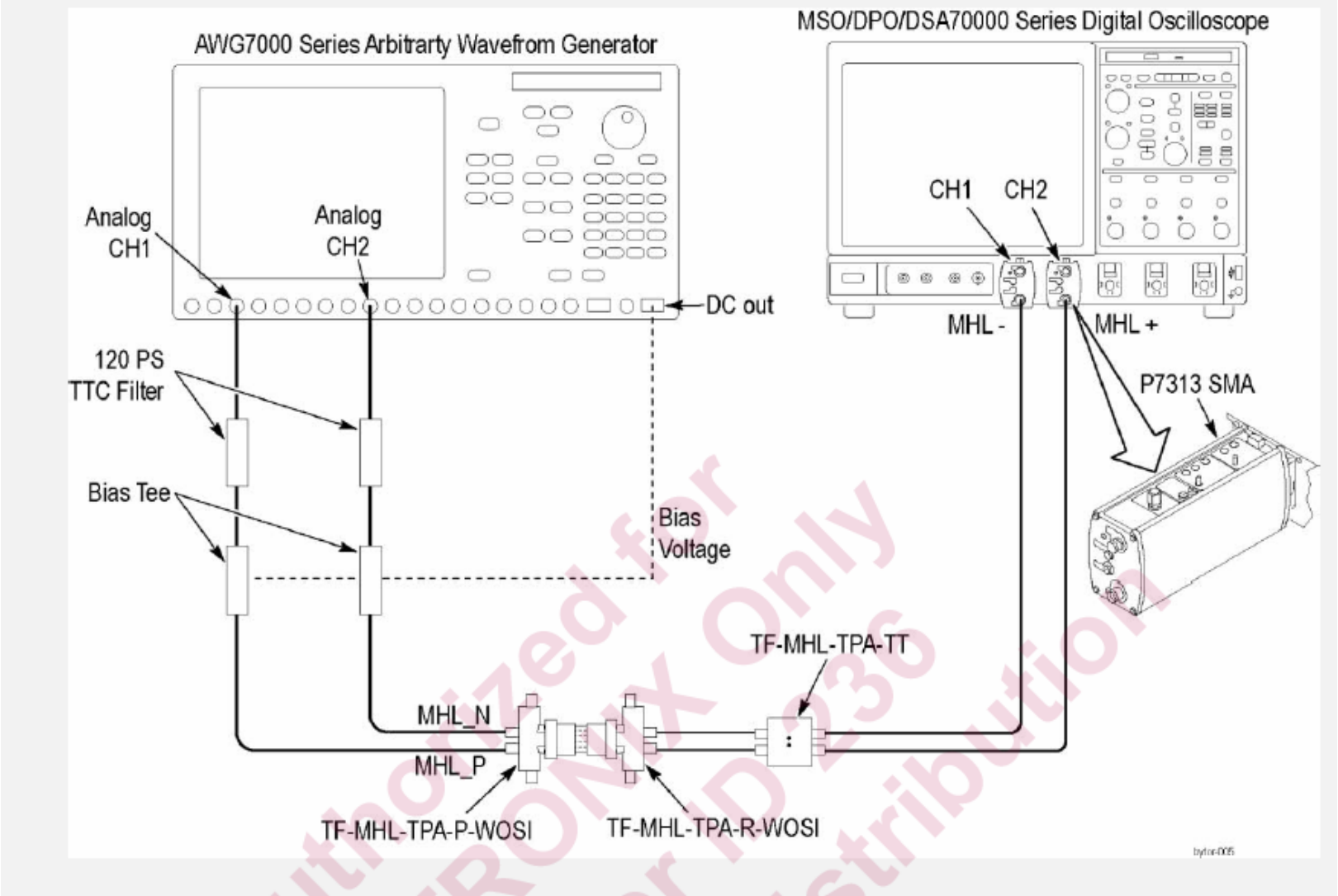
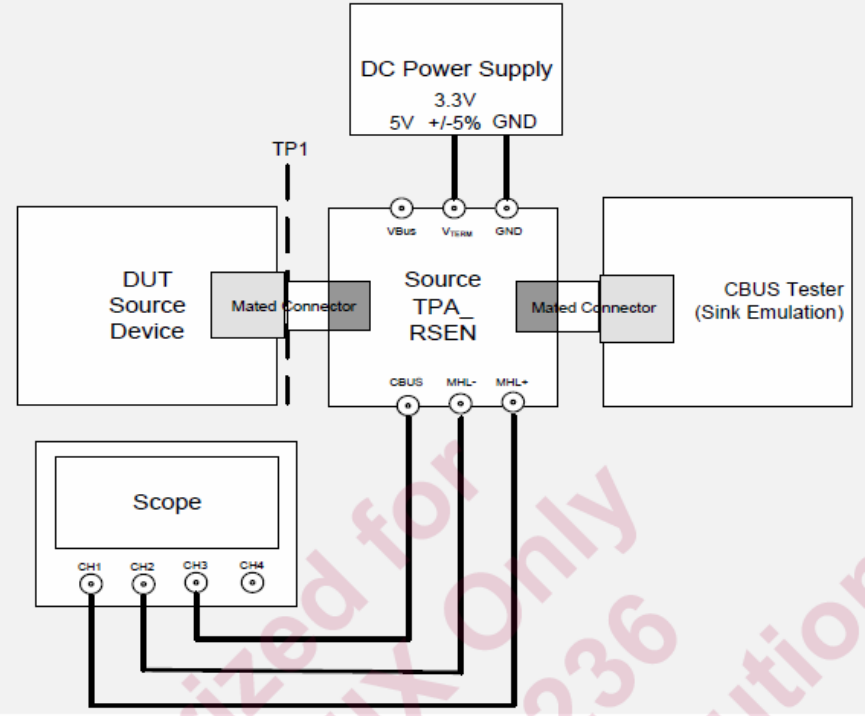


Figure 67. Single-Ended Signals Calibration Setup for Sink Tests – Tektronix Setup

MHL CBus tests (RxSEN)

- The CBus tester (Source emulation) provides CBus control for RxSense test of a Sink DUT or Dongle DUT.
- A CBus tester (Sink emulation) provides CBus control for RxSense of a Source DUT.
- Equipments
  - Low BW scopes DPO2024 / MSO2024 / MSO4054 with Opt DPO4EMBD
  - Passive probes P2221 / TPP500
  - Source meter – Kiethly 2400
  - Tek Power supply
  - Tek Digital Multi-meter



Innovative MHL Protocol Analyser Solution

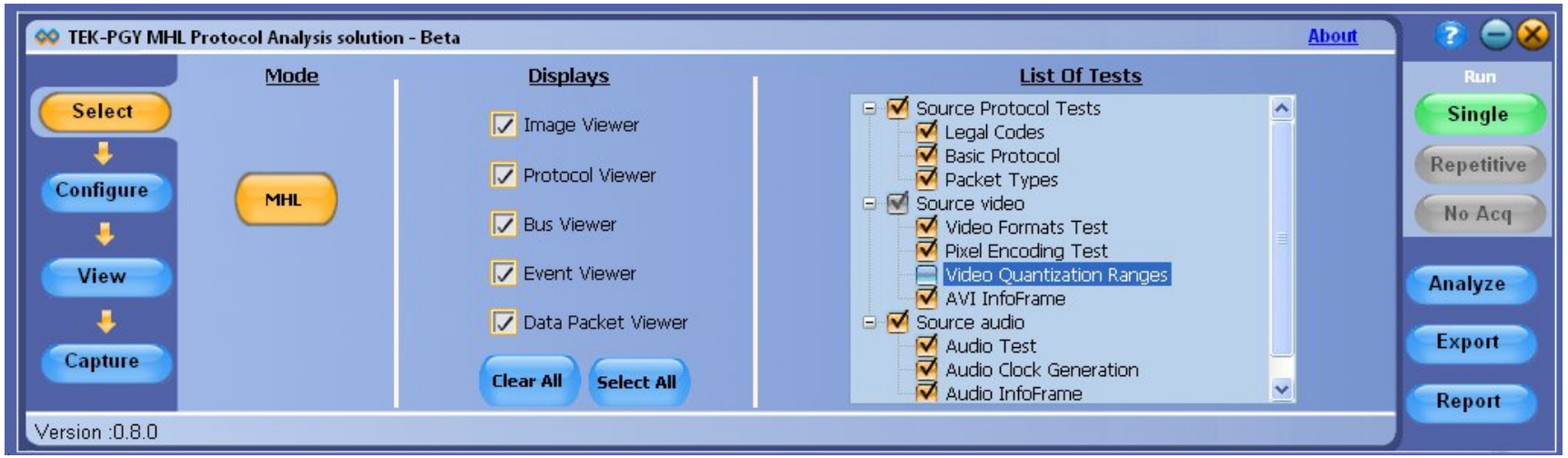
- Introducing Tektronix' MHL Protocol solution

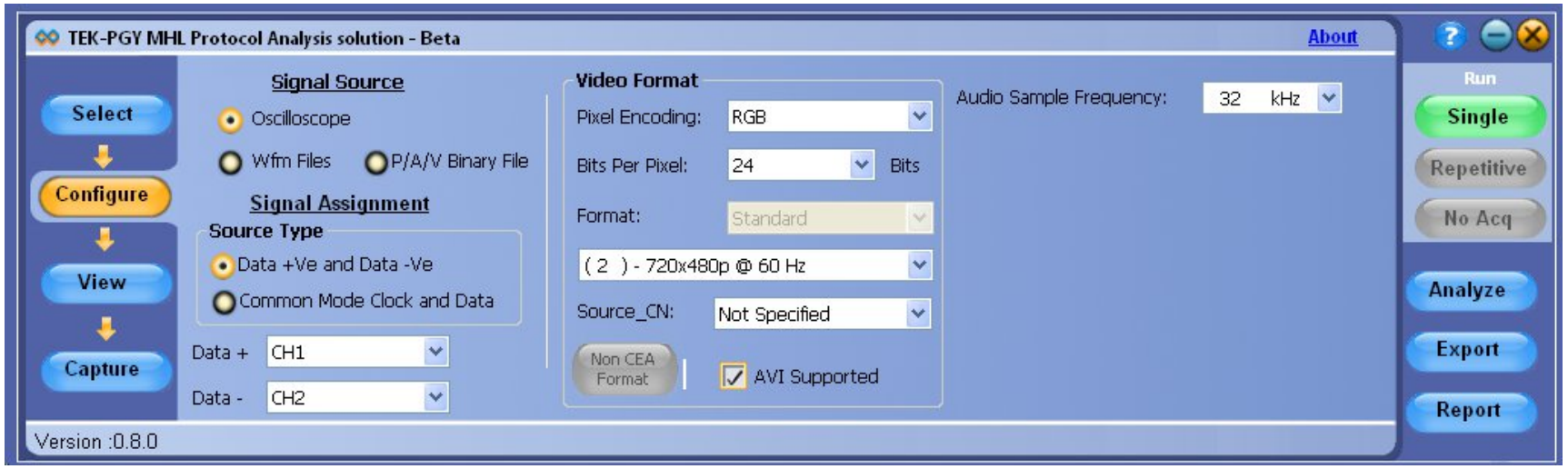
Tektronix®

Tektronix MHL Protocol Analysis Solution

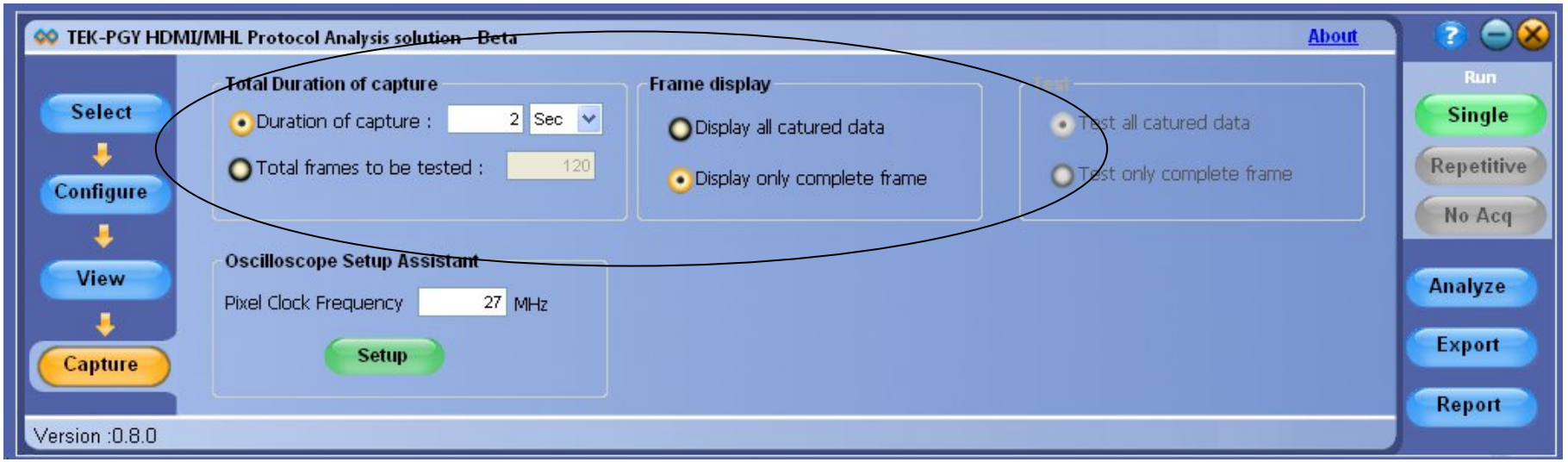
- MHL Protocol Analysis software running on the **Tektronix REAL TIME Oscilloscope**.
  - Unique value proposition as the same real time scope is used for both Physical layer testing and Protocol testing.
  - Gives the seamless transition from Phy layer to Protocol.
  - Cost effective solution.
- Features
  - Multi View support
    - Bus Analysis
    - Image Viewer
    - Event Viewer
    - Protocol Viewer
    - Linked to the analog waveform
- Tektronix Nomenclature – **TEK-PGY-MHL-PA-SW**

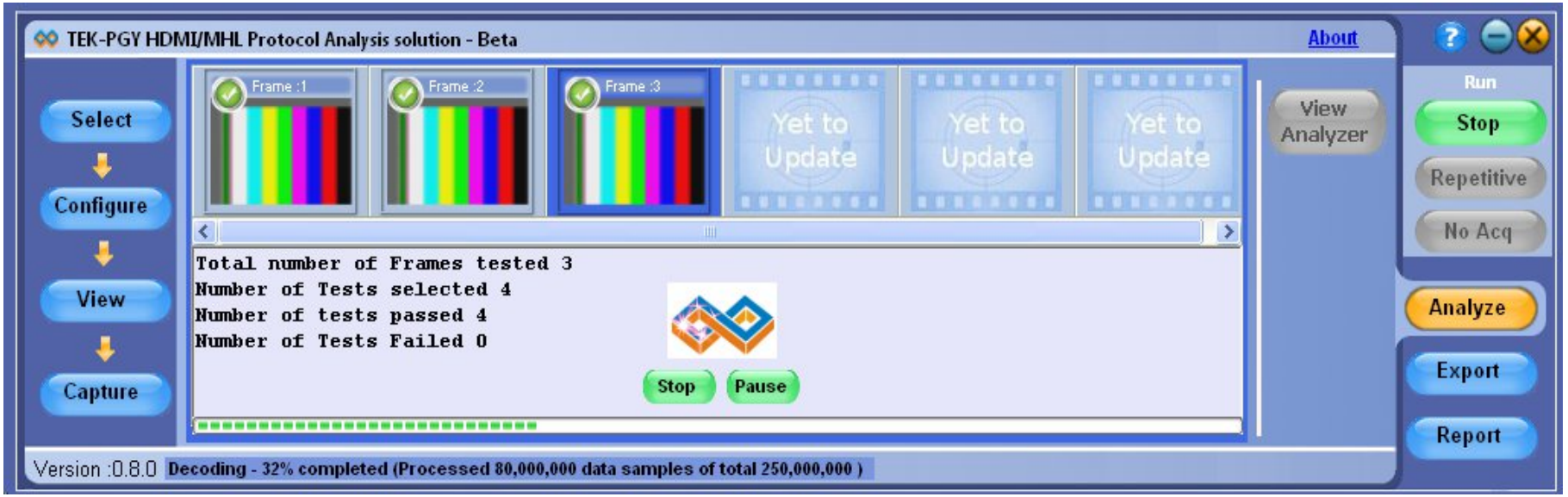
Tek MHL Protocol Analyser



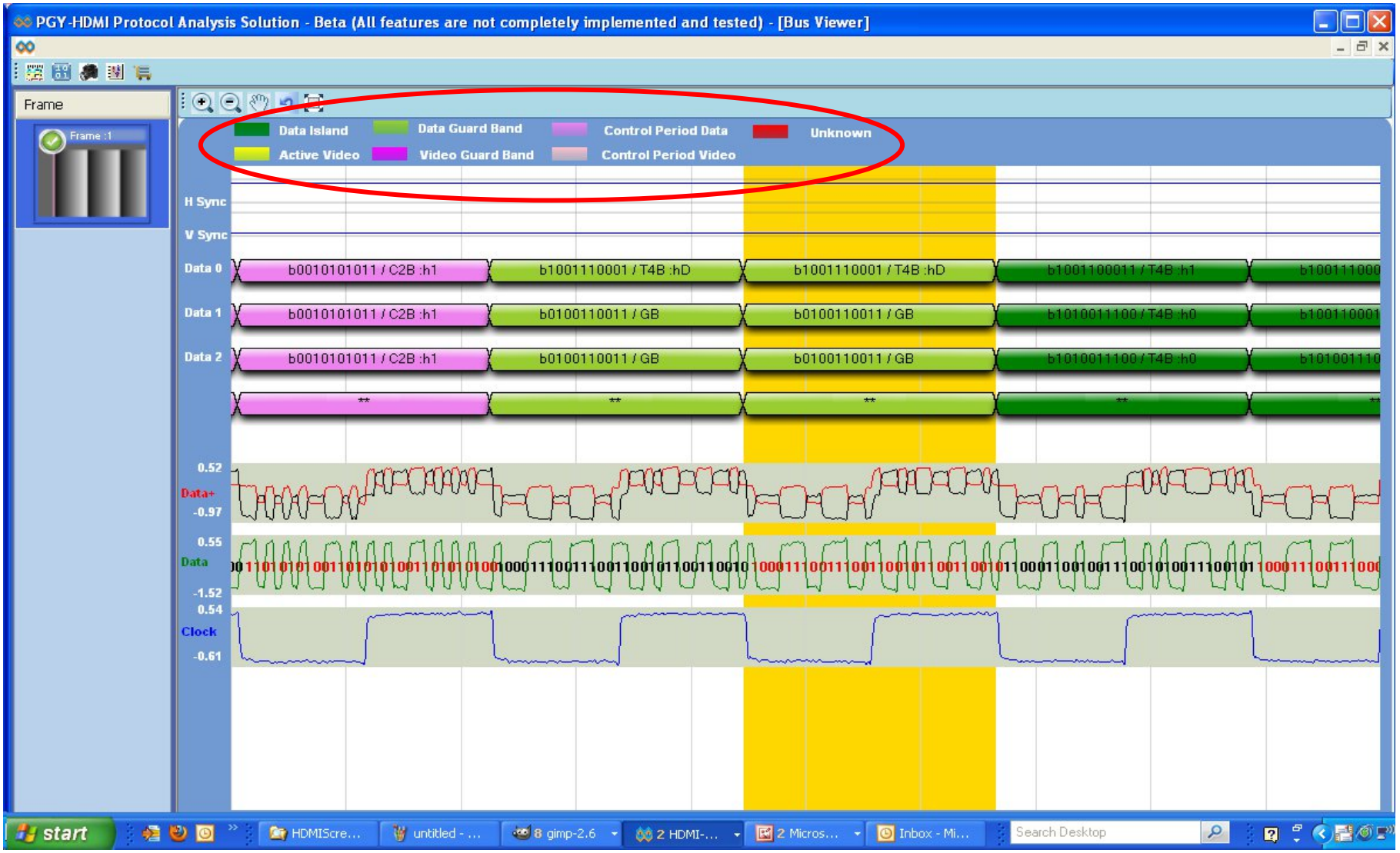


Tek MHL Protocol Analyzer



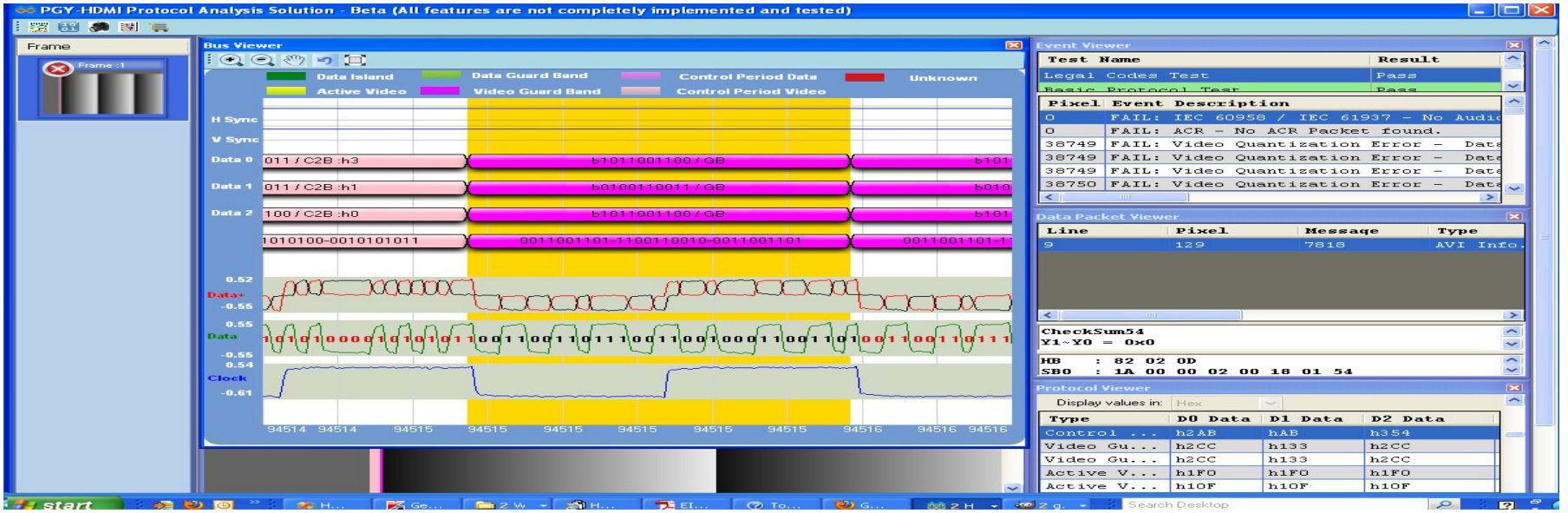


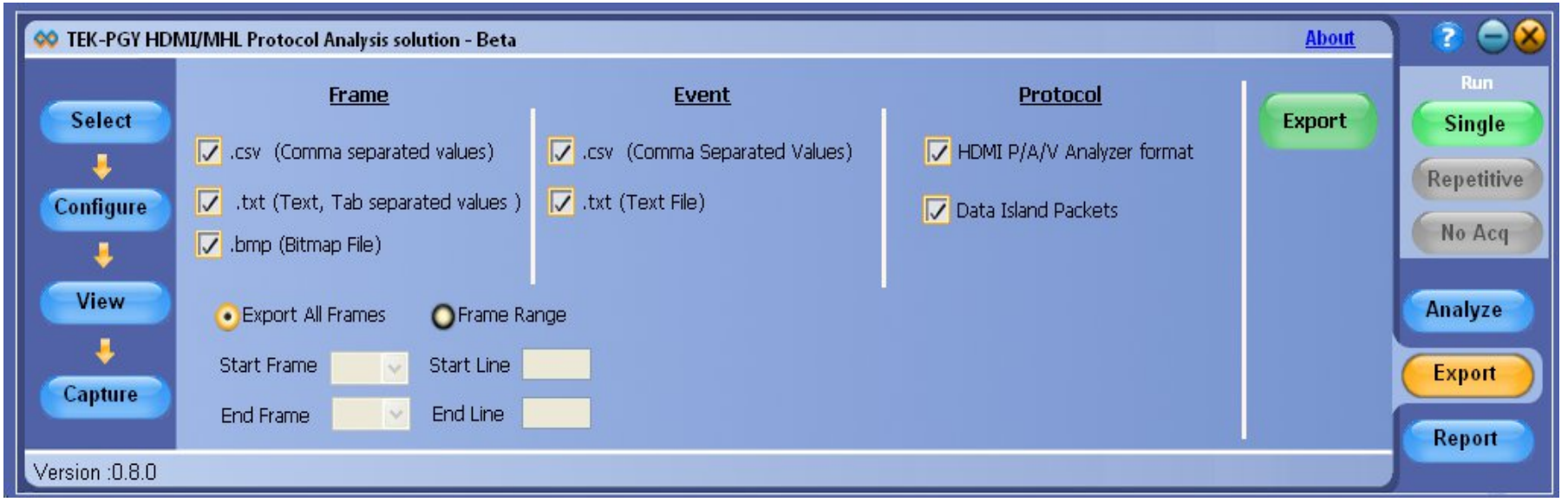
Tek MHL Protocol Analyser –Seamless PHY and Link layer testing



Tektronix®

Tek MHL Protocol Analyzer - Unique Multi View analysis





Tektronix®

MHL Compliance test analysis

All the tests's pass/ fail depends on one frame data or maximum of two continuous frame data at a time. So with multiple acquisition the protocol analyzer can produce the same result as 2 sec data as per CTS requirement.

- Source Protocol Tests
  - Legal codes
  - Basic Protocol
  - Packet Types
- Source Video Test
  - Required Video formats
  - Optional Video formats
  - Required Pixel Encoding
  - Optional Pixel Encoding
  - Video Quantization ranges
  - AVI Infoframe
- Source Audio
  - IEC 60958/IEC 61937
  - Audio Clock Regeneration
  - Audio InfoFrame

Comparison of MHL Protocol Analysis Solution

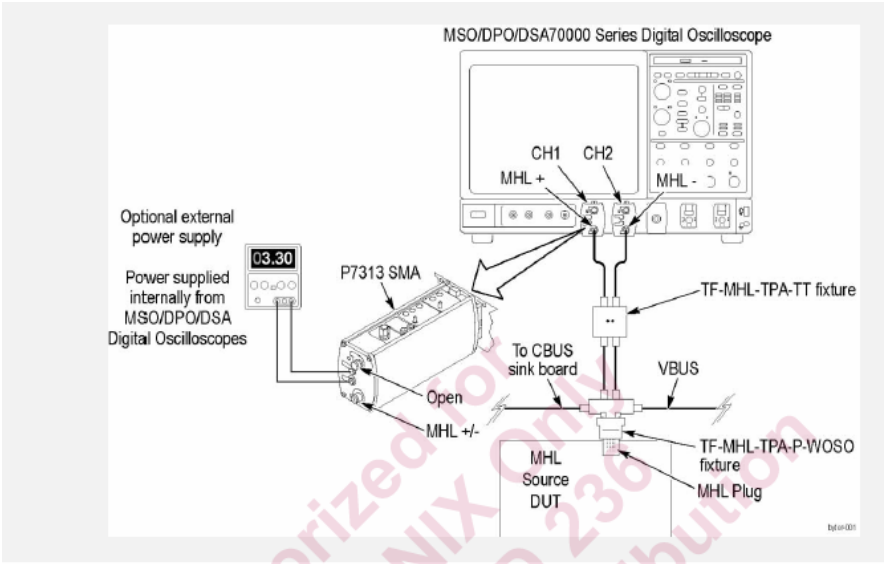


Figure 2. Recommended Tektronix MHL Protocol Analyzer and Adapter

Table 1. Tektronix Detailed Equipment List

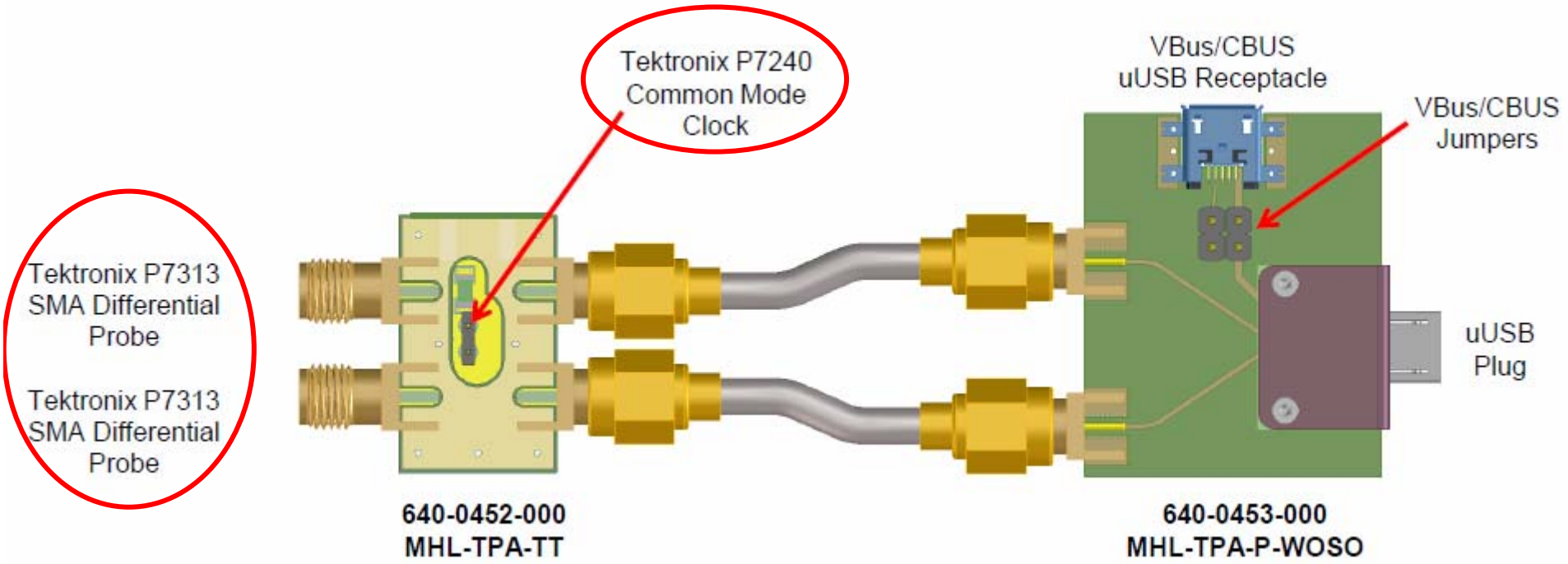
No.	Description	Recommended TE	Quantity
	Digital Real Time Scope	8GHZ , Digital Storage Oscilloscope DPO/DSA/MSO 70000/B/C series Real time Oscilloscopes with BW greater than or equal to 8GHz with Opt DJA,Opt10XL/20XL	1
	MHL Protocol Analyzer Software	MHL Protocol Analyzer Software TEK-PGY-MHL-PA-SW working on the recommended real time scope.	1
	Probes	P7313SMA	2
	Test Fixture	TF-MHL-TPA-P-WTSO micro USB Pluggable to be used for Source testing.	1
	Power Supply	PWS4205 or PWS2185	1

Tektronix®

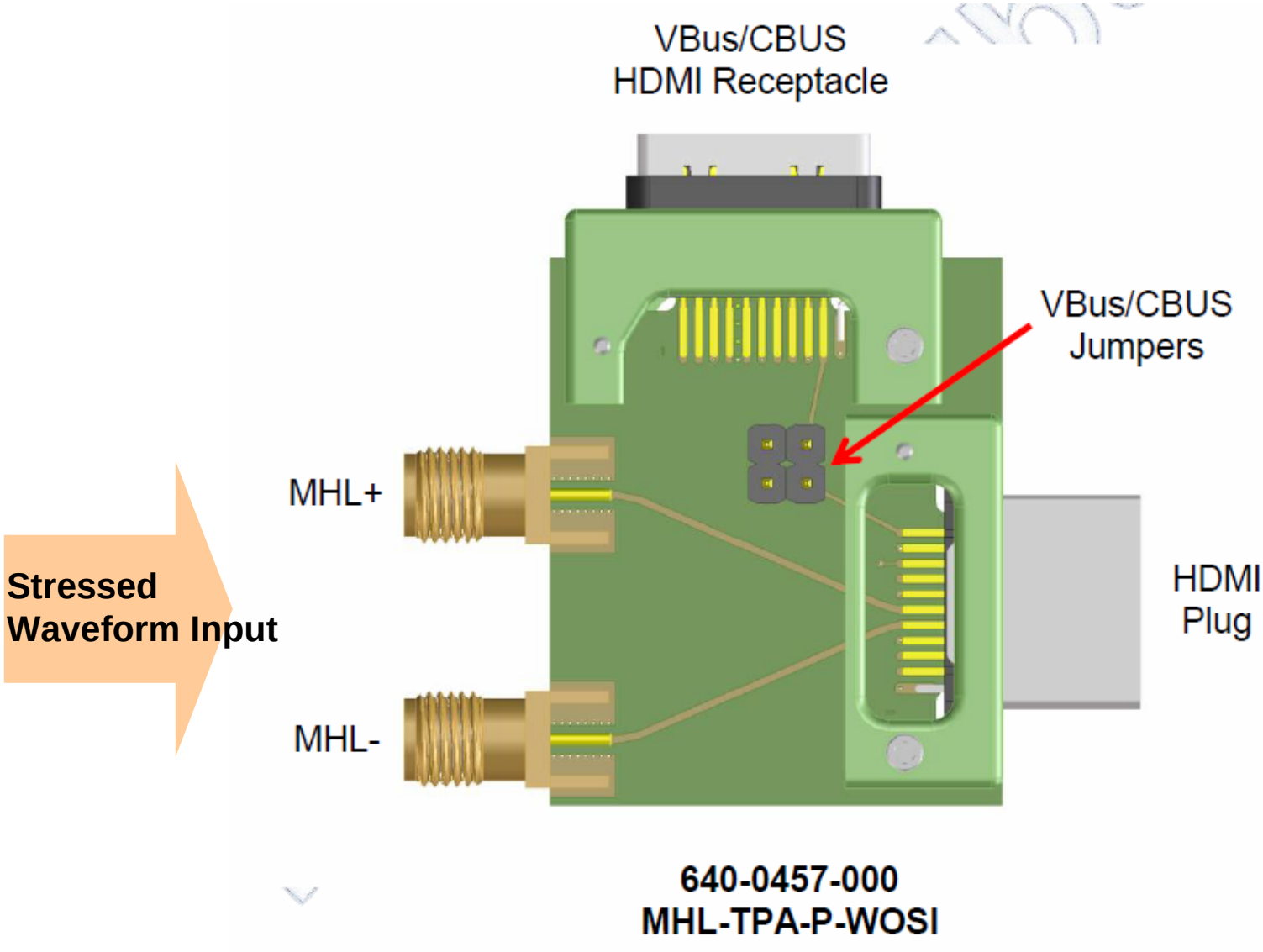
MHL Fixture

WT Part #	Test Fixture Configuration	MHL Testing
640-0452-000	Tektronix Source/Sink Termination	Source/Sink with Termination (two board)
WT Part #	**Test Fixture Configuration**	**MHL Testing**
640-0453-000	Micro USB Plug to SMA - Micro USB Receptacle (VBUS/CBUS)	Source with Termination - Dongle Cal
640-0454-000	Micro USB Receptacle to SMA - HDMI Receptacle (VBUS/CBUS)	Dongle Testing
640-0455-000	Micro USB Receptacle to SMA - SMA (VBUS/CBUS)	Cable Testing
640-0456-000	HDMI Receptacle to SMA - SMA (VBUS/CBUS)	Sink Cal - Cable Testing
640-0457-000	HDMI Plug to SMA - HDMI Receptacle (VBUS/CBUS)	Sink w/o Termination Testing
640-0458-000	HDMI Receptacle to uUSB Receptacle	Source Rx Sense
640-0459-000	HDMI Receptacle to uUSB Receptacle	Sink and Dongle Rx Sense

Wilder fixtures for Tektronix MHL Source Testing

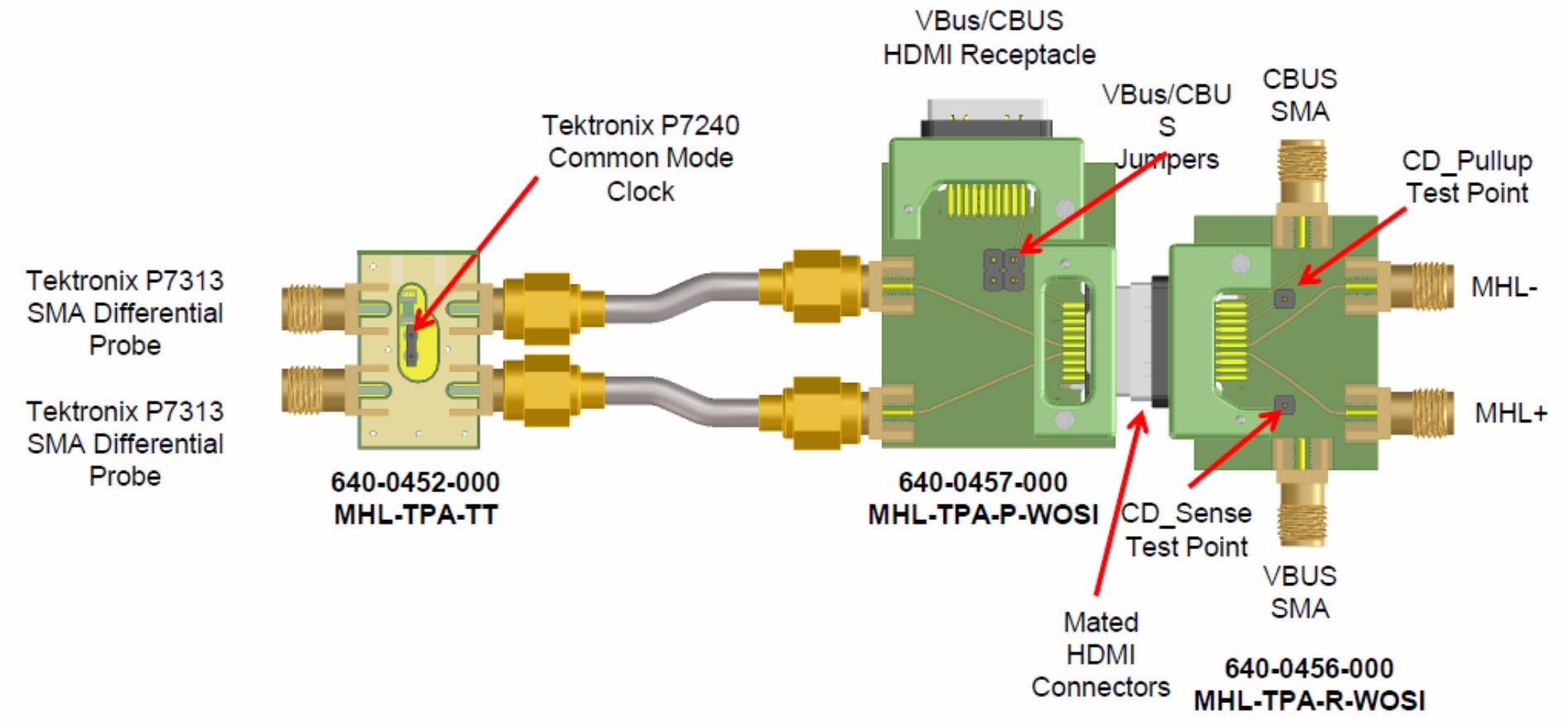


Wilder fixtures for Tektronix MHL Sink Testing



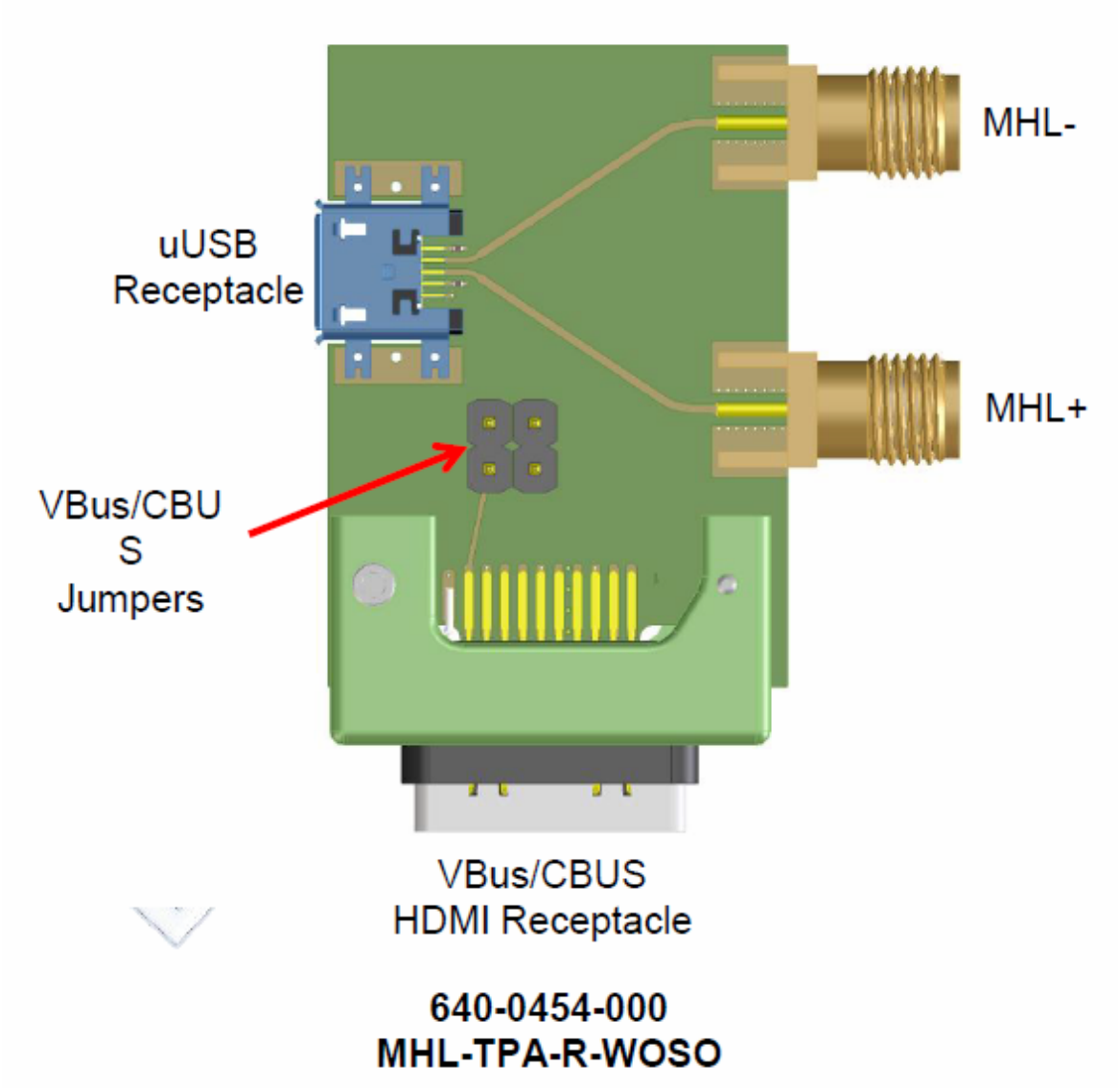
Tektronix®

Wilder fixtures for Tektronix MHL Sink signal verification



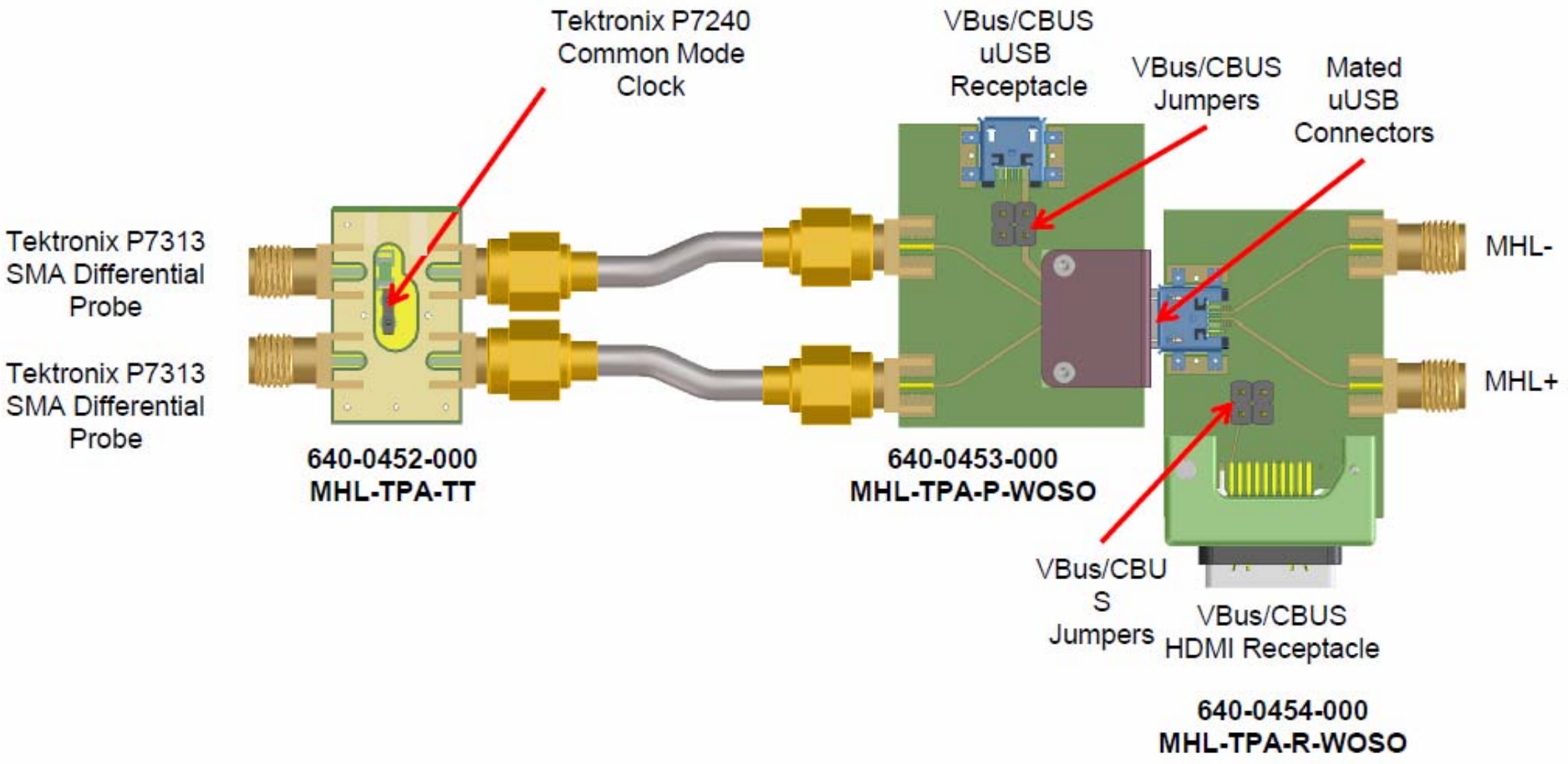
Tektronix®

Wilder fixtures for Tektronix MHL Dongle Testing



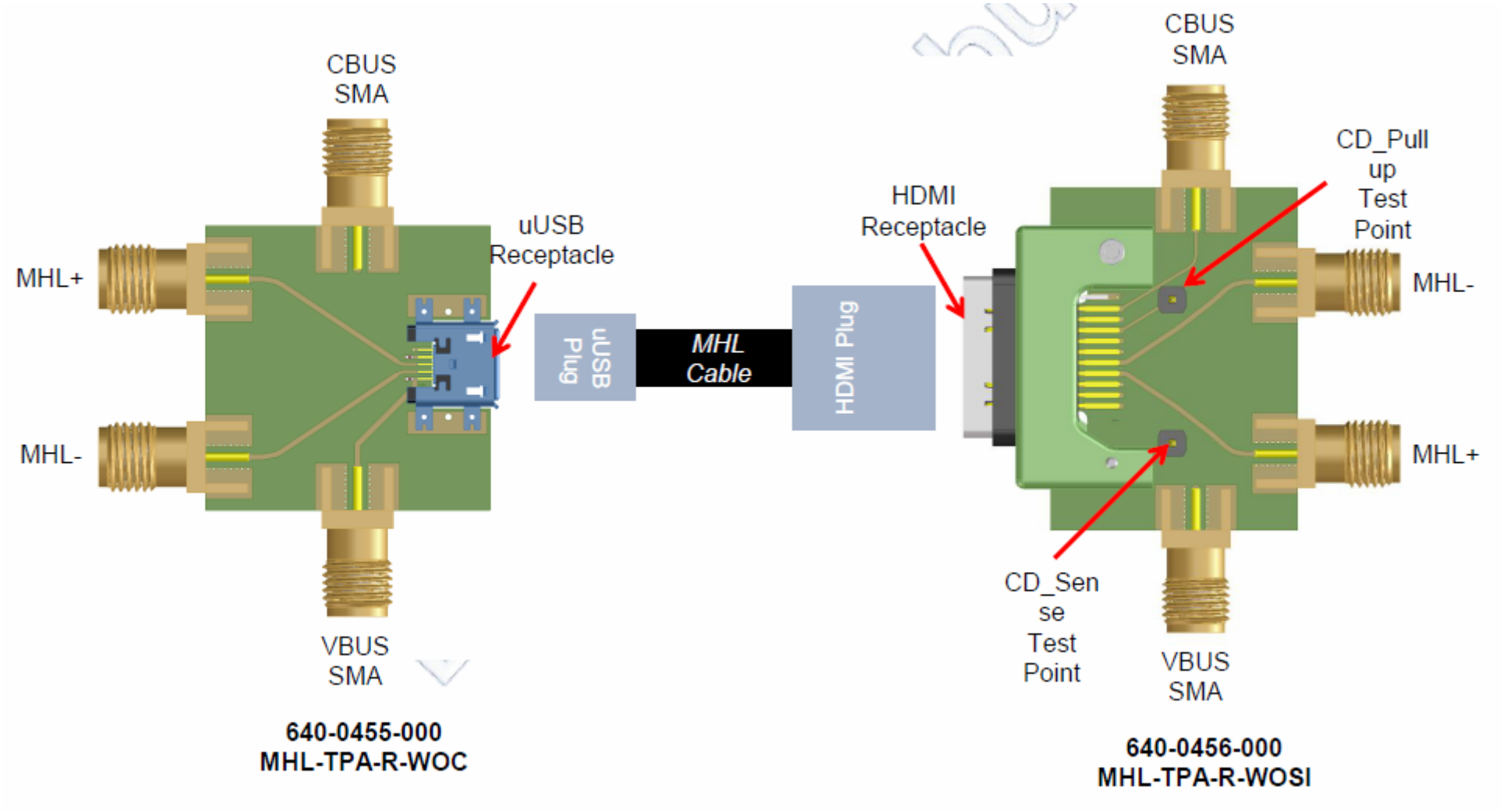
Tektronix®

Wilder fixtures for Tektronix MHL Dongle signal verification



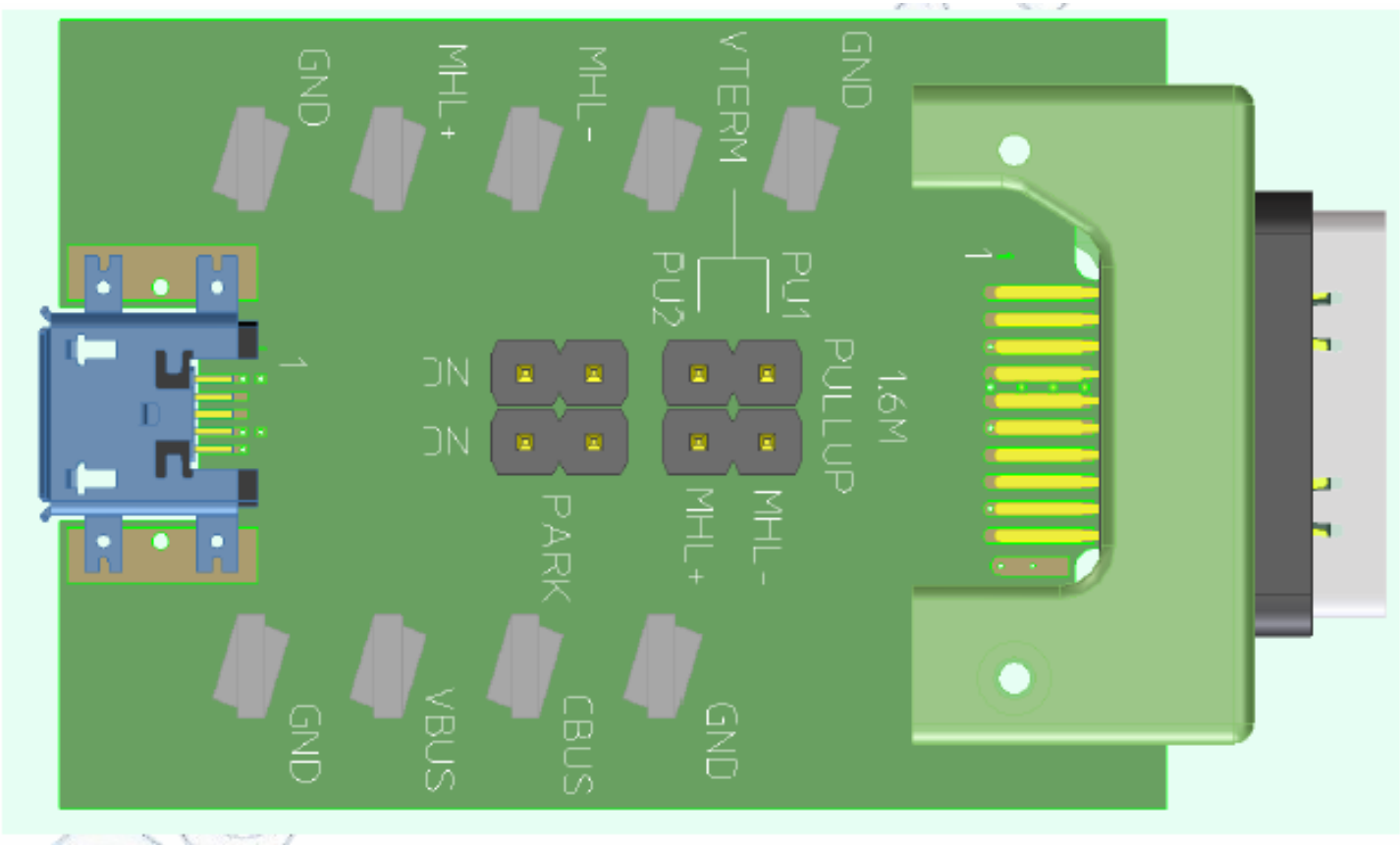
Tektronix®

Wilder fixtures for Tektronix MHL Source RxSEN Testing



Tektronix®

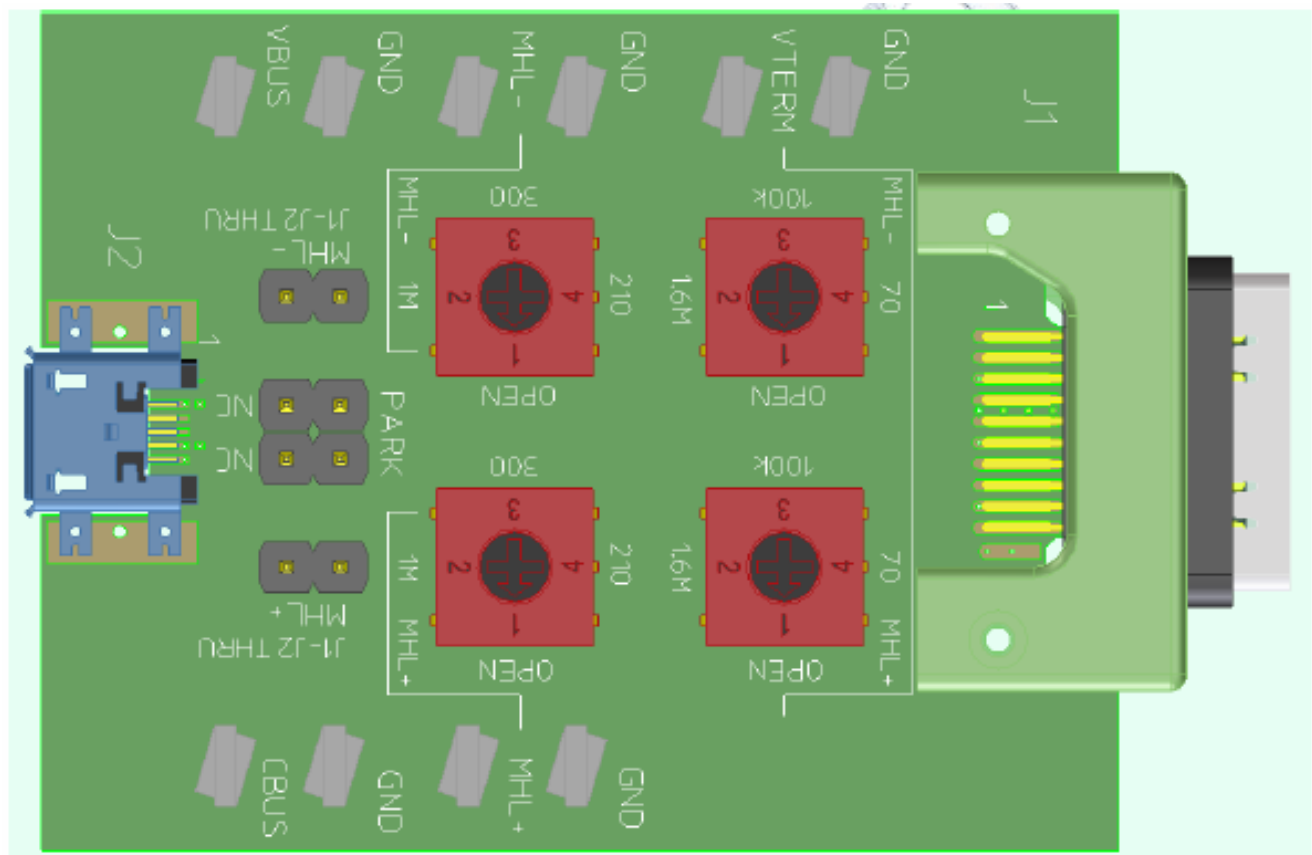
Wilder fixtures for Tektronix MHL Dongle Testing



640-0458-000
MHL-TPA-R-SO-RSEN

Tektronix®

Wilder fixtures for Tektronix MHL Sink and Dongle RxSEN Testing



640-0458-000
MHL-TPA-R-SI-RSEN

Conclusion

- **Tektronix MHL Physical Layer Tx test setups are easy to use and automated.**
  - **Simple test setups common for most tests.**
  - **Vterm provided by scope itself.**
  - **MHL fixtures are available from our fixture partner Wilder Technologies.**

- **Tektronix MHL Physical Layer Rx test setups are easy to use (MOI based).**
  - **TRUE MHL SIGNAL Generation as there is no need for external combiners/Filters**
  - **No need for external ISI boards as we leverage our AWG direct Synthesis Capability with common setups for Sink and Dongle testing**

- **Tektronix introduces an innovative combined solution for Physical Layer Testing and Protocol Testing:**
  1. **Providing seamless link between PHY and Link layer testing.**
  2. **An economical MHL test solution.**
     - **ONE BOX solution for PHY and Protocol testing.**
  3. **Easy access to legacy P/A/V data format.**

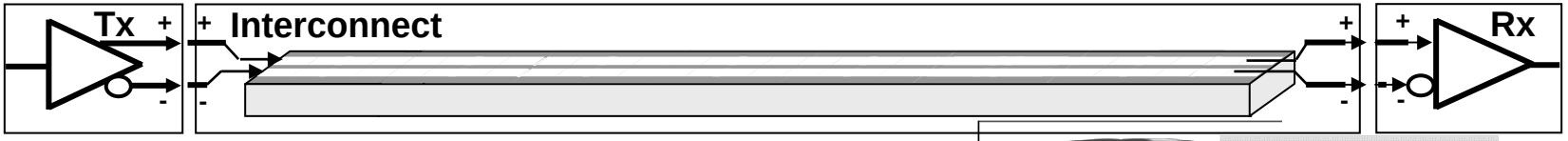
- **Tektronix also offers complete MHL solution with**
  - **DSA8200 or Equivalent Sampling scope with 80E03/04 and I-connector S/W for MHL Cable testing (performed manually using MOIs)**
  - **Low Bandwidth Oscilloscopes,**
  - **Keithley Source Meter (Now part of Tektronix)**
  - **Programmable Power Supply**
  - **Digital Multi-meters**

Complete MHL solution available from Tektronix aligned to CTS 1.1 announcement.

High-Speed Serial Data Test Solutions

Design → Verification → Compliance Test

PCI EXPRESS · SERIAL ATA · SUPERSPEED USB · ddr3 · IEEE · GbE · DisplayPort · HDMI · MHL …



Logic Analyzers

Real-time Scopes

System Integration
Digital Validation & Debug

Transmitter Testing

Receiver Test
Margin Testing

Arbitrary Waveform Generator

Probing Fixtures

Interconnect Test

Sampling Scopes

Compliance Test

Compliance Test Software

Tektronix®

THANK YOU

Tektronix®