Application Note

Complete Methodology for Signal Integrity Analysis of Gigabit Interconnects

As modern signaling standards push digital designs to the gigahertz and gigabit ranges, interconnect performance becomes the key factor in enabling reliable system operation. Signal integrity issues such as reflections, crosstalk, frequency dependent transmission line loss and dispersion can significantly degrade system performance and reliability. The ability to simulate and accurately predict the effect of these signal integrity issues is critical to achieving a working design, and this ability is contingent on the designer's ability to obtain accurate interconnect models for each part of the interconnect link - from the driver chip, through the package into the daughtercard; through a high-speed backplane connector to the backplane, and to the cable interconnect between subsystems.

Deterministic jitter and eye-diagram degradation are caused by frequency dependent losses and crosstalk in interconnects, and must be modeled using coupled and lossy transmission line models. Signal distortion and digital switching errors result from crosstalk, reflections and ringing in interconnects. Modeling the crosstalk requires coupled line-modeling techniques. Understanding reflection demands increased impedance measurement accuracy and transmission line modeling. Signal ringing requires understanding of interaction between the lumped (RLC) and distributed (transmission line) elements in the system.

Measurement-Based Modeling Methodology

The different pieces of the interconnect puzzle include backplane traces (single-run or differential, on a single layer or different board layers), vias, connectors and connector-cable assemblies, IC packages and sockets. Electrically short structures, such as vias, packages and connectors, can be modeled using a lumped (RLC) approach, whereas board traces and cables must be represented by distributed elements (transmission lines). For the backplane traces and cables that are long, we must include frequency dependent losses in the transmission line model in order to accurately predict propagation delay, jitter, and eye diagram degradation.

We can use a lumped model for the interconnect or interconnect segment if the interconnect propagation delay is much shorter than the rise time of the signal propagating through the interconnect:

$$t_{prop\ delay} << t_{rise\ time} \quad (1)$$

It is imperative that the designer defines the range of validity of the model through the rise time specification. This rise time is typically determined as the fast corner of the drivers to be used with a given signaling or I/O standard. A model that operates to a faster rise time than necessary will take much more time to extract and simulate without providing any benefits to the designer.

Once the accurate measurement-based model is extracted, it is important to validate the accuracy of the model by running simulations in the designer's simulator of choice and comparing them to the measurements.

The designer can analyze his or her interconnects, and extract the interconnect models using a number of pre-layout analysis and electromagnetic-field-solver tools. However, comparing the model with real measurements is paramount.

RLC Connector and Package Modeling

If the lumped model for a package or a connector is applicable, typically the JEDEC extraction method described in [1] and [2] is the easiest and most accurate modeling technique. This technique was originally developed for package characterization, but is equally applicable to connectors, sockets, and boards vias.

Impedance Profile Modeling of Backplanes and Cable Assemblies

Any impedance measurement errors caused by an effect known as "multiple reflections" can be corrected using an impedance-deconvolution algorithm [3]-[4]. The designer can also use the impedance-profile-modeling approach discussed in [4] to generate a Spice or IBIS signal-integrity model for the interconnect. The model generated using the impedance-profile approach based on TDR (time domain reflectometry) measurements has the advan-

Printed in the EE Times, December 8, 2003

tage of a one-to-one correlation to the physical geometry of the backplane or cable interconnects. Each transmission line corresponds to a backplane trace or a cable segment; each lumped element corresponds to a board via or a connector. Because all the modern standards are differential, all of this analysis must be performed in differential (4-port) mode, for example as described in [5].

Lossy Line Modeling Techniques

Frequency dependent transmission line losses need to be modeled for longer segments of backplane traces and cables. Skin effect and dielectric loss are the two key components of the transmission line losses, contributing to rise time degradation and amplitude degradation in the signal [6]. Rise time degradation can cause significant difference in delay between the driver and a receiver, and amplitude degradation can completely prevent the receiver from switching. Both of these effects, combined with the crosstalk-related pattern dependent jitter, may result in significant degradation of the eye diagram.

Even though a vector network analyzer (VNA) is the instrument that allows direct measurement of frequency dependent behavior of an interconnect, TDR measurements contain all the information about the frequency dependence of an interconnect, see Figure 1 below.

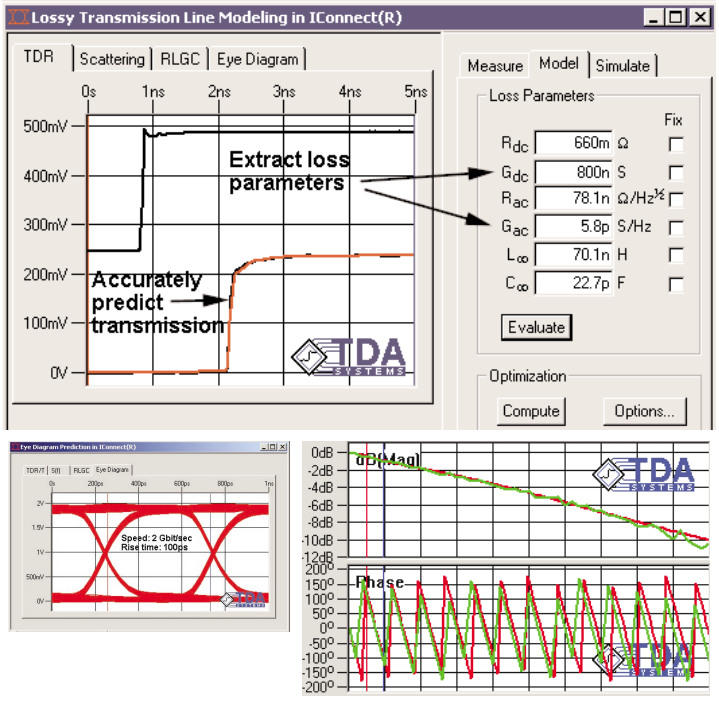

Figure 1. Lossy line modeling. Both time and frequency domain behavior of lossy lines must be modeled accurately

Modeling complex structures with frequency dependent response

Sometimes, it is difficult to distinguish losses from impedance variations when doing measurement based analysis. In cases like this, you may need to use a behavioral modeling algorithm. Such an algorithm does not discriminate between losses and reflections, but instead creates a complete model for an interconnect directly based on the corresponding TDR or VNA measurements, and this model will accurately predict both the time and frequency domain behavior of the interconnect.

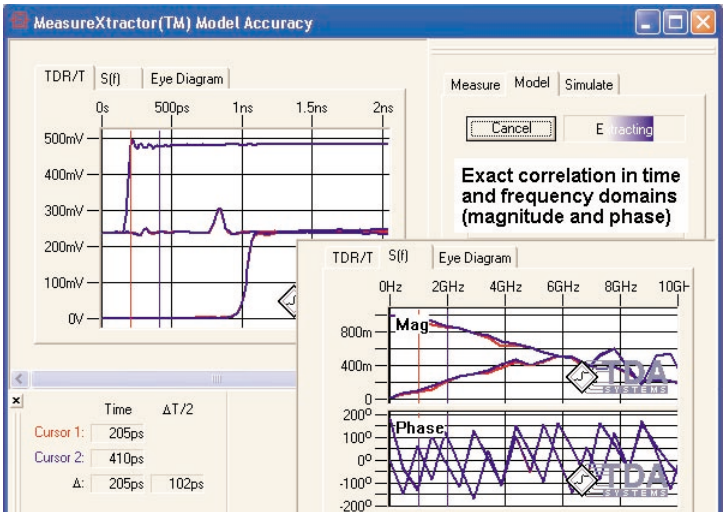

Figure 2. Behavioral modeling results in a model that matches the interconnect performance in time and frequency domain exactly

The advantage of behavioral algorithms is that they can generate a model fully automatically, and can even automatically select an appropriate topology for the model. However, this selected topology does not necessarily match the expected physical topology for the DUT. When using a behavioral model, one would not be able, for example, to separate the model for the connector out of the bigger backplane model. Therefore, behavioral models are great for generating a quick model for the interconnect when designer needs to include such model in the simulation, but they are not as useful when a designer is trying to find the causes of problems in his interconnect link.

Putting It All Together

Based on the techniques described above, it's possible to put together a complete methodology for modeling an interconnect link. The behavioral modeling algorithms can be applied when the designer needs to generate a quick model, or when a topological model is difficult to obtain. It's possible to combine lossy line modeling with impedance profile (Z-line) based modeling to generate an accurate topological model, and the JEDEC-based RLC modeling can be used to model isolated lumped element components in the link.

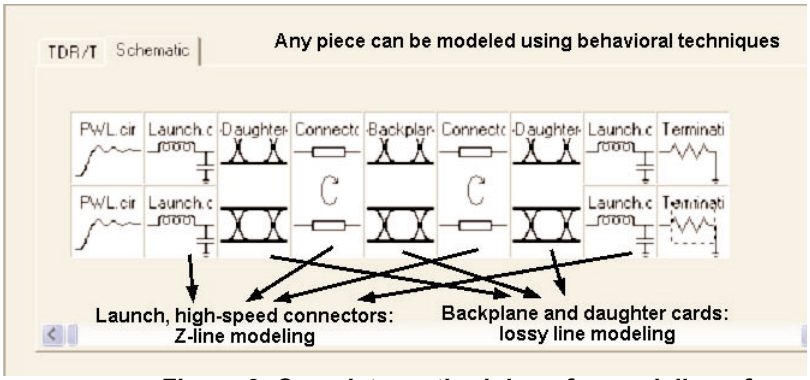

Figure 3. Complete methodology for modeling of the differential interconnect link

To demonstrate this methodology, we applied it to a Gigabit Ethernet backplane populated with two daughtercards. First, we extracted the lossy line model for the daughtercard. Second, we extracted the daughtercard-to-backplane connector model using the impedance profile. Then, we extracted the lossy line model for the backplane. The simulations using this model were performed in HSpice and Berkeley SPICE, and the resulting correlation is shown Figure 4.

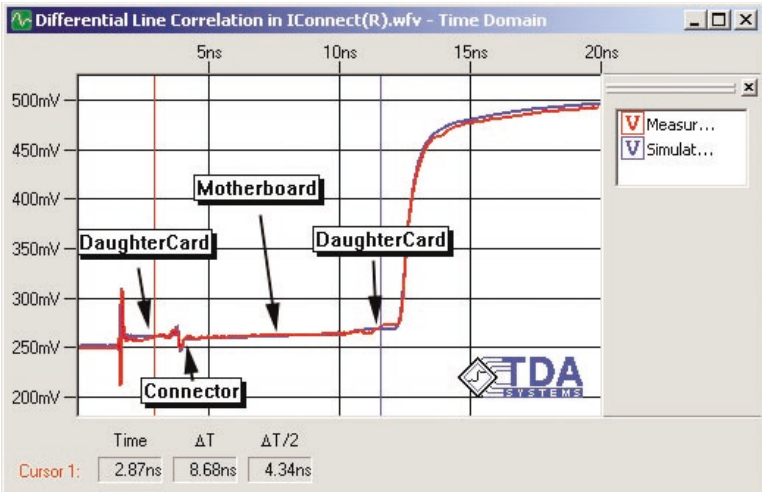

Figure 4. Correlation between Spice simulation and measurements in IConnect for a Gigabit Ethernet differential backplane assembly

The eye diagram can be predicted based on these modeling results, or directly predicted based on TDT measurements.

Summary

We presented a complete methodology for signal integrity analysis of the interconnect system running at gigabit speeds. With the TDR-based analysis techniques presented in this paper, the gigabit system designer can produce more accurate models for the gigabit interconnect, which will results in more reliable higher performance system design.

Bibliography

[1] Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters, - JEDEC Publication #123, JC-15 Committee, October 1995

[2] D.A. Smolyansky, "TDR Techniques for Characterization and Modeling of Electronic Packaging," - High Density Interconnect Magazine, March and April 2001, 2 parts (TDA Systems Application Note PKGM-0101)

[3] L.A. Hayden, V.K. Tripathi, "Characterization and modeling of multiple line interconnections from TDR measurements,"-IEEE Transactions on Microwave Theory and Techniques, Vol. 42, September 1994, pp.1737-1743

[4] D.A. Smolyansky, S.D. Corey, "PCB Interconnect Characterization from TDR Measurements" -Printed Circuit Design Magazine, May 1999 (TDA Systems Application Note PCBD-0699-02)

[5] D. A. Smolyansky, S. D. Corey, "Characterization of Differential Interconnects from Time Domain Reflectometry Measurements,"-Microwave Journal, Vol. 43, No. 3, pp. 68-80 (TDA Systems application note DIFF-1099)

[6] H.W.Johnson, M. Graham, "High-Speed Digital Design, A Handbook of Black Magic"-Prentice Hall, 1993

[7] E. Bogatin, S. Corey, M. Resso, "Practical Characterization, Analysis and Simulation of Lossy Lines," - DesignCon 2001, Santa Clara, CA, January 2001 (TDA Systems Application Note loss-0601)

[8] D. A. Smolyansky, "Simulation and Modeling of Lossy Transmission Lines," - Printed Circuit Design and Fabrication, March 2003 (TDA Systems Application Note siml-0203)

The Interconnect Analysis Company™

4000 Kruse Way Pl. #2-300, Lake Oswego, OR 97035 USA
Telephone: (503) 246-2272 Fax: (503) 246-2282
E-mail: info@tdasystems.com Web site: www.tdasystems.com

SIGI-1203

Data subject to
change without notice