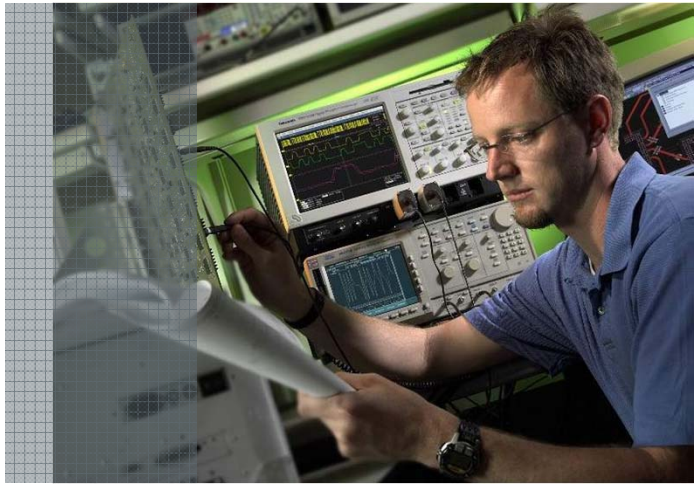
# Receiver Testing to Third Generation Standards

Jim Dunford, October 2011

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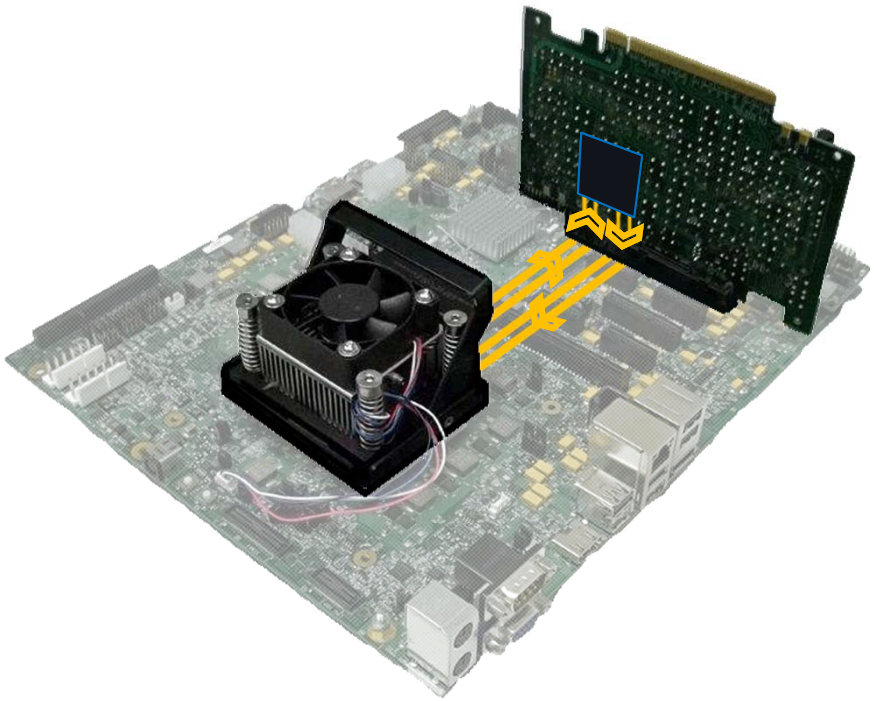
# Agenda

designinsight

# 1. Introduction

2. Stressed Eye
3. System Aspects
4. Beyond Compliance
5. Resources
6. Receiver Test Demonstration



*PCI Express is a trademark of PCI-Sig, www.pcisig.com*
*USB is a trademark of USB-IF, www.usb.org*



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# Introduction

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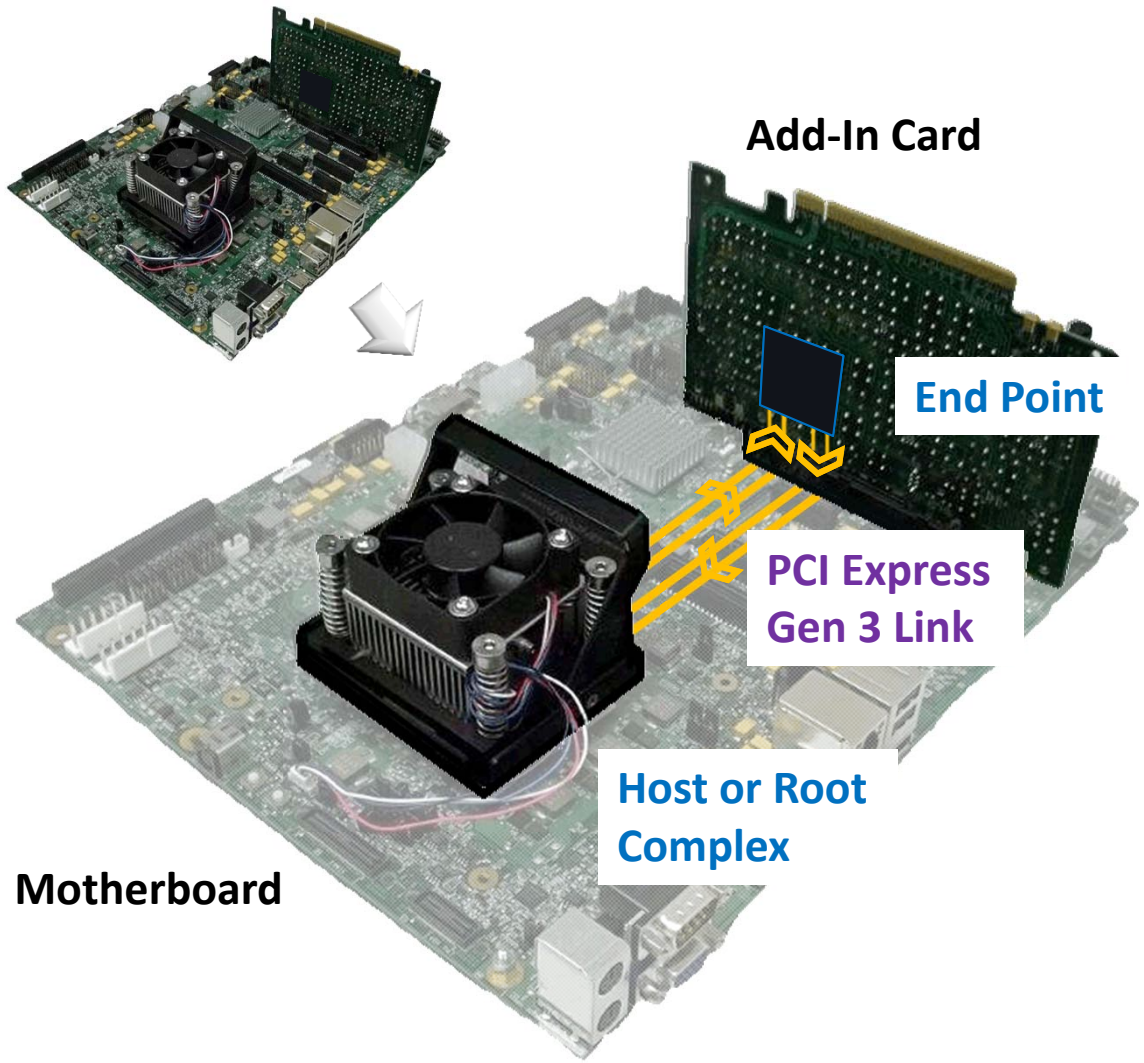


- Latest Generation Computer Standards have some **common trends**.
- We'll use **PCI Express Gen 3** as our main example
- We'll also use **USB 3.0**
- **Similar themes** are emerging in **other new standards** such as IEEE 100GbE etc.
- Conceptual example PCI Express link shown.



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# Introduction - Basics

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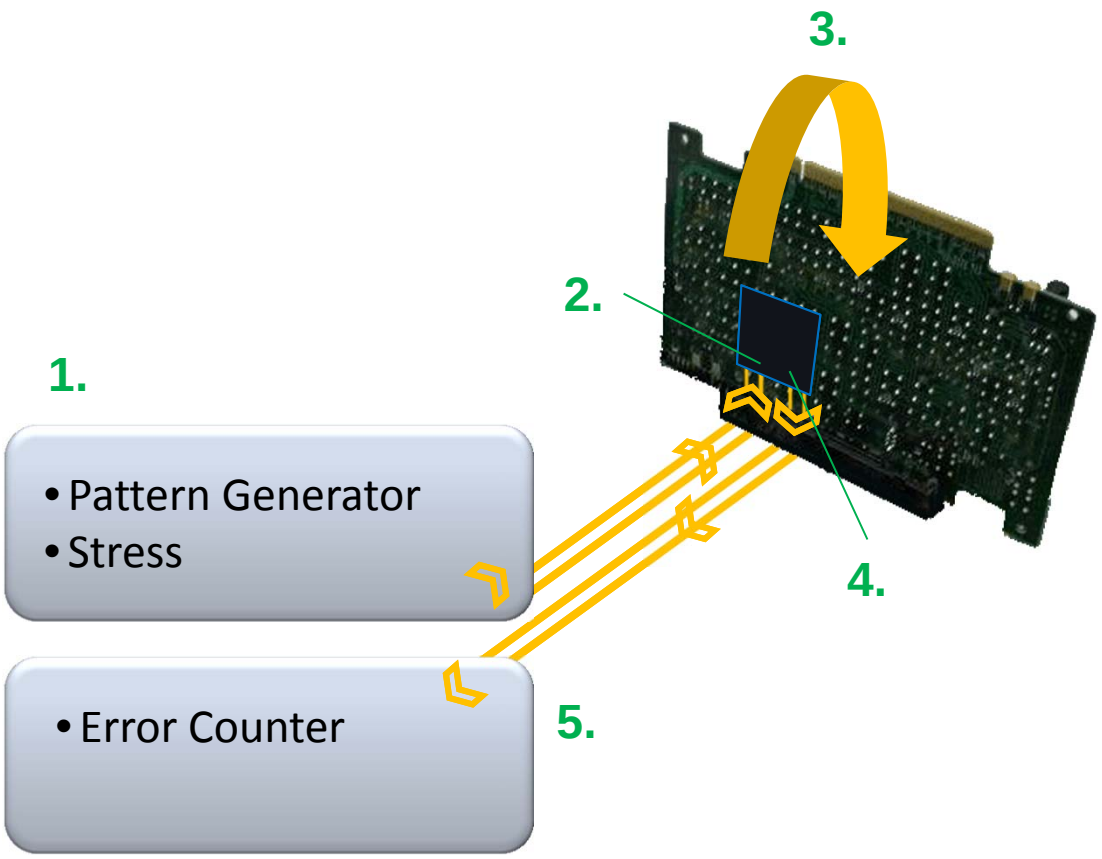


At the simplest level, receiver testing is composed of:

1. Send **impaired signal** to the receiver under test
2. The **receiver decides** whether the incoming bits are a one or a zero
3. The chip **loops back** the bit stream to the transmitter
4. The **transmitter sends out** exactly the bits it received
5. An **error counter** compares the bits to the expected signal and looks for mistakes (errors)



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# Introduction - Trends

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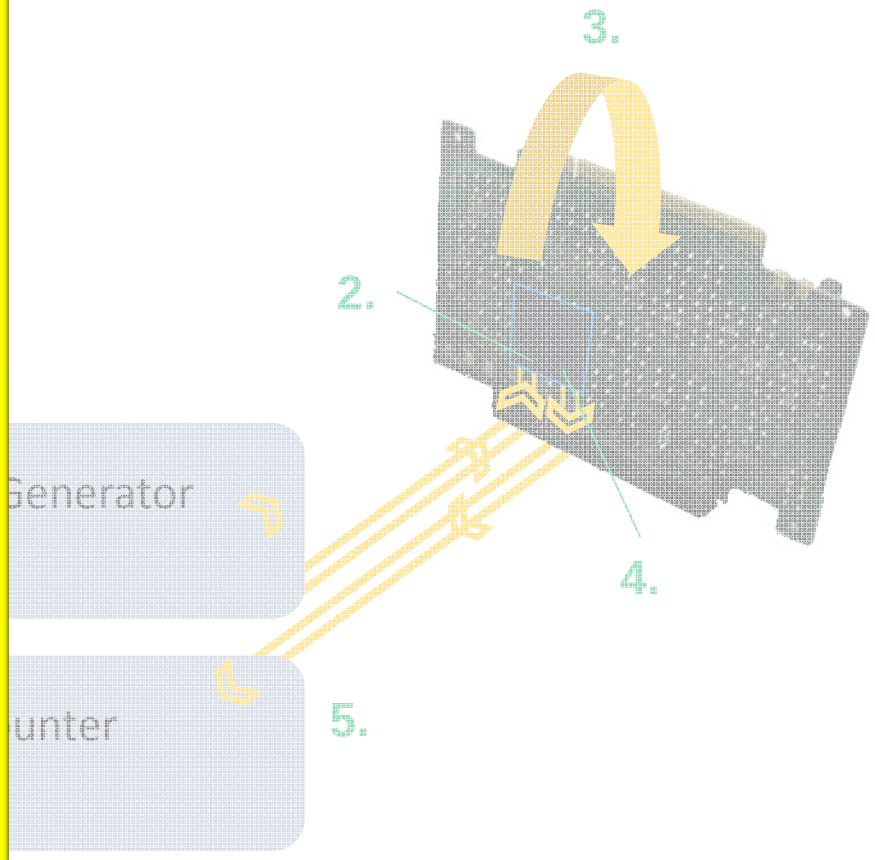
**Higher speeds** on **cheap** channel **materials** causing **closed eyes** from ISI and crosstalk

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# Introduction - Trends

designinsight

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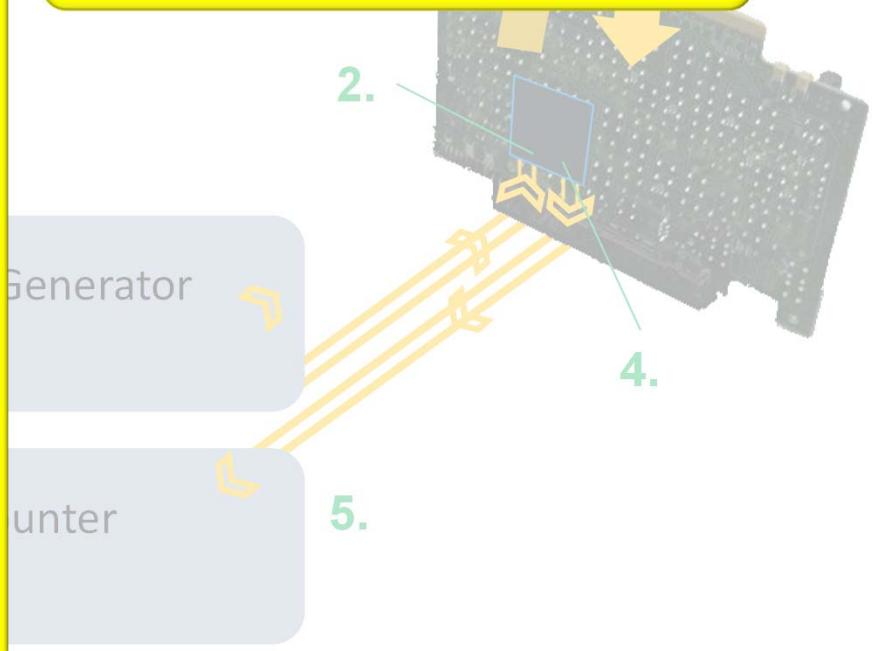
Test signal is changing:
- **Vertical eye closure**
- **Closed eye**

**Calibration** is difficult

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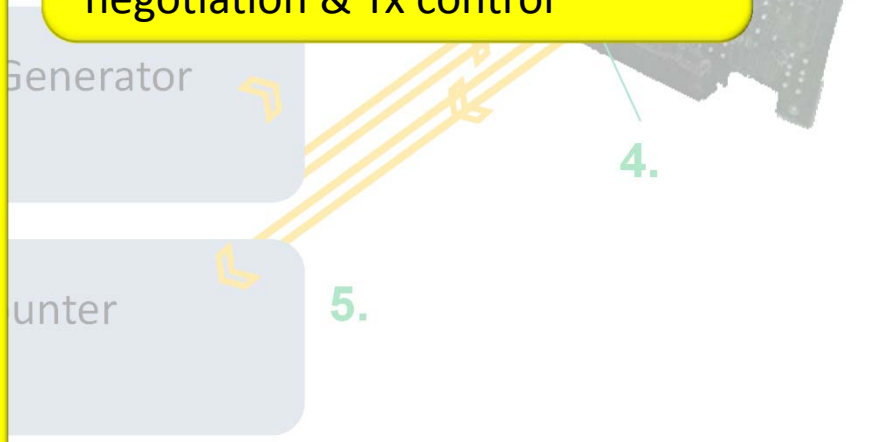


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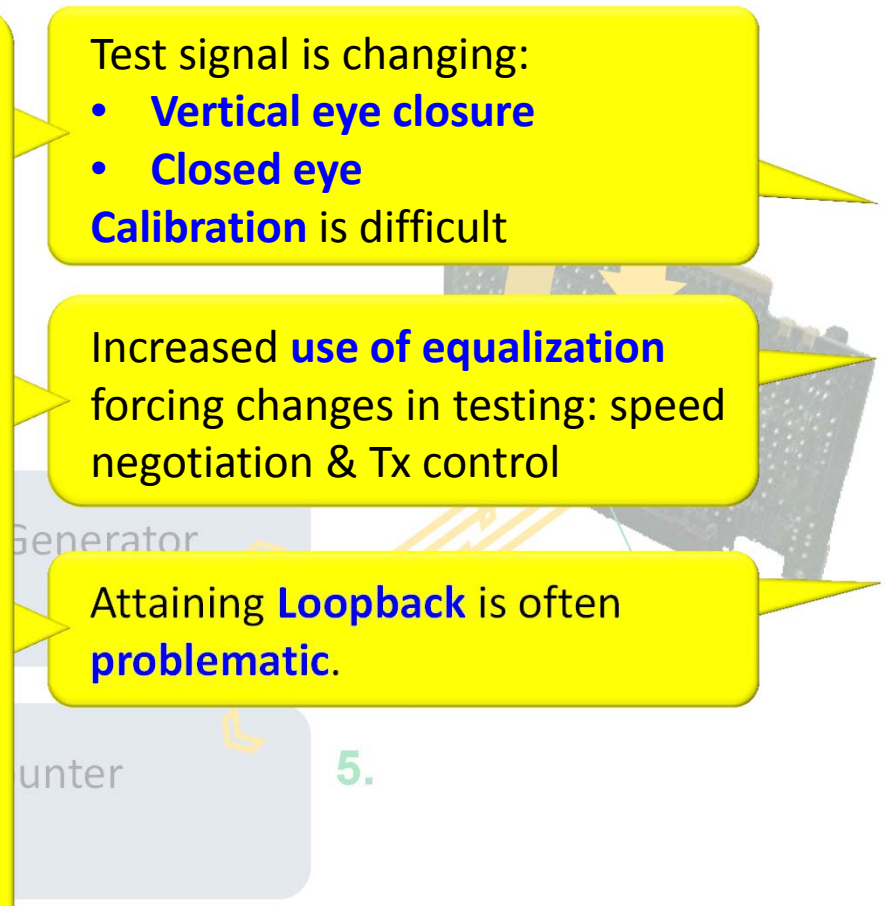


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**Calibration** is difficult

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Attaining **Loopback** is often **problematic**.

**Returned signal** is often also a **closed eye**, making error counting difficult

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# Agenda

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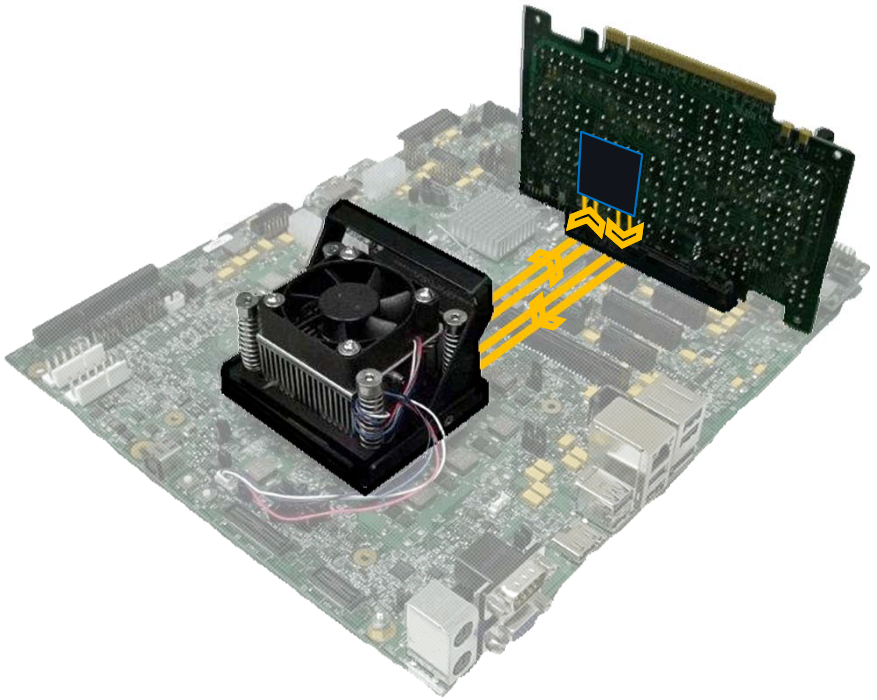
# 2. Stressed Eye

3. System Aspects
4. Beyond Compliance
5. Resources





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# Agenda

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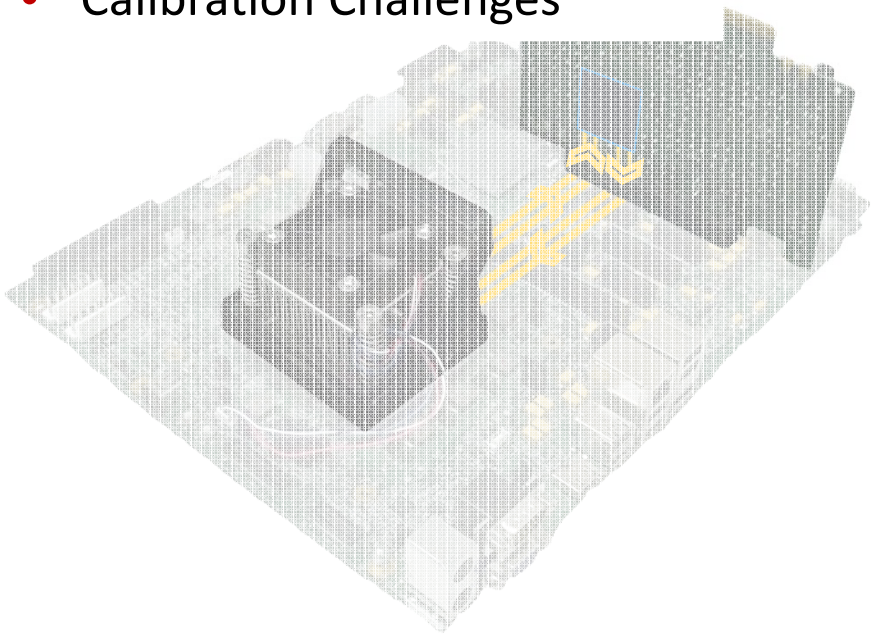
1. Introduction

## 2. Stressed Eye

- Changing Test Signal Recipes
- Channel Considerations
- Calibration Challenges



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4. Beyond Compliance
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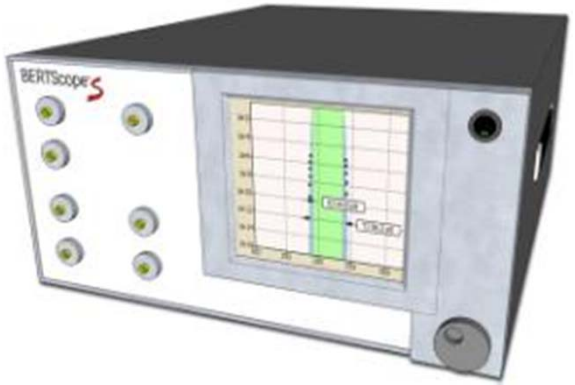
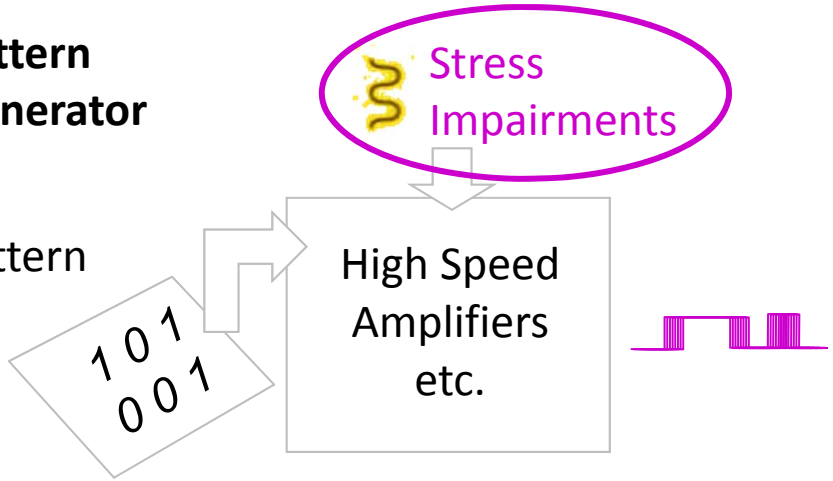
# Receiver Testing (a.k.a “Jitter Tolerance”) Review

designinsight

- Test receiver for **error free operation** (0 BER) while stressed **with input jitter/impairments**.
- **Calibrated jitter/stress** is added to Pattern Generator (PG), **output is increased** until receiver **experiences bit errors**, or test limit is reached.
- Test often repeated at another jitter frequency, results are plotted.



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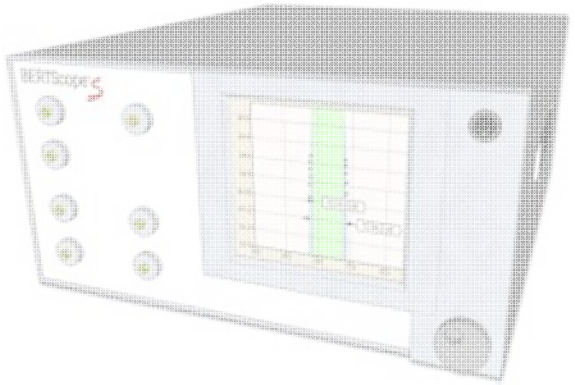

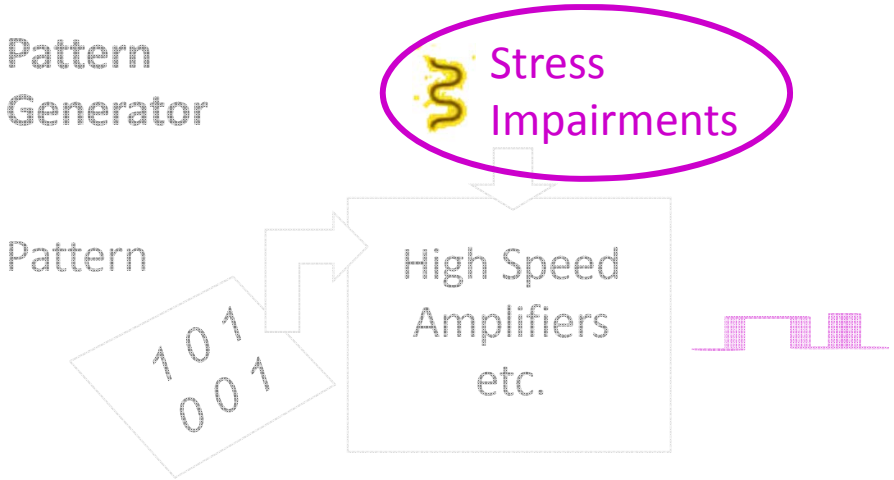


- **Stress recipe varies by standard**. In theory it emulates the system impairments for the expected use.
- ***Higher data rates mean closed eyes and crosstalk are bigger issues***.



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# Generic Stress Recipe

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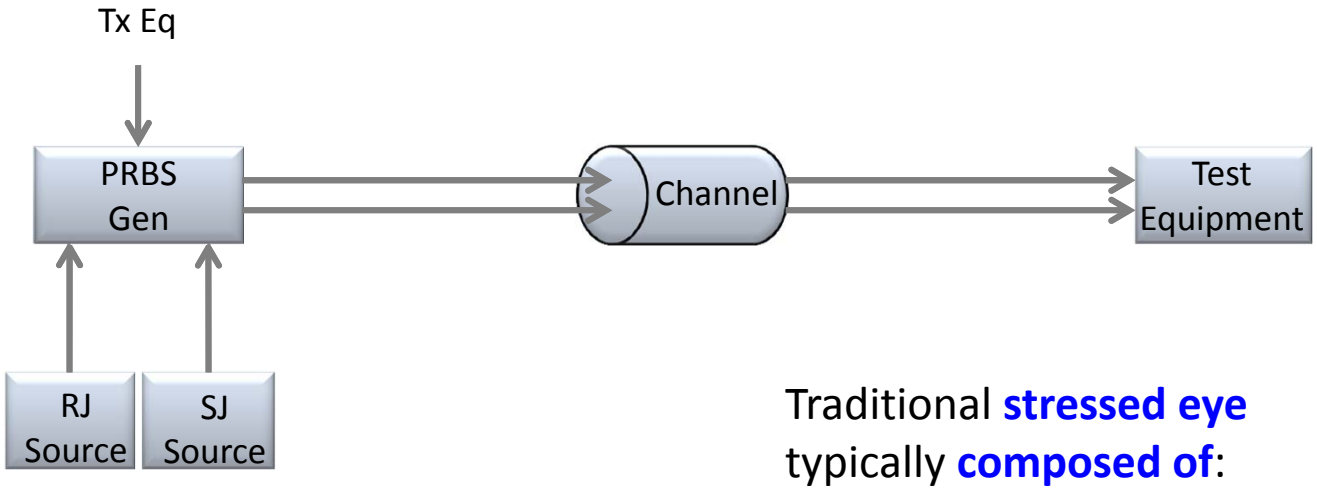


Traditional **stressed eye** typically **composed of**:

- PRBS **data signal**
- + **Pre-emphasis**
- + Jitter such as Random (**RJ**) and Sinusoidal (**SJ**)
- + Channel Inter-Symbol Interference (**ISI**)



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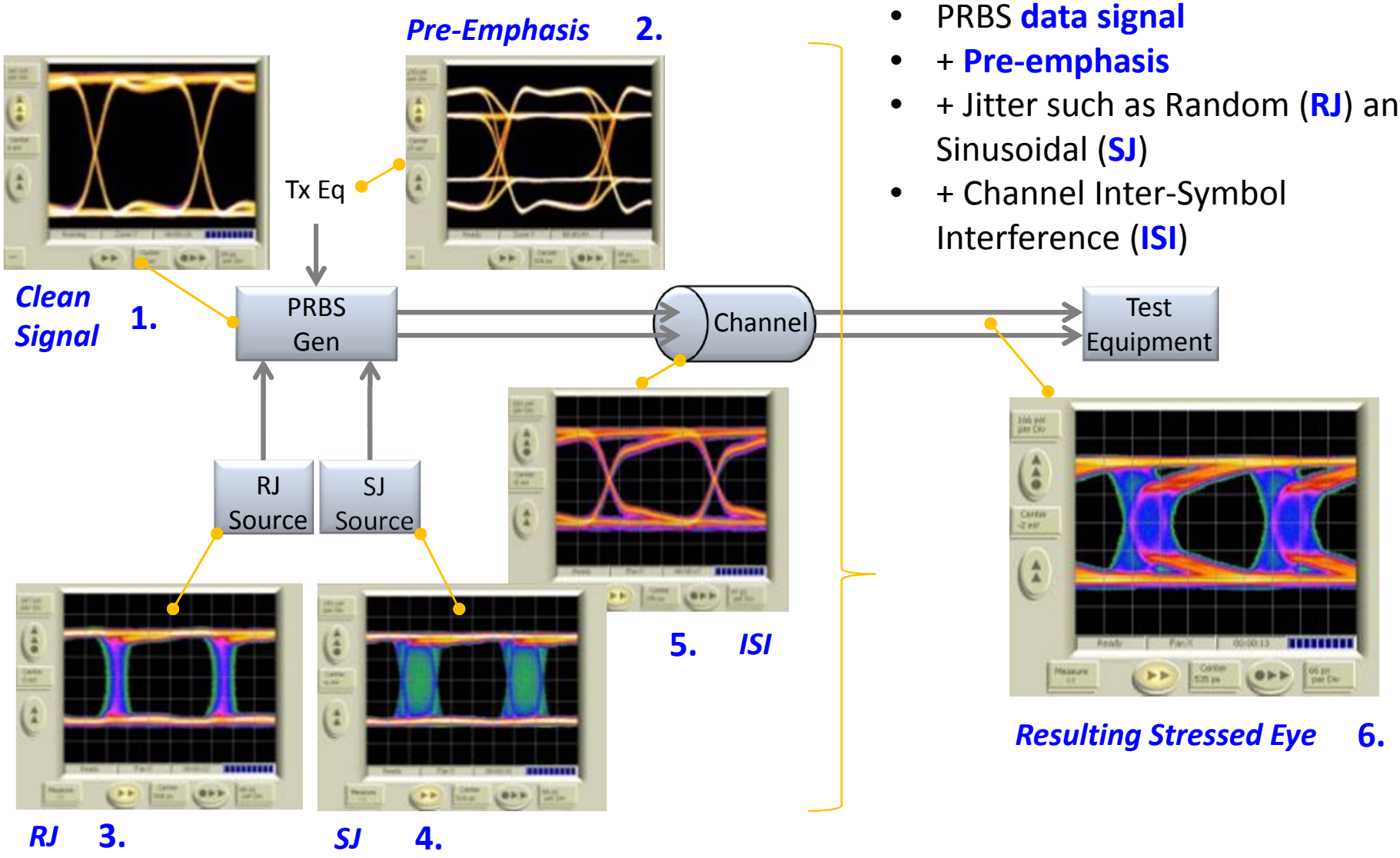
# Generic Stress Recipe

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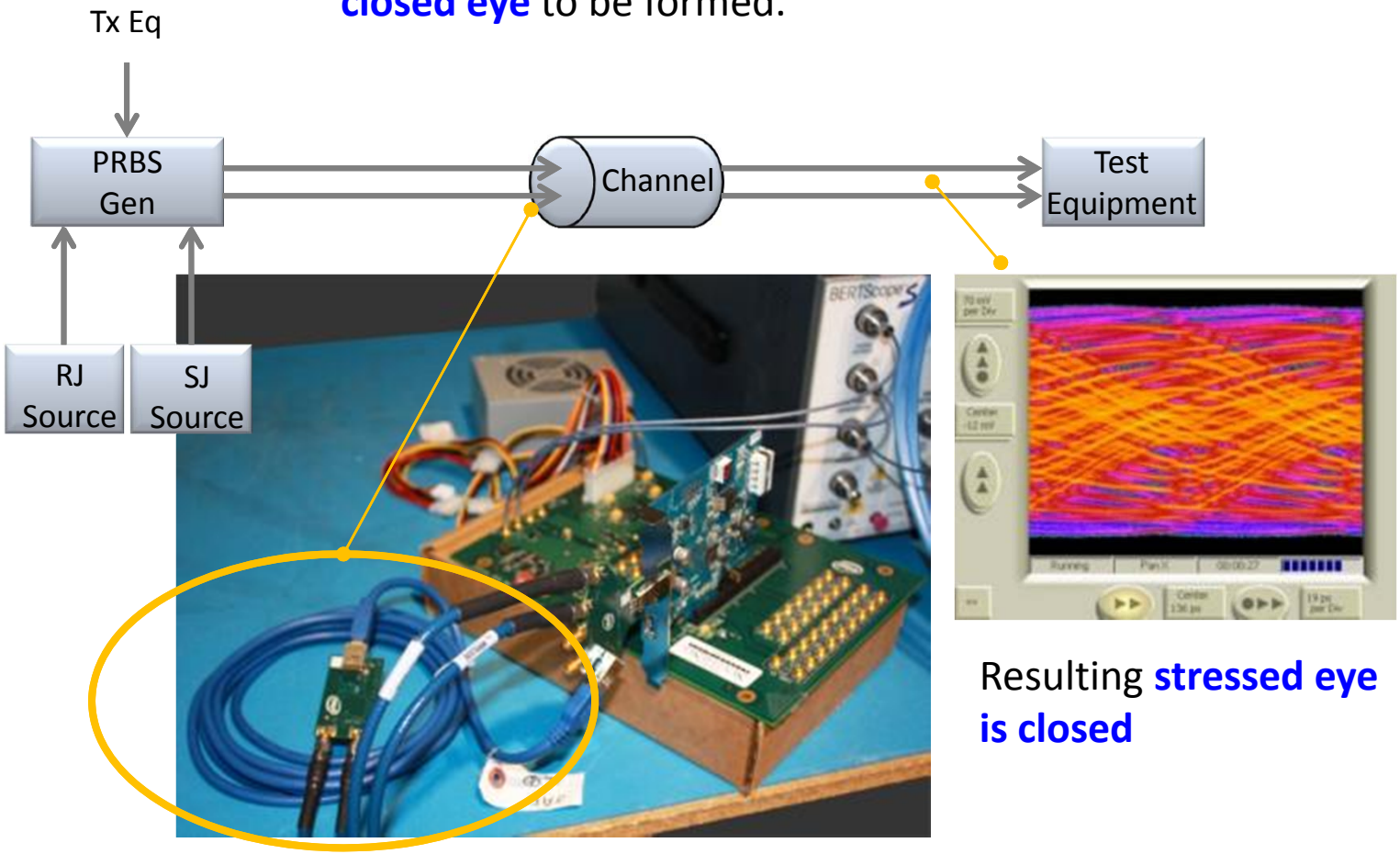
# USB 3.0 Stress Recipe

designinsight

| | |
|---|---|
| PCIe 3 | |
| USB 3 | ✓ |

USB 3.0 uses a representative **channel** – a **long USB cable**, which at 5Gb/s causes a **closed eye** to be formed.




Resulting **stressed eye is closed**



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# PCIe Gen 3 Stress Recipe - Overview

| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |

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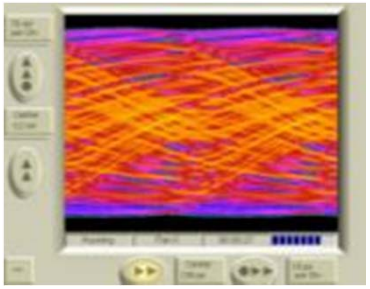
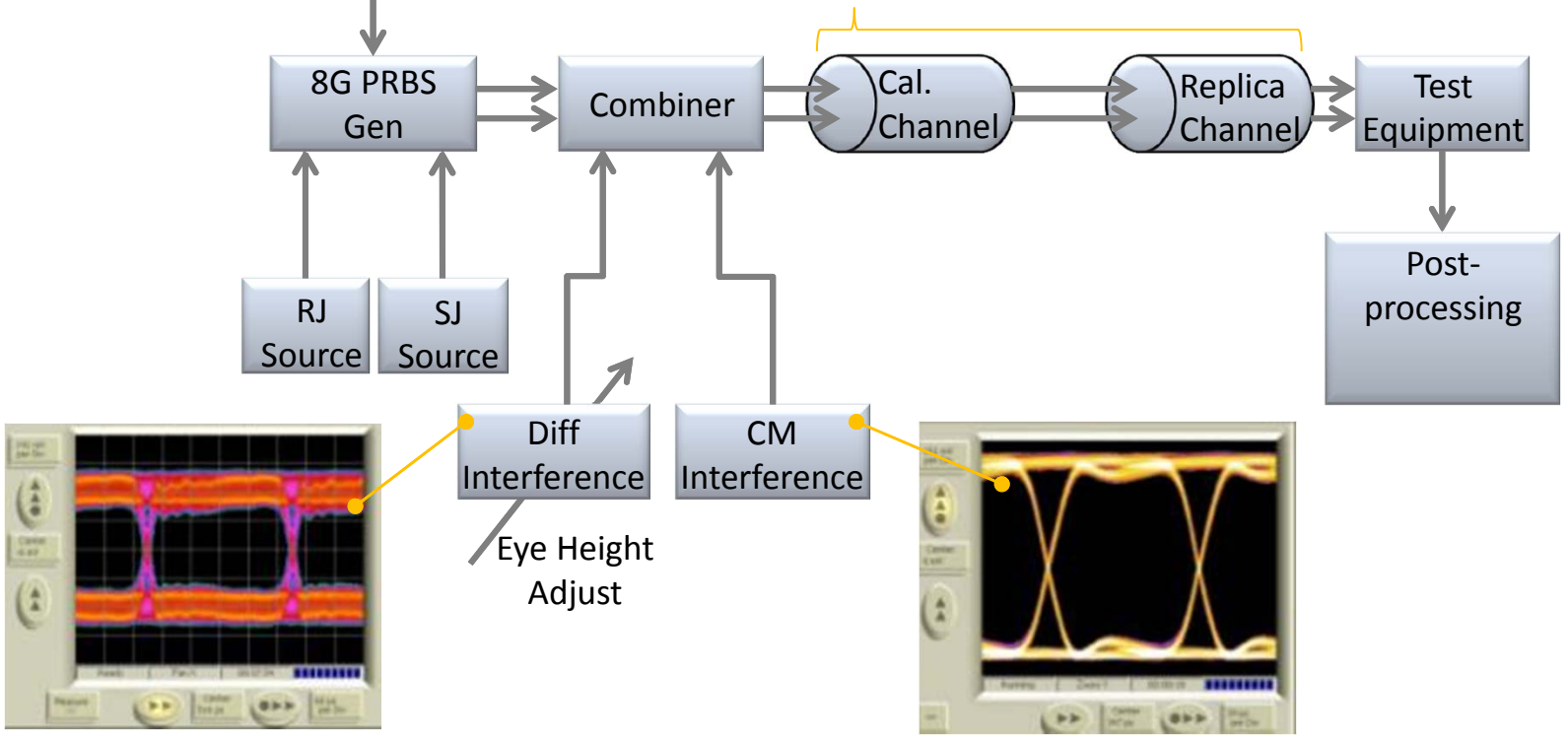


PCI Express Gen 3 uses a long circuit board channel that closes the eye, and two forms of vertical eye closure ('Interference').




(Taken from PCI Express Base Spec, Figure 4-71)



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# PCIe Gen 3 Stress Recipe - Interference

| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |

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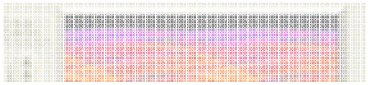
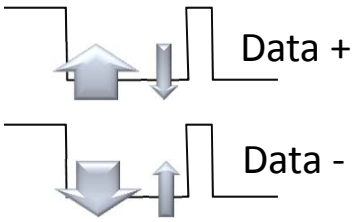
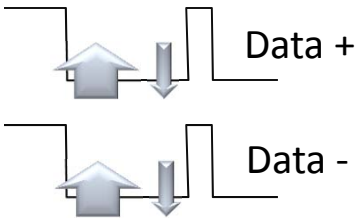
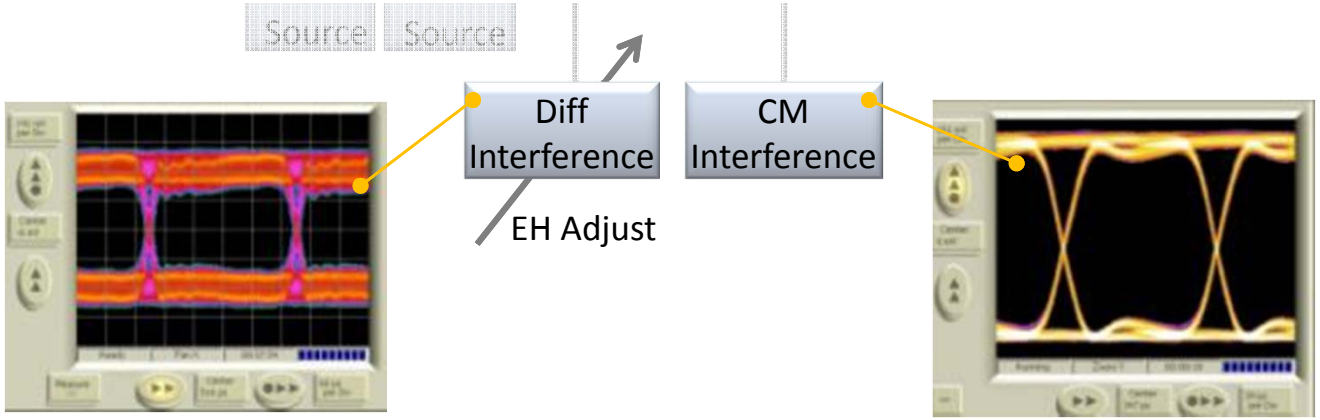


**Differential Mode** interference is used to simulate ***uncorrelated crosstalk***. Operating PCIe3 systems have multiple (x16) lanes sitting right next to each other with high likelihood of coupling from adjacent signals.




**Common Mode** interference is used to simulate ***modulated voltage and ground rails***. It is difficult to completely filter out switching supplies in a PCIe3 system and other low frequency modulation effects beyond the loop bandwidth of the system.



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# PCIe Gen 3 Stress Recipe - Channel

| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |

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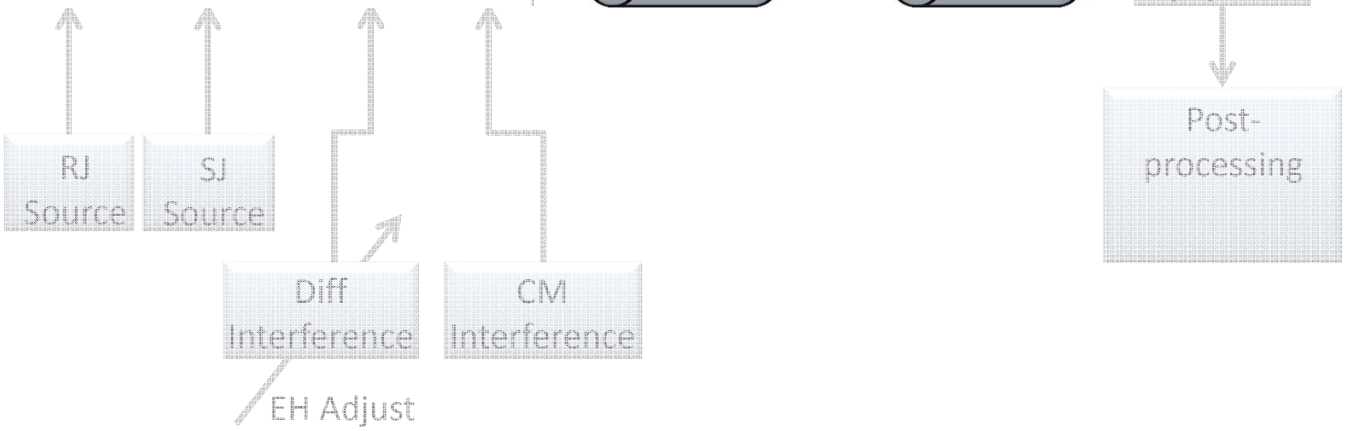
- Depending upon Host or Add-in Card, different test fixtures/combinations are used.
- ISI is large enough to mean the **Eye is closed at the receiver.**



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# PCIe Gen 3 Stress Recipe - Calibration

| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |

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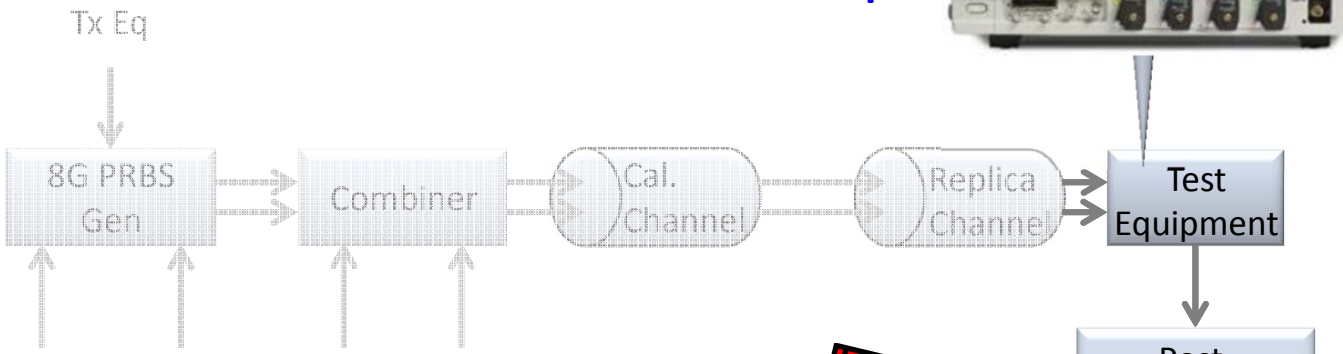
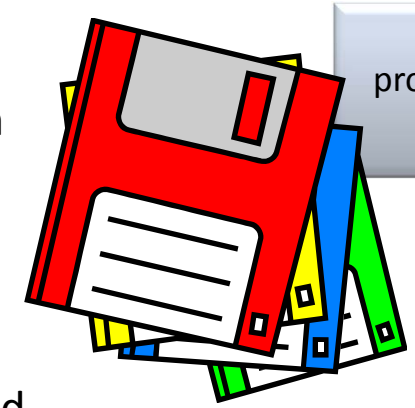
Long waveform **capture by Real Time Scope**




**Post-processing by software**.
Several complex elements are accommodated in software including the IC package and elements within the IC including the equalizer.



***This is still in flux*** – Correlation work ongoing between simulation and direct measurement and analysis techniques. **Being refined at Plugfests**



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# USB 3.0 Stress Recipe - Calibration

| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |

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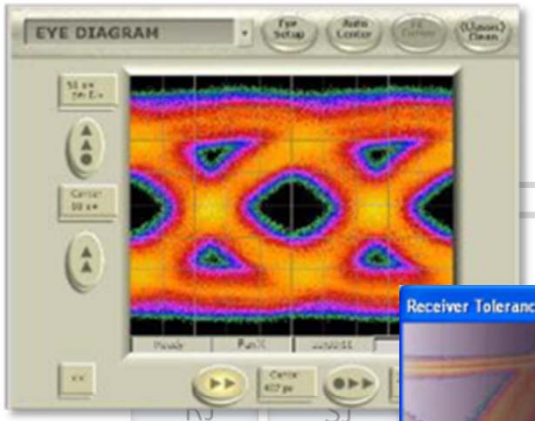
Long waveform **capture by Real Time Scope**

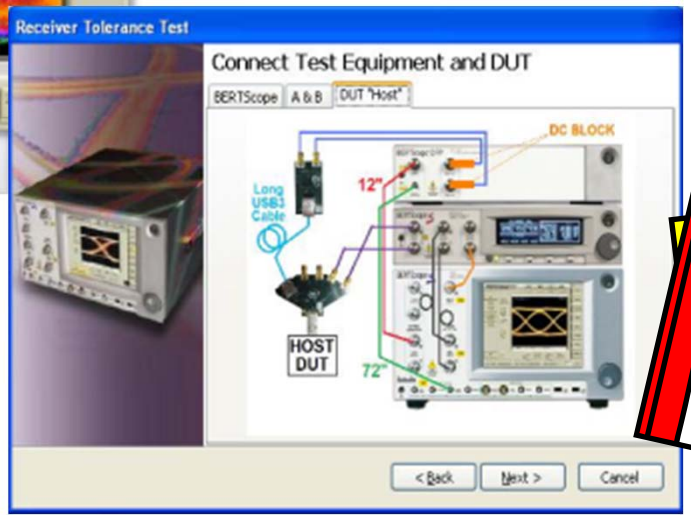



Channel

Test Equipment

✓

Post-processing




**Mature standard** with **fully automated** solutions for stress calibration and **good correlation**



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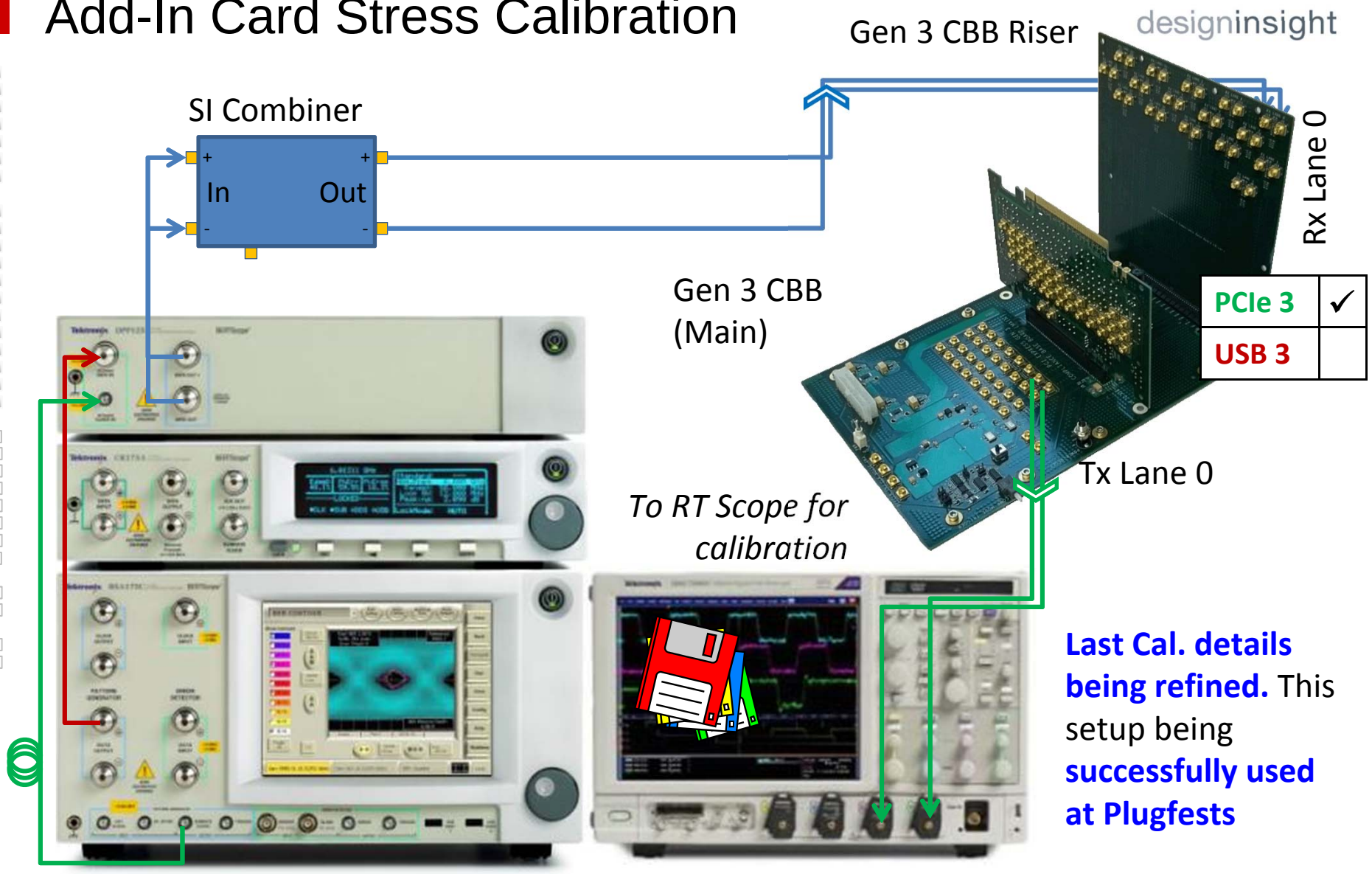
# PCIe Gen 3: Example
# Add-In Card Stress Calibration




**Last Cal. details being refined.** This setup being **successfully used at Plugfests**



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# 3. System Aspects

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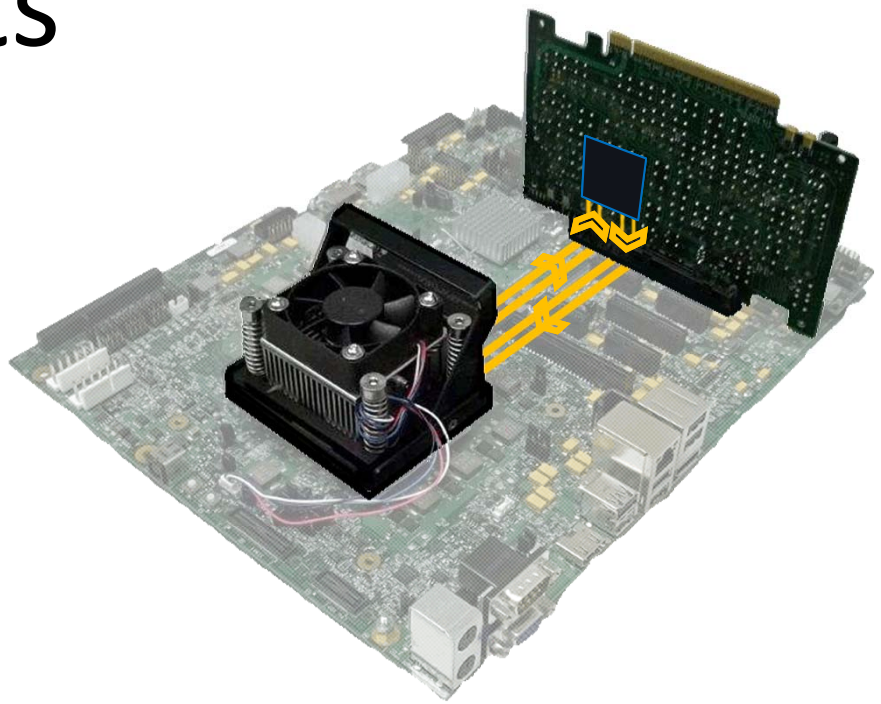



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# Agenda

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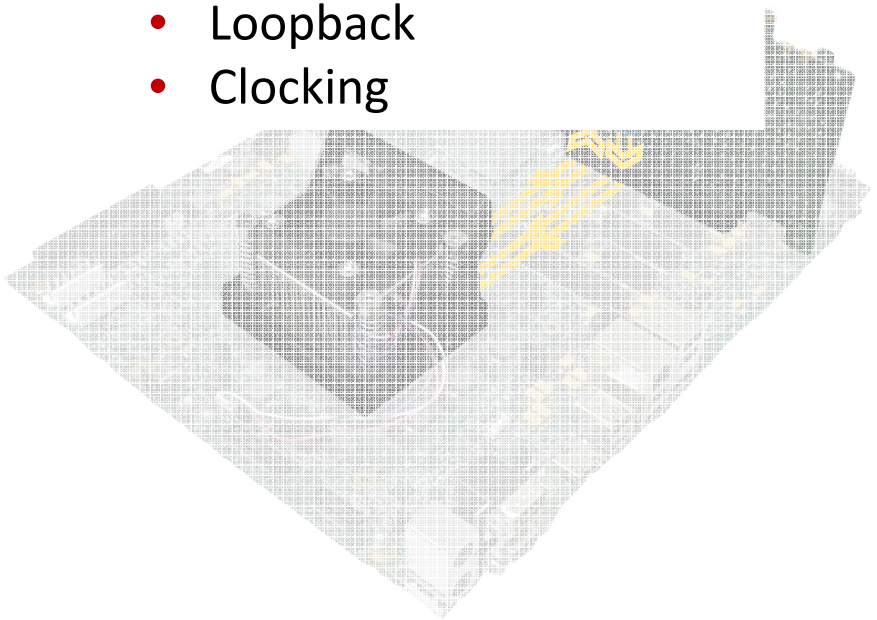
1. Introduction
2. Stressed Eye

# 3. System Aspects

- Closed Eye Return Signal
- Loopback
- Clocking



4. Beyond Compliance
5. Resources



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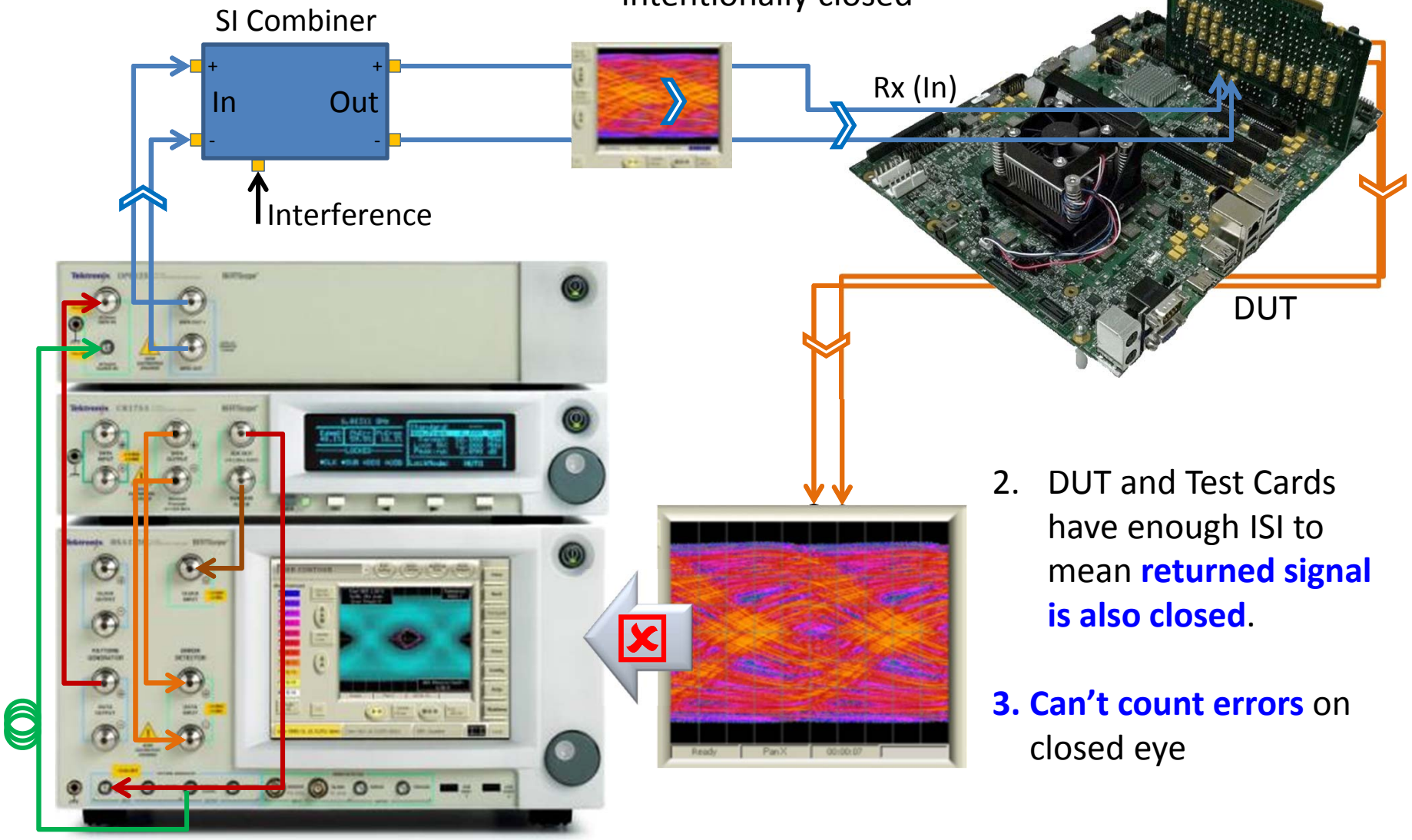
# PCIe Gen 3:
## Test Setup with DUT

| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |

1. **Stressed Eye** is intentionally closed




2. DUT and Test Cards have enough ISI to mean **returned signal is also closed**.

3. **Can't count errors** on closed eye



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# PCIe Gen 3:
## Test Setup with DUT & Eye Opener

| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |

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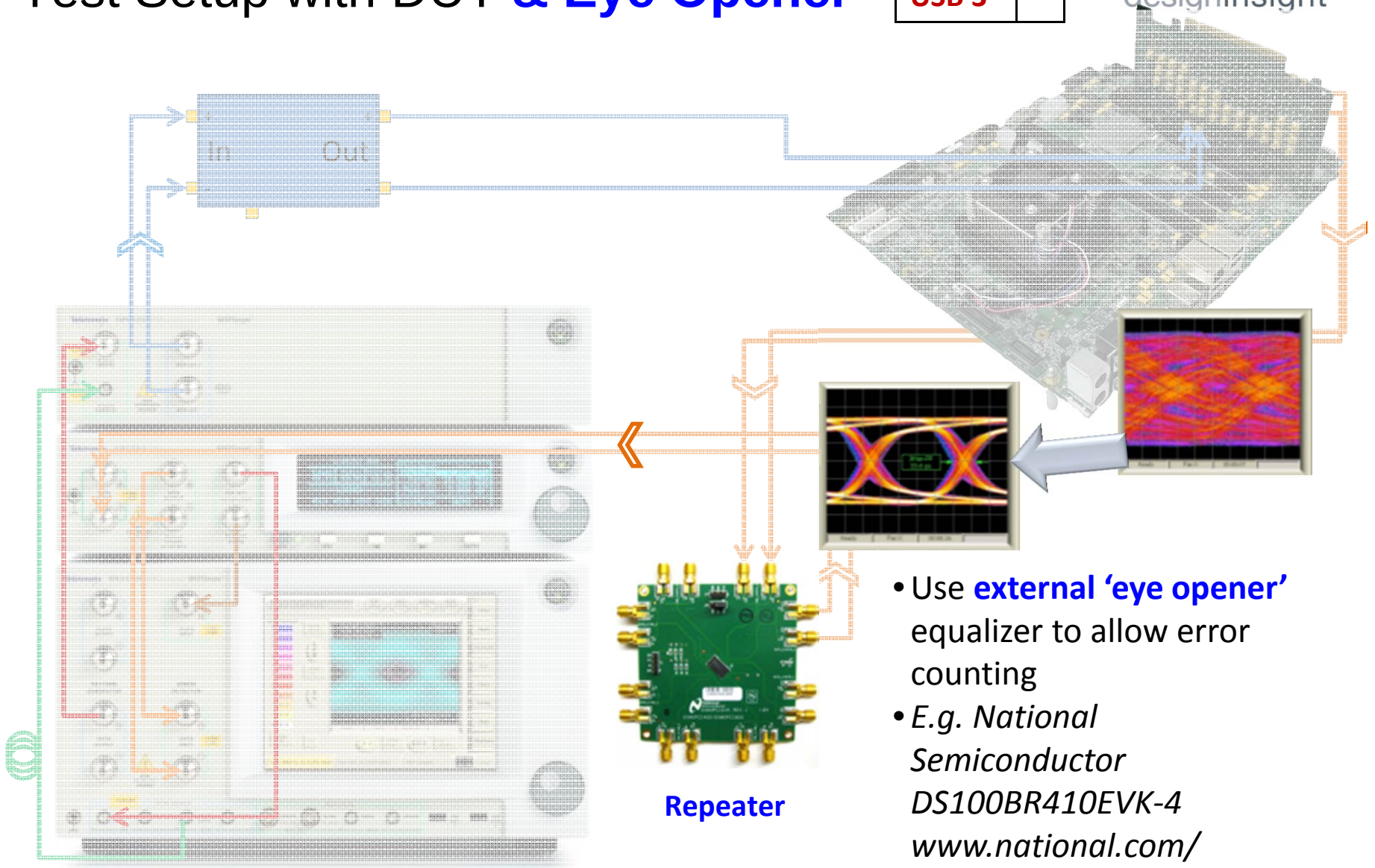


Repeater

- Use **external 'eye opener'** equalizer to allow error counting
- *E.g. National Semiconductor DS100BR410EVK-4 www.national.com/*



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# Loopback

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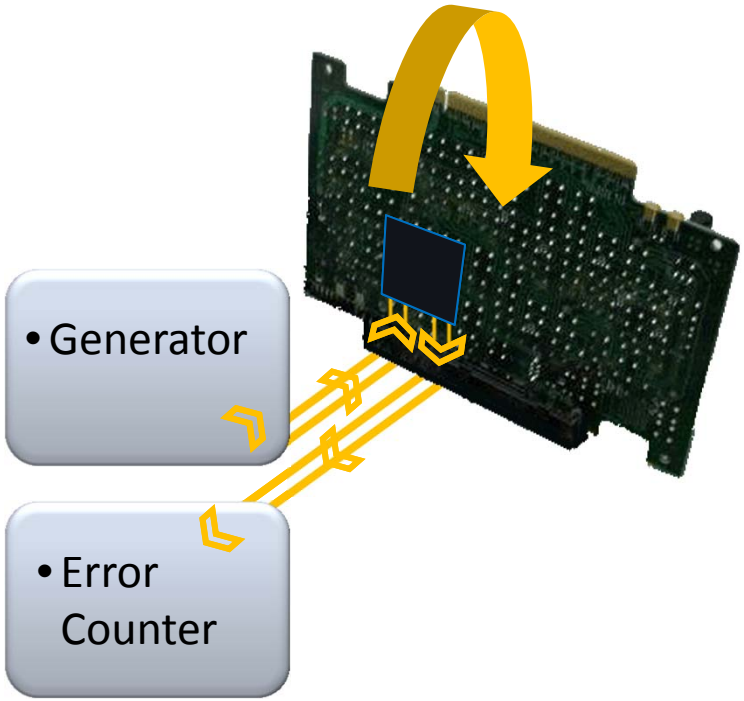
1. Loopback usually **specified in the standard** with a method to initiate it.
   1. **IC companies have control** over their chips and can **usually force the chip into loopback**
   2. Often a pattern sent from a generator of a **particular sequence** is supposed to cause it also.
      1. Obeying loopback rules is not part of compliance test, so **rules frequently broken.**
      2. Attaining loopback at **Plugfests can be painful**.

2. Devices often **fall out** of loopback during testing.

3. Often **hard to know** device has attained loopback (*waveform analyzer such as BERTScope ED often useful*)



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# Loopback – **USB3**

| | |
|---|---|
| PCIe 3 | |
| USB 3 | ✓ |

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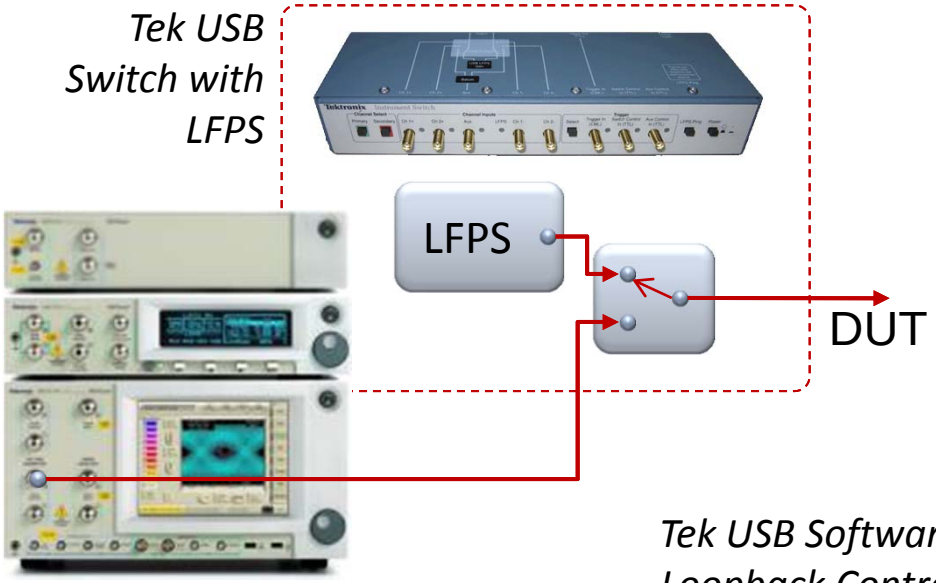
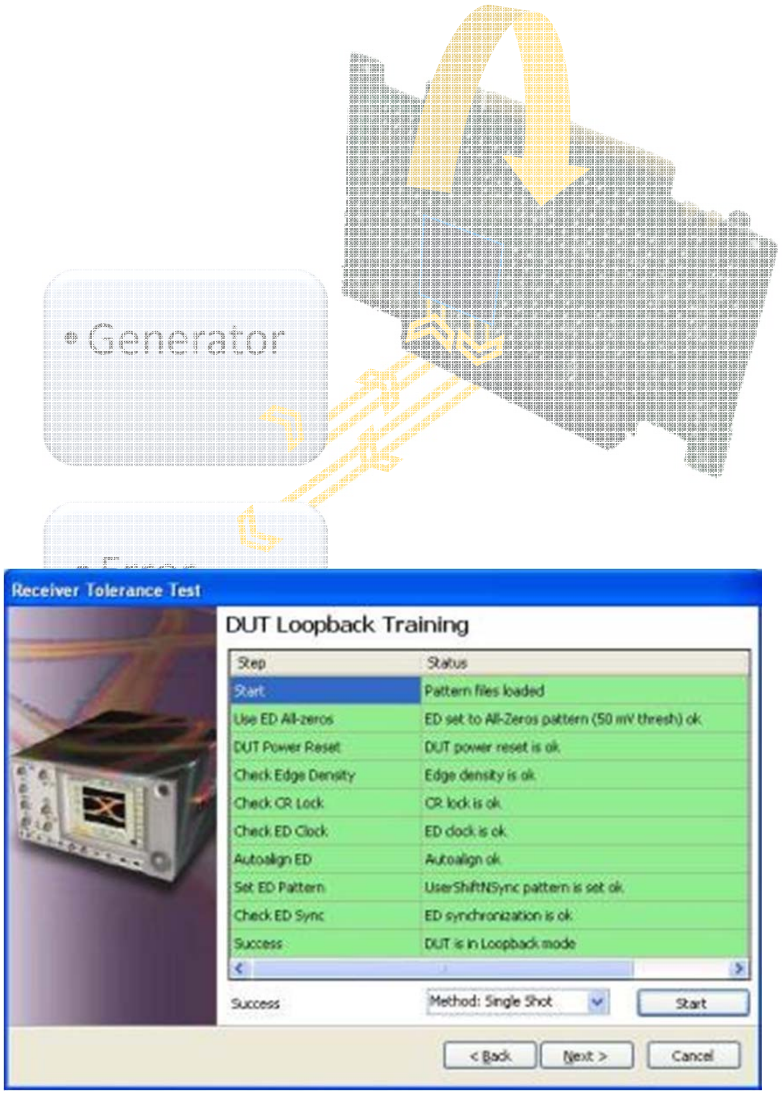
- USB3 specifies a sequence of bits to initiate it that forms a **low frequency square wave** (“LFPS”).
- Frequently test equipment will use a **separate generator** for loopback initiation which **switches** out once loopback is attained.




*Tek USB Switch with LFPS*




*Tek USB Software Loopback Control*



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| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |

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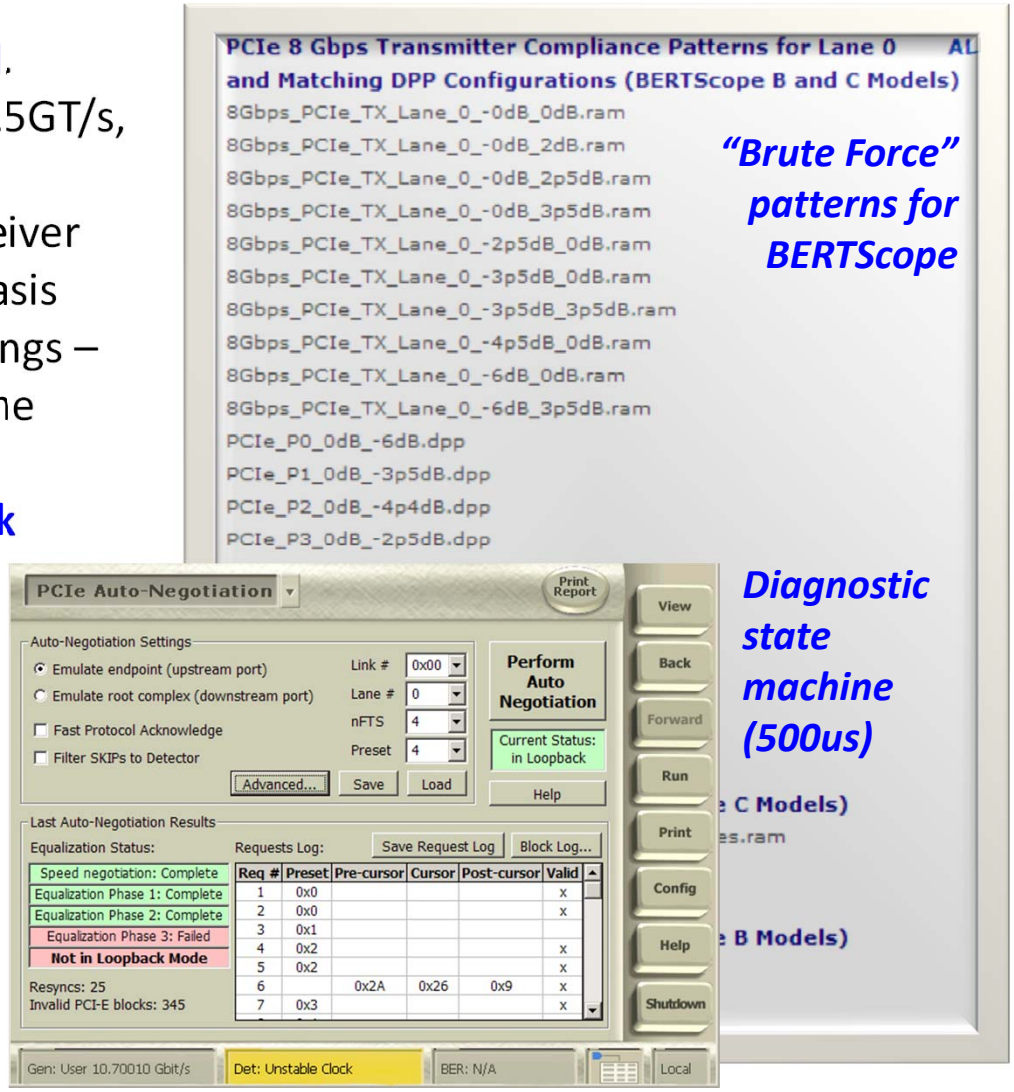
# Loopback – PCIe 3

- **PCIe 3 loopback is more complicated**.
  1. **Speed negotiation** – natively 2.5GT/s, needs to negotiate up to 8GT/s
  2. **Equalization negotiation** – receiver controls transmitter pre-emphasis and find optimum Tx & Rx settings – 500ns compliance response time limit
  3. **Setting of device into Loopback**
- Initially "**brute force**" with static patterns
- Now **compliant state machine**

- Feedback from Plugfests is that Add-In Card manufacturers **aren't implementing equalization negotiation yet**. Instead test with limited number of pre-emphasis presets (3)



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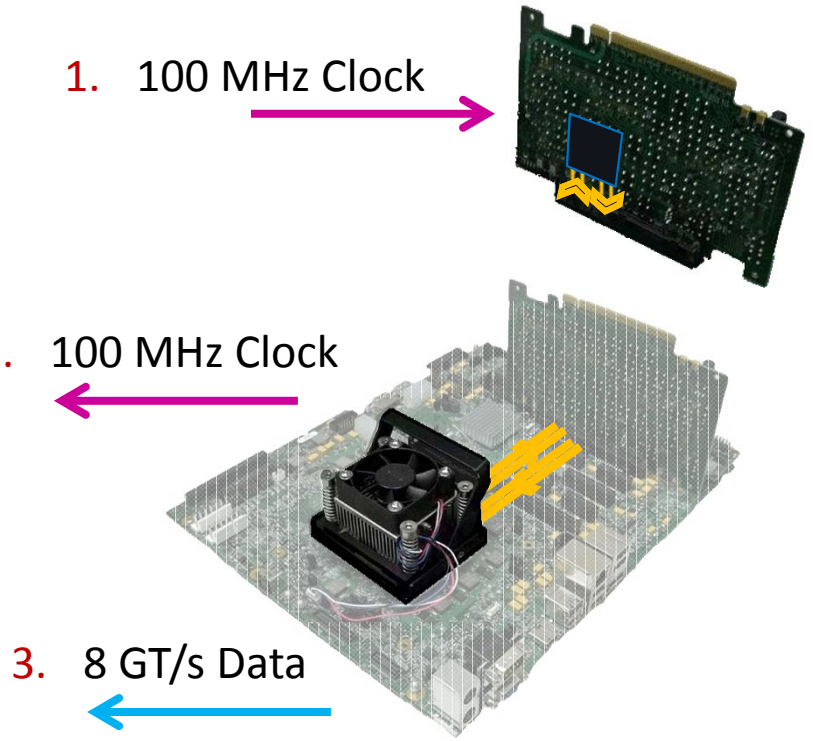
# Clocking – PCIe3

designinsight

- **Add-in cards** take in a 100 MHz clock.
  - This is **straight forward**, test equipment usually provides sub-rate clock easily (**1**).
- **Motherboards are harder** – DUT provides 100 MHz clock (**2**), but test equipment needs **8 GHz clock**.
  - Could derive clock from 8 GT/s data signal using clock recovery (**3**). Device margins are small enough to mean worries about extra jitter added by the transmitter.
  - **Ideally** use **well controlled clock multiplier** from system 100 MHz clock.




| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |



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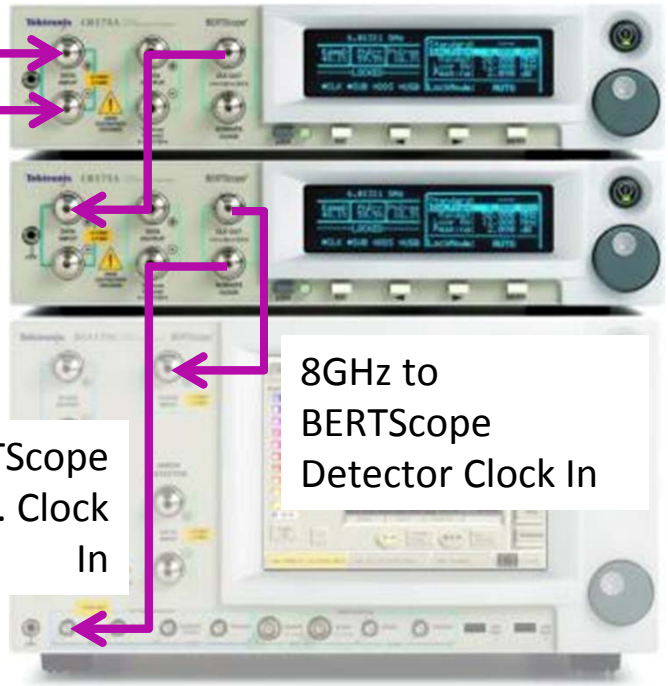
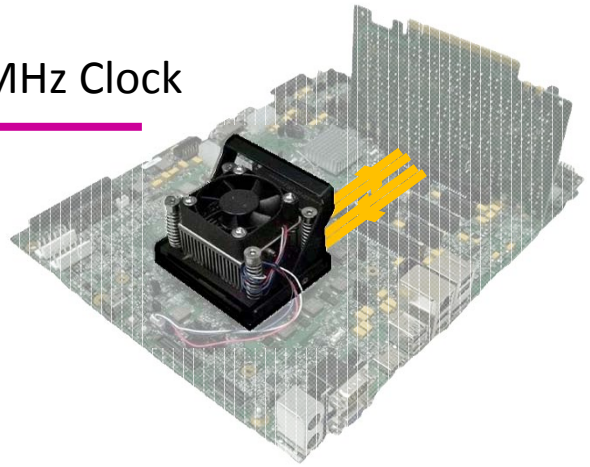
# Clocking

designinsight

- **Practical setup** used for Plugfests to multiply system clock (**2**)
- Clock multiplied in two stages to preserve **compliant loop bandwidth & peaking**




2. 100 MHz Clock



| | |
|---|---|
| PCIe 3 | ✓ |
| USB 3 | |



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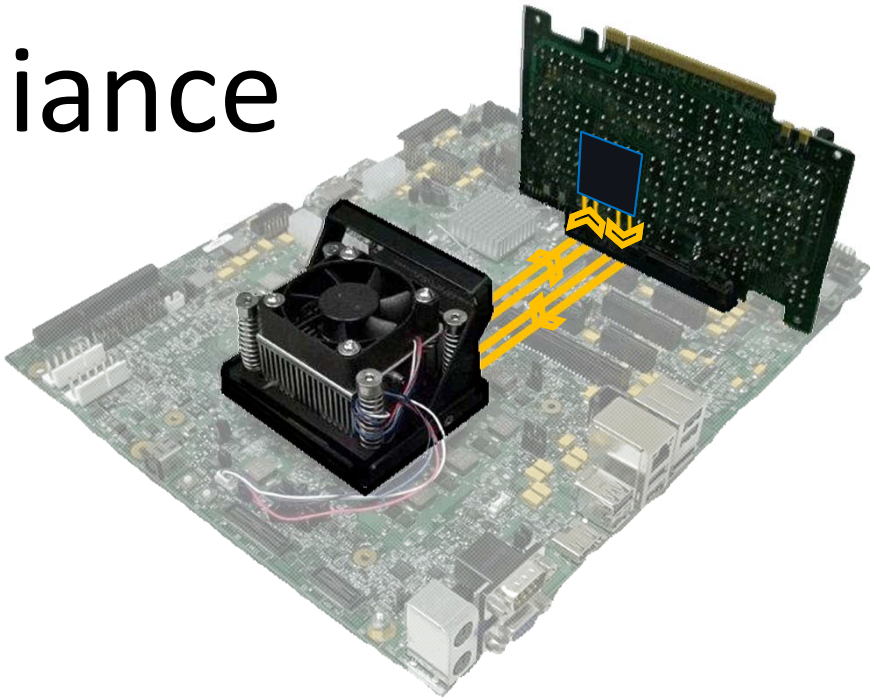
# Agenda

designinsight

1. Introduction
2. Stressed Eye
3. System Aspects

# 4. Beyond Compliance

5. Resources



**When a Device Fails… What Next?**



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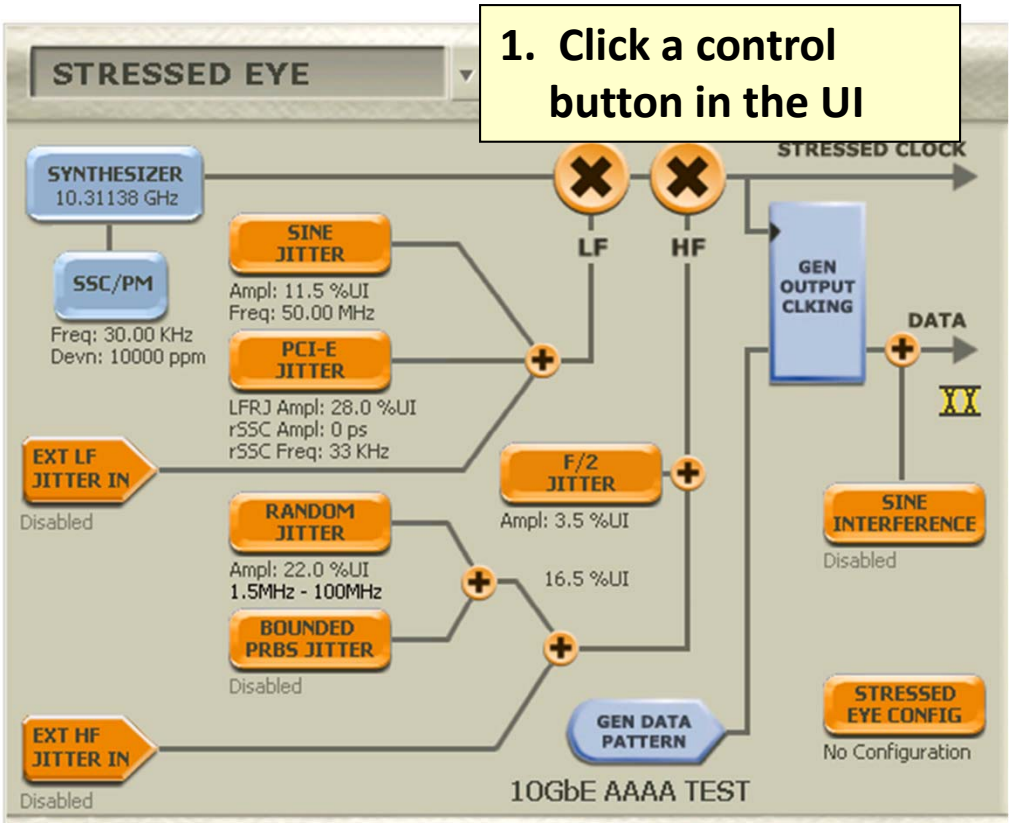
# Beyond Compliance
# BERTScope = Debug/Characterization

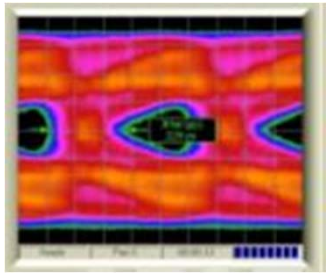
designinsight




**2. Adjust**

*Easy adjust with turn of the knob*

**3. Changes happen *instantly***



- You may need to **try lots of** different **signal conditions**
- May want to **monitor BER** while **changing stress conditions** on the fly



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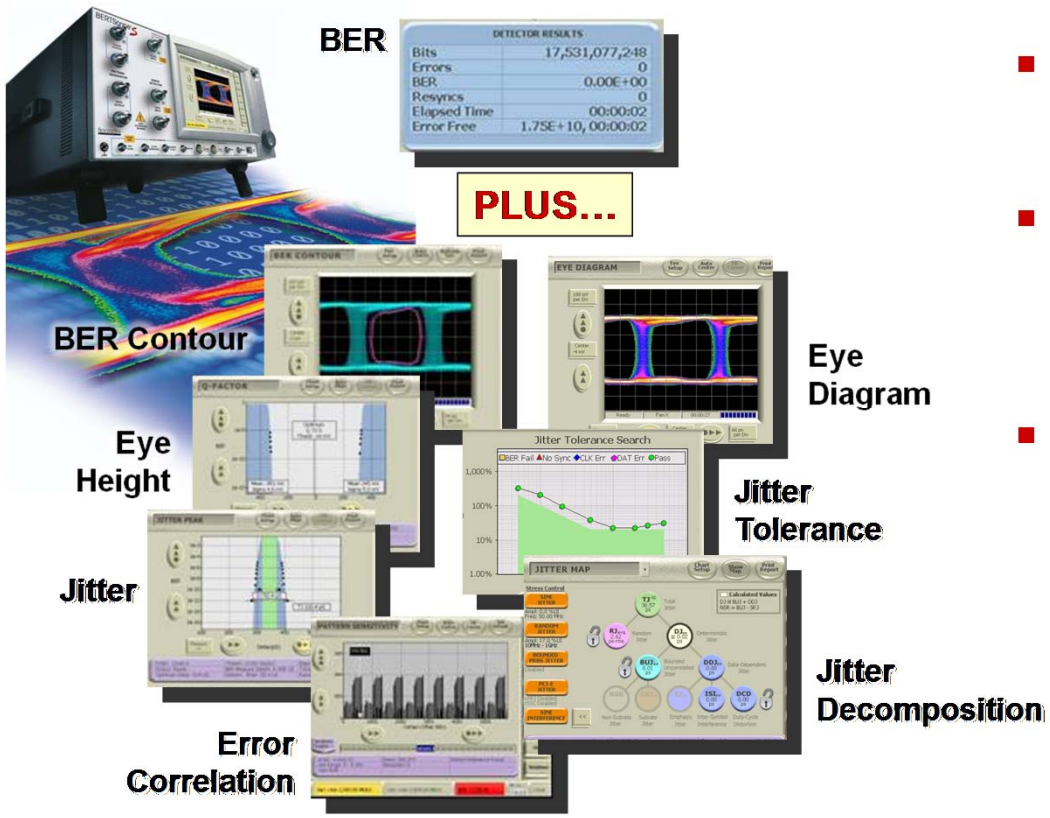
# Beyond Compliance
# The BERTScope Analysis Tools

designinsight

- Besides being a BERT, the BERTScope's **"Scope" functionality** brings benefits that complement those of the Tektronix scopes
- **Analysis tools are full featured and easy to use**




- Frees up the scope for other tasks
- **Eye diagram for quick diagnosis** of synchronization and BER failure issues
- **Debug** challenging **signal integrity problems**



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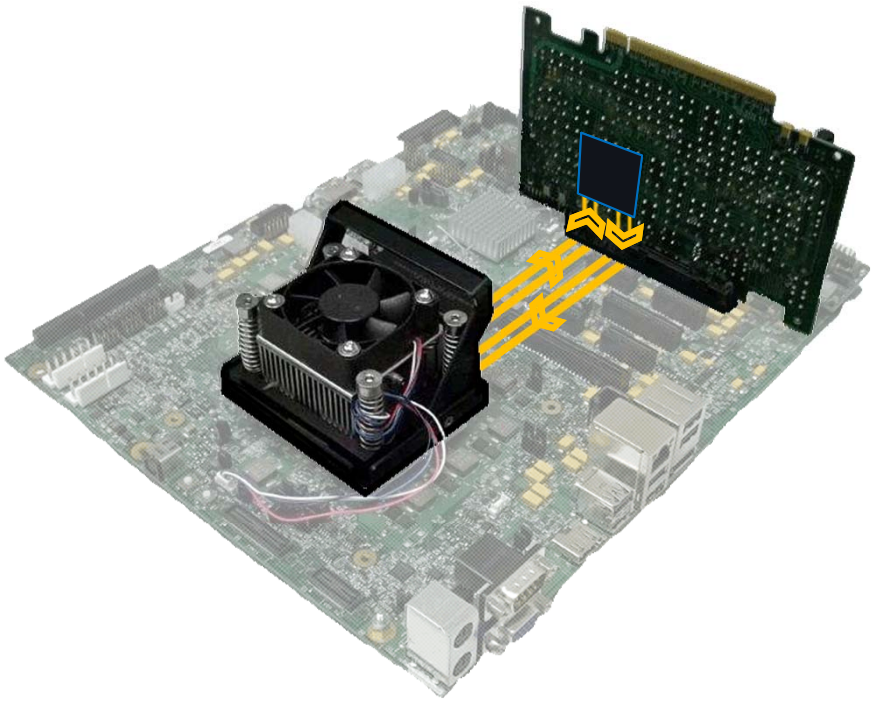
# Agenda

designinsight

1. Introduction
2. Stressed Eye
3. System Aspects
4. Beyond Compliance
5. Demonstration

# 6. Resources





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# Resources


Extensive application information at:

**www.tek.com**

**PCI-Sig,** www.pcisig.com
**USB-IF,** www.usb.org



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# Summary

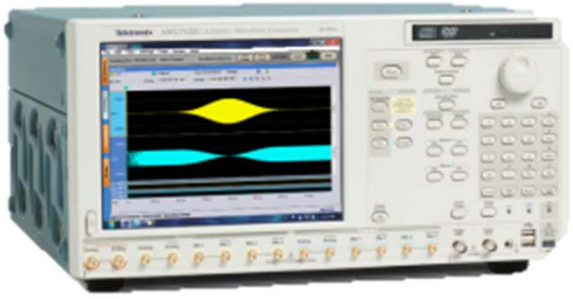
designinsight

- **Higher speeds** on **cheap** channel **materials** causing **closed eyes** from ISI and crosstalk
- Increased **use of equalization** forcing changes in testing: speed, equalization negotiation & Tx control
- Test signal is changing:
  - **Vertical eye closure**
  - **Closed eye**
- **Calibration** is evolving
- Attaining **Loopback** is often **problematic**.
- **Returned signal** is often also a **closed eye**, meaning eye needs opening before error counting

High Speed Receiver Test Solutions from Tektronix:

**BERTScope** Family

Arbitrary Waveform Generator (**AWG**) Family





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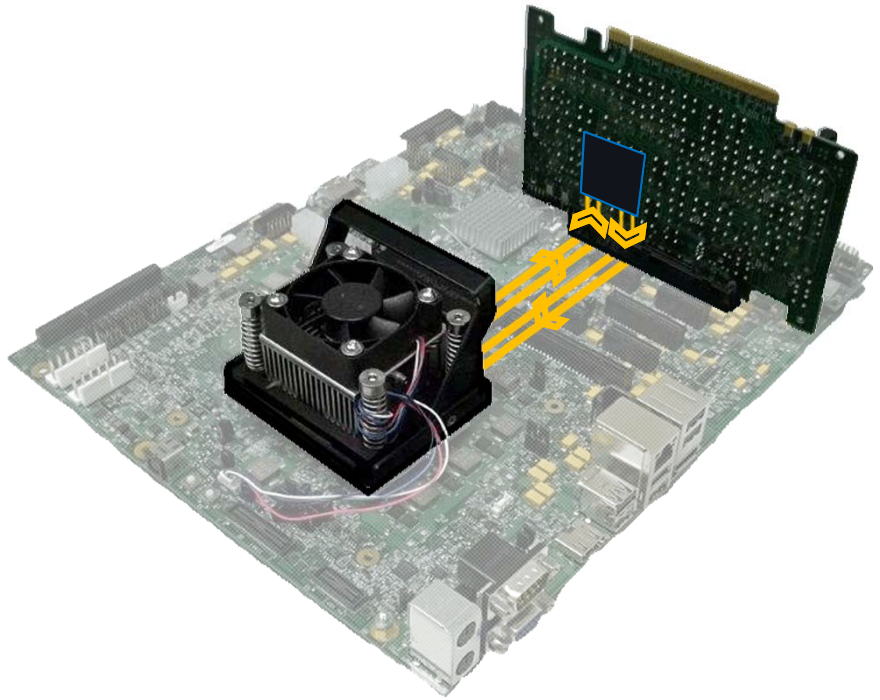
# Questions?

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