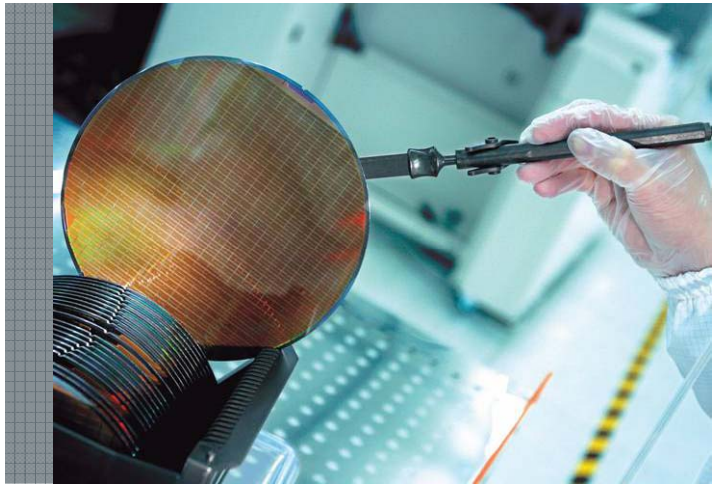
Serial Data Transmitter & Link Analysis

The Evolution of Serial Data testing and how to prepare for next generation standards

John Calvin, Tektronix



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Serial Data Transmitter & Link Analysis

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- High Speed Serial Data Overview and Standards
- Channel modeling and Equalizers
- Transmitter Characterization
  - Core AC parametric and Jitter Measurements
  - Advances in jitter decomposition.
  - BUJ and relevance to multilane topologies.
- Digital Trigger and Data Decode
- Emerging High Speed Standards

Standards REFERENCES

(1) Richard Mellitz: Intel: T10/ 11-275r0 SAS-3 12Gbs Transmitter Device Test Proposal

(2) Doron Lapidot: Tyco: T10/10-219r0 SAS 3.0 B-t-B Connector & Cable assembly Channel Performance @ 12Gbps "Modeling, Measurements & Simulations for BER compliance with multi Aggressor System Interconnect"

(3) Mickey Felton: EMC: T10/11-239r0 Channel compliance points and lengths

(4) Kevin Witt: Maxim: T10/11-221r4 SAS-3 Electrical Spec (Draft)

(5) Mathieu Gagnon : PMC-SIERRA: T10/11-008r3 SAS-PHY: SAS3_EYEOPENING update

(6) Mladen Luksic: SATA-IO: IW12 Roadmap Update

(7) Intel: Thunderbolt .5 Revision Specification

General REFERENCES:

[1] IEEE is 25Gb/s on-board signaling Viable? KAM et al.: IEEE Transactions on advanced Packaging, Vol. 32, No. 2, May 2009.

[2] IEEE CMOS SerDes core with feed-forward and decision-feedback equalization . T. Beukem et al.: IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2633–2645

High Speed Serial Data Overview and Standards

High Speed Serial: Defined

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- Fast serialized data buses are replacing many parallel buses
  - Fast serial signals were found mostly in Telecom and Datacom industries. They now span several industries including Computer, Consumer, Government, and even Automotive.
  - ***High Speed Serial*** applications range from hundreds of MHz to tens of GHz: these speeds span the Tektronix performance and high bandwidth products.

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Specific Requirements for High Speed Standards
Very different technologies which share a great deal.

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	Data rate/lane [Gbps]	Pre- / De-emphasis in Tx	Equalization: FFE only: ○ FFE/DFE: ● CTLE: ♦	Far End Channel Emulation
USB 3.0	**5**	●	♦	●
DisplayPort HBR2	**5.4**	●	♦	♦
SATA Gen 3	**6**			●
SATA Express (Gen 4)	**8**	●	♦	●
PCI Express 3.0	**8**	●	♦	●
SAS-3	**12**	●	●	●
10GE Ethernet KR (backplane)	**10.3125**	●	●	●
Thunderbolt	**10.3125**	●	●	
FibreChannel 16GFC InfiniBand FDR	**14.025**	●	●	●
IEEE 802.3ba 100 GbE 4x25	**28 (w FEC)**	●	●	●

Channel modeling and Equalizers

History: One has to know where they've been to see where they are going

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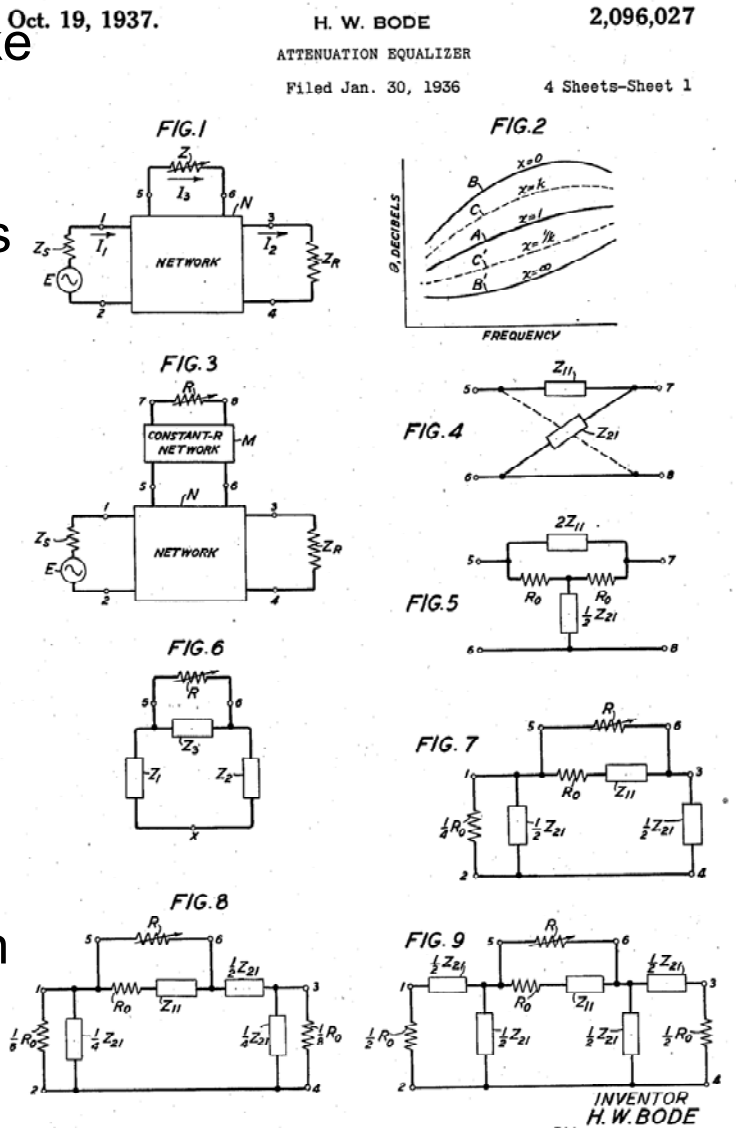
- Modern transmission control systems make use of an array of Transmit (Tx) and Receiver (Rx) equalization techniques to overcome the frequency dependant losses found in all transmission media.

- In 1929 Hendrik Bode working for Bell Labs, literally wrote the book (ISBN: 0882752421) on transmission equalization methods and network analysis which continues today as the foundation of modern Data-Comm engineering.



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Fast forward 70 years: Digital Feed Forward and Decision Feedback equalization

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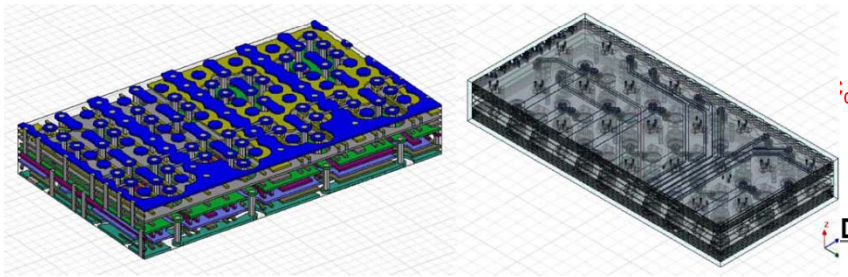
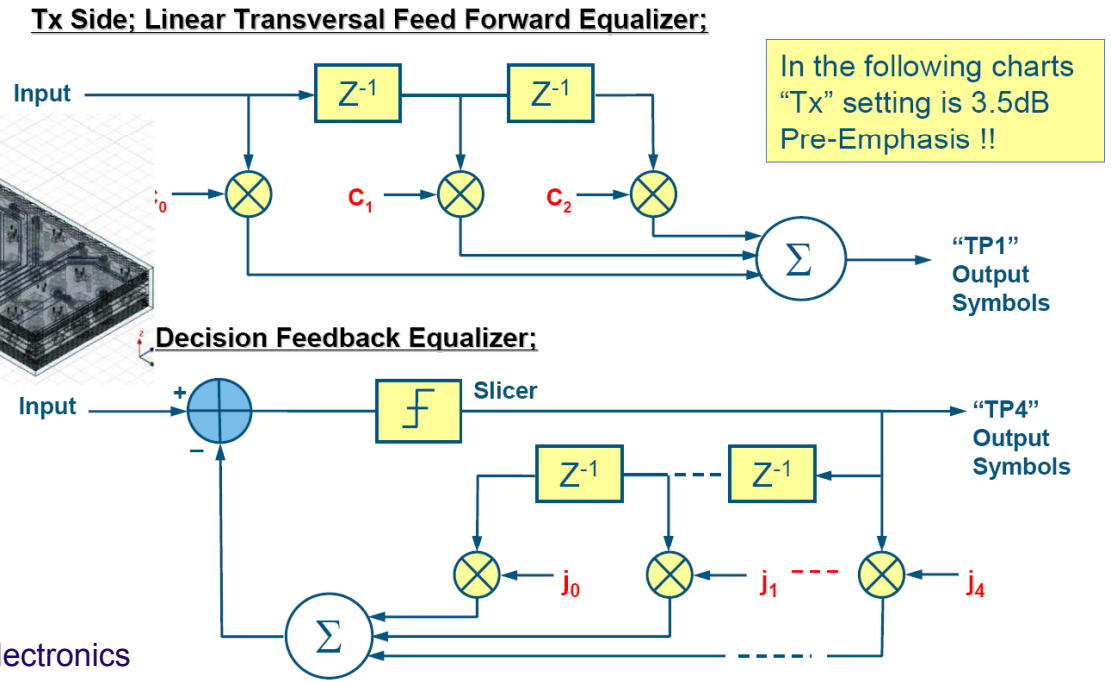
- A non-recursive DFE can only compensate a fixed time span of ISI. In very low-bandwidth channels, significant post-cursor ISI may fall outside the time span covered by the DFE taps.
- FFE can compensate ISI over a very wide time span since the FFE filter response is convolved with the impulse response of the channel.
- The utility of FFE alone drops off rapidly over complex channels which have spectral nulls (Via stubs, connectors, etc) which require many FFE taps to cancel reflections.
- Optimal solutions exist around 4-tap FFE with 20+ tap DFE designs. More emphasis is required in the Receiver section of the topology as more aggressive FFE makes crosstalk worse.

Ref:[1], [2]





Ref:[2]: Tyco Electronics

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SDLA (Serial Data Link Analysis)
High Speed Serial Requirements

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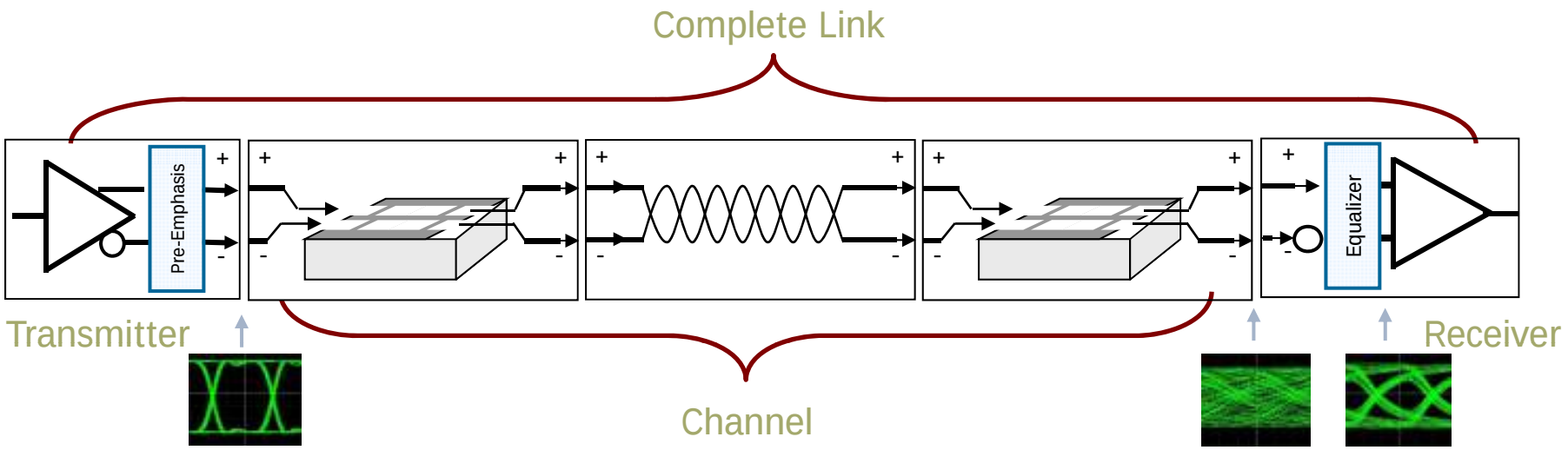

- Traditional measurement techniques are inadequate – e.g., measuring transmitter or receiver alone is insufficient
- Must understand interactions between transmitter, channel and receiver
- New techniques (Equalization) employed to compensate for signal loss at speeds >2.5 Gb/s
- Must analyze pre-emphasis effects at the transmitter output – to see if sufficient
- Need to understand effects/remove of measurement systems (e.g., test fixture, probing)
- Channel performance does not easily scale with transmitter/receiver performance

Complete Link Needs to be Considered – Need for Serial Data Link Analysis

Dynamic Range Range -vs Data Rates –vs- Channel Loss

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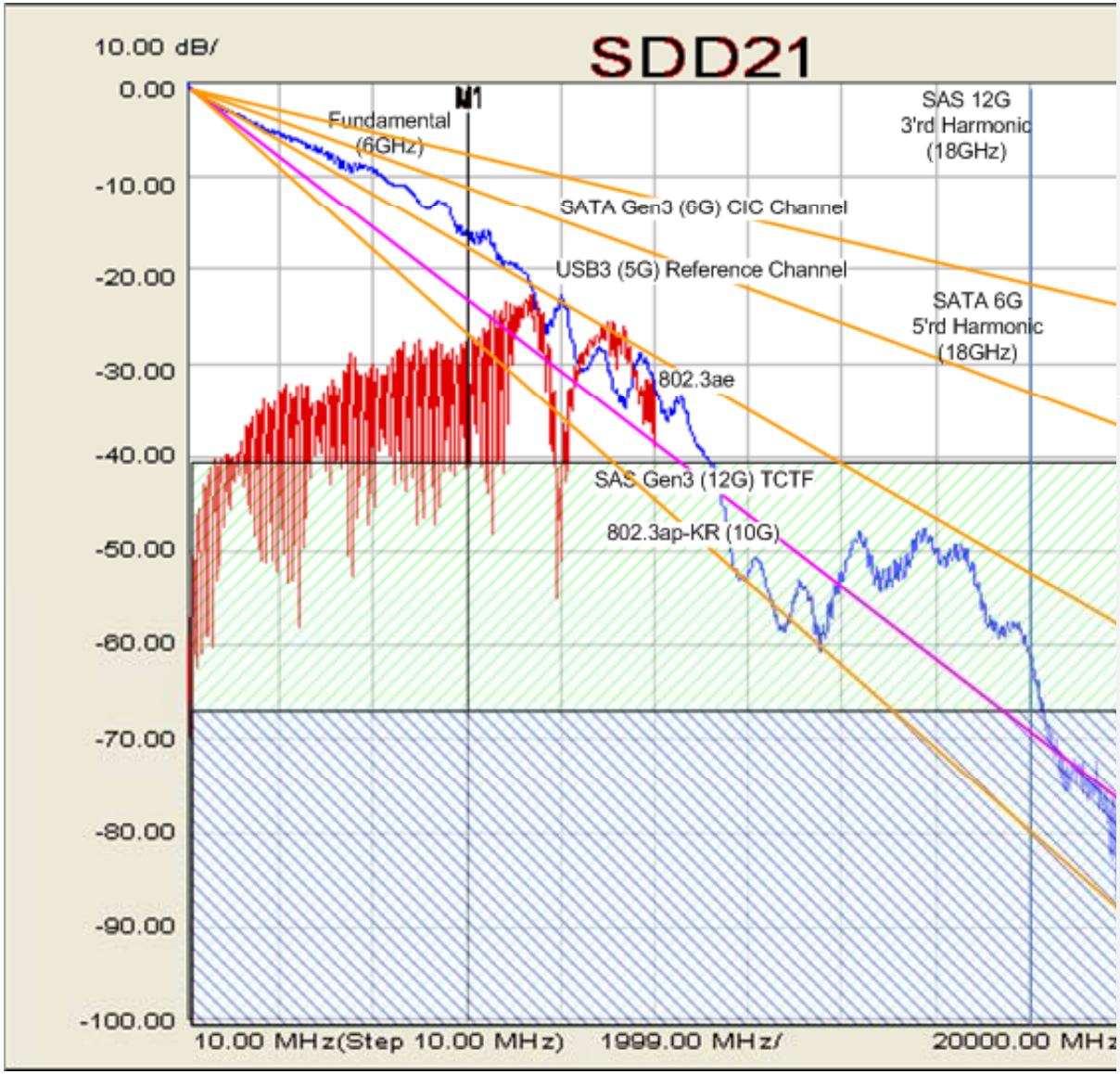

- 10+G datarates are being achieved by both advanced DFE, and FFE systems with link training and adaptive channel compensation.
- Channel bandwidth is determined largely by the intersection of de-embed stop bands and even signal harmonic content.
- The focus is on ***extracting the un-tapped carrier capacity*** in the low dynamic range regions of the transmission channels.

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Design Problem:
FFE, Crosstalk, Crosstalk, Crosstalk, DFE, 50mV

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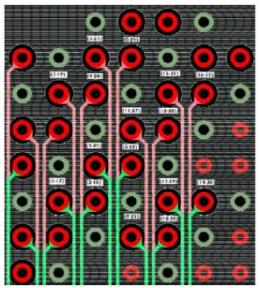
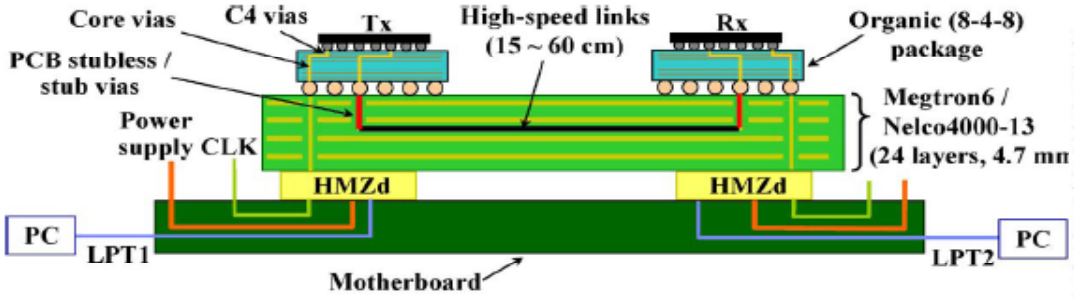
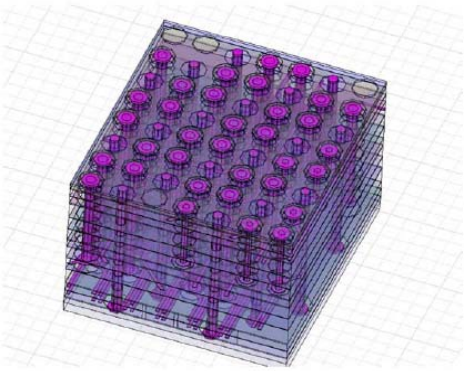
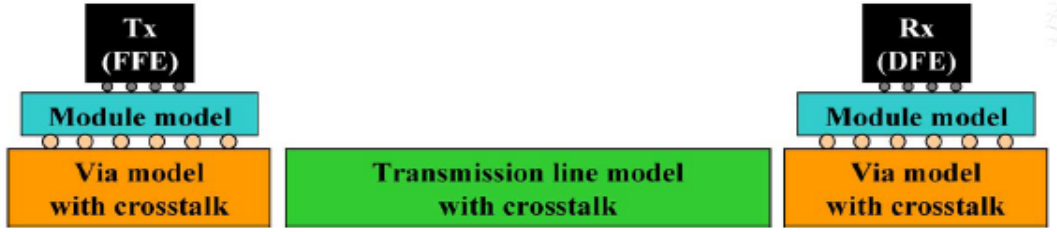
- Significant advances in high tap count Decision Feedback Equalization are key to operating above 10Gbs.
- Mitigating the complex Channel Crosstalk and Signal loss problems are the largest design challenge today.
- Typical Escape Structure bandwidth is 18GHz.
- Crosstalk is often beyond the capability of current equalization architectures to combat, and needs to be quantified if accurate performance projections are to be made based on experimental measurements. For short channels, NEXT may be less of an issue since the insertion loss is not as severe; however, in longer links and at higher data rates it has the potential to become a dominant design consideration. Ref:[1]

KAM *et al.*: IS 25 Gb/s ON-BOARD SIGNALING VIABLE? 329









Ref[1]: IEEE

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Spectrum
PRBS7 12G NRZ Power Spectrum

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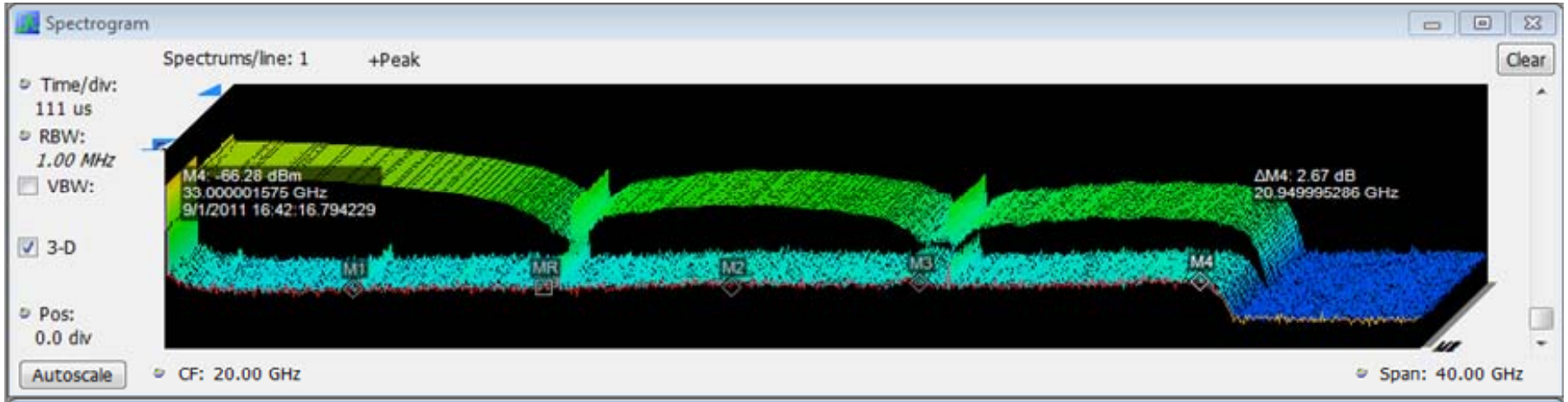

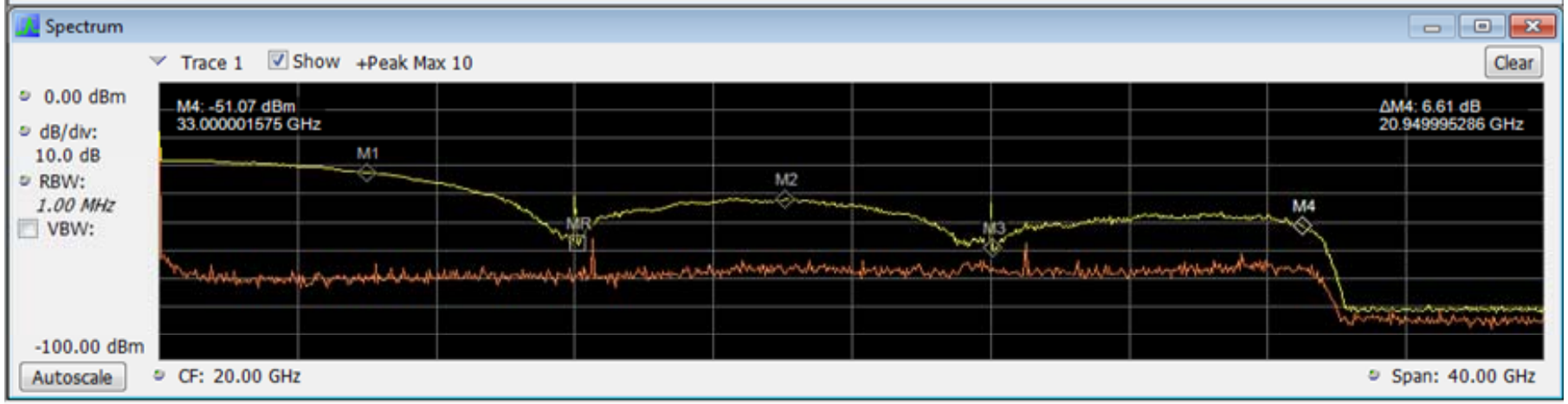

Marker Readout Table

Marker	Frequency	Δ Frequency	Δ Time	Spectrum	Δ Spectrum	Spectrogram	Δ Spectrogram
M2	18.050004939 GHz	5.99999865 GHz	---	-42.01 dBm	15.67 dB	-68.71 dBm	0.24 dB
M3	24.050003589 GHz	11.9999973 GHz	---	-59.20 dBm	-1.52 dB	-66.74 dBm	2.21 dB
M4	33.000001575 GHz	20.949995286 GHz	---	-51.07 dBm	6.61 dB	-66.28 dBm	2.67 dB

Bandwidth

Signal Acquisition and bit rate harmonics

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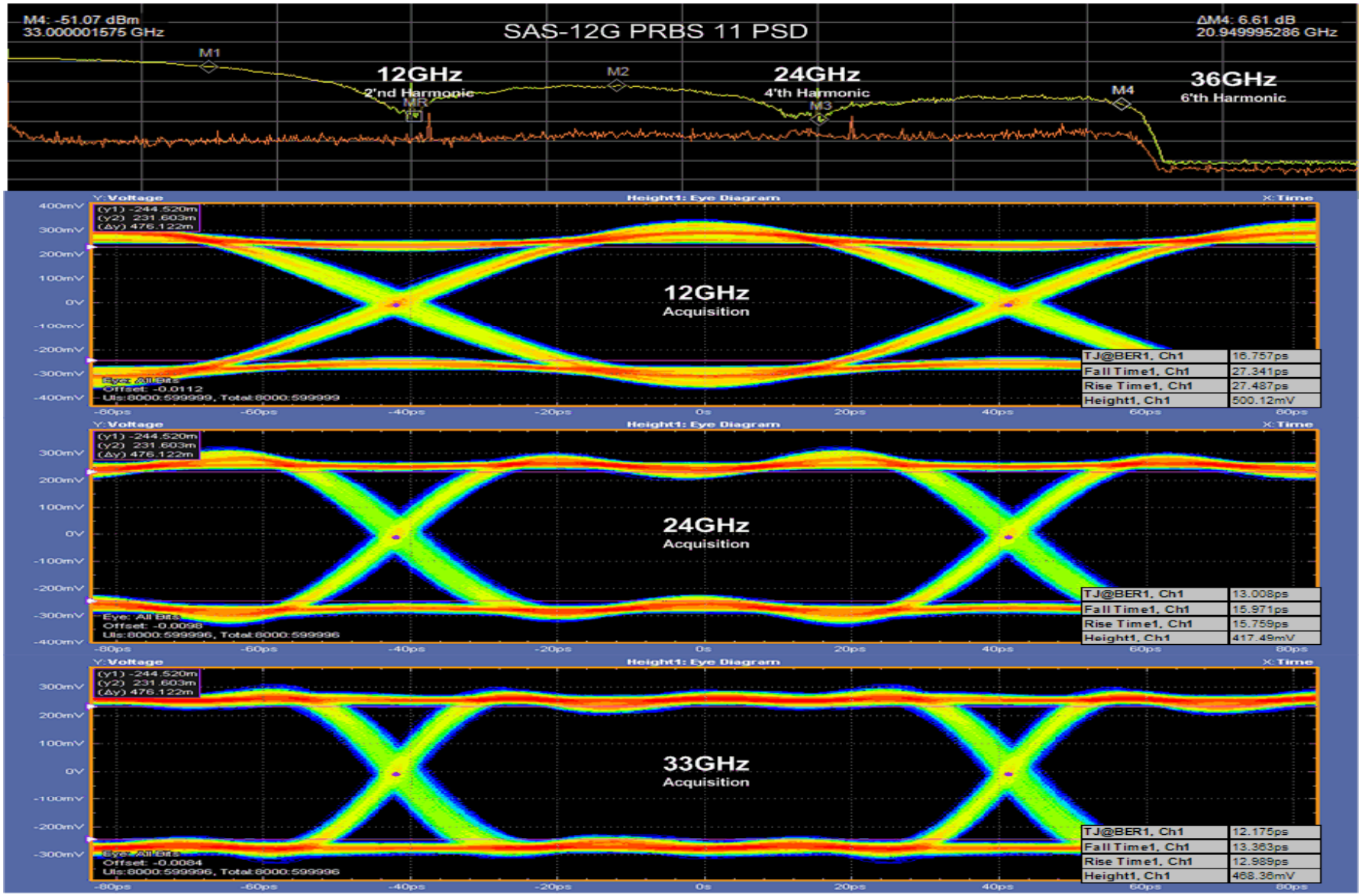

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Bandwidth
Filter Stop-Band Characteristics

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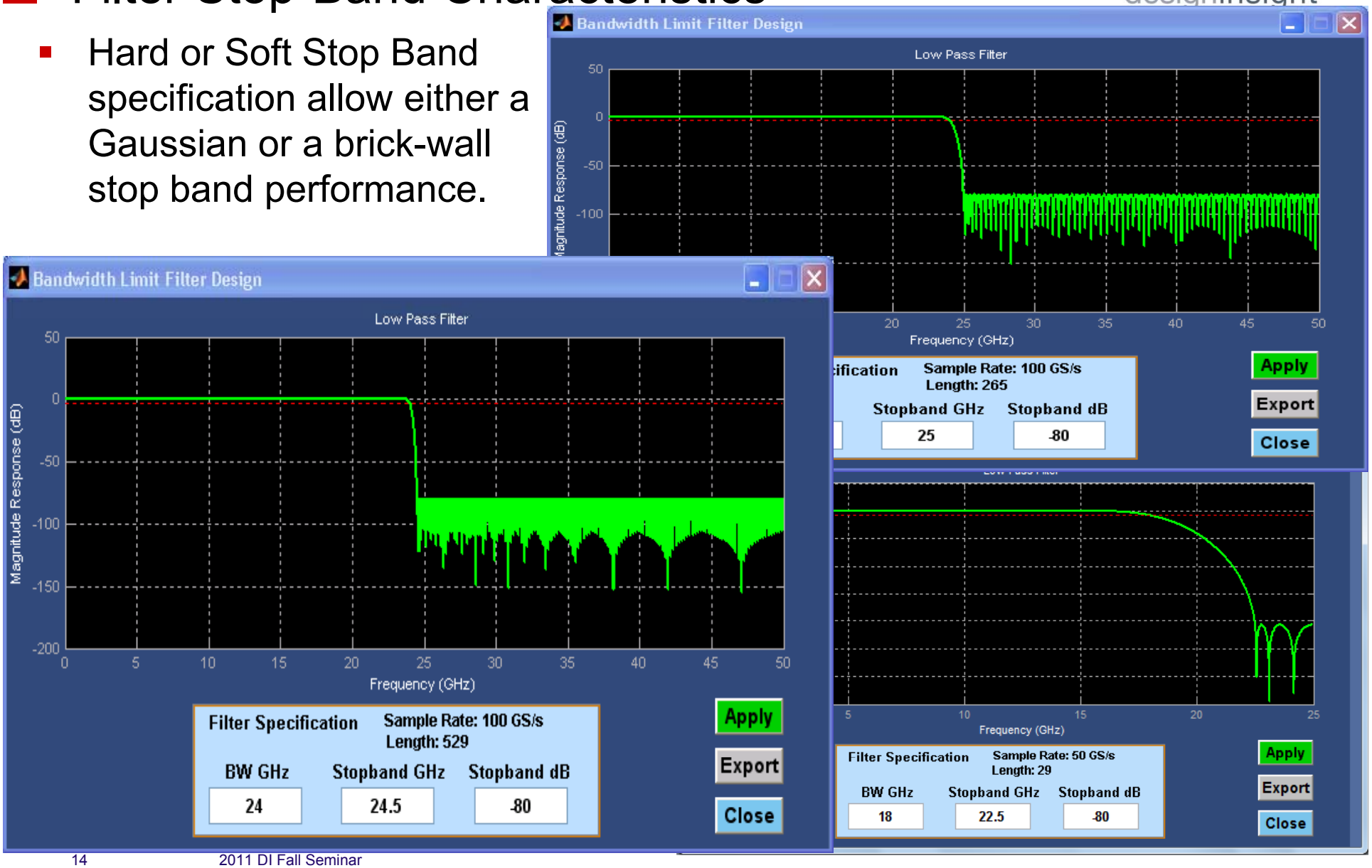
- Hard or Soft Stop Band specification allow either a Gaussian or a brick-wall stop band performance.



Bandwidth
Signal Acquisition and bit rate harmonics

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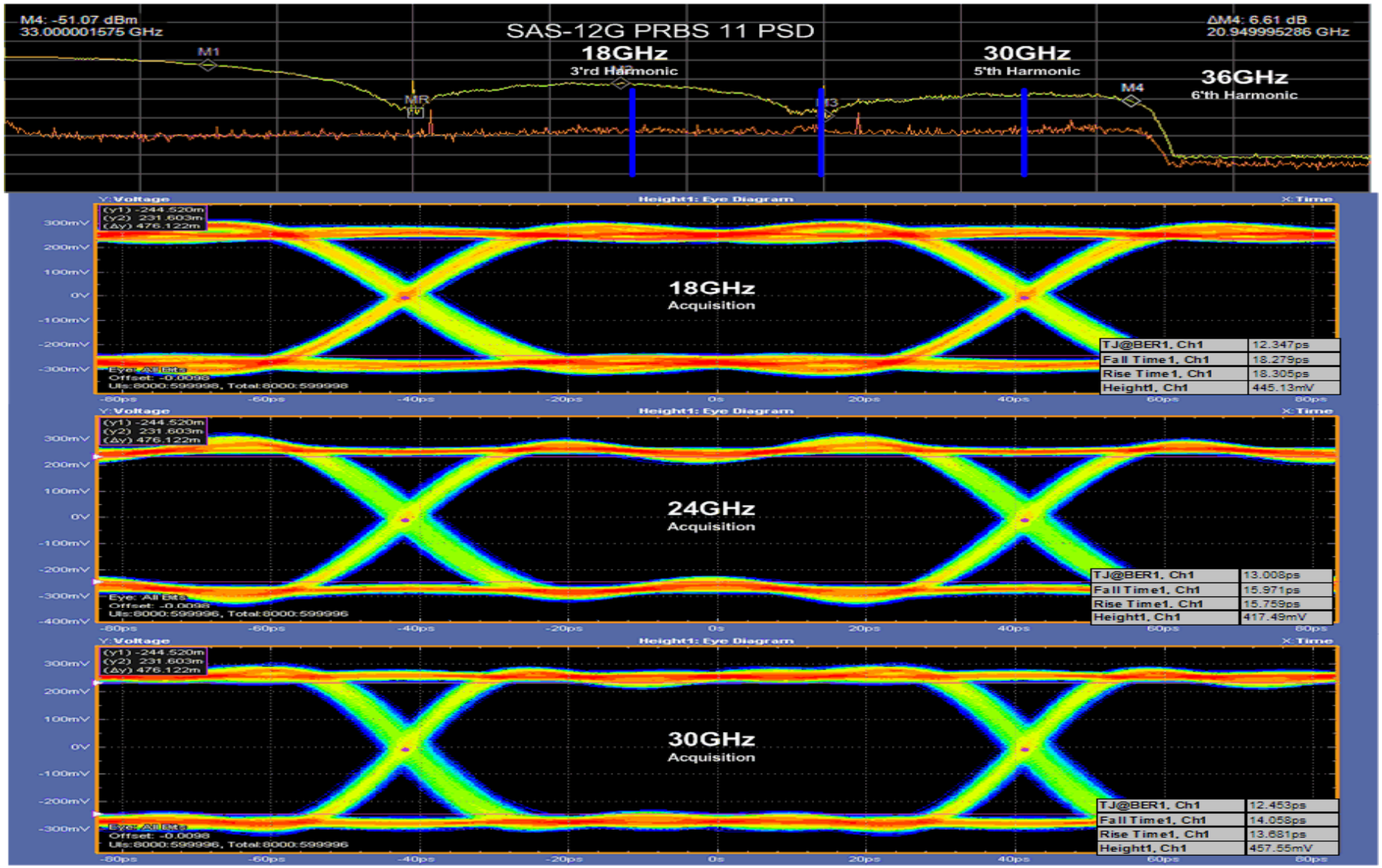

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De-Embed
Transmitter Topology and test points

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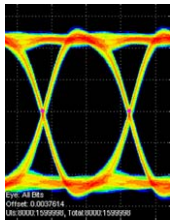
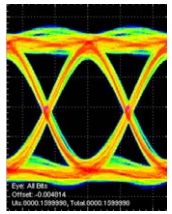
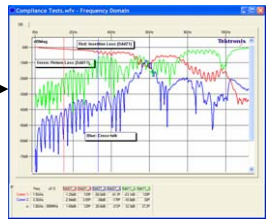
- Base Specification Measurements are defined at the pins of the transmitter
- Signal access at the pins is often not accessible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- S-parameters are acquired on the replica channel



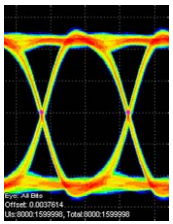
Signal at TX Pins



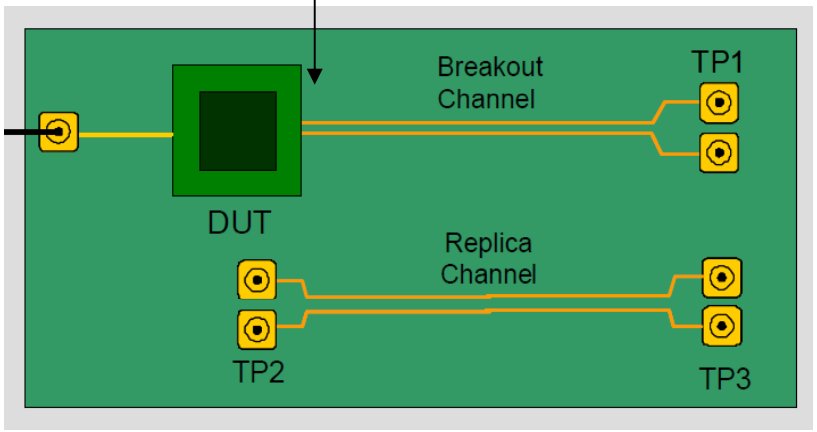
Measured Signal at TP1



Apply S-parameters



Signal with Channel Effects Removed



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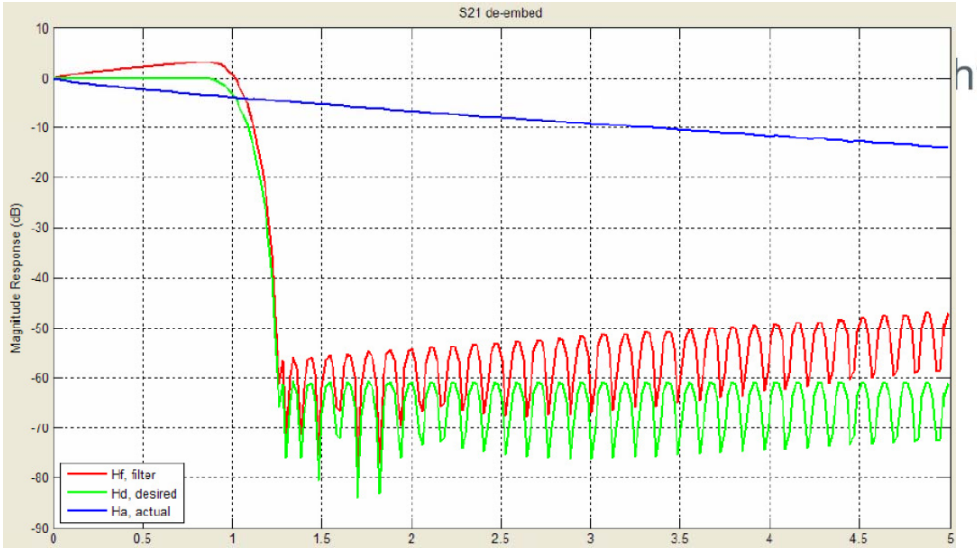
De-Embed Basics



- Classical performance vs robustness design tradeoff
- Performance specification
  - Given closed-loop response, an ideal transfer function with flat response
  - Gain 1 and then steep roll-off to avoid any aliasing and noise amplification
  - Influenced by the quality of the board, noise content of the S-parameter measurements, assumed receiver bandwidth and noise sensitivity.
- Robustness specification
  - How much does the “plant” vary? If we use the same de-embed filter for a slightly different channel than the S-parameters is it stable? Is the performance anywhere close to original objective?
  - Sensitivity to noise
- De-embedding issues
  - Causality, passivity, phase aliasing, interpolation/extrapolation

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De-Embed
Thunderbolt Fixture De-Embed example

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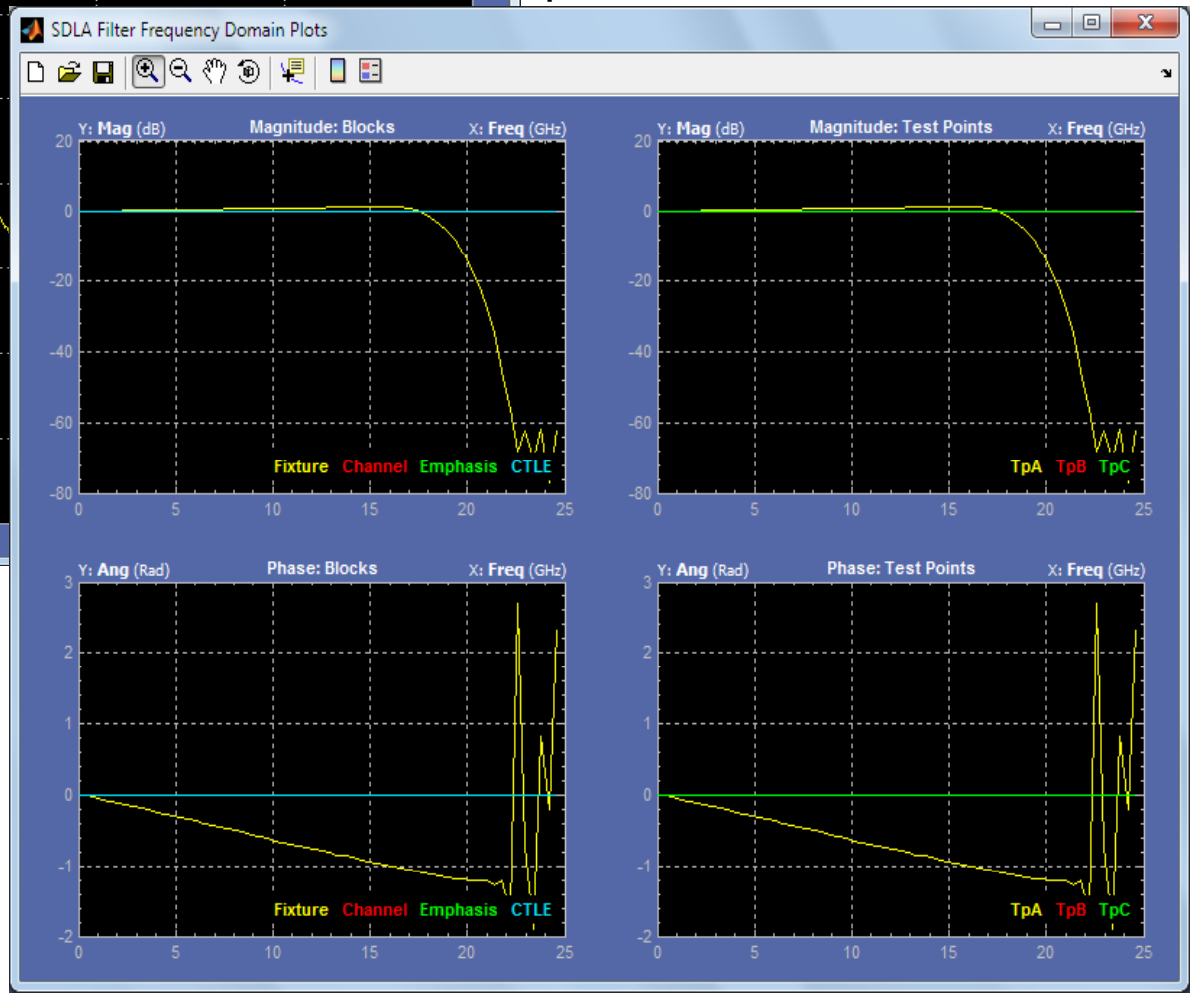
Starting with a Fixtures and Channel's SDD21 profile



- The inverse of this channel response convolved with a user specified stop band provides a de-embed solution which removes "most" of the undesired effects.

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De-Embed
Thunderbolt Fixture De-Embed results

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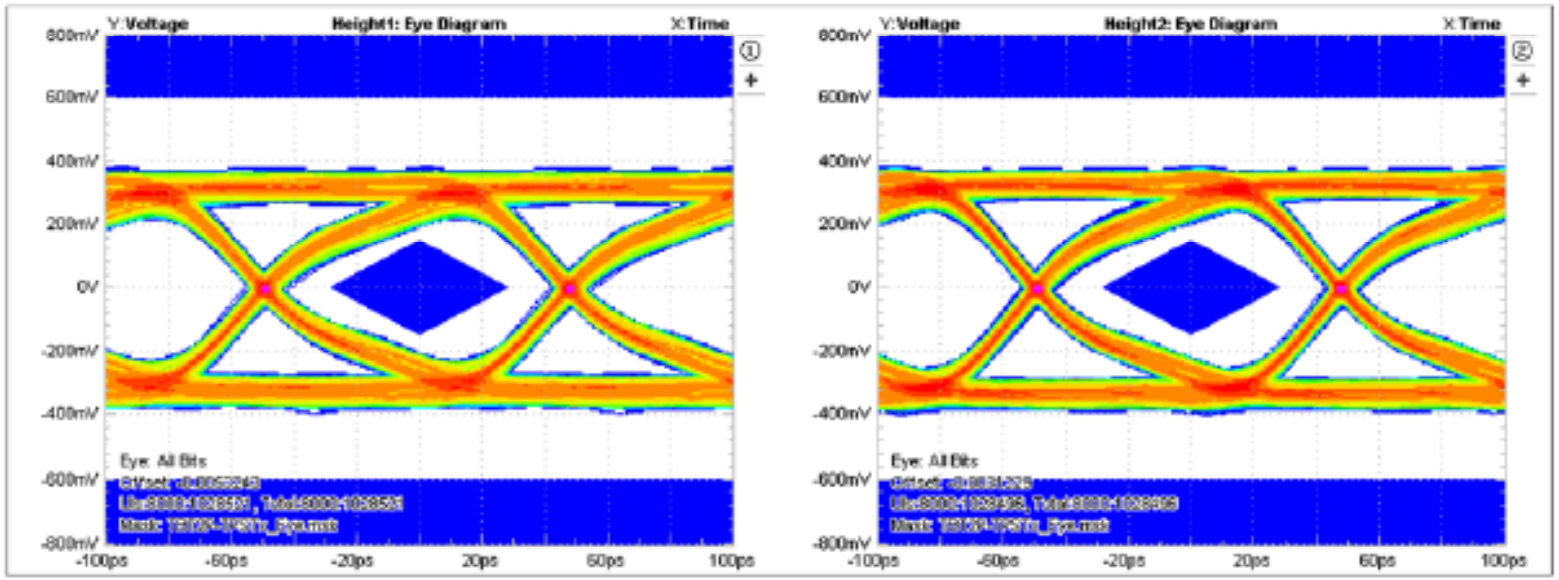
- **Measurement Results**

Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Height1, Math1	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Height2, Math3	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
TJ@BER1, Math1	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
TJ@BER2, Math3	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s

- **Pass/Fail Summary** No pass/fail limits are currently selected.
- **Plot Images**
  - **Measurement Plot(s)**



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Impedance Matching
Re-Normalization

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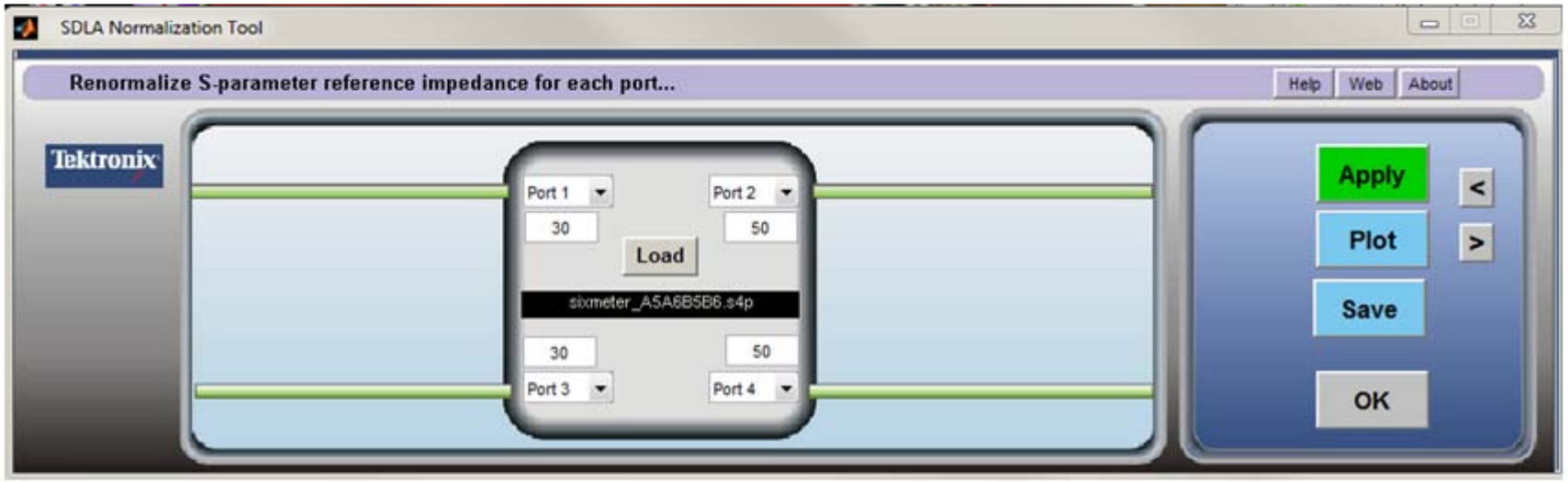
- S-parameters can now be re-normalized
- Click the Tools button on the main SDLA screen (this is in the right panel)
- Click load to load the S-parameter file
- Change the reference impedance (in this example 30ohm)
- Click Apply and then Save. The new S-parameter can now be used in the fixture or channel blocks



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Transmitter Characterization

Transmitter Characterization: Measurements

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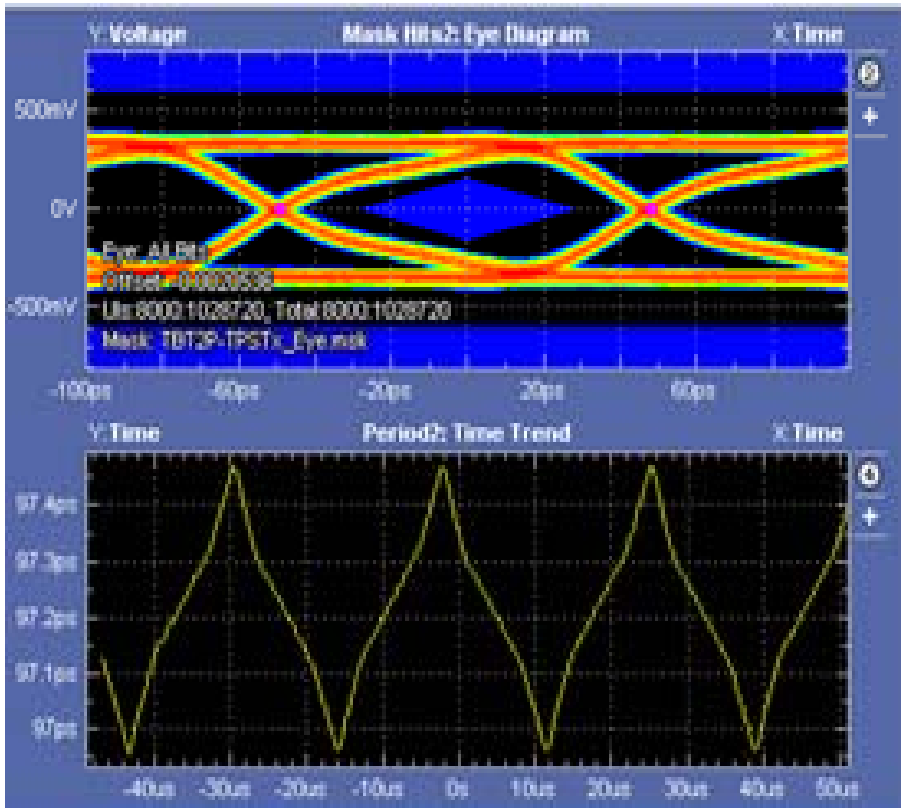
- Most standards call out a wide set of electrical specifications required to ensure product interoperability as Industry and Regional regulations.
- These tests are performed on a wide set of test patterns designed to stress different susceptibilities.
  - Transition Timing (Rise/Fall)
  - Intra-Pair Skew
  - AC Common Mode RMS
  - AC Common Mode Peak
  - JTF Eye Height
  - JTF Eye Width
  - Max Differential Voltage
  - JTF Total Jitter at $10^{-12/13}$ BER
    - Rj, Dj, Tj
  - Unit Interval
  - SSC Modulation Frequency
  - SSC Modulation Deviation



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Transmitter Characterization:
Precise Characterization of Silicon

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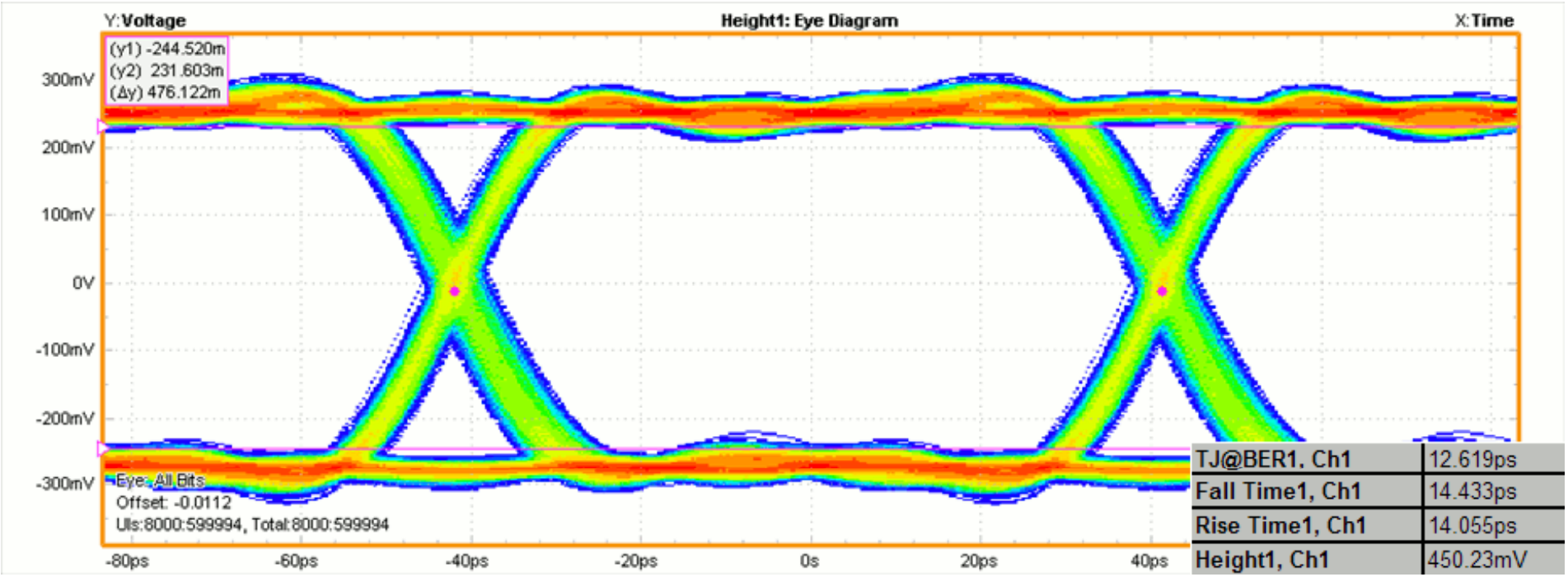

- 33GHz multi-channel acquisition offers 100GS/sec resolution to resolve edges down to 9psec.
- 250M/channel acquisitions.

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Digital Trigger and Data Decode

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Search

Trigger and Search on 8b/10b Buses

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Decode

User customizable multi lane decode.

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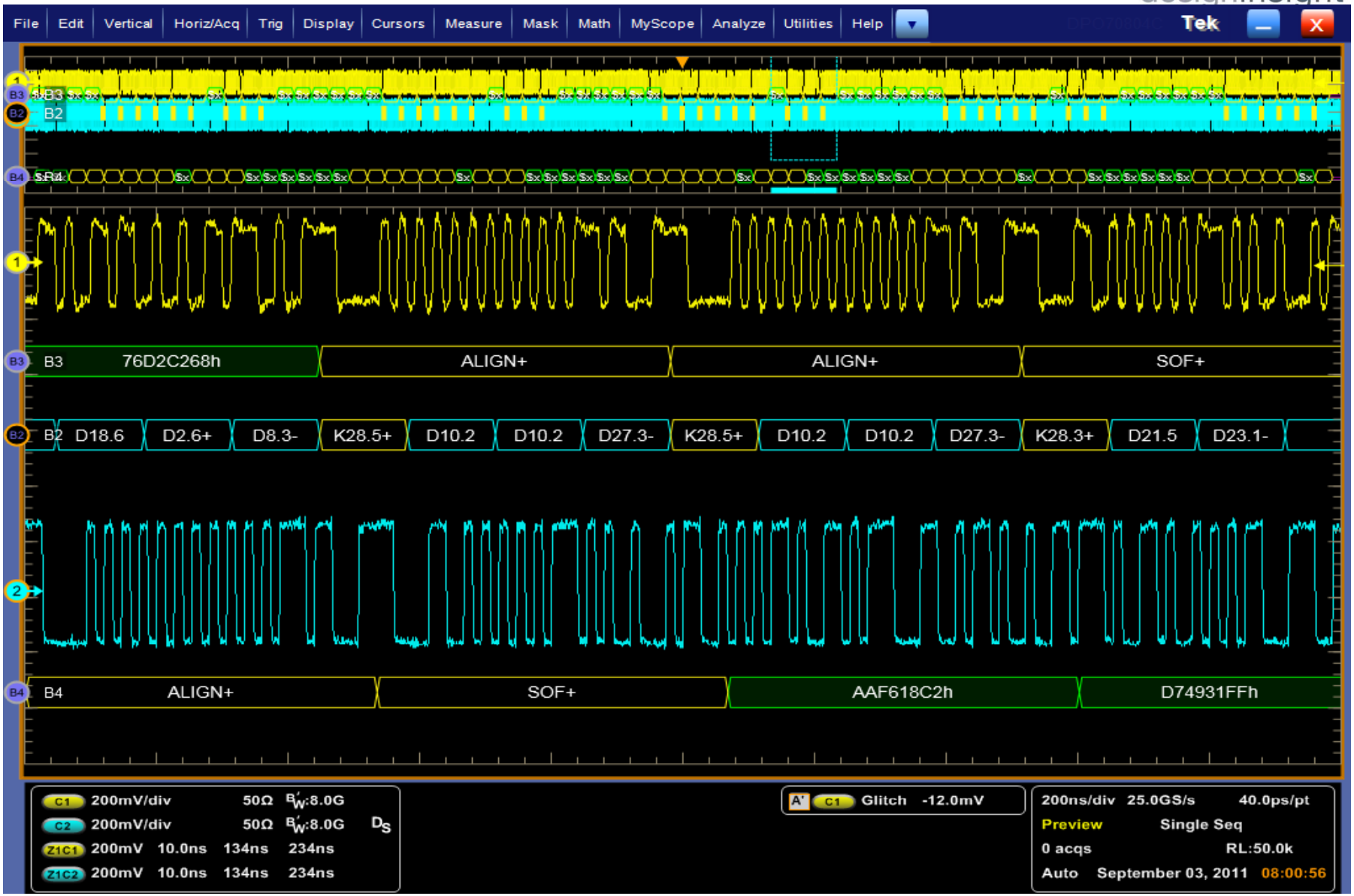

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Emerging High Speed Standards

Emerging Standards

SAS-3

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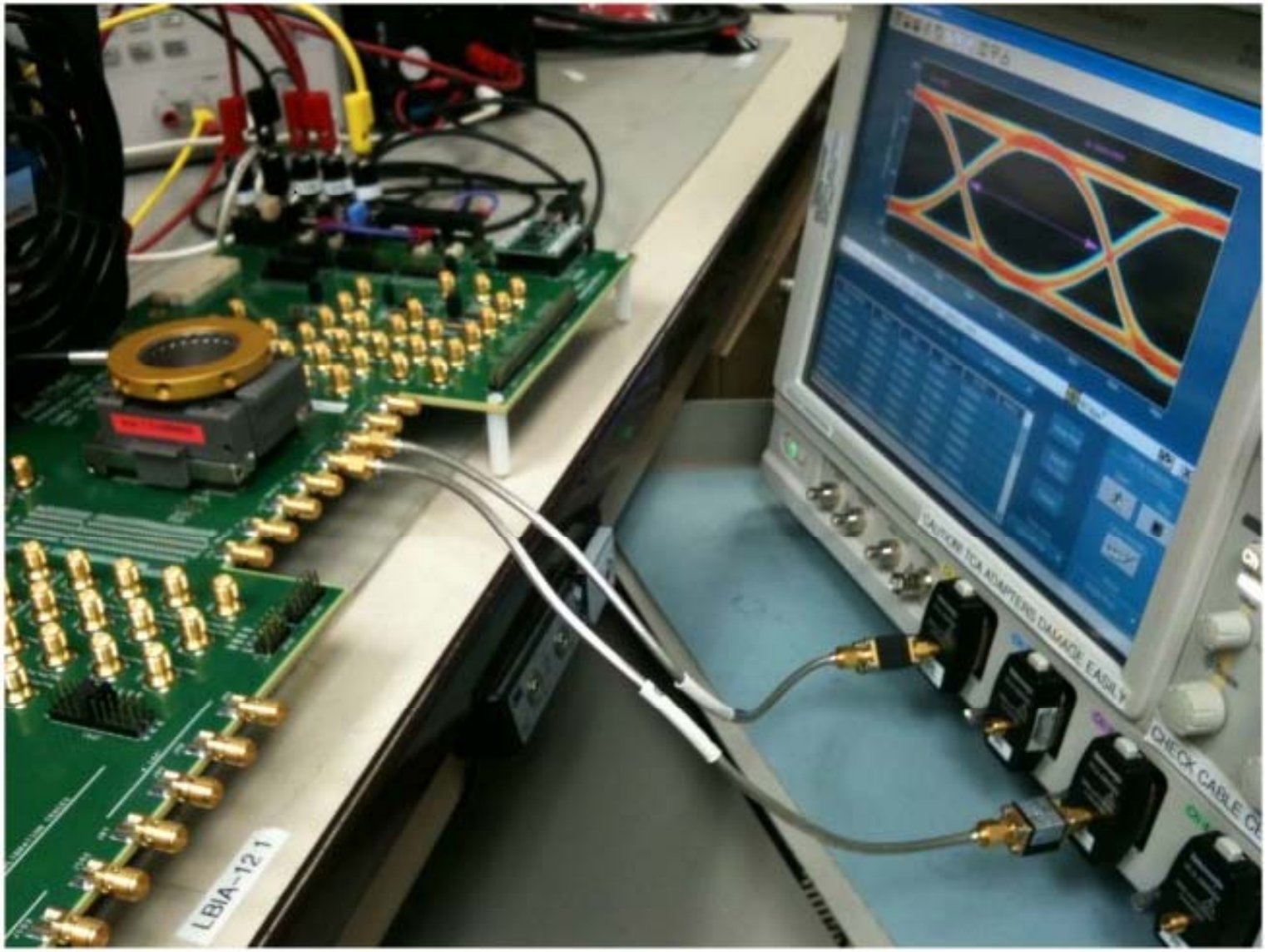

Ref(5): PMC

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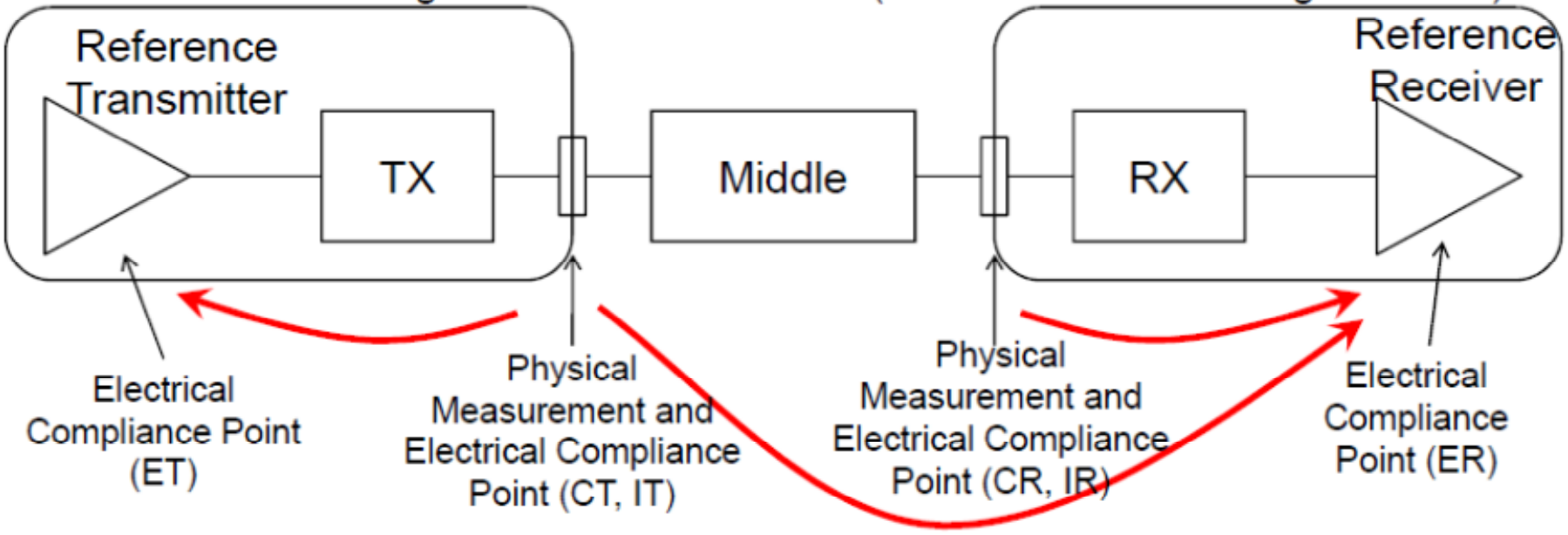
SAS3_EYEOPENING Usage Review
Compliance Points

PMC-SIERRA
Enabling connectivity. Empowering people.

- SAS3_EYEOPENING is used to transform the measurement from a Physical Compliance point into an Electrical Compliance Point
  - CT/IT into ET for TX Equalization & Amplitude
  - CT/IT into ER for TX ISI and crosstalk
  - CR/IR into ER for crosstalk and RX stress pattern calibration and for Middle section ISI compliance
  - De-embedding of test fixture is allowed (other "Probe Point" usage in SAS2)



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Preliminary SAS-3 Tx PreC, PostC Requirements

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Table 34 — Transmitter waveform command set and transmitter circuit response

Description	COEFFICIENT 1[a]	COEFFICIENT 2[a]	COEFFICIENT 3[a]	Vpk(k+1)-Vpk(k) (mV)	v1(k+1)-V1(k) (mV)	v2(k+1)-V2(k) (mV)	v3(k+1)-V3(k) (mV)
Hold	hold	hold	hold	-10 to 10	-10 to 10	-10 to 10	-10 to 10
Increase Pre-Cursor Equalization & Hold Amplitude	dec	dec	hold				
Decrease Pre-Cursor Equalization & Hold Amplitude	inc	inc	hold				
Increase Post-Cursor Equalization & Hold Amplitude	hold	dec	dec				
Decrease Post-Cursor Equalization & Hold Amplitude	hold	inc	inc				

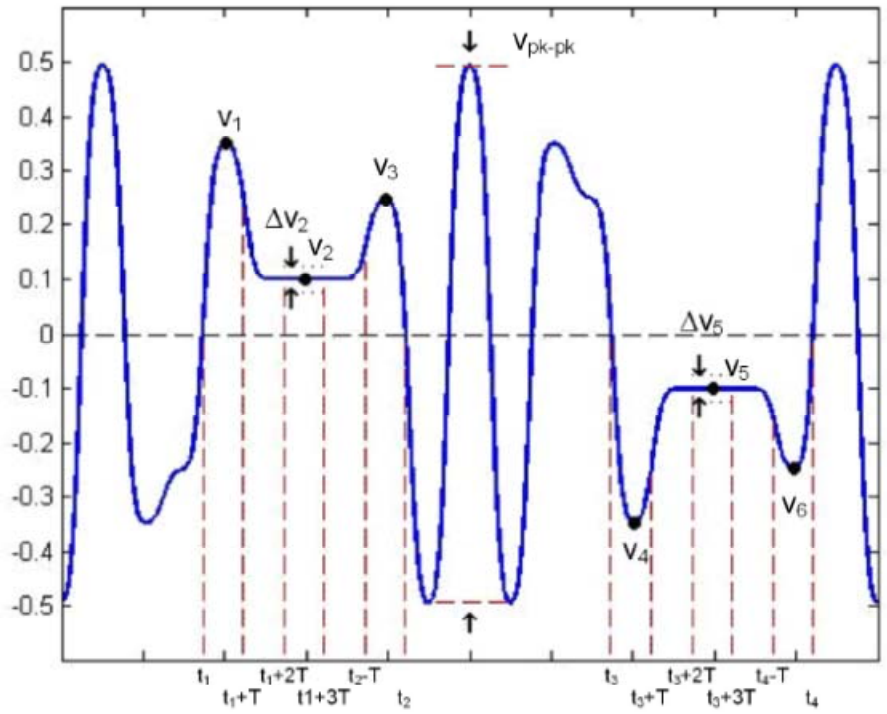

Figure 107 — 12 Gbps Reference Transmitter Circuit Output Waveform

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Post Cursor and signal swing controls in DP12 for reference (Very similar to SAS-3)

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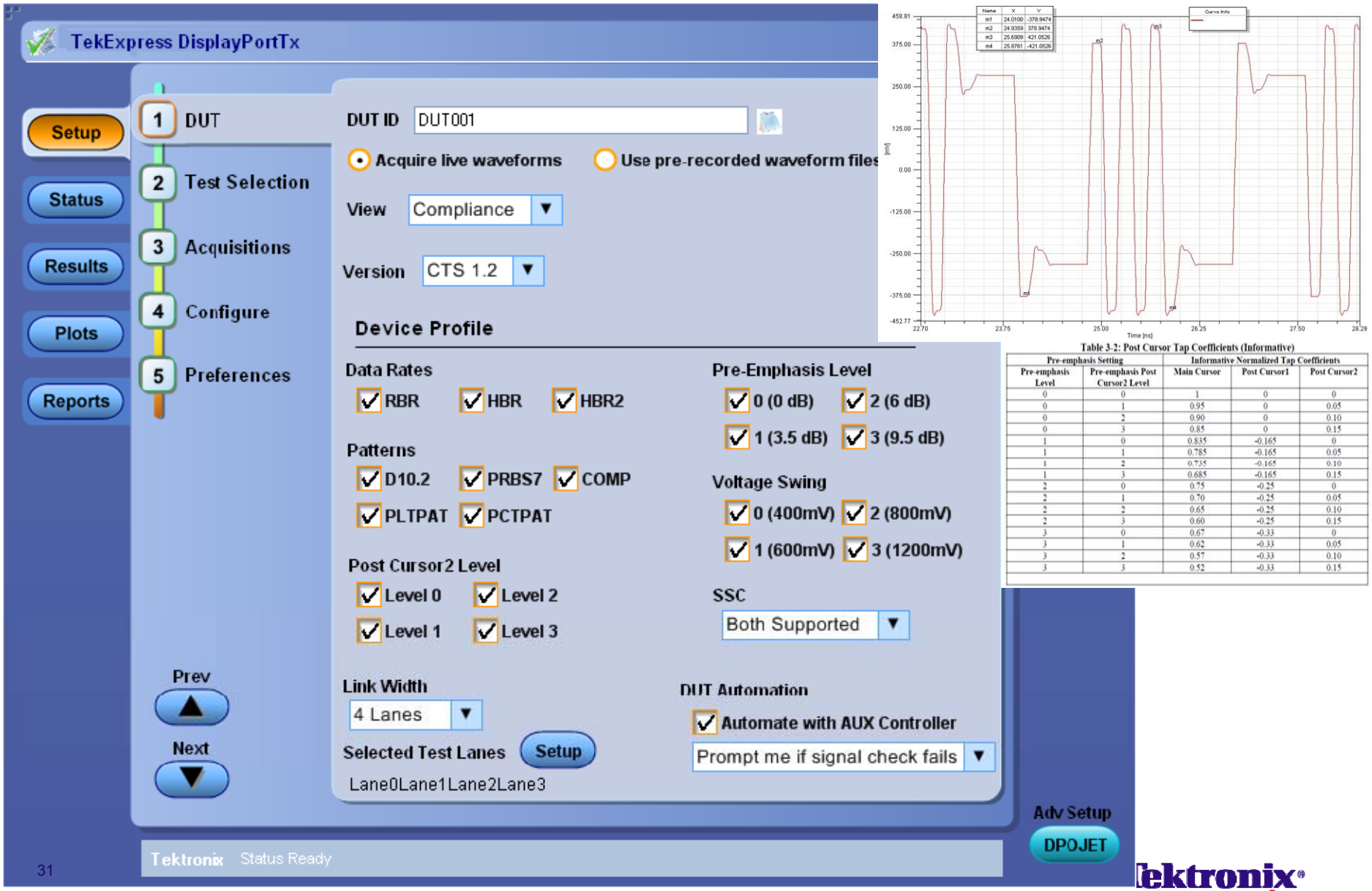

Table 3-2: Post Cursor Tap Coefficients (Informative)

Pre-emphasis Setting		Informative Normalized Tap Coefficients		
Pre-emphasis Level	Pre-emphasis Post Cursor2 Level	Main Cursor	Post Cursor1	Post Cursor2
0	0	1	0	0
0	1	0.95	0	0.05
0	2	0.90	0	0.10
0	3	0.85	0	0.15
1	0	0.835	-0.165	0
1	1	0.785	-0.165	0.05
1	2	0.735	-0.165	0.10
1	3	0.685	-0.165	0.15
2	0	0.75	-0.25	0
2	1	0.70	-0.25	0.05
2	2	0.65	-0.25	0.10
2	3	0.60	-0.25	0.15
3	0	0.67	-0.33	0
3	1	0.62	-0.33	0.05
3	2	0.57	-0.33	0.10
3	3	0.52	-0.33	0.15

Mini-SAS HD Plug Test Adapter Top Views

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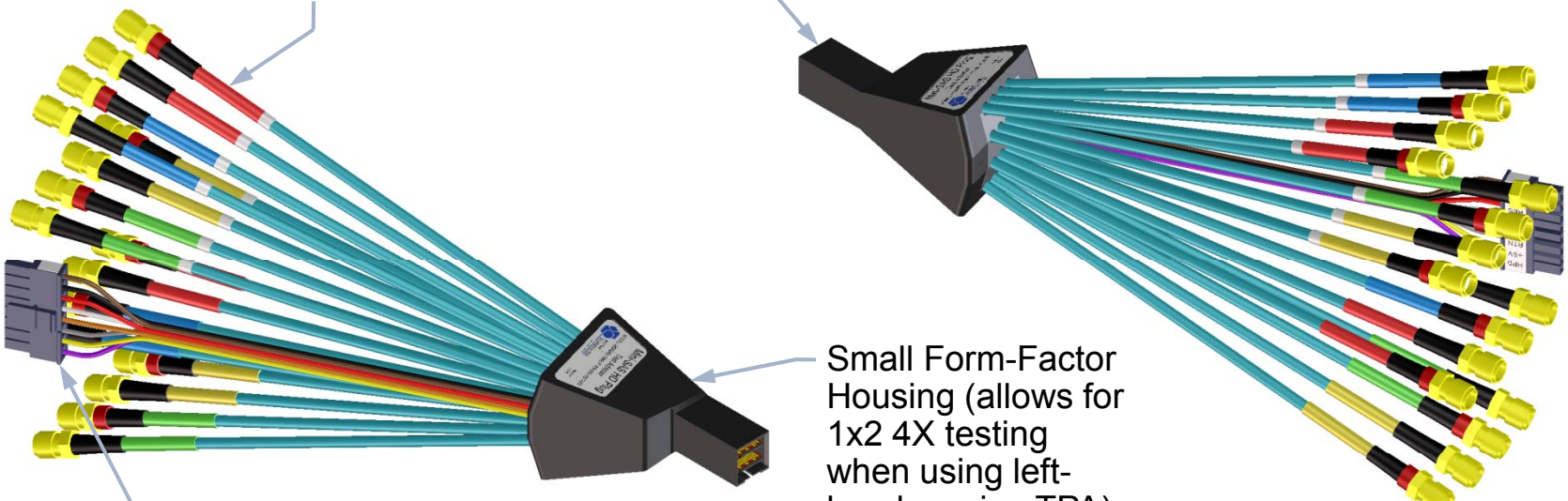

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Emerging Standards

Thunderbolt

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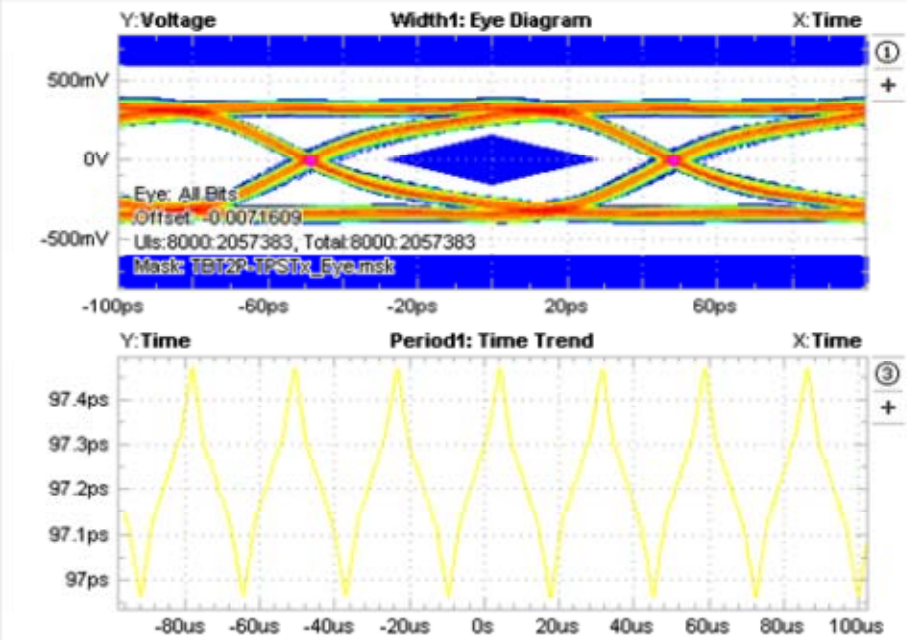

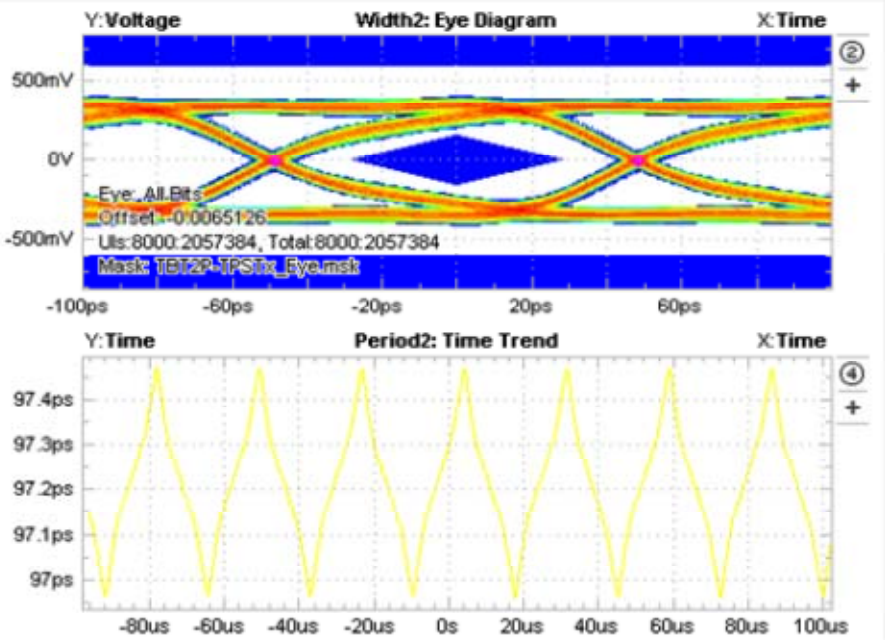

Thunderbolt Overview

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- Thunderbolt signaling is a dual NRZ (64/66b Encoded) 10.3125Gb/sec (Same as SFP+) differential Tx pairs and two differential Rx pairs.
- Instrument BW has been set at 16GHz by Intel. The connectors do not pass significant energy beyond 16GHz, and the noise content beyond 16G is regarded as a significant measurement liability. All instruments will use a hard 16G limit on BW.
- Tektronix and GRL have partnered on test development and efforts towards enabling the Thunderbolt ecosystem with an test MOI which illustrates sanctioned methods of test for Transmitter, Receiver and Channel characterization.
- Intel Thunderbolt Overview with Intel's Jason Ziller: http://www.youtube.com/watch?v=gk69pCcVSSQ

Thunderbolt Transmitter Testing

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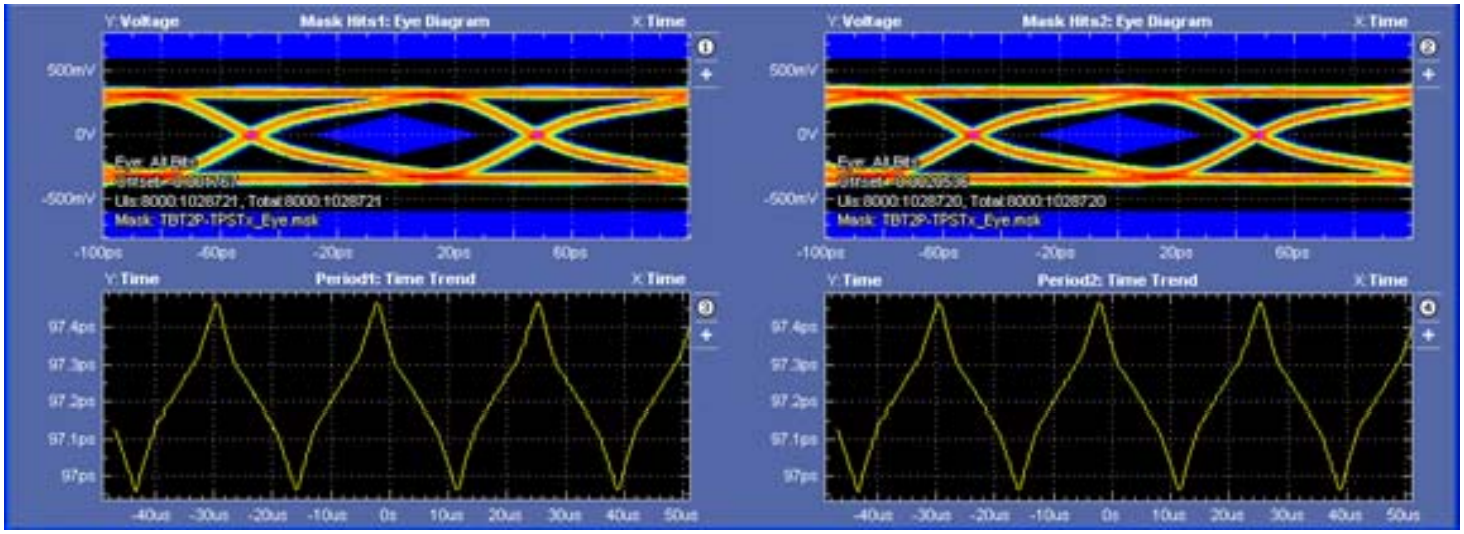

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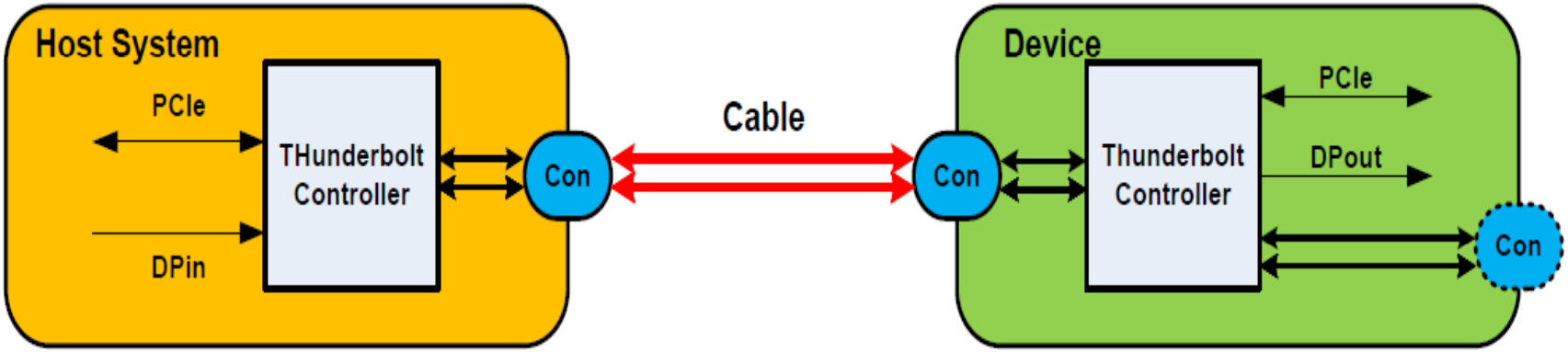
Thunderbolt Transmitter Testing



- One of the key benefits of the Thunderbolt design is an architecture which alleviates needs to perform “Far End” signal integrity analysis as found in other standards such as USB3, SAS, or PCIE.
- The absence of link negotiation and having to deal with the uncertainty of an unknown cable (Channel) and a unknown receiver (Disk Drive for instance) greatly simplifies and improves the link integrity.
  - The Tx system has to manage a fairly simple contract to deliver bits to the connector point with a 1E-12 BER certainty.
  - The Active Cable (which does it’s own smart link negotiation on power up) has an independent contract to deliver bits from one end to the other with a 1E-12 BER certainty.
  - The Rx system has to manage the receipt of the signals to a certainty 1E-12 BER.
- The three independent contracts are designed to work together as a system, but complex system level link negotiation is not required.

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Thunderbolt Receiver: Stressed Pattern Calibration

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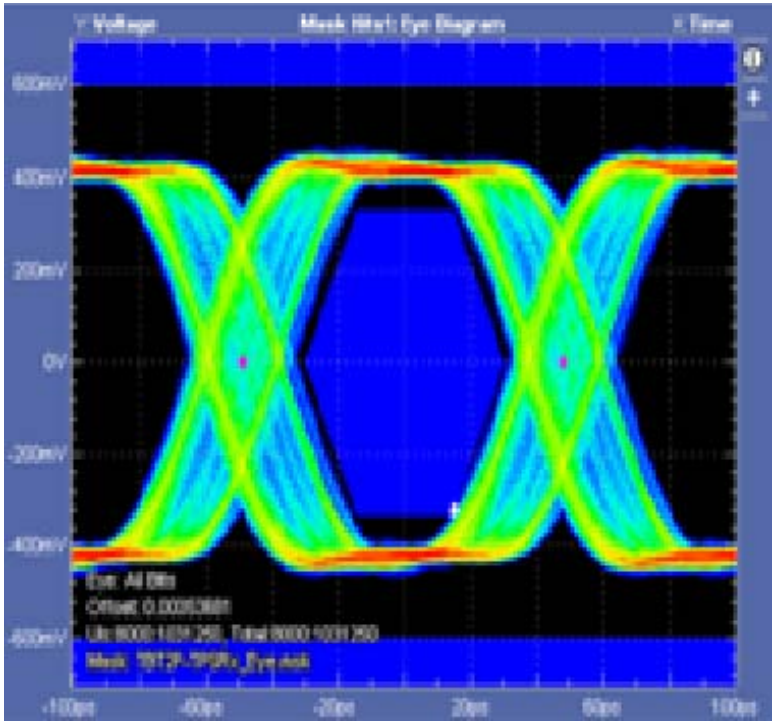
- The Receiver test pattern used in Thunderbolt is a PRBS-31, however the calibration is performed on a PRBS-11 pattern.

Freq	*BERScopeSj*	*DPOJET Measured Pj*
3MHz	*26%*	*310mUI*
4.8MHz	*7%*	*123mUI*
100MHz	*8%*	*128mUI*

Receiver Tolerance	PHY4.1		PRBS-31	TBD	Spec Figure 4-4		UI pp	BSA125C BERTScope
	Receiver Stress Calibration:			SSC			kHz	
				Inner Eye Voltage			mV	
				AC-CM_rms			mV rms	
				AC-CM_pk_pk			mV pp	
				SJ Amplitude				
				3MHz			UI pp	
				4.8MHz			UI pp	
				100MHz			UI pp	
				DDJ			UI pp	
				RJ			UI pp	
				TJ			UI	



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Instrument Considerations

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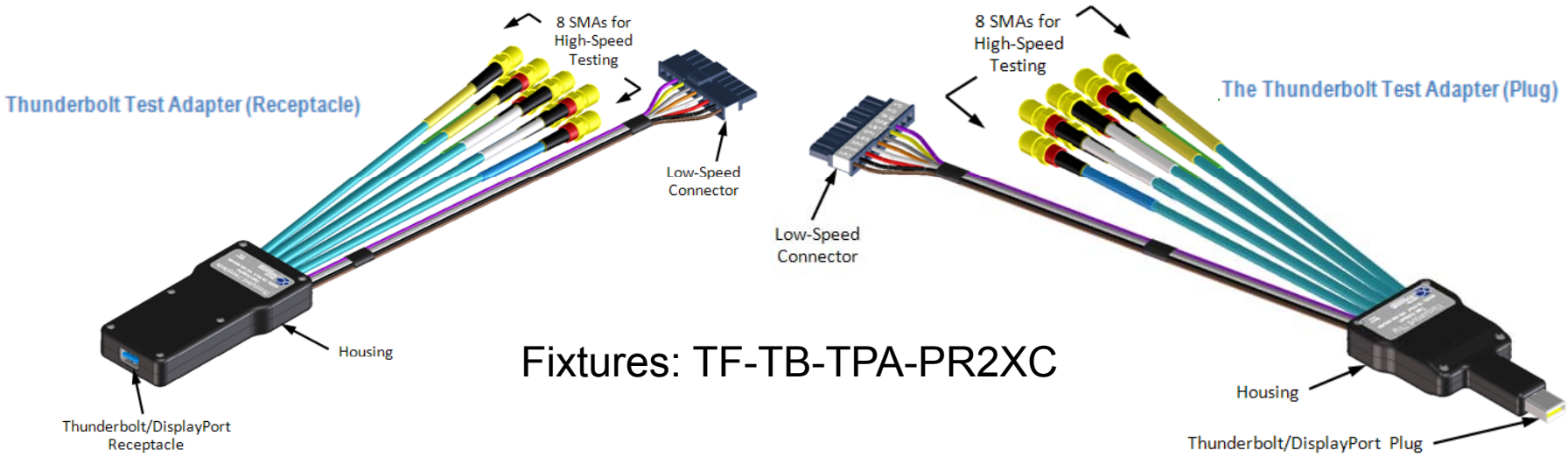
- Phase 0 (Thunderbolt Silicon/System Designers):
  - 30+G Real Time Oscilloscope to Tx Characterization and Rx Calibration
  - BertScope: 12G stimulus and error detector for Receiver Testing/Cable Testing.
- Phase 1-2 (ODM/OEM):
  - 20 GHz Real Time Instrumentation (**De-Embed Stop Band set to 4'th harmonic**)
  - 12.5G BertScope for receiver testing.



Fixtures: TF-TB-TPA-PR2XC

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Thunderbolt Digital Port Micro Controller

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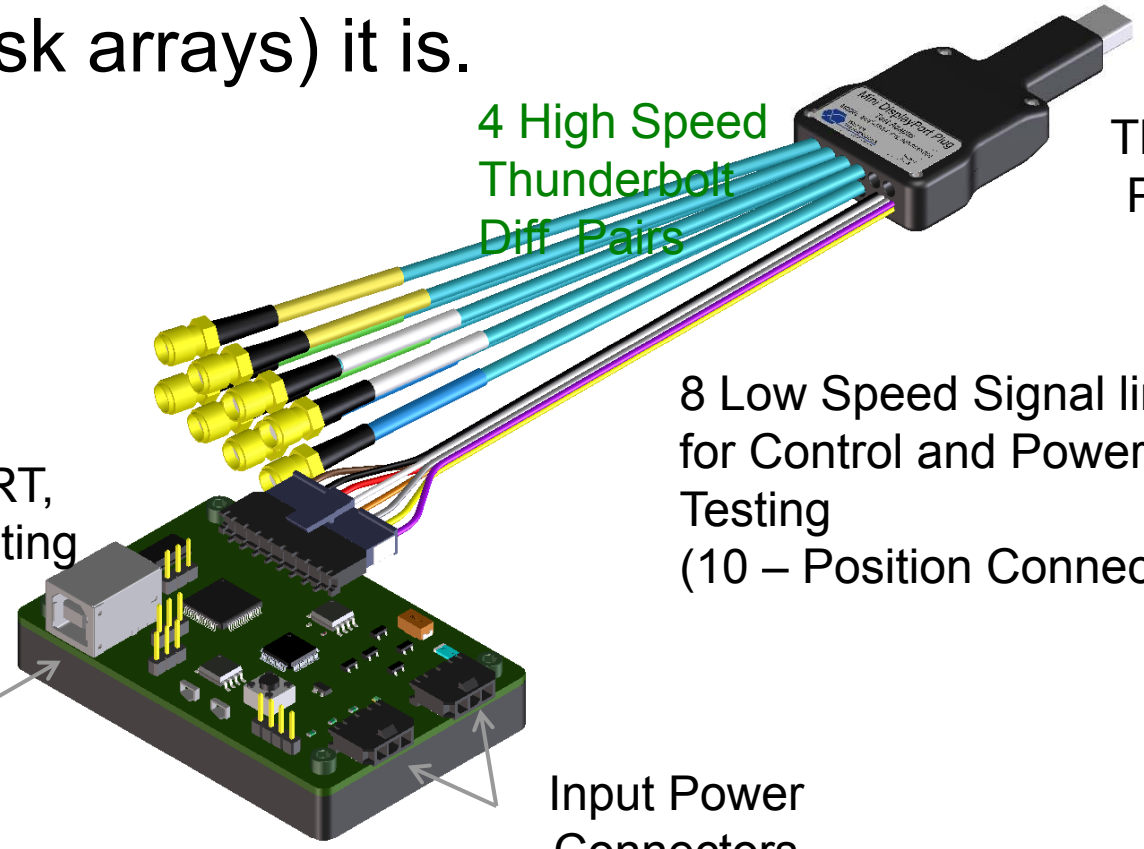
- The Digital Port Micro is responsible for Test Pattern and general state control, as well as error polling in the DUT. For hosts this is not essential but for devices (disk arrays) it is.



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