

High Speed Design Testing Solutions

- Advanced Tools for Compliance, Characterization and Debug



name
title

Agenda

- High-Speed Serial Test Challenges
- High-Speed Serial Test Simplified
 - Characterization
 - Debug
 - Compliance
- Measurement Example: PCI Express®

Tektronix and the Digital Age



Wireless Everywhere

Enabled by
Digital RF
Technologies



Video Explosion

Enabled by
Digital Video
Technologies



Accelerating Performance

Enabled by
High Speed Serial
Technologies



Pervasive Electronics

Enabled by
Embedded Systems
Technologies



Next Generation Networks

Enabled by
Growing Wireless
Users & Convergence

High-Speed Serial Trends and Implications



Industry/Technology/Market Trends

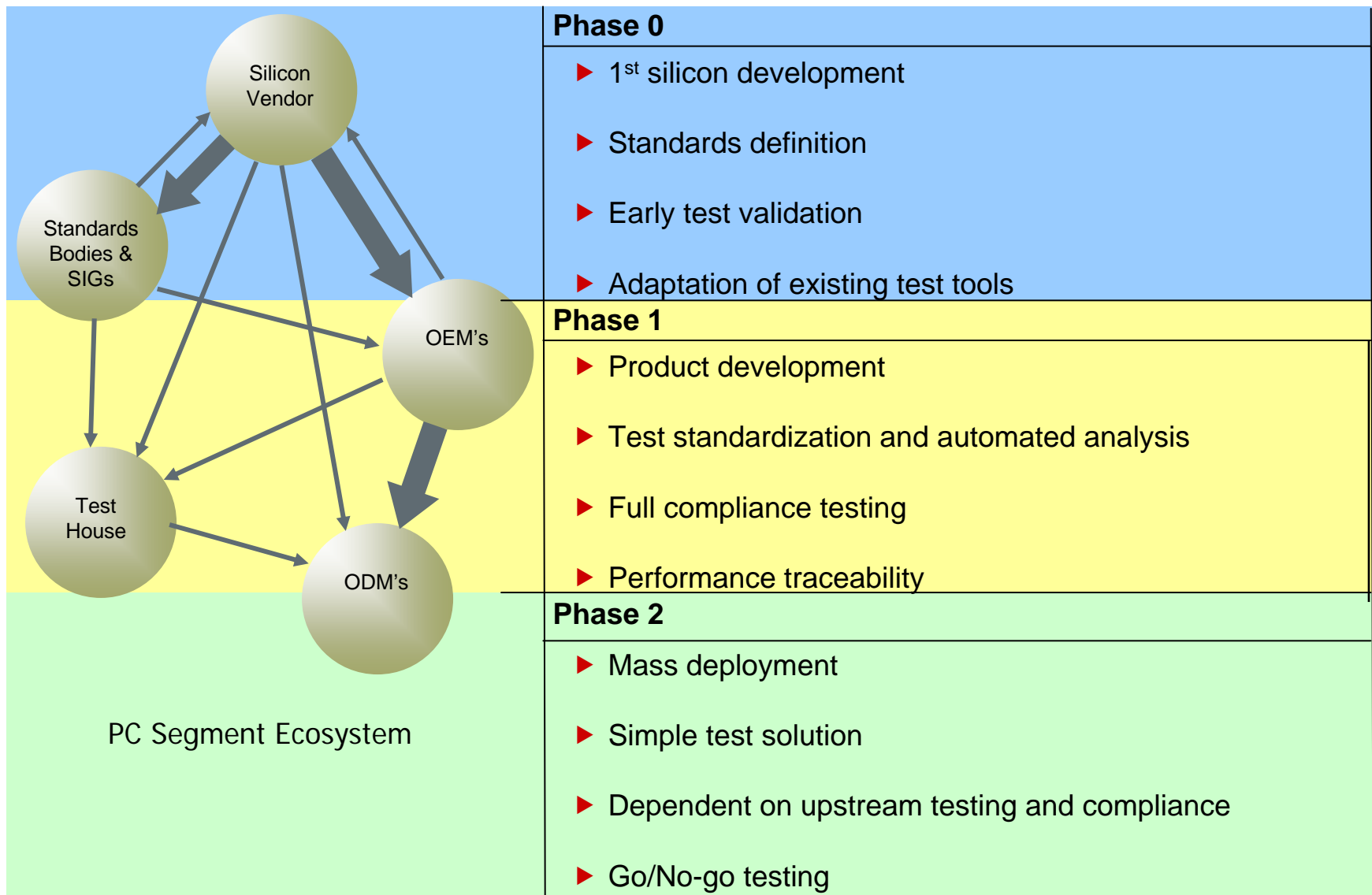
- Interfaces have moved from parallel to high-speed serial implementations
- Data transfer rates continue to increase: 3 \Rightarrow 6 \Rightarrow 10 \Rightarrow 12 Gb/s
- Industry standardization for plug-and-play interoperability
- Consumer electronics becoming a bigger driver

Implications for Test & Measurement

- Giga-bit data rates require higher performance instruments
- Industry standards are defining stringent measurement and analysis requirements
- Complete system testing of transmitter, receiver and transmission path or cable
- Requires broad product portfolio and more automation of compliance testing
- T&M role in standards bodies is key

Digital World Drivers – Accelerating Performance

HSS Industry Ecosystem – Standard Evolution

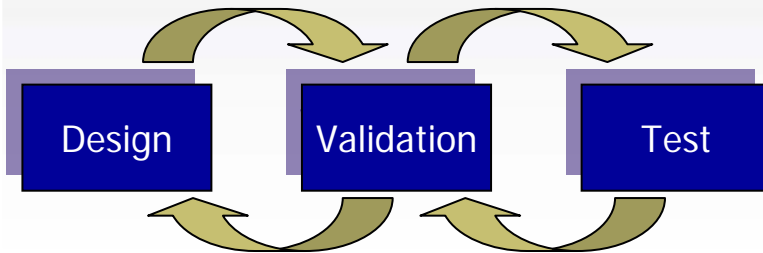


Digital World Drivers – Accelerating Performance

Serial Data Design and Test Challenges

Engineering Test Challenges

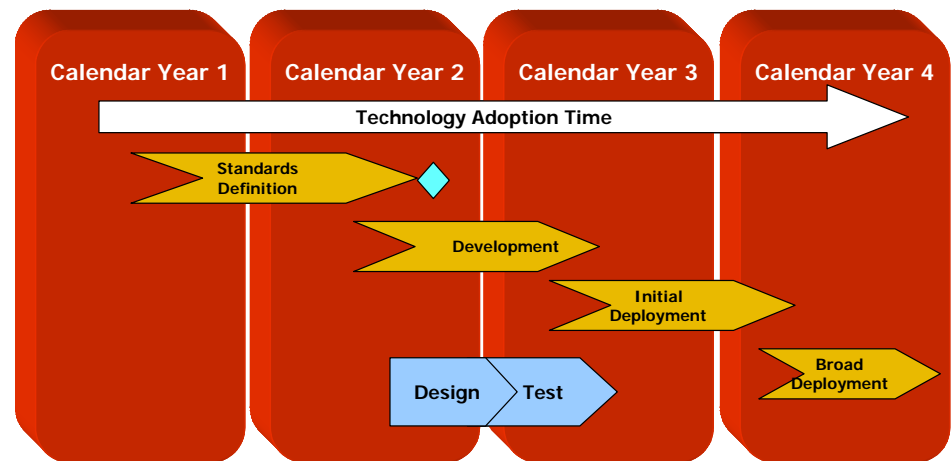
- Shorter development time
 - Aligned to market and new technologies
- Design correlation between simulation and test
- Gigabit data rates reduce design margins
- “Signal integrity” measurement and analysis
- Conformance to industry standards



Signal integrity is biggest of many design problems



Source: EE Times survey

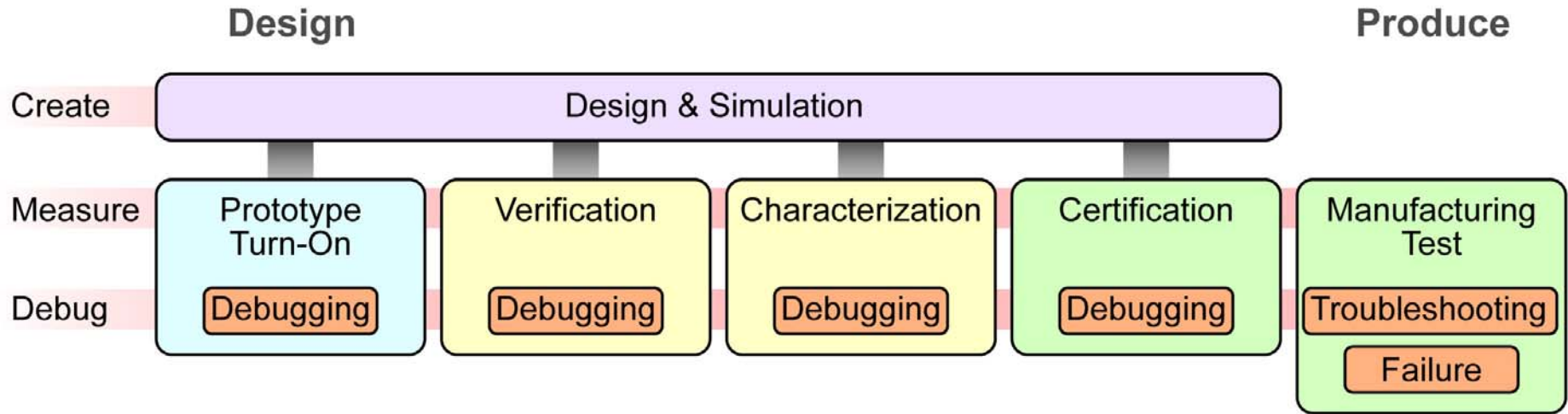


"The speeds and layout techniques involved [in high speed serial] make debug almost impossible"

Agenda

- High-Speed Serial Test Challenges
- High-Speed Serial Test Simplified
 - Characterization
 - Debug
 - Compliance
- Measurement Example: PCI Express

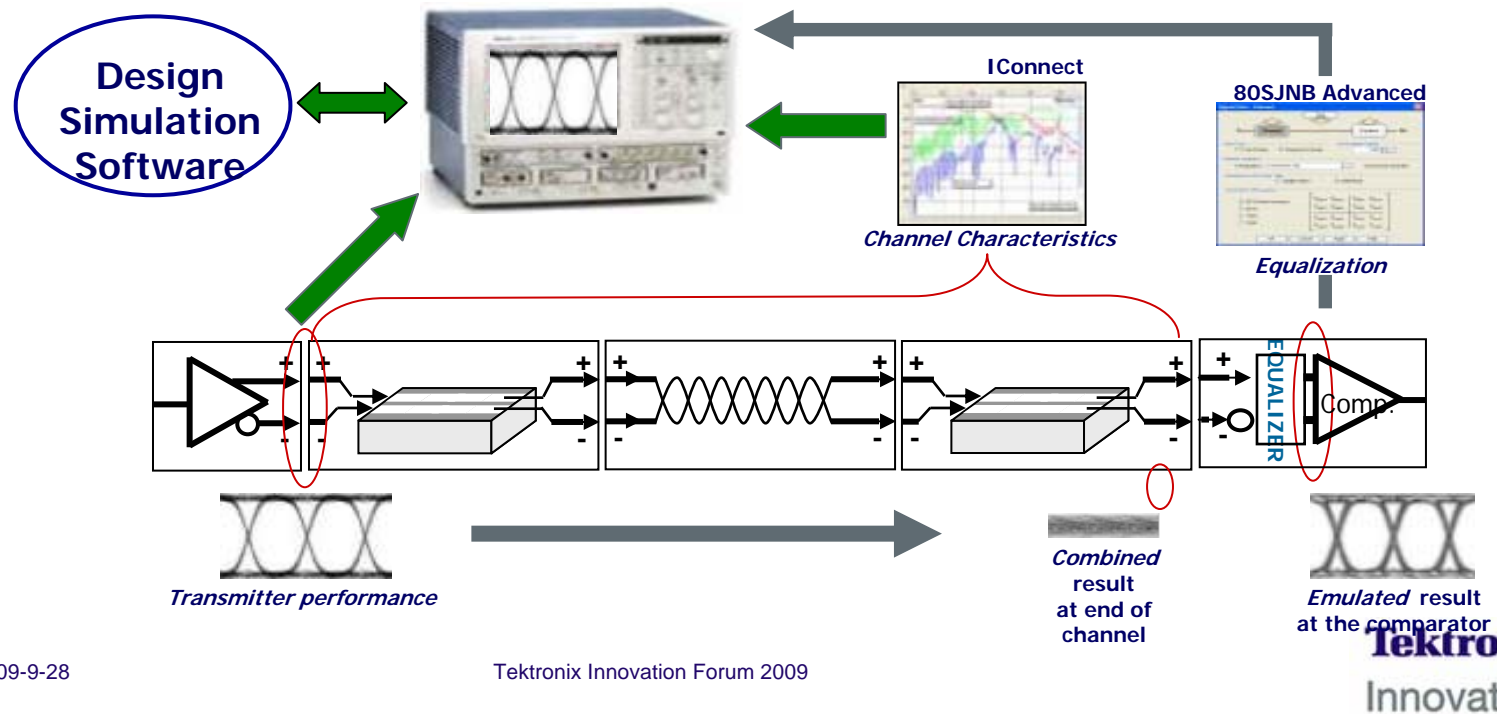
High Speed Design Process



| | |
|---------------------------|--|
| Prototype Turn-on | Establish prototype “vital signs” to assure safe and expected operation |
| Verification | Signal integrity and timing analysis, discovery of issues under nominal conditions |
| Debug | Identify root cause of signal and system issues |
| Characterization | Characterize circuit behavior under range of conditions; margin testing |
| Certification | Testing for certification to an industry or internal standard |
| Manufacturing Test | Testing to production requirements |
| Troubleshooting | Isolating root cause of defective unit (verified design, broken product) |
| Failure Analysis | Post-production analysis of defective unit to improve design |

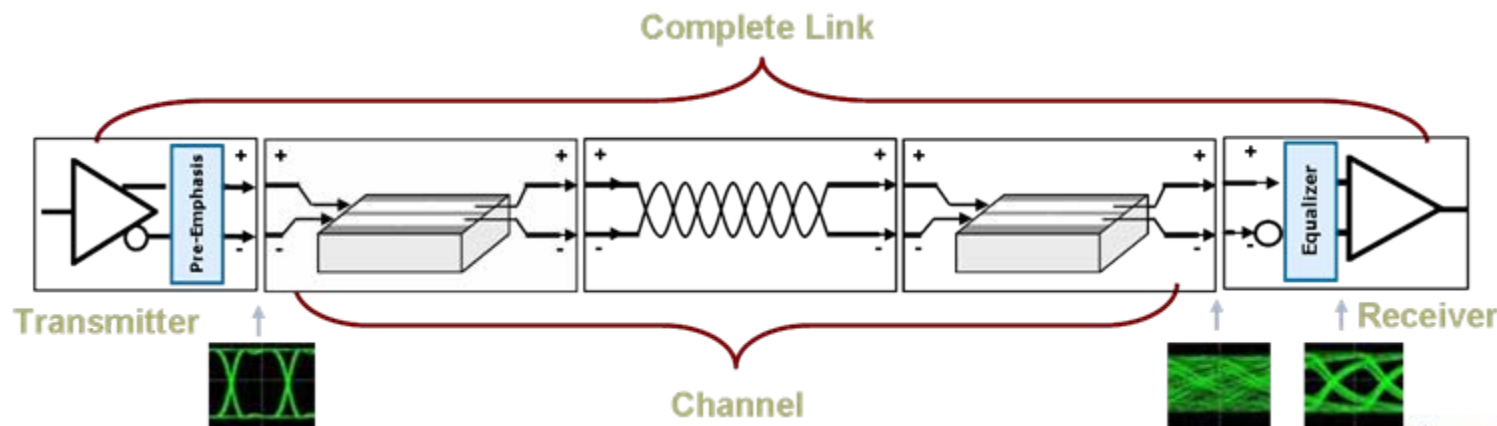
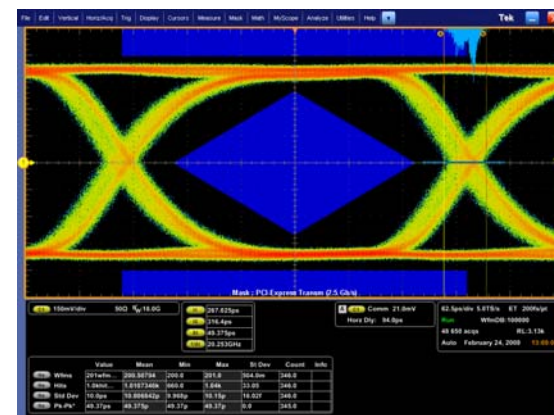
Design Characterization

- Quantify performance limits
- Precise understanding of circuit behavior under range of conditions
- Margin Analysis
 - Parameter variation: voltage, process, temperature
 - Correlate test results to simulation models and update models if necessary
 - Validate margins before handing off to manufacturing



Trends in Physical Layer Testing

- Traditional methods
 - Basic amplitude and timing measurements
 - Mask and template testing
 - Histogram-based jitter measurements
- Emerging requirements
 - Link analysis with equalization
 - S-Parameter-based de-embedding
 - Channel emulation (Compliance Interconnect Channel)
 - Jitter and noise separation



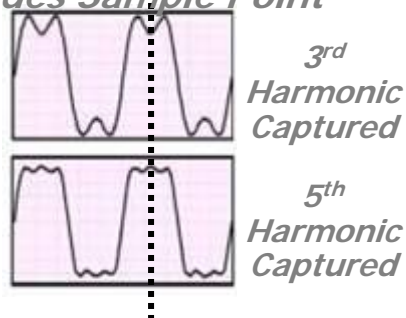
New Digital World Drivers – Accelerating Performance

Gigabit Data Rates Require High-Bandwidth Test

| Serial Bus Data Rate | Fundamental Frequency | 3 rd Harmonic | 5 th Harmonic |
|----------------------------|-----------------------|--------------------------|--------------------------|
| 2.5 Gb/s (PCI-Express) | 1.25 GHz | 3.75 GHz | 6.25 GHz |
| 3.0 Gbps (SATA II) | 1.5GHz | 4.5 GHz | 7.5 GHz |
| 3.125 Gbps (XAUI) | 1.56 GHz | 4.69 GHz | 7.81 GHz |
| 4.25 Gb/s (Fibre Channel) | 2.125 GHz | 6.375 GHz | 10.625 GHz |
| 4.8 Gb/s (FBD) | 2.4 GHz | 7.2 GHz | 12.0 GHz |
| 5.0 Gb/s (PCI-Express 2.0) | 2.5 GHz | 7.5 GHz | 12.5 GHz |
| 6.0 Gb/s (SATA III) | 3.0 GHz | 9.0 GHz | 15.0 GHz |
| 6.25 Gb/s (2x XAUI) (CEI) | 3.125 GHz | 9.375 GHz | 15.625 GHz |
| 6.4Gb/s (Front Side Bus) | 3.2 GHz | 9.6 GHz | 16.0 GHz |
| 8.0 Gb/s (Front Side Bus) | 4.0 GHz | 12.0 GHz | 20.0 GHz |
| 8.0 Gb/s (PCI-Express 3.0) | 4.0 GHz | 12.0 GHz | 20.0 GHz |

- ▶ GHz bandwidth performance ensures signal fidelity
- ▶ Provides critical accuracy for characterization and analysis
- ▶ Ensures complete testing of design margins
- ▶ Tektronix DSA72004B is only 20 GHz real-time scope to support next generation signal capture to the 5th harmonic

Serdes Sample Point



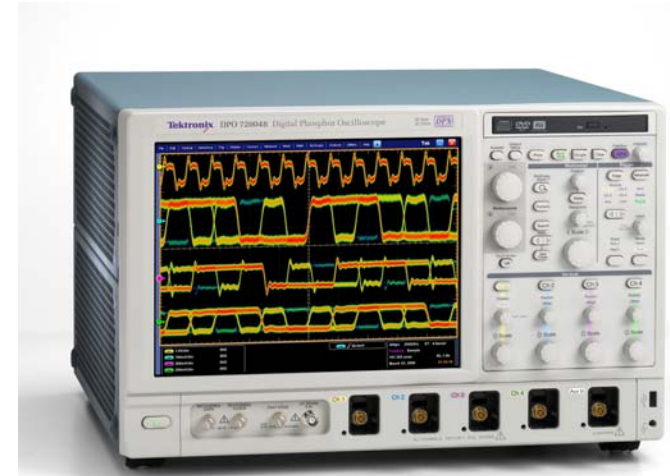
| DUT Signal | Measurement System Bandwidth Required | | |
|--------------------------|---------------------------------------|-------------|-------------|
| Rise/Fall time (20%-80%) | 10% Accuracy | 5% Accuracy | 3% Accuracy |
| 50 ps | 8.0 GHz | 9.6 GHz | 11.2 GHz |
| 40 ps | 10.0 GHz | 12.0 GHz | 14.0 GHz |
| 30 ps | 13.3 GHz | 16.0 GHz | 18.7 GHz |
| 20 ps | 20 GHz | 24 GHz | 28 GHz |

Powerful Signal Acquisition

Introducing

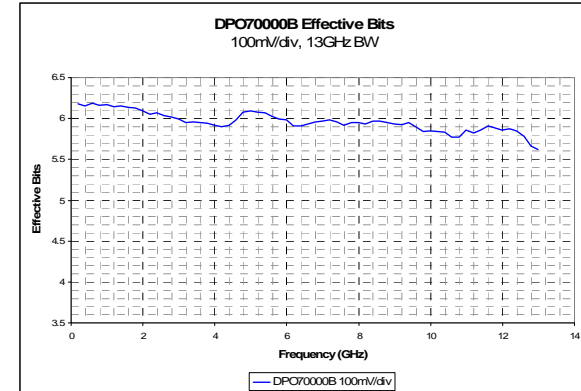
World's Fastest Oscilloscopes Enhanced for Next Generation Serial Data Analysis

- **NEW: Industry's Lowest Vertical Noise, Highest Number of Effective Bits (ENOB) and Flattest Frequency Response**
 - More margin to allow your test to pass
- **Complementing Industry's Leading Oscilloscope**
 - Up to 20GHz and 50GS/s for 5th harmonic measurements for data rates up to 8Gb/s on all 4 channels
 - Reduce debug time with industry's highest waveform capture rate >300,000 wfm/s
 - Increase your measurement margin with industry's lowest jitter noise floor

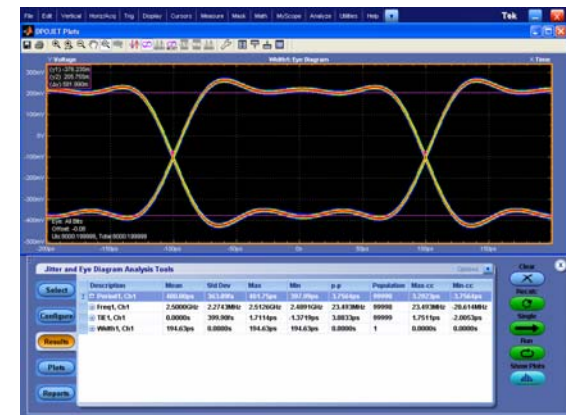


Highest Performance for Emerging Technologies

- Enhanced Signal Integrity for Serial Data Measurements
 - Industry's best Effective Number of Bits (ENOB)
 - Flattest Frequency Response
 - Lowest noise floor
- Higher data rates = less available margin. Tek gives some of that margin back!
- New High Speed Serial Standards Require Test Instrumentation With Higher Signal Fidelity, Able to Capture a TRUE Representation of the Test Signal



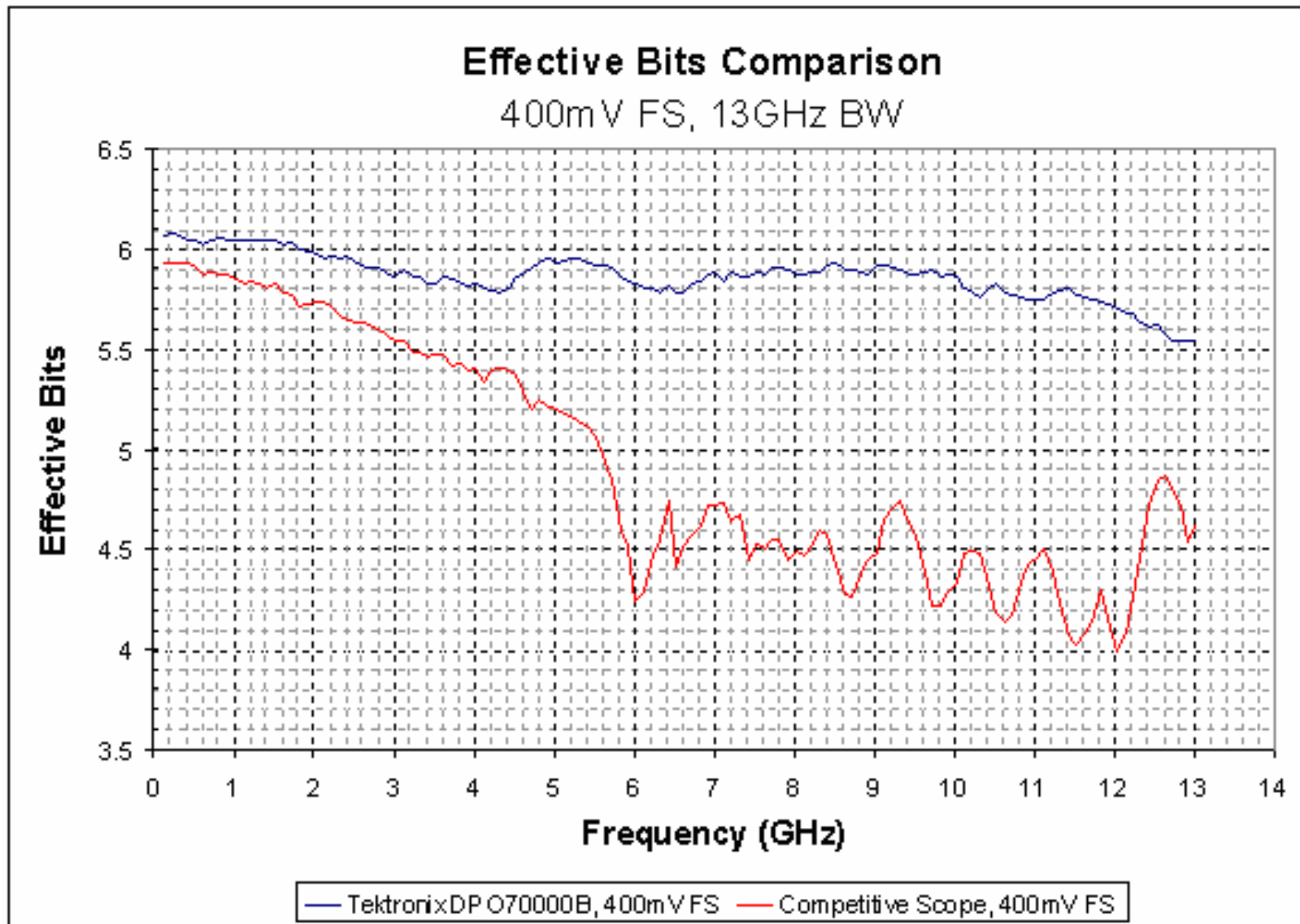
Maximize test margins through the industry's best signal integrity and signal fidelity



Enhanced Signal Integrity for Data Measurements

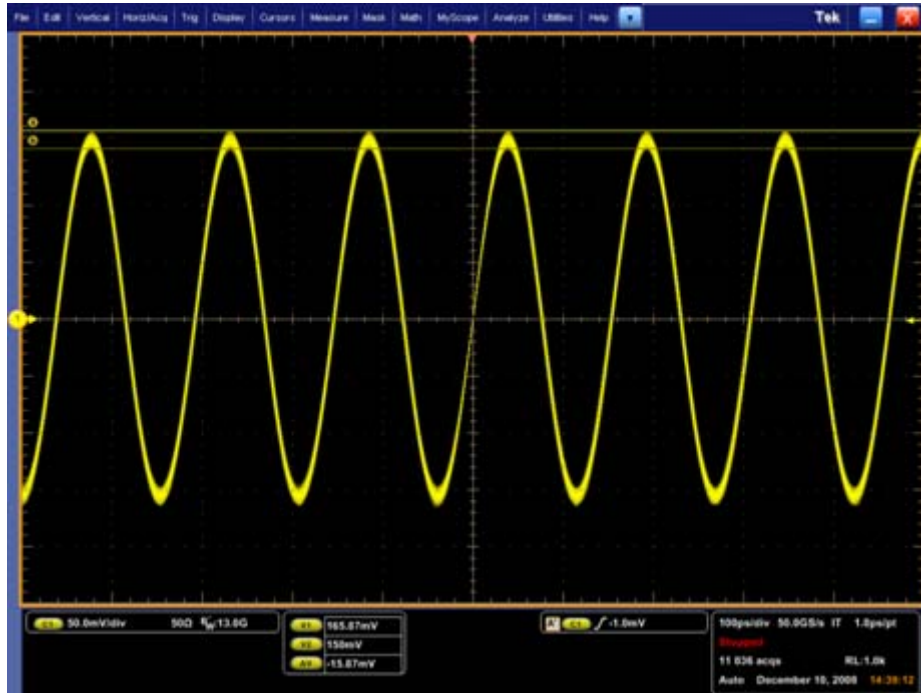
The Industry's Best Signal Integrity with Less System Noise

- Comparison of DPO70000B to Competitive Scope

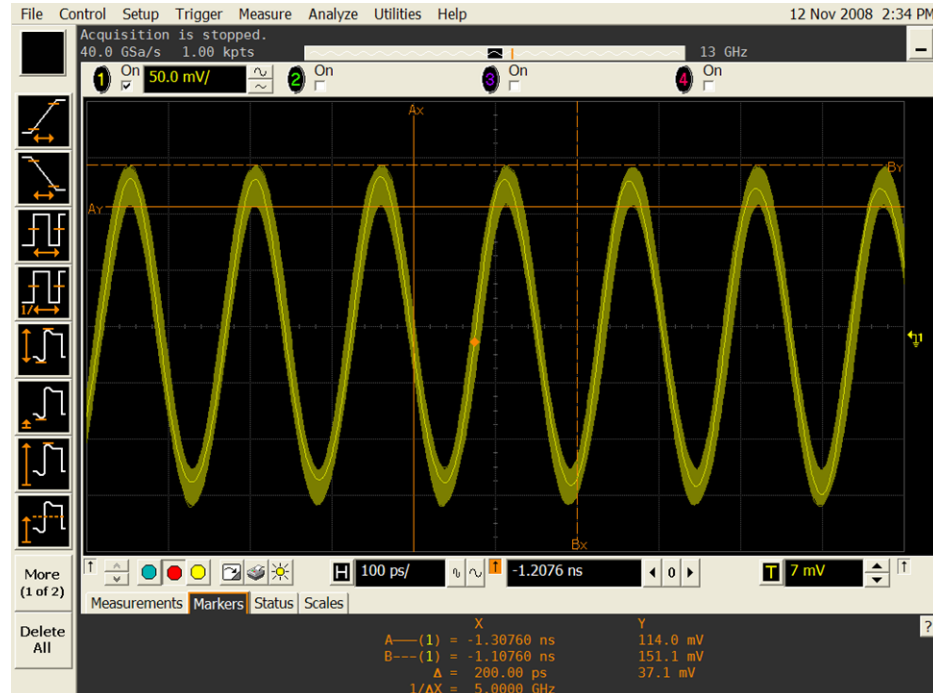


Highest Performance Industry's Lowest Noise Floor

Tektronix DSA70000B



Alternative solution



Higher data rates = less available margin

*New High Speed Serial Standards
Require Test Instrumentation With Higher
Signal Fidelity, Able to Capture a TRUE
Representation of the Test Signal*

*6.5GHz sine wave of identical source
same settings used on both instruments*
Measured noise:

Tektronix = 15.9 mV pk-pk

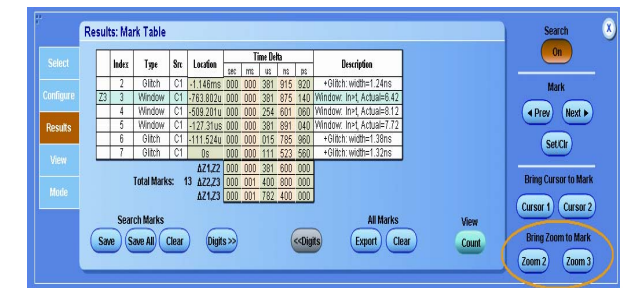
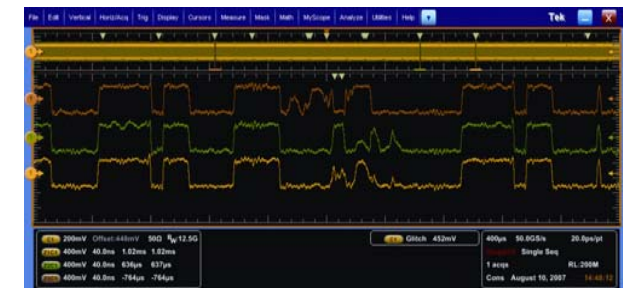
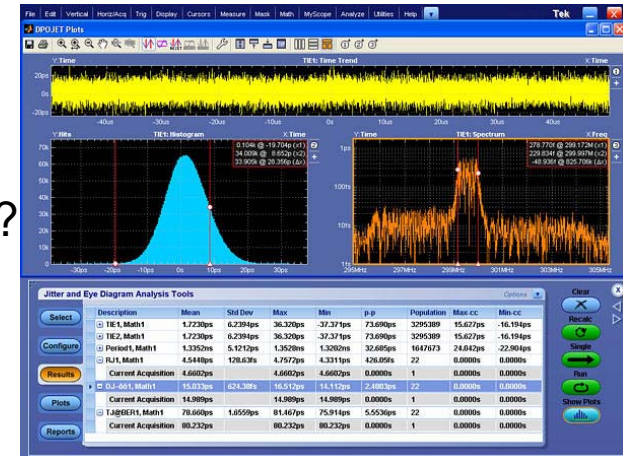
Alternative = 37 mV pk-pk

Agenda

- High-Speed Serial Test Challenges
- High-Speed Serial Test Simplified
 - Characterization
 - Debug
 - Compliance
- Measurement Example: PCI Express

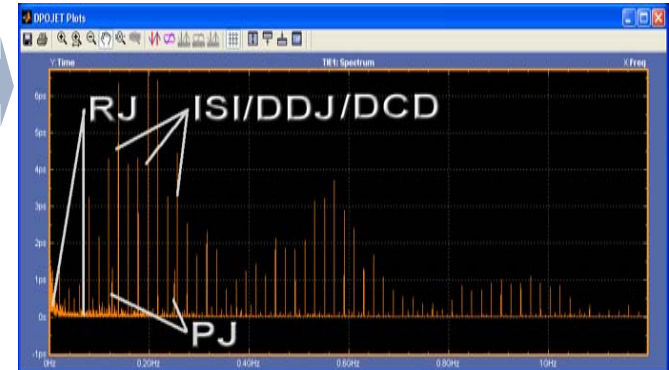
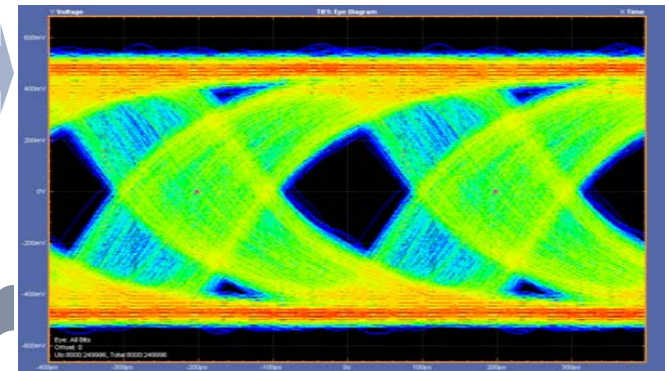
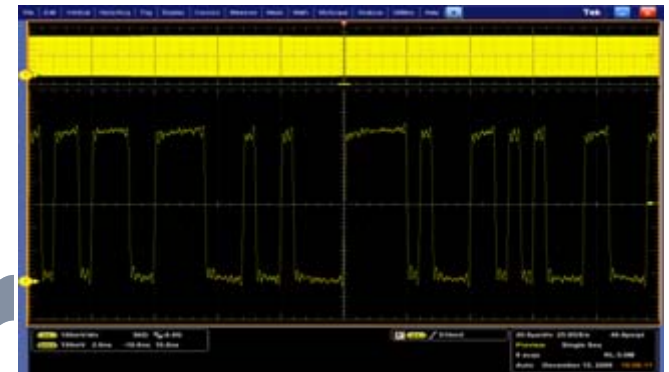
High Speed Serial Debug Tools

- Issues manifested in different layers of the protocol stack
 - Crosstalk, jitter, reflections, skew
 - Disparity, encoding or CRC errors
- Where do I start debugging? What tools are available?
- DPOJET Jitter and Eye Tools
 - Fast jitter measurements with 'One Button' Jitter Wizard
 - Compare timing, jitter, eye, amplitude measurements with user-definable clock recovery, filters, pass/fail limits, and reference levels
- PinPoint™ Triggering
 - HW Serial trigger for data rates up to 5 Gb/s
 - Over 1400 combinations of Sequence A-B triggers
- Advanced Search and Mark
 - Scan data for multiple events and mark each one
 - Quickly jump from event to event for more efficient navigation
 - Pass event timestamps into DPOJET and analyze only areas of interest



Data Visualization with DPOJET

- Deep memory capture
 - Long records needed for low frequency events (SSC, periodic jitter, low speed clocks)
 - Frequency window related to time capture
 - 1 SSC cycle (33kHz) => Need 30us time record
- Eye Diagram Analysis
 - Quick visual indicator of voltage and timing performance
 - Related to Bit Error Rate (BER)
- Jitter Decomposition
 - Knowledge of jitter types and sources aids in debug
 - Common jitter sources
 - Power supply coupling
 - PLL (tracking or overshoot)
 - Limited channel bandwidth and reflections (ISI)
 - Driver imbalance (Rise/fall time asymmetry)



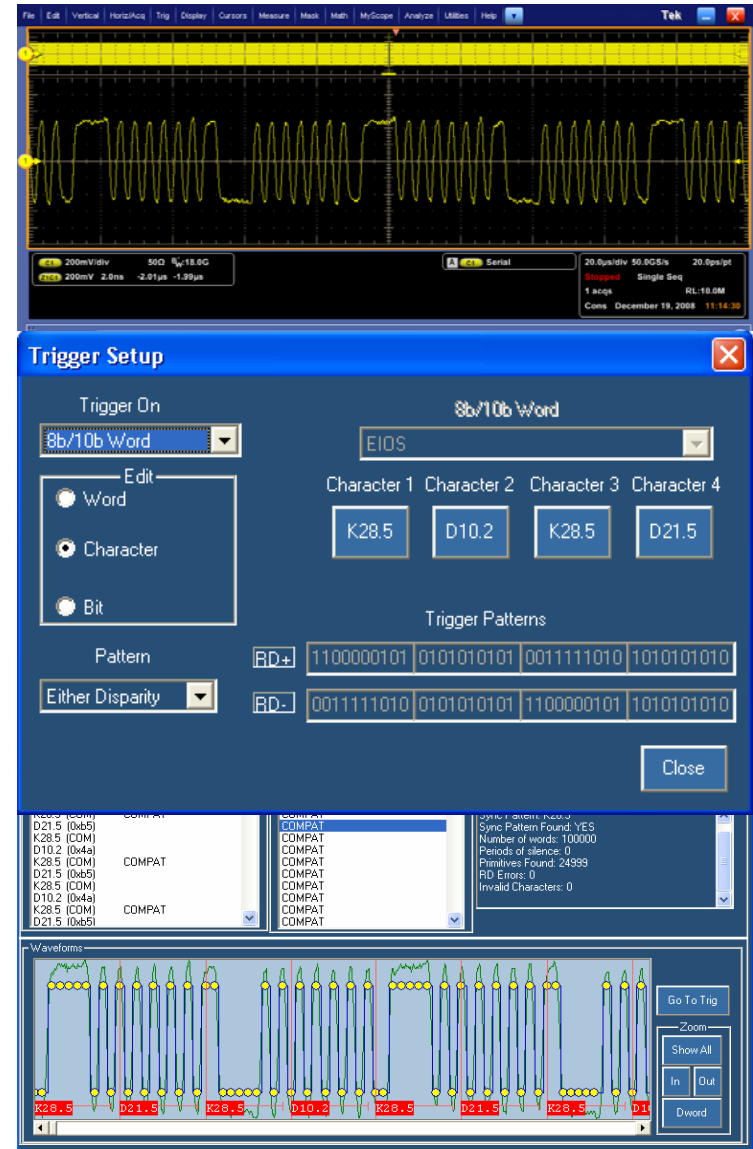
Triggering for High Speed Serial Bus Designs

Hardware-based triggering up to 5 Gb/s

- Serial pattern triggering captures a specified pattern with a length up to 64 bits long or 40 bits long for 8b/10b encoded serial data.
- De-embeds clock data in serial buses
- Serial Lane Skew Violation Trigger triggers on out-of-tolerance time skew between any two lanes.

Efficient debugging for fast root cause isolation

- Triggering support for the fastest serial busses including SATA, XAUI, Infiniband, PCI Express and others that transmit data and clock signals through differential techniques.



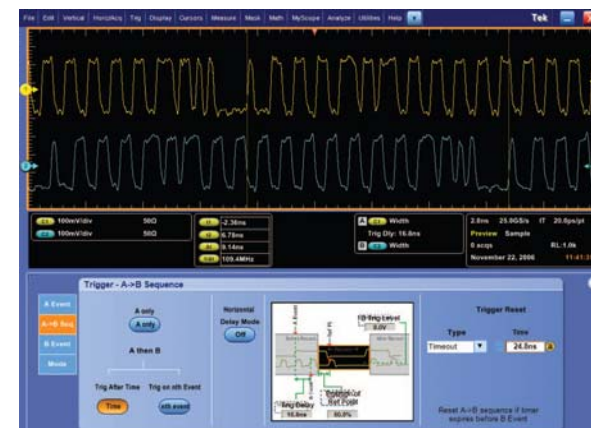
Serial Pattern Trigger Applications

- USB 3.0 5.0 Gb/s Loopback Error preamble decode
 - USB Rx designs include Bit Error Rate Test (BERT) commands
 - Unique characters enable error count and reporting
 - Error count request returns BERT Count (BCNT)

Table 6-18. BCNT

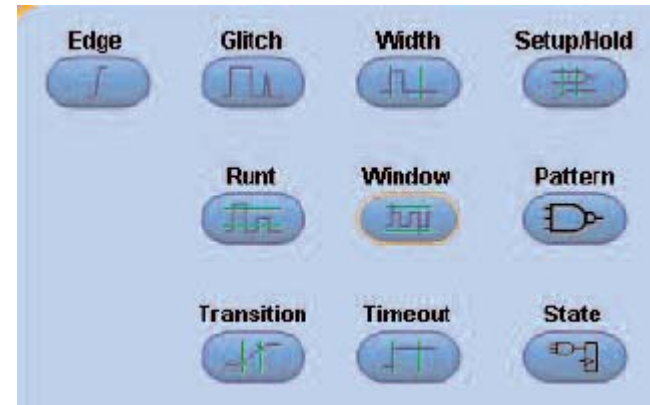
| Symbol Number | Encoded Values | Description |
|---------------|----------------|-----------------------------|
| 0 | K28.3 | BERC |
| 0 | K28.3 | BERC |
| EC<0:7> | DCODE | Error count (not scrambled) |
| EC<0:7> | DCODE | Error count (not scrambled) |

- System error detection and debug
 - System reported K28.6 upon failure
 - Only occurred once every few minutes
- Validation of encoding latency
 - Specific word is encoded into the data to be easily recognizable in the decoded serial data stream
 - Data propagates through and is checked at output for delay



ASM Features Increase Waveform Analysis Productivity

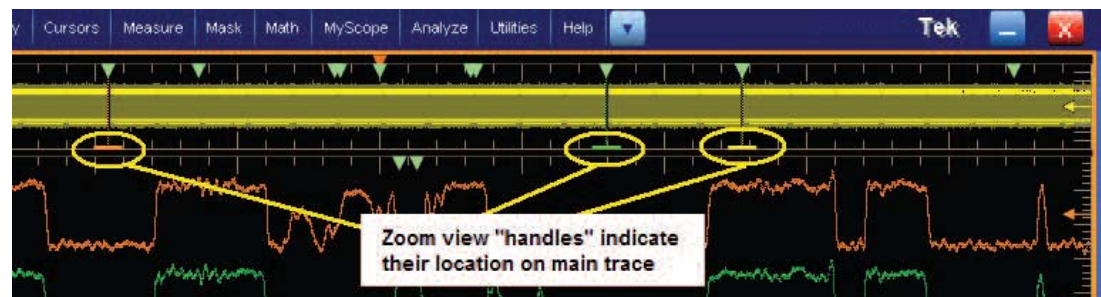
- Pinpoint Trigger Palette of Search Methods
 - Uses Pinpoint triggers to find events
 - Send and receive settings with Pinpoint
 - Performs 8 search methods simultaneously
 - 'Stop on Found' performs as a pseudo-trigger
- Fast, Efficient Navigation Controls
 - Jump between 'Marks' in long records
 - Add descriptions to each event Mark
 - Bring Cursors to Marks
- Results Table summarizes events
 - Precision Time stamp of each event Mark
 - Describe trigger event of each Mark
 - Select and jump to the event on any line
 - Export data to .CSV file
- Compare results with MultiView Zoom Display
 - Display multiple events in MultiView Zoom
 - Bring Zoom to Mark



Results: Mark Table

| Select | Index | Type | Src | Location | Time Delta | | | | | Description |
|-----------|-----------------|--------|-----|----------|------------|-----|-----|-----|-----|-----------------------|
| | | | | | sec | ms | us | ns | ps | |
| Configure | 3 | Glitch | C1 | 494.36ns | 000 | 000 | 000 | 247 | 740 | +Glitch: width=1.88ns |
| Results | 4 | Glitch | C1 | 742.16ns | 000 | 000 | 000 | 247 | 800 | +Glitch: width=1.78ns |
| View | 5 | Glitch | C1 | 989.96ns | 000 | 000 | 000 | 247 | 800 | +Glitch: width=1.8ns |
| Mode | 6 | Glitch | C1 | 1.238us | 000 | 000 | 000 | 247 | 820 | +Glitch: width=1.8ns |
| | 7 | Glitch | C1 | 1.486us | 000 | 000 | 000 | 247 | 900 | +Glitch: width=1.88ns |
| | 8 | Glitch | C1 | 1.734us | 000 | 000 | 000 | 247 | 840 | +Glitch: width=1.82ns |
| | Total Marks: 64 | | | | | | | | | |

Search Marks: Save Save All Clear Digits >> << Digits All Marks: Export Clear

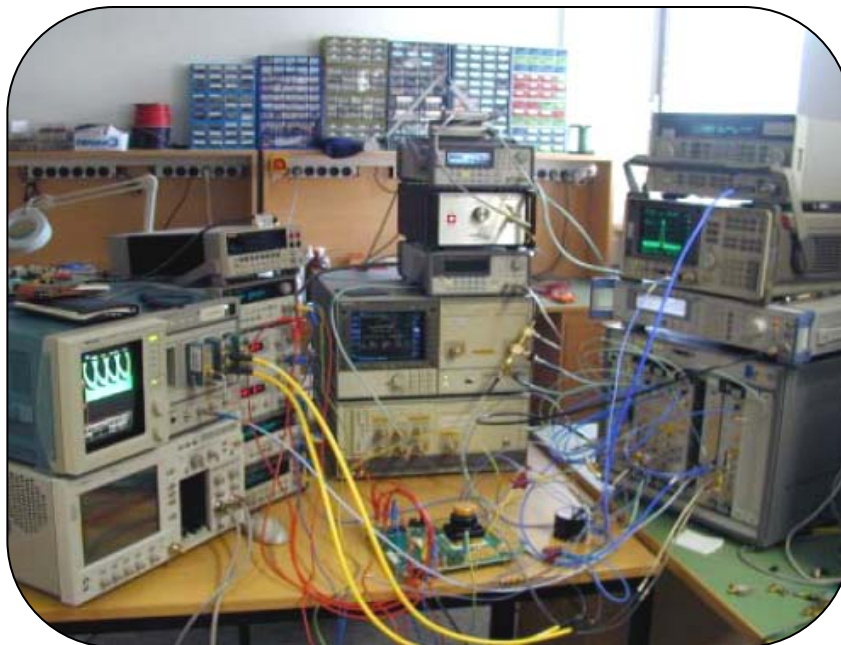


Agenda

- High-Speed Serial Test Challenges
- High-Speed Serial Test Simplified
 - Characterization
 - Debug
 - Compliance
- Measurement Example: PCI Express

Compliance Testing – An *Industry* Productivity Issue

- Greater speed means greater design complexity, necessitating...
- Greater test complexity
 - More instruments, configurations, and setup time
- More tests
 - Highly specialized – e.g., SSC modulation analysis, advanced receiver testing.
- Requires highly experienced, senior users
- Can require days to perform standards compliance tests



“Banner specs are no longer the gating issue. The latest equipment provides ample raw performance. What’s needed is greater ease of use and automation.”

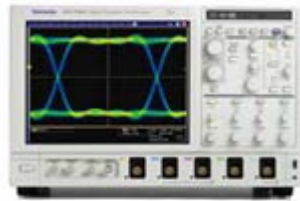
- Customer feedback

Proven Expertise in High Speed Serial Data Design & Test

PCI Express Solutions

■ Transmitter Signal Quality and Ref Clock Testing

- 4Ch Real Time Oscilloscopes
- High BW SMA Differential Probes
- Jitter and Eye Analysis Tools



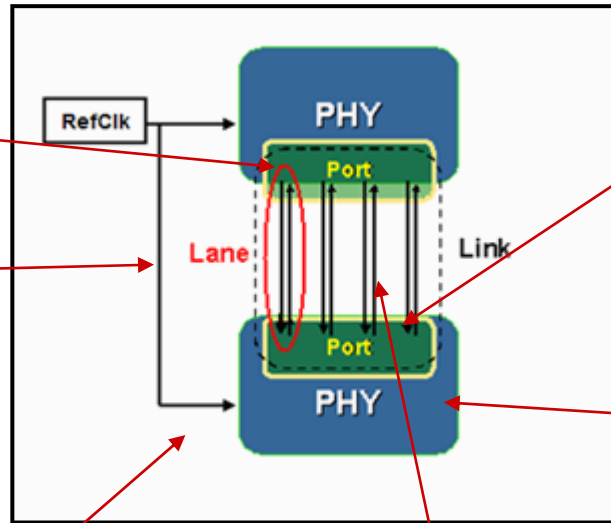
20GHz DSA

only Real-time Oscilloscope
System Electrical Validation
& Debug Solution for PCI 3.0

Tx, CEM



RefClk



■ Receiver Testing

- Arbitrary Waveform Generators
- Jitter Synthesis Tools

A new approach for easy,
thorough and repeatable
receiver testing



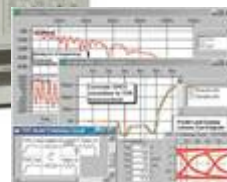
Rx



■ Interconnect Testing

- Sampling Oscilloscopes
- TDR Heads
- TDNA SW

S Parameters



■ Digital Validation and Debug

- Logic Analyzers and PCIe Serial Analyzers



Only Logic Analysis Debug
& Validation Solution for
PCIe 1 and 2.0

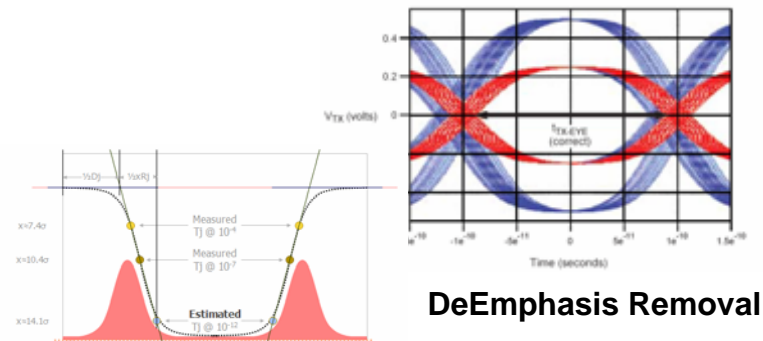
■ PLL Loop BW

- Real Time Spectrum Analyzers

Proven Expertise in High Speed Serial Data Design & Test

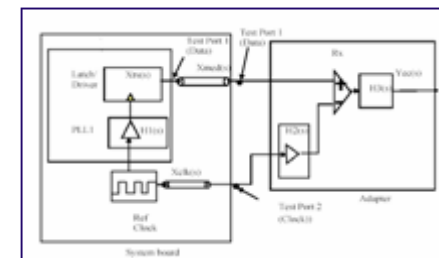
PCI Express 1.1/2.0 Testing

- Gen 1 Testing
 - DeEmphasis removal
 - Eye height of transition/non-transition bits
 - Common mode measurements
 - 1st Order PLL, median-max jitter
- Gen 2 Testing
 - Measurement Channel De-convolution
 - 2nd Order PLL, Dual-Dirac Jitter @ 10^{-12} BER
 - Signal Quality Eye and Jitter Testing
 - 1 Million UI Capture (10 Million Samples)
 - Dual-Dirac Jitter @ 10^{-12} BER
 - Receiver Test
 - Loop BW Test



DeEmphasis Removal

Dual-Dirac Jitter



Dual Port – 4Ch Capture

| Serial Bus Data Rate | Fundamental Frequency | 3 rd Harmonic | 5 th Harmonic |
|----------------------------|-----------------------|--------------------------|--------------------------|
| 2.5 Gb/s (PCI Express 1.1) | 1.25GHz | 3.75GHz | 6.25GHz |
| 3.0 Gb/s (SATA Gen 2) | 1.5GHz | 4.5GHz | 7.5GHz |
| 5.0 Gb/s (PCI-Express 2.0) | 2.5GHz | 7.5GHz | 12.5GHz |
| 6.0 Gb/s (SATA Gen 3) | 3.0GHz | 9.0GHz | 15 GHz 20 GHz |
| 8.0 Gb/s (PCI Express 3.0) | 4.0GHz | 12GHz | |

Proven Expertise in High Speed Serial Data Design & Test

Debug and Validation of PCI Express

- DPOJET and Option PCE
 - Measurement and setup library for PCIe Rev 1.1/2.0 and preliminary Rev 3.0
 - Measurements, limits and masks for three compliance test points
 - Base Spec Transmitter test point
 - System test point (using Compliance Load Board or CLB)
 - Add-In Card test point (using Compliance Base Board or CBB)
- Integrated analysis for easy validation and fast debug
 - Accurate Jitter Decomposition and TJ(BER) Estimation with Selectable Jitter Models Support
 - Analyze jitter with plots: Eye Diagram, CDF Bathtub, Spectrum, Histogram, and Trend
 - Software Clock Recovery including PCIe Golden PLL and custom PLL settings



PCI-E Electrical Compliance Testing

2.5Gb – 3.5dB

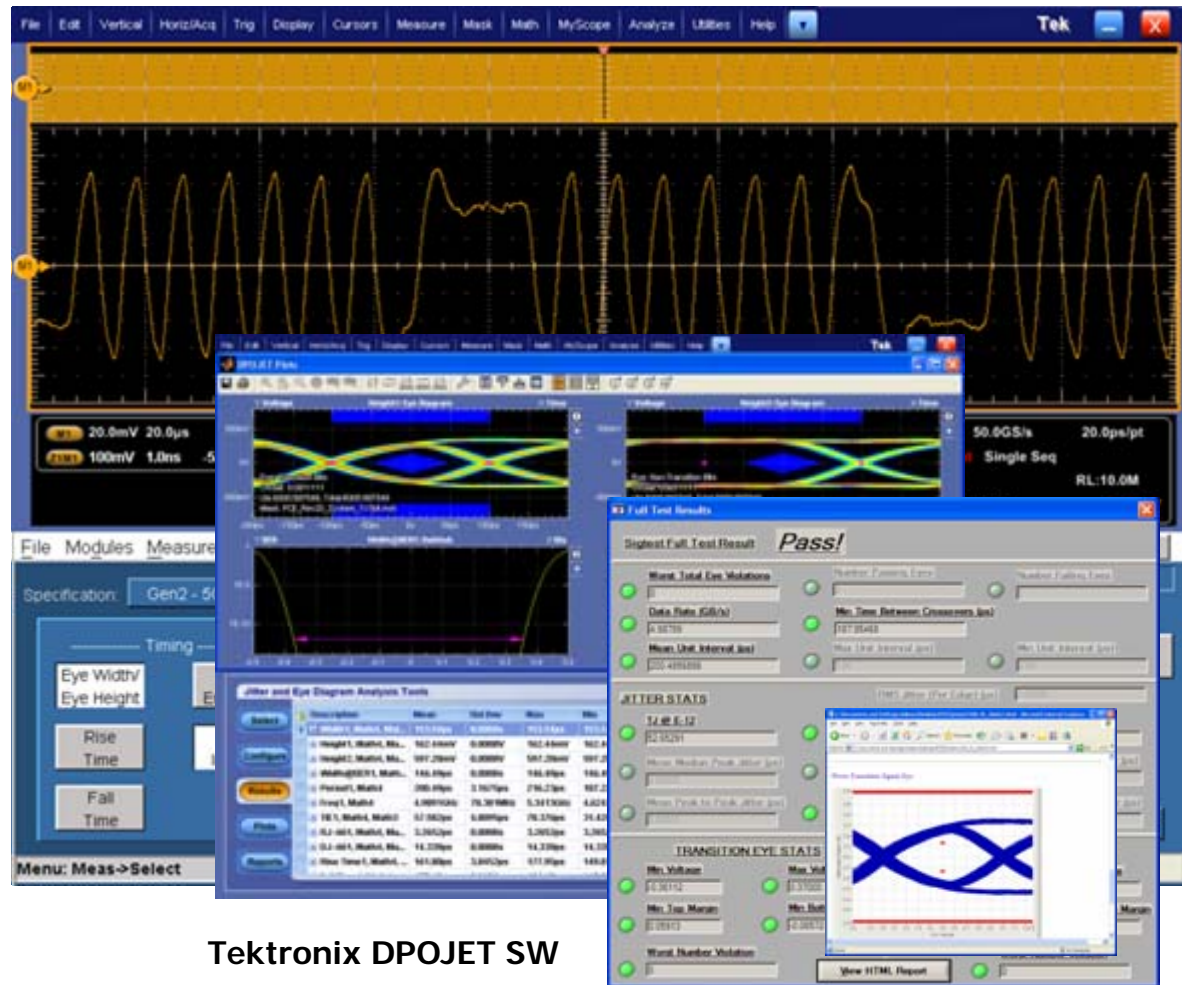


5Gb – 3.5dB



5Gb – 6.0dB

Speed/DeEmphToggle



Tektronix DPOJET SW

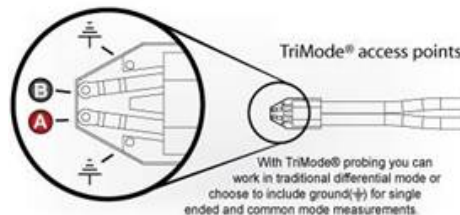
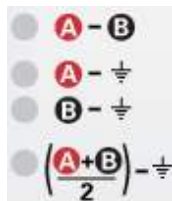
PCI-SIG Compliance Procedures:

http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library#electrical20

PCI-SIG SigTest SW

Common Mode Measurements

- Typically used when a signal needs to be measured and no SMA or RF connector is available
- Debug
 - Require a quick way to check that signals are present
 - Handheld probing offers the best versatility
 - Solder tips can be used for a more permanent connection for troubleshooting
- Validation and Compliance Testing
 - Chip to chip buses
 - Small solder tips are ideal for attaching to small features and give a permanent hands free connection to the signal
 - Fixtured probes can be used when soldering to a board is problematic



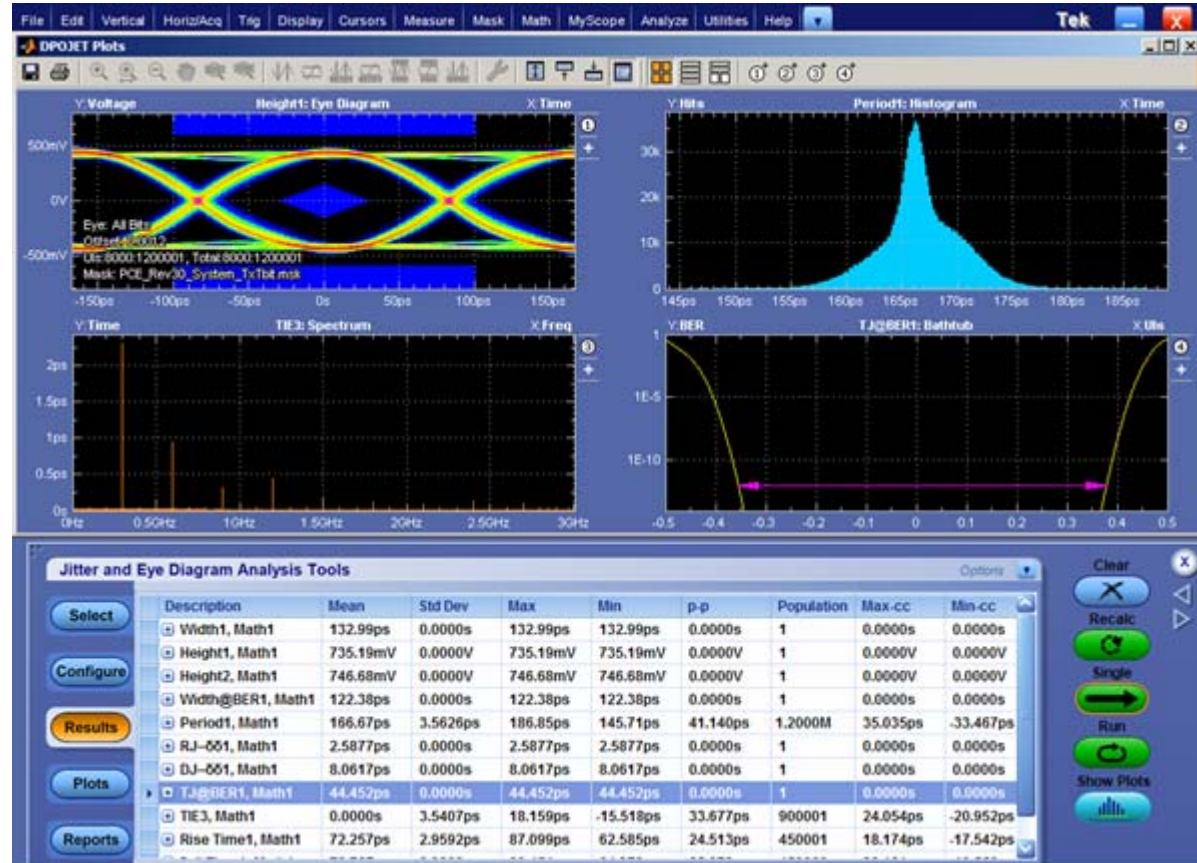
World's Highest Performing Solution For Next Generation Serial Technologies
A Perfect Combination -- DSA72004B 20 GHz Real-Time Digital Serial Analyzer + P7520 20 GHz Probe

Proven Expertise in High Speed Serial Data Design & Test

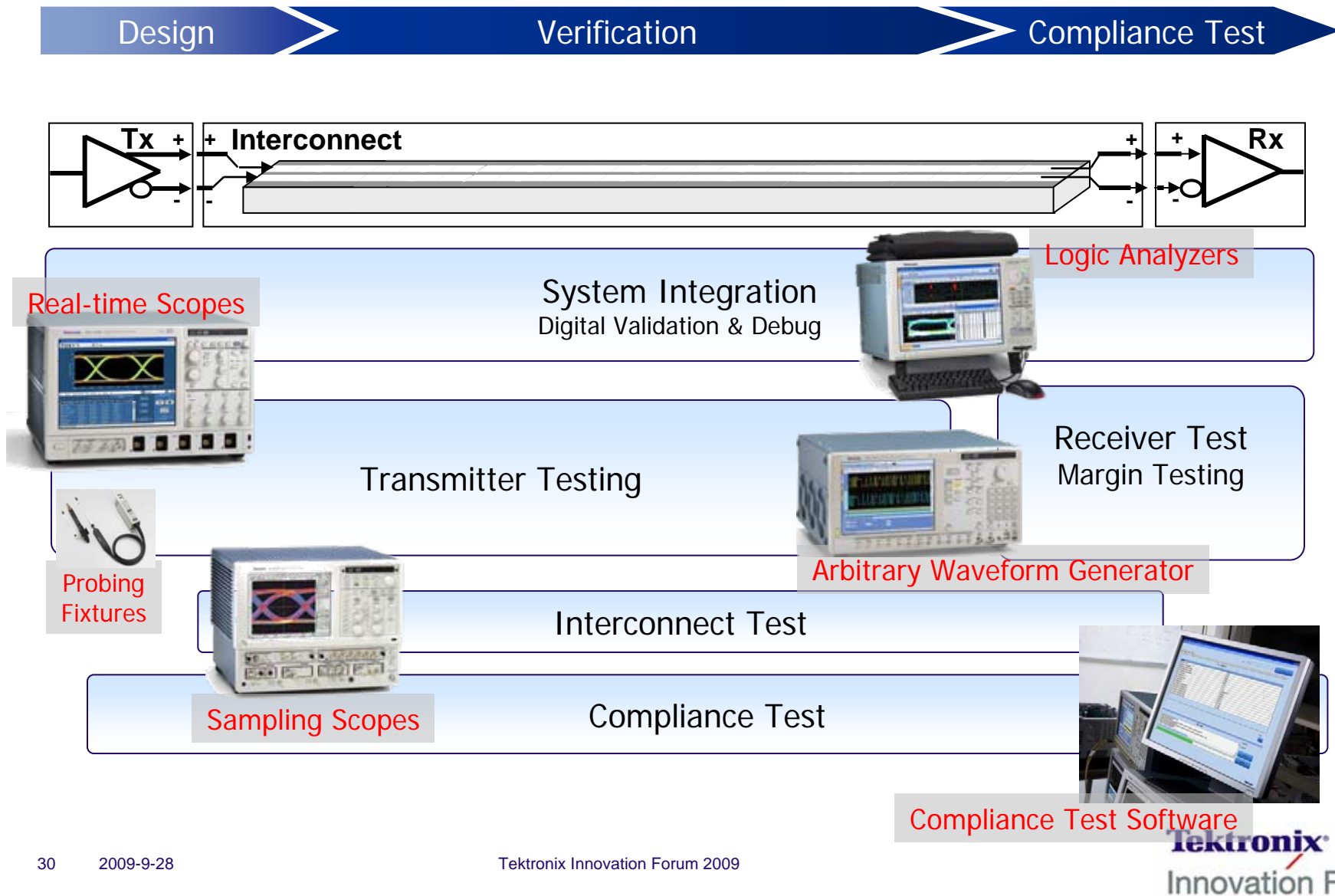
PCI Express 3.0 Electrical Testing

only Real-time Oscilloscope System Electrical Validation & Debug Solution for PCI 3.0

- DSA72004B Real-Time Oscilloscope
- DPOJET Jitter and Eye Tools Software
- P7500 TriMode™ Differential Probes
- AWG7122B Arbitrary Waveform Generator



High-Speed Serial Data Test Solutions



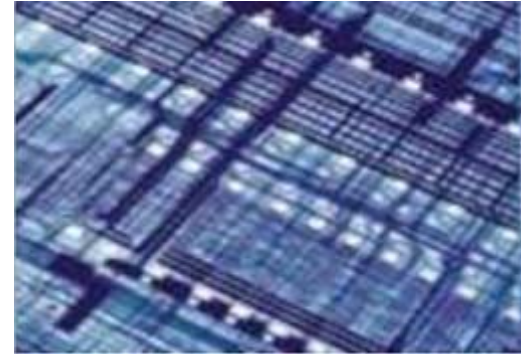
Serial Data Debug and Validation Summary

- Pressures of cost, design and layout simplicity have made advances in bit-rates even more complex
- The incredible complexity of systems today mandate a list of measurements for compliance which regularly number in the hundreds of tests.
- A generation of measurement tools has followed the evolution of serial architectures, giving you better tools for accelerated testing and to help you with serial measurement and compliance challenges.

■ http://www.tektronix.com/serial_data

[illegible]

Enabling Innovation in the Digital World



Accelerating Performance

Enabled by High-speed Serial Technologies