Tektronix Active Time Domain Method of Implementation: EDR Active Cables

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Revision History:

07/19/2014	Rev 0.46	Sampling calibration and interconnect de-embed incorporated in Appendix 9.
09/19/2014	Rev 0.47	IBTA CIWG Review Candidate.
09/24/2014	Rev 0.48	Incorporated John Smith's edits and corrections.
10/01/2014	Rev 0.49	Incorporated CIWG review comments from 09/25/2014 - Modify calibration process to center on 6.45GHz (fundamental of 1100 pattern)

Table of Contents

Glossary

This section provides definitions of the terminology used throughout this document. The reference diagram in Figure 1 is a considerably simplified representation of the ATD test system presented in this document, illustrating the terms defined in the glossary.

AOC	Active-Optical Cable assembly. Cable assemblies that use fiber–optic transceivers and fiber-optic interconnects to transmit high-speed serial data such as InfiniBand and Ethernet.
ATD	Active Time-Domain testing. A test methodology for active-cable-assemblies, (primarily Active Cable) where time-domain parameters such as jitter, eye-height and eye-width are measured on a stressed victim signal.
Cross-Talk	The phenomena of a signal transmitted on one channel coupling energy onto an adjacent channel, causing an undesirable effect.
Co-Propagating Input Aggressors	Adjacent channels which generate crosstalk energy and are driven from the input side of the test system and propagate in the same direction as the victim channel.
Counter-Propagating Output Aggressors	Adjacent channels which are driven from the output side of the test system, propagating in the opposite direction as the victim channel, and imposing crosstalk energy onto the victim channel at the output side of the ATD test system.
Counter-Propagating Input Aggressors	Adjacent channels which are driven from the output side of the test system, propagating in the opposite direction as the victim channel, and imposing crosstalk energy onto the victim channel at the input side of the ATD test system.
FEXT	Far-End Cross-Talk. Cross-Talk which occurs at the Far-End of a link. In ATD testing, the location of the Far-End is defined with respect to where the victim measurement is performed. FEXT will normally occur at the input of the ATD test system.
HCB	Host Compliance Board. PCB board or interface with known signal integrity characteristics that allow testing of host or switch specifications. The HCB is used for calibrating signals in the ATD test system. (HCB not illustrated below)
MCB	Module Compliance board. PCB board or interface with known signal integrity characteristics which allows testing of “modules” such as QSFP cable assemblies.
NEXT	Near-End Cross-Talk. Cross-Talk which occurs at the Near-End of a link. In ATD testing, the location of the Near-End is defined with respect to where the victim measurement is performed. NEXT will normally occur at the output of the ATD test system.
PPG	Pulse Pattern Generator. Signal generator used to generate pseudo random binary data for traffic.
LE320	2 channel 32Gbps , 9 Tap Continuous Time Linear Equalizer with independent tap and amplitude control.

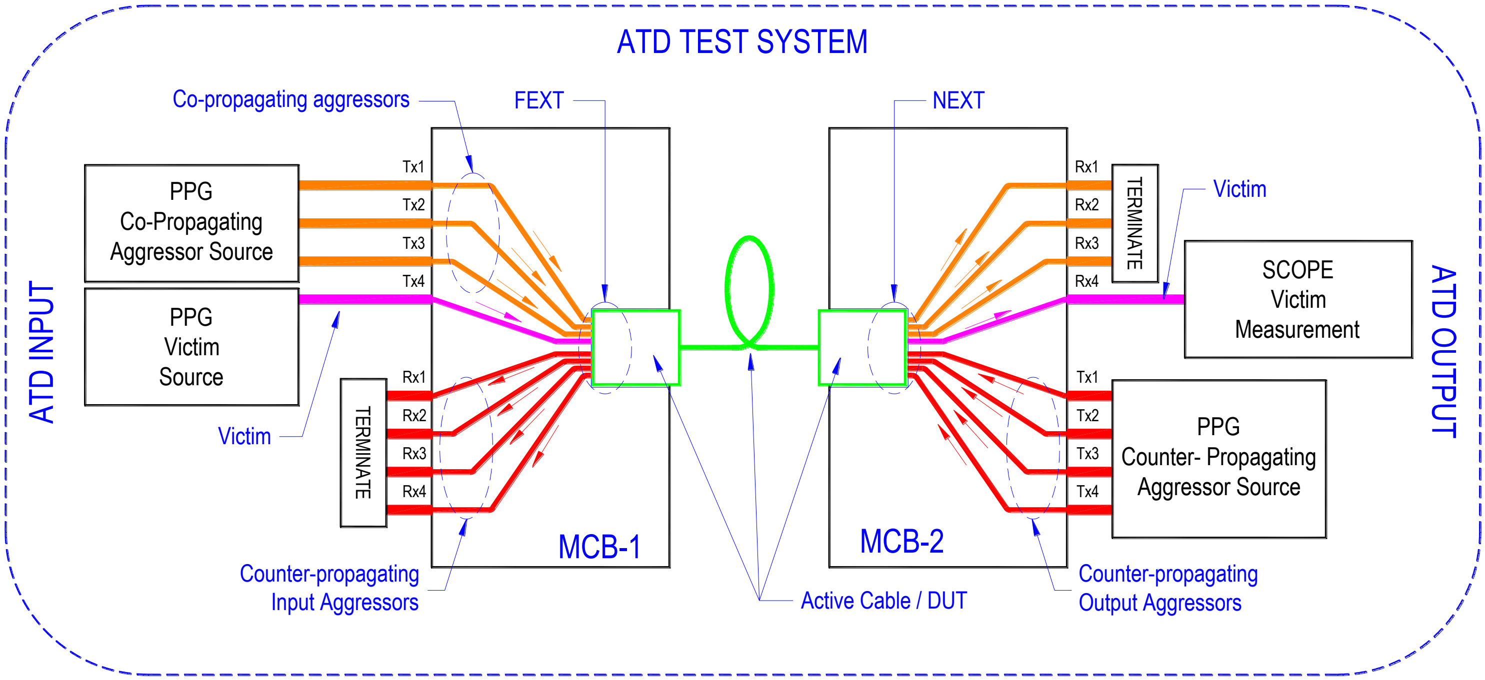


Figure 1. Glossary Reference Diagram

References:
IBTA Volume 2 Physical Specification Draft – November 6th 2012

Equipment List

- **Tektronix BSA286CL** – 28.6Gbps Low Noise BERTScope
- **Tektronix PPG3001** – 30Gbps 1 channel Pulse Pattern Generator
- **Tektronix LE320** – Tektronix 32G 2 channel linear equalizer/ 9 tap in-channel digital FIR filter.
- **Tektronix DSA8300** – Equivalent-Time Digital Signal Analyzer ~~(Used at QDR, EDR and EDR Speeds)~~
- **Tektronix 80E10B** – 50 GHz sampling Head
- **Tektronix 82A04B** – 30 GHz phase reference
- **Tektronix CR286A** – (Option HS, **80A08** Cabling & Splitters)
- **Tektronix 80A08 Kit** – High performance accessory kit for remote clock recovery pickoff
- **Tektronix TF-QSFP-TPACG-MCB-R** – (Wilder OEM) QSFP+ Test Point Adaptor, Module Compliance Board Receptacle
- **Tektronix TF-QSFP-TPACG-KT** – (Wilder OEM) QSFP+ Test Point Adaptor, Module Compliance Board Receptacle, Plug Kit.
- **Tektronix PSM5410** USB based Power Meter
- **Tektronix 4.0GHz lowpass filter** – PN: 119-6983-00 (note this in included in 80A08 Kit)

- **Tektronix/Picosecond Pulse Labs 5334-257** (2.92mm): Qty 2 – 5 Way Power Splitters

- **SMA Interconnect Cables**: Qty8 – Specified to a bandwidth of at least 18Ghz (25GHz Preferred); Phased matched pairs to +/- 2pS
- **Mellanox/Diolan I2C-Bridge** –I2C to USB Adaptor Dongle
- **PC Running Windows –** Used to control the I2C-Bridge device

Alternate QSFP test board options:

- PCB-111114-3020-REVA – Molex Host Compliance Board
- Molex MCB **r**equires 12 short <1ps phase matched cable pairs 6” in length to extend to power combiners. Tek part number 174636200 or equivalent.

NOTE : Reference Appendix 6 for specific guidance on allowable measurement windows.
Reference Appendix 9 for interconnect de-embed and instrument calibration procedures.

Quick Overview of Fixture Calibration and DUT testing

- **NOTE: This setup assumes TX4 is the victim**
  - *Any of the lanes could be tested as victims, and if this kind of testing was really done thoroughly each of the four victim lanes would be tested in turn. At IBTA Plug-Fest events there is only time to test one of the lanes as an audit. Other lanes could be selected as the victim for the audit on a case by case basis.*
- Quick Overview of DUT Testing: Refer to **Figure 2** which is a diagram named: "EDR ATD DUT Test Diagram, Tektronix Generator"
  - Figure-2 shows the complete setup for DUT testing
  - All Calibration steps for the victim, NEXT aggressors and FEXT aggressors need to be completed before DUT testing can proceed
  - The victim input signals and the co-propagating (FEXT) aggressors are connected to MCB-1
  - Counter-propagating (NEXT) Crosstalk are connected to the Tx connectors of MCB-2
  - The stressed eye Victim measurements are taken off MCB-2 using a Tektronix DSA8300 Equivalent Time Oscilloscope.
  - A 80SJNB automated routine measures all the appropriate parameters
- Results are collected and a report is generated from the 80SJNB tool.

- Quick Overview of calibration steps:
  - Set up connections to Tektronix test equipment
    - Refer to **Figure-3 'EDR ATD DUT** Victim and FEXT Calibration Test Diagram
    - Use MCB -HCB mated pair
    - Divider networks are used for the FEXT and NEXT aggressors in conjunction with LE320's for signal fan-out and amplitude control.
    - Load the proper Tektronix 80SJNB setup file for the victim stressed eye testing
  - Initial rough calibration of Victim stressed-eye to set amplitude and emphasis tuning
    - The victim signal should be roughly setup before FEXT and NEXT aggressors are calibrated
    - The Tektronix BSA286CL and the LE320 emphasis unit should be configured to output a rough approximation of the amplitude and emphasis required for victim signal calibration.
    - The victim eye should be initially measured at the TEK DSA8300 using 80SJNB SW
  - Calibration of FEXT aggressors:
    - Refer to **Figure-3 EDR ATD DUT Victim and FEXT Calibration** Test Diagram
    - The FEXT aggressors are measured at TP7A using the TEK DSA8300
  - Calibration of NEXT aggressor
    - Refer to **Figure-4** EDR ATD DUT NEXT Calibration Test Diagram
    - Use MCB –HCB mated pair
    - The NEXT aggressor are measured at TP6A using the TEK DSA8300
  - Calibration of Victim with properly calibrated FEXT and NEXT aggressors
    - Refer to **Figure-3 EDR ATD DUT** Victim and FEXT Calibration Test Diagram
    - It will likely take a few tuning trials until all victim stressed eye specifications are met
    - Adjust the amplitude and emphasis of the victim to meet victim eye-mask and jitter specs
    - The settings on the jitter generator will need to modified as required
    - The Final measurements of the victim should be recorded
      - A 80SJNB report should be generated and saved
  -

Divider Networks (Electronic/Passive)

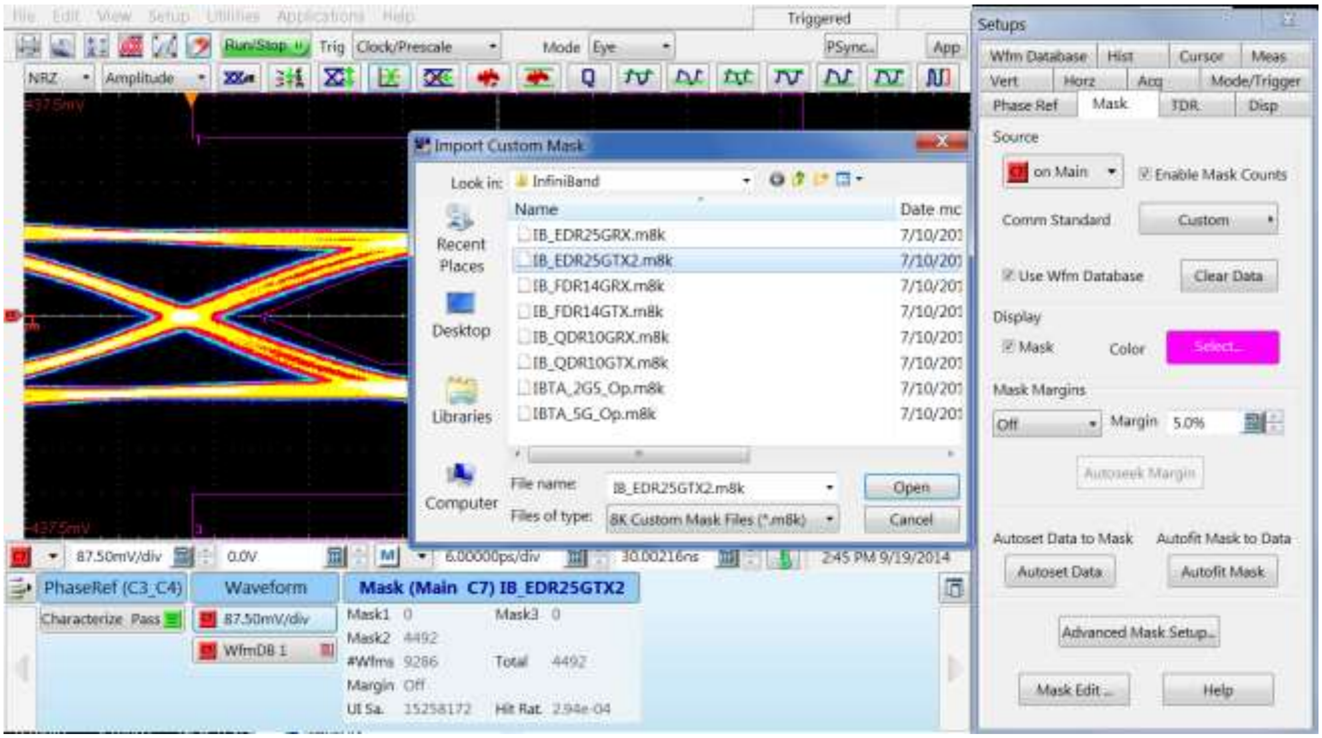
- Passive Power Divider networks are used to split a signal coming from the BERTScope or PPG into multiple signals. This allows two PPG units to drive all the aggressor signals required for testing
- There are obvious pros and cons of using divider networks, for testing
    - Passive Divider networks permit the recirculation of reflected energy off of the QSFP fixture making the signal calibration and control a significant challenge. The SDD11 (differential return loss) of the QSFP fixture can be approximately -10dB, resulting in 30% reflected signal incident to the fixture. There are 4 reflected signal paths re-entering the signal divider, and the resulting interference complicates calibration.
    - Electronic Divider networks such the Tektronix LE320 provide several important benefits in this situation. 1. They can be used to convert a single ended signal from a splitter into a buffered and independently controlled differential signal with variable amplitude. 2. The act as a 1 way valve, preventing reflected energy from the QSFP fixture from working back into the divider network. 3. The active FIR filtering capability permit channel effects de-embed and signal phase reversal.

      <u>For this set of reasons, this MOI leverages 4 LE320's</u> to permit controlled, aggressor, co-propagated FEXT and counter propagated NEXT signal configurations, with in effect a digitally controlled active splitter arrangement.

- Please note in the setup diagrams, that the second PPG unit used to drive the NEXT aggressors is set to a slightly lower data rate of 25.0Gbps, compared to 25.78127 for the victim and FEXT aggressors.
    - This is to make the NEXT aggressors out of phase with the victim input signal
- Also note that the signal ended "P" and N" pairs for the NEXT and FEXT signals should be alternated so that lanes are 180^{o} out of phase with each other.

TEKTRONIX DSA8300 Equivalent-Time Oscilloscope Mask Setup Files

- Tektronix DSA8300 setup files which contain the ~~QDR, EDR and~~ EDR Mask geometries can be downloaded here. These were updated on July 2014. Replace all prior versions with these.
  https://danahertm.box.com/s/o78d91exe7ldstehj7o0
  These Masks should be imported into the DSA8300 as follows:
  Mask Setup needs to be configured to Custom, Wfm Database.
  From the File->Import Custom Mask menu, select the IB_EDR25GTX2.m8k file contained in the above mentions network link.



Note: (To be incorporated into setup file at some future date)

Ensure sampling density is set to 1000

Waveforms to be accrued before stop should be set to 2000

In this configuration, the display shows 2 UI's of data. Only the center UI is measured against the mask. This means 1000 samples * 2000 accrued waveforms / 2UI which offers 5.0E-5 mask certainty with 50 hits maximum.

Voltage Range Setting for EDR AOC Assemblies Using Mellanox-Diolan I2C-Bridge

NOTE: Please refer to the IBTA specification for full information on range settings for EDR AOC assemblies.

- The range setting on EDR AOC assemblies needs to be set at both DUT plug-ends
  - Range settings in EDR AOC assemblies are a non-sticky setting in the AOC QSFP memory map
    - Range settings are accessed on Page-3 bytes 238 and 239 (0xEE and 0xFF)
- The IBTA / IOL uses the Mellanox-Diolan I2C-Bridge USB to I2C dongle to program the proper bytes
  - A PC is used to control the Diolan I2C-Bridge device
  - **PLEASE see the Appendix for "bat" files that have been created to program range settings**
  - DUT "Plug-2" is connected to MCB-2 where the O-scope measurement is made
    - The DUT measurement must be made with Range-0 set
    - Bytes 238 and 239 should be set to "zero"
  - DUT "Plug-1" is connected to MCB-1, where the victim signal is driven
    - Plug-1 should be set to Range-0, to emulate the worst case cross-talk environment
    - Bytes 238 and 239 should be set to "zero"

STEP-1 - Calibrate the Counter-Propagating (output) Aggressor Signals Required for Victim Stressed-Eye-Calibration on MCB-1

- **Please refer to Figure-3: diagram titled: "EDR ATD DUT Victim and FEXT Calibration Test Diagram"**
  - Connect the HCB to MCB-1 to form a mated pair
  - Connect the counter-propagating Crosstalk (NEXT) sources from the divider network driven by Tektronix PPG3001 **CH 1** (Data +) to the HCB-RX SMA connectors (Rx1P, RX1N,RX2P,RX2N,RX3P,RX3N,RX4P,RX4N)
  - Measure the Counter-propagating (output) NEXT aggressor signals on the MCB-1 at TP7a Rx-SMA Connectors - Rx1P, RX1N,RX2P,RX2N,RX3P,RX3N,RX4P,RX4N)

    Change the cross-talk source settings on the PPG as required to meet the specified limits amplitude and rise and fall transition time limits
  - Please see **Appendix-2** for target value for amplitude and transition times of the counter-propogating NEXT output-aggressors

    Note: These aggressors emulate the counter-propagating signals at the output of the cable DUT which will be set to amplitude range 0
  - For EDR The measured r/f transition time at MCB-1 TP7A should measure 17ps at each test point-Measured with a 17GHz low-pass filter

STEP-2 - Co-Propagating Cross-talk (FEXT) Calibration on MCB-1

- **Please refer to Figure-3: diagram titled: "EDR ATD Victim FEXT Calibration Test Diagram"**
- Start with same mated pair setup from Step-1; with the now calibrated counter-propagating Cross-talk source
  - Terminate the MCB-1 RX SMA connectors with eight 50-ohm loads (Rx1P, RX1N,RX2P,RX2N,RX3P,RX3N,RX4P,RX4N)
  - Plug the Victim generating source into the selected victim TX lane of MCB-1: Tx4P and TX4P
    - We will calibrate the victim in Step 3; For now leave the victim to work on the three other co-propagating cross-talk lanes
  - Connect the Co-Propagating Cross-talk (FEXT) sources from the divider network driven by Tektronix BSA286CL (**Data -)** into MCB-1 on into the non-victim" Tx lines: TX1P,TX1N, TX2P, TX2N, TX3P,TX3N
    - Turn on the crosstalk source generator, PPG3001
  - One by one, measure the six Co-propagating cross-talk signals at TP6A of the HCB: TX1P,TX1N, Tx2P,Tx2N,TX3P,TX3N,
    - Change the cross-talk source settings as required to meet the specified limits

- Please refer to **Appendix-2** for target value for amplitude and transition times of the co-propogating FEXT Input aggressors.
- The rise /fall transition time at TP6A should be measured with a 17GHz low-pass filter
- After each crosstalk signal is successfully measured to spec limits, terminate the SMA connectors with 50-ohm loads

STEP-3 - Victim Stressed-Eye Calibration

- Start with same mated pair setup from Step 2, with all of the cross-talk sources calibrated and terminated in the correct places
  - Verify that the Victim source generator is connected and is set up to reasonable starting settings (for instance the settings from PF-21 are a good starting point)
  - Connect the Victim output on the HCB TX4P, TX4N to a TEK DSA8300 equivalent time oscilloscope with 80SJNB80SJNB based Jitter and eye-mask measurement tools

    Load the 80SJNB setup configured for ATD Victim calibration found here.

    https://danahertm.box.com/s/o78d91exe7ldstehj7o0

  - Measure the eye-mask, jitter and DDPWS parameters. Refer to Appendix 3 for DDPWS adjustment specifics.
    - Modify the amplitude, emphasis and jitter sources to meet the victim input specs in the presence of Far-end and near-end crosstalk; It will most likely take several trial before the specifications are met
  - Please see **Appendix-1** Victim-Input Specifications for the target parameters of the Stressed-eye Victim Measurements in the presence of FEXT and NEXT crosstalk.

STEP 4 - Calibrating the Counter-Propagating (Input) Aggressors (NEXT) On MCB-2

- **Please Refer to Figure 4: EDR ATD DUT NEXT Calibration Test Diagram:**
  - Disconnect HCB from MCB-1
  - Remove the crosstalk sources from RX lines on HCB
  - Connect the HCB to MCB-2 to form a mated pair
  - Connect the "counter-propagating" cross-talk sources to the TX SMA connectors on MCB-2 TP5a: TX1P, TX1N, TX2P, TX2N, TX3P,TX3N,TX4P,TX4N
  - Turn on the Counter propagating Cross-talk source generator Tektronix PPG 300**1, Ch 1 (Data+) (Figure 4)**
    - Note the input clock to the Pattern generator is intentionally set to 25.0GHz
    - The data rate of the counter propagating PPG will slightly offset form the standard data rate of 25.0 Gbps to help create a worst case aggressor source
  - Measure the (input) counter-propagating signals at the HCB TP6A: TX1P, TX1N, TX2P, TX2N, TX3P,TX3N,TX4P,TX4N
  - Please see **Appendix-2** for target value for amplitude and transition times of the Counter-propogating NEXT Input aggressors.
    - ***Note: These aggressors emulate the counter-propagating signals generated by the switch (or host) to the input of the cable***
  - After each crosstalk signal is successfully measured to spec limits, terminate the SMA connectors with 50-ohm loads
  - Disconnect the HCB from MCB-2

Step 5 - DUT Testing

- **All calibration steps must be completed before DUT testing can commence**
  - **Figure-2** shows the complete setup for DUT testing

- Connect Plug-1 of the DUT cable into MCB-1 that has victim and aggressors calibrated using step-2 above
- Connect Plug-2 of the DUT cable into MCB-2 that has the counter-propagating aggressors (NEXT) calibrated using Step-4 above
- Run the proper I2C-USB Bridge commands to set Plug-2 in MCB-2 to range-0 for DUT testing
  - Plug-1 in MCB-1 should be set to Range-1
- Connected the TEK DSA8300 equivalent time Oscilloscope to the MCB-2 victim lane (RX4P, RX4N)
- Load the proper TEK 80SJNB and Mask setup files for EDR Limiting Active Cable Testing
- Run TEK 80SJNB80SJNB and Measure the victim to IBTA Specifications:
  - Eye-mask hit ratio test set at Tx amplitude Range-0
- Record measured values in proper DUT spreadsheet
- Perform a print to file operation on 80SJNB to capture a full report for this DUT.80SJNB
- **NOTE**: It is recommended that the DSA8300 Bandwidth be limited (Setup->Vertical Menu) to ~~20GHz for QDR, 30GHz for EDR and~~ 60GHz for EDR speeds.

Figure 2: EDR ATD DUT Test Diagram, Tektronix Generator:

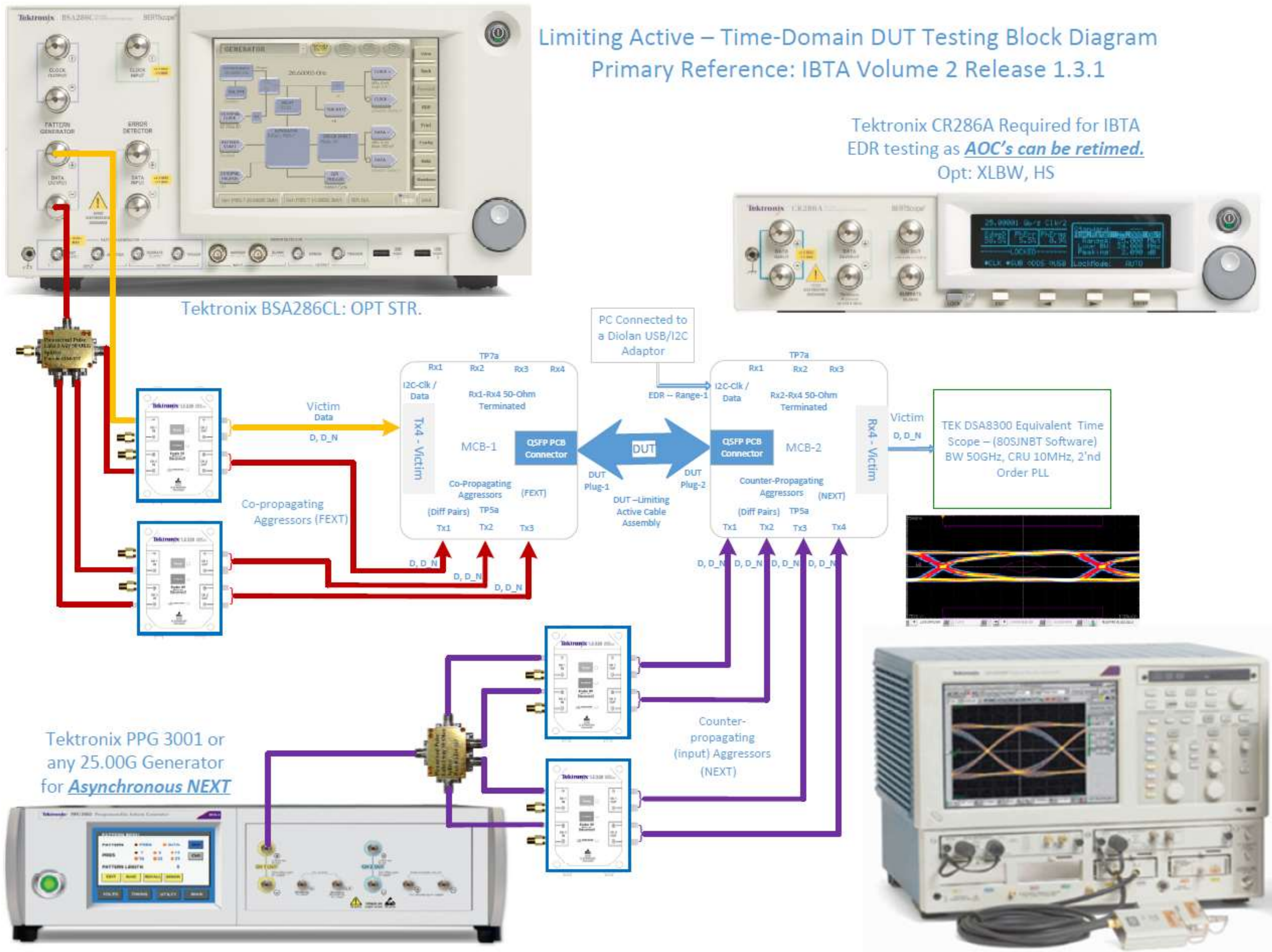


Figure 3: EDR ATD DUT Victim and FEXT Calibration Test Diagram:

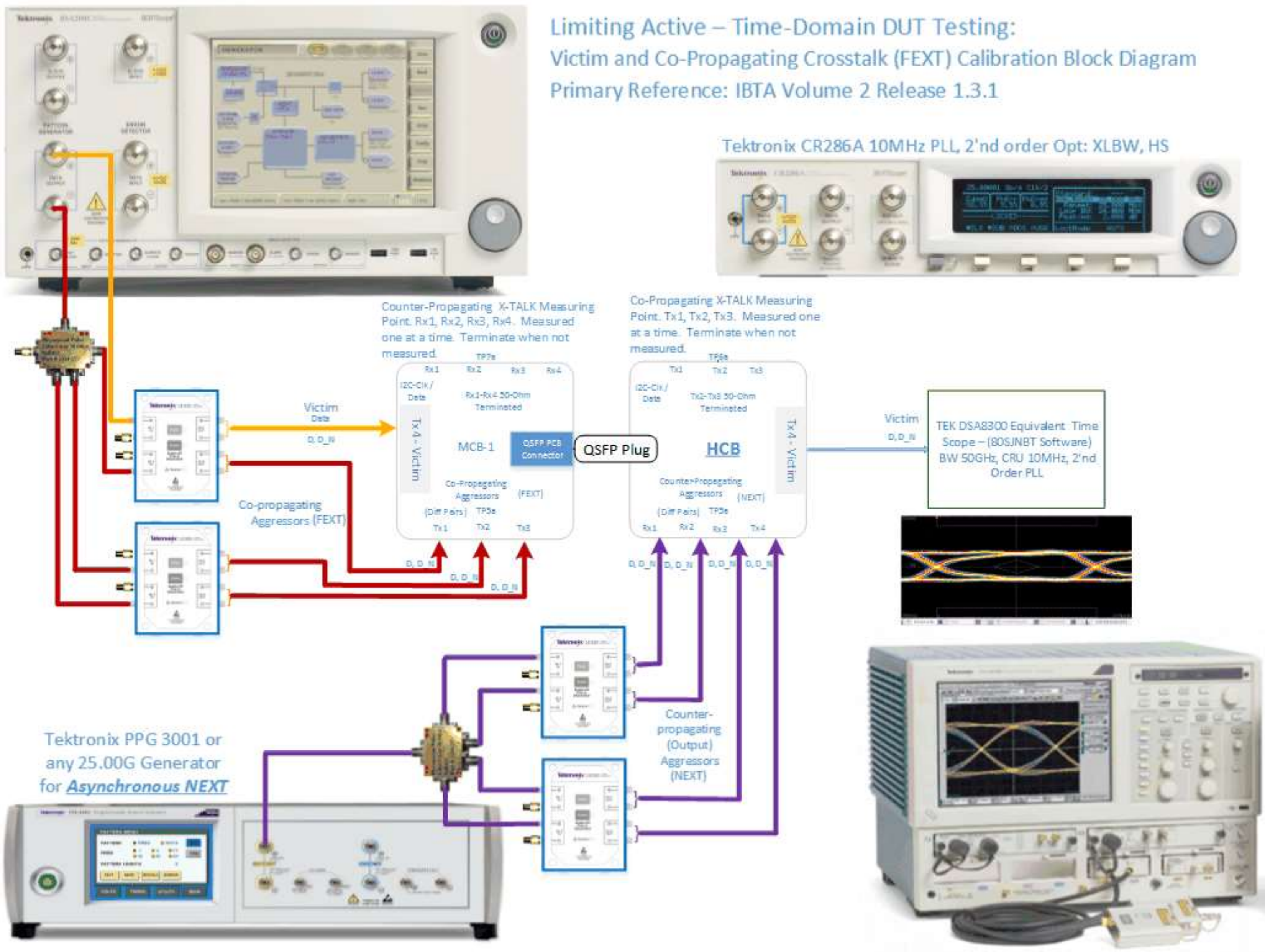
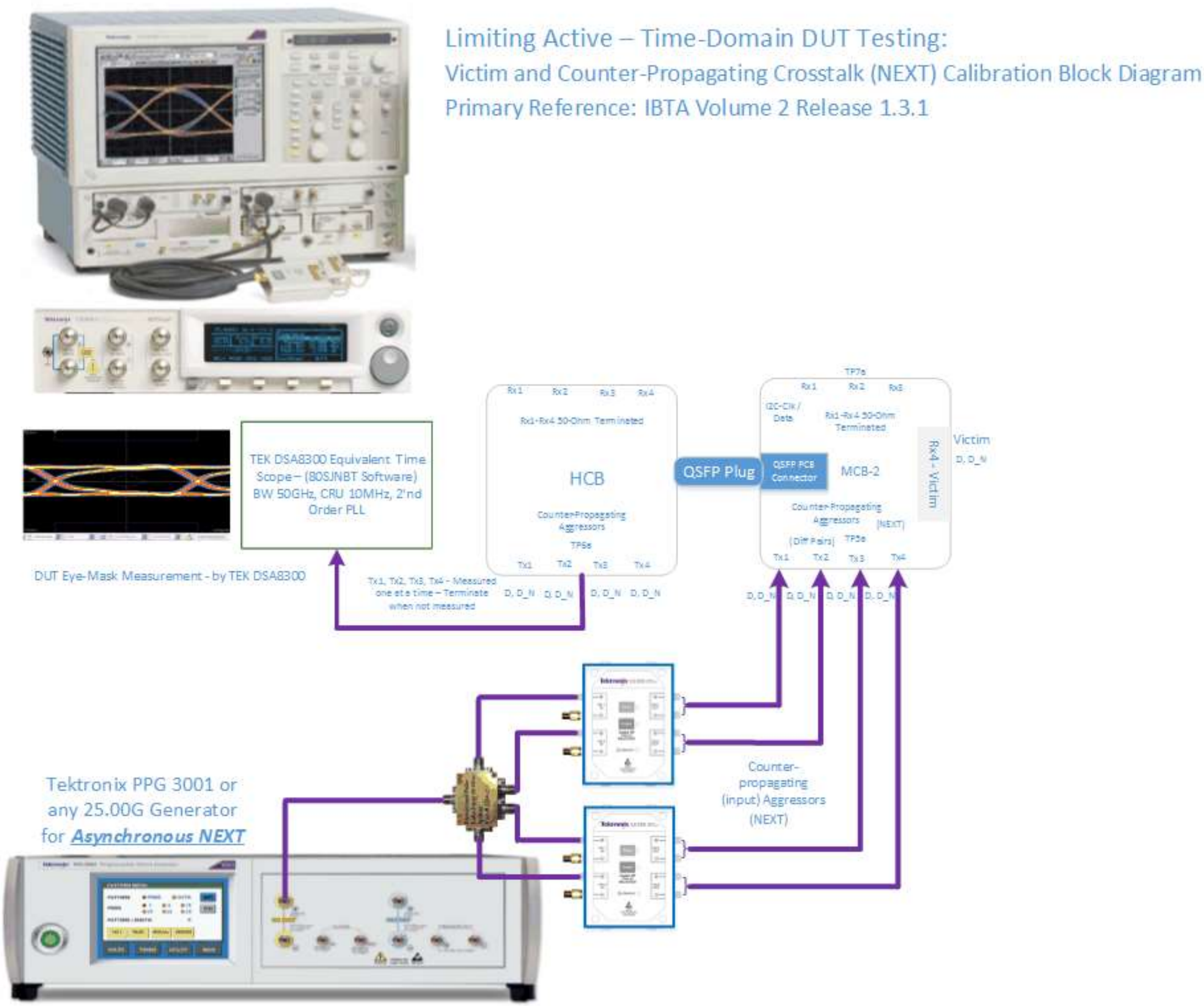


Figure 4: EDR ATD DUT NEXT Calibration Test Diagram:



Appendix 1: Tables of EDR IBTA Victim Specifications

Victim Input Specifications - EDR		
Data Rate	25.78125Gbps	
UI	38.7879ps	
Pattern	PRBS31 (PRBS9-DDPWS)	
X1*	0.11UI	4.267ps
X2*	0.31UI	12.024ps
Y1*	95mV	190mVpp Swing
Y2*	350mV	700mVpp Swing
J2*	0.19UI	7.37ps
J9*	0.34UI	13.19ps

Victim Output Specifications - EDR		
Data Rate	25.78125Gbps	
UI	38.7879ps	
Pattern	PRBS31	
X1-Max*	0.30UI	11.6363ps
Y1*	50mv	100mVpp Swing
Y2*	225mV	450mVpp Swing
J2-Max*	0.44UI	17.06ps
J9-Max*	0.69UI	26.76ps
tr-Min*	10ps (20/80)	

Appendix 2: Tables of ~~QDR and~~ EDR IBTA Aggressor Parameters

Counter Propagating NEXT Output Aggressors - EDR		
Data Rate	**25.0Gbps**	**Comment**
UI	40ps	
Pattern	PRBS31	
Amplitude	450mV PP	NOT to exceed*
tr**	17ps (20/80)	No faster than
*Intention is to source largest amplitude allowed by Table 88		

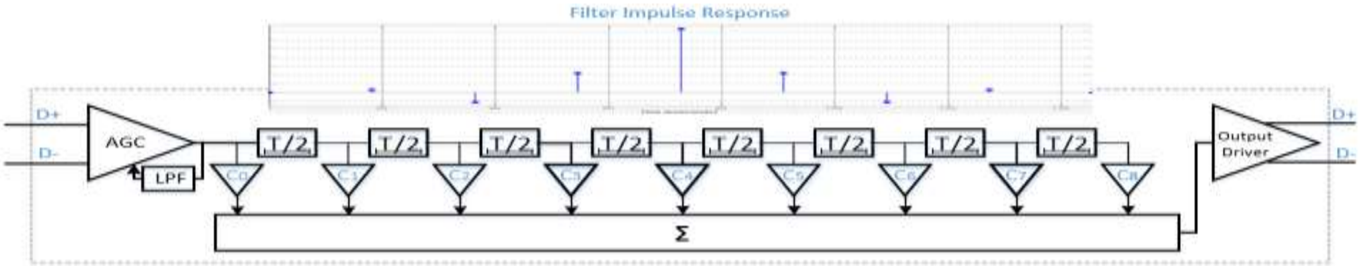
Counter Propagating NEXT Input Aggressors - EDR		
Data Rate	**25.0Gbps**	**Comment**
UI	40ps	
Pattern	PRBS31	
Amplitude	700mV PP	NOT to exceed*
tr**	24ps (20/80)	As close as possible
*Intention is to source largest amplitude allowed by Table 87		

Co- Propagating FEXT Output Aggressors - EDR		
Data Rate	**25.78127**	**Comment**
UI	38.7879ps	
Pattern	PRBS31	
Amplitude	450mV PP	NOT to exceed*
tr**	13ps (20/80)	No faster than
*Intention is to source largest amplitude allowed by Table 88		

Co- Propagating FEXT Input Aggressors - EDR		
Data Rate	**25.78127**	**Comment**
UI	38.7879ps	
Pattern	PRBS31	
Amplitude	700mV PP	NOT to exceed*
tr**	13ps (20/80)	As close as possible
*Intention is to source largest amplitude allowed by Table 87		

Appendix 3: LE320 Calibration Process

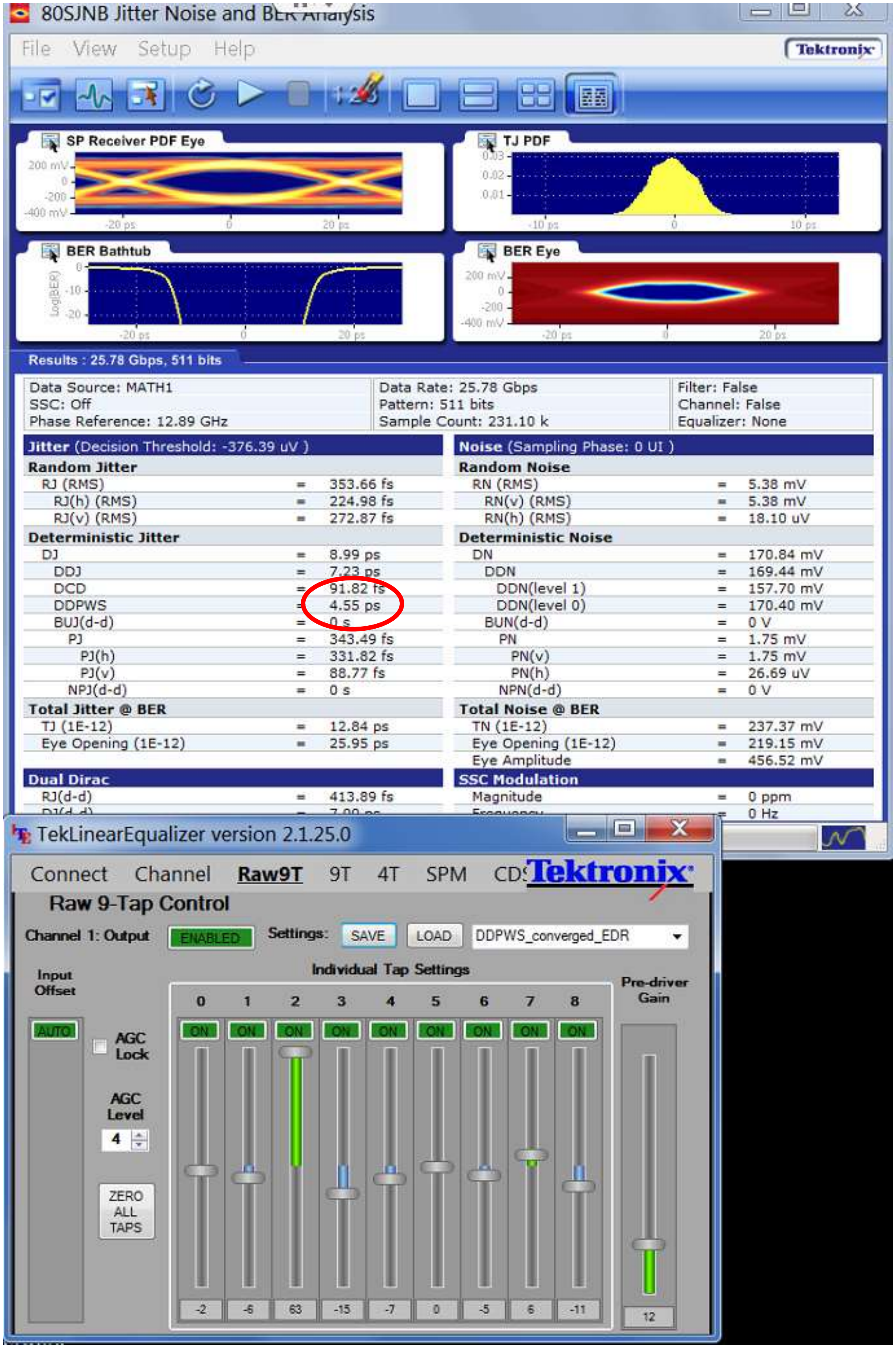
The LE320 is a multi-channel FIR filter with independent taps and amplitude controls.



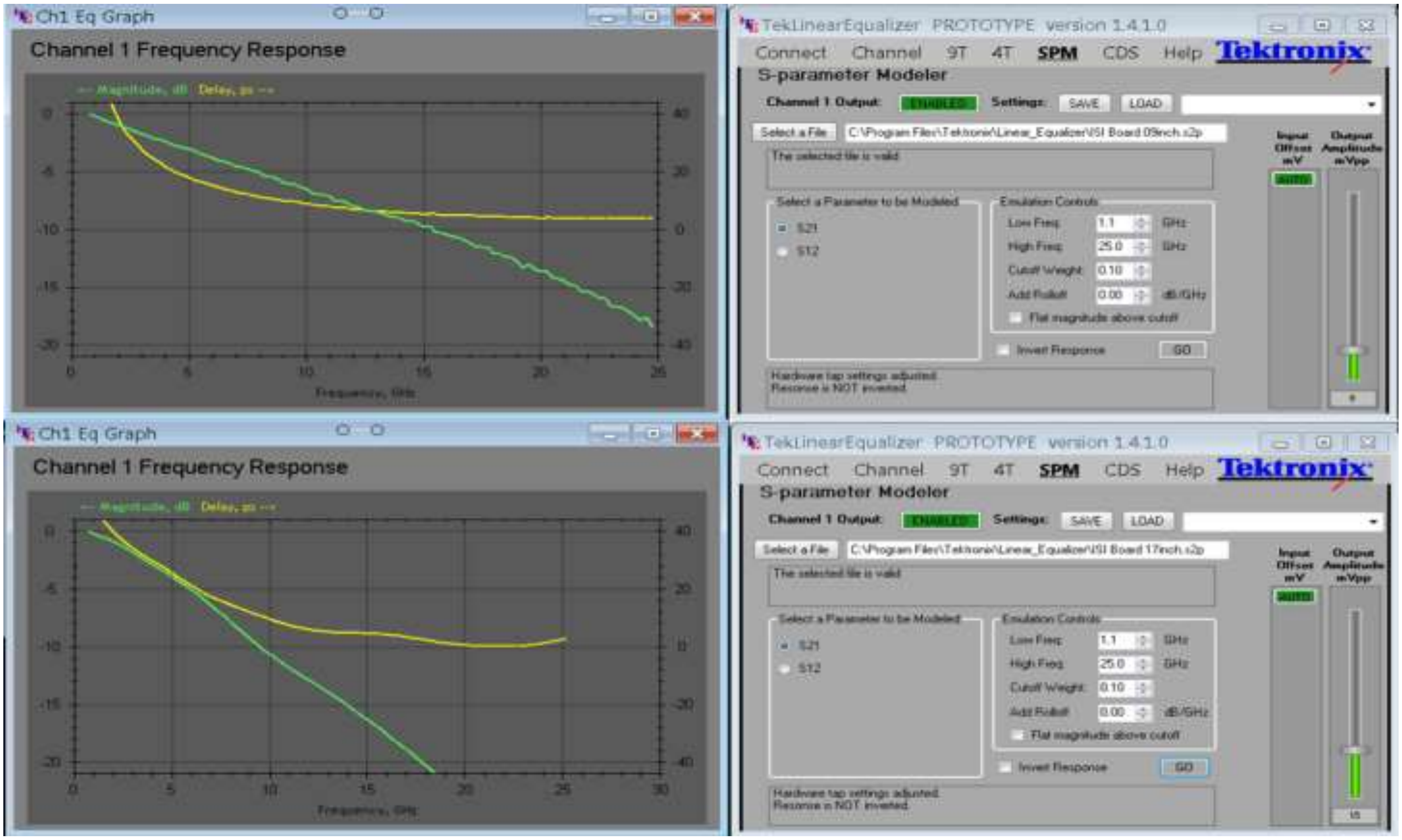
It's utilization in this EDR AOC configuration is twofold. Its independent output amplitude and phase controls permits worst case alignment of aggressor –vs- victim signal transitions. This permits for effective isolation of crosstalk elements which are common issues in current AOC setups.

The filters are manually controllable through a UI, or an automation interface via USB. Tektronix provides a series of tools with the LE320 which allow one to carefully construct a channel impulse filter response which may exhibit a particular frequency dependent loss profile. These electronic channel loss profiles are key to calibrating Data Dependent Pulse Width Shrinkage (DDPWS) which is an isolated form of DDJ measurement.

The illustration here, shows the synthesis of a single channel impulse response derived from a user's S2p (Touchstone) file inputs. Fine adjustment can be applied to hit a precise DDJ or DDPS target value as shown here for EDR



Tektronix LE320 settings showing EDR DDPWS convergence.



Tektronix LE320 S-Parameter Modeler UI

Appendix 4: (place holder for interop data)

Appendix 5: EDR Range Settings Commands using the Mellanox-Diolan – I2C-Bridge Device

These are the contents of "bat" files that have been created to control the Mellanox-Diolan I2C Bridge dongle

- **Set Range 0 – File name: w238-239_to0.bat**
  - Contents:

```
cd C:\Program Files (x86)\Diolan\I2CBridge.x64\bin
i2c r -s:0x50 -a:0x1:0x7f -d:0x1
i2c w -s:0x50 -a:0x1:0x7f -d:0x1 3
i2c r -s:0x50 -a:0x1:0x7f -d:0x1

i2c r -s:0x50 -a:0x1:0xee -d:0x1
i2c w -s:0x50 -a:0x1:0xee -d:0x1 00
PING 127.0.0.1 -n 1 >nul
i2c r -s:0x50 -a:0x1:0xef -d:0x1
i2c w -s:0x50 -a:0x1:0xef -d:0x1 00
PING 127.0.0.1 -n 1 >nul
i2c r -s:0x50 -a:0x1:0xee -d:0x2
```

- **Set Range 1 – File name: w238-239_to1.bat**
  - Contents:

```
cd C:\Program Files (x86)\Diolan\I2CBridge.x64\bin
i2c r -s:0x50 -a:0x1:0x7f -d:0x1
i2c w -s:0x50 -a:0x1:0x7f -d:0x1 3
i2c r -s:0x50 -a:0x1:0x7f -d:0x1
i2c r -s:0x50 -a:0x1:0xee -d:0x1i2c w -s:0x50 -a:0x1:0xee -d:0x1 11
PING 127.0.0.1 -n 1 >nul
i2c r -s:0x50 -a:0x1:0xef -d:0x1
i2c w -s:0x50 -a:0x1:0xef -d:0x1 11
PING 127.0.0.1 -n 1 >nul
i2c r -s:0x50 -a:0x1:0xee -d:0x2
```

Appendix 6: Allowable Spec and Measurement value margins.

Key sections of this MOI outline spec precise target measurement and calibration values. This table outlines acceptable upper and lower bounds on these measurements.

Parameter	Unit	Min	Nominal	Max	Margin	Window Size	MOI Step	Notes
Data Rate	Gb/s	25.7786	25.7812	25.7838	100ppm			Per Spec
1 UI	ps	38.7840	38.7879	38.7918				Per Spec
Mask Hit Ratio PRBS 31	-	4×10^{-5}	-	5×10^{-5}		1×10^{-5}		Mask Hits/Violations
							Step 5	
J2 PRBS 31	ps	7.00	7.37	7.74	5%	.74		Calculated
	UI	0.18	0.19	0.2		0.02	Step 3	Normative Spec
J9 PRBS 31	ps	12.53	13.19	13.85	5%	1.32		Calculated
	UI	0.32	0.34	0.36		0.03	Step 3	Normative Spec
DDPWS PRBS9	ps	4.05	4.27	4.48	5%	0.43		Calculated
	UI	0.1	0.11	0.12		0.01	Step 3	Normative Spec
Counter-Propagating NEXT	mV	686	700	700	2%	70	Step 4	Nominal per spec
Counter-Propagating FEXT	mV	441	450	450	2%	45	Step 1	Nominal per spec
Co-Propagating FEXT	mV	441	450	450	2%	45	Step 2	Nominal per spec

EDR limiting active cable input electrical specifications, Spec excerpts.

Table 87 EDR limiting active cable input electrical specifications

Symbol	Parameter	Specification value(s)	Unit	Conditions
X1, X2	eye mask parameter, time; see Figure 87 on page 277	0.11, 0.31	UI	At TP6a, at FDR and higher data rates Hit ratio=5x10^{-5}
Y1, Y2	eye mask parameter, voltage	95, 350	mV	
	Crosstalk signal Vpk-pk	+/- 20% (See Conditions)	mV	At TP6a. Co-propagating aggressors. Crosstalk signal Vpk-pk to match lane under test, to within +/- 20%.
	Crosstalk signal transition time, 20%-80%	13	ps	
	Crosstalk calibration signal Vpk-pk, each aggressor	450	mV	At TP7a. Counter-propagating aggressors. Apply during crosstalk calibration only[a]
	Crosstalk calibration signal transition time, 20%-80%	10	ps	

Symbol	Parameter	Max	Min	Unit	Conditions
	Single-ended input voltage	4	-0.3	V	At TP6a
V_{CM}	AC common mode input voltage tolerance (RMS)	20		mV	At TP6a
DDPWS	Data Dependent Pulse Width Shrinkage	0.11		UI	At TP6a
J2	J2 Jitter tolerance	0.19		UI	At TP6a, with TX CDR bypassed (i.e., disabled)
		0.44		UI	At TP6a, with TX CDR enabled
J9	J9 Jitter tolerance	0.34		UI	At TP6a, with TX CDR bypassed (i.e., disabled)
		0.69		UI	At TP6a, with TX CDR enabled
S_{DD11}	Differential input return loss	Eq. 5 on page 297		dB	At TP5a, 50 MHz to 26 GHz
S_{CC11}	Common mode input return loss	-2		dB	At TP5a, 200 MHz to 26 GHz
S_{DC11}	Common mode to differential reflection	Eq. 6 on page 297		dB	At TP5a, 50 MHz to 26 GHz

a. Please refer to CIWG Method of Implementation (MOI) document Active Time Domain Testing for detailed specification of testing methodology and parameters.

Table 88 EDR limiting active cable output electrical specifications

Symbol	Parameter	Specification value(s)	Unit	Conditions
X	eye mask parameter, time	0.30	UI	Hit ratio=5E-5 with 100 Ohm load at TP7a (Note [a])
Y1, Y2	Diff. unsigned output voltage range 0 (required) range 1 (optional) range 2 (optional)	50, 225 100, 350 150, 450	mV	
	Crosstalk signal Vpk-pk, each aggressor	700	mV	At TP6a. Counter-propagating aggressors.[b]
	Crosstalk signal transition time, 20%-80%	13	ps	Transition time measured at this PRBS9 test pattern transition: 111111111**10**000011...

Symbol	Parameter	Max	Min	Unit	Conditions
Vout	Single-ended output voltage	4.0	-0.3	V	Referred to Signal Ground; measured at TP7a
V_{CM}	AC common mode output voltage (RMS)	20		mV	at TP7a
	Termination mismatch	5		%	1 MHz; at TP7a
S_{DD22}	Differential output return loss	Eq. 5 on page 297		dB	At TP7a, 50 MHz to 26 GHz
S_{CC22}	Common mode output return loss	-2		dB	At TP7a, 200 MHz to 26 GHz
S_{DC22}	Common mode to differential reflection	Eq. 6 on page 297		dB	At TP7a, 50 MHz to 26 GHz
t_r, t_f	Output transition time		10	ps	20-80%, Transition time measured at these PRBS9 test pattern transitions: 111111111**10**0000**01**11101...
J2	J2 Jitter	0.44		UI	At TP7a
J9	J9 jitter	0.69		UI	At TP7a

a. Output range is set for QSFP+ interfaces using page 03, addresses 238 & 239; see Section 8.5.
For CXP interfaces, output range is set using Rx Addresses 62-67; see Section 8.7.2.
b. Please refer to CIWG Method of Implementation (MOI) document Active Time Domain Testing for detailed specification of testing methodology and parameters.

Appendix 8: Diagram at Active Optical Time Domain DUT Test Fixture

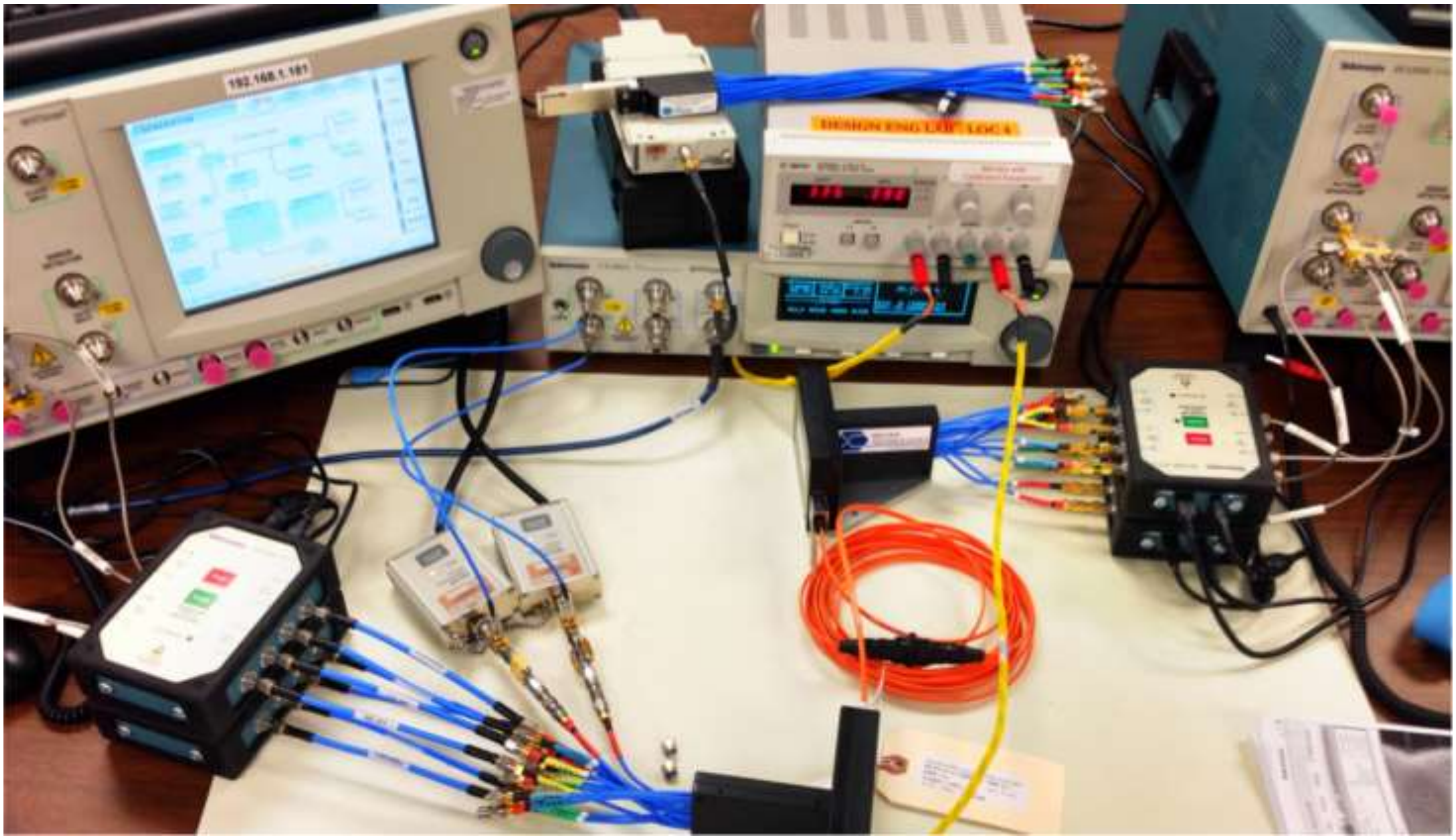


Figure 5: Picture of an AOC assembly being tested using Tektronix BSA286CL, LE320 test equipment

Appendix 9: High Precision Sampling Instrument Calibration.

1. Rationale for calibration close to Nyquist frequency

Traditional oscilloscope calibration is performed at low frequency or at DC, to avoid high frequency related uncertainties.

This calibration at low frequency has served the most applications well, but it is not particularly practical for high speed serial data (HSSD) and similar measurements, since typical HSSD signals contain no useful information at DC and at very low frequency and most of the signal's energy is below the Nyquist frequency (1/2 of the symbol rate, e.g. 12.89GHz for 25.78 GBd PAM2 or similar signal). Given that the amplitude response of the oscilloscope is typically guaranteed to be only within 3 dB of the nominal, the amplitudes measured by different instruments can be significantly different – theoretically as different as 6 dB apart. Additional variation due to not-perfectly-flat amplitude response of interconnects such as signal pick-offs, cables, DC blocks, etc. adds to the uncertainty of the calibration of the oscilloscope itself, which this procedure corrects.

It should be noted that both input channels of the sampling scope need to be independently corrected using this procedure.

Although in practical cases the amplitude readings on a HSSD signal by different oscilloscopes are closer that the worst case above, calibration difference has been observed to cause questioning of results at some standard events, notable at InfiniBand plug-fests.

To answer these concerns we propose to calibrate at higher frequency, in particular near the peak of the HSSD's spectral peak, removes many of these problems from the system.

2. Nyquist Calibration process

Calibration with a simple sinewave signal is easily performed in an operating system and this is what we recommend.

2.1. System diagram

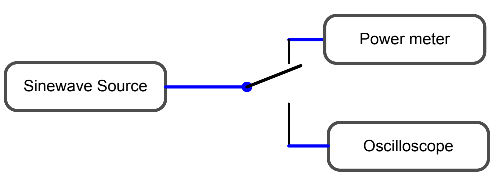


Figure 6 **Basic calibration setup**

In case that a appropriate Sinewave source is not available a similar setup using just a BERT or a Pattern Generator can be used (see figure 7). The Low Pass Filter should have frequency of about 1/8th to 1/16th of Symbol rate.

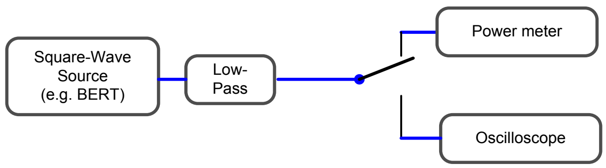


Figure 7 Calibration setup using a square-wave generator in place of a sine-wave generator

2.2. Comments on signal shape

The calibration signal is often not an exact sine wave; for example, some sine wave generators contain significant sub-harmonic content.

We recommend to use a true RMS power meter for the power meter measurement, and a oscilloscope's RMS measurement for the measurement on oscilloscope. This way the impurity of the sinewave is first-order irrelevant.

3. Calibration Procedure

3.1. List of equipment

1. Signal Source – e.g. a BERTScope generating a 1100 ~ 6.45GHz Clock, or a CW Synthesizer generating a leveled sinewave at 6.45GHz.
2. Lowpass For 25 to 32 Gb/s select e.g. 7.5 GHz lowpass filter (PN: Picosecond 5933-110-7.46GHz) which is used in this overview.
3. Power Meter: Tektronix USB based PSM5410
4. 2 male to male 2.92mm interconnects.

3.2. Calibration Procedure

1. Set the BERT to generate at 1100 (2 unit interval consecutive run length) data pattern, at 25.78125Gbps with an amplitude of 500mV. (refer to figure 8.)

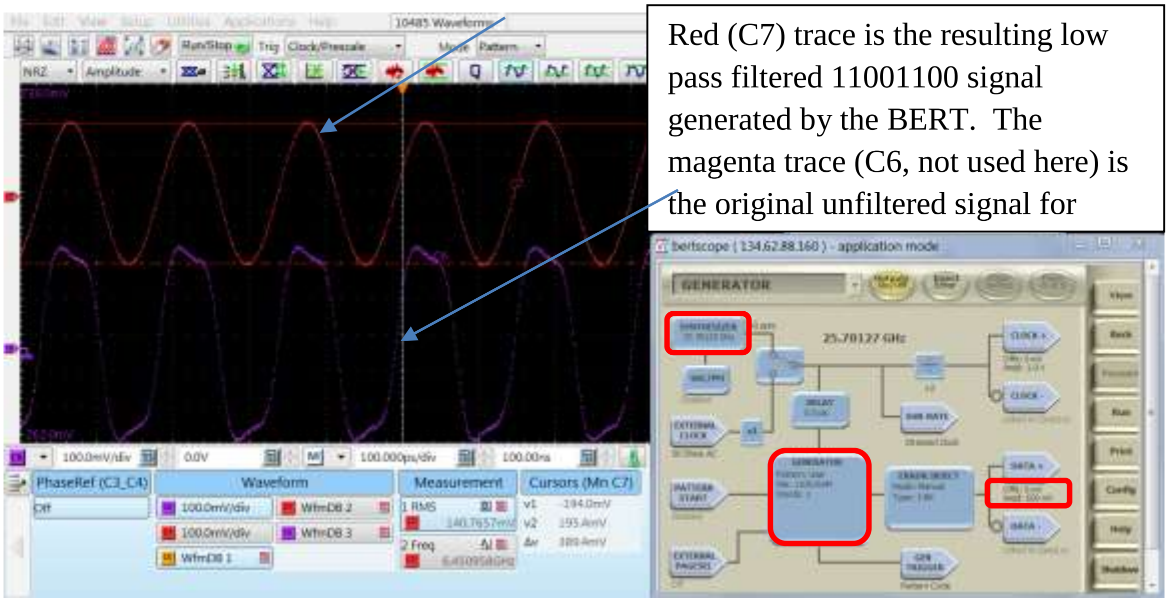


Figure 8 (BERT pattern setup, and low pass filtered sine wave)

2. Attach the 7.5 GHz Low Pass Filter to the D+ leg of the BERT (refer to Figure 9.) and inspect the resulting sinewave on the Sampling Scope, ensuring it's relatively clean (refer to Figure 8.).

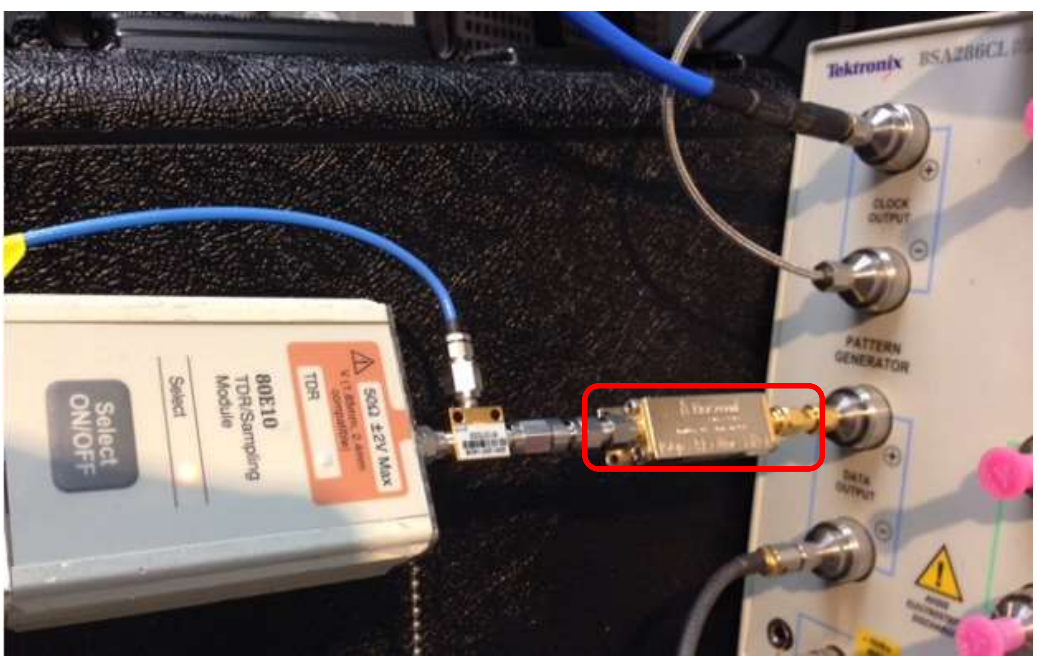


Figure 9 (7.5GHz Low pass filter connected to BERT D+ output)

3. Select the measurement: Setup->Measurement →Vertical → AC RMS Amplitude[1]; (refer to Figure 10.) Select Pulse for measurement type; uncheck 'WfmDB' for the measurement method

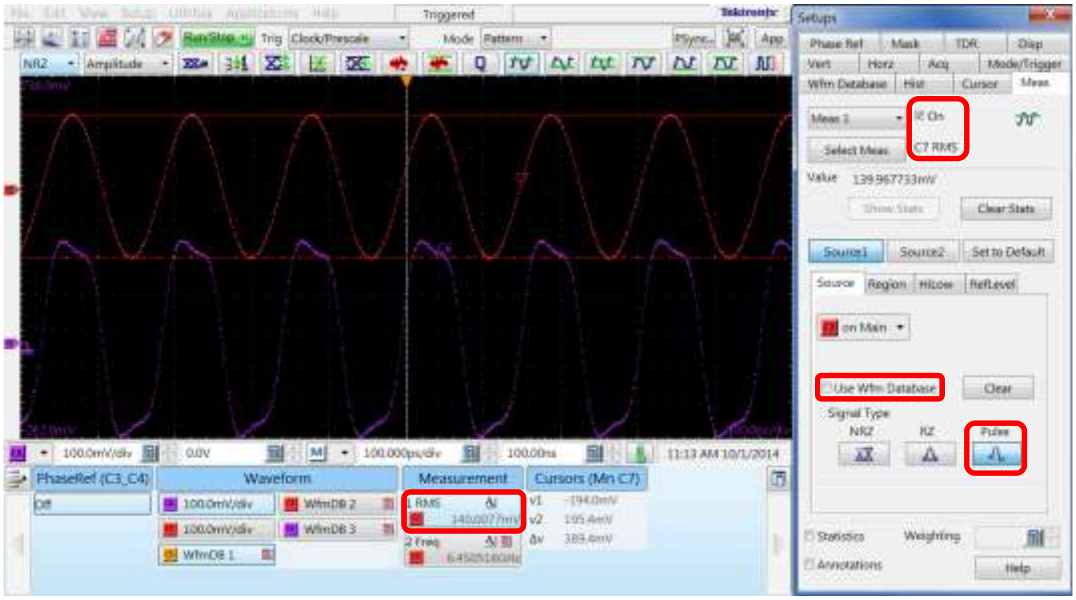


Figure 10 (RMS Amplitude measurement setup)

4. Make note of the un-compensated RMS signal level and record it as $\mathbf{V_{osc}}$ which in this illustration (Figure 10) is 140.0mV.

5. Remove the sampling head and Clock Recovery pickoff arrangement and attach the power meter, to the output of the 7.5 GHz Low Pass (refer to Figure 11.).

[1] This is assuming that either the sinewave source has no DC signal and/or a DC block is used. If the power source has a DC component then place a DC block at its output.

Figure 11 (Power Meter attached to 7.5GHz low pass filter output)

6. Configure the Power meter to filter out higher order harmonics beyond the fundamental of interest which in this case is 6.5GHz as shown in Figure 12. Set the readings from dBm to mV, for a CW signal.

Figure 12 (Power Meter configuration and RMS reading)

7. Make note of the Power meter RMS reading un-compensated RMS signal level and record it as $\mathbf{V_{pm}}$ which in this illustration (Figure 12) is 171.013mV.

8. Calculate correction factor: cf := V_{pm}/V_{osc} In this case cf is 171.013/140.0 = 1.22

9. On the oscilloscope, open the panel Setup →Vertical (select the appropriate Channel C7 in this case)

10. Enter the correction factor cf into the oscilloscope Setup->Vertical External Attenuation field, Linear (not 'dB') (Figure 13) and verify correlation error is less than 1% in error.

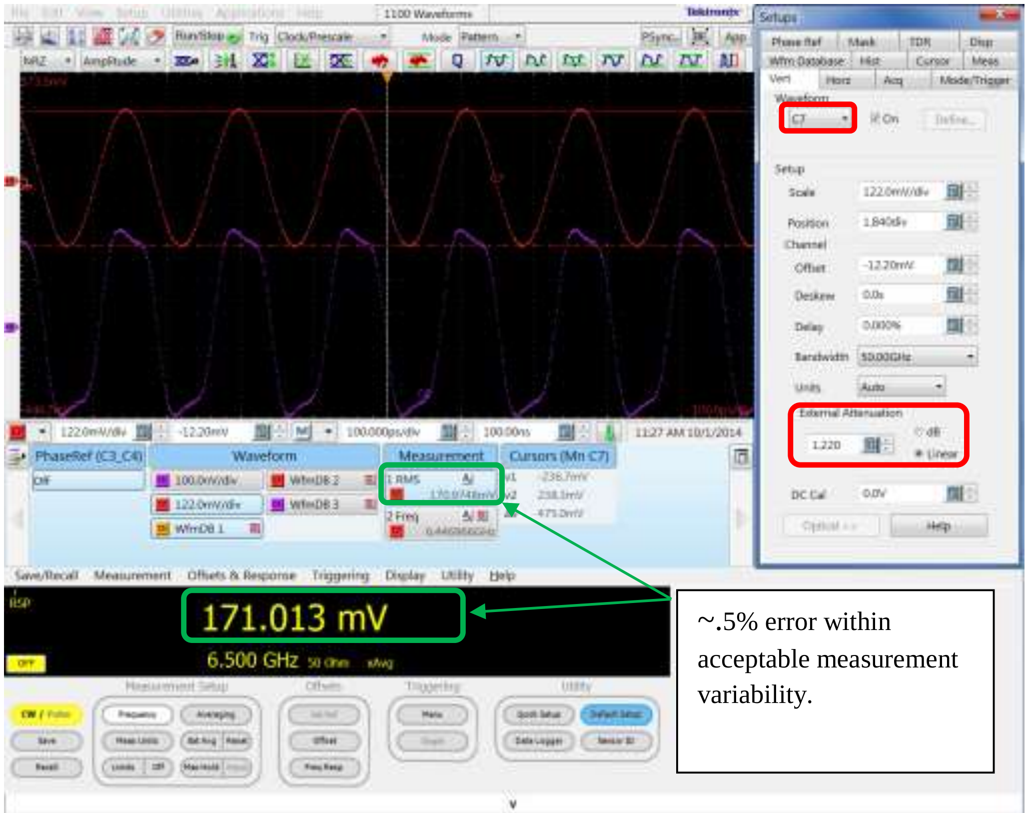


Figure 13 (Final Corrected/Calibrated Sampling Head + Interconnect)

11. Repeat this process on the other differential sampling input.

Note: If the other single ended leg has a signal attenuation which is different from the other leg by more than 5%, revisit your setup and change pick-off components as this can result in significant DC common mode error and effect jitter calibration (DCD will be higher.

4. Conclusion

This calibration procedure effectively compensates to frequency dependent losses attributed to signal pickoff and connection assemblies, which are considerable at 25.78Gbps.